intel® Technical Advisory

TA-608-2

5200 NE Elam Young Parkway
Hillsboro, OR 97124

February 10, 2003

SHG2 Processor #1 Error 8180 during POST and Watchdog Timer/FRB2 Events in System Event Log

Products Affected

Product Code	PBA number
SHG2	A77226-506 and previous revisions
BHG2BB	A77226-506 and previous revisions

Description

When the SHG2 server board is used in a uni-processor configuration, and installed in the SC5200 base chassis (product code KHD3BASE450), spontaneous system reboots may occur approximately six minutes after POST, whether or not the system has booted to an operating system. Following the spontaneous system reboot, the following error will be displayed on the next POST boot:

> Processor #1 Error 8180
>
> Press <F1> to continue, <F2> to Setup

The system event log (SEL) will contain a watchdog timer hard reset event, followed by an FRB2/Hang in POST failure event.

This issue has the potential of appearing on any SHG2 server board with PBA number A77226-506 and previous revisions, when the SHG2 server board is used in a uni-processor configuration in either the SC5200 base chassis with Intel's standard sensor data record (SDR) file for this configuration, or in a reference chassis if the SDR for the secondary processor fan is loaded by the BMC firmware. Using Intel's supplied FRU/SDR package, this could occur if the user erroneously answers "yes" to the "Is there a fan sink on processor 2" question.

Root Cause

The root cause of this issue is an erratum in the SHG2 baseboard management controller (BMC) firmware code that polls the processor fans. In cases where the BMC expects a processor fan to be present, based on the system's sensor data record (SDR) configuration, and finds it to be missing, a 10-second delay occurs before the BMC resumes normal operation. The end user may observe this as a noticeable delay after engaging certain server management functions; for example, a system reset may occur several seconds after the user presses the reset button. The 10-second delay also interferes with BIOS to BMC interactions, sometimes preventing the system BIOS from disabling the six-minute FRB2 watchdog timer. In such cases, the BMC will reset the system after the watchdog timer expires, even if the system has already booted to an operating system.

This erratum was exposed by a mismatch between the SDR configuration and the actual physical processor fan configuration, which occurs in SHG2 uni-processor configurations in the SC5200 base chassis. The current SDR file for this system configuration will install SDRs for both processor fans, regardless of the actual number of installed

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processors and processor fans. In a uni-processor configuration, this will expose the BMC firmware erratum, because the secondary processor fan will not be present even though the SDR has been installed. This erratum does not affect dual-processor configurations as long as both processor fans are installed.

Corrective Action / Resolution

A fix for this erratum has been included in SHG2 BMC firmware version 20 and FRU/SDR version 5.0.8. The new BMC firmware and FRU/SDR versions are being incorporated into the SHG2 server board on December 6, 2002 by an engineering change notification (ECO), described in PCN 102873-01. BMC firmware version 20 and FRU/SDR version 5.0.8 are also available for download at http://support.intel.com. SHG2 server boards with PBA number A77226-507 and later revisions will include BMC firmware and FRU/SDR versions that incorporate a fix for this issue.

Intel recommends that customers with SHG2 server boards with PBA numbers A77226-506 and previous revisions update to BMC firmware version 20 and FRU/SDR file version 5.0.8 (or later versions), if the SHG2 server board is being used in a uni-processor configuration in the SC5200 base chassis, in order to prevent this issue from occurring.

On SHG2 server boards that have previously experienced this issue, it is necessary to perform the following steps after updating the server board to BMC firmware version 20 and FRU/SDR file version 5.0.8 (or later versions) in order to clear the error from continuing to be displayed during POST:

1. During POST, enter BIOS Setup by pressing <F2>
2. Set the Main → Processor Settings → Processor Retest option to "Yes"
3. Press <F10> and select "Yes" to Save configuration changes and exit now
4. On system reboot, the processor POST error will no longer be displayed

Please contact your Intel Sales Representative if you require more specific information about this issue.

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