Intel® Server Board SE7501BR2

Technical Product Specification

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Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
05/2002	0.7	First release
11/2002	0.97	Second release
12/2002	1.0	Corrected grammatical errors and modified for first public release
06/2003	1.1	Updated to reflect HostRAID*, One-Boot Update Utility and Intel Server Chassis fan integration.
06/2004	1.2	Corrected Absolute Maximum Ratings, added more Extended POST Error Messages and Codes.

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1. Introduction

The SE7501BR2 Technical Product Specification (TPS) provides a high level technical description for the Intel® SE7501BR2 Server Board. It details the architecture and feature set for all functional sub-systems that make up the server board.

This document is sub-divided into the following main categories:

Chapter 2: Server Board Overview

Chapter 3: Functional Architecture

Chapter 4: Configuration and Initialization

Chapter 5: Clock Generation and Distribution

Chapter 6: PCI I/O Subsystem

Chapter 7: Server Management

Chapter 8: System BIOS

Chapter 9: BIOS Error Reporting and Handling

Chapter 10: Connectors and Headers

Chapter 11: Configuration Jumpers

Chapter 12: General Specifications

Chapter 13: Product Regulatory Compliance

Chapter 14: Mechanical Specifications

1.1 Audience

This document is intended for technical personnel who want a technical overview of the SE7501BR2 server board. Familiarity with personal computers, Intel server architecture and the Peripheral Component Interconnect (PCI) local bus architecture is assumed.

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2. Server Board Overview

The SE7501BR2 server board is a monolithic printed circuit board with features that were designed to support the general-purpose server market. The architecture is based around the Intel® E7501 chipset and is capable of supporting one or two Intel® Xeon™ processors with 512KB L2 cache and up to 8 GB of DDR266 registered memory.

2.1 SE7501BR2 Feature Set

The SE7501BR2 server boards support the following feature set:

- Dual Intel® Xeon™ processors with 512KB L2 Cache in the INT3-mPGA or FC-mPGA2P package using the Socket 604.
- 533 MHz Front Side Bus backwards compatible to 400 MHz
- Intel® server chipset
  - Intel® E7501 Memory Controller Hub (MCH)
  - Intel® 82870P2 PCI/PCI-X 64-bit Hub2 (P64H2) PCI/PCI-X Controller Hub
  - Intel® 82801CA I/O Controller Hub3 (ICH3-S) I/O Controller Hub
- Support for four DDR266 compliant registered ECC DDR DIMMs providing up to 8 GB of memory
- Three separate and independent PCI buses:
  - Segment A: 32-bit, 33 MHz, 5 V, Full length PCI (P32-A) supporting the following configuration:
    - Two slots: 32-bit/33MHz PCI slots (PCI Slot 5 and Slot 6)
    - 2D/3D graphics controller: ATI Rage* XL Video Controller with 8 MB of SDRAM
    - Intel® 10/100/1000 82540EM Gigabit Ethernet Controller (NIC2)
    - Intel® 10/100 82550PM Fast Ethernet Controller (NIC1)[1]
  - Segment B: 64-bit, 100/66 MHz, 3.3 V, Full length PCI (P64-B) supporting the following configuration:
    - Two slots: 64-bit/100MHz PCI-X slots (PCI-X Slot 3 and Slot 4)
    - Single-channel Adaptec* AIC-7901 wide Ultra-320 SCSI controller[2]
    - Zero Channel RAID (ZCR) support via slot 4. Also known as modular RAID on motherboard (M-ROMB)[3]
  - Segment C: 64-bit, 133/100/66 MHz, 3.3 V, Full-length PCI (P64-C) supporting the following configuration:
    - Two slots: 64-bit/100MHz[4] PCI-X slots (PCI-X Slot 1 and PCI-X Slot 2)
- LPC (Low Pin Count) bus segment with two embedded devices:

[1] NIC1 is the designated Server Management NIC.

[2] Single Ended Mode not supported.

[3] Some RAID controllers may only operate at PCI 66 MHz.

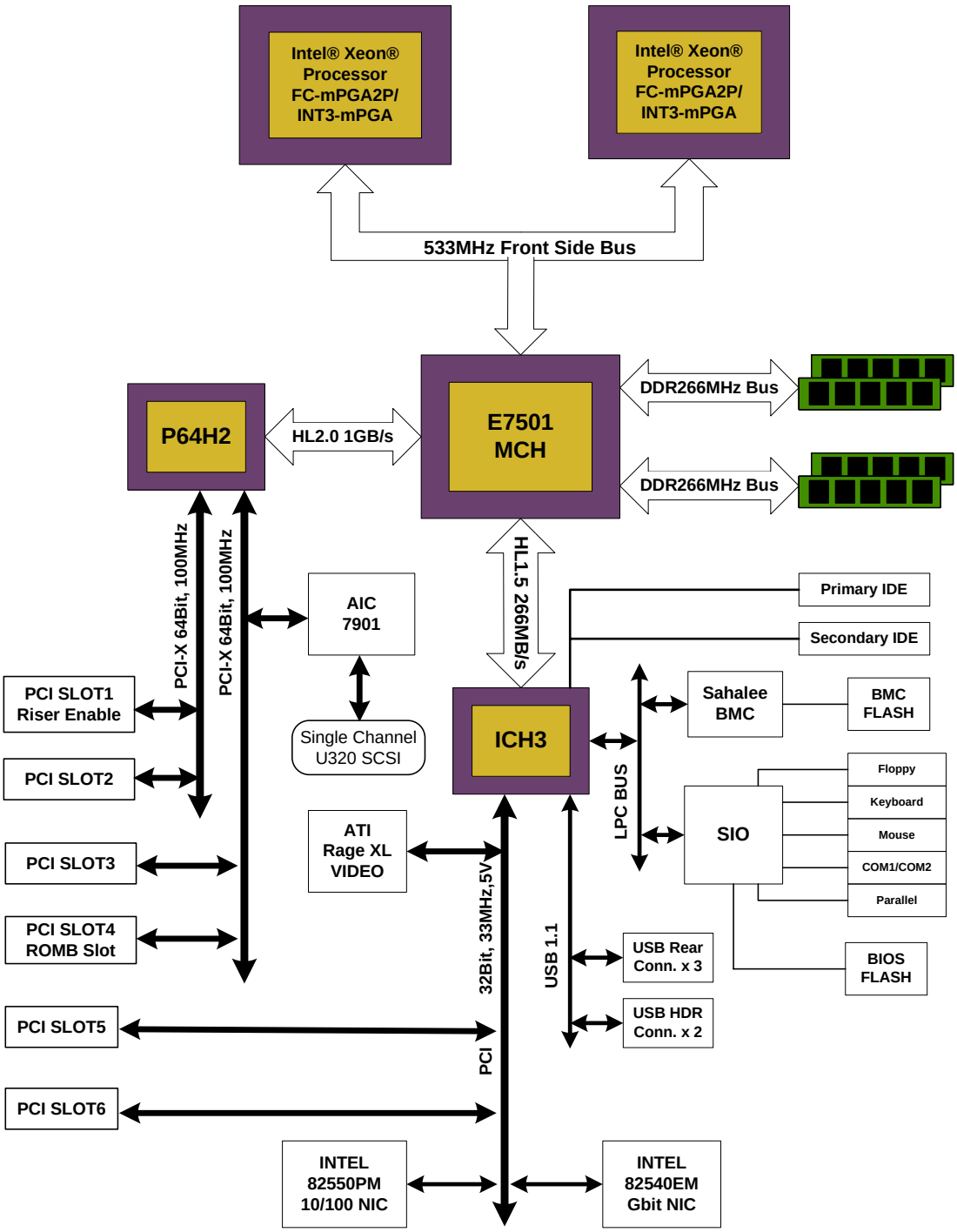
[4] The BIOS is responsible for setting the mode (PCI or PCI-X) and bus speed for the two segments provided by the P64H2. The actual bus mode/speed will be determined by the least capable card installed on that bus. BIOS will program the bus at 133MHz when one slot is populated, and at 100MHz when two slots are populated.

  - Baseboard Management Controller (BMC) providing monitoring, alerting, and logging of critical system information obtained from embedded sensors on server board.
  - Super I/O controller chip providing all PC-compatible I/O (floppy, serial, parallel, keyboard, mouse).
- X-Bus segment with one embedded device:
  - Flash ROM device for system BIOS: Intel® 32 megabit 28F320C3 Flash ROM.
- Three external Universal Serial Bus (USB) ports with an additional internal header providing two optional USB ports[5] for front panel support.
- Two serial ports: One external serial port (Serial A) on the rear I/O area of the board and one internal header is also available providing an optional port (Serial B[6]).
- Two IDE connectors, supporting up to four ATA-100 compatible devices.
- Six multi-speed system fan headers (two for redundancy) and two single speed CPU fan headers.
- Multiple server management headers providing on-board interconnects to the board's server management features.
- SSI-EEB3.0 compliant board form factor, the board size is 12 inch by 13 inch.
- SSI-compliant connectors for SSI interface support the 34-pin front panel, floppy, ATA-100 and power connectors.

The figure below shows the functional blocks of the server board and the plug-in modules that it supports.

[5] Only one port may be routed to the chassis front panel when integrating into the Intel® SC5200 Server Chassis.
[6] Serial B is the designated Server Management serial port.

Figure 1. SE7501BR2 Server Board Block Diagram



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3. Functional Architecture

This chapter provides a high-level description of the functionality distributed between the architectural blocks of the SE7501BR2 server board.

3.1 Processor and Memory Subsystem

The E7501 chipset provides a 36-bit address, 64-bit data processor host bus interface, operating at 533MHz in the AGTL+ signaling environment. The MCH component of the chipset provides an integrated memory controller, an 8-bit Hub Interface, and three 16-bit hub interfaces.

The Hub Interface provides the interface to two 64-bit, 133MHz, Rev 1.0 compliant PCI-X buses via the P64H2. The SE7501BR2 server board directly supports up to 8 GB of registered ECC memory, using four DDR266 compliant ECC DIMMs. The ECC implementation in the MCH can detect and correct single-bit errors, detect multiple-bit errors, and it supports the Intel® x4 Single Device Data Correction feature with x4 DIMMs.

3.1.1 Processor Support

The SE7501BR2 server board supports one or two Intel® Xeon™ processors using a FC-mPGA2P or INT3-mPGA package via Socket 604 on the board. The server board will support the Intel® Xeon™ processor with 512KB L2 Cache. When two processors are installed, all processors must be of identical revision, core voltage, and bus/core speed. When only one processor is installed, it should be in the socket labeled CPU1. The other socket is kept empty. The support circuitry on the server board consists of the following:

- Dual Socket 604 INT3-mPGA & FC-mPGA2P CPU sockets supporting 400 & 533 MHz FSB.
- Processor host bus AGTL+ support circuitry.

Table 1. SE7501BR2 Supported Processor Matrix

Processor Family	*Package Type*	*FSB*	*Frequency*	*L2 Cache Size*	*L3 Cache Size*
Intel® Xeon™ 512KB L2 Cache	INT3-mPGA	400MHz	All	512KB	
Intel® Xeon™ 512KB L2 Cache	FC-mPGA2P	533MHz	All	512KB	
Intel® Xeon™ 512KB L2 Cache 1M L3 Cache	FC-mPGA2P	533MHz	All	512KB	1MB

Notes:

- Processors must be populated in the sequential order. That is, processor socket #1 must be populated before processor socket #2.

- SE7501BR2 is designed to provide up to 65 Amps per processors. Processors with higher current requirements are not supported.

In addition to the circuitry described above, the processor subsystem contains the following:

- Processor module presence detection logic
- Server management registers and sensors
- Reset configuration logic
- APIC bus

3.1.1.1 Processor VRM

The SE7501BR2 baseboard has a single, integrated VRM (Voltage Regulator Module) to support two processors. It is compliant with the VRM 9.1 specification and provides a maximum of *130* AMPs, which is capable of supporting current supported processors as well as processors that do not exceed the 65 Amp limit.

The board hardware and BMC will read the processor VID (voltage identification) bits for each processor before turning on the VRM. If the VIDs of the two processors are not identical, then the BMC will not turn on the VRM and a beep code is generated.

3.1.1.2 Reset Configuration Logic

The BIOS determines the processor stepping, cache size, etc through the CPUID instruction. The requirements are that all processors in the system must operate at the same frequency, have the same cache sizes, and same VID. No mixing of product families is supported.

The processor information is read at every system power-on and the speed is set to the fixed processor speed.

Note: No manual processor speed setting options exist either in the form of a BIOS setup option or jumpers.

3.1.1.3 Processor Module Presence Detection

Logic is provided on the baseboard to detect the presence and identity of installed processors. The PMC checks the logic and will not turn on the system DC power unless the VIDs of both the processors match in a DP configuration.

3.1.1.4 Interrupts and APIC

Interrupt generation and notification to the processors is done by the APICs in the ICH3-S and the P64H2 using messages on the front side bus.

3.1.1.5 Server Management Registers and Sensors

The baseboard management controller (BMC) manages registers and sensors associated with the processor / memory subsystem.

3.1.2 Memory Subsystem

The SE7501BR2 server board provides four DIMM slots (two contiguous slots per memory bank) for a maximum memory capacity of 8 GB. The DIMM organization is x72, which includes eight ECC check bits. The memory interface runs at 266MHz when configured with 533MHz FSB processors, and it runs at 200MHz with 400MHz FSB processors. The memory controller supports memory scrubbing, single-bit error correction, multiple-bit error detection, and Intel(r) x4 Single Device Data Correction support with x4 DIMMs. Memory can be implemented with either single sided (one row) or double-sided (two row) DIMMs.

The figure below provides a block diagram of the memory sub-system implemented on the SE7501BR2 server board.

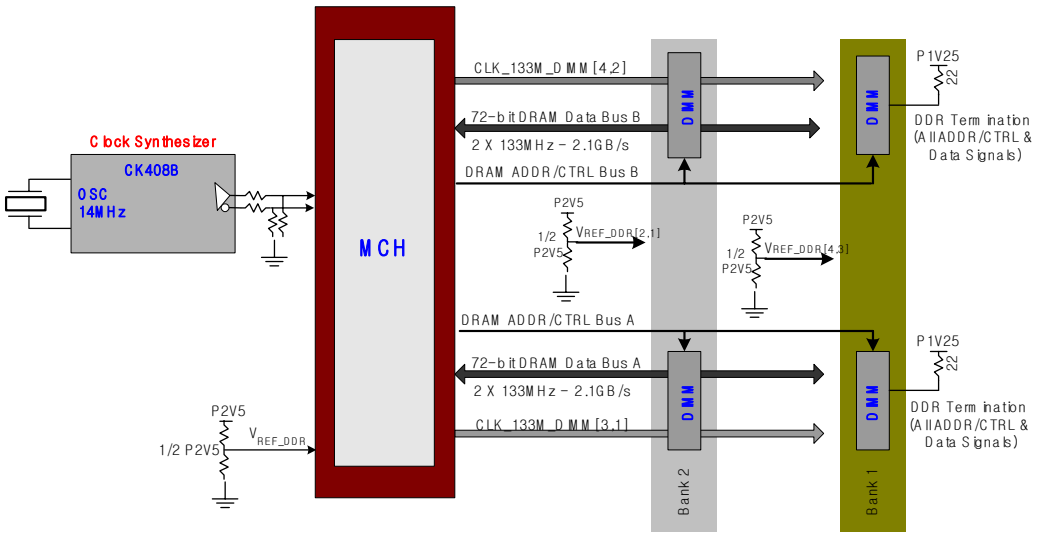

Figure 2. Memory Sub-system Block Diagram

3.1.2.1 Memory DIMM Support

The SE7501BR2 server board supports DDR266 compliant registered ECC DIMMs. Only DIMMs tested and qualified by Intel or a designated memory test vendor are supported on the SE7501BR2 server board. A list of qualified DIMMs will be made available. Note that all DIMMs are supported by design, but only fully qualified DIMMs will be supported.

The minimum supported DIMM size is 128 MB. Therefore, the minimum main memory configuration is 2 x 128 MB or 256 MB. The largest size DIMM supported is a 2 GB stacked registered DDR266 or DDR266 ECC DIMM based on 512 megabit technology.

- Only registered DDR266 compliant, ECC, DDR memory DIMMs will be supported
- Using ECC, single-bit errors will be corrected and multiple-bit error will be detected
- The SE7501BR2 supports the Intel® x4 Single Device Data Correction feature with x4 DIMMs
- The maximum memory capacity is 8 GB

- The minimum memory capacity is 256 MB

3.1.2.2 Memory Configuration

Memory interface between the MCH and DIMMs is 144 bits wide. This requires that two DIMMs be populated per bank in order for the system to operate. At least one bank has to be populated in order for the system to boot. If additional banks have less than two DIMMs, the memory for that bank(s) will not be available to the system.

There are two banks of DIMMs, labeled Bank1 and Bank2. Bank1 contains DIMM locations DIMM1A and DIMM1B and Bank2 contains DIMM2A and DIMM2B. DIMM socket identifiers are marked with silk screen next to each DIMM socket on the baseboard. The sockets associated with any given bank are located next to each other.

The baseboard's signal integrity is optimized when memory banks are populated in order. Therefore, DIMM Bank1 must be populated before Bank2.

DIMM and memory configurations must adhere to the following:

- DDR266 DDR registered DIMM modules
- DIMM organization: x72 ECC
- Pin count: 184
- DIMM capacity: 128 MB, 256 MB, 512 MB, 1 GB, 2 GB
- Serial PD: JEDEC Rev 2.0
- Voltage options: 2.5 V (VDD/VDDQ)
- Interface: SSTL2
- Two DIMMs must be populated in a bank for a 144-bit wide memory data path
- One or two memory banks may be populated

Table 2. Memory Bank Labels

Memory DIMM	Bank	Row
J8D22 (DIMM 1A), J8D15 (DIMM 1B)	1	0, 1
J8D7 (DIMM 2A), J8D1 (DIMM 2B)	2	2, 3

Note: Memory must be installed in pairs; DIMM Bank1 must be populated before DIMM Bank2. Memory within a DIMM bank must be identical; between banks only the DIMM size may be different.

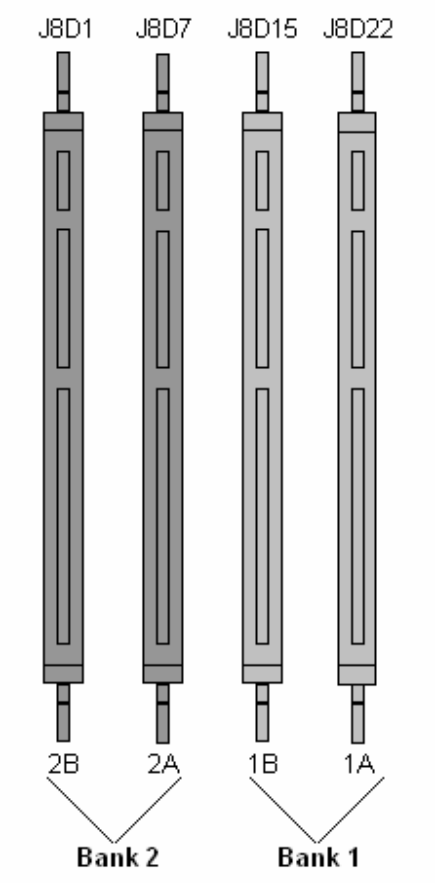

Figure 3. Memory Bank Label Definition

3.1.2.3 I²C Bus

An I²C bus connects the BMC, ICH3-S, MCH, P64H2 and the four DIMM slots. This bus is used by the system BIOS to retrieve DIMM information needed to program the MCH memory registers which are required to boot the system.

The following table provides the I²C addresses for each DIMM slot.

Table 3. I²C Addresses for Memory Module SMB

Device	Address
DIMM 1A	0xA2
DIMM 1B	0XAA
DIMM 2A	0XA0
DIMM 2B	0xA8

3.2 Intel® E7501 Chipset

The SE7501BR2 server board is designed around the Intel® E7501 chipset. The chipset provides an integrated I/O bridge and memory controller, and a flexible I/O subsystem core (PCI-X). This is targeted for multiprocessor systems and standard high-volume servers. The Intel® E7501 chipset consists of three components:

- **MCH: Memory Control Hub North Bridge.** The MCH North Bridge accepts access requests from the host (processor) bus and directs those accesses to memory or to one of the PCI buses. The MCH monitors the host bus, examining addresses for each request. Accesses may be directed to a memory request queue for subsequent forwarding to the memory subsystem, or to an outbound request queue for subsequent forwarding to one of the PCI buses. The MCH also accepts inbound requests from the P64H2 and the ICH3. The MCH is responsible for generating the appropriate controls to control data transfer to and from memory.
- **P64H2: PCI-X 64bit Hub 2.0 I/O Bridge.** The P64H2 provides the interface for 64-bit, 133MHz Rev. 1.0 compliant PCI-X buses. The P64H2 is both master and target on both PCI-X buses.
- **ICH3-S: IO Control Hub South Bridge.** The ICH3-S controller has several components. It provides the interface for a 32-bit, 33-MHz Rev. 2.2-compliant PCI bus. The ICH3-S can be both a master and a target on that PCI bus. The ICH3-S also includes a USB controller and an IDE controller. The ICH3-S is responsible for much of the power management functions, with ACPI control registers built in. Finally, the ICH3-S also provides a number of GPIO pins and has the LPC bus to support low speed legacy I/O.

The MCH, P64H2, and ICH3-S chips provide the pathway between processor and I/O systems. The MCH is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to one of the PCI buses or legacy I/O locations. If the cycle is directed to one of the 64-bit PCI segments, the MCH communicates with the P64H2 through a private interface called the Hub Interface (HI) 2.0 bus. The P64H2 translates the HI 2.0 bus operation to a 64-bit PCI Rev. 2.2-compliant signaling environment operating from 133MHz to 33 MHz. The HI 2.0 bus is 16-bit wide and operates at 66 MHz running 8x data transfers, providing over 1 GB per second of bandwidth. If the cycle is directed to the ICH3-S, the cycle is output on the MCH's HI 1.5 bus. The HI 1.5 bus is 8-bit wide and operates at 66 MHz running 4x data transfers, providing 266MB per second of bandwidth.

All I/O for the SE7501BR2, including PCI and PC-compatible, is directed through the MCH and then through either the P64H2 or the ICH3 provided PCI buses.

- The ICH3-S provides a 32-bit/33-MHz PCI bus hereafter called P32-A.
- The P64H2 provides two independent 64-bit PCI-X buses hereafter called P64-B, and P64-C. The mode/speed of each bus is set by BIOS during startup and is determined by the least capable card installed on each bus. The mode/speed of P64-C is set by BIOS as PCI-X 64-bit/133MHz when only one slot is populated, and as PCI-X 64-bit/100MHz when two slots are populated. The mode/speed of P64-B is set by BIOS as PCI-X 64-bit/100MHz with one or two slots populated as the integrated SCSI controller resides on this bus.

This independent bus structure allows all three PCI buses to operate.

3.2.1 Memory Controller Hub (MCH)

The E7501 MCH North Bridge (MCH) is a 1005 ball FC-BGA device and uses the proven components of previous generations. In addition, the MCH incorporates a Hub Interface (HI) 2.0. The HI 2.0 interface enables the MCH to directly interface with the P64H2. The MCH also increases the main memory interface bandwidth and maximum memory configuration with a 144-bit wide memory interface.

The MCH integrates three main functions:

- An integrated high performance main memory subsystem
- An HI 2.0 bus interface that provides a high-performance data flow path between the host bus and the I/O subsystem
- A HI 1.5 bus which provides an interface to the ICH3-S (South Bridge).

Other features provided by the MCH include the following:

- Full support of ECC on the memory bus
- Full support of Intel® x4 Single Device Data Correction on the memory interface with x4 DIMMs
- Twelve deep in-order queue
- Full support of registered DDR266 ECC DIMMs
- Support for 8 GB of DDR memory
- Memory scrubbing

3.2.1.1 MCH - Memory Architecture Overview

On the SE7501BR2, the MCH supports a 144-bit Memory sub-system that can support a maximum of 8 GB when using 2.0 GB DDR266 compliant registered stacked DIMMs.

The memory interface runs at 266 MHz. It uses fifteen address lines (BA[1:0] and MA[12:0]) and supports 128Mb, 256Mb, 512Mb DRAM densities. The DDR DIMM interface supports memory scrubbing, single-bit error correction, multiple bit error detection, and Intel® x4 Single Device Data Correction with x4 DIMMs.

3.2.1.2 DDR Configurations

The DDR interface supports up to 8 GB of main memory and supports single- and double-density DIMMs. The SE7501BR2 will only support registered DDR266 compliant DIMMs that have cache latencies (CL) of 2.0 and 2.5. The following table shows the DDR DIMM technology supported.

Table 4. Supported DDR DIMM Technologies

DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	# SDRAM Devices/rows/Banks	# Address bits rows/Banks/column
128MB	16M x 72	64Mbit	16M x 4	18/1/4	12/2/10
128MB	16M x 72	64Mbit	8M x 8	18/2/4	12/2/9
128MB	16M x 72	128Mbit	16M x 8	9/1/4	12/2/10

256MB	32M x 72	64Mbit	16M x 4	36/2/4	12/2/10
256MB	32M x 72	128Mbit	32M x 4	18/1/4	12/2/11
256MB	32M x 72	128Mbit	16M x 8	18/2/4	12/2/10
256MB	32M x 72	256Mbit	32M x 8	9/1/4	13/2/10
512MB	64M x 72	128Mbit	32M x 4	36/2/4	12/2/11
512MB	64M x 72	256Mbit	64M x 4	18/1/4	13/2/11
512MB	64M x 72	256Mbit	32M x 8	18/2/4	13/2/10
512MB	64M x 72	512Mbit	64M x 8	9/1/4	13/2/11
1GB	128M x 72	256Mbit	64M x 4	36/2/4	13/2/11
1GB	128M x 72	512Mbit	64M x 8	18/2/4	13/2/11
1GB	128M x 72	512Mbit	128M x 4	18/1/4	13/2/12
2GB	256M x 72	512Mbit	128M x 4	36/2/4	13/2/12

3.2.2 P64H2 I/O Bridge

The P64H2 is a 567-ball FC-BGA device and offers an integrated I/O bridge that provides a high-performance data flow path between the HI 2.0 and the 64-bit I/O subsystem. This subsystem supports two peer 64-bit PCI-X segments: P64-B and P64-C. Because it has two PCI interfaces, the P64H2 can provide large and efficient I/O configurations. The P64H2 functions as the bridge between the HI 2.0 and the two 64-bit PCI-X I/O segments. The HI 2.0 interface can support up to 1 GB/s of data bandwidth.

Note: The system BIOS is responsible for setting the mode (PCI or PCI-X) and bus speed for the two segments provided by the P64H2. The actual bus mode/speed will be determined by the least capable card installed on that bus. The mode/speed of P64-C is set by BIOS as PCI-X 64-bit/133MHz when only one slot is populated, and as PCI-X 64-bit/100MHz when two slots are populated. The mode/speed of P64-B is set by BIOS as PCI-X 64-bit/100MHz with one or two slots populated as the integrated SCSI controller resides on this bus.

3.2.2.1 PCI Bus P64-B I/O Subsystem

P64-B supports the following embedded devices and connectors:

- Two 64-bit 100/66 MHz, 3.3V keyed PCI-X slots (PCI-X slots 3 and 4)
- One Adaptec* AIC-7901 single-channel Ultra-320 SCSI controller
- PCI slot 4 has support for a Zero Channel RAID (ZCR) card (aka M-ROMB) which utilizes the SCSI features of the onboard SCSI controller
- Full length PCI card support.

3.2.2.2 PCI Bus P64-C I/O Subsystem

P64-C supports the following connectors:

- Two 64-bit 133/100/66 MHz 3.3V keyed PCI-X slots (PCI-X slots 1 and Slot 2)
- Full length PCI card support

3.2.3 ICH3-S I/O Controller Hub

The ICH3-S I/O Controller Hub is a multi-function device, housed in a 421-pin BGA device, providing a HI 1.5 to PCI bridge, a PCI IDE interface, a PCI USB controller, and a power management controller. Each function within the ICH3-S has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

On the SE7501BR2 server board, the primary role of the ICH3-S is to provide the gateway to all PC-compatible I/O devices and features. The SE7501BR2 uses the following ICH3-S features:

- PCI bus interface
- LPC bus interface
- IDE interface, with Ultra DMA 100 capability
- Universal Serial Bus (USB) interface
- PC-compatible timer/counter and DMA controllers
- APIC and 8259 interrupt controller
- Power management
- General Purpose I/O
- System RTC

The following sections describe how each supported feature is used on the SE7501BR2.

3.2.3.1 PCI Bus P32-A I/O Subsystem

The ICH3-S provides a legacy 32-bit PCI subsystem and acts as the central resource on this PCI interface.

P32-A supports the following embedded devices and connectors:

- Two 32-bit/33MHz, 5V keyed PCI slots (PCI Slot 1 and 2)
- One Intel® 82550PM 10/100 Fast Ethernet PCI network interface controller
- One Intel® 82540EM 10/100/1000 Gigabit Ethernet PCI network interface controller
- An ATI Rage* XL video controller with 3D/2D graphics accelerator

3.2.3.2 PCI Bus Master IDE Interface

The ICH3-S acts as a PCI-based Ultra DMA/100 IDE controller that supports programmed I/O transfers and bus master IDE transfers. The ICH3-S supports two IDE channels, supporting two drives each (drives 0 and 1) through two 40-pin (2x20) IDE connectors. The SE7501BR2 IDE interface supports Ultra DMA/100 Synchronous DMA Mode transfers on each channel.

3.2.3.3 USB Interface

The ICH3-S contains three USB 1.1 compliant controllers and six USB ports. The USB controller moves data between main memory and the USB connectors. All six ports function identically and with the same bandwidth.

The SE7501BR2 can support up to 5 USB ports. Three external connectors are found on the ATX I/O panel, located on the back edge of the server board. The fourth and fifth USB ports are optional and can be accessed by special cabling (not bundled with product) from the internal 9-

pin header located to external USB ports located in either the front or the rear of a given chassis.

3.2.3.4 Compatibility Interrupt Control

The ICH3 provides the functionality of two 82C59 PIC devices for ISA-compatible interrupt handling.

3.2.3.5 APIC

The ICH3 integrates an IO APIC that is used to distribute 24 PCI interrupts.

3.2.3.6 General Purpose Input and Output Pins

The ICH3-S provides a number of general purpose input and output pins. Many of these pins have alternate functions, and thus all are not available. The following table lists the GPI and GPO pins used on the SE7501BR2 baseboard and gives a brief description of their function.

Table 5. ICH3-S GPIO Usage Table

Pin #	Signal Name	Description
D4	P64H_RASERR_L	Reliability, Availability, Serviceability Error
B6	ICH3_RST_VIDEO_L	Disable Video Controller
B3	ICH3_RST_SCSI_L	Disable SCSI Controller
Y3	ICH3_RST_NIC1_L	Disable Network Interface Controller #1
W4	ICH3_RST_NIC2_L	Disable Network Interface Controller #2
Y2	SIO_PME_L	PME# from SIO
V2	IDE_CBL_DET_P	Primary IDE Bus 80 Conductor Cabel Detect
V4	BMC_IRQ_SMI_L	BMC System Management Interrupt
F21	ZZ_MFG_MODE	Manufacturing Mode Detect for Test
G19	ZZ_PASSWORD_CLR_L	Password Clear
E22	ZZ_BIOS_RCVR_L	Enable Recovery Boot
E21	ZZ_BB_ID0	Baseboard ID 0 - Used to identify revision of board
H21	ZZ_BB_ID1	Baseboard ID 1 - Used to identify revision of board
G23	ZZ_BB_ID2	Baseboard ID 2 - Used to identify revision of board
G21	ZZ_ICH3_FRB3_TIMER_HALT_L	ICH3 FRB3 Timer Halt Output
D23	ZZ_CMOS_CLR_L	CMOS clear
E23	IDE_CBL_DET_S	Secondary IDE Bus 80 Conductor Cabel Detect

3.2.3.7 Power Management

One of the embedded functions of the ICH3-S is a power management controller. The SE7501BR2 server board uses this to implement ACPI-compliant power management features. The SE7501BR2 supports sleep states S0, S1, S4, and S5.

3.2.3.8 Real-time Clock

SE7501BR2 server board uses RTC function provided by ICH3-S.

3.3 Super I/O

The National Semiconductor* PC87417 Super I/O device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, PS/2-compatible keyboard and mouse, and hardware monitor controller. The SE7501BR2 server board supports the following features:

- GPIOs
- Two serial ports
- Parallel port
- Floppy Controller
- Keyboard and mouse through PS/2 Connectors
- "Wake-on" control

3.3.1 GPIOs

The National Semiconductor* PC87417 Super I/O provides number of general-purpose input/output pins that the SE7501BR2 server board utilizes. The following table identifies the pin, the signal name used in the schematic and a brief description of its usage:

Table 6. Super I/O GPIO Usage Table

Pin #	Signal Name	Description
49	ROMB_PRESENT_L	ROMB Present in add-in connector
35	BMC_SLP_BTN_L	Sleep Button from BMC
38	SIO_PME_L	PME# to ICH3
124	SIO_EMP_INUSE	Enable EMP port
20	PA_PCIXCAP	P64-B PCI-X Capability
21	PB_PCIXCAP	P64-C PCI-X Capability
50	PA_PME_L	PME# from P64H2 P64-B
51	FP_PWR_LED_L	Front Panel Power Idicator
52	PB_PME_L	PME# from P64H2 P64-C
53	BMC_SCI_L	SCI signal

3.3.2 Serial Ports

The SE7501BR2 server board provides two serial ports, one DB9 connector (J8A18) is located on the rear ATX I/O to provide Serial Port A and an internal 9-pin header (J1B11); which can be routed to the front or the back of the chassis, provides Serial Port B[7]. See section 10.13 for the connector pin-outs.

3.3.3 Parallel Port

The SE7501BR2 server board provides one parallel port via a DB-25 connector (J7A28) located on the rear ATX I/O. See section 10.14 for the connector pin-outs.

[7] Serial Port B is the designated Server Management serial port.

3.3.4 Floppy Disk Controller

The floppy disk controller (FDC) in the SIO is functionally compatible with floppy disk controllers in the DP8473 and N844077. All FDC functions are integrated into the SIO including analog data separator and 16-byte FIFO. The SE7501BR2 provides an SSI compliant 36-pin connector (J4J7).

3.3.5 Keyboard and Mouse

Two stacked (J9A5) PS/2 ports are provided to support both a keyboard and mouse. The top connector is labeled “mouse” and the bottom is labeled “keyboard,” although the board set can support swapping of these connections.

3.3.6 Wake-on Control

The Super I/O contains functionality that allows various events to control the power-on and power-off the system.

3.3.7 BIOS Flash

The SE7501BR2 server board incorporates an Intel® 3-Volt Advanced+ Boot Block 28F320C3 Flash memory component. The 28F320C3 is a high-performance 32-megabit memory component that provides 2048K x 16 of BIOS and non-volatile storage space. The flash device is connected through the X-bus from the SIO.

4. Configuration and Initialization

This chapter describes the initial programming environment including address maps for memory and I/O, techniques and considerations for programming ASIC registers, and configuration of hardware options.

4.1 Memory Space

At the highest level, the Xeon™ processor address space is divided into 3 regions, as shown in the following figure. Each region contains sub-regions as described in following sections. Attributes can be independently assigned to regions and sub-regions using the SE7501BR2 registers.

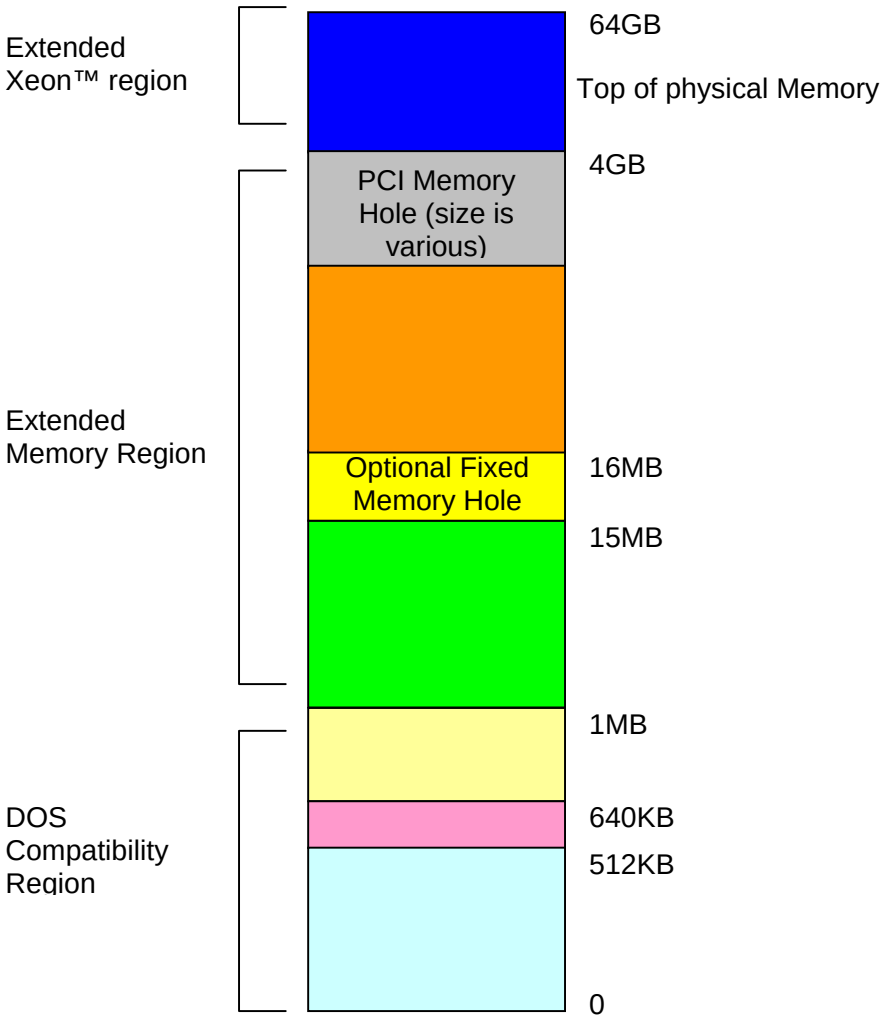

Figure 4. Xeon™ Processor Memory Address Space

4.1.1 DOS Compatibility Region

The first region of memory below 1 MB was defined for early PCs, and must be maintained for compatibility reasons. The region is divided into sub-regions as shown in the following figure.

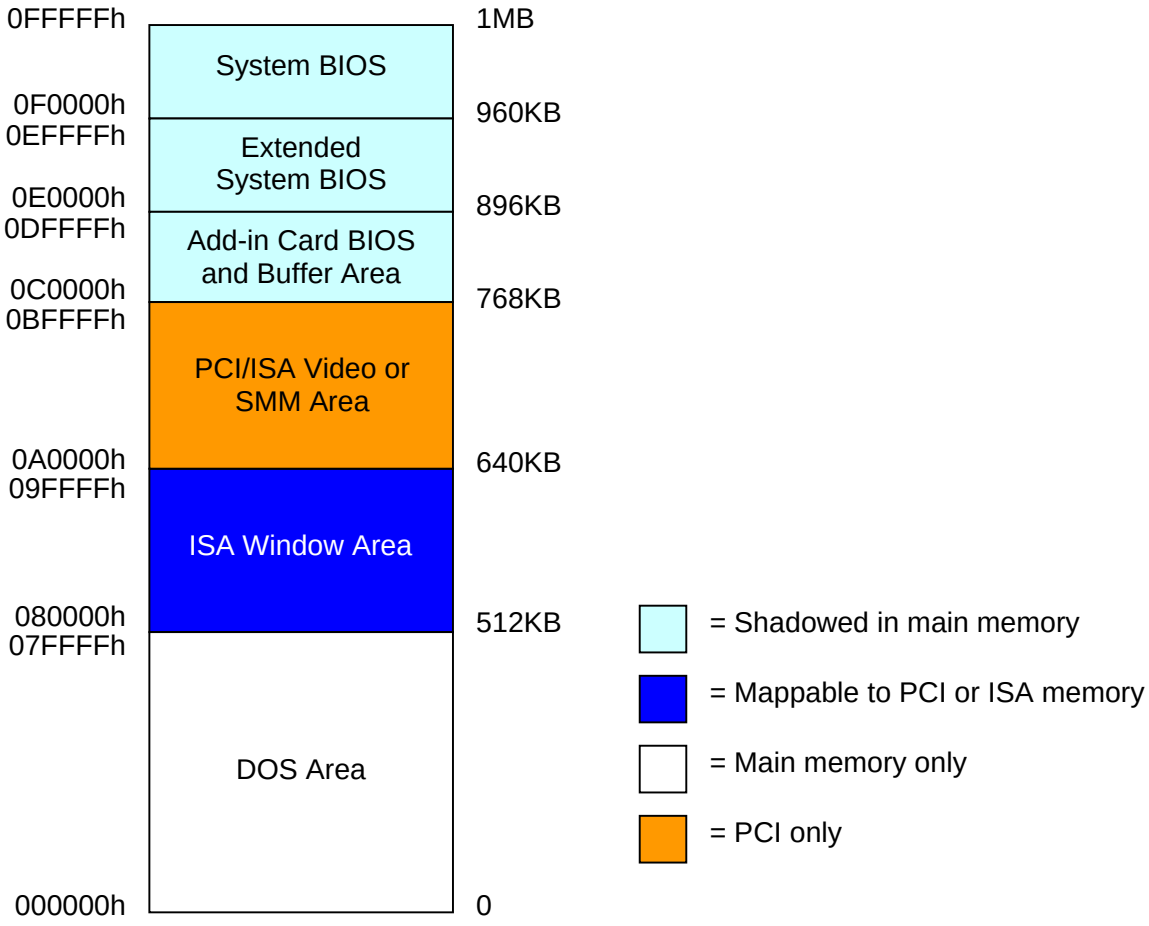

Figure 5. DOS Compatibility Region

4.1.1.1 DOS Area

The DOS region is 512 KB in the address range 0 to 07FFFFh. This region is fixed and all accesses go to main memory.

4.1.1.2 ISA Window Memory

The ISA Window Memory is 128 KB between the address of 080000h to 09FFFFh. This area can be mapped to the PCI bus or main memory.

4.1.1.3 Video or SMM Memory

The 128 KB Graphics Adapter Memory region at 0A0000h to 0BFFFFh is normally mapped to the VGA controller on the PCI bus. This region is also the default region for SMM space.

4.1.1.4 Add-in Card BIOS and Buffer Area

The 128 KB region between addresses 0C0000h to 0DFFFFh is divided into eight segments of 16 KB segments mapped to ISA memory space, each with programmable attributes, for expansion cards buffers. Historically, the 32 KB region from 0C0000h to 0C7FFFh has contained the video BIOS location on the video card

4.1.1.5 Extended System BIOS

This 64 KB region from 0E0000h to 0EFFFFh is divided into 4 blocks of 16 KB each, and may be mapped with programmable attributes to map to either main memory or to the PCI bus. Typically this area is used for RAM or ROM. This region can also be used extended SMM space.

4.1.1.6 System BIOS

The 64 KB region from 0F0000h to 0FFFFFh is treated as a single block. By default this area is normally read/write disabled with accesses forwarded to the PCI bus. Through manipulation of R/W attributes, this region can be shadowed into main memory. This region can also be used for extended SMM space.

4.1.2 Extended Memory Region

Extended memory on SE7501BR2 is defined as all address space greater than 1MB. Extended Memory region covers 4GB of address space from addresses 0100000h to FFFFFFFFh, as shown in the following figure.

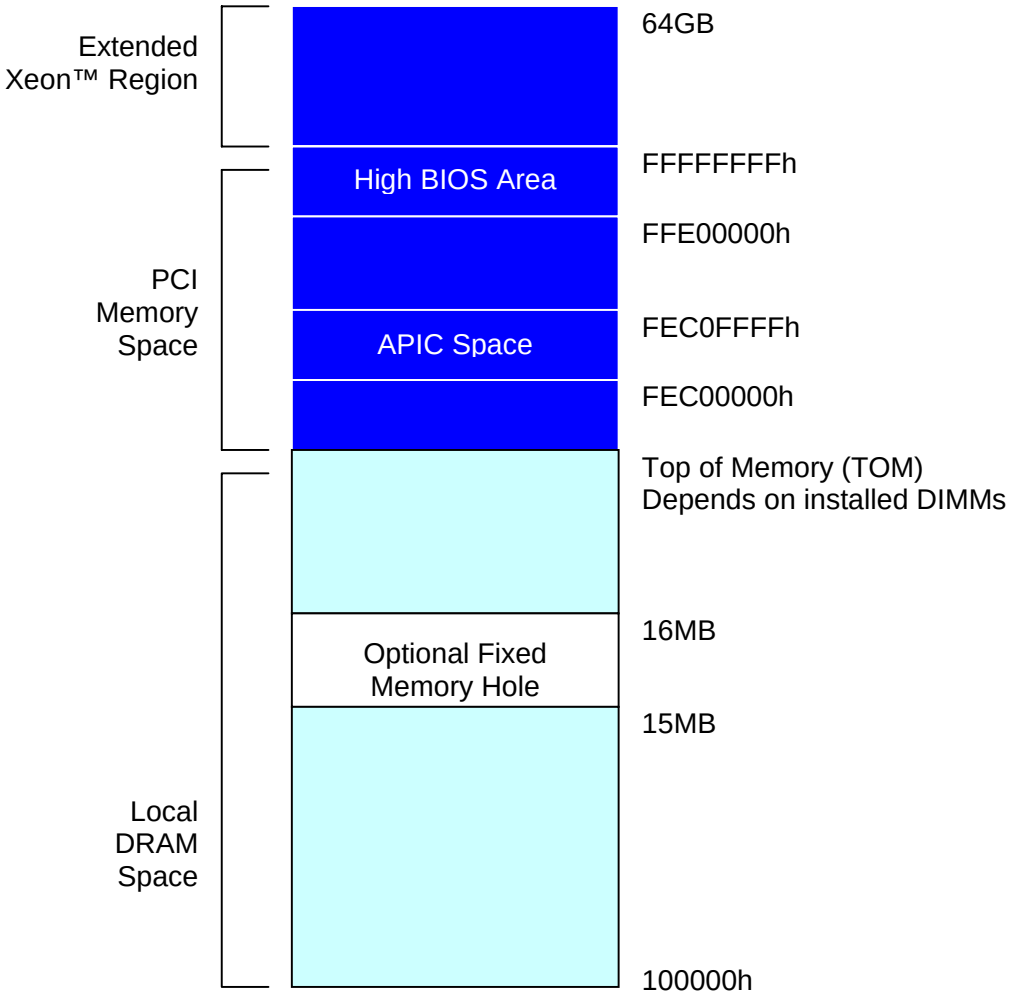

Figure 6. Extended Memory Map

4.1.2.1 Main Memory

All installed Memory greater than 1 MB is mapped to local main memory, up to top of physical memory at 8 GB. Memory between 1 MB to 15 MB is considered to be standard ISA extended memory. 1 MB of memory starting at 15 MB can be optionally mapped to the PCI bus memory space.

The remainder of this space, up to 8 GB, is always mapped to main memory, unless Extended SMRAM is used, which limits the top of memory to 256MB.

4.1.2.2 PCI Memory Space

Memory addresses below 4 GB range are mapped to the PCI bus. This region is divided into three sections: High BIOS, APIC Configuration Space, and General-purpose PCI Memory. The General-purpose PCI Memory area is typically used memory-mapped I/O to PCI devices. The memory address space for each device is set using PCI configuration registers.

4.1.2.3 High BIOS

The top 2 MB of Extended Memory is reserved for the system BIOS, extended BIOS for PCI devices, and A20 aliasing by the system BIOS. The Xeon processor begins executing from the high BIOS region after reset.

4.1.2.4 I/O APIC Configuration Space

A 64 KB block located 20 MB below 4 GB (0FEC00000 to 0FEC0FFFFh) is reserved for the I/O APIC configuration space.

I/O APIC units are located beginning at a base address determined by subtracting 013FFFF0h from the reset vector. The first I/O APIC is located at FEC00000h. Each I/O APIC unit is located at FEC0c000h where x is the I/O APIC unit (0 through F).

4.1.2.5 Extended Xeon™ Processor Region (above 4GB)

A Xeon processor-based system can have up to 64 GB of addressable memory. BIOS uses Extended Addressing mechanism to use the address ranges.

4.1.3 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into main memory. Typically this is done to allow ROM code to execute more rapidly out of RAM. ROM is designated read-only during the copy process while RAM at the same address is designated write-only. After copying, the RAM is designated read-only and the ROM is designated write-only (shadowed). Processor bus transactions are routed accordingly. Transactions originated from the PCI bus or ISA masters and targeted at shadowed memory block will not appear on the processor’s bus.

4.1.4 System Management Mode Handling

The Intel E7501 MCH supports System Management Mode (SMM) operation in standard (compatible) mode. System Management RAM (SMRAM) provides code and data storage space for the SMI_L handler code, and is made visible to the processor only on entry to SMM, or other conditions which can be configured using Intel E7501 PCI registers. Compatible SMRAM, located in main memory below the 1 MB boundary at addresses 000A0000h through 000B0000h is non-cacheable.

4.2 I/O Map

The SE7501BR2 allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including the ICH3-S, have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On SE7501BR2, the ICH3-S provides the bridge to ISA functions through the LPC bus.

4.3 Accessing Configuration Space

All PCI devices contain PCI configuration space, accessed using mechanism #1 defined in the PCI Local Bus Specification.

If dual processors are used, only the processor designated as the BSP should perform PCI configuration space accesses. Precautions should be taken to guarantee that only one processor performs system configuration.

Two DWORD I/O registers in the Intel Chipset are used for the configuration space register access:

CONFIG_ADDRESS (I/O address 0CF8h)

CONFIG_DATA (I/O address 0CFCh)

When CONFIG_ADDRESS is written to with a 32-bit value selecting the bus number, device on the bus, and specific configuration register in the device, a subsequent read or write of CONFIG_DATA initiates the data transfer to/from the selected configuration register. Byte enables are valid during accesses to CONFIG_DATA; they determine whether the configuration register is being accessed or not. Only full DWORD reads and writes to CONFIG_ADDRESS are recognized as a configuration access by the Intel chipset. All other I/O accesses to CONFIG_ADDRESS are treated as normal I/O transactions.

4.3.1 CONFIG_ADDRESS Register

CONFIG_ADDRESS is 32 bits wide and contains the field format shown in the following figure. Bits [23::16] choose a specific bus in the system. Bits [15::11] choose a specific device on the selected bus. Bits [10:8] choose a specific function in a multi-function device. Bit [7::2] select a specific register in the configuration space of the selected device or function on the bus.

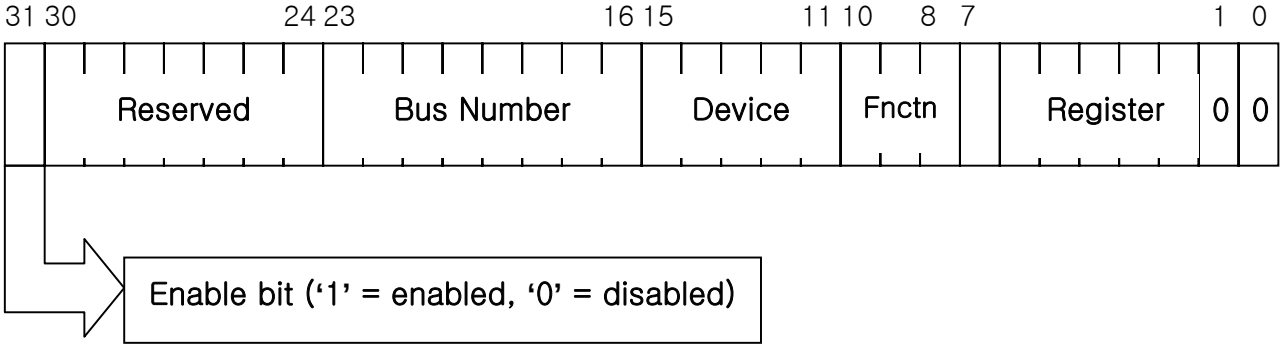

Figure 7. CONFIG_ADDRES Register

4.3.1.1 Bus Number

PCI configuration space protocol requires that all PCI buses in a system be assigned a Bus Number. Furthermore, bus numbers must be assigned in ascending order within hierarchical buses. Each PCI bridge has registers containing its PCI Bus Number and subordinate PCI Bus Number, which must be loaded by POST code. The Subordinate PCI Bus Number is the bus number of the last hierarchical PCI bus under the current bridge. The PCI Bus Number and the Subordinate PCI Bus Number are the same in the last hierarchical bridge.

4.3.1.2 Device Number and IDSEL Mapping

Each device under a PCI bridge has its IDSEL input connected to one bit out of the PCI bus address/data signals AD[31::11] for the PCI bus. Each IDSEL-mapped AD bit acts as a chip select for each device on PCI. The host bridge responds to a unique PCI device ID value, that along with the bus number, cause the assertion of IDSEL for a particular device during configuration cycles. The following table shows the correspondence between IDSEL values and PCI device numbers for the PCI bus. The lower 5-bits of the device number are used in CONFIG_ADDRESS bits [15::11].

Table 7. PCI Device IDs

Device Description	Bus # (segment)	Device ID (Hex)
MCH	0	00
ICH3-S P2P Bridge	0	1E
ICH3-S USB	0	1D
ICH3-S IDE	0	1F
Video	1	0C
P64H2 P2P P64-B	2	1F
P64H2 P2P P64-C	2	1D
Gigabit NIC	1	04
10/100 NIC	1	03
Slot 1 (PCI-X 64-bit, 66/100/133 MHz)	4 (P64-C)	02
Slot 2 (PCI-X 64-bit, 66/100/133 MHz)	4 (P64-C)	01
Slot 3 (PCI 64-bit, 66/100 MHz)	3 (P64-B)	02
Slot 4 (PCI 64-bit, 66/100 MHz)	3 (P64-B)	01
Slot 5 (PCI 32-bit, 33 MHz)	1 (P32-A)	09
Slot 6 (PCI 32-bit, 33 MHz)	1 (P32-A)	08
SCSI	3	03

4.4 Hardware Initialization

An Intel® Xeon™ processor system based on Intel® E7501 MCH is initialized the following manner.

1. When power is applied, after receiving RST_PWRGD_PS from the power supply, the BMC provides resets using the RST_P6_PWRGOOD signal. The ICH3-S asserts RST_PCIRST_L to MCH, P64H2, and other PCI devices. MCH then assert RST_CPURST_L to reset the processor(s).

2. The MCH is initialized, with its internal registers set to default values. Before RST_CPURST_L is deasserted, the MCH asserts BREQ0_L. Processor(s) in the system determine which host bus agents they are, Agent 0 or Agent 1, based on whether their BREQ0_L or BREQ1_L is asserted. This determines bus arbitration priority and order.

3. After the processor(s) in the system determines which processor will be the BSP, the non-BSP processor becomes an application processor and idles, waiting for a Startup Inter Processor Interrupt (SIPI).

4. The BSP begins by fetching the first instruction from the reset vector.

5. The Intel E7501 chipset registers are updated to reflect memory configuration. DIMM is sized and initialized.

6. All PCI and ISA I/O subsystems are initialized and prepared for booting.

Refer to the SE7501BR2 BIOS EPS for more detail regarding system initialization and configuration

5. Clock Generation and Distribution

All buses on the SE7501BR2 baseboard operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 100 MHz at 3.3 V logic levels. For processors, MCH, and ITP port.
- 66 MHz at 3.3 V logic levels: For MCH, ICH3-S and P64H2 clock
- 33 MHz at 3.3 V logic levels: For ICH3, BMC, Video, SIO, PCI32/33 Slots, NIC1 & NIC2
- 48 MHz at 3.3 V logic levels: ICH3-S and SIO
- 14 MHz at 3.3V logic levels: ICH3-S and SIO

The synchronous clock sources on the SE7501BR2 baseboard are:

- 133-MHz clock for PCI-X Slots
- 100-MHz host clock for processors, MCH, Memory DIMMs, and the ITP
- 66-MHz clock for MCH, ICH3, P64H2, and SCSI
- 48-MHz clock for ICH3-S and SIO
- 33-MHz clock for ICH3, BMC, Video, SIO, PCI32/33 Slots, NIC1 & NIC2
- 14-MHz clock for ICH3-S and Video

For information on processor clock generation, see the *CK408B Synthesizer/Driver Specification*.

The SE7501BR2 baseboard also provides asynchronous clock generators:

- 40-MHz clock for the embedded SCSI controller
- 25-MHz clocks for the embedded network interface controllers
- 32.768-KHz clock for the ICH RTC
- 40-MHz clock for the BMC

The following figure illustrates clock generation and distribution on the SE7501BR2 server board.

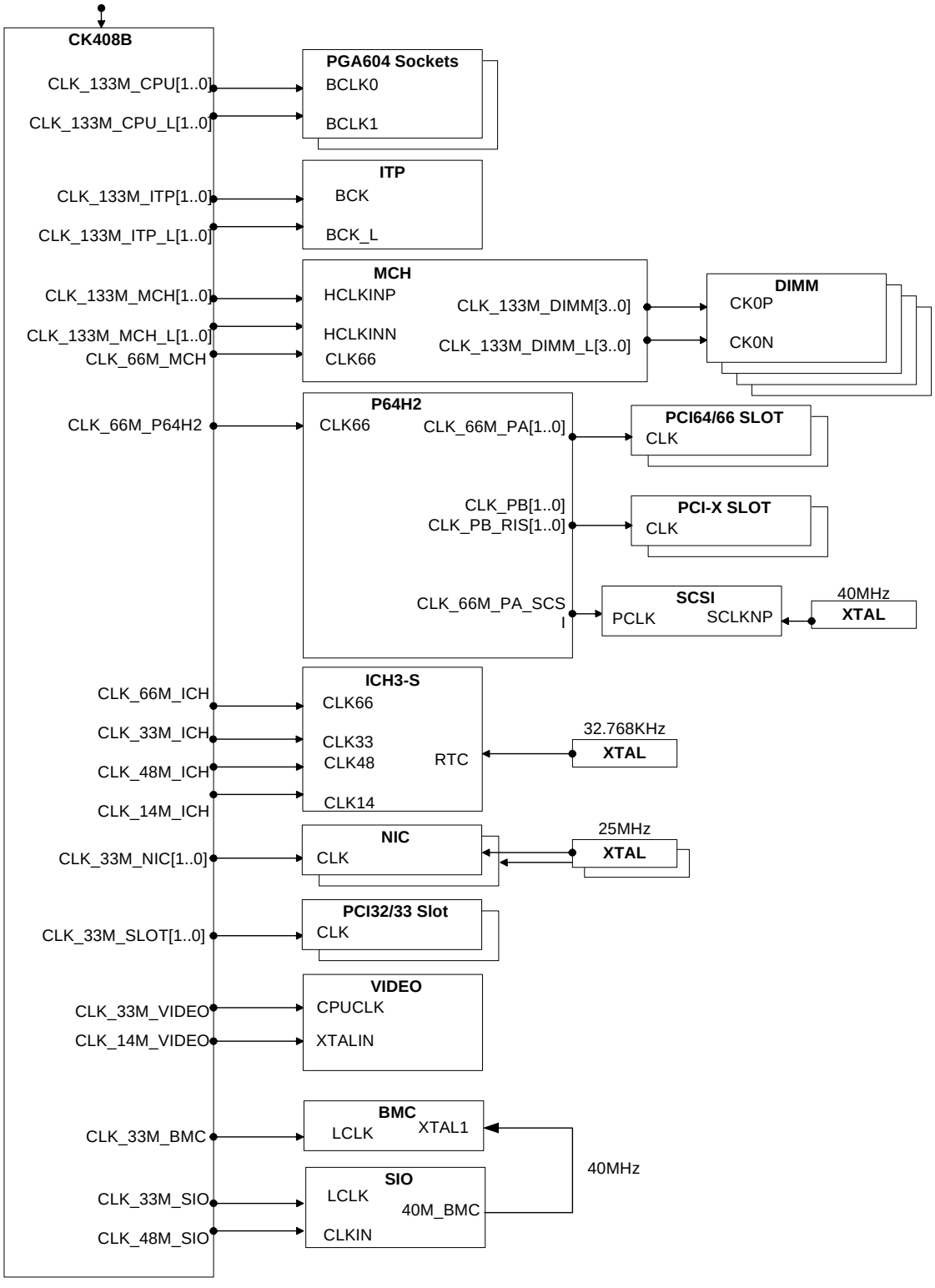

Figure 8. SE7501BR2 Baseboard Clock Distribution

6. PCI I/O Subsystem

6.1 PCI Subsystem

The primary I/O bus for the SE7501BR2 server board is PCI, with three independent PCI bus segments. The PCI buses comply with the *PCI Local Bus Specification*, Rev 2.2 and PCI-X specification rev 1.0. The P32-A bus segment is directed through the ICH3-S while the two 64-bit segments, P64-B and P64-C, are directed through the P64H2. The table below lists the characteristics of the three PCI bus segments.

Table 8. PCI Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Mode	Speed	PCI Slots
P32-A	5 V	32 bits	PCI	33 MHz	Slots 5 & 6. Supports Full-length cards, 5V bus
P64-B	3.3 V	64 bits	PCI-X	100/66 MHz	Slots 3 & 4. Supports Full-length cards, 3.3V bus
P64-C	3.3 V	64 bits	PCI-X	133/100/66 MHz	Slots 1 & 2. Supports Full-length cards, 3.3V bus

Note: The system BIOS is responsible for setting the mode (PCI or PCI-X) and bus speed for the two segments provided by the P64H2. The actual bus mode/speed will be determined by the least capable card installed on that bus. The mode/speed of P64C is set by BIOS as PCI-X 64-bit/133MHz when only one slot is populated, and as PCI-X 64-bit/100MHz when two slots are populated. The mode/speed of P64B is set by BIOS as PCI-X 64-bit/100MHz with one or two slots populated as the integrated SCSI controller resides on this bus.

6.1.1 P32-A: 32-bit, 33-MHz PCI Subsystem

All 32-bit, 33-MHz PCI I/O for the SE7501BR2 server board is directed through the ICH3-S. The 32-bit, 33-MHz PCI segment created by the ICH3-S is known as the P32-A segment. The P32-A segment supports the following embedded devices and connectors:

- 2D/3D Graphics Accelerator: ATI Rage* XL Video Controller
- 10/100 NIC: Intel® 82550PM Fast Ethernet Controller (NIC1[8])
- 10/100/1000 NIC: Intel® 82540EM Gigabit Ethernet Controller (NIC2)
- Two 32-bit/33MHz PCI slots (PCI Slot 5 and Slot 6)

Each of the embedded devices listed above will be allocated a GPIO to disable the device. The PCI segment will support full length, full height PCI cards as well as half-length PCI cards.

6.1.1.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD[31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a

[8] NIC1 is the designated Server Management NIC.

unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P32-A devices, and the corresponding device description.

Table 9. P32-A Configuration IDs

IDSEL Value	Device
24	PCI Slot 6
25	PCI Slot 5
19	Intel 82550PM Fast Ethernet Controller
20	Intel 82540EM Giga bit Ethernet Controller
28	ATI Rage* XL video controller

6.1.1.2 P32-A Arbitration

P32-A supports six PCI masters (ATI Rage XL, Intel 82550PM, Intel 82540EM, the ICH3-S, and two PCI 32-bit slots). All PCI masters must arbitrate for PCI access, using resources supplied by the ICH3-S. The host bridge PCI interface (ICH) arbitration lines REQx* and GNTx* are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 10. P32- Arbitration Connections

Baseboard Signals	Device
PCI_REQ_L4/PCI_GNT_L4	PCI32/33 Slot6
PCI_REQ_L3/PCI_GNT_L3	PCI32/33 Slot5
PCI_REQ_L2/PCI_GNT_L2	Intel 82550PM Fast Ethernet Controller (NIC1)
PCI_REQ_L1/PCI_GNT_L1	Intel 82540EM Gigabit Ethernet Controller (NIC2)
PCI_REQ_L0/PCI_GNT_L0	ATI Rage XL video controller

6.1.2 P64-B: 64-bit, 100/66-MHz PCI-X Subsystem

The P64-B PCI-X segment is directed through the P64H2. It supports 3.3 volts, 64-bit, 100/66-MHz PCI-X/PCI devices. The P64-B segment supports the following embedded devices and connectors:

- SCSI controller: Adaptec* AIC-7901 Single-channel U320 SCSI Controller[9]
- Two 64-bit/100MHz PCI-X slots (PCI-X Slot 3 and Slot 4)

Note: PCI-X Slot 4 is ZCR (Zero Channel RAID) capable. When the ZCR option is used, the entire P64-B PCI-X bus may operate in PCI 64 bit/66MHz mode.

Slots on the P64-B segment will support full length, full height PCI cards as well as half-length PCI cards.

[9] Single Ended Mode not supported.

6.1.2.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD[31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P64-B devices, and the corresponding device description.

Table 11. P64-B Configuration IDs

IDSEL Value	Device
19	On-board SCSI controller
18	PCI-X Slot 3
17	PCI-X Slot 4

6.1.2.2 P64-B Arbitration

P64-B supports four PCI masters (AIC-7901, the P64H2, and two PCI-X 64-bit slots). All PCI masters must arbitrate for PCI access using resources supplied by the P64H2. The host bridge PCI interface (P64H2) arbitration lines REQx* and GNTx* are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 12. P64-B Arbitration Connections

Baseboard Signals	Device
PA_REQ_L2/PA_GNT_L2	On-board SCSI controller
PA_REQ_L1/PA_GNT_L1	PCI-X Slot 3
PA_REQ_L0/PA_GNT_L0	PCI-X Slot 4

6.1.2.3 Zero Channel RAID (ZCR) Capable – PCI-X Slot 4

The SE7501BR2 server board is capable of supporting zero channel RAID add-in cards. The ZCR cards[10] are only supported in PCI-X Slot 4 located in the P64-B segment.

The ZCR add-in cards leverage the on-board SCSI controller along with their own built-in intelligence to provide a complete RAID controller subsystem on-board. The baseboard uses an implementation commonly referred to as RAID I/O Steering (RAIDIOS) specification version 1.0 to support this feature.

When one of the supported RAID cards is installed, the SCSI interrupts are routed to the RAID adapter instead of to the PCI interrupt controller. In addition, the IDSEL of the SCSI controller is not driven to the controller and thus will not respond as an on board device. The host-based I/O device is effectively hidden from the system.

[10] Refer to the Tested Hardware & Operating System List for a complete list of all ZCR controllers supported in the SE7501BR2 server board.

6.1.3 P64-C: 64-bit, 133/100/66-MHz PCI-X Subsystem

The P64-C PCI-X segment is directed through the P64H2. It supports 3.3 volts, 64-bit, 133/100/66-MHz PCI-X/PCI devices. The P64-C segment supports the following embedded devices and connectors:

- Two 64-bit/100MHz PCI-X Slots (PCI-X Slot 1 and Slot 2)

The PCI-X segment will support full length, full height PCI cards as well as half-length PCI cards.

6.1.3.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD[31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P64-C devices, and the corresponding device description.

Table 13. P64-C Configuration IDs

IDSEL Value	Device
18	PCI-X Slot 1
17	PCI-X Slot 2

6.1.3.2 P64-C Arbitration

P64-C supports four PCI masters (P64H2 and two PCI-X slots). All PCI masters must arbitrate for PCI access using resources supplied by the P64H2. The host bridge PCI interface (P64H2) arbitration lines REQx* and GNTx* are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 14. P64-C Arbitration Connections

Baseboard Signals	Device
PA_REQ_L1/P64_S_GNT1	PCI-X Slot 1
PA_REQ_L0/P64_S_GNT0	PCI-X Slot 2

6.2 Ultra 320 SCSI

The SE7501BR2 server board utilizes the Adaptec* AIC-7901 to provide an embedded single-channel SCSI bus capable of supporting the Ultra 320 SCSI or Ultra 320 Entry Level RAID via Adaptec HostRAID*.

The AIC-7901 is a 356-pin BGA device which houses a single SCSI controller that provides a single 64-bit, 100-MHz PCI-X bus master interface as a multifunction device. Internally, the controller is capable of operations using LVD SCSI providing 80 MBps (Ultra 2), 160 MBps

(Ultra 160), or 320 MBps (Ultra 320). The controller has its own set of PCI configuration registers and PCI I/O registers. The SE7501BR2 server board supports disabling of the on-board SCSI controller through the BIOS setup menu.

The SCSI sub-system on the SE7501BR2 server board also supports a single on board 68-pin connector interface, active terminators, termination voltage, a resetable fuse, and a protection diode to guard the board from unwanted power, as supplied from an external peripheral power source. By default the on-board SCSI termination is always enabled, however, when using a SCSI Y-cable, the on-board SCSI termination can be disabled by entering the Adaptec BIOS Setup utility during POST.

Note: Single ended mode is not supported by the board.

6.2.1 Adaptec HostRAID*

The SE7501BR2 server board enables entry-level RAID functionality known as HostRAID* via Adaptec's AIC-7901 SCSISelect* Utility embedded in the controller's option ROM (Ctrl-A), and an Alert Utility used to provide automatic error/warning notification and task information[11]. The HostRAID functionality while supporting all major SCSI peripherals enables support for up to 2 RAID arrays on the AIC-7901 single channel controller meeting the following configuration:

- One RAID 0 with 3 or 4 drives
- Two RAID 0s with two drives each
- One RAID 0 with two drives and one RAID 1
- Two RAID 1s with or without a spare each

6.3 Video Controller

The SE7501BR2 server board provides an ATI* Rage* XL PCI graphics accelerator, along with 8 MB of video SDRAM and support circuitry for an embedded SVGA video subsystem. The ATI Rage XL chip contains a SVGA video controller, clock generator, 2D and 3D engine, and RAMDAC in a 272-pin PBGA. One 2Mx32 SDRAM chip provides 8 MB of video memory.

The SVGA subsystem supports a variety of modes, up to 1600 x 1200 resolution in 8/16/24/32 bits per pixel (bpp) modes under 2D, and up to 1024 x 768 resolution in 8/16/24/32 bpp modes under 3D. It also supports both CRT and LCD monitors up to 100 Hz vertical refresh rate.

The SE7501BR2 server board provides a standard 15-pin VGA connector and supports disabling of the on-board video through the BIOS Setup menu or automatically when a plug-in video card is installed in any of the PCI slots.

6.3.1 Video Modes

The ATI* Rage* XL chip supports all standard IBM* VGA modes. The following table shows the 2D/3D modes supported for both CRT and LCD. The table specifies the minimum memory requirement for various display resolution, refresh rates, and color depths.

[11] For Operating System support, system requirements, compatibility, RAID array configuration and use on HostRAID and the Adaptec Alert refer to Adaptec's Host RAID User's Guide available in the boxed board's resource CD.

Table 15. Video Modes

2D Mode	Refresh Rate (Hz)	SE7501BR2 2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
800x600	60, 70, 75, 90, 100	Supported	Supported	Supported	Supported
1024x768	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
1280x1024	43, 60	Supported	Supported	Supported	Supported
1280x1024	70, 72	Supported	–	Supported	Supported
1600x1200	60, 66	Supported	Supported	Supported	Supported
1600x1200	76, 85	Supported	Supported	Supported	–
3D Mode	**Refresh Rate (Hz)**	**SE7501BR2 3D Video Mode Support with Z Buffer Enabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	–	–
1600x1200	60,66,76,85	Supported	–	–	–
3D Mode	**Refresh Rate (Hz)**	**SE7501BR2 3D Video Mode Support with Z Buffer Disabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	Supported	–
1600x1200	60,66,76,85	Supported	Supported	–	–

6.3.2 Video Memory Interface

The memory controller subsystem of the Rage XL arbitrates requests from direct memory interface, the VGA graphics controller, the drawing coprocessor, the display controller, the video scalar, and hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

The SE7501BR2 supports an 8 MB (512Kx32bitx4 Banks) SDRAM device for video memory. The following table shows the video memory interface signals:

Table 16. Video Memory Interface

Signal Name	I/O Type	Description
CAS#	O	Column Address Select
CKE	O	Clock Enable for Memory
CS#[1..0]	O	Chip Select for Memory
DQM[7..0]	O	Memory Data Byte Mask
DSF	O	Memory Special Function Enable
HCLK	O	Memory Clock

[11..0]	O	Memory Address Bus
MD[31..0]	I/O	Memory Data Bus
RAS#	O	Row Address Select
WE#	O	Write Enable

6.3.3 Host Bus Interface

The ATI* Rage* XL supports a PCI 33 MHz bus. The following diagram shows the signals for the PCI interface:

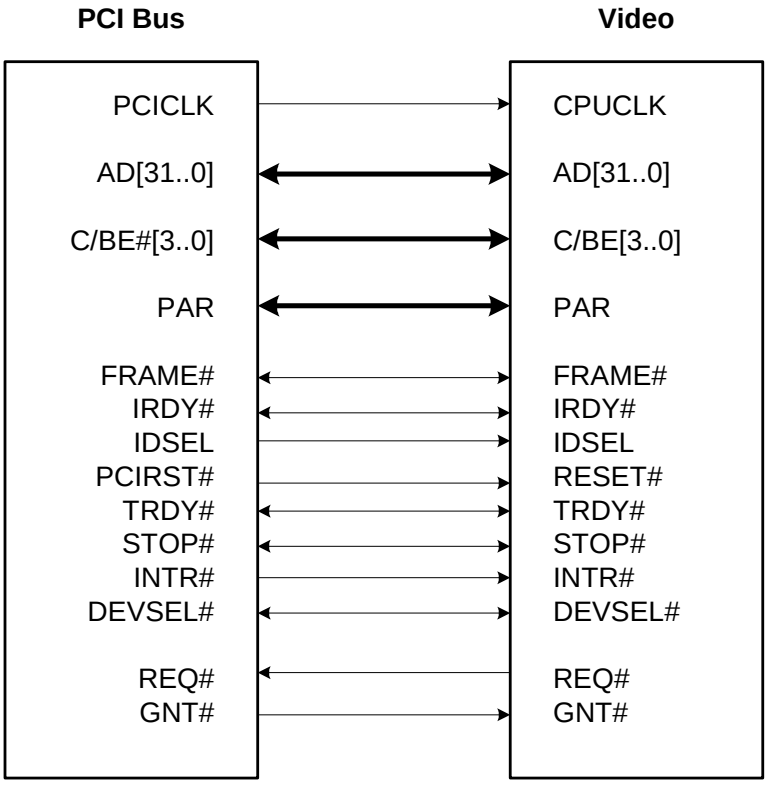

Figure 9. Video Controller PCI Bus Interface

6.4 Network Interface Controller (NIC)

The SE7501BR2 server board supports a 10Base-T/100Base-TX Fast Ethernet Network Controller based on the Intel® 82550PM controller (NIC1) and a 10Base-T/100Base-TX/1000Base-TX Gigabit Ethernet controller based on the Intel® 82540EM controller (NIC2). NIC1 is the designated Server Management NIC.

The 82550PM and 82540EM are highly integrated PCI LAN controllers in a thin 15 mm^2 BGA package. The controller's baseline functionality is equivalent to that of the Intel 82559 with the addition of alert-on-LAN functionality. The SE7501BR2 server board supports independent disabling of the two NIC controllers using the BIOS setup menu.

The 82550PM supports the following features:

- Glueless 32-bit PCI, CardBus master interface (Direct Drive of Bus), compatible with *PCI local Bus Specification, Revision 2.2.*
- Integrated IEEE 802.3 10Base-T and 100Base-TX compatible PHY.
- IEEE 820.3u auto-negotiation support.
- Full duplex support at both 10 Mbps and 100 Mbps operation.
- Integrated UNDI ROM support.
- MDI/MDI-X and HWI support.
- Low power +3.3 V device.

The 82540EM supports the following features:

- Glueless 32-bit PCI, CardBus master interface (Direct Drive of Bus), compatible with *PCI local Bus Specification, Revision 2.2.*
- Integrated IEEE 802.3 10Base-T, 100Base-TX and 1000Base-TX compatible PHY
- IEEE 820.3u auto-negotiation support
- Full duplex support at 10 Mbps, 100Mbps and 1000 Mbps operation
- Integrated UNDI ROM support
- MDI/MDI-X and HWI support

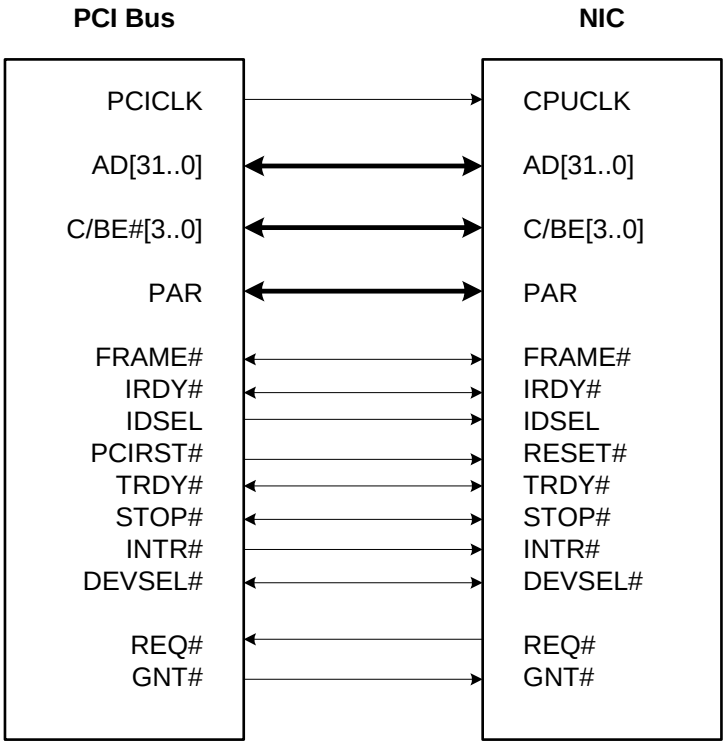

Figure 10. NIC Controller PCI Bus Interface

6.4.1 NIC Connector and Status LEDs

The 82550PM (NIC1) drives two LEDs located on the network interface connector (connector on the right side when looking from the back at the ATX I/O rear panel). The green LED to the right of the connector indicates network connection when on and transmit / receive activity when blinking. The green LED to the left of the connector indicates 100-Mbps operation when lit and 10-Mbps when off.

Table 17. NIC1 Status LED

LED Color	LED State	NIC 1 State
Green (left)	Off	10-Mbps
	On	100-Mbps
Green (right)	On	On
	Blinking	Transmit / Receive activity

The 82540EM (NIC2) drives two LEDs located on the network interface connector (connector in the left side when looking from the back at the ATX I/O rear panel). The green LED to the right of the connector indicates network connection when on, and Transmit/Receive activity when blinking. The bi-color LED to the left of the connector indicates 1000-Mbps operation when yellow, 100-Mbps operation when green, and 10-Mbps when off.

Table 18. NIC2 Status LED

LED Color	LED State	NIC 2 State
Green/Yellow (left)	Off	10-Mbps
	Green	100-Mbps
	Yellow	1000-Mbps
Green (right)	On	On
	Blinking	Transmit / Receive activity

6.5 Interrupt Routing

The SE7501BR2 interrupt architecture accommodates both PC-compatible PIC mode and APIC mode interrupts through use of the integrated I/O APICs in the ICH3 and the P64H2.

6.5.1 Legacy Interrupt Routing

For PC-compatible mode, the ICH3-S provides two 82C59-compatible interrupt controllers. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing.

Interrupts, both PCI and IRQ types, are handled by the ICH3-S. The ICH3-S then translates these to the APIC bus. The numbers in the table below indicate the ICH3-S PCI interrupt input

pin to which the associated device interrupt (INTA, INTB, INTC, INTD) is connected. The ICH3's I/O APIC exists on the I/O APIC bus with the processors.

6.5.1.1 Legacy Interrupt Sources

The table below recommends the logical interrupt mapping of interrupt sources on the SE7501BR2 server board. The actual interrupt map is defined using configuration registers in the ICH3-S.

Table 19. PCI Interrupt Routing/Sharing

ISA Interrupt	Description
INTR	Processor interrupt.
NMI	NMI to processor.
IRQ1	Keyboard interrupt.
IRQ3	Serial port A or B interrupt from SIO device, user-configurable.
IRQ4	Serial port A or B interrupt from SIO device, user-configurable.
IRQ5	
IRQ6	Floppy disk.
IRQ7	Parallel Port
IRQ8_L	Active low RTC interrupt.
IRQ9	
IRQ10	
IRQ11	
IRQ12	Mouse interrupt.
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1.
IRQ15	
SMI*	System Management Interrupt. General purpose indicator sourced by the ICH3 and BMC to the processors.
SCI*	System Control Interrupt. Used by system to change sleep states and other system level type functions.

6.5.1.2 Serialized IRQ Support

The server board SE7501BR2 supports a serialized interrupt delivery mechanism. Serialized IRQs (SERIRQ) consists of a start frame, a minimum of 17 IRQ / data channels, and a stop frame. Any slave device in the quiet mode may initiate the start frame. While in the continuous mode, the start frame is initiated by the host controller.

6.5.2 APIC Interrupt Routing

For APIC mode, the SE7501BR2 interrupt architecture incorporates three Intel® I/O APIC devices to manage and broadcast interrupts to local APICs in each processor. One of the APIC is located in the ICH3-S, and the other two APICs are in the P64H2 (1 for each PCI bus). The Intel® I/O APICs monitor each interrupt on each PCI device including PCI slots. When an interrupt occurs, a message corresponding to the interrupt is sent to the processors. The I/O APICs can also supply greater than 16 interrupt levels to the processor(s).

The figure below shows how the interrupts from the embedded devices and the PCI slots are connected.

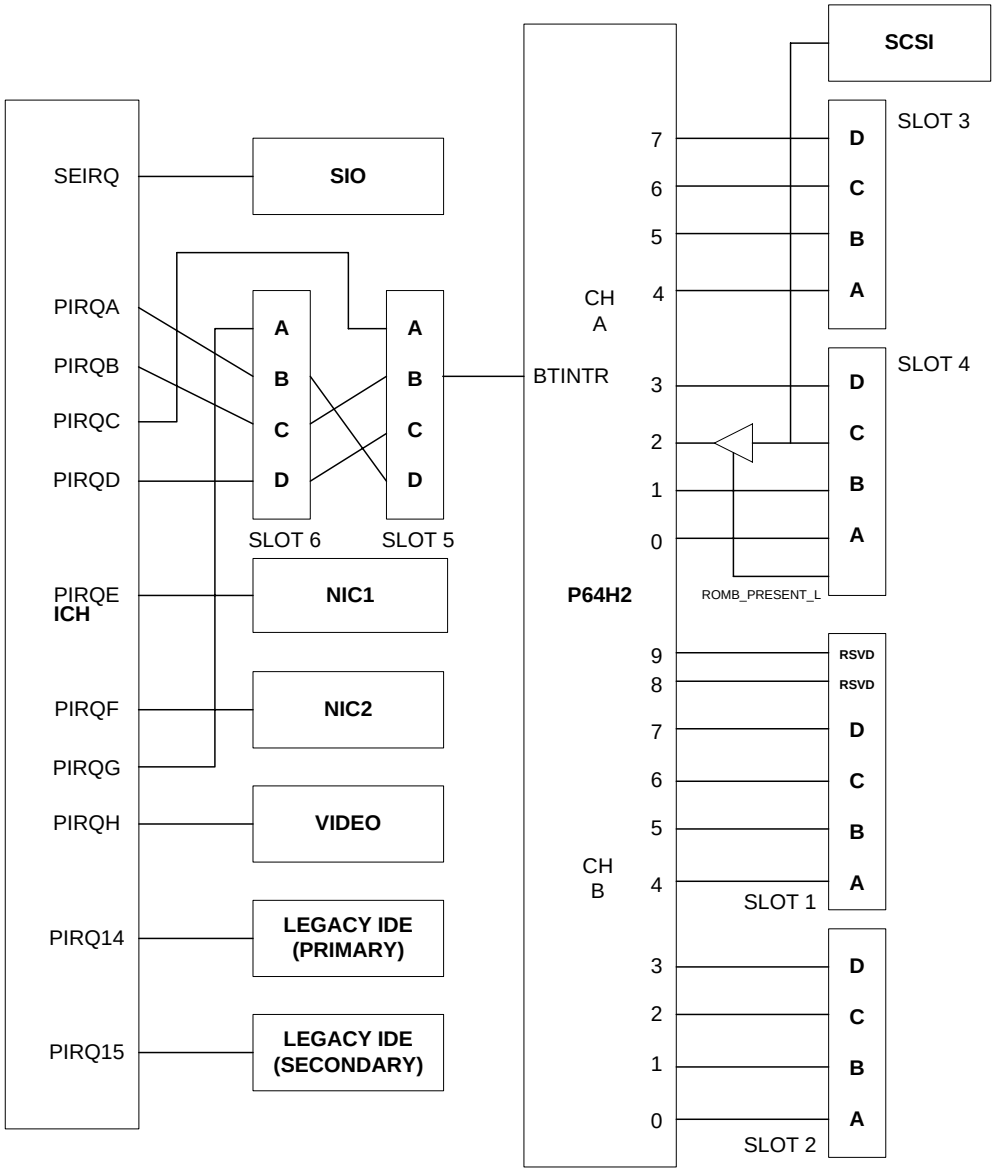

Figure 11. SE7501BR2 Interrupt Routing Diagram

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7. Server Management

The SE7501BR2 server management features are implemented using the Sahalee server board management controller chip. The Sahalee BMC is an ASIC packaged in a 156-pin BGA that contains a 32-bit RISC processor core and associated peripherals. The following diagram illustrates the SE7501BR2 server management architecture.

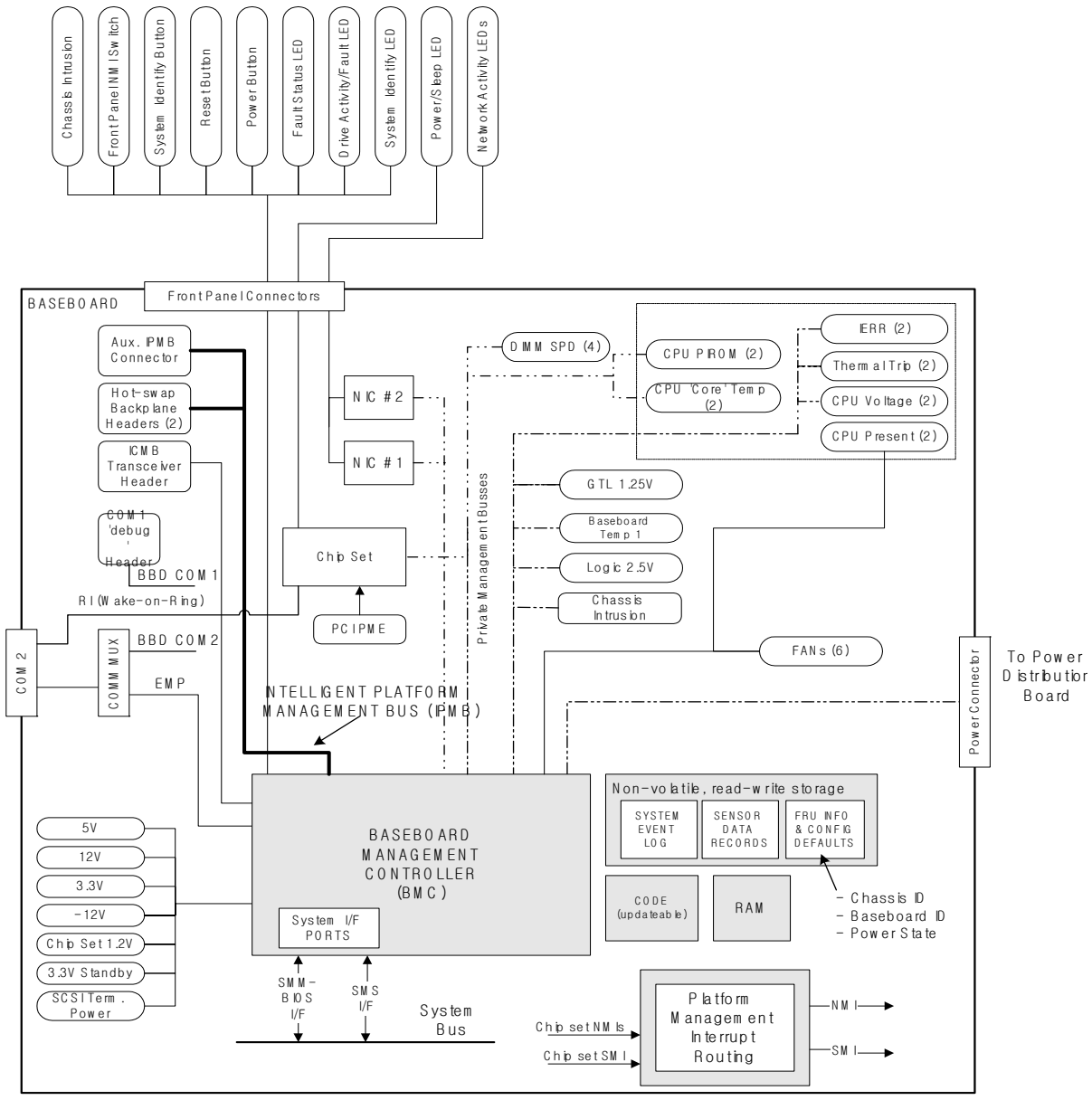

Figure 12. SE7501BR2 Sahalee BMC Block Diagram

7.1 Sahalee Baseboard Management Controller

The Sahalee BMC contains a 32-bit RISC processor core and associated peripherals used to monitor the system for critical events. The Sahalee BMC is packaged in a 156-pin BGA and monitors all power supplies, including those generated by the external power supplies and those regulated locally on the server board. It also monitors SCSI termination voltage, fan tachometers for detecting a fan failure, and system temperature. Temperature is measured on each of the processors and at locations on the server board away from the fans. When any monitored parameter is outside of the defined thresholds, the Sahalee BMC logs an event in the System Event Log.

Management controllers and sensors communicate on the I^2C*-based Intelligent Platform Management Bus (IPMB). Attached to one of its private I^2C bus is Heceta5, an ADM1026, which is a versatile systems monitor ASIC. Some of its features include:

- Analog measurement channels
- Fan speed measurement channels
- General-Purpose Logic I/O pins
- Remote temperature measurement
- On-chip temperature sensor
- Chassis intrusion detect

The following table details the inputs/outputs on the Sahalee BMC as used in SE7501BR2.

Table 20. Sahalee BMC Pin-out

Pin #	Signal Name	Ball	Type	Net Name	Description
1	TDI	B2	Bidir	BMC_TDI	Test Data In
2	TDO	B1	Bidir	BMC_TDO	Test Data Out
3	TRST#	C2	Bidir	BMC_TRST_L	Test Reset
4	TMS	C1	Bidir	BMC_TMS	Test Mode select
5	TCK	D2	Bidir	BMC_TCK	Test clock
6	TEST_MODE_L	D3	Input	PU_BMC_1	Dedicated test mode pin that places Sahalee into production test mode, pulled-up to 3.3Vstandby
7	RST#	D1	Input	BMC_RST_DLY_L	Resets the Sahalee
8	LPCRST#	D4	Input	RST_LPC_BMC_L	LPC bus reset
9	LPCPD#	E2	Input	ICH3_SLP_S1_L	Power down indication
10	LAD(3)	E1	Bidir	LPC_AD<3>	Address Data Bus
11	LAD(2)	E3	Bidir	LPC_AD<2>	Address Data Bus
12	I/O VCC	E4		P3V3_STBY	I/O Power, 3.3V
13	LAD(1)	F2	Bidir	LPC_AD<1>	Address Data Bus
14	LAD(0)	F1	Bidir	LPC_AD<0>	Address Data Bus
15	LFRAME#	F3	Bidir	LPC_FRAME_L	Cycle framing
16	LDRQ#	F4	Bidir	LPC_DRQ_L<0>	DMA_Request
17	SYSIRQ	G2	Bidir	BMC_SYSIRQ	Interrupt
18	LCLK	G1	Input	CLK_33M_BMC	Bus Clock

Pin #	Signal Name	Ball	Type	Net Name	Description
19	Core GND	G4		Ground	Ground
20	Core VCC	H3		P3V3_STBY	Core VCC
21	CS#(1)	G3	Bidir	BMC_SRAM_CE_L	Select line indicating that region 1(external memory-mapping) is active for the current cycle
22	CS#(0)	H1	Bidir	BMC_CS0_L	Select line indicating that region 0(external memory-mapping) is active for the current cycle
23	ADDR(21)	H2	Bidir	BMC_A<21>	Address bit 21, used to clock data into external latch
24	ADDR(20)	H4	Bidir	Not Connected	Address bit 20
25	ADDR(19)	J1	Bidir	BMC_A<19>	Address bit 19
26	ADDR(18)	J3	Bidir	BMC_A<18>	Address bit 18
27	ADDR(17)	J2	Bidir	BMC_A<17>	Address bit 17
28	I/O GND	J4		Ground	Ground
29	ADDR(16)	K1	Bidir	BMC_A<16>	Address bit 16
30	ADDR(15)	K3	Bidir	BMC_A<15>	Address bit 15
31	ADDR(14)	K2	Bidir	BMC_A<14>	Address bit 14
32	ADDR(13)	K4	Bidir	BMC_A<13>	Address bit 13
33	ADDR(12)	L1	Bidir	BMC_A<12>	Address bit 12
34	ADDR(11)	L3	Bidir	BMC_A<11>	Address bit 11
35	ADDR(10)	L2	Bidir	BMC_A<10>	Address bit 10
36	VDD5V	M1	SB5V	P5V_STBY	Standby Power
37	ADDR(9)	M3	Bidir	BMC_A<9>	Address bit 9
38	ADDR(8)	M2	Bidir	BMC_A<8>	Address bit 8
39	ADDR(7)	N1	Bidir	BMC_A<7>	Address bit 7
40	ADDR(6)	N2	Bidir	BMC_A<6>	Address bit 6
41	ADDR(5)	P2	Bidir	BMC_A<5>	Address bit 5
42	I/O VCC	N3		P3V3_STBY	Core VCC
43	ADDR(4)	P3	Bidir	BMC_A<4>	Address bit 4
44	ADDR(3)	N4	Bidir	BMC_A<3>	Address bit 3
45	ADDR(2)	M4	Bidir	BMC_A<2>	Address bit 2
46	ADDR(1)	P4	Bidir	BMC_A<1>	Address bit 1
47	ADDR(0)	L4	Bidir	BMC_A<0>	Address bit 0
48	DATA(15)	N5	Bidir	BMC_D<15>	Data bit 15
49	DATA(14)	P5	Bidir	BMC_D<14>	Data bit 14
50	DATA(13)	M5	Bidir	BMC_D<13>	Data bit 13
51	DATA(12)	L5	Bidir	BMC_D<12>	Data bit 12
52	DATA(11)	N6	Bidir	BMC_D<11>	Data bit 11
53	DATA(10)	P6	Bidir	BMC_D<10>	Data bit 10
54	DATA(9)	M6	Bidir	BMC_D<9>	Data bit 9
55	I/O GND	L6		GND	Ground
56	DATA(8)	N7	Bidir	BMC_D<8>	Data bit 8
57	DATA(7)	P7	Bidir	BMC_D<7>	Data bit 7
58	Core GND	L7		GND	Ground

Pin #	Signal Name	Ball	Type	Net Name	Description
59	Core VCC	M8		P3V3_STBY	Core VCC
60	XTAL2	M7	Output	Not Connected	
61	XTAL1	P8	Input	SIO_CLK_40M_BMC	40MHz Clock Input
62	DATA(6)	N8	Bidir	BMC_D<6>	Data bit 6
63	DATA(5)	L8	Bidir	BMC_D<5>	Data bit 5
64	DATA(4)	P9	Bidir	BMC_D<4>	Data bit 4
65	DATA(3)	M9	Bidir	BMC_D<3>	Data bit 3
66	DATA(2)	N9	Bidir	BMC_D<2>	Data bit 2
67	DATA(1)	L9	Bidir	BMC_D<1>	Data bit 1
68	DATA(0)	P10	Bidir	BMC_D<0>	Data bit 0
69	WE#	M10	Bidir	BMC_WE_L	Write enable signal
70	OE#	N10	Bidir	BMC_OE_L	Output enable
71	I/O VCC	L10		P3V3_STBY	Core VCC
72	REG#	P11	Input	BMC_CPU2_SKTOCC_L	Indicates that CPU2 socket is occupied.
73	CE#(2)	M11	Output	RST_VRM_DIS_L	Disables VCCP VRM
74	CE#(1)	N11	Input	BMC_CPU1_SKTOCC_L	Indicates that CPU1 socket is occupied.
75	SBHE#	P12	Bidir	BMC_SBHE_L	Byte High Enable
76	IOR#	M12	Output	BMC_SECURE_MODE_KB_L	Disable keyboard in Secure Mode
77	IOW#	N12	Input	FP_PWR_BTN_L	Front panel power button control
78	MEMR#	P13	Input	FP_ID_BTN_L	Front panel unit ID button control
79	MEMW#	N13	Input	FP_SLP_BTN_L	Front panel sleep button control
80	BALE	N14	Input	FP_NMI_BTN_L	Assert NMI signal from front panel (diagnostic control)
81	IOCHRDY	M13	Input	FP_RST_BTN_L	Front panel reset button control
82	BW8#	M14	Ouptput	BMC_SLP_BTN_L	Enable sleep function
83	XINT(7)	L13	Bidir	BMC_NMI_L	Assert/monitor NMI signal
84	XINT(6)	L12	Input	BMC_CPU12_PROCHOT_L	High temperature warning indicated from CPU1 and/or CPU2
85	XINT(5)	L14	Input	NIC2_SMBALERT_L	Interrupt Source
86	I/O GND	L11		GND	Ground
87	XINT(4)	K13	Input	NIC1_SMBALERT_L	Interrupt Source
88	XINT(3)	K14	Input	FRB3_TIMER_HALT_L	FRB3 timer disable from Jumper
89	XINT(2)	K12	Input	ICH3_CPU_SLP_L	Sleep initiated from chipset
90	XINT(1)	K11	Input	ICH3_SLP_S5_L	Sleep state S5 initiated from chipset
91	XINT(0)	J13	Input	RST_PWRGD_PS	System reset
92	BAUD	J14	Output	BMC_IRQ_SMI_L	BMC initiated SMI
93	RI#	J12	Input	SPB_RI_L	Ring Indicate Input
94	DTR#(1)	J11	Output	BMC_LATCH_OE_L	External latch enable
95	DCD#(1)	H13	Input	BMC_ICMB_RX	Tied to ICMB_RX
96	CTS#(1)	H14	Input	BMC_FRC_UPDATE_L	BMC Forced Update
97	Core GND	H11		GND	Ground

Pin #	Signal Name	Ball	Type	Net Name	Description
98	Core VCC	G12		P3V3_STBY	Core VCC
99	RTS#(1)	H12	Output	BMC_ICMB_TX_ENB_L	Transmit Enable of ICMB
100	RX(1)	G14	Input	BMC_ICMB_RX	Received data of ICMB
101	TX(1)	G13	Output	BMC_ICMB_TX	Transmit data of ICMB
102	I/O VCC	G11		P3V3_STBY	Core VCC
103	DTR#(0)	F14	Output	BMC_DTR_L	Serial B/EMP port DTR
104	DCD#(0)	F12	Input	BMC_DCD_L	Serial B/EMP port DCD
105	CTS#(0)	F13	Input	BMC_CTS_L	Serial B/EMP port CTS
106	RTS#(0)	F11	Output	BMC_RTS_L	Serial B/EMP port RTS
107	VDD5V	E14		SB5V	Standby 5V
108	RX(0)	E12	Input	BMC_SIN	Serial B/EMP port Rx Data
109	TX(0)	E13	Output	BMC_SOUT	Serial B/EMP port Tx Data
110	TIC4_IN	E11	Input	CLK_32K_RTC	32KHz Clock input from SIO
111	TIC3_OUT	D14	Input	ICH3_SMI_BUFF_L	SMI asserted from chipset
112	TIC2_IN(7)	D12	Schmitt input	FAN8_TACH	Fan tach signal
113	TIC2_IN(6)	D13	Schmitt input	FAN7_TACH	Fan tach signal
114	TIC2_IN(5)	C14	Schmitt input	FAN6_TACH	Fan Tach signal
115	I/O GND	C12		GND	Ground
116	TIC2_IN(4)	C13	Schmitt input	FAN5_TACH	Fan Tach Signal
117	TIC2_IN(3)	B14	Schmitt input	FAN4_TACH	Fan Tach Signal
118	TIC2_IN(2)	B13	Schmitt input	FAN3_TACH	Fan Tach Signal
119	TIC2_IN(1)	A13	Schmitt input	FAN2_TACH	Fan Tach Signal
120	TIC2_IN(0)	B12	Schmitt input	FAN1_TACH	Fan Tach Signal
121	TIC1_OUT	A12	Output	BMC_SPKR_L	Speaker output
122	LSMI#	B11	Output	BMC_SCI_L	BMC generate System Control Interrupt
123	LED(5)	C11	Output	RST_P6_PWRGOOD	Power Good signal to CPUs
124	LED(4)	A11	Output	RST_BMC_PS_PWR_ON_L	Power Supply on/off control
125	LED(3)	D11	Output	BMC_PWR_BTN_L	Power Button output
126	LED(2)	B10	Output	BMC_SPB_OE_L	Serial port B enable
127	LED(1)	A10	Input	G_CPU2_BSEL0	
128	LED(0)	C10	Input	G_CPU1_BSEL0	
129	I/O VCC	D10		P3V3_STBY	I/O Vcc
130	SDA(5)	B9	Schmitt bidir	PB4_I2C_3VSB_SDA	SMB Data/Address for NICs
131	SCL(5)	A9	Schmitt bidir	PB4_I2C_3VSB_SCL	SMB Clock for NICs

Pin #	Signal Name	Ball	Type	Net Name	Description
132	SDA(4)	C9	Schmitt bidir	PB3_I2C_3V_SDA	Private I2C Bus #3 Data/Address to Chipset and Processors
133	SCL(4)	D9	Schmitt bidir	PB3_I2C_3V_SCL	Private I2C Bus #3 Clockto Chipset and Processors
134	SDA(3)	B8	Output	SERIAL_TO_LAN_L	Serial to LAN enable
135	SCL(3)	A8	Output	STPW_EN_L	Onboard SCSI termination enable
136	Core GND	D8		GND	Ground
137	Core VCC	C7		P3V3_STBY	Core VCC
138	SDA(2)	C8	Schmitt bidir	PB1_I2C_5VSB_SDA	Private I2C Bus #1Data /Address to Front panel, SIO, Heceta and Power supply
139	SCL(2)	A7	Schmitt bidir	PB1_I2C_5VSB_SCL	Private I2C Bus #1 Clock to Front panel, SIO, Heceta and Power supply
140	SDA(1)	B7	Schmitt bidir	SMB_I2C_3VSB_SDA	SMB Address
141	SCL(1)	D7	Schmitt bidir	SMB_I2C_3VSB_SCL	SMB Data
142	SDA(0)	A6	Schmitt bidir	IPMB_I2C_5VSB_SDA	IPMB Address
143	I/O GND	C6		GND	Ground
144	SCL(0)	B6	Schmitt bidir	IPMB_I2C_5VSB_SCL	IPMB Data
145	AVDD	D6	Analog power	P3V3_STBY	Analog 3.3 supply
146	A2D(7)	A5	Analog input	Not Connected	
147	A2D(6)	C5	Analog input	CON_TERMPWR_MON	SCSI Terminator Power Monitor
148	A2D(5)	B5	Analog input	Not Connected	
149	A2D(4)	D5	Analog input	Not Connected	
150	A2D(3)	A4	Analog input	Not Connected	
151	A2D(2)	C4	Analog input	Not Connected	
152	A2D(1)	B4	Analog input	Not Connected	
153	A2D(0)	A3	Analog input	Not Connected	
154	VREF	C3	Analog input	BMC_VREF_A_2P5V	Use accurate stable and low noise 2.5 source
155	AVS	B3	Analog ground	GND	analog negative power supply, not connected to substrate
156	AVSUB	A2	Analog ground	GND	Analog negative power supply, connected to substrate

An ADM* 1026 Heceta has been attached to the private I^2C bus for monitoring the system temperature, additional analog voltages, and the voltage identifications bits for both processors. The following table describes these added signals. The ADM 1026 device also provides a PWM (Pulse Width Modulation) for fan speed control.

Table 21. ADM 1026 Input Definition

Pin	Signal Name	Type	Description
3	FAN0/GPIO0	Digital Input	CPU2 VID [0]
4	FAN1/GPIO1	Digital Input	CPU2 VID [1]
5	FAN2/GPIO2	Digital Input	CPU2 VID [2]
6	FAN3/GPIO3	Digital Input	CPU2 VID [3]
9	FAN4/GPIO4	Digital Input	CPU2 VID [4]
10	FAN5/GPIO5	Digital Input	CPU2 IERR
11	FAN6/GPIO6	Digital Input	CPU2 Thermal Trip
12	FAN7/GPIO7	Digital Output	CPU2 disable
2	GPIO8	Digital Input	CPU1 VID [0]
1	GPIO9	Digital Input	CPU1 VID [1]
48	GPIO10	Digital Input	CPU1 VID [2]
47	GPIO11	Digital Input	CPU1 VID [3]
46	GPIO12	Digital Input	CPU1 VID [4]
45	GPIO13	Digital Input	CPU1 IERR
44	GPIO14	Digital Input	CPU1 Thermal Trip
43	GPIO15	Digital Output	CPU1 disable
16	Chassis Intrusion	Digital Input	An active high input which captures a chassis intrusion event in Bit 7 of Status Register 4. This bit will remain set until cleared,
29	VBAT	Digital Input	So long as battery voltage is applied to the VBAT input, even when the ADM1026 is powered off
13	SCL	Digital Input	BMC Private I2C Bus 1 Clock
14	SDA	Digital I/O	BMC Private I2C Bus 1 Data
15	ADDR	Digital Input	I2C Device address select, 0 ohm pull-down to GND
18	PWM	Digital Output	Pulse-width modulated output for control of fan speed. Open drain.
19	RESET_STBY	Digital Output	Power-on Reset. 5 mA driver (open drain), active low output with a 200 ms minimum pulse width. This is asserted whenever 3.3VSTBY is below the reset threshold. It remains asserted for approx. 200ms after 3.3VSTBY rises above the reset threshold.
30	5VIN	Analog Input	Monitors +5 V supply
31	-12VIN	Analog Input	Monitors -12 V supply
32	+12VIN	Analog Input	Monitors +12 V supply
33	+VCCP	Analog Input	Monitors processor core voltage (0 to 3.0 V)
34	AIN7	Analog Input	Monitors +1.2V supply
35	AIN6	Analog Input	Monitors VTT supply
36	AIN5	Analog Input	Monitors +12V VRM supply
37	AIN4	Analog Input	Monitors +1.8V supply
38	AIN3	Analog Input	Monitors +2.5V supply
39	AIN2	Analog Input	Monitors +5V Standby supply
40	AIN1	Analog Input	Monitors +1.8V Standby supply

Pin	Signal Name	Type	Description
41	AIN0	Analog Input	Monitors +3.3V Standby supply
24	VREF	Analog Input	+2.5V analog reference voltage
25	D1-	Analog Input	CPU1 Thermal Diode
26	D1+	Analog Input	CPU1 Thermal Diode
27	D2-	Analog Input	CPU2 Thermal Diode
28	D2+	Analog Input	CPU2 Thermal Diode

7.2 System Reset Control

Reset circuitry on the SE7501BR2 server board looks at resets from the front panel, ICH3-S, ITP, and the processor subsystem to determine proper reset sequencing for all types of resets. The reset logic accommodates several methods to reset the system, which can be divided into the following categories:

- Power-up reset
- Hard reset
- Soft (programmed) reset

The following subsections describe each type of reset.

7.2.1 Power-up Reset

When the system is disconnected from AC power, all logic on the server board is powered off. When a valid input (AC) voltage level is provided to the power supply, 5-volt standby power will be applied to the server board. The baseboard has a 5-volt to 3.3-volt regulator to produce 3.3-volt standby voltage. A power monitor circuit on 3.3-volt standby will assert BMC_RST_L, causing the BMC to reset. The BMC is powered by 3.3 volt standby and monitors and controls key events in the system related to reset and power control.

After the system is turned on, the power supply will assert the RST_PWRGD_PS signal after all voltage levels in the system have reached valid levels. The BMC receives RST_PWRGD_PS and after 500 ms asserts RST_P6_PWRGOOD, which indicates to the processors and ICH3-S that the power is stable. Upon RST_P6_PWRGOOD assertion, the ICH3-S will toggle PCI reset.

7.2.2 Hard Reset

A hard reset can be initiated by resetting the system through the front panel switch. During the reset, the Sahalee BMC de-asserts RST_P6_PWRGOOD. After 500 ms, it is reasserted, and the power-up reset sequence is completed.

Note: The Sahalee BMC is not reset by a hard reset. It is only reset when AC power is applied to the system.

7.2.3 Soft Reset

A soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers. Soft resets can be generated by the keyboard controller located in the SIO, by the ICH3-S, or by the operating system.

7.3 Intelligent Platform Management Buses (IPMB)

Management controllers (and sensors) communicate on the I^2C-based Intelligent Platform Management Bus. A bit protocol, defined by the *I^2C Bus Specification*, and a byte-level protocol, defined by the *Intelligent Platform Management Bus Communications Protocol Specification*, provide an independent interconnect for all devices operating on this I^2C bus.

The IPMB extends throughout the server board and system chassis. An added layer in the protocol supports transactions between multiple servers on Inter-Chassis Management Bus (ICMB) I^2C segments.

SE7501BR2 provides two 4-pin IPMB connectors to support dual Hot-Swap Back Plane (HSBP) configuration. In addition to the "public" IPMB, the Sahalee BMC also has three private I^2C busses. The Sahalee BMC is the only master on the private busses. The following table lists all server board connections to the Sahalee BMC I^2C busses.

Table 22. SE7501BR2 I2C Bus Address Map

I2C Bus	I^2C Addr	Device
Private Bus 1	0x58	Heceta5
	0x60	SIO
	0xAC	Power Distribution Board
	0xA0	Power Supply1
	0xA2	Power Supply2
	0xA4	Power Supply3
Private Bus 3	0x30	CPU1 therm sensor
	0x32	CPU2 therm sensor
	0x44	ICH3-S
	0x60	MCH
	0xA2	DIMM1
	0xA0	DIMM3
	0xA6	CPU1 SEEPROM
	0xAA	DIMM2
	0xA8	DIMM4
	0xAE	CPU2 SEEPROM
	0xC4	P64H2
	0xD2	CK408B
Private Bus 4	0x84	NIC1
	0x86	NIC2

7.4 Inter Chassis Management Bus (ICMB)

The BMC on SE7501BR2 has built in support for ICMB interface. However an optional ICMB card is required to use this feature since the ICMB transceivers are not provided on the board. A five pin ICMB connector on the SE7501BR2 board provides the interface to the ICMB module.

7.5 Error Reporting

This section documents the types of system bus error conditions monitored by the SE7501BR2 board set.

7.5.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors on the SE7501BR2, which can be disabled and enabled individually, can be categorized as follows:

- PCI bus
- Processor bus errors
- Memory single- and multi-bit errors
- General Server Management sensors

On the SE7501BR2 platform, general server management sensors are managed by the Sahalee BMC.

7.5.1.1 PCI Bus Errors

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled in BIOS Setup.

7.5.1.2 Intel® Xeon™ Processor Bus Errors

The MCH supports the data integrity features supported by the Intel Xeon processor system bus, including address, request, and response parity. In addition, the MCH can generate BERR# on unrecoverable errors detected on the processor bus. Unrecoverable errors are routed to an NMI by the BIOS.

7.5.1.3 Memory Bus Errors

The MCH is programmed to generate an SMI on single-bit or double-bit data errors in the memory array if ECC memory is installed. The MCH performs the scrubbing. The SMI handler records the error and the DIMM location to the system event log.

7.5.2 ID LED

The blue “ID LED”, located at the back edge of the baseboard next to the 10/100 NIC connector, is used to help locate a given server platform when the server is installed in a multi-system enclosure. The LED is lit when the front panel ID button is pressed and is turned off when the button is pressed again. The ID LED Front Panel button is available on the SC5200 server chassis rack SKU only. A user-defined interface can be developed to activate the ID LED remotely.

7.5.3 System Status LED

The System Status LED is located on the Front Panel board and can be viewed with the SC5200 front system bezel open or closed. Each LED state is described below.

Table 23. System Status LED

LED Color	LED State	Description
Green	ON	Running. BIOS Initialization complete, boot started / normal operation.
	Blink	Degraded condition
Amber	ON	Critical or Non-Recoverable Condition
	Blink	Non-Critical Condition (e.g. Fan fault)
Off	Off	POST / System Stop.

7.5.3.1 System Status Indications

Critical Condition (Amber LED)

Any critical or non-recoverable threshold crossing associated with the following events:

- Temperature, Voltage, or Fan critical threshold exceeded.
- Power Subsystem Failure. The BMC asserts this failure whenever it detects a power control fault (e.g., the BMC detects that the system power is remaining ON even though the BMC has disserted the signal to turn off power to the system.
  A hot-swap backplane would use the Set Fault Indication command to indicate when one or more of the drive fault status LEDs are asserted on the hot-swap backplane.
- The system is unable to power up due to incorrectly installed processor(s), or processor incompatibility.
- Satellite controller sends a critical or non-recoverable state, via the Set Fault Indication command to the BMC.
- “Critical Event Logging” errors.

Non-Critical Condition (Blinking Amber LED)

- Temperature, Voltage, or Fan non-critical threshold exceeded.
- Chassis Intrusion.
- Satellite controller sends a non-critical state, via the Set Fault Indication command, to the BMC.
- Set Fault Indication Command.

Degraded Condition (Blinking Green LED)

- Non-redundant power supply operation. This only applies when the BMC is configured for a redundant power subsystem. The power unit configuration is configured via OEM SDR records.
- A processor is disabled by FRB or BIOS.
- BIOS has disabled or mapped out some of the system memory.
-

7.5.4 Temperature Sensors

The SE7501BR2 server has the ability to measure the system and board temperature from a variety of sources. The first is located inside the Heceta chip (U5F10) and is used to measure the baseboard temperature. Diodes located inside each processor are used by the SE7501BR2 to monitor the temperature at the processors.

When the SE7501BR2 board is integrated into an Intel SC5200 server chassis, the server board will also monitor temperature sensors on the front panel and Hot Swap Backplanes to measure the ambient temperature. If the ambient temperature is determined by the BMC to be too high, the BMC will boost the speed of the system fans.

Table 24. Temperature Sensors

Temperature Sensor	Description	Resolution	Accuracy	Location
Server board	Server board temperature sensor, Located in hot-spot selected accoring to thermal design	8-bit	+/- 3°C or better	U5F10
Primary Processor	Primary processor socket thermal sensor	8-bit	+/- 5°C or better	J8H8
Secondary Processor	Secondary processor socket thermal sensor	8-bit	+/- 5°C or better	J6H8

7.5.5 BMC Diagnostics and Beep Code Generation

The BMC generates beep codes upon detection of the failure conditions listed in the following table. Each digit in the code is represented by a sequence of beeps whose count is equal to the digit.

Table 25. BMC Beep Code

Code	Reason for Beep
1	Front panel CMOS clear initiated
1-5-1-1	FRB failure (processor failure)
1-5-2-1	No processors installed or processor socket 1 is empty.
1-5-2-3	Processor configuration error (e.g., mismatched VIDs, Processor slot 1 is empty)
1-5-2-4	Front-side bus select configuration error (e.g., mismatched BSELs)
1-5-4-2	Power fault: DC power unexpectedly lost (e.g. power good from the power supply was deasserted)
1-5-4-3	Chipset control failure
1-5-4-4	Power control failure (e.g., power good from the power supply did not respond to power request)

Note: For BIOS beep codes, which do not follow the 1-5-x-x format, refer to section 9.11.2 POST Error Beep Codes.

8. System BIOS

This section describes the BIOS-embedded software for the server board SE7501BR2. This section also describes BIOS support utilities that are required for system configuration (ROM resident) and flash ROM update (not ROM resident). The BIOS contains standard PC-compatible basic input/output (I/O) services and standard Intel® server features.

The BIOS is implemented as firmware that resides in the flash ROM. Support for applicable baseboard peripheral devices (SCSI, NIC, video adapters, etc.) that are also loaded into the baseboard flash ROM are not specified in this document. Hooks are provided to support adding BIOS code for these adapters. The binaries for these must be obtained from the peripheral device manufacturers and loaded into the appropriate locations.

8.1 System Flash ROM Layout

The flash ROM contains system initialization routines, the BIOS Setup Utility, and runtime support routines. The exact layout is subject to change, as determined by Intel. A 16 KB user block is available for user ROM code or custom logos. A 96 KB area is used to store the string database. The flash ROM also contains initialization code in compressed form for on-board peripherals, like SCSI and video controllers.

The complete ROM is visible, starting at physical address 4 GB minus the size of the flash ROM device. The Flash Memory Update utility loads the BIOS image minus the recovery block to the flash.

Because of shadowing, none of the flash blocks is visible at the aliased addresses below 1 MB.

A 16 KB parameter block in the flash ROM is dedicated to storing configuration data that controls the system configuration (ESCD) and the on-board SCSI configuration. Application software must use standard APIs to access these areas; application software cannot access the data directly.

8.2 Memory

The following is a list of memory specifications that the system BIOS supports:

- Only registered DDR266 registered ECC memory is supported. When populated with more than 4 GB of memory, the memory between 4 GB and 4 GB minus 256 MB is remapped and may not accessible for use by the operating system and may be lost to the user. This area is reserved for the BIOS, for APIC configuration space, for PCI adapter interface, and for virtual video memory space. This memory space is also remapped if the system is populated with memory configurations between 3.75 GB and 4 GB.
- The system BIOS supports registered DIMMs with CL=2.5 components and CL=2 components.
- The baseboard is hard-wired for dual memory channel architecture via 4 DIMM sockets distributed across two memory banks.

- The system BIOS supports only ECC memory. Single-bit errors are corrected and multiple-bit errors are detected. When utilizing x4 DIMMs, the board supports Intel(R) x4 Single Device Data Correction (x4 SDDC).
- DIMMs within a bank must be identical, each memory bank can have different size DIMMs. Memory timing defaults to the slowest DIMM.

All DIMMs must use SPD EEPROM to be recognized by the BIOS. Mixing vendors of DIMMs is supported but it is not recommended because the system defaults to the slowest speed that will work with all of the vendors' DIMMs.

8.2.1 Memory Sizing and Initialization

During POST, the BIOS tests and sizes memory, and configures the memory controller. The BIOS determines the operational mode of the MCH based on the number of DIMMS installed and the type, size, speed, and memory attributes found on the on-board EEPROM or serial presence detect (SPD) of each DIMM.

The memory system is based on rows. Since the server board SE7501BR2 supports a dual memory architecture, DIMMs must be populated in pairs. This means two DIMMs are required to constitute a row. Although DIMMs within a row must be identical, the BIOS supports various DIMM sizes and configurations allowing the rows of memory to be different. Memory sizing and configuration is guaranteed only for DIMMs listed on the Intel tested memory list.

The memory-sizing algorithm determines the size of each row of DIMMs. The BIOS tests extended memory according to the option selected in the BIOS Setup Utility. The total amount of configured memory can be found using INT 15h, AH = 88h;[12] INT 15h, function E801h;[13] or INT 15h, function E820h.[14]

The BIOS creates a hole just below 4 GB to accommodate the system BIOS flash, APIC memory, and memory-mapped I/O located on PCI devices. The size of this hole depends upon the number of PCI cards and the memory mapped resources requested by them. It is typically less than 128 MB.

8.2.2 ECC Initialization

Because only ECC memory is supported, the BIOS must to initialize all memory locations before using them. The BIOS uses the auto-initialize feature of the MCH to initialize ECC.

Note: ECC memory initialization cannot be aborted and may result in a noticeable delay depending on the amount of memory in the system.

[12] INT 15h, AH=88h can report a maximum of 64 MB of contiguous memory.

[13] INT 15h, function E801h can report a maximum of 4096 MB of contiguous memory.

[14] INT 15h, function E820h can report up to 2^{65} –1 bytes of memory including non-contiguous memory regions.

8.2.3 Memory Remapping

During POST memory testing, the detection of single-bit and multi-bit errors in DRAM banks is enabled. If a single-bit error is detected, a single DIMM number will be identified. If a multiple-bit error is detected, a bank of DIMMs will be identified.[15] The BIOS logs all memory errors into the system event log (SEL).

If an error is detected, the BIOS will reduce the usable memory so that the byte containing the error is no longer accessible. This prevents a single-bit error (SBE) from becoming a multi-bit error (MBE) after the system has booted, and prevents SBEs from being detected and logged each time the failed location(s) are accessed. This is done automatically by the BIOS during POST. User intervention is not required.

Memory remapping can occur during base memory testing or during extended memory testing. If remapping occurs during the base memory testing, the SEL event is not logged until after the BIOS remaps the memory and successfully configures and tests 8 MB of memory. In systems where all memory is found to be unusable, only the BIOS beep codes indicate the memory failure. Once the BIOS locates a functioning bank of memory, remapping operations and other memory errors are logged into the SEL and reported to the user at the completion of POST.

8.3 Processors

The BIOS determines the processor stepping, cache size, etc through the CPUID instruction. The requirements are as follows:

- Only Intel® Xeon™ processors with 512KB L2 Cache in a FC-mPGA2P or INT3-mPGA package are supported
- All processors in the system must operate at the same frequency and have the same cache sizes. No mixing of product families supported
- Processors run at a fixed speed and cannot be programmed to operate at a lower or higher speed

8.4 Extended System Configuration Data (ESCD), Plug and Play (PnP)

The system BIOS supports industry standards for making the system Plug-and-Play ready: Refer to the following reference documents:

- *Advanced Configuration and Power Interface Specification*
- *PCI Local Bus Specification*
- *PCI BIOS Specification*
- *System Management BIOS Reference Specification*

[15] The BIOS reduces the memory size if either single-bit or multi-bit errors are detected during memory tests. Since BIOS does not “correct” either error (only reduces memory size to avoid the failing location,) both types of errors are reported as “Uncorrectable ECC” errors in the SEL. Note that single bit errors will be reported as “Correctable ECC” errors when found and corrected at “runtime.”

In addition, refer to the relevant sections of the following specifications:

- *Extended System Configuration Data Specification*
- *Plug and Play ISA Specification*
- *Plug and Play BIOS Specification*

8.4.1 Resource Allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Intel servers. The BIOS scans for the following, in order:

1. ISA devices: Although add-in ISA devices are not supported on these systems, some standard PC peripherals may require ISA-style resources. Resources for these devices are reserved as needed.

2. Add-in video graphics adapter (VGA) devices: If found, the BIOS initializes and allocates resources to these devices.

3. PCI devices: The BIOS allocates resources according to the *PCI Local Bus Specification*, Revision 2.2 and *PCI –X Addendum to the PCI Local Bus Specification, Revision 1.0a*.

The system BIOS Power-on Self Test (POST) guarantees there are no resource conflicts prior to booting the system. Note that PCI device drivers must support sharing IRQs, which should not be considered a resource conflict. Only four legacy IRQs are available for use by PCI devices. Therefore, most of the PCI devices share legacy IRQs. In SMP mode, the I/O APICs are used instead of the legacy “8259-style” interrupt controller. There is very little interrupt sharing in SMP mode.

8.4.2 PnP ISA Auto-Configuration

The system BIOS does the following:

- Supports relevant portions of the *Plug and Play ISA Specification*, Revision 1.0a and the *Plug and Play BIOS Specification*, Revision 1.0A.
- Assigns I/O, memory, direct memory access (DMA) channels, and IRQs from the system resource pool to the embedded PnP Super I/O device.
- Does not support add-in PnP ISA devices.

8.4.3 PCI Auto-Configuration

The system BIOS supports the INT 1Ah, AH = B1h functions, in conformance with the *PCI Local Bus Specification*, Revision 2.1. The system BIOS also supports the 16- and 32-bit protected mode interfaces as required by the *PCI BIOS Specification*, Revision 2.1.

Beginning at the lowest device, the BIOS uses a “depth-first” scan algorithm to enumerate the PCI buses. Each time a bridge device is located, the bus number is incremented and scanning continues on the secondary side of the bridge until all devices on the current bus are scanned.

The BIOS then scans for PCI devices using a “breadth-first” search. All devices on a given bus are scanned from lowest to highest before the next bus number is scanned.

The system BIOS POST maps each device into memory[16] and/or I/O space, and assigns IRQ channels as required. The BIOS programs the PCI-ISA interrupt routing logic in the chipset hardware to steer PCI interrupts to compatible ISA IRQs.

The BIOS dispatches any option ROM code for PCI devices to the DOS compatibility hole (C0000h to E7FFFh[17]) and transfers control to the entry point. Because the DOS compatibility hole is a limited resource, system configurations with a large number of PCI devices may encounter a shortage of this resource. If the BIOS runs out of option ROM space, some PCI option ROMs are not executed and a POST error is generated. The scanning of PCI option ROMs can be controlled on a slot by slot basis in BIOS setup.

Drivers and/or the operating system can detect installed devices and determine resource consumption using the defined PCI, legacy PnP BIOS, and/or ACPI BIOS interface functions.

8.5 NVRAM API

The non-volatile RAM (NVRAM) API and the PCI data records are not supported by the system BIOS. The configuration information of the PCI devices is stored in ESCD.

8.6 Legacy ISA Configuration

Legacy ISA add-in devices are not supported.

8.7 Automatic Detection of Video Adapters

The BIOS detects video adapters in the following order:

1. Off-board PCI
2. On-board PCI

The on-board (or off-board) video BIOS is shadowed, starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to off-board devices.

8.8 Keyboard / Mouse Configuration

The BIOS will support a mouse and a keyboard via the two PS/2 connectors. The devices are detected during POST and the KBC is programmed accordingly.

8.8.1 Boot without Keyboard and/or Mouse

The system can boot with or without a keyboard and/or mouse. Setup does not include an option to disable them. The presence of the keyboard and mouse is detected automatically during POST, and, if present, the keyboard is tested. The BIOS displays the message

[16] The BIOS does not support devices behind PCI-to-PCI bridges that require mapping to the first 1 MB of memory space due to PCI architectural limitations (refer to the *PCI-to-PCI Bridge Architecture Specification*).

[17] Note that the BIOS size may increase thereby limiting the area used by option ROMs to 0C0000h – 0E0000h.

"Keyboard Detected" if it detects a keyboard during POST and it displays the message "Mouse Initialized" if it detects a mouse during POST. The system does not halt for user intervention on errors if either the keyboard or the mouse is not detected[18].

8.9 Floppy Drives

The SE7501BR2 server BIOS supports floppy controllers and floppy drives that are compatible with IBM* XT/AT standards. Most floppy controllers have support for two floppy drives although such configurations are rare. At a minimum, the SE7501BR2 BIOS supports 1.44 MB and 2.88 MB floppy drives. LS-120 floppy drives are attached to the IDE controller and are covered elsewhere.

The BIOS does not attempt to auto-detect the floppy drive because there is no reliable algorithm for detecting the floppy drive type if no media is installed. The BIOS auto-detects the floppy media if the user specifies the floppy drive type through setup.

See Table 26 below for details on various floppy types supported by each floppy drive. The 1.25/1.2 MB format is primarily used in Japan. 1.25/1.2 MB floppies use the same raw media as the 1.44 MB floppies, but must be read using 3-mode drives. In order to access the 1.25/1.2 MB floppies, the BIOS must change the spindle speed to 360 rpm. Please note that the 1.44 MB media uses spindle speed 300 RPM. The DENSSEL (density select) pin on a 3-mode floppy drives selects the spindle speed. The spindle rotates at 300 RPM when DENSSEL signal is high. The BIOS sets the spindle speed to match the media.

Table 26. Allowed Combinations of Floppy Drive and Floppy Media

Floppy Drive	Floppy Format	Note
1.44 MB (3 mode)	1.25 MB (Toshiba*) 1.25 MB (NEC* PC98) 1.44 MB	Floppies formatted under 1.25 MB NEC PC98 format require a special driver. The BIOS has native support for 1.25 MB Toshiba format.
1.44 MB (ordinary)	1.44 MB	DENSEL pin is ignored by these floppy drives
2.88 MB (3 mode)	1.25 MB (Toshiba) 1.25 MB (NEC PC98) 1.44 MB 2.88 MB	Floppies formatted under 1.25 MB NEC PC98 format require special driver. The BIOS has native support for 1.25 MB Toshiba format
2.88 MB (ordinary)	1.44 MB 2.88 MB	The DENSEL pin is ignored by these floppy drives

The BIOS provides a setup option to disable the floppy controller. In addition, some platforms support the 3-mode floppy BIOS extension specification, revision 1.0. This specification defines a 32-bit protected mode interface that can be invoked from a 32-bit operating system.

Note: The recovery BIOS requires a 1.44 MB media in a 1.44 MB floppy drive or LS-120 drive.

[18] IRQ 12 is not available for other devices if a mouse is not present.

8.10 Universal Serial Bus (USB)

The SE7501BR2 server BIOS supports USB keyboard, mouse and boot devices. The SE7501BR2 server platform contains three USB host controllers. Each host controller includes the root hub and two USB ports. Five ports are available in the SE7501BR2 board. During POST, the BIOS initializes and configures the root hub ports and looks for a keyboard, mouse, boot device, and the USB hub and enables them.

Note: Legacy USB must be enabled in BIOS Setup for Keyboard and mouse devices to operate.

The BIOS implements legacy USB keyboard support. USB legacy support in BIOS translates commands that are sent to the PS/2 devices into the commands that USB devices can understand. It also makes the USB keystrokes and the USB mouse movements appear as if they originated from the standard PS/2 devices.

The emulation is transparent to the software. It is accomplished by trapping accesses to the PS/2 keyboard controller port and redirecting them to the appropriate USB device as a USB command. Legacy support is required if the system does not contain a PS/2 keyboard and mouse. BIOS support is not meant to replace a USB driver but will enable the system to allow the USB driver to control these devices.

The PS/2 keyboard/mouse port is considered the primary connection for these input devices. USB ports are treated as a contingency. Use of legacy USB emulation is not encouraged for the following reasons.

- USB legacy support involves many SMIs and slows the POST and operating system loader.
- It is possible to breach system security with a USB keyboard and mouse. Security features are covered in Section 8.16.

8.11 BIOS Supported Server Management Features

The SE7501BR2 server BIOS supports many standards-based server management features and several proprietary features. The Intelligent Platform Management Interface (IPMI) is an industry standard that defines standardized abstracted interfaces to platform management hardware. The SE7501BR2 server BIOS supports version 1.5 of the IPMI specification. The BIOS also implements many proprietary features that are allowed by the IPMI specification, but which are outside of the scope of the IPMI specification.

This section describes the implementation of the standard and the proprietary features including console redirection, the Emergency Management Port (EMP), Service Partition boot, Direct Platform Control over the serial port, Platform Event Paging and Filtering. The BIOS owns console redirection over a serial port, but plays only a minimal role in Platform Event Paging and Filtering.

8.11.1 Console Redirection

The BIOS supports redirection of both video and keyboard via a serial link (Serial A or Serial B). When console redirection is enabled, the local (host server) keyboard input and video output are passed both to the local keyboard and video connections, and to the remote console via the

serial link. Keyboard inputs from both sources are valid and video is displayed to both outputs. As an option, the system can be operated without a keyboard or monitor attached to the host system and run entirely from the remote console. Setup and any other text-based utilities can be accessed through console redirection.

8.11.2 Keystroke Mappings

For keys that have a 7-bit character ASCII mapping, such as A and Ctrl-A, the remote system sends the ASCII character. For keys that do not have an ASCII mapping, such as F1 and Alt-A, the remote system must send a string of characters. This character string is a function of the terminal emulation supported by the BIOS. There are two non-overlapping terminal emulation systems supported simultaneously by Intel BIOS. These are known as VT100+ and a PC-ANSI.

Microsoft* prescribes a terminal emulation that they call VT100+ for use with Microsoft systems. Microsoft Windows systems will interpret input <ESC> sequences and other character sequences using this terminal emulation interpretation. The VT100+ terminal emulation is based upon the behavior of the DEC* VT100 terminal and its keyboard character sequences.

Another common terminal emulation, different from VT100+, is called PC-ANSI. The PC-ANSI terminal emulation is also based on the DEC VT100 terminal behavior. However, it maps its function keys, and other auxiliary (non-alpha-numeric-symbol) keys such as Page Up, Page Down, etc using different character sequences than the Microsoft defined VT100.

The BIOS will accept input simultaneously from either a VT100+ or a PC-ANSI terminal emulation. Because the differences in these two terminal emulations occur only in specific input key sequences, and not in output sequences and positioning data, this is possible. In addition, the different input key sequences do not reuse any of the same sequences for different things. Therefore, it is possible to accept and recognize the F1 key press by either the VT100+ sequence for this event, or the PC-ANSI sequence for this event. The BIOS will accept either encoding, in something of a “super” VT100+/PC-ANSI terminal emulation. This input character mapping is given in Table 27.

Table 27. Non-ASCII Key Mappings

Key	PC-ANSI	VT100+	Shift	Ctrl	Alt
ESC	^[	^[	NS	NS	NS
F1	<ESC>OP	<ESC>1	NS	NS	NS
F2	<ESC>OQ	<ESC>2	NS	NS	NS
F3	<ESC>OR	<ESC>3	NS	NS	NS
F4	<ESC>OS	<ESC>4	NS	NS	NS
F5	<ESC>OT	<ESC>5	NS	NS	NS
F6	<ESC>OU	<ESC>6	NS	NS	NS
F7	<ESC>OV	<ESC>7	NS	NS	NS
F8	<ESC>OW	<ESC>8	NS	NS	NS
F9	<ESC>OX	<ESC>9	NS	NS	NS
F10	<ESC>OY	<ESC>0	NS	NS	NS
F11	<ESC>OZ	<ESC>!	NS	NS	NS
F12	<ESC>O1	<ESC>@	NS	NS	NS
Print Screen	NS	NS	NS	NS	NS

Key	PC-ANSI	VT100+	Shift	Ctrl	Alt
Scroll Lock	NS	NS	NS	NS	NS
Pause	NS	NS	NS	NS	NS
Insert	<ESC> [L	<ESC>+	NS	NS	NS
Delete	(7Fh)	<ESC>-	NS	NS	NS
Home	<ESC> [H	<ESC>h	NS	NS	NS
End	<ESC> [K	<ESC>k	NS	NS	NS
Pg Up	<ESC> [M	<ESC>?	NS	NS	NS
Pg Down	<ESC> [2J	<ESC>/	NS	NS	NS
Up Arrow	<ESC> [A	<ESC>[A	NS	NS	NS
Down Arrow	<ESC> [B	<ESC>[B	NS	NS	NS
Right Arrow	<ESC> [C	<ESC>[C	NS	NS	NS
Left Arrow	<ESC> [D	<ESC>[D	NS	NS	NS
Tab	(09h)	^I	NS	NS	NS
Shift Modifier		<ESC>^S			
Alt Modifier	<ESC>}	<ESC>^A			
Ctrl Modifier		<ESC>^C			

Notes:
NS = Not supported
(xxh) = ASCII character xx

Table 28. ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
Backspace (^H)	(08h)	(08h)	(7Fh)	<ESC>}(08h)
(accent) `	`	(tilde) ~	NS	<ESC>}`
1	1	!	NS	<ESC>}1
2	2	@	NS	<ESC>}2
3	3	#	NS	<ESC>}3
4	4	$	NS	<ESC>}4
5	5	%	NS	<ESC>}5
6	6	^	NS	<ESC>}6
7	7	&	NS	<ESC>}7
8	8	*	NS	<ESC>}8
9	9	(	NS	<ESC>}9
0	0	)	NS	<ESC>}0
(dash) -	-	(under) _	(1Fh)	<ESC>}-
=	=	+	NS	<ESC>}=
a to z	a to z	A to Z	(01h) to (1Ah)	<ESC>}a to <ESC>}z
[	[	{	(1Bh)	<ESC>}[
]	]	}	(1Dh)	<ESC>}]
\	\	|	(1Ch)	<ESC>}\
(semi-colon) ;	;	(colon) :	NS	<ESC>};
(apostrophe) '	‘	(quote) "	NS	<ESC>}'
(comma) ,	,	<	NS	<ESC>},

Key	Normal	Shift	Ctrl	Alt
(period) .	.	>	NS	<ESC>}.
/	/	?	NS	<ESC>}/
(space)	(20h)	(20h)	(20h)	<ESC>}(20h)
(carriage return or ^M)	(0Dh)			

Notes:
NS = Not supported
(xxh) = ASCII character xx

8.11.3 SOL (Serial over LAN)

The text based console redirection is also supported over the Serial Over LAN (SOL) protocol. SOL is built on top of the IPMI-over-LAN infrastructure specified in the IPMI v1.5 specification. When the SOL feature is activated by establishing a LAN connection to the BMC and activating the SOL to be enabled, the EMP-based connectivity is disabled.

The BMC uses the UDP datagrams to send SOL character data as “SOL Messages”. The “SOL Messages” packet format follows that used for IPMI-over-LAN with extensions to support SOL Messages as a new message type. SOL requires the support of VT/UTF-8 character set specified in the Windows .Net* headless requirements from Microsoft. The application displaying SOL data must be VT/UTF-8 aware. The console sends keystrokes in a UDP packet to the server.

The BIOS follows the same path as specified in section 2.3.2 of the Alliance BIOS Specification 2.0 for IPMI based redirection. The BIOS looks at the session ID from the boot information parameters. The BMC has a SOL status command to notify BIOS whether there is a valid SOL session and with a Session ID.

If the session ID of SOL matches with session ID in boot Block info, then BIOS starts serial based redirection services. If the Session IDs do not match, the BIOS follows the path specified in the IPMI section and launches LAN or serial console redirection services.

8.11.4 Terminal Type (VT-UTF8) Support

In addition to the character sets and encoding, data terminals have certain operating characteristics that are dependent on hardware (or emulation) implementation. These include character color and background color, special function keys, cursor positioning, and special display attributes such as “blink” and “high intensity” (“bold”). These are typically controlled (speaking from the server end) on output, and represented in input, by escape sequences, i.e. by multi-character groupings usually beginning with the ESC character.

Fortunately, there are only two major sets of terminal controls to be dealt with in this respect, and most of their escape sequences for positioning and color and attributes are standardized as “ANSI control sequences”, originally based on the DEC VT100 terminals. In general, only non-character keys present different escape sequences.

There are four distinct terminal types, with different combinations of controls, character sets, and codesets:

- There are the “VT100” terminal type and its superset “VT100+” terminal type, derived from the early DEC VT100 video terminals. These terminal types are used most

commonly by the Unix/Linux server community. They differ in that the VT100 does not support color codes or VT100+ function key definitions. The implementation Intel supports uses the 7-bit ASCII character set and codeset.

- Another major type is the “PC-ANSI” terminal, which is essentially an emulation of the PC keyboard and display under DOS, with the use of VT100-type display controls but a different representation for non-character keys. This terminal type is primarily used for servers running Windows*, NetWare*, and other PC-derived server operating systems. It supports the PC-ANSI character set and codeset with multi-language characters and special characters.
- The VT-UTF8 terminal type uses VT100+ display controls and VT100+ non-character key representations, but uses the UFT8 Unicode codeset. This is the new standard recommended by Windows.NET, and required by WHQL for server BIOS. The Intel implementation supports the PC-ANSI character set as a subset within the Unicode character set, using UTF8 Unicode encoding.

8.11.5 Limitations

Console redirection is a real-mode BIOS extension. It does not operate outside of real mode. In addition, console redirection will not function if the operating system or a driver, such as EMM386*, takes the processor into protected mode. If an application moves the processor in and out of protected mode, it should inhibit redirection before entering protected mode and restart redirection when it returns to real mode.

Video is redirected by scanning and sending changes in text video memory. Therefore, console redirection is unable to redirect video in graphics mode. Since the BIOS scans the text video memory, an additional limitation exists if the system does not contain a video graphics adapter or a proprietary means of buffering the video memory. The BIOS may not have a method to send changes in text video memory if an application such as an option ROM writes directly to video memory.

Keyboard redirection operates through the use of the BIOS INT 16h handler. Software bypassing this handler does not receive redirected keystrokes.

8.11.6 Emergency Management Port (EMP)

The SE7501BR2 server board has two serial ports; Serial A (COM1) available on the rear DB9 connector, and Serial B (COM2) available off on-board 9-pin header which can be cabled to front or rear. The Serial B port (COM2) can be used for both the emergency management port and for a modem use. The SE7501BR2 provides communication between Serial port B and the BMC. The BMC controls a multiplexer that determines if the external Serial B (COM2) connector is electrically connected to the BMC or to the standard serial port of the Super I/O.

8.11.6.1 Interaction with BIOS Console Redirection

Additional features are available if BIOS console redirection is enabled on the same serial port as the Emergency Management Port, and the EMP mode is set to “Always active” or “Preboot.”

BIOS console redirection supports an extra control escape sequence to force the serial port to the BMC. After this command is sent, the Serial B port attaches to the BMC Emergency Management Port serial port and the Super I/O Serial B data is ignored. This feature allows a remote user to monitor the status of POST using the standard BIOS console redirection features

and then takes control of the system reset or power using the Emergency Management Port features. If a failure occurs during POST, a watchdog time-out feature in the BMC automatically takes control of the Serial B port.

The character sequence that switches the multiplexer to the BMC serial port is “ESC O 9”. This is also denoted as ^[O9. This key sequence is above the normal ANSI function keys and will not be used by an ANSI terminal.

One restriction of using the same serial port for both the Emergency Management Port and BIOS console redirection is that console redirection must be set up to CTS/RTS for direct connection and to CTS/RTS+CD for a modem connection. Both the Emergency Management Port and console redirection assume N, 8, 1 mode. The BIOS redirection and the Emergency Management Port can work at different baud rates by using the auto baud feature of the modem.

8.11.7 Service Partition Boot

The SE7501BR2 server BIOS supports a Service Partition boot. The Service Partition is installed as a separate file system partition on one of the local hard drives. It hosts the DOS operating system, the System Setup Utility, and diagnostics agents and tests. The Service Partition communicates with remote console applications, and it can transfer files between the Service Partition over the LAN, serial port, or a modem.

The BIOS provides setup options to configure the Service Partition type (the default is 98h), and the option for enabling and disabling the Service Partition boot. A remote agent can direct the BMC firmware to set the Service Partition boot request and reboot the system.

Upon rebooting, the system BIOS checks for a Service Partition boot request. On finding a boot request, the system searches for the Service Partition type starting from the highest disk number in the scan order. If a Service Partition is found, the system boots from it. The drive containing the Service Partition becomes the C: drive.

The drive numbers of all other drives are incremented by one, except for the drive that has a scan order that is higher than the Service Partition drive. The BIOS can be directed by the user to perform a one-time boot from the Service Partition. The Service Partition is serviced once per request. The Service Partition boot option is disabled upon each boot attempt.

The BIOS considers a Service Partition boot as a continuation of the BIOS POST. The BIOS does not hide the serial port that is used by console redirection or the Emergency Management Port if it is booting to the Service Partition. The state of all Emergency Management Port functionality remains in the same state as in POST. The state of Pre-Boot and Always-Active EMP mode also do not change. The Service Partition is always scanned for presence, even if Service Partition booting is inactive.

The BIOS sets the watchdog timer inside the BMC while it is attempting to boot from a Service Partition. This timer is reset upon booting of the Service Partition by an application. If the system hangs on booting, a reset brings the system out of the Service Partition boot and an error is logged.

The BIOS starts serial console redirection on a Service Partition boot. Console redirection is turned on with Serial B, 19200 baud. Any reboot after a Service Partition boot reverts to the

previous settings of Serial Console Redirection. For example, if console redirection was turned off before the service boot, it reverts to disabled.

Note: The “F4 Boot to Service Partition” prompt is displayed on the screen on the second boot after proper installation and configuration with the Service Partition Administrator.

8.12 Microsoft Windows* Compatibility

The SE7501BR2 server board is compliant with the *Hardware Design Guide v3.0*.

The Hardware Design Guide (HDG) for a Windows NT platform is intended for systems that are designed to work with Windows NT class operating systems. Each specification classifies the systems further and has different requirements based on the intended usage for that system. For example, a server system used in small home/office environments has different requirements than one that is used for enterprise applications.

The SE7501BR2 server BIOS meets the applicable requirements as specified in version 3.0 of the HDG specification for the basic server class.

8.12.1 Quiet Boot

Version 3.0 of the Hardware Design Guide for Windows NT requires that the BIOS provide minimal startup display during BIOS POST. The system start-up must only draw the user’s attention in case of errors or when there is a need for user interaction. By default, the system must be configured so the screen display does not display memory counts, device status, etc, but presents a "clean" BIOS start-up. The only screen display allowed is the OEM splash screen, which can include information such as copyright notices.

The SE7501BR2 server BIOS supports the <ESC> and <F2> hot-keys during POST, giving the user the ability to temporarily disable the splash screen to view all diagnostic and initialization messages for the current boot. The BIOS displays a message about the hot-keys below the splash screen, at the bottom of the display.

The splash screen can be disabled for all subsequent boot up sequences by going into the BIOS setup utility and enabling the “Boot-time Diagnostic Screen” option found under the “Advanced” menu. The Boot-time Diagnostic option is enabled by BIOS when using BIOS console redirection, since it cannot redirect the video if configured for graphics mode.

If the Service Partition boot is enabled, the BIOS turns off the splash screen for that boot and restores it during subsequent, normal boots. The BIOS may temporarily remove the splash screen when the user is prompted for a password during POST. The BIOS also allows an OEM to override the standard Intel splash screen with a custom one.

The SE7501BR2 BIOS maintains the splash screen during option ROM initialization. Since option ROMs expect the video to be in text mode, the BIOS emulates text mode. The BIOS remembers the Int 10 calls made by the option ROMs and displays the option ROM screen if the user presses the <Esc> key. The ROM screen is restored if the BIOS detects any key combination that includes the <Ctrl> or <Alt> key during option the ROM scan. This is because many option ROMs use one of these key combinations to enter setup.

The SE7501BR2 BIOS displays a progress meter at the top of the screen. This meter provides a visual indication of percentage of POST completed. The BIOS measures the amount of time required for completing POST during every boot and uses that information to update the progress meter during the next boot.

Note: If the "Extended Memory Test" option in BIOS setup is set for "Extensive", the progress meter may stop until the memory test has completed, causing the system to appear to be hung. Once the memory test has completed, the progress meter will continue as POST progresses. Depending on the amount of memory installed, the progress meter may stop for anywhere between 15 seconds to several minutes.

8.13 BIOS Serviceabilty Features

8.13.1 CMOS Reset

The CMOS configuration RAM may be reset by one of two methods: the CMOS clear jumper located on the baseboard, or the CMOS clear button sequence from the front panel. The CMOS can also be set to a default setting through the BIOS Setup. It will automatically be reset if it becomes corrupted.

Five steps are required to reset the CMOS through the buttons on the front panel:

1. Power off the system, but leave the AC power connected so the 5 V standby is available.
2. Assure that the CMOS clear jumper is in the 'BMC Control' position.
3. Hold down the reset button for at least 4 seconds.
4. While reset button is still depressed, press the on / off button.
5. Simultaneously release both the on / off button and reset buttons.

Upon completion of these steps, the BMC asserts the clear CMOS signal to emulate the movement of the clear CMOS jumper. The BIOS clears CMOS as if the user had moved the CMOS clear jumper on the baseboard. CMOS is cleared only once per front panel button sequence. The BMC releases the CMOS clear line during the next system reset.

Note: Removing the CMOS Clear jumper from the baseboard can disable the Front Panel CMOS reset function. The jumper should be retained in case the CMOS needs to be cleared using the baseboard header.

When the BIOS detects a reset CMOS request, CMOS defaults are loaded during the next POST sequence. Note that non-volatile storage for embedded devices may or may not be affected by the clear CMOS operation depending on the available hardware support.

8.14 BIOS Updates

There are two methods of updating the BIOS code stored in Flash memory. One is via the IFLASH command as explained in the Flash Update Utility section below. An alternate method enabled in the SE7501BR2 Server Board referred to as the One-Boot Update Utility[19] is a new

[19] For further details on features, system requirements, compatibility, and use of the One-Boot Update Utility, refer to the the Intel Server Management version 5.0 Technical Product Specification.

method which provides the capability to perform a BIOS and BMC Firmware update while the server host operating system is running.

8.14.1 Flash Update Utility

The Flash Memory Update utility (iFLASH) loads a fresh copy of the BIOS into flash ROM. The loaded code and data include the following:

- On-board video BIOS, SCSI BIOS, and other option ROMs for the devices embedded on the system board
- The Setup utility
- A user-definable flash area (user binary area)
- A language file

When running iFLASH in interactive mode, the user may choose to update a particular Flash area. Updating a Flash area reads a file, or a series of files, from a hard or floppy disk, and loads it in the specified area of flash ROM. In interactive mode, iFLASH can display the header information of the selected files.

Note: The iFLASH utility must be run without the presence of a 386 protected mode control program, such as Windows* or EMM386*. iFLASH uses the processor's flat addressing mode to update the Flash component.

8.14.2 Loading the System BIOS

The new BIOS is contained in .BIx files. The number of .BIx files is determined by the size of the BIOS area in the flash part. The number of files is constrained by the fact that the image and the utilities fit onto a single, 1.44 MB DOS-bootable floppy. These files are named as follows:

- xxxxxxxx.BIO
- xxxxxxxx.BI1
- xxxxxxxx.BI2

The first eight letters of each filename can be any value, but the files cannot be renamed. Each file contains a link to the next file in the sequence. iFLASH does a link check before updating to ensure that the process is successful. However, the first file in the list can be renamed, but all subsequent filenames must remain unchanged. See Section 8.14.4.

Updating the system BIOS overwrites the language files. If a custom language file has been created, it must be flashed in after the system BIOS has been updated. The user binary area is also updated during a system BIOS update. The user binary can be updated independently from the system BIOS. CMOS is not cleared when the system BIOS is updated in normal or recovery mode. Configuration information like ESCD is not overwritten during BIOS flash update. The user is prompted to reboot after a BIOS update completes.

8.14.3 User Binary Area

The baseboard includes an area in flash for implementation-specific OEM add-ons. The user binary area can be saved and updated as described above in the *System BIOS* section. For this update, only one file is needed. The valid extension for user files is .USR.

8.14.4 BIOS Recovery Mode

If a .BIx image is corrupt, or if an update to the system BIOS is not successful, or if the system fails to complete POST and is unable to boot an operating system, it may be necessary to run the BIOS recovery procedure.

To place the baseboard into recovery mode, move the boot option jumper located on the baseboard, to the BIOS Recovery Boot position. The BIOS is then able to execute the recovery BIOS (also known as the boot block) instead of the normal BIOS. The recovery BIOS is a self-contained image that exists solely as a fail-safe mechanism for installing a new BIOS image. The recovery BIOS boots from a 1.44 MB floppy diskette as used in one of the following devices: a standard 1.44 MB floppy drive, a USB 1.44 MB floppy drive, or an LS-120 removable drive.

Recovery mode requires at least 4 MB of RAM, and drive A: must be set up to support a 3.5” 1.44 MB floppy drive. This is the mode of last resort, used only when the main system BIOS will not come up. In recovery mode operation, iFLASH (in non-interactive mode only) automatically updates only the main system BIOS. iFLASH senses that the platform is in recovery mode and automatically attempts to update the system BIOS.

Note: During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beeps. Failure is indicated by a long series of short beeps. If the recovery disk is not bootable or a recovery disk is not inserted the user will hear three beeps and a POST code value of F0h will be displayed on the port 80h card, then the system will halt.

8.14.4.1 Performing BIOS Recovery

The follow procedure boots the recovery BIOS and flashes the normal BIOS:

1. Turn off the system power.
2. Move the BIOS recovery jumper to the Recovery Boot position.
3. Insert a bootable BIOS update diskette containing the new BIOS image files.
4. Turn on the system power.

The recovery BIOS boots from the DOS-bootable recovery diskette and emits one beep when it passes control to DOS. DOS then executes a special AUTOEXEC.BAT that contains “iFLASH” on the first line. If it is determined that the system is in recovery mode, iFLASH will start the flash update without user intervention. iFLASH reads the flash image and programs the necessary blocks. It emits one beep to indicate the beginning of the flash operation. After a period of time, the BIOS emits two beeps to indicate that the flash procedure was completed successfully. If the flash procedure fails, the BIOS emits a continuous series of beeps.

When the flash update completes:

1. Turn off the system power.
2. Remove the recovery diskette.
3. Restore the jumper to its original position.
4. Turn on the system power.
5. Re-flash any custom blocks, such as user binary or language blocks.

The system should now boot normally using the updated system BIOS.

8.15 BIOS and System Setup Utility

Two utilities are used to configure BIOS and system resources: the BIOS Setup utility and the System Setup Utility. On-board devices are configured with the BIOS Setup utility that is embedded in flash ROM. BIOS Setup provides enough configuration functionality to boot an operating system image or a CD-ROM containing the System Setup Utility. The System Setup Utility is used to view and configure additional settings that are not available at the BIOS Setup utility Level (e.g. SEL viewer application). The System Setup Utility is released on diskette or CD-ROM.

The configuration utilities allow the user to modify the CMOS RAM and NVRAM. The actual hardware configuration is accomplished by the BIOS POST routines and the BIOS Plug-N-Play Auto-configuration Manager. The configuration utilities update a checksum for both areas, so potential data corruption is detected by the BIOS before the hardware configuration is saved. If the data is corrupted, the BIOS requests that the user reconfigure the system and reboot.

8.15.1 BIOS Setup Utility

This section describes the ROM-resident Setup utility that provides the means to configure the platform. The BIOS Setup utility is part of the system BIOS and allows limited control over on-board resources. The System Setup Utility must be used for configuring the on-board devices and add-in cards.

The user can disable embedded PCI devices through the setup menus. When these devices are disabled through setup, their resources are freed. The following embedded devices can be disabled through setup menus, making them invisible to a plug-and-play operating system that scans the PCI bus:

- Embedded SCSI
- Embedded video
- Each embedded NICs (2)
- ICH3-S USB Controller

Note: The BIOS options described in this section may or may not be present in pre-production versions of the system BIOS. This section describes the BIOS utility as it is planned to be at production and is subject to change. Option locations in a given menu of the BIOS setup utility as described in this section may be different from those observed on any one pre-production version if the system BIOS. This section will be updated in the 1.0 release of this document.

8.15.2 Setup Utility Operation

The ROM-resident BIOS Setup utility is only used to configure on-board devices. The System Setup Utility is required to configure added PCI cards.

The BIOS Setup utility screen is divided into four functional areas. Table 29 describes each area:

Table 29. Setup Utility Screen

Functional Area	Description

Keyboard Command Bar	Located at the bottom of the screen or as part of the help screen. This bar displays the keyboard commands supported by the Setup utility.
Menu Selection Bar	Located at the top of the screen. Displays the various major menu selections available to the user. The server Setup utility major menus are: Main Menu, Advanced Menu, Security Menu, Server Menu, Boot Menu, and the Exit Menu.
Options Menu	Each Option Menu occupies the left and center sections of the screen. Each menu contains a set of features. Selecting certain features within a major Option Menu drops you into sub-menus.
Item Specific Help Screen	Located at the right side of the screen is an item-specific Help screen.

8.15.2.1 Entering the BIOS Setup Utility

During the BIOS POST operation, the user is prompted to use the F2 function key to enter Setup as follows:

```
Press <F2> to enter Setup
```

A few seconds might pass before Setup is entered. This is the result of POST completing test and initialization functions that must be completed before Setup can be entered. When Setup is entered, the Main Menu options page is displayed.

8.15.2.2 Keyboard Command Bar

The bottom portion of the Setup screen provides a list of commands that are used to navigate through the Setup utility. These commands are displayed at all times. Each menu page contains a number of configurable options and/or informational fields. The Keyboard Command Bar supports the following table.

Table 30. Keyboard Command Bar

Key	Option	Description
Enter	Execute Command	The Enter key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected option has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu.
ESC	Exit	The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered. When the ESC key is pressed in any sub-menu, the parent menu is re-entered. When the ESC key is pressed in any major menu, the exit confirmation window is displayed and the user is asked whether changes can be discarded. If “No” is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before ESC was pressed without affecting any existing any settings. If “Yes” is selected and the Enter key is pressed, setup is exited and the BIOS continues with POST.
↑	Select Item	The up arrow is used to select the previous value in a pick list, or the previous options in a menu item’s option list. The selected item must then be activated by pressing the Enter key.
↓	Select Item	The down arrow is used to select the next value in a menu item’s option list, or a value field’s pick list. The selected item must then be activated by pressing the Enter key.
↔	Select Menu	The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed.

Key	Option	Description
Tab	Select Field	The Tab key is used to move between fields. For example, Tab can be used to move from hours to minutes in the time item in the main menu.
-	Change Value	The minus key on the keypad is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list.
+	Change Value	The plus key on the keypad is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list. On 106-key Japanese keyboards, the plus key has a different scan code than the plus key on the other keyboard, but will have the same effect
F9	Setup Defaults	Pressing F9 causes the following to appear: **Setup Confirmation** **Load default configuration now?** **[Yes] [No]** If "Yes" is selected and the Enter key is pressed, all Setup fields are set to their default values. If "No" is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before F9 was pressed without affecting any existing field values
F10	Save and Exit	Pressing F10 causes the following message to appear: **Setup Confirmation** **Save Configuration changes and exit now?** **[Yes] [No]** If "Yes" is selected and the Enter key is pressed, all changes are saved and Setup is exited. If "No" is selected and the Enter key is pressed, or the ESC key is pressed, the user is returned to where they were before F10 was pressed without affecting any existing values.

8.15.2.3 Menu Selection Bar

The Menu Selection Bar is located at the top of the screen. It displays the various major menu selections available to the user:

- Main Menu
- Advanced Menu
- Security Menu
- Server Menu
- Boot Menu
- Exit Menu

These and associated sub-menus are described below.

8.15.2.4 Main Menu Selections

The following tables describe the available functions on the top-level menus and on various sub-menus. Default values are highlighted.

Table 31. Main Menu Selections

Feature	Option	Description
System Time	HH:MM:SS	Set the System Time.
System Date	MM/DD/YYYY	Set the System Date.
Floppy A	Not Installed **1.44 / 1.2 MB 3½"** 2.88 MB 3½"	Selects Diskette Type.
Hard Disk Pre-delay	**Disabled** 3 seconds 6 seconds 9 seconds 12 seconds 15 seconds 21 seconds 30 seconds	Allows slower spin-up drives to come ready.
Primary IDE Master	Informational. Drive size CD-ROM or ATAPI Removable	Also selects sub-menu
Primary IDE Slave	Informational. Drive size CD-ROM or ATAPI Removable	Also selects sub-menu
Secondary IDE Master	Informational. Drive size CD-ROM or ATAPI Removable	Also selects sub-menu
Secondary IDE Slave	Informational. Drive size CD-ROM or ATAPI Removable	Also selects sub-menu
Processor Settings	N/A	Selects sub-menu
Language	English (US) Español Deutsch Italiano Francais	Selects which language BIOS displays.

Table 32. Primary/Secondary Master and Slave Adapters Sub-menu Selections

Feature	Option	Description
Type	None **Auto**	Auto allows the system to attempt auto-detection of the drive type. None informs the system to ignore this drive.

Feature	Option	Description
LBA Mode Control	**Disabled** Enabled	Disabled by default if no devices are detected, otherwise the setting is auto detected This field is informational only.
Multi-Sector Transfer	**Disabled** 2 Sectors 4 Sectors 8 Sectors 16 Sectors	Displays the number of sectors per block for multiple sector transfers. This field is informational only. This option is viewable only if an IDE HDD is detected.
PIO Mode	Standard 1 2 3 3 / DMA 1 4 4 / DMA 2	Displays the method for moving data to/from the drive. This field is informational only.
Ultra DMA	Mode 2 Mode 4	Displays the method for moving data to/from the drive. This field is informational only.

Table 33. Processor Settings Sub-menu

Feature	Option	Description
Processor POST Speed	Information Only	Displays the measured processor speed
Processor Retest	**Disabled** Enabled	If enabled, BIOS will clear historical processor status and retest all processors on the next boot.
Hyper-Threading Support	Disabled **Enabled**	If disabled, Hyper-Threading will be disabled
Processor 1 CPUID	N/A	Reports CPUID for Processor 1.
Processor 1 L2 Cache Size	N/A	Reports L2 Cache Size for Processor 1.
Processor 2 CPUID	N/A	Reports CPUID of Processor 2.
Processor 2 L2 Cache Size	N/A	Reports L2 Cache Size for Processor 2.

8.15.2.5 Advanced Menu Selections

The following tables describe the menu options and associated sub-menus available on the Advanced Menu.

Table 34. Advanced Menu Selections

Feature	Option	Description
PCI Configuration	N/A	Selects sub-menu.
Peripheral Configuration	N/A	Selects sub-menu.
Memory Configuration	N/A	Selects sub-menu.
Advanced Chipset Control	N/A	Selects sub-menu. May not be present, if there are no advanced chipset settings under user control.

Boot-time Diag Screen	**Disabled** Enabled	If disabled, the BIOS will display the OEM logo during POST. This option is hidden if the BIOS does not detect a valid logo in the flash area reserved for this purpose.
Reset Configuration Data	**No** Yes	Select 'Yes' if you want to clear the System Configuration Data during next boot. Automatically reset to 'No' in next boot.
Numlock	On **Off**	Sets power on Numlock state.
Sleep Button	**Enabled** Disabled	If disabled, sleep button will be disabled.

Table 35. PCI Configuration Sub-menu Selections

Feature	Option	Description
USB Function	N/A	Selects sub-menu
On-board NIC 1 (10/100 MB)	N/A	Selects sub-menu
On-board NIC 2 (1.0 GB)	N/A	Selects sub-menu
On-board SCSI	N/A	Selects sub-menu,
On-board Video	N/A	Selects sub-menu
PCI Slot 1 ROM	**Enabled** Disabled	Enable option ROM scan of the device in the selected 64-bit 100 MHz PCI-X slot.
PCI Slot 2 ROM	**Enabled** Disabled	Enable option ROM scan of the device in the selected 64-bit 100 MHz PCI-X slot.
PCI Slot 3 ROM	**Enabled** Disabled	Enable option ROM scan of the device in the selected 64-bit 100 MHz PCI-X slot. Slot will operate at PCI 64-bit 66 MHz with onboard SCSI controller enabled.
PCI Slot 4 ROM	**Enabled** Disabled	Enable option ROM scan of the device in the selected 64-bit 100 MHz PCI-X slot. Slot will operate at PCI 64-bit 66 MHz with onboard SCSI controller enabled. This slot supports MROMB with onboard SCSI controller enabled.
PCI Slot 5 ROM	**Enabled** Disabled	Enable option ROM scan of the device in the selected 32-bit 33MHz PCI slot.
PCI Slot 6 ROM	**Enabled** Disabled	Enable option ROM scan of the device in the selected 32-bit 33MHz PCI slot.

Table 36. PCI Configuration, Embedded Devices

Feature	Option	Description
USB Function	Disabled **Enabled**	If disabled, the USB controller is turned off and the device resources are hidden from the system.
On-board NIC 1	Disabled **Enabled**	If disabled, embedded NIC 1 is turned off and the device resources are hidden from the system.
On-board NIC 1 ROM	**Enabled** Disabled	If enabled, initialize NIC 1 expansion ROM.
On-board NIC 2	Disabled **Enabled**	If disabled, the embedded NIC 2 is turned off and the device resourses are hidden from the system.

Feature	Option	Description
On-board NIC 2 ROM	**Enabled** Disabled	If enabled, initialize NIC 2 expansion ROM. (This option is only present in the SCSI SKU)
On-board SCSI	Disabled **Enabled**	If disabled, the embedded SCSI device is turned off and the device resourses are hidden from the system.
On-board SCSI ROM	**Enabled** Disabled	If enabled, initialize embedded SCSI device expansion ROM.
On-board Video	**Enabled** Disabled	If disabled, embedded video is turned off and the device resources are hidden from the system.

Table 37. Peripheral Configuration Sub-menu Selections

Feature	Option	Description
Serial Port A Address	Disabled **3F8h** 2F8h 3E8h 2E8h	Selects the base I/O address for Serial port A.
Serial Port A IRQ	**4** 3	Selects the IRQ for Serial port A.
Serial Port B Address	Disabled 3F8h **2F8h** 3E8h 2E8h	Selects the base I/O address for Serial port B.
Serial Port B IRQ	4 **3**	Selects the IRQ for Serial port B.
Parallel Port Address	Disabled **378h** 278h 3BCh	Selects the base I/O address for Parallel port
Parallel Port IRQ	5 **7**	Selects the IRQ for Parallel port
Parallel Port Mode	Normal Bi-Directional EPP **ECP**	Selects the mode for Parallel port
ECP Mode DMA channel	0 1 2 **3**	Selects the DMA channel for ECP mode
Diskette Controller	Disabled **Enabled**	If disabled, the diskette controller in the Super I/O is disabled.

Feature	Option	Description
Legacy USB support	Disabled Keyboard only **Auto** Keyboard and Mouse	If disabled, legacy USB support is turned off at the end of the BIOS POST.
Front Panel USB	Disabled **Enabled**	If disabled, the front panel USB ports are inactive.

Table 38. Memory Configuration Menu Selections

Feature	Option	Description
Extended Memory Test	1 MB 1 KB Every Location **Disabled**	Selects the size of step to use during Extended RAM tests. “Every Location” will increase the boot time considerably depending on the amount of memory installed.
Memory Bank #1 (DIMM 1A, 1B)	Installed **Not Installed** Disabled	Displays the current status of the memory bank. Disabled indicated that a DIMM in the bank has failed and the entire bank has been disabled.
Memory Bank #2 (DIMM 2A, 2B)	Installed **Not Installed** Disabled	Displays the current status of the memory bank. Disabled indicated that a DIMM in the bank has failed and the entire bank has been disabled.
Memory Retest	**Disabled** Enabled	Causes BIOS to retest all memory on next boot.

Table 39. Advanced Chipset Control Sub-menu Selections

Feature	Option	Description
Wake On Ring	Enabled **Disabled**	Only controls legacy wake up.
Wake On LAN	Enabled **Disabled**	Only controls legacy wake up.
Wake On PME	Enabled **Disabled**	Only controls legacy wake up.
Wake On RTC Alarm	Enabled **Disabled**	Only controls legacy wake up

8.15.2.6 Security Menu Selections

Table 40. Security Menu Selections

Feature	Option	Description
User Password is	**Not Installed** Installed	Status only; user cannot modify. Once set, can be disabled by setting to a null string, or clear password jumper on board.

Feature	Option	Description
Administrator Password is	**Not Installed** Installed	Status only; user cannot modify. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Set Admin Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Set User Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Password On Boot	Disabled **Enabled**	If enabled, requires password entry before boot. (This option is only present when User password is Installed)
Fixed Disk Boot Sector	**None** Write Protect	Will write protect the boot sector of the hard drive to prevent viruses from corrupting the device under DOS if set to Write Protect.
Secure Mode Timer	**1 minute** 2 minutes 5 minutes 10 minutes 20 minutes 60 minutes 120 minutes	Period of key/PS/2 mouse inactivity specified for Secure Mode to activate. A password is required for Secure Mode to function. (This option is only present when User password is Installed)
Security Hot Key (Ctrl-Alt-)	**[L]** [Z]	Key assigned to invoke the secure mode feature. Can be disabled by entering a new key followed by a backspace or by entering delete. (This option is only present when User password is Installed)
Secure Mode Boot	**Disabled** Enabled	System boots in Secure Mode. The user must enter a password to unlock the system. (This option is only present when User password is Installed)
Video Blanking	**Disabled** Enabled	Blank video when Secure mode is activated. A password is required to unlock the system. This option is only present if the system includes an embedded video controller. (This option is only present when User password is Installed)
Power Switch Inhibit	**Disabled** Enabled	When enabled, the power switch is inoperable.
NMI control	Disabled **Enabled**	When enabled, NMI control through BMC for the front panel NMI button is operable.

8.15.2.7 Server Menu Selections

Table 41. Server Menu Selections

Feature	Option	Description
System Management	N/A	Selects sub-menu.
Console Redirection	N/A	Selects sub-menu.
Event Log Configuration	N/A	Selects sub-menu.
Fault Resilient Booting	N/A	Selects sub-menu
Assert NMI on PERR	**Disabled** Enabled	If enabled, PCI bus parity error (PERR) is enabled and is routed to NMI.

Feature	Option	Description
Assert NMI on SERR	**Enabled** Disabled	If enabled, PCI bus system error (SERR) is enabled and is routed to NMI.
FRB-2 Policy	**Disable BSP** Do Not Disable BSP Retry 3 Times Disable FRB2 Timer	Controls the policy of the FRB-2 timeout. This option determines when the Boot Strap Processor (BSP) should be disabled if FRB-2 error occur.
POST Error Pause	**Enabled** Disabled	If enabled, the system will wait for user intervention on critical POST errors. If disabled, the system will boot with no intervention, if possible.
Boot Monitoring	**Disabled** 5 minutes 10 minutes 15 minutes 20 minutes 5 minutes 30 minutes 35 minutes 40 minutes 45 minutes 50 minutes 55 minutes 60 minutes	Set the amount of time the operating system Watchdog timer is programmed with. If disabled, the operating system watchdog timer is not programmed.
Boot Monitoring Policy	**Retry 3 Times** Retry Service Boot Always Reset	Configures the system response to the expiration of the operating system watchdog timer.
PXE OS Boot Timeout	**Disable** 5 minutes 10 minutes 15 minutes 20 minutes	Controls the limit allowed to load the operating system from a device compliant with the PXE specification. This timer must be DISABLED by Platform Instrumentation Software after operating system load.

Table 42. System Management Sub-menu Selections

Feature	Option	Description
Board Part Number	N/A	Information field only
Board Serial Number	N/A	Information field only
System Part Number	N/A	Information field only
System Serial Number	N/A	Information field only
Chassis Part Number	N/A	Information field only
Chassis Serial Number	N/A	Information field only
BIOS Revision	N/A	Information field only. Full BIOS version information
BMC Device ID	N/A	Information field only
BMC Firmware Revision	N/A	Information field only. Only if available through IPMI command.
BMC Device Revision	N/A	Information field only
PIA Revision	N/A	Information field only
SDR Revision	N/A	Information field only
Primary HSBP Revision	N/A	Information field only, hidden if not detected

Feature	Option	Description
Secondary HSBP Revision	N/A	Information field only, hidden if not detected

Table 43. Console Redirection Sub-menu Selections

Feature	Option	Description
BIOS Redirection Port	**Disabled** Serial A Serial B	If enabled, BIOS uses the specified serial port to redirect the console to a remote ANSI terminal. Enabling this option disables Quiet Boot.
ACPI Redirection port	**Disabled** Serial A Serial B	Enable ACPI OS Headless Console Redirection. “Disable” completely disables ACPI OS Headless Console Redirection.
Baud Rate	9600 **19.2K** 57.6K 115.2K	When console redirection is enabled, use the baud rate specified. When the Emergency Management Port shares the COM port as console redirection, the baud rate must be set to 19.2 k to match the Emergency Management Port baud rate, unless auto-baud feature is used.
Flow Control	No Flow Control **CTS/RTS** XON/XOFF CTS/RTS + CD	None = No flow control. CTS/RTS = Hardware based flow control. XON/XOFF = Software flow control. CTS/RTS +CD = Hardware based + Carrier Detect flow control. When EMP is sharing the COM port as console redirection, the flow control must be set to CTS/RTS or CTS/RTS+CD depending on whether a modem is used.
Terminal Type	PC-ANSI **VT100+** VT-UTF8	This selects the character set to send out the serial port when console redirection is enabled. VT-UTF8 makes use of Unicode characters and is intended specifically for use by new Microsoft software or other companies that use Unicode. VT100+ only works with English. PC-ANSI is the standard PC-type terminal.

Table 44. Event Log Configuration Sub-menu Selections

Feature	Option	Description
Clear All Event Logs	**No** Yes	When yes is chosen, the BIOS will clear the System Event Log on the next boot.
Event Logging	Disabled **Enabled**	Enables / disables System Event Logging.
Critical Event Logging	Disabled **Enabled**	Enables/ disables critical system event logging including PERR, SERR, ECC memory errors, and NMI.

Table 45. Fault Resilient Booting Sub-menu Selections

Feature	Option	Description

Feature	Option	Description
Late POST Timer	**Disable** 5 minutes 10 minutes 15 minutes 20 minutes	Controls the time limit allowed for add-in card option ROM initialization. The system reboots if the timer times out.
Fault Resilient Booting	**Stay On** Reset PowerOff	Controls the policy upon timeout.
Hard Disk OS Boot Timeout	**Disable** 5 minutes 10 minutes 15 minutes 20 minutes	This contols the time limit allowed for booting an OS from a hard disk drive.
PXE OS Boot Timeout	**Disable** 5 minutes 10 minutes 15 minutes 20 minutes	Controls the limit allowed to load the operating system from a device compliant with the PXE specification. This timer must be DISABLED by Platform Instrumentation Software after operating system load.

Note: If the "Boot monitoring" option on the "Server" menu is set to anything other than "Disabled", then the "Fault Resilient booting" menu options for "Hard Disk OS boot Timeout" and "PXE OS Boot Timeout" are no longer available. They are completely removed from the "Fault Resilient booting" menu. Also, if either "Hard Disk OS boot Timeout" or "PXE OS Boot Timeout" options on the "Fault Resilient booting" menu are set to anything other than "Disabled", then the "Server" menu options "Boot monitoring" and "Boot Monitoring Policy" are no longer available. They are completely removed from the "Server" menu.

8.15.2.8 Boot Menu Selections

Boot Menu options allow the user to select the boot device. The following table is an example of a list of devices ordered in priority of the boot invocation. Items can be re-prioritized by using the up and down arrow keys to select the device. Once the device is selected, use ↑ key to move the device higher in the boot priority list. Use ↓ key to move the device lower in the boot priority list.

Table 46. Boot Menu Selections

Feature	Option	Description
Boot Device Priority	N/A	Selects sub-menu.
Hard Disk Drives	N/A	Selects sub-menu.
Removable Devices	N/A	Selects sub-menu.
ATAPI CD-ROM Drives	N/A	Selects sub-menu.

Table 47. Boot Device Priority Selections

Boot Priority	Device	Description

Boot Priority	Device	Description
1	Removable Devices	Attempt to boot from a legacy floppy A: or removable media device like LS-120.
2	Hard Drive	Attempt to boot from a hard drive device.
4	ATAPI CD-ROM Drive	Attempt to boot from an ATAPI CD-ROM drive.
5	(any) SCSI CD-ROM Drive	Attempt to boot from a SCSI CD-ROM containing bootable media. This entry will appear if there is a bootable CD-ROM that is controlled by a BIOS Boot Specification compliant SCSI option ROM.
6	PXE UNDI	Attempt to boot from a network. This entry will appear if there is a network device in the system that is controlled by a PXE compliant option ROM.

Table 48. Hard Drive Selections

Option	Description
Drive #1 (or actual drive string) Other bootable cards Additional entries for each drive that has a PnP header	To select the boot drive, use the up and down arrows to highlight a device, then press ↑ key to move it to the top of the list or ↓ key to move it down. Other bootable cards cover all the boot devices that are not reported to the system BIOS through BIOS boot specification mechanism. It may or may not be bootable, and may not correspond to any device. If BIOS boot spec. support is set to limited, this item covers all drives that are controlled by option ROMs (like SCSI drives). Press ESC to exit this menu.

Table 49. Removable Devices Selections

Feature	Option	Description
Lists Bootable Removable Devices in the System	↑ ↓	Use ↑ / ↓ keys to place the removable devices in the boot order you want. Includes Legacy 1.44 MB floppy, 120 MB floppy etc.

Table 50. ATAPI CDROM Drives Selections

Feature	Option	Description
Lists ATAPI CDROM Drives in the System	↑ ↓	Use ↑ / ↓ keys to place the removable devices in the boot order you want

8.15.2.9 Exit Menu Selections

The following menu options are available on the Exit menu. The up and down arrow keys are used to select an option, then the Enter key is pressed to execute the option.

Table 51. Exit Menu Selections

Option	Description
Exit Saving Changes	Exit after writing all modified Setup item values to NVRAM.
Exit Discarding Changes	Exit leaving NVRAM unmodified. User is prompted if any of the setup fields were modified.
Load Setup Defaults	Load default values for all SETUP items.
Load Custom Defaults	Load values of all Setup items from previously saved Custom Defaults. Hidden if custom defaults are not valid.
Save Custom Defaults	Stores Custom Defaults in NVRAM.
Discard Changes	Read previous values of all Setup items from NVRAM.

8.16 BIOS Security Features

The SE7501BR2 server BIOS provides a number of security features. This section describes the security features and operating model.

Note: The server board SE7501BR2 has the ability to boot from a device attached to the USB port, such as a floppy disk, disk drive or CD-ROM, or ZIP* drive, even if it is attached through a hub. The security model is not supported when booting to a USB device.

8.16.1 Operating Model

The following table summarizes the operation of security features supported by the SE7501BR2 server BIOS.

Table 52. Security Features Operating Model

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Secure mode	Keyboard Inactivity Timer, Runtime activation of PS/2 keyboard controller Hotkey	User Password enabled in setup	• On-board video goes blank (if enabled in Setup). • All switches on the front panel except NMI are disabled • No PS/2 mouse or PS/2 keyboard input is accepted. • Keyboard LEDs flash	User Password	• Video is restored. • Front Panel switches are enabled. • Keyboard and mouse inputs are accepted.

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Secure boot	Power On/Reset	User Password and Secure Boot Enabled	• Prompts for password, if booting from drive A • Enter secure mode just before scanning option ROMs i.e. Keyboard LEDs flash, but video blanking and front panel lock is not invoked until operating system boot • All the switches on the front panel are disabled except NMI. • No input from PS/2 mouse or PS/2 keyboard is accepted; however, the Mouse driver is allowed to load before a password is required. • If booting from drive A, and the user enters correct password, the system boots normally.	User Password	• Floppy writes are re-enabled. • Front panel switches are re-enabled. • PS/2 Keyboard and PS/2 mouse inputs are accepted. • System attempts to boot from drive A. If the user enters correct password, and drive A is bootable, the system boots normally
Password on boot	Power On/Reset	User Password set and password on boot enabled and Secure Boot Disabled in setup	• System halts for user Password before scanning option ROMs. The system is not in secure mode. • No mouse or keyboard input is accepted except the password.	User Password	• Front Panel switches are re-enabled. • PS/2 Keyboard and PS/2 mouse inputs are accepted. • The system boots normally. Boot sequence is determined by setup options.
Fixed disk boot sector	Power On/Reset	Set feature to Write Protect in Setup	Will write protect the master boot record of the IDE hard drives only if the system boots from a floppy. The BIOS will also write protect the boot sector of the drive C: if it is an IDE drive.	Set feature to Normal in Setup	Hard drive will behave normally.

8.16.2 Password Protection

The BIOS uses passwords to prevent unauthorized tampering with the system. Once secure mode is entered, access to the system is allowed only after the correct password(s) has been entered. Both the user and administrator passwords are supported by the BIOS. The administrator password must be set prior to setting the user password. The maximum length of the password is seven characters. The password can have only alphanumeric characters (a-z, A-Z, 0-9). The user and administrator passwords are not case sensitive.

Note: Numbers entered via the NumPad are recognized as different characters than numbers from the top row of a standard QWERTY keyboard.

Once set, a password can be cleared by changing it to a null string. The user password is cleared when the administrator password is cleared. Entering the user password allows the user to modify the time, date, language, user password, secure mode timer, and secure mode hot-key setup fields. The user password also allows the system to boot if secure boot is enabled. Other setup fields can be modified only if the administrator password is entered. If only one password is set, this password is required to enter Setup. The Administrator has control over all fields in the setup, including the ability to clear user password.

If the user enters three wrong passwords in a row during the boot sequence, the system will be placed into a halt state. This feature makes it difficult to break the password by “trial and error” method. When entering a password, the backspace key is accepted as a character of the password. Entering the backspace key will result in a wrong password.

BIOS Setup may provide an option for setting the Emergency Management Port password. However, the Emergency Management Port password is only utilized by the BMC, this password does not effect the BIOS security in any way, nor does the BIOS security engine provide any validation services for this password. Emergency management port security is handled primarily through the BMC and Emergency Management Port utilities.

8.16.3 Inactivity Timer

If the inactivity timer function is enabled, and no keyboard or mouse actions have occurred for the specified time-out period, the following occurs until the user password is entered:

- PS/2 keyboard and PS/2 mouse input is disabled. PS/2 keyboard lights start blinking.
- On-board video is blanked (if selected in setup)
- Floppy drive is write protected (if selected in setup)
- Front panel reset, sleep (if present) and power switches are locked

If a user password is entered, a time-out period must be specified in setup.

8.16.4 Hot Key Activation

Instead of waiting for the inactivity time-out to expire, a hot-key combination allows the user to activate secure mode immediately. The hot-key combination is configured through Setup. The following keys are valid hot keys: Ctrl-Alt <L, Z>. Setup will not permit the user to choose any other key as the hot key.

Note: that the hotkey will only work on PS/2 keyboards.

8.16.5 Password Clear Jumper

If the user or administrator password(s) is lost or forgotten, both passwords may be cleared by moving the password clear jumper on the baseboard, into the “Clear” position. The BIOS determines if the password clear jumper is in the “Clear” position during BIOS POST and clears any passwords if required. The password clear jumper must be restored to its original position before a new password(s) can be set.

8.16.6 Secure Mode (Unattended Start)

Secure mode refers to a system state where many of the external inputs and outputs are disabled to prevent tempering. These include PS/2 ports, floppy and on-board video.

8.16.7 Front Panel Lock

The front panel buttons, including power and reset, are always disabled when the system is in secure mode. If the system has a sleep switch, it will also be disabled while the system is in secure mode.

8.16.8 Video Blanking

If enabled in Setup, and a monitor is attached to the embedded VGA controller, the video will be blanked upon entering secure mode. This feature prevents unauthorized users from viewing the screen while system is in secure mode.

Note: Video monitors attached to add-in video adapters will not be blanked regardless of the setting of the video blanking feature.

8.16.9 PS/2 Keyboard and Mouse Lock

Keyboard and/or mouse devices attached to the PS/2 connector are unavailable while the system is in secure mode. The keyboard controller will not pass any keystrokes or mouse movements to the system until the correct user password is entered.

Note: As secure mode has direct control of the keyboard controller and is able to secure access to the system via the PS/2 connector, the USB ports are not under secure mode control. USB ports are still functional when the system is in secure mode. It is recommended that all USB ports be “Disabled” in BIOS setup if a Secure Mode environment is in use.

8.16.10 Secure Boot (Unattended Start)

Secure boot allows the system to boot and run the operating system without requiring the user password even if a user password is set. Secure boot is nothing but booting the system while keeping it in secure mode. However, until the user password is entered, mouse input, keyboard input, and activation of the enabled secure mode features described above are not accepted.

In secure boot mode, if the BIOS detects a floppy diskette in the A: drive at boot time, it displays a message and waits for the user password before booting. After the password is entered, the system can boot from the floppy and secure mode is disabled. Any of the secure mode triggers will cause the system to return to secure mode.

If there is no diskette in drive A, the system will boot from the next boot device and will automatically be placed into secure mode. The PS/2 keyboard and mouse are locked before option ROMs are scanned. Video is blanked and the front panel is locked immediately before the operating system boots. If secure boot is enabled, the user cannot enter option ROM setup unless the user password is entered. This prevents entering the configuration utilities in the option ROMs where it is possible to format drives, etc. The on-board video is not blanked until the end of the POST.

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9. BIOS Error Reporting and Handling

This section defines how errors are handled by the system BIOS. It also discusses the role of the BIOS in handling errors, and the interaction between the BIOS, platform hardware, and server management firmware with regard to error handling. In addition, error-logging techniques are described and beep codes for errors are defined.

9.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handles system errors. System errors which can be disabled and enabled individually or as a group, can be categorized as follows:

- PCI bus.
- Memory single- and multi-bit errors.
- Sensors.
- Processor internal errors, bus/address errors, thermal trip errors, temperatures and voltages, and GTL voltage levels.
- Errors detected during POST, logged as 'POST errors'.

Sensors are managed by the BMC. The BMC is capable of receiving event messages from individual sensors and logging system events. Refer to the SE7501BR2 BMC EPS for additional information concerning BMC functions.

9.2 SMI Handler

The SMI handler is used to handle and log system level events that are not visible to the server management firmware. If the SMI handler control bit is disabled in Setup, SMI signals are not generated on system errors. If enabled, the SMI handler preprocesses all system errors, even those that are normally considered to generate an NMI. The SMI handler sends a command to the BMC to log the event and provides the data to be logged. System events that are handled by the BIOS generate SMI.

9.3 PCI Bus Error

The PCI bus defines two error pins, PERR# for reporting parity errors, and SERR# for reporting system errors. The BIOS can be instructed to enable or disable reporting PERR# and SERR# through NMI[20]. For a PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if bit 2 of I/O register 61 is set to 0. If SERR# is enable in BIOS setup, all PCI-to-PCI bridges will generate an SERR# on the primary interface whenever an SERR# occurs on the secondary side of the bus. The same is true for PERR#s.

[20] Disabling NMI for PERR# and/or SERR# also disables logging of the corresponding event.

9.4 Processor Failure

The BIOS detects and logs any processor BIST failure. The failed processor can be identified by the first OEM data byte field in the log. For example, if processor 0 fails, the first OEM data byte will be 0. The BIOS depends on the BMC to log the watchdog timer reset event.

9.5 Processor Bus Error

If irrecoverable errors are encountered on the host processor bus, proper execution of the BIOS SMI handler cannot be guaranteed. The BIOS SMI handler will record errors to the system event log only if the system has not experienced a catastrophic failure that compromises the integrity of the SMI handler.

9.6 Single Bit ECC Error Throttling Prevention

The system detects, corrects, and logs correctable errors as indicated in Section 8.2.3 as long as these errors occur infrequently, the system should continue to operate without a problem.

Occasionally, correctable errors are caused by a persistent failure of a single component. Although these errors are correctable, continual calls to the error logger can throttle the system, preventing further useful work.

For this reason, the system counts certain types of correctable errors and disables reporting if errors occur too frequently. Error correction remains enabled but calls to the error handler are disabled. This allows the system to continue running, despite a persistent correctable failure. The BIOS adds an entry to the event log to indicate that logging for that type of error has been disabled. This entry indicates a serious hardware problem that must be repaired at the earliest possible time.

The SE7501BR2 system BIOS implements this feature for correctable bus errors. If ten errors occur within an hour, the corresponding error handler disables further reporting of that type of error. The BIOS re-enables logging and SMIs the next time the system is rebooted.

9.7 System Limit Error

The BMC monitors system operational limits. It manages the A/D converter, defining voltage and temperature limits as well as fan sensors and chassis intrusion. Any sensor values outside of specified limits are fully handled by BMC. The BIOS does not generate an SMI to the host processor for these types of system events.

Refer to the SE7501BR2 *Server Management External Architecture Specification* for details on various sensors and how they are managed.

9.8 Boot Event

The BIOS downloads the system date and time to the BMC during POST and logs a boot event in the System Event Log. Software applications that parse the event log should not treat this boot event as an error.

9.9 Fault Resilient Booting (FRB)

The BIOS and firmware provides a feature to guarantee that the system boots, even if one or more processors fail during POST. The BMC contains two watchdog timers that can be configured to reset the system upon time-out.

9.9.1 FRB3

FRB3 refers to the FRB algorithm that detects whether the BSP is healthy enough to run BIOS at all. The BMC starts the FRB3 timer when the system is powered up or hard reset. The BIOS stops this timer in the power-on self test (POST) by asserting the *FRB3 timer halt* signal to the BMC. This requires that the BSP runs BIOS code. If the timer is not stopped within 5 seconds, and it expires, the BMC disables the BSP, logs an FRB3 error event, chooses another BSP (from the set of non-failed processors), and resets the system. FRB3 provides a check to verify that the selected BSP is not dead on start up and can actually run code. This process repeats until either the system boots without an FRB3 timeout, or all of the remaining processors have been disabled. If all of the processors have been disabled, the BMC will attempt to boot the system on one processor at a time, irrespective of processor error history. This is called desperation mode.

9.9.2 FRB2

FRB2 refers to the level of FRB in which the BIOS uses the BMC watchdog timer to back up its operation during POST. The BIOS configures the watchdog timer for approximately 6-10 minutes indicating that the BIOS is using the timer for the FRB2 phase of operation.

After BIOS has identified the BSP and saved that information, it will check to see if the watchdog timer expired on the previous boot. If so, it will store the Time Out Reason bits in a fixed CMOS location (token name = cmosWDTimerFailReason) for applications or a User Binary to examine and act upon. Next, it sets the watchdog timer FRB2 timer use bit, loads the watchdog timer with the new timeout interval, and disables FRB3 using the *FRB3 timer halt* signal. This sequence ensures that no gap exists in watchdog timer coverage between FRB3 and FRB2.

Note: FRB2 is not supported when the BIOS is in Recovery Mode.

If the watchdog timer expires while the watchdog use bit is set to FRB2, the BMC logs a Watchdog expiration event showing an FRB2 timeout (if so configured). It then hard resets the system, assuming Reset was selected as the watchdog timeout action.

The BIOS is responsible for disabling the FRB2 timeout before initiating the option ROM scan, prior to displaying a request for a Boot Password or prior to an Extensive Memory Test. The BIOS will re-enable the FRB2 timer after the Extensive Memory Test. The BIOS will provide a user-configurable option to change the FRB2 response behavior. These four options are:

- Disable BSP on FRB2
- Never Disable BSP
- Disable BSP after 3 consecutive FRB2
- Disable FRB2 timer

The option of “Disable BSP on FRB2” will do the following. If the FRB2 timer expires (i.e., a processor has failed FRB2), the BMC resets the system. As part of its normal operation, the BIOS obtains the watchdog expiration status from the BMC. If this status shows an expiration of the FRB2 timer, the BIOS logs an FRB2 event with the event data being the last Port 80h code issued in the previous boot. The BIOS also issues a Set Processor State command to the BMC, indicating an FRB2 failure and telling it to disable the BSP and reset the system. The BMC then disables the processor that failed FRB2 and resets the system, causing a different processor to become the BSP.

The option of “Never Disable BSP” will perform all the same functions as “Disable BSP on FRB2” with the exception that the BIOS will not send a *Set Processor State* command to the BMC. The BIOS will still log the FRB2 event in the SEL.

The option of “Disable BSP after 3 consecutive FRB2” will perform all the same functions as “Disable BSP on FRB2” with the following exception. The BIOS will maintain a failure history of the successive boots. If the same BSP fails three consecutive boots with an FRB2, the processor would then be disabled. If the system successfully boots to a BSP, the failure history maintained by the BIOS should be cleared.

The option of “Disable FRB2 Timer” will cause the BIOS to not start the FRB2 timer in the BMC during POST. If this option is selected, the system will have no FRB protection after the FRB3 timer is disabled. The BIOS and BMC implement additional safeguards to detect and disable the application processors (AP) in a multiprocessor system. If an AP fails to complete initialization within a certain time, it is assumed to be nonfunctional. If the BIOS detects that an AP is nonfunctional, it requests the BMC to disable that processor. When the BMC disables the processor and generates a system reset, the BIOS will not see the bad processor in the next boot cycle. The failing AP is not listed in the MP table (refer to the *Multi-Processor Specification,* Rev. 1.4), nor in the ACPI APIC tables, and is invisible to the operating system.

All FRB failures including the failing processor are recorded into the System Event Log. However, the user should be aware that if the setup option for error logging is disabled these failures are not recorded. The FRB3 failure is recorded automatically by the BMC while the Late POST, PXE Boot, FRB2, and AP failures are logged to the SEL by the BIOS. In the case of an FRB-2 failure, some systems will log additional information into the OEM data byte fields of the SEL entry. This additional data indicates the last POST task that was executed before the FRB2 timer expired. This information may be useful for failure analysis.

The BMC maintains failure history for each processor in nonvolatile storage. Once a processor is marked “failed,” it remains “failed” until the user forces the system to retest the processor. The BIOS reminds the user about a previous processor failure during each boot cycle until all processors have been retested and successfully pass the FRB tests or AP initialization. Processors that have failed in the past are not allowed to become the BSP and are not listed in the MP table and ACPI APIC tables.

It might happen that all the processors in the system are marked bad. An example is a uni-processor system where the processor has failed in the past. If all the processors are bad, the system does not alter the BSP and it attempts to boot from the original BSP. Error messages are displayed on the console, and errors are logged in the System Event Log of a processor failure.

If the user replaces a processor that has been marked bad by the system, the user must inform the system of this change by running BIOS Setup and selecting that processor to be retested. If a

bad processor is removed from the system, the BMC automatically detects this condition and clears the status flag for that processor during the next boot.

There are three possible states for each processor slot:

- Processor installed (status only, indicates processor has passed BIOS POST).
- Processor failed. The processor may have failed FRB-2 or FRB-3, and it has been disabled.
- Processor not installed (status only, indicates the processor slot has no processor in it).

9.9.2.1 Late POST Timer

Near the end of POST, before the option ROMs are initialized, the BIOS reads a user selectable option to either disable the FRB2 timer or repurpose the timer for Late POST Timeout timer support during option ROM scanning.

The FRB2 timer will be active from before option ROM scanning until platform instrumentation software disables it, with the following exceptions. If the following conditions are true, the timer is restarted after each 1 GB of memory testing to ensure premature expiration of the timer does not occur. This is because the memory test may take longer than 6 minutes.

- System contains more than 1 GB of memory
- The user chooses to test every DWORD of memory
- The Late POST watchdog timer is selected as enabled

Otherwise, the timer is disabled before the extended memory test starts. If the Late POST watchdog timer is enabled, then the BIOS will repurpose the timer to BIOS / POST and set the time at the value selected by the setup option (5, 10, 15, or 20 minutes) before giving control to each option ROM.

WARNING: If the option ROM takes longer than this time, as could happen if a user enters an embedded option ROM setup utility, the option ROM will likely time out. In order to avoid potential confusion caused by these timeouts, this BIOS option is only intended for system administrators.

9.9.2.2 PXE OS Boot Timeout Timer

If the BIOS is going to boot to a known PXE compliant device, then the BIOS reads the setup option for PXE OS Boot timeout and either disables the timer or enables the timer with a value read from the option selected in BIOS Setup (5, 10, 15, or 20 minutes).

9.9.3 FRB1

In addition to Late POST, Boot Monitoring, FRB3 and FRB2 timers, the BIOS provides FRB1. Early in POST, the BIOS checks the Built-in Self Test (BIST) results of the BSP. If the BSP fails BIST, the BIOS requests the BMC to disable the BSP. The BMC disables the BSP, selects a new BSP and generates a system reset. If there is no alternate processor available, the BMC beeps the system speaker and halts the system.

The BIOS and BMC implement additional safeguards to detect and disable the application processors (AP) in a multiprocessor system. If an AP fails to complete initialization within a certain time, it is assumed to be nonfunctional. If the BIOS detects that an AP has failed BIST or is nonfunctional, it requests the BMC to disable that processor. When the BMC disables the processor and generates a system reset, the BIOS will not see the bad processor in the next boot cycle. The failing AP is not listed in the MP table (refer to the *Multi-Processor Specification,* Rev. 1.4), nor in the ACPI APIC tables, and is invisible to the operating system.

Additional information on FRB may be found in the *Server Management EAS* and the *Baseboard Management Controller Interface Specification.*

9.10 Boot Monitoring

9.10.1 Purpose

The Boot Monitoring feature is designed to allow watchdog timer protection of the operating system load process. This is done in conjunction with an OS-present device driver or application that will disable the watchdog timer once the operating system has successfully loaded. If the operating system load process fails, the BMC will reset the system. This feature can be configured through BIOS Setup to operate in one of three modes or be disabled (the default state).

In the “Always Reset” mode, the BMC will reset the system if the OS-present device driver or application does not disable the watchdog timer. In the “Retry 3 times” mode, after three consecutive failures to load the operating system successfully, the BIOS will automatically boot to the Service Partition, if present. If a valid Service Partition is not detected, the system should continue to boot. If the Service Partition boot fails, the cycle starts again. In the “Retry Service Boot” mode, the system operates in a similar manner to the “Retry 3 times” mode. The system will instead try to boot the Service partition up to three consecutive times. If this is unsuccessful, the system halts. Additionally, in this mode, if a valid Service Partition is not detected, the system will halt rather than attempting to boot to it.

9.11 POST Codes, Error Messages, and Error Codes

The BIOS indicates the current testing phase during POST by writing a hex code to port 80h. See Table 55 for a list of supported POST progress codes. If errors are encountered, error messages or codes will either be displayed to the video screen, or if an error has occurred prior to video initialization, errors will be reported through a series of audio beep codes. POST errors are logged in to the System Event Log (SEL).

The error codes are defined by Intel and whenever possible are backward compatible with error codes used on earlier platforms.

Table 53. Boot Block POST Progress Codes

POST Code	Description
06h	Uncompressing the POST code.
10h	The NMI is disabled. Strart Power-on delay. Initialization code checksum verified.
11h	Initialize the DMA controller, perform the keyboard controller BAT test, start memory refresh, and enter 4 GB flat mode.

POST Code	Description
12h	Get start of initialization code and check BIOS header.
13h	Memory sizing.
14h	Test base 512K of memory. Return to real mode. Execute any OEM patches and set up the stack.
15h	Pass control to the uncompressed code in shadow RAM. The initialization code is copied to segment 0 and control will be transferred to segment 0.
16h	Control is in segment 0. Verify the system BIOS checksum. If the system BIOS checksum is bad, go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
17h	Pass control to the interface module.
18h	Decompress of the main system BIOS failed.
19h	Build the BIOS stack. Disable USB controller. Disable cache.
1Ah	Uncompress the POST code module. Pass control to the POST code module.
1Bh	Decompress the main system BIOS runtime code.
1Ch	Pass control to the main system BIOS in shadow RAM.
D2h	Starting chipset register initialization and memory sizing.
D3h	Doing memory sizing and chipset register initialization. First set BIOS size to 128K and do memory sizing.
D5h	The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BIOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
A0h	Detect memory device type using SPD
A8h	To program ECC Mode
E0h	Start of recovery BIOS. Initialize interrupt vectors, system timer, DMA controller, and interrupt controller.
E8h	Initialize extra module if present.
E9h	Initialize floppy controller.
EAh	Try to boot floppy diskette.
EBh	If floppy boot fails, intialize ATAPI hardware.
ECh	Try booting from ATAPI CD-ROM drive.
EEh	Jump to boot sector.
EFh	Disable ATAPI hardware.

Table 54. POST Progress Code Table

POST Code	Description
0Eh	The keyboard controller BAT command result has been verified. It is auto-sensing of external keyboard and mouse mostly used in laptop.
15h	8254 timer.read/ write test on channel 2.
20h	Uncompress various BIOS Modules
22h	Verify password Checksum
24h	Verify CMOS Checksum.
26h	Read Microcode updates from BIOS ROM.
28h	Initializing the processors. Set up processor registers. Select least featured processor as the BSP.
2Ah	Go to Big Real Mode
2Ch	Decompress INT13 module

POST Code	Description
2Eh	Keyboard Controller Test: The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller
30h	Keyboard/Mouse port swap, if needed
32h	Write Command Byte 8042: The initialization after the keyboard controller BAT command test is done. The keyboard command byte will be written next.
34h	Keyboard Init: The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands
36h	Disable and initialize 8259
38h	Detect Configuration Mode, such as CMOS clear.
3Ah	Chipset Initialization before CMOS initialization
3Ch	Init System Timer: The 8254 timer test is over. Starting the legacy memory refresh test next.
3Eh	Check Refresh Toggle: The memory refresh line is toggling. Checking the 15 second on/off time next
40h	Calculate CPU speed
42h	Init interrupt Vectors: Interrupt vector initialization is done.
44h	Enable USB controller in chipset
46h	Initialize SMM handler. Initialize USB emulation.
48h	Validate NVRAM areas. Restore from backup if corrupted.
4Ah	Load defaults in CMOS RAM if bad checksum or CMOS clear jumper is detected.
4Ch	Validate date and time in RTC.
4Eh	Determine number of micro code patches present
50h	Load Micro Code To All CPUs
52h	Scan SMBIOS GPNV areas
54h	Early extended memory tests
56h	Disable DMA
58h	Disable video controller
5Ah	8254 Timer Test on Channel 2
5Ch	Enable 8042. Enable timer and keyboard IRQs. Set Video Mode: Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
5Eh	Init PCI devices and motherboard devices. Pass control to video BIOS. Start serial console redirection.
60h	Initialize memory test parameters
62h	Initialize AMI display manager Module. Initialize support code for headless system if no video controller is detected.
64h	Start USB controllers in chipset
66h	Set up video parameters in BIOS data area.
68h	Activate ADM: The display mode is set. Displaying the power-on message next.
6Ah	Initialize language module. Display splash logo.
6Ch	Display Sign on message, BIOS ID and processor information.
6Eh	Detect USB devices
70h	Reset IDE Controllers
72h	Displaying bus initialization error messages.
74h	Display Setup Message: The new cursor position has been read and saved. Displaying the Hit Setup message next.
76h	Ensure Timer Keyboard Interrupts are on.
78h	Extended background memory test start
7Ah	Disable parity and nmi reporting.

POST Code	Description
7Ch	Test 8237 DMA Controller: The DMA page register test passed. Performing the DMA Controller 1 base register test next
7Eh	Init 8237 DMA Controller: The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
80h	Enable Mouse and Keyboard: The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next
82h	Keyboard Interface Test: A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
83h	Disable parity and NMI.
84h	Check Stuck Key Enable Keyboard: The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
86h	Disable parity NMI: The command byte was written and global data initialization has completed. Checking for a locked key next
88h	Display USB devices
8Ah	Verify RAM Size: Checking for a memory size mismatch with CMOS RAM data next
8Ch	Lock out PS/2 keyboard/mouse if unattended start is enabled.
8Eh	Init Boot Devices: The adapter ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
90h	Display IDE mass storage devices.
92h	Display USB mass storage devices.
94h	Report the first set of POST Errors To Error Manager.
96h	Boot Password Check: The password was checked. Performing any required programming before Setup next.
98h	Float Processor Initialize: Performing any required initialization before the coprocessor test next.
9Ah	Enable Interrupts 0,1,2: Checking the extended keyboard, keyboard ID, and NUM Lock key next. Issuing the keyboard ID command next
9Ch	Init FDD Devices. Report second set of POST errors To Error messager
9Eh	Extended background memory test end
A0h	Prepare And Run Setup: Error manager displays and logs POST errors. Waits for user input for certain errors. Execute setup.
A2h	Set Base Expansion Memory Size
A4h	Program chipset setup options, build ACPI tables, build INT15h E820h table
A6h	Set Display Mode
A8h	Build SMBIOS table and MP tables.
AAh	Clear video screen.
ACh	Prepare USB controllers for operating system
AEh	One Beep to indicate end of POST. No beep if silent boot is enabled.
F2h	Enable USB function/Clock. Initialize GPC for USB. GPC initialization consist of USB initialization and APM initialization.
F5h	Validate the NVRAM area. Called at check point 27h.
000h	POST completed. Passing control to INT 19h boot loader next.

9.11.1 POST Error Codes and Messages

The following table defines POST error codes and their associated messages. The BIOS prompts the user to press a key in case of serious errors. Some of the error messages are

preceded by the string "Error" to highlight the fact that the system might be malfunctioning. All POST errors and warnings are logged in the system event log, unless the SEL is full.

Table 55. Standard POST Error Messages and Codes

Error Code	Error Message	Pause on Boot
100	Timer Channel 2 Error	Yes
101	Master Interrupt Controller	Yes
102	Slave Interrupt Controller	Yes
103	CMOS Battery Failure	Yes
104	CMOS Options not Set	Yes
105	CMOS Checksum Failure	Yes
106	CMOS Display Error	Yes
107	Insert Key Pressed	Yes
108	Keyboard Locked Message	Yes
109	Keyboard Stuck Key	Yes
10A	Keyboard Interface Error	Yes
10B	System Memory Size Error	Yes
10E	External Cache Failure	Yes
110	Floppy Controller Error	Yes
111	Floppy A: Error	Yes
112	Floppy B: Error	Yes
113	Hard disk 0 Error	Yes
114	Hard disk 1 Error	Yes
115	Hard disk 2 Error	Yes
116	Hard disk 3 Error	Yes
117	CD-ROM disk 0 Error	Yes
118	CD-ROM disk 1 Error	Yes
119	CD-ROM disk 2 Error	Yes
11A	CD-ROM disk 3 error	Yes
11B	Date/Time not set	Yes
11E	Cache memory bad	Yes
120	CMOS clear	Yes
121	Password clear	Yes
140	PCI Error	Yes
141	PCI Memory Allocation Error	Yes
142	PCI IO Allocation Error	Yes
143	PCI IRQ Allocation Error	Yes
144	Shadow of PCI ROM Failed	Yes
145	PCI ROM not found	Yes
146	Insufficient Memory to Shadow PCI ROM	Yes

Table 56. Extended POST Error Messages and Codes

Error Code	Error Message	Pause on Boot
8100	Processor 1 failed BIST	No
8101	Processor 2 failed BIST	No
8110	Processor 1 Internal error (IERR)	No
8111	Processor 2 Internal error (IERR)	No
8120	Processor 1 Thermal Trip error	No
8121	Processor 2 Thermal Trip error	No
8130	Processor 1 disabled	No
8131	Processor 2 disabled	No
8140	Processor 1 failed FRB-3 timer	No
8141	Processor 2 failed FRB-3 timer	No
8150	Processor 1 failed initialization on last boot.	No
8151	Processor 2 failed initialization on last boot.	No
8160	Processor 01: unable to apply BIOS update	Yes
8161	Processor 02: unable to apply BIOS update	Yes
8170	Processor P1 :L2 cache Failed	Yes
8171	Processor P2 :L2 cache Failed	Yes
8180	BIOS does not support current stepping for Processor P1	Yes
8181	BIOS does not support current stepping for Processor P2	Yes
8190	Watchdog Timer failed on last boot	No
8191	4:1 Core to bus ratio: Processor Cache disabled	Yes
8192	L2 Cache size mismatch	Yes
8193	CPUID, Processor Stepping are different	Yes
8194	CPUID, Processor Family are different	Yes
8195	Front Side Bus Speed mismatch. System Halted	Yes, Halt
8196	Processor Model are different	Yes
8197	CPU Speed mismatch	Yes
8198	Failed to load processor microcode	Yes
8199	Boot processor failed BIST	Yes
8300	Baseboard Management Controller failed to function	Yes
8301	Front Panel Controller failed to Function	Yes
8305	Hotswap Controller failed to Function	Yes
8306	OS Boot watchdog timer failure	Yes
8307	BIOS/POST watchdog timer failure	Yes
8310	Change in server management configuration	No
8420	Intelligent System Monitoring Chassis Opened	Yes
84F1	Intelligent System Monitoring Forced Shutdown	Yes
84F2	Server Management Interface Failed	Yes
84F3	BMC in Update Mode	Yes
84F4	Sensor Data Record Empty	Yes
84FF	System Event Log Full	No
8500	Bad or missing memory in slot 2A	Yes
8501	Bad or missing memory in slot 1A	Yes
8504	Bad or missing memory in slot 2B	Yes
8505	Bad or missing memory in slot 1B	Yes

Error Code	Error Message	Pause on Boot
8601	All Memory marked as fail. Forcing minimum back online.	Yes

9.11.2 POST Error Beep Codes

The following three tables list POST error beep codes. Prior to system video initialization, BIOS uses these beep codes to inform users on error conditions. Short beeps will be generated and an error code will be posted on debug port 80h.

9.11.2.1 BIOS Recovery Beep Codes

In the case of a Bootblock update, where video is not available for text messages to be displayed, speaker beeps are necessary to inform the user of any errors. The following table describes the type of error beep codes that may occur during the Bootblock update.

Table 57. BIOS Recovery Beep Codes

Beeps	Error message	POST Progress Code	Description
1	Recovery started		Start recovery process
2	Recovery boot error	Flashing series of post codes: E9h EEh EBh ECh EFh	Unable to boot to floppy, ATAPI, or ATAPI CD-ROM. Recovery process will retry.
Series of long low-pitched single beeps	Recovery failed	EEh	Unable to process valid BIOS recovery images. BIOS already passed control to operating system and flash utility.
2 long high-pitched beeps	Recovery complete	EFh	BIOS recovery succeeded, ready for power-down, reboot.
3	Recovery Failed	F0h	Recovery diskette is not bootable or a recovery diskette is not inserted.

Recovery BIOS will generate two beeps and flash post code sequence of E9h, EAh, EBh, ECh, and EFh on the Port 80 diagnostic LEDs.

During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beeps. Failure is indicated by a long series of short beeps.

9.11.2.2 Bootblock Error Beep Codes

Table 58. Bootblock Error Beep Codes

Beeps	Error message	Description

Beeps	Error message	Description
1	Refresh timer failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity error	Parity can not be reset
3	Boot Block Failure	Boot Block Failure failure. **See "3-Beep-Boot Block Failure Error Code" table for additional error details.
4	System timer	System timer is not operational
5	Processor failure	Processor failure detected
6	Keyboard controller Gate A20 failure	The keyboard controller may be bad. The BIOS cannot switch to protected mode.
7	Processor exception interrupt error	The CPU generated an exception interrupt.
8	Display memory read/write error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM checksum error	System BIOS ROM checksum error
10	Shutdown register error	Shutdown cmos register read/write error detected
11	Invalid BIOS	General BIOS ROM error

Table 59. 3-Beep Boot Block Failure Error Codes

Beep Code	POST Code	Description
3	00h	No memory was found in the system
3	01h	Memory mixed type detected
3	02h	EDO is not supported
3	03h	First row memory test failure
3	04h	Mismatched DIMMs in a row
3	05h	Base memory test failure
3	06h	Failure on decompressing post module
3	07h-0Dh	Generic memory error
3	0Eh	SMBUS protocol error
3	0Fh	Generic memory error
3	DDh	CPU microcode cannot be found for processor in slot 0.
3	EEh	CPU microcode cannot be found for processor in slot 1.

Note: For beep codes controlled by the BMC in the format or 1-5-x-x refer to section 7.5.5 BMC Diagnostics and Beep Code Generation.

9.12 "POST Error Pause" Option

In case of POST error(s), which occur during system boot-up, BIOS will stop and wait for the user to press an appropriate key before booting the operating system or entering BIOS setup. The user can override this option by setting "POST Error Pause" to "Disabled" in BIOS setup

Advanced menu page. If "POST Error Pause" option is selected to "disabled", the system will boot the operating system without user-intervention. Option default value is set to "enabled".

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10. Connectors and Headers

10.1 Main Power Connector

The main power supply connection is obtained using the 24-pin connector. The following table defines the pin-outs of the connector.

Table 60. Power Connector Pin-out (J9B13)

Pin	Signal	Color	Pin	Signal	Color
1	+3.3V	Orange	13	+3.3V	Orange
2	+3.3V	Orange	14	-12V	Blue
3	GND	Black	15	GND	Black
4	+5V	Red	16	PS_ON#	Green
5	GND	Black	17	GND	Black
6	+5V	Red	18	GND	Black
7	GND	Black	19	GND	Black
8	PWR_OK	Gray	20	RSVD_(5V)	White
9	5VSB	Purple	21	+5V	Red
10	+12V	Yellow	22	+5V	Red
11	+12V	Yellow	23	+5V	Red
12	+3.3V	Orange	24	GND	Black

Table 61. Power Supply Signal Connector (J9B27)

Pin	Signal	Color
1	5VSB_SCL	Orange
2	5VSB_SDA	Black
3	PS_ALERT_L	Red
4	GND	Yellow
5	3.3V SENSE(+)	Green

Table 62. 12V Power Connector (J4K10)

Pin	Signal	Color
1	GND	Black
2	GND	Black
3	GND	Black
4	GND	Black
5	+12Vdc	Yellow
6	+12Vdc	Yellow
7	+12Vdc	Yellow
8	+12Vdc	Yellow

10.2 Memory Module Connector

The SE7501BR2 server board has four DIMM connectors and supports registered ECC DDR modules. For additional DIMM information, refer to the *DDR266 Registered DIMM Specification.*

Table 63. DIMM Connectors (J8D1, J8D7, J8D15, J8D22)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	34	GND	67	DQS5	100	GND	133	DQ31	166	DQ53
2	DQ0	35	DQ25	68	DQ42	101	NC	134	CB4	167	FETEN
3	GND	36	DQS3	69	DQ43	102	NC	135	CB5	168	VDD
4	DQ1	37	A4	70	VDD	103	A13	136	VDDQ	169	DM6
5	DQS0	38	VDD	71	RSVD	104	VDDQ	137	CK0P	170	DQ54
6	DQ2	39	DQ26	72	DQ48	105	DQ12	138	CK0N	171	DQ55
7	VDD	40	DQ27	73	DQ49	106	DQ13	139	GND	172	VDDQ
8	DQ3	41	A2	74	GND	107	DM1	140	DM8	173	NC
9	NC	42	GND	75	RSVD	108	VDD	141	A10	174	DQ60
10	RESET*	43	A1	76	RSVD	109	DQ14	142	CB6	175	DQ61
11	GND	44	CB0	77	VDDQ	110	DQ15	143	VDDQ	176	GND
12	DQ8	45	CB1	78	DQS6	111	CKE1	144	CB7	177	DM7
13	DQ9	46	VDD	79	DQ50	112	VDDQ	145	GND	178	DQ62
14	DQS1	47	DQS8	80	DQ51	113	BA2	146	DQ36	179	DQ63
15	VDDQ	48	A0	81	GND	114	DQ20	147	DQ37	180	VDDQ
16	RSVD	49	CB2	82	VDDID	115	A12	148	VDD	181	SA0
17	RSVD	50	GND	83	DQ56	116	GND	149	DM4	182	SA1
18	GND	51	CB3	84	DQ57	117	DQ21	150	DQ38	183	SA2
19	DQ10	52	BA1	85	VDD	118	A11	151	DQ39	184	VDDSPD
20	DQ11	53	DQ32	86	DQS7	119	DM2	152	GND	185	NC
21	CKE0	54	VDDQ	87	DQ58	120	VDD	153	DQ44	186	NC
22	VDDQ	55	DQ33	88	DQ59	121	DQ22	154	RAS*	187	NC
23	DQ16	56	DQS4	89	GND	122	A8	155	DQ45		
24	DQ17	57	DQ34	90	NC	123	DQ23	156	VDDQ		
25	DQS2	58	GND	91	SDA	124	GND	157	CS0*		
26	GND	59	BA0	92	SCL	125	A6	158	CS1*		
27	A9	60	DQ35	93	GND	126	DQ28	159	DM5		
28	DQ18	61	DQ40	94	DQ4	127	DQ29	160	GND		
29	A7	62	VDDQ	95	DQ5	128	VDDQ	161	DQ46		
30	VDDQ	63	WE*	96	VDDQ	129	DM3	162	DQ47		
31	DQ19	64	DQ41	97	DM0	130	A3	163	RSVD		
32	A5	65	CAS*	98	DQ6	131	DQ30	164	VDDQ		
33	DQ24	66	GND	99	DQ7	132	GND	165	DQ52		

10.3 Processor Socket

The SE7501BR2 has two Socket 604 processor sockets. The following table provides the processor socket pin numbers and pin names:

Table 64. Socket 604 Processor Socket Pinout

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	Reserved	B6	VCC	C11	A30#	D16	A17#	E21	RS0#
A2	VCC	B7	A31#	C12	A23#	D17	A9#	E22	HIT#
A3	SKTOCC#	B8	A27#	C13	VSS	D18	VCC	E23	VSS
A4	Reserved	B9	VSS	C14	A16#	D19	ADS#	E24	TCK
A5	VSS	B10	A21#	C15	A15#	D20	BR0#	E25	TDO
A6	A32##	B11	A22#	C16	VCC	D21	VSS	E26	VCC
A7	A33#	B12	VCC	C17	A8#	D22	RS1#	E27	FERR#
A8	VCC	B13	A13#	C18	A6#	D23	BPRI#	E28	VCC
A9	A26#	B14	A12#	C19	VSS	D24	VCC	E29	VSS
A10	A20#	B15	VSS	C20	REQ3#	D25	Reserved	E30	VCC
A11	VSS	B16	A11#	C21	REQ2#	D26	VSSENSE	E31	VSS
A12	A14#	B17	VSS	C22	VCC	D27	VSS	F1	VCC
A13	A10#	B18	A5#	C23	DEFER#	D28	VSS	F2	VSS
A14	VCC	B19	REQ0#	C24	TDI	D29	VCC	F3	VID0
A15	Reserved	B20	VCC	C25	VSS	D30	VSS	F4	VCC
A16	Reserved	B21	REQ1#	C26	IGNNE#	D31	VCC	F5	BPM3#
A17	LOCK#	B22	REQ4#	C27	SMI#	E1	VSS	F6	BPM0#
A18	VCC	B23	VSS	C28	VCC	E2	VCC	F7	VSS
A19	A7#	B24	LINT0	C29	VSS	E3	VID1	F8	VPM1#
A20	A4#	B25	PROCHOT#	C30	VCC	E4	BPM5#	F9	GTLREF
A21	VSS	B26	VCC	C31	VSS	E5	IERR#	F10	VCC
A22	A3#	B27	VCCSENSE	D1	VCC	E6	VCC	F11	VINIT#
A23	HITM#	B28	VSS	D2	VSS	E7	BPM2#	F12	BR1#
A24	VCC	B29	VCC	D3	VID2	E8	BPM4#	F13	VSS
A25	TMS	B30	VSS	D4	STPCLK#	E9	VSS	F14	ADSTB1#
A26	Reserved	B31	VCC	D5	VSS	E10	AP0#	F15	A19#
A27	VSS	C1	VSS	D6	INIT#	E11	BR2#[1]	F16	VCC
A28	VCC	C2	VCC	D7	MCERR#	E12	VCC	F17	ADSTB0#
A29	VSS	C3	VID3	D8	VCC	E13	A28#	F18	DBSY#
A30	VCC	C4	VCC	D9	AP1#	E14	A24#	F19	VSS
A31	VSS	C5	Reserved	D10	BR3#[1]	E15	VSS	F20	BNR#
B1	Reserved	C6	RSP#	D11	VSS	E16	COMP1	F21	RS2#
B2	VSS	C7	VSS	D12	A29#	E17	VSS	F22	VCC
B3	VID4	C8	A35#	D13	A25#	E18	DRDY#	F23	GTLREF
B4	VCC	C9	A34#	D14	VCC	E19	TRDY#	F24	TRST#
B5	OTDEN	C10	VCC	D15	A18#	E20	VCC	F25	VSS

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
F26	THERMTRIP#	J3	VSS	L24	VCC	P1	VSS	T9	VSS
F27	A20M#	J4	VCC	L25	VSS	P2	VCC	T23	VSS
F28	VSS	J5	VSS	L26	VCC	P3	VSS	T24	VCC
F29	VCC	J6	VCC	L27	VSS	P4	VCC	T25	VSS
F30	VSS	J7	VSS	L28	VCC	P5	VSS	T26	VCC
F31	VCC	J8	VCC	L29	VSS	P6	VCC	T27	VSS
G1	VSS	J9	VSS	L30	VCC	P7	VSS	T28	VCC
G2	VCC	J23	VSS	L31	VSS	P8	VCC	T29	VSS
G3	VSS	J24	VCC	M1	VCC	P9	VSS	T30	VCC
G4	VCC	J25	VSS	M2	VSS	P23	VSS	T31	VSS
G5	VSS	J26	VCC	M3	VCC	P24	VCC	U1	VCC
G6	VCC	J27	VSS	M4	VSS	P25	VSS	U2	VSS
G7	VSS	J28	VCC	M5	VCC	P26	VCC	U3	VCC
G8	VCC	J29	VSS	M6	VSS	P27	VSS	U4	VSS
G9	VSS	J30	VCC	M7	VCC	P28	VCC	U5	VCC
G23	LINT1	J31	VSS	M8	VSS	P29	VSS	U6	VSS
G24	VCC	K1	VCC	M9	VCC	P30	VCC	U7	VCC
G25	VSS	K2	VSS	M23	VCC	P31	VSS	U8	VSS
G26	VCC	K3	VCC	M24	VSS	R1	VCC	U9	VCC
G27	VSS	K4	VSS	M25	VCC	R2	VSS	U23	VCC
G28	VCC	K5	VCC	M26	VSS	R3	VCC	U24	VSS
G29	VSS	K6	VSS	M27	VCC	R4	VSS	U25	VCC
G30	VCC	K7	VCC	M28	VSS	R5	VCC	U26	VSS
G31	VSS	K8	VSS	M29	VCC	R6	VSS	U27	VCC
H1	VCC	K9	VCC	M30	VSS	R7	VCC	U28	VSS
H2	VSS	K23	VCC	M31	VCC	R8	VSS	U29	VCC
H3	VCC	K24	VSS	N1	VCC	R9	VCC	U30	VSS
H4	VSS	K25	VCC	N2	VSS	R23	VCC	U31	VCC
H5	VCC	K26	VSS	N3	VCC	R24	VSS	V1	VSS
H6	VSS	K27	VCC	N4	VSS	R25	VCC	V2	VCC
H7	VCC	K28	VSS	N5	VCC	R26	VSS	V3	VSS
H8	VSS	K29	VCC	N6	VSS	R27	VCC	V4	VCC
H9	VCC	K30	VSS	N7	VCC	R28	VSS	V5	VSS
H23	VCC	K31	VCC	N8	VSS	R29	VCC	V6	VCC
H24	VSS	L1	VSS	N9	VCC	R30	VSS	V7	VSS
H25	VCC	L2	VCC	N23	VCC	R31	VCC	V8	VCC
H26	VSS	L3	VSS	N24	VSS	T1	VSS	V9	VSS
H27	VCC	L4	VCC	N25	VCC	T2	VCC	V23	VSS
H28	VSS	L5	VSS	N26	VSS	T3	VSS	V24	VCC
H29	VCC	L6	VCC	N27	VCC	T4	VCC	V25	VSS
H30	VSS	L7	VSS	N28	VSS	T5	VSS	V26	VCC
H31	VCC	L8	VCC	N29	VCC	T6	VCC	V27	VSS
J1	VSS	L9	VSS	N30	VSS	T7	VSS	V28	VCC

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
J2	VCC	L23	VSS	N31	VCC	T8	VCC	V29	VSS
V30	VCC	Y22	VCC	AB1	VSS	AC11	D43#	AD21	D29#
V31	VSS	Y23	D5#	AB2	VCC	AC12	D41#	AD22	DBI1#
W1	VCC	Y24	D2#	AB3	BSEL1[b]	AC13	VSS	AD23	VSS
W2	VSS	Y25	VSS	AB4	VCCA	AC14	D50#	AD24	D21#
W3	Reserved	Y26	D0#	AB5	VSS	AC15	DP2#	AD25	D18#
W4	VSS	Y27	Reserved	AB6	D63#	AC16	VCC	AD26	VCC
W5	BCLK1	Y28	Reserved	AB7	PWRGOOD	AC17	D34#	AD27	D4#
W6	TESTHI0	Y29	SM_TS1_A1	AB8	VCC	AC18	DP0#	AD28	SM_ALERT#
W7	TESTHI1	Y30	VSS	AB9	DBI3#	AC19	VSS	AD29	SM_WP
W8	TESTHI2	Y31	VSS	AB10	D55#	AC20	D25#	AD30	VCC
W9	GTLREF	AA1	VCC	AB11	VSS	AC21	D26#	AD31	VSS
W23	GTLREF	AA2	VSS	AB12	D51#	AC22	VCC	AE2	VSS
W24	VSS	AA3	BSEL0[b]	AB13	D52#	AC23	D23#	AE3	VCC
W25	VCC	AA4	VCC	AB14	VCC	AC24	D20#	AE4	Reserved
W26	VSS	AA5	VSSA	AB15	D37#	AC25	VSS	AE5	TEST
W27	VCC	AA6	VCC	AB16	D32#	AC26	D17#	AE6	SLP#
W28	VSS	AA7	TESTHI4	AB17	D31#	AC27	DBI0#	AE7	D58#
W29	VCC	AA8	D61#	AB18	VCC	AC28	SM_CLK	AE8	VCC
W30	VSS	AA9	VSS	AB19	D14#	AC29	SM_DAT	AE9	D44#
W31	VCC	AA10	D54#	AB20	D12#	AC30	VSS	AE10	D42#
Y1	VSS	AA11	D53#	AB21	VSS	AC31	VCC	AE11	VSS
Y2	VCC	AA12	VCC	AB22	D13#	AD1	Reserved	AE12	DBI2#
Y3	Reserved	AA13	D48#	AB23	D9#	AD2	VCC	AE13	D35#
Y4	BCLK0	AA14	D49#	AB24	VCC	AD3	VSS	AE14	VCC
Y5	VSS	AA15	VSS	AB25	D8#	AD4	VCCIOPLL	AE15	Reserved
Y6	TESTHI3	AA16	D33#	AB26	D7#	AD5	TESTHI5	AE16	Reserved
Y7	VSS	AA17	VSS	AB27	VSS	AD6	VCC	AE17	DP3#
Y8	RESET#	AA18	D24#	AB28	SM_EP_A2	AD7	D57#	AE18	VCC
Y9	D62#	AA19	D15#	AB29	SM_EP_A1	AD8	D46#	AE19	DP1#
Y10	VCC	AA20	VCC	AB30	VCC	AD9	VSS	AE20	D28#
Y11	DSTBP3#	AA21	D11#	AB31	VSS	AD10	D45#	AE21	VSS
Y12	DSTBN3#	AA22	D10#	AC1	Reserved	AD11	D40#	AE22	D27#
Y13	VSS	AA23	VSS	AC2	VSS	AD12	VCC	AE23	D22#
Y14	DSTBP2#	AA24	D6#	AC3	VCC	AD13	D38#	AE24	VCC
Y15	DSTBN2#	AA25	D3#	AC4	VCC	AD14	D39#	AE25	D19#
Y16	VCC	AA26	VCC	AC5	D60#	AD15	VSS	AE26	D16#
Y17	DSTBP1#	AA27	D1#	AC6	D59#	AD16	COMP0	AE27	VSS
Y18	DSTBN1#	AA28	SM_TS1_A0	AC7	VSS	AD17	VSS	AE28	SM_VCC
Y19	VSS	AA29	SM_EP_A0	AC8	D56#	AD18	D36#	AE29	SM_VCC
Y20	DSTBP0#	AA30	VSS	AC9	D47#	AD19	D30#		
Y21	DSTBN0#	AA31	VCC	AC10	VCC	AD20	VCC		

Note:

a. These are “Reserved” pins on the Intel® Xeon™ processor. In systems utilizing the Intel® Xeon™ processor, the system designer must terminate these signals to the processor Vcc.
b. Base boards treating AA3 and AB3 as Reserved will operate correctly with a bus clock of 100MHz

10.4 System Management Headers

10.4.1 ICMB Header

Table 65. ICMBHeader Pin-out (J2A7)

Pin	Signal Name	Type	Description
1	5 V standby	Power	+5 V Standby
2	Transmit	Signal	UART signals
3	Transmit Enable	Signal	UART signals
4	Receive	Signal	UART signals
5	Ground	GND	

10.4.2 OEM IPMB Header

Table 66. IPMB Header Pin-out (J4K1)

Pin	Signal Name	Description
1	Local I2C SDA	BMC IMB 5 V Standby Data Line
2	GND	
3	Local I2C SCL	BMC IMB 5 V Standby Clock Line

10.4.3 SCSI IPMB Header

Table 67. IPMB Header Pin-out (J4K2, J4J5)

Pin	Signal Name	Description
1	5VSB SDA	Data Line
2	GND	
3	5VSB SCL	Clock Line
4	Not used	

10.5 PCI Slot Connector

There are three peer PCI buses implemented on the SE7501BR2 board. Segment A supports 5V PCI 32-bit/33MHz, segment B supports 3.3V PCI-X 64-bit, 100/66MHz, and segment C supports 3.3V PCI-X 64-bit, 133/100/66MHz operation. All segments supports full-length PCI add-in cards. The tables below list the characteristics for the PCI slots and their pin-out.

Table 68. PCI Slot Characteristics

Slot No.	Mode	Width	Speed[21]	Voltage	Notes
1	PCI-X	64-bit	133/100/66 MHz	3.3V	
2	PCI-X	64-bit	133/100/66 MHz	3.3V	
3	PCI-X	64-bit	100/66 MHz	3.3V	
4	PCI-X	64-bit	100/66 MHz	3.3V	Supports ZCR (Zero Channel RAID)
5	PCI	32-bit	33MHz	5V	
6	PCI	32-bit	33MHz	5V	

Table 69. Slot 1 PCI-X 64-bit 3.3V Pin-out (J4D12)

Pin	Side B	Side A	Pin	Side B	Side A
1	-12 V	TRST#	49	M66EN	AD[09]
2	TCK	+12 V	50	Ground	Ground
3	Ground	TMS	51	Ground	Ground
4	TDO	TDI	52	AD[08]	C/BE[0]#
5	+5 V	+5 V	53	AD[07]	+3.3 V
6	+5 V	INTA#	54	+3.3 V	AD[06]
7	INTB#	INTC#	55	AD[05]	AD[04]
8	INTD#	+5 V	56	AD[03]	Ground
9	PRSNT1#	SLOT1_REQ#	57	Ground	AD[02]
10	SLOT2_GNT#	+3.3 V	58	AD[01]	AD[00]
11	PRSNT2#	SLOT1_GNT#	59	+3.3 V	+3.3 V
12	**Connector Key**	**Connector Key**	60	ACK64#	REQ64#
13	**Connector Key**	**Connector Key**	61	+5 V	+5 V
14	SLOT2_REQ#	3.3 VAUX	62	+5 V	+5 V
15	Ground	RST#		**Connector Key**	**Connector Key**
16	CLK	+3.3 V		**Connector Key**	**Connector Key**
17	Ground	GNT#	63	RISER_CLK1	Ground
18	REQ#	Ground	64	Ground	C/BE[7]#
19	+3.3 V	PME#	65	C/BE[6]#	C/BE[5]#
20	AD[31]	AD[30]	66	C/BE[4]#	+3.3 V
21	AD[29]	+3.3 V	67	Ground	PAR64
22	Ground	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Ground
24	AD[25]	Ground	70	+3.3 V	AD[60]
25	+3.3 V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]#	IDSEL	72	AD[57]	Ground

[21] The actual bus mode/speed for segment C (Slots 1 and 2) and segment B (Slot 3 and 4) will be determined by the least capable card installed on that bus. For segment C, the system BIOS will program the bus at 133MHz when one slot is populated, and at 100MHz when two slots are populated.

Pin	Side B	Side A	Pin	Side B	Side A
27	AD[23]	+3.3 V	73	Ground	AD[56]
28	Ground	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	+3.3 V
30	AD[19]	Ground	76	Ground	AD[52]
31	+3.3 V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Ground
33	C/BE[2]#	+3.3V	79	+3.3 V	AD[48]
34	Ground	FRAME#	80	AD[47]	AD[46]
35	IRDY#	Ground	81	AD[45]	Ground
36	+3.3 V	TRDY#	82	Ground	AD[44]
37	DEVSEL#	Ground	83	AD[43]	AD[42]
38	PCIXCAP	STOP#	84	AD[41]	+3.3 V
39	LOCK#	+3.3 V	85	Ground	AD[40]
40	PERR#	SMBUS SCL	86	AD[39]	AD[38]
41	+3.3 V	SMBUS SDA	87	AD[37]	Ground
42	SERR#	Ground	88	+3.3 V	AD[36]
43	+3.3 V	PAR	89	AD[35]	AD[34]
44	C/BE[1]#	AD[15]	90	AD[33]	Ground
45	AD[14]	+3.3 V	91	Ground	AD[32]
46	Ground	AD[13]	92	SLOT_INT1#	SLOT_INT2#
47	AD[12]	AD[11]	93	RISER_PRESENCE#	GND
48	AD[10]	Ground	94	Ground	RISER_CLK2

Table 70. Slot 2 & 3 PCI-X 64bit 3.3V Pin-out (J3D15, J3D14)

Pin	Side B	Side A	Pin	Side B	Side A
1	-12 V	TRST#	49	M66EN	AD[09]
2	TCK	+12 V	50	Ground	Ground
3	Ground	TMS	51	Ground	Ground
4	TDO	TDI	52	AD[08]	C/BE[0]#
5	+5 V	+5 V	53	AD[07]	+3.3 V
6	+5 V	INTA#	54	+3.3 V	AD[06]
7	INTB#	INTC#	55	AD[05]	AD[04]
8	INTD#	+5 V	56	AD[03]	Ground
9	PRSNT1#	RSV	57	Ground	AD[02]
10	RSV	+3.3 V	58	AD[01]	AD[00]
11	PRSNT2#	RSV	59	+3.3 V	+3.3 V
12	**Connector Key**	**Connector Key**	60	ACK64#	REQ64#
13	**Connector Key**	**Connector Key**	61	+5 V	+5 V
14	RSV	3.3 VAUX	62	+5 V	+5 V
15	Ground	RST#		**Connector Key**	**Connector Key**
16	CLK	+3.3 V		**Connector Key**	**Connector Key**
17	Ground	GNT#	63	RSV	Ground
18	REQ#	Ground	64	Ground	C/BE[7]#

Pin	Side B	Side A	Pin	Side B	Side A
19	+3.3 V	PME#	65	C/BE[6]#	C/BE[5]#
20	AD[31]	AD[30]	66	C/BE[4]#	+3.3 V
21	AD[29]	+3.3 V	67	Ground	PAR64
22	Ground	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Ground
24	AD[25]	Ground	70	+3.3 V	AD[60]
25	+3.3 V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]#	IDSEL	72	AD[57]	Ground
27	AD[23]	+3.3 V	73	Ground	AD[56]
28	Ground	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	+3.3 V
30	AD[19]	Ground	76	Ground	AD[52]
31	+3.3 V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Ground
33	C/BE[2]#	+3.3V	79	+3.3 V	AD[48]
34	Ground	FRAME#	80	AD[47]	AD[46]
35	IRDY#	Ground	81	AD[45]	Ground
36	+3.3 V	TRDY#	82	Ground	AD[44]
37	DEVSEL#	Ground	83	AD[43]	AD[42]
38	Ground	STOP#	84	AD[41]	+3.3 V
39	LOCK#	+3.3 V	85	Ground	AD[40]
40	PERR#	SMBUS SCL	86	AD[39]	AD[38]
41	+3.3 V	SMBUS SDA	87	AD[37]	Ground
42	SERR#	Ground	88	+3.3 V	AD[36]
43	+3.3 V	PAR	89	AD[35]	AD[34]
44	C/BE[1]#	AD[15]	90	AD[33]	Ground
45	AD[14]	+3.3 V	91	Ground	AD[32]
46	Ground	AD[13]	92	RSV	RSV
47	AD[12]	AD[11]	93	RSV	GND
48	AD[10]	Ground	94	Ground	RSV

Table 71. Slot 4 PCI-X 64-bit 3.3V ZCR (Zero Channel RAID) Pin-out (J2D11)

Pin	Side B	Side A	Pin	Side B	Side A
1	-12 V	TRST#	49	M66EN	AD[09]
2	TCK	+12 V	50	Ground	Ground
3	Ground	TMS(PA_TMS)	51	Ground	Ground
4	TDO	TDI (ROMB_PRESENT_L)	52	AD[08]	C/BE[0]#
5	+5 V	+5 V	53	AD[07]	+3.3 V
6	+5 V	INTA#	54	+3.3 V	AD[06]
7	INTB#	INTC#	55	AD[05]	AD[04]
8	INTD#	+5 V	56	AD[03]	Ground

Pin	Side B	Side A	Pin	Side B	Side A
9	PRSNT1#	RSV	57	Ground	AD[02]
10	RSV	+3.3 V	58	AD[01]	AD[00]
11	PRSNT2#	RSV	59	+3.3 V	+3.3 V
12	**Connector Key**	**Connector Key**	60	ACK64#	REQ64#
13	**Connector Key**	**Connector Key**	61	+5 V	+5 V
14	RSV	3.3 VAUX	62	+5 V	+5 V
15	Ground	RST#		**Connector Key**	**Connector Key**
16	CLK	+3.3 V		**Connector Key**	**Connector Key**
17	Ground	GNT#	63	RSV	Ground
18	REQ#	Ground	64	Ground	C/BE[7]#
19	+3.3 V	PME#	65	C/BE[6]#	C/BE[5]#
20	AD[31]	AD[30]	66	C/BE[4]#	+3.3 V
21	AD[29]	+3.3 V	67	Ground	PAR64
22	Ground	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Ground
24	AD[25]	Ground	70	+3.3 V	AD[60]
25	+3.3 V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]#	IDSEL	72	AD[57]	Ground
27	AD[23]	+3.3 V	73	Ground	AD[56]
28	Ground	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	+3.3 V
30	AD[19]	Ground	76	Ground	AD[52]
31	+3.3 V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Ground
33	C/BE[2]#	+3.3V	79	+3.3 V	AD[48]
34	Ground	FRAME#	80	AD[47]	AD[46]
35	IRDY#	Ground	81	AD[45]	Ground
36	+3.3 V	TRDY#	82	Ground	AD[44]
37	DEVSEL#	Ground	83	AD[43]	AD[42]
38	Ground	STOP#	84	AD[41]	+3.3 V
39	LOCK#	+3.3 V	85	Ground	AD[40]
40	PERR#	SMBUS SCL	86	AD[39]	AD[38]
41	+3.3 V	SMBUS SDA	87	AD[37]	Ground
42	SERR#	Ground	88	+3.3 V	AD[36]
43	+3.3 V	PAR	89	AD[35]	AD[34]
44	C/BE[1]#	AD[15]	90	AD[33]	Ground
45	AD[14]	+3.3 V	91	Ground	AD[32]
46	Ground	AD[13]	92	RSV	RSV
47	AD[12]	AD[11]	93	RSV	GND
48	AD[10]	Ground	94	Ground	RSV

Table 72. Slots 5 & 6 PCI 32-bit 5V Pin-out (J2C1, J1C11)

Pin	Side B	Side A	Pin	Side B	Side A

Pin	Side B	Side A	Pin	Side B	Side A
1	-12 V	TRST#	32	AD[17]	AD[16]
2	TCK	+12 V	33	C/BE[2]#	+3.3 V
3	Ground	TMS	34	Ground	FRAME#
4	TDO	TDI	35	IRDY#	Ground
5	+5 V	+5 V	36	+3.3 V	TRDY#
6	+5 V	INTA#	37	DEVSEL#	Ground
7	INTB#	INTC#	38	Ground	STOP#
8	INTD#	+5 V	39	LOCK#	+3.3 V
9	PRSNT1#	RSV	40	PERR#	SMBUS CLK
10	RSV	+5 V (I/O)	41	+3.3 V	SMBUS DAT
11	PRSNT2#	RSV	42	SERR#	Ground
12	Ground	Ground	43	+3.3 V	PAR
13	Ground	Ground	44	C/BE[1]#	AD[15]
14	RSV	3.3 VSB	45	AD[14]	+3.3 V
15	Ground	RST#	46	Ground	AD[13]
16	CLK	+5 V (I/O)	47	AD[12]	AD[11]
17	Ground	GNT#	48	AD[10]	Ground
18	REQ#	Ground	49	Ground	AD[09]
19	+5 V	PME#	50	**Connector Key**	**Connector Key**
20	AD[31]	AD[30]	51	**Connector Key**	**Connector Key**
21	AD[29]	+3.3 V	52	AD[08]	C/BE[0]#
22	Ground	AD[28]	53	AD[07]	+3.3 V
23	AD[27]	AD[26]	54	+3.3 V	AD[06]
24	AD[25]	Ground	55	AD[05]	AD[04]
25	+3.3 V	AD[24]	56	AD[03]	Ground
26	C/BE[3]#	IDSEL	57	Ground	AD[02]
27	AD[23]	+3.3 V	58	AD[01]	AD[00]
28	Ground	AD[22]	59	+5 V	+5 V (I/O)
29	AD[21]	AD[20]	60	ACK64#	REQ64#
30	AD[19]	Ground	61	+5 V	+5 V
31	+3.3 V	AD[18]	62	+5 V	+5 V

10.6 Front Panel Connectors

A standard SSI 34-pin header (J1J2) is provided to support a system front panel. The headers contain reset, NMI, power control buttons, and LED indicators. The following tables detail the pin outs of the headers.

Table 73. Front Panel 34-Pin Header Pin-out (J1J2)

Pin	Signal Name	Pin	Signal Name
1	Power LED Anode	2	5VSB
3	Key	4	Fan Fail LED Anode
5	Power LED Cathode	6	Fan Fail LED Cathode
7	HDD Activity LED Anode	8	Power Fault LED Anode

Pin	Signal Name	Pin	Signal Name
9	HDD Activity LED Cathode	10	Power Fault LED Cathode
11	Power Switch	12	NIC#1 Activity LED Anode
13	GND (Power Switch)	14	NIC#1 Activity LED Cathode
15	Reset Switch	16	I2C SDA
17	GND (Reset Switch)	18	I2C SCL
19	ACPI Sleep Switch	20	Chassis Intrusion
21	GND (ACPI Sleep Switch)	22	NIC#2 Activity LED Anode
23	NMI to CPU Switch	24	NIC#2 Activity LED Cathode
25	KEY	26	Key
27	ID LED Anode	28	System Ready Anode
29	ID LED Cathode	30	System Ready Cathode
31	ID Switch	32	HDD Fault Anode
33	GND (ID Switch)	34	HDD Fault Cathode

10.7 VGA Connector

The following table details the pin-out of the VGA connector.

Table 74. VGA Connector Pin-out (J7A6)

Pin	Signal Name
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND
6	GND
7	GND
8	GND
9	No connection
10	GND
11	No connection
12	DDCDAT
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	DDCCLK

10.8 SCSI Connector

The SE7501BR2 server board provides an internal wide SCSI connector. The following table details the pin-out of the SCSI connector.

Table 75. 68-pin SCSI Connector Pin-out (J1F1)

Connector Contact Number	Signal Name	Signal Name	Connector Contact Number
1	+DB(12)	-DB(12)	35
2	+DB(13)	-DB(13)	36
3	+DB(14)	-DB(14)	37
4	+DB(15)	-DB(15)	38
5	+DB(P1)	-DB(P1)	39
6	+DB(0)	-DB(0)	40
7	+DB(1)	-DB(1)	41
8	+DB(2)	-DB(2)	42
9	+DB(3)	-DB(3)	43
10	+DB(4)	-DB(4)	44
11	+DB(5)	-DB(5)	45
12	+DB(6)	-DB(6)	46
13	+DB(7)	-DB(7)	47
14	+DB(P)	-DB(P)	48
15	GROUND	GROUND	49
16	DIFFSENSE	GROUND	50
17	TERMPWR	TERMPWR	51
18	TERMPWR	TERMPWR	52
19	RESERVED	RESERVED	53
20	GROUND	GROUND	54
21	+ATN	-ATN	55
22	GROUND	GROUND	56
23	+BSY	-BSY	57
24	+ACK	-ACK	58
25	+RST	-RST	59
26	+MSG	-MSG	60
27	+SEL	-SEL	61
28	+C/D	-C/D	62
29	+REQ	-REQ	63
30	+I/O	-I/O	64
31	+DB(8)	-DB(8)	65
32	+DB(9)	-DB(9)	66
33	+DB(10)	-DB(10)	67
34	+DB(11)	-DB(11)	68

10.9 NIC Connectors

The SE7501BR2 server board provides two network interfaces using RJ45 connectors, one for the 10/100-Mbit Fast Ethernet (RJ45_MPG) (NIC1), and the other for the Gigabit Ethernet (RJ45_W_MAGNETIC) (NIC2). The following table details the pin-out of each connector.

Table 76. NIC1 10/100Mb RJ45_MPG Connector Pin-out (J5A16)

Pin	Signal Name	Pin	Signal Name
1	TXDP	2	TXDM
3	N/C	4	N/C
5	N/C	6	N/C
7	RXDP	8	RXDM
9	Activity LED Cathode	10	Link LED Anode
11	Speed LED Anode	12	3VSB

Table 77. NIC2 1.0Gb RJ45_W_MAGNETIC Connector Pin-out (J6A16)

Pin	Signal Name	Pin	Signal Name
1	P2V5	2	MDIA[1]-
3	MDIA[3]-	4	MDIA[2]+
5	MDIA[0]+	6	P2V5
7	P2V5	8	MDIA[3]+
9	MDIA[1]+	10	MDIA[0]-
11	MDIA[2]-	12	P2V5
13	LILED#	14	ACTLED#
15	LINKA 100#	16	LINKA 1000#

10.10 ATA Connectors

The SE7501BR2 board provides two 40-pin low-density ATA-100 connectors. The pin-out for both connectors is identical and is listed in the following table.

Table 78. ATA-100 40-pin Connectors Pin-out (J2J5, J1J24)

Pin	Signal Name	Pin	Signal Name
1	RESET_L	2	GND
3	DD7	4	IDE_DD8
5	DD6	6	IDE_DD9
7	DD5	8	IDE_DD10
9	DD4	10	IDE_DD11
11	DD3	12	IDE_DD12
13	DD2	14	IDE_DD13
15	DD1	16	IDE_DD14
17	DD0	18	IDE_DD15
19	GND	20	KEY
21	IDE_DMAREQ	22	GND
23	IDE_IOW_L	24	GND
25	IDE_IOR_L	26	GND
27	IDE_IORDY	28	GND
29	IDE_DMAACK_L	30	GND
31	IRQ_IDE	32	Test Point
33	IDE_A1	34	DIAG

Pin	Signal Name	Pin	Signal Name
35	IDE_A0	36	IDE_A2
37	IDE_DCS0_L	38	IDE_DCS1_L
39	IDE_HD_ACT_L	40	GND

10.11USB Connector

The SE7501BR2 server board supports three USB connectors, which are stacked in a single housing. The pin-out for each connector is identical and is detailed in the following table.

Table 79. USB Connectors Pin-out (J9A6)

Pin	Signal Name
1	USB_PWR<0> (Fused 5 V)
2	USB_BCK0_L
3	USB_BCK0
4	GND
5	USB_PWR<1> (Fused 5 V)
6	USB_BCK1_L
7	USB_BCK1
8	GND
9	USB_PWR<2> (Fused 5 V)
10	USB_BCK2_L
11	USB_BCK2
12	GND

In addition, a header on the server board (DH10) provides an option to support two additional USB ports. The pin-out of the header is detailed in the following table.

Table 80. Optional USB Connection Header Pin-out (J4J3)

Pin	Signal Name	Description
1	USB_PWR<5>	USB Port 5 Power
2	USB_PWR<4>	USB Port 4 Power
3	USB_BCK5_L	USB Port 5 Negative Signal
4	USB_BCK4_L	USB Port 4 Negative Signal
5	USB_BCK5	USB Port 5 Positive Signal
6	USB_BCK4	USB Port 4 Positive Signal
7	Ground	
8	Ground	
9	No Connect	KEY
10	TP_USB_OVRCUR3_L	Front Panel USB Overcurrent signal. This signal is not used

10.12 Floppy Connector

The SE7501BR2 server board provides a standard 34-pin interface to the floppy drive controller. The following tables detail the pin-out of the 34-pin legacy floppy connector.

Table 81. Legacy 34-pin Floppy Connector Pin-out (J4J3)

Pin	Signal Name	Pin	Signal Name
1	GND	2	FD_DENSEL0
3	GND	4	Test Point
5	KEY	6	FD_DENSEL1
7	GND	8	FD_INDEX_L
9	GND	10	FD_MTR0_L
11	GND	12	FD_DS1_L
13	GND	14	FD_DS0_L
15	GND	16	FD_MTR1_L
17	Test Point	18	FD_DIR_L
19	GND	20	FD_STEP_L
21	GND	22	FD_WDATA_L
23	GND	24	FD_WGATE_L
25	GND	26	FD_TRK0_L
27	Test Point	28	VCC
29	GND	30	FD_RDATA_L
31	GND	32	FD_HDSEL_L
33	GND	34	FD_DSKCHG_L

10.13 Serial Port Connector

The SE7501BR2 supports two serial ports:

- A DB-9 connector located on the back I/O area of the baseboard enabling Serial Port A
- A 9-pin DH-10 header on the server board (J1B11) enables an optional Serial Port B port

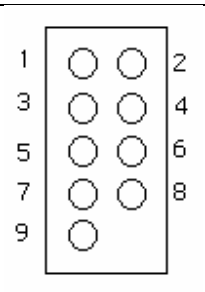
The following tables detail the pin-outs of these two ports:

Table 82. Rear DB-9 Serial A Port Pin-out (J8A18)

Pin	Signal Name	Description
7	RTS	Request To Send
4	DTR	Data Terminal Ready
3	TD	Transmit Data
5	SGND	Signal Ground
9	RI	Ring Indicate
2	RD	Receive Data
1	DCD	Carrier Detect
8	CTS	Clear to send

6	DSR	Data Set Ready

Table 83. 9-pin Header Serial B Port Pin-out (J1B11)

Pin	Signal Name	Description	COM2 Pin-out
1	DCD	Carrier Detect	
2	DSR	Data Set Ready	
3	RD	Receive Data	
4	RTS	Request To Send	
5	TD	Transmit Data	
6	CTS	Clear To Send	
7	DTR	Data Terminal Ready	
8	RI	Ring Indicator	
9	SGND	Signal Ground	

10.14 Parallel Port

The SE7501BR2 supports one DB-25 parallel port connector provided on the rear I/O. The following table details the pin-out of the connector.

Table 84. DB-25 Parallel Port Pin-out (J7A28)

Pin	Signal Name	Pin	Signal Name
1	STROBE_L	2	DATA0
3	DATA1	4	DATA2
5	DATA3	6	DATA4
7	DATA5	8	DATA6
9	DATA7	10	ACK_L
11	BUSY	12	PAPER_END
13	SELECT	14	AUTOFD_L
15	ERROR_L	16	INIT_L
17	SLCT_INPUT_L	18	GND
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	GND		

10.15 Keyboard and Mouse Connector

Two stacked PS/2* ports are provided in a single housing for keyboard and mouse support. Although the board set supports swapping of these connections, the top port is color-coded green to designate mouse support, and the bottom port is color-coded violet to designate keyboard support. The following table details the pin-out of the PS/2 connectors.

Table 85. Keyboard and Mouse PS2 Connector Pin-out (J9A5)

Keyboard		Mouse	
Pin	**Signal Name**	**Pin**	**Signal Name**
1	KBDATA	1	MSDATA
2	N/C	2	N/C
3	GND	3	GND
4	Fused 5V	4	Fused 5V
5	KBCLK	5	MSCLK
6	N/C	6	N/C

10.16 Fan Headers

The SE7501BR2 server board provides eight 3-pin fan headers. The fans are labeled “Sys Fan1” through “Sys Fan6”, “CPU1 Fan”, and “CPU2 Fan”. All “Sys Fan*X*” connectors have variable speed control and are capable of supporting variable speed fans. CPU1 Fan and CPU2 Fan will only support steady 12-volt power and cannot support variable speed fans. They will only support fan types that do not require controlled speed, such as those used on CPU fan heat sinks.

Table 86. 3-pin CPU Fan Headers Pin-out (J7F21, J5F1)

Pin	Signal Name	Type	Description
1	Ground	Power	GROUND is the power supply ground
2	Fan Power	Power	Straight 12V
3	Fan Tach	Out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

Table 87. 3-pin System Fan Headers Pin-out (J7B12, J7B11, J1K14, J2K5, J4K6, J4K11)

Pin	Signal Name	Type	Description
1	Ground	Power	GROUND is the power supply ground
2	Fan Power	Power	Variable Speed Fan Power
3	Fan Tach	Out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

10.16.1 Intel Server Chassis Fan Connections

The following section describes the proper chassis fans connections to the server boards’ fan headers for all supported Intel Server Chassis.

Table 88. Intel Server Chassis SC5250-E

Fan Location	Fan Label	Fan Size	Server Board Fan Header
Back of chassis above ATX I/O panel	NA	120x38mm	SYS FAN2 (J7B11)
Front of hard drive cage	NA	92x25mm	SYS FAN5 (J2K6)

Table 89. Intel Server Chassis SC5200 Base and Base Redundant Power

Fan Location	Fan Label	Fan Size	Server Board Fan Header
Back of chassis closest to memory connectors	NA	80x25mm	SYS FAN1 (J7B12)
Back of chassis closest to PCI slots	NA	80x25mm	SYS FAN2 (J7B11)
Front of chassis closest to IDE connectors	NA	80x32mm	SYS FAN3 (J1K14)
Front of chassis closest to processor sockets	NA	80x32mm	SYS FAN4 (J2K5)

Table 90. Intel Server Chassis SC5200 Hot-Swap Redundant Power

Fan Location	Fan Label	Fan Size	Server Board Fan Header
Back of chassis closest to memory connectors	Fan1	80x38mm	SYS FAN1 (J7B12)
Back of chassis closest to PCI slots	Fan2	80x38mm	SYS FAN2 (J7B11)
Front of chassis closest to IDE connectors - back	Fan3	92x25mm	SYS FAN3 (J1K14)
Front of chassis closest to IDE connectors - front	Fan4	92x25mm	SYS FAN4 (J2K5)
Front of chassis closest to processor sockets	Fan5	80x38mm	SYS FAN5 (J2K6)

Table 91. Intel Server Rack SR1350-E

Fan Location	Fan Label	Fan Size	Server Board Fan Header
Back of chassis closest to outer edge	Fan6	40x40mm	SYS FAN1 (J7B12)
Back of chassis closest to I/O shield	Fan7	40x40mm	SYS FAN2 (J7B11)
Front of chassis closest power supply	Fan1	40x40mm	CPU1 FAN (J7F21)
Front of chassis next to Fan1	Fan2	40x40mm	SYS FAN3 (J1K14)
Front of chassis next to Fan2	Fan3	40x40mm	CPU2 FAN (J5F1)
Front of chassis next to Fan3	Fan4	40x40mm	SYS FAN4 (J2K5)
Front of chassis closest to intrusion switch	Fan5	40x40mm	SYS FAN5 (J2K6)

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11. Configuration Jumpers

This section describes configuration jumper options on the SE7501BR2 server board.

11.1 System Recovery and Update Jumpers

SE7501BR2 provides 2 jumper blocks. One 11-pin single inline header (J1H1), located on the edge of the baseboard next to the Front Panel connector, provides a total of three 3-pin jumper blocks that are used to configure several system recovery and update options. The second 3-pin header (J1J1) provides a 3-pin jumper block that is used to configure BMC recovery options. The figure below shows the factory default locations for each jumper option.

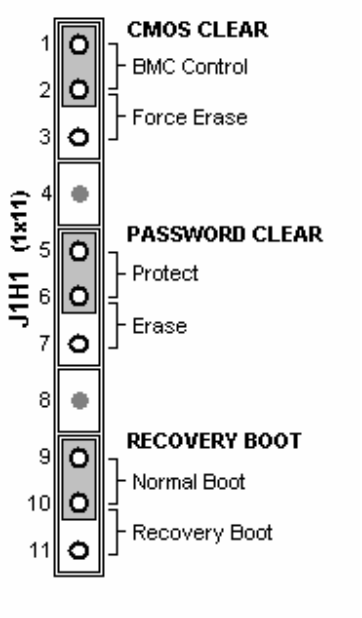

Figure 13. SE7501BR2 Configuration Jumpers (J1H1)

The following table describes each jumper option.

Table 92. Configuration Jumper Options

Option	Description
CMOS Clear	If pins 1 and 2 are jumpered (default), preservation of configuration CMOS through system reset is controlled by the BMC. If pins 2 and 3 are jumpered, CMOS contents are set to manufacturing default during system reset.
Password Clear	If pins 1 and 2 are jumpered (default), the current BIOS Setup Utility passwords are maintained during system reset. If pins 2 and 3 are jumpered, the Administrator and user passwords are cleared on reset.
Recovery Boot	If pins 1 and 2 are jumpered (default) the system will attempt to boot using the BIOS programmed in the Flash memory. If pins 2 and 3 are jumpered, the BIOS will attempt a recovery boot, loading BIOS code from a floppy disk into the Flash device. This is typically used when the BIOS code has been corrupted.

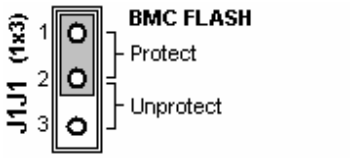

Figure 14. SE7501BR2 BMC Configuration Jumpers (J1J1)

The following table describes the jumper option.

Table 93. BMC Configuration Jumper Options

Option	Description
BMC Boot Block	If pins 1 and 2 are jumpered (default) the BMC will write-protect the BMC Flash. If pins 2 and 3 are jumpered, the BMC will unlock the boot block for update.

Note: The "BMC Flash" configuration jumper should only be moved from its factory default setting in the rare event of having to update the BMC Boot Block. Moving the "BMC Flash" jumper is **NOT** necessary if only the BMC operational code is being updated. Release Notes that accompany all BMC updates should inform the user if a Boot Block Update is required.

12. General Specifications

12.1 Absolute Maximum Ratings

Operating an SE7501BR2 baseboard at conditions beyond those shown in the following table may cause permanent damage to the system. The table is provided for stress testing purposes only. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 94. Absolute Maximum Ratings

Operating Temperature	0 degrees C to 55 degrees C
Storage Temperature	-40 degrees C to +70 degrees C
Voltage on any signal with respect to ground	-0.3 V to Vdd + 0.3V
3.3 V Supply Voltage with Respect to ground	-0.3 V to 3.63 V
5 V Supply Voltage with Respect to ground	-0.3 V to 5.5 V

Notes:

- Chassis design must provide proper airflow to avoid exceeding Intel® Xeon processor maximum case temperature.
- VDD means supply voltage for the device

12.2 Processor Power Support

The SE7501BR2 is designed to support the Thermal Design Point (TDP) guideline for Intel® Xeon™ processors. In addition, the Flexible Motherboard Guidelines (FMB) have been followed to help determine the suggested thermal and current design values for anticipating future processor needs. The following table provides maximum values for Icc, TDP power and T_{CASE} for the Intel® Xeon™ processor family

Table 95. Intel® Xeon™ processor DP TDP Guidelines

TDP Power	Max TCASE	Icc MAX
84.2W	81C	64.2A

Note: These values are for reference only. The Processor EMTS contains the actual specifications for the processor. If the values found in the EMTS are different then those published here, the EMTS values will supercede these, and should be used.

12.3 SE7501BR2 Power Budget

The following table shows the power consumed on each supply line for a SE7501BR2 server board that is configured as follows:

- two 2.4GHz Xeon® processors with 512KB cache (each 65W TDP). Two of these processors @ 80% VRM efficiency is equal to 13.55A.
- four DIMMs stacked burst, 70% max,

- 6 PCI add in cards
- 5 SCSI HDDs.

The numbers provided in the table should be used for reference purposes only. Different hardware configurations will produce different numbers. The numbers in the table reflect a common usage model operating at a higher than average stress level.

Table 96. SE7501BR2 Power Budget

SC5200	3.3V	5.V	12.V	5.VSB	
Processors (2.4GHz)			13.55A		
Memory/Keyboard/Mouse		1.00A	2.70A		
Server Board	2.90A	1.10A	2.20A	1.68A	
Fans			2.50A		
Hard Drives (5units)		4.70A	5.60A		
PCI Slots (6 cards)	12.12A	4.00A			
Peripherals		1.47A	1.10A		
Total Current	15.02A	12.27A	25.45A	1.68A	**Total Power**
Total Power	49.57W	61.35W	305.40W	8.38W	424.7W

12.4 Power Supply Specifications

This section provides power supply design guidelines for an SE7501BR2-based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 97. SE7501BR2 Power Supply Voltage Specification

Output	Min	Max	Tolerance
+3.3 V	3.20 V	3.46 V	+5 / -3 %
+5 V	4.80 V	5.25 V	+5 / -4 %
+12 V	11.52 V	12.6 V	+5 / -4 %
+5 V SB	4.80 V	5.25 V	+5/ -4%

12.4.1 Power Timing

This section discusses the timing requirements for operation with a single power supply. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 ms to 70 ms. The +3.3 V, +5 V and +12 V output voltages start to rise approximately at the same time. All outputs must rise monotonically. The +5 V output must be greater than the +3.3 V output during any point of the voltage rise, however, never by more than 2.25 V. Each output voltage shall reach regulation within 50 ms (T_{vout_on}) of each other and begin to turn off within 400 ms (T_{vout_off}) of each other. The following figure shows the output voltage timing parameters.

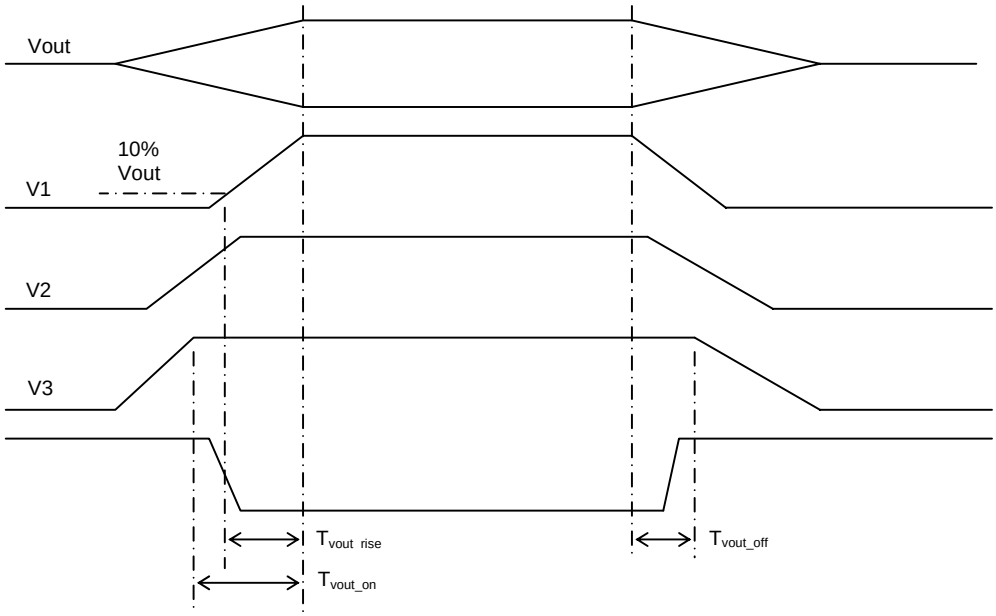

Figure 15. Output Voltage Timing

The following tables show the timing requirements for a single power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied. The ACOK# signal is not being used to enable the turn on timing of the power supply.

Table 98. Voltage Timing Parameters

Item	Description	Min	Max	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	70	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	msec
T_{vout_off}	All main outputs must leave regulation within this time.		400	msec

Table 99. Turn On / Off Timing

Item	Description	Min	Max	Units
Tsb_on_delay	Delay from AC being applied to 5VSB being within regulation.		1500	msec
T ac_on_delay	Delay from AC being applied to all output voltages being within regulation.		2500	msec
Tvout_holdup	Time all output voltages stay within regulation after loss of AC.	21		msec
Tpwok_holdup	Delay from loss of AC to de-assertion of PWOK	20		msec
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T pson_pwok	Delay from PSON# deactive to PWOK being de-asserted.		50	msec
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec

T pwok_off	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	2		msec
Tpwok_low	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		msec
Tsb_vout	Delay from 5 V SB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	msec

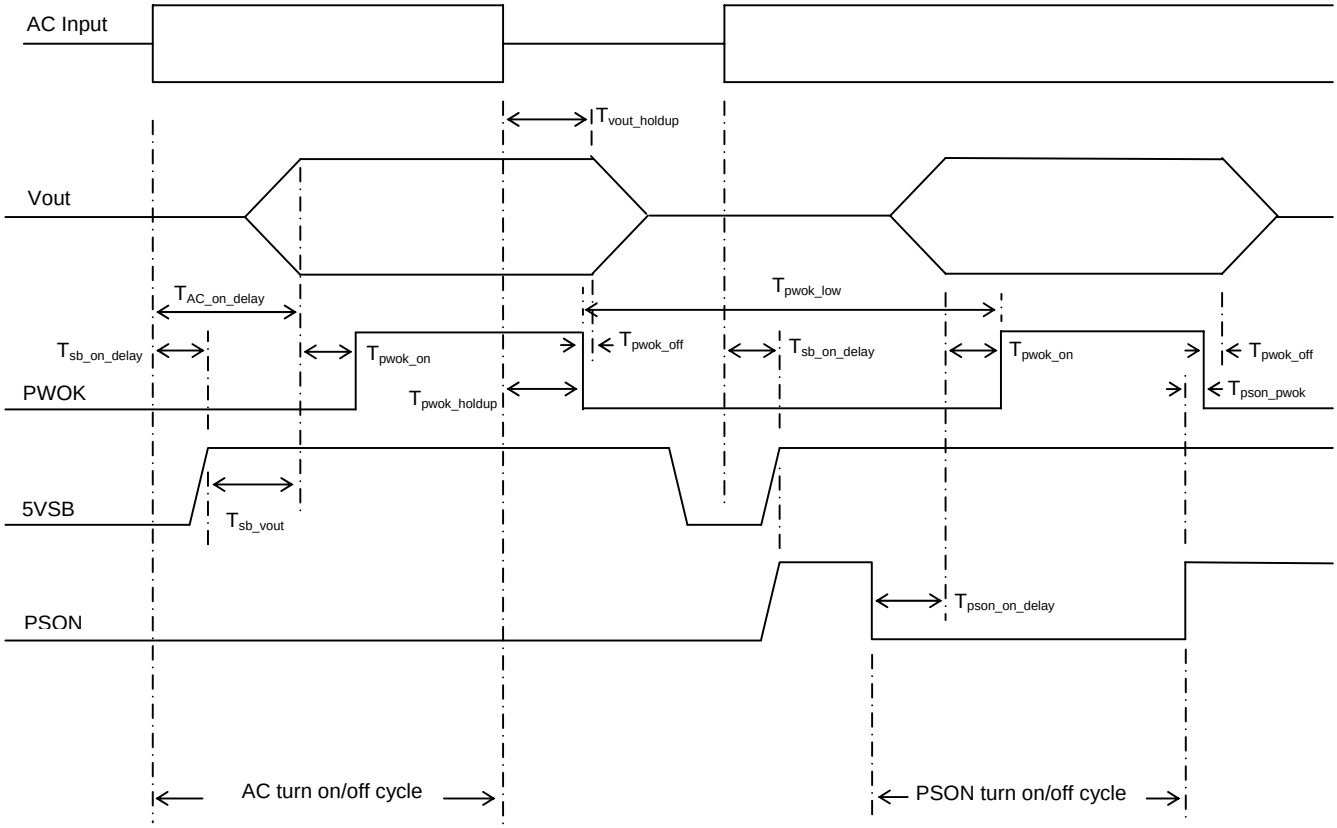

Figure 16. Turn on / off Timing

12.4.2 Voltage Recovery Timing Specifications

The power supply must conform to the following specifications for voltage recovery timing under load changes:

- Voltage shall remain within +/- 5% of the nominal set voltage on the +5 V, +12 V, 3.3 V, -5 V and -12 V output, during instantaneous changes in load shown in the following table.
- Voltage regulation limits shall be maintained over the entire AC input range and any steady state temperature and operating conditions specified.

- Voltages shall be stable as determined by bode plot and transient response. The combined error of peak overshoot, set point, regulation, and undershoot voltage shall be less than or equal to +/-5% of the output voltage setting. The transient response measurements shall be made with a load changing repetition rate of 50 Hz to 5 kHz. The load slew rate shall not be greater than 0.2 A/μs.

Table 100. Transient Load Requirements

Output	Step Load Size	Starting Level	Finishing Level	Slew Rate
+3.3 V	4.8 A	30Min. Load	Min. load + 4.8 A and step up to max. load	0.50 A/μs
+5 V	3.0 A	30Min. Load	Min. load + 3.0 A and step up to max. load	0.50 A/μs
+12 V	10.4 A	Min. Load	Min. load + 10.4 A and step up to max. load	0.50 A/μs
+5 VSB	500 mA	Min. Load	Min. load + 500 mA and step up to max. load	0.50 A/μs
-12 V	325 mA	Min. Load	Min load +325 mA and step up to max. load	0.50 A/μs

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13. Product Regulatory Compliance

13.1.1 Product Safety Compliance

The SE7501BR2 complies with the following safety requirements:

- UL 1950 - CSA 950 (US/Canada)
- EN 60 950 (European Union)
- IEC60 950 (International)
- CE – Low Voltage Directive (73/23/EEC) (European Union)
- EMKO-TSE (74-SEC) 207/94 (Nordics)
- GOST R 50377-92 (Russia)

13.1.2 Product EMC Compliance

The SE7501BR2 has been has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations when installed in a compatible Intel host system. For information on compatible host system(s), contact your local Intel representative.

- FCC (Class A Verification) – Radiated & Conducted Emissions (USA)
- ICES-003 (Class A) – Radiated & Conducted Emissions (Canada)
- CISPR 22, 3rd Edition (Class A) – Radiated & Conducted Emissions (International)
- EN55022 (Class A) – Radiated & Conducted Emissions (European Union)
- EN55024 (Immunity) (European Union)
- CE – EMC Directive (89/336/EEC) (European Union)
- AS/NZS 3548 (Class A) – Radiated & Conducted Emissions (Australia / New Zealand)
- RRL (Class A) Radiated & Conducted Emissions (Korea)
- BSMI (Class A) Radiated & Conducted Emissions (Taiwan)
- GOST R 29216-91 (Class A) Radiated & Conducted Emissions (Russia)
- GOST R 50628-95 (Immunity) (Russia)

13.1.3 Product Regulatory Compliance Markings

This product is provided with the following product certification markings:

- cURus Recognition Mark
- CE Mark
- Russian GOST Mark
- Australian C-Tick Mark
- Korean RRL MIC Mark
- Taiwan BSMI DOC Mark and BSMI EMC Warning

13.2 Electromagnetic Compatibility Notices

13.2.1 FCC (USA)

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.
Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class A or B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.
All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals, that are not shielded and grounded may result in interference to radio and TV reception.

13.2.2 Industry Canada (ICES-003)

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled: "Digital Apparatus," ICES-003 of the Canadian Department of Communications.
Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Apparelis Numériques", NMB-003 édictee par le Ministre Canadian des Communications.

13.2.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE mark to illustrate its compliance.

13.2.4 Australian Communications Authority (ACA) (C-Tick Declaration of Conformity)

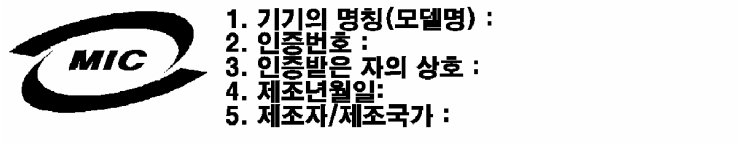
This product has been tested to AS/NZS 3548, and complies with ACA emission requirements. The product has been marked with the C-Tick mark to illustrate its compliance.

13.2.5 Ministry of Economic Development (New Zealand) Declaration of Conformity

This product has been tested to AS/NZS 3548, and complies with New Zealand's Ministry of Economic Development emission requirements.

13.2.6 Korean RRL Compliance

This product has been tested and complies with MIC Notices No. 1997-41 and 1997-42. The product has been marked with the MIC logo to illustrate compliance.



13.2.7 BSMI (Taiwan)

The BSMI DOC Mark is silk screened on the component side of the server board; and the following BSMI EMC warning is marked on the server board.

13.3 Replacing the Back-Up Battery

The lithium battery on the server board powers the RTC for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

⚠ WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

⚠ ADVARSEL**!**

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.


ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.


VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.


VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

14. Mechanical Specifications

14.1 Estimated Mean Time Between Failure (MTBF)

The estimated Mean-Time Between Failures (MTBF) is calculated at 94,385 hours at a maximum operating temperature of 35 C.

14.2 Mechanical Specifications

The following figure shows the server board mechanical drawing.

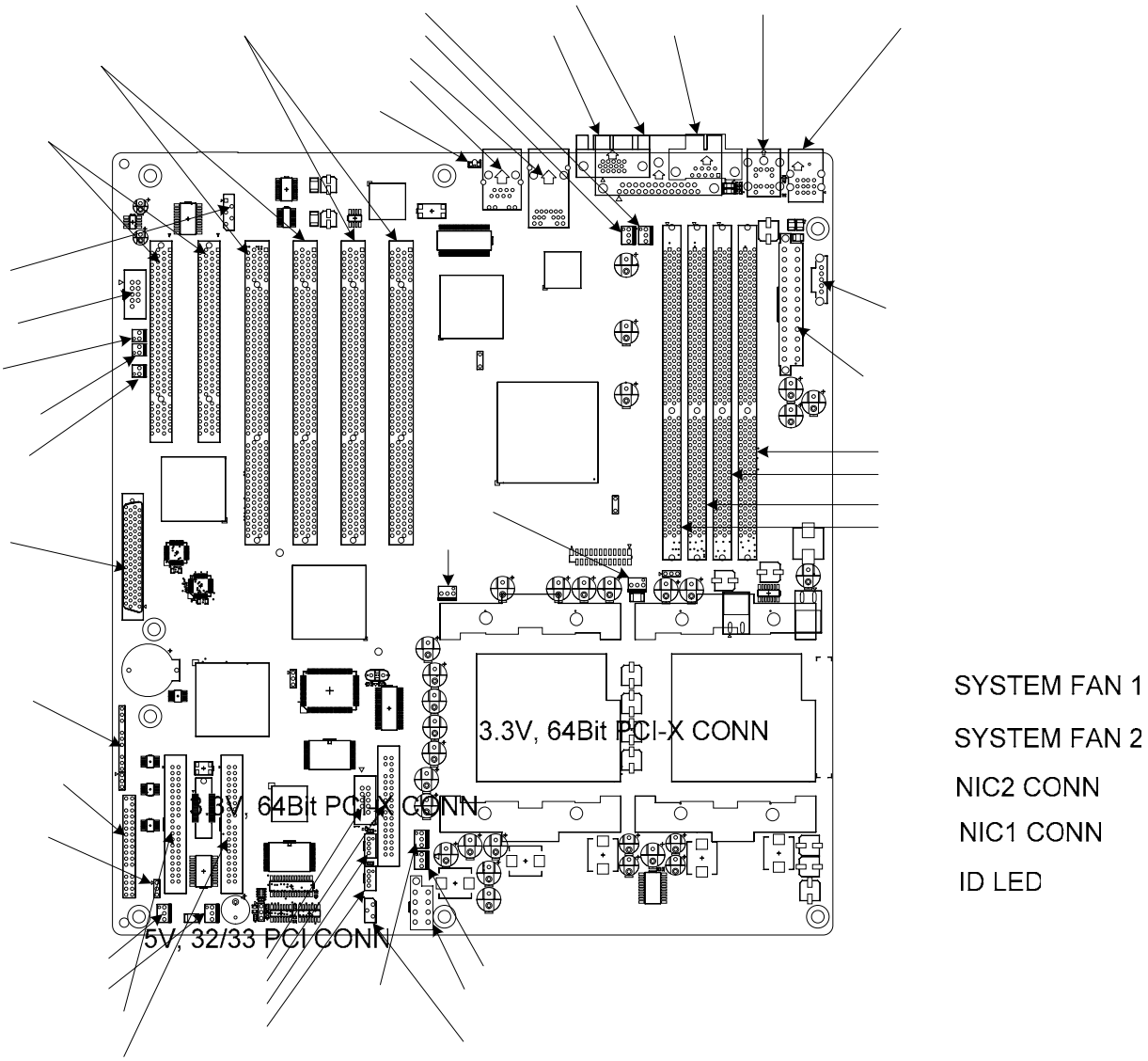


Figure 17. SE7501BR2 Server Board Mechanical Drawing

Table 101. Server Board Connector Specifications

Item	Qty.	Manufacturer and Part Number	Description
1	1	AMP* 6-316173-7	68P SCSI Connector
2	2	FOXCONN* PZ60403-013-T	604P PGA604 Socket
3	1	TACT* 100-009-501-J11-T	9P Header type USB Connector
4	2	Foxconn HF55040-P1	4P External IPMB Connector
5	3	Foxconn HF06021-P1	2P Chass intrusion, HDD LED Connector and EMP INUSE
6	8	Foxconn HF08030-P1	3P Fan Connector
7	1	Foxconn MH11061-PD2	6P single PS/2 Connector (keyboard / mouse)
8	1	JAEE* JE920-2003	2P Battery Holder
9	4	Molex* 89177-9260	184P 64-bit PCI Riser Connector
10	1	Molex 22-44-7031	3P IPMB Connector
11	1	Molex 44472-2470	24P Power Connector
12	1	Molex 22-43-6050	5P ICMB Connector
13	1	Molex 70545-0039	5P AUX Power Connector
14	1	Molex 39-29-9082	8P 12V PWR Connector
15	4	Win Win* W2DRD-184-A2A-3L2B	184P DIMM Connector
16	1	TACT 147-015-601-C1A-T	15P Video Connector
17	1	WORWIN* W31-007-4020	40P IDE Connector BLUE
18	1	WORWIN*BH-40SW-20	40P IDE Connector WHITE
19	2	Wooyoung* HDC-120-1.27D	120P 32bit PCI Connector
20	5	Wooyoung SPS01-S03A-5A1	3P Jumper (BMC,MFG,SHMOO)
21	2	Wooyoung 44472-2470	11P Jumper Header
22	1	Wooyoung BHS-33A-2.54D	33P FDD Connector
23	1	Wooyoung BHS-9A(R)-2.54D	10P Serial Port Connector
24	1	Wooyoung SPS01-D34A-R3	34P FP Connector
25	1	Wooyoung BHS-10A-2.54D-R1	9P USB Connector
26	1	AMP*	12P NIC 10/100 Connector
27	1	INNET* SI-50097 (REV.X3)	16P NIC GIGA Connector
28	1	Foxconn UB11123-M1	12P USB 3 STACK
29	1	TACT 106-025-601-51A-T	25P PARALLEL PORT
30	2	AAVID* A13494	2P Anchor
31	1	FCI* 61698-302	25P ITP Connector
32	1	AMP 767054-1	38P SMM Connector
33	1	Wooyoung SPS01-S06A-5A2	6P FW DEBUG JUMPER

Appendix A: Integration and Usage Tips

This section provides a bullet list of useful information that is unique to the SE7501BR2 server board and should be kept in mind while assembling and configuring your SE7501BR2 based server.

- Only Intel Xeon processors with 512K cache are supported on SE7501BR2
- Processors must be populated in the sequential order; that is, socket CPU#1must be populated before socket CPU #2
- You do not need to populate a terminator in an unused processor socket
- The SE7501BR2 supports DDR266 SDRAM memory only. Memory installation occurs in pairs of contiguous sockets (sockets 1A & 1B and sockets 2A & 2B). Within each pair, the DIMMs need to be the same size and vendor. DIMM pair 1 is located closest to the edge of board.
- The board provides two RJ45 connectors for the on-board Network Interface Controllers. If looking at the rear I/O panel of the board, the Gigabit RJ45 port is on the left (NIC2), the 10/100 RJ45 port is the connector on the right (NIC1).
- When integrating the SE7501BR2 server board in the SC5200 server chassis, users will be required to install two additional standoffs and one bumper in the chassis base plate. Refer to the Quick Start User's Guide for further details.
- The SE7501BR2 server board enables six (6) System Fan Headers: Sys Fan 1 through Sys Fan 6. Sys Fan1 through Sys Fan 4 are used when integrating the server board in the SC5200 Base Chassis. Sys Fan 5 is used for the additional System Fan when integrating the server board in the SC5200 650W Hot-Swap Redundant Power (HSRP). Sys Fan 6 is available for reference chassis.

Appendix B: SE7501BR2 Platform Sensors

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets
Power Unit Status	01h	Power Unit 09h	Sensor Specific 6Fh	Power Off Power Cycle A/C Lost Soft Power Control Fault Power Unit Failure	As	–
Power Unit Redundancy	02h	Power Unit 09h	Generic 0Bh	Redundancy lost	As	–
Watchdog	03h	Watchdog2 23h	Sensor Specific 6Fh	Timer Expired Hard Reset Power Down Power Cycle Timer Interrupt	As & De	–
Platform Security Violation	04h	Platform Security Violation Attempt 06h	Sensor Specific 6Fh	Secure mode violation attempt Out-of-band access password violation	As	–
Physical Security Violation	05h	Physical Security 05h	Sensor Specific 6Fh	General Chassis Intrusion LAN Leash Lost	As & De	General Chassis Intrusion LAN Leash Lost
POST Error	06h	POST error 0Fh	Sensor Specific 6Fh	POST error	As	–
Critical Inerrupt Sensor	07h	Critical Interrupt 13h	Sensor Specific 6Fh	Front Panel NMI Bus Error	As & De	–
Memory	08h	Memory 0Ch	Sensor Specific 6Fh	Uncorrectable ECC	As	–
Event Logging Disabled	09h	Event Logging Disabled 10h	Sensor Specific 6Fh	Correctable Memory Error Logging Disabled Log Area Reset/Cleared	As	–
Session Audit	0Ah	Session Audit 2Ah	Sensor Specific 6Fh	00: Session Activation 01: Session Deactivation	As	–
BB +1.2V	10h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB +1.25V_A	11h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets
BB +1.8V	13h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB +1.8V Standby	14h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB +2.5V	15h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB +3.3V	16h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB +3.3V Auxillary	17h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB +5V	18h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB +5V Standby	19h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB +12V	1Ah	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB +12V VRM	1Bh	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB -12V	1Ch	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB VBAT	1Dh	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
BB Temp	30h	Temp 01h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Front Panel Temp	31h	Temp 01h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Fan Boost BB Temp	32h	OEM C7h	Threshold 01h	[u][nc]	As & De	Analog
Fan Boost Front Panel Temp	33h	OEM C7h	Threshold 01h	[u][nc]	As & De	Analog
Tach Fan 1	40h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Tach Fan 2	41h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Tach Fan 3	42h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Tach Fan 4	43h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Tach Fan 5	44h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Tach Fan 6	45h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Digital Fan 1	50h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets
Digital Fan 2	51h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–
Digital Fan 3	52h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–
Digital Fan 4	53h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–
Digital Fan 5	54h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–
Digital Fan 6	55h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–
LVDS SCSI channel terminator power	60h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Power Supply Status 1 (SC5200)	70h	Power Supply 08h	Sensor Specific 6Fh	Presence Failure Predictive Fail A/C Lost	As & De	–
Power Supply Status 2 (SC5200)	71h	Power Supply 08h	Sensor Specific 6Fh	Presence Failure Predictive Fail A/C Lost	As & De	–
Power Supply Status 3 (SC5200)	72h	Power Supply 08h	Sensor Specific 6Fh	Presence Failure Predictive Fail A/C Lost	As & De	–
Power Cage Fan 1	73h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Power Cage Fan 2	74h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Power Cage Temp	76h	Temp 01h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Processor Missing	80h	Module / Board 15h	Digital Discrete 03h	State Asserted State Deasserted	As	–
System ACPI Power State	82h	System ACPI Power State 22h	Sensor Specific 6Fh	S0 / G0 S1 S4 S5 / G2 • G3 Mechanical Off	As	–

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets
System Event	83h	System Event 12h	Sensor Specific 6Fh	OEM System Boot Event (Hard Reset) • PEF Action	As	–
Button	84h	Button 14h	Sensor Specific 6Fh	Power Button Sleep Button Reset Button	As	–
SMI Timeout	85h	SMI Timeout F3h	Digital Discrete 03h	State Asserted State Deasserted	As	–
Sensor Failure	86h	Sensor Failure F6h	OEM Sensor Specific 73h	I^2C device not found I^2C device error detected I^2C Bus Timeout	As	–
NMI Signal State	87h	OEM C0h	Digital Discrete 03h	State Asserted State Deasserted	–	–
SMI Signal State	88h	OEM C0h	Digital Discrete 03h	State Asserted State Deasserted	–	–
Front Side Bus Speed Mismatch	89h	BSEL Mismatch F7h	Digital Discrete 03h	State Asserted	As	–
Proc 1 Status	90h	Processor 07h	Sensor Specific 6Fh	Presence Thermal Trip IERR, FRB1. FRB2. FRB3 Disabled Terminator Presence	As & De	–
Proc 2 Status	91h	Processor 07h	Sensor Specific 6Fh	Presence Thermal Trip IERR. FRB1, FRB2, FRB3, Disabled • Terminator Presence	As & De	–
Proc 1 Core Temp	98h	Temp 01h	Threshold 01h	• [u,l][c,nc]	As & De	Analog
Proc 2 Core Temp	99h	Temp 01h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Fan Boost Proc 1 Core Temp	A0h	OEM C7h	Threshold 01h	[u,l][nc]	As & De	Analog
Fan Boost Proc 2 Core Temp	A1h	OEM C7h	Threshold 01h	[u,l][nc]	As & De	Analog

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets
Processor 1 Fan	A8h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Processor 2 Fan	A9h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Proc Vccp	B8h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog
Processor HOT	C0h	Temp 01h	Digital Discrete 03h	State Asserted State Deasserted	As & De	–
DIMM 1	E0h	Slot Connector 21h	Sensor Specific 6Fh	Fault Status Asserted Device Installed Disabled	As	–
DIMM 2	E1h	Slot Connector 21h	Sensor Specific 6Fh	Fault Status Asserted Device Installed Disabled	As	–
DIMM 3	E2h	Slot Connector 21h	Sensor Specific 6Fh	Fault Status Asserted Device Installed Disabled	As	–
DIMM 4	E3h	Slot Connector 21h	Sensor Specific 6Fh	Fault Status Asserted Device Installed Disabled	As	–

Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
AP	Application Processor
ASIC	Application Specific Integrated Circuit
ASR	Asynchronous Reset
BGA	Ball-grid Array
BIOS	Basic input/output system
BIST	Built-in self test
BMC	Server board Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other.
BSP	Bootstrap processor
Byte	8-bit quantity.
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DDR	Synchronous Dynamic RAM
DMA	Direct Memory Access
DMTF	Distributed Management Task Force
ECC	Error Correcting Code
EMC	Electromagnetic Compatibility
EMP	Emergency management port.
EPS	External Product Specification
ESCD	Extended System Configuration Data
FDC	Floppy Disk Controller
FIFO	First-In, First-Out
FRB	Fault resilient booting
FRU	Field replaceable unit
GB	1024 MB.
GPIO	General purpose I/O
GUID	Globally Unique ID
HDG	Hardware Design Guide
Hz	Hertz (1 cycle/second)
I^2C	Inter-integrated circuit bus
IA	Intel® architecture
ICMB	Intelligent Chassis Management Bus
IERR	Internal error
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IRQ	Interrupt Request
ISC	Intel® Server Control
ITP	In-target probe
KB	1024 bytes

Term	Definition
KCS	Keyboard Controller Style
LAN	Local area network
LBA	Logical Block Address
LCD	Liquid crystal display
LPC	Low pin count
LSB	Least Significant Bit
LVD	Low-Voltage Differential
MB	1024 KB
MBE	Multi-Bit Error
ms	milliseconds
MSB	Most Significant Bit
MTBF	Mean Time Between Failures
Mux	multiplexor
NIC	Network Interface Card
NMI	Non-maskable Interrupt
OEM	Original equipment manufacturer
Ohm	Unit of electrical resistance
P32-A	32-bit PCI Segment A
P64-B	64-bit PCI Segment B
P64-C	64-bit PCI Segment C
PBGA	Pin Ball Grid Array
PDB	Power Distribution Board
PEF	Platform Event Filtering
PERR	Parity Error
PET	Platform Even Trap
PIO	Programmable I/O
PMB	Private Management Bus
PMC	Platform Management Controller
PME	Power Management Event
PnP	Plug and Play
POST	Power-on Self Test
PWM	Pulse-Width Modulator
RAM	Random Access Memory
RI	Ring Indicate
RISC	Reduced instruction set computing
RMCP	Remote Management Control Protocol
ROM	Read Only Memory
RTC	Real Time Clock
SAF-TE	SCSI Accessed Fault-Tolerant Enclosure Specification
SBE	Single-Bit Error
SCI	System Configuration Interrupt
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic RAM
SEL	System Event Log

Term	Definition
SERIRQ	Serialized Interrupt Requests
SERR	System Error
SM	Server Management
SMI	Server management interrupt. SMI is the highest priority nonmaskable interrupt
SMM	System Management Mode
SMS	System Management Software
SNMP	Simple Network Management Protocol
SPD	Serial Presence Detect
SSI	Server Standards Infrastructure
SSU	Server Setup Utility
TBD	To Be Determined
TPS	Technical Product Specification
UART	Universal asynchronous receiver and transmitter
USB	Universal Serial Bus
VGA	Video Graphic Adapter
VID	Voltage Identification
VRM	Voltage Regulator Module
Word	16-bit quantity
ZCR	Zero Channel RAID

Reference Documents

Refer to the following documents for additional information:

- *PCI Local Bus Specification* Revision 2.2
- *PCI-X Specification 1.0a*
- *ATI Rage XL Graphics Controller Specifications, Technical Reference Manual*, Rev 2.01
- RAID I/O Steering (RAIDIOS) specification version 1.0
- VRM 9.1 DC-DC Converter Design Guide Line
- Intel® Xeon™ Processor Voltage Regulator Down Design Guide Lines
- I2C Bus Specification
- IPMB Communications Protocol Specification
- SE7501BR2 Product Guide
- SE7501BR2 Quick Start User's Guide

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