Enterprise Server Group

Intel S450NX MP Server Board Set
Technical Product Specification

intel.

Revision History

Revision	Revision History	Date
Rev 1.0	Initial Release	7/98

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1. Board Set Descriptions

1.1   Baseboard Overview

The Intel S450NX MP Server is a flat baseboard design featuring a quad Pentium® II Xeon™ processor-based server system that combines the latest technology and integrated features to provide a high-performance platform at mid-range cost efficiency.

The S450NX MP Server baseboard utilizes the Intel 82450NX PCIset, the latest in chipset technology from Intel, to maximize system performance for 32-bit application software and operating systems.

The S450NX MP Server design is complemented with an array of features. These include:

- Edge connector interface to memory card supports up to 4GB of memory using commodity EDO DIMM devices.
- The Intel 82450NX PCIset as PCI host bridge and memory controller (Memory and I/O Controller (MIOC), PCI Expansion Bridge (PXB)).
- Dual 32-bit, 33MHz PCI segments compliant with revision 2.1 of the PCI specification. PCI-A and PCI-B are provided by the PXB in the Intel 82450NX PCIset, with a total of 7 expansion slots; 3 on PCI-A, 4 on PCI-B (one shared with ISA).
- 1 ISA slot and PC Compatible I/O (serial, parallel, mouse, and keyboard).
- PIIX4(e) PCI-to-ISA bridge, IDE controller, USB controller, and power management.
- Other embedded PCI I/O devices, including SCSI, and IDE controllers.
- Server management features, including thermal/voltage monitoring, chassis intrusion detection, and fan failure detection.
- High-performance 2D PCI video controller (Cirrus Logic GD5480) with 2MB of SGRAM onboard.
- Four "Slot 2" Single Edge Contact (SEC) cartridge connectors (to accommodate 1 to 4 Pentium II® Xeon™ processors and future processor upgrades).

The S450NX MP Server baseboard supports one to four Pentium II Xeon processors (conforming to the Slot 2 specification) contained on Single Edge Contact (SEC) cartridges. The SEC cartridges enclose the processor with integrated ECC L2 cache to enable high-frequency operation. The baseboard provides four "Slot 2" connectors, and connectors for six, VRM 8.3-compliant, plug-in voltage regulator modules. The S450NX MP Server baseboard design will accommodate identified upgrades to future Intel processing technology.
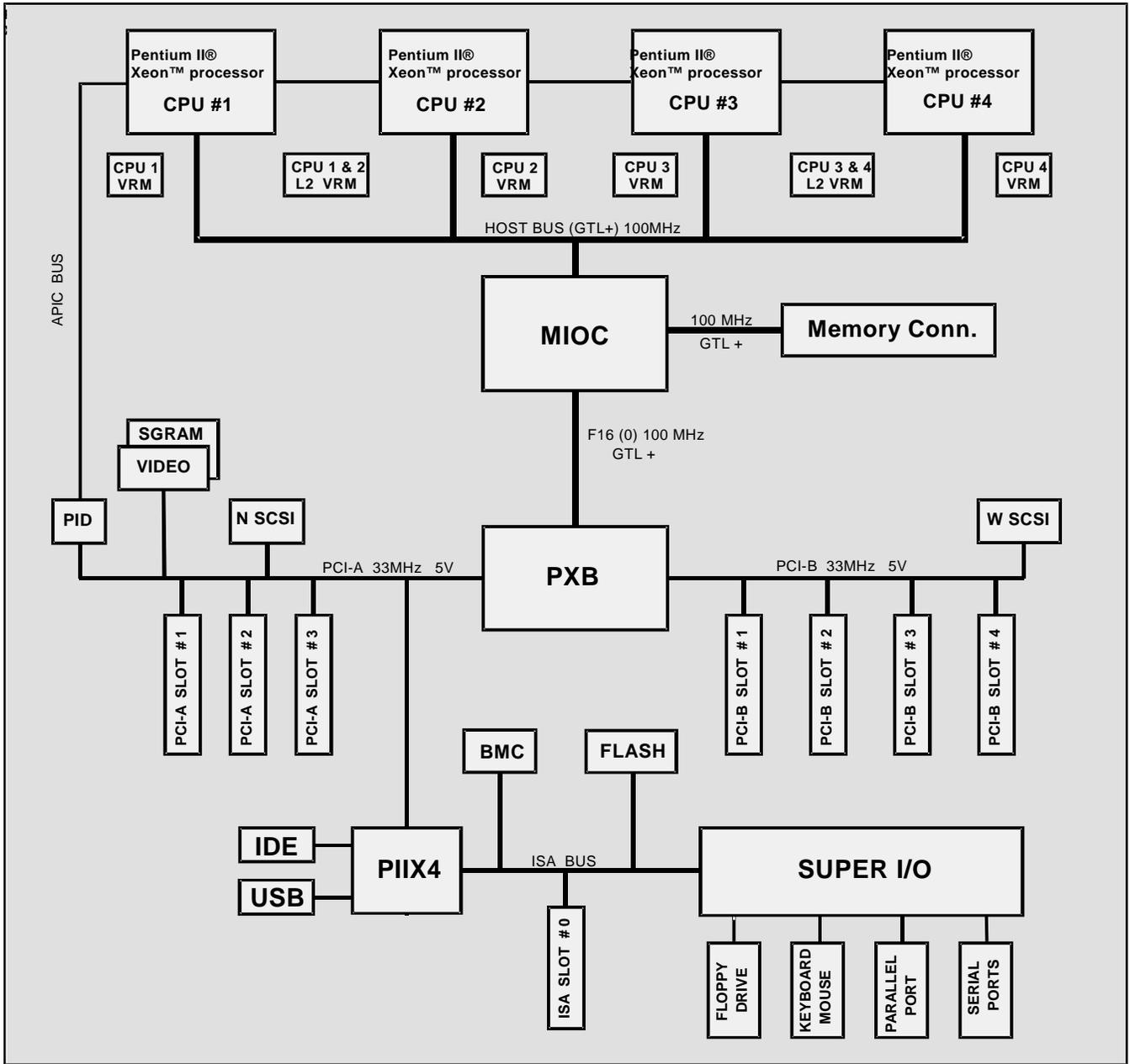
Figure 1.1: S450NX MP Server Functional Block Architecture

The diagram shows the following blocks and connections:

- **Pentium II® Xeon™ processor CPU #1**
- **Pentium II® Xeon™ processor CPU #2**
- **Pentium II® Xeon™ processor CPU #3**
- **Pentium II® Xeon™ processor CPU #4**

- CPU 1 VRM
- CPU 1 & 2 L2 VRM
- CPU 2 VRM
- CPU 3 VRM
- CPU 3 & 4 L2 VRM
- CPU 4 VRM

HOST BUS (GTL+) 100MHz

APIC BUS

MIOC — 100 MHz GTL + — **Memory Conn.**

F16 (0) 100 MHz GTL +

SGRAM
VIDEO
PID
N SCSI
W SCSI

PCI-A 33MHz 5V — **PXB** — PCI-B 33MHz 5V

- PCI-A SLOT # 1
- PCI-A SLOT # 2
- PCI-A SLOT # 3
- PCI-B SLOT # 1
- PCI-B SLOT # 2
- PCI-B SLOT # 3
- PCI-B SLOT # 4

BMC
FLASH

IDE
USB
PIIX4

ISA BUS

ISA SLOT # 0

SUPER I/O

- FLOPPY DRIVE
- KEYBOARD MOUSE
- PARALLEL PORT
- SERIAL PORTS

1.1.1 Baseboard Diagram

The following diagram shows the placement of major components and connector interfaces on the S450NX MP Server baseboard.
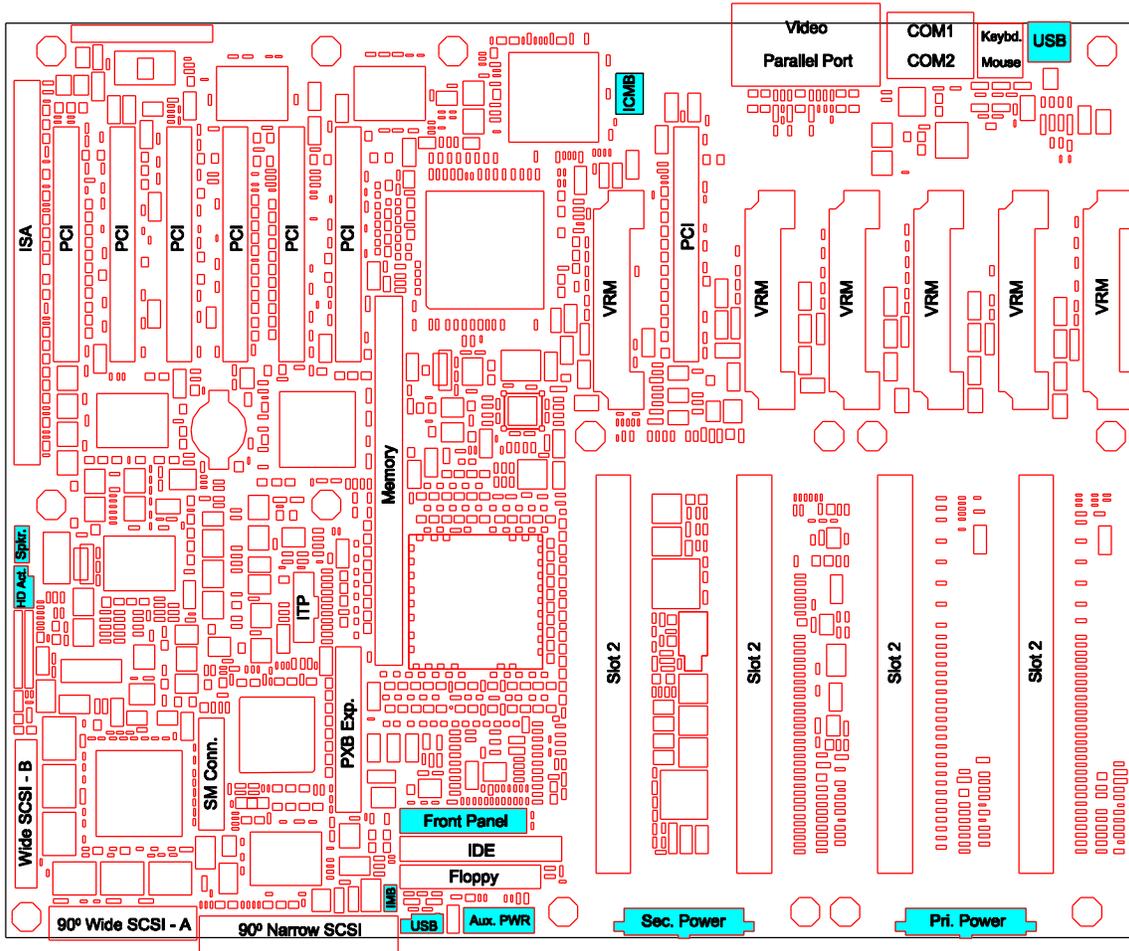
Figure 1.2: S450NX MP Baseboard Layout

1.2   Processor/PCI Host Bridge

The processor/PCI bridge/memory sub-system consists of one to four identical Pentium II® Xeon™ processors, a plug-in memory board, and support circuitry on the baseboard consisting of the following:

- Intel 82450NX PCIset which provides an integrated I/O bridge and memory controller and a flexible I/O sub-system core (PCI) optimized for multiprocessor systems and standard high-volume (SHV) servers

- Quad "Slot 2" edge connectors that accept Pentium II Xeon processors

- 242-pin connector interface to memory board

- Processor host bus AGTL+ support circuitry, including termination power supply

- Six sockets for plug-in VRMs to power SEC processor cartridges

- APIC bus

- Miscellaneous logic for reset configuration, processor presence detection, and server management
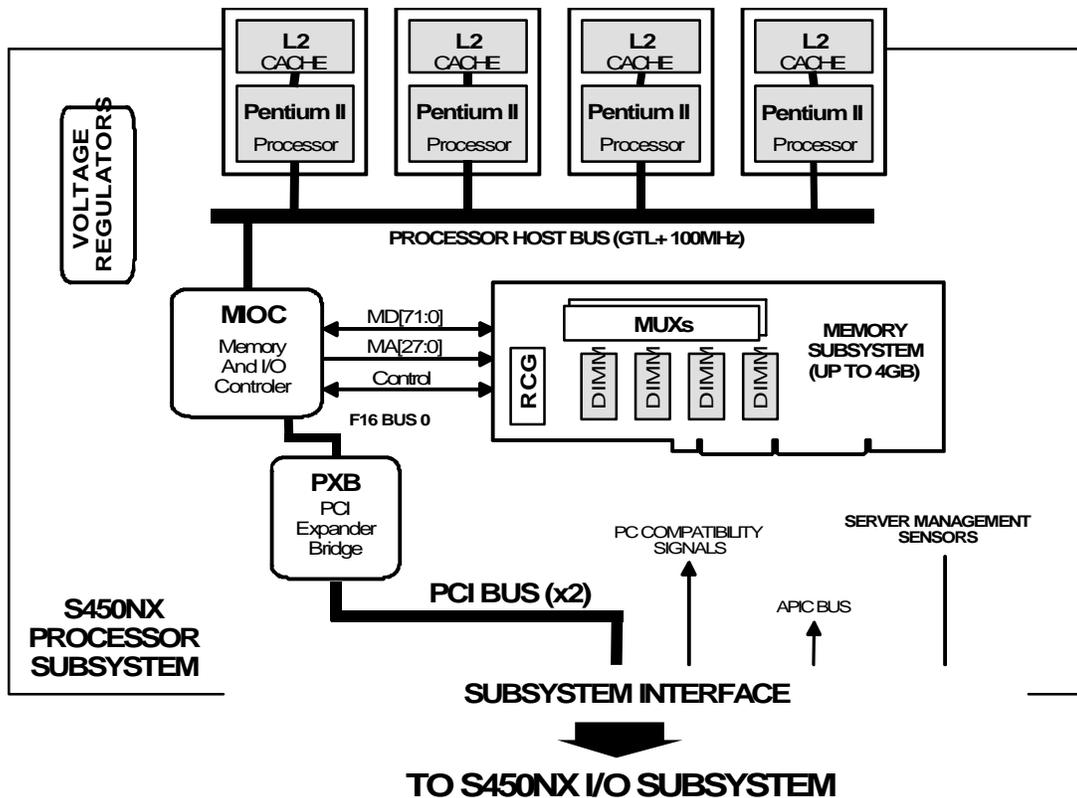
Figure 1.3: Processor/PCI Host Bridge/Memory Sub-system

1.3　Pentium II® Xeon™ Processor Cartridge

The S450NX MP Server Baseboard is designed to accommodate the Pentium II Xeon cartridge. The L1 cache, and L2 cache components are on a pre-assembled printed circuit board, approximately 4.8" x 6" in size. The L2 cache and processor core/L1 cache connect using a private bus isolated from the processor host bus. This L2 cache bus operates at the processor core frequency.

The Pentium II Xeon processor cartridge external interface is designed to be MP-ready. Each processor contains a local APIC section for interrupt handling. When four processor cartridges are installed, all processor cartridges must be of identical revision, core voltage, and bus/core speeds.

1.3.1　Retention Module
The Pentium II® Xeon™ processor retention module is used to add stability to the processor cartridge connector and a way of providing attachment to the baseboard. The processor retention module is attached with screws.

1.3.2　Processor Cartridge Connector
The Pentium II Xeon processor cartridge edge connector conforms to the "Slot 2" specification, which can also accommodate future processor cartridges. The baseboard provides 4 Slot 2 processor cartridge connectors. Processors and Slot 2 connectors are keyed to ensure proper orientation.

1.3.3　Processor Heat/Fan Sinks
The S450NX MP Server baseboard is not dependent on having fansinks, nor are fansinks supported by the S450NX MP Server baseboard.

1.3.4　Processor Bus Termination/Regulation/Power
The termination circuitry required by the Pentium II processor bus (GTL+) signaling environment, and the circuitry to set the GTL+ reference voltage are implemented directly on the processor cartridges. The baseboard provides 1.5V GTL+ termination power (VTT), and VRM 8.3-compliant DC-to-DC converters to provide processor power (VCCP and L2) at each connector. Six sockets are provided on the baseboard for VRMs to power the processors, which derive power from the 12V supply. Refer to the *VRM 8.3 DC-DC Converter Specification* for more information.

1.3.5　Termination Card
Logic is provided on the baseboard to detect the presence and identity of installed processor or termination cards. If any SEC processor cartridge is not installed in the system, a termination card *must* be installed in the vacant SEC processor cartridge slot to ensure reliable system operation. The termination card contains AGTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector. The system will not boot unless all slots are occupied with a processor or termination card.

1.3.6　APIC Bus

Interrupt notification and generation for the processors is done using an independent path between local APICs in each processor and the Intel I/O APIC in PID located on the baseboard. This bus consists of 2 data signals and one clock line. Refer to "Interrupts and the PID" later in this chapter for more information.

1.4   82450NX PCIset

The Intel 82450NX PCIset provides an integrated I/O bridge and memory controller and a flexible I/O sub-system core (PCI), targeted for multi-processor systems and standard high-volume (SHV) servers based on the Pentium II® Xeon™ processor. The Intel 82450NX PCIset consists of five components, as listed below:

MIOC - Memory and I/O Controller. The MIOC is responsible for accepting access requests from the host (processor) bus, and directing those accesses to memory or one of the PCI buses. The MIOC monitors the host bus, examining addresses for each request. Accesses may be directed to a memory request queue, for subsequent forwarding to the memory sub-system, or to an outbound request queue, for subsequent forwarding to the PXB and hence to the PCI buses. The MIOC also accepts inbound requests from the PXB representing requests from the PCI buses. The MIOC is also responsible for generating the appropriate controls to the RCG and MUX to control data transfer to and from the memory.

PXB - PCI Expander Bridge. The PXB provides the interface to two independent 32-bit 33MHz Rev 2.1-compliant PCI buses. The PXB is both master and target on each PCI bus. The two buses are processed completely independent except where transactions must be forwarded across the Expander (F16) Bus between PXB and MIOC.

RCG - RAS/CAS Generator. The RCG is responsible for accepting memory requests from the MIOC and converting these into the specific signals and timings required by the DRAM.

MUX - Data Path Multiplexers. The two MUX components provide the multiplexing and staging required to support memory interleaving between the DRAMs and the MIOC.

1.4.1 82450NX System I/O Access

The MIOC and PXB components provide the pathway between processor and I/O systems. The MIOC is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to the PXB through the F16 Bus. The PXB then translates the F16 Bus operation to a 32-bit PCI Rev. 2.1 compliant, 5V signaling environment at 33MHz. The PXB also handles arbitration for the PCI bus segments.

The PCI interface provides greater than 100 MB/s data streaming for PCI to DRAM accesses, while supporting concurrent processor host bus and PCI transactions to main memory. This is accomplished using extensive data buffering, with processor-to-DRAM and PCI-to-DRAM write data buffering and write-combining support for processor-to-PCI burst writes.

1.4.2 82450NX Main Memory Access

The MIOC also provides the memory controller for the system, issuing commands to the RCGs and MUXs, and accepting the data returned from the DRAMs. Memory amounts from 128MB to 4GB of DIMMs are supported, with a 64/72-bit four-way-interleaved pathway to main memory which is located on a plug-in module. The memory controller supports EDO DRAMs. The ECC used for the memory module is capable of correcting single-bit errors and detecting 100% of double-bit errors over one code word. Nibble error detection is also provided.

1.5   PCI-A I/O Sub-system

All I/O for S450NX, including PCI and PC-compatible, is directed through the PXB. The two PCI buses on S450NX run concurrently, with PCI-A and B at the same level. PCI-A supports the following embedded devices and connectors:

- Three 120-pin, 32-bit PCI expansion slot connectors, numbered PCI-A1, PCI-A2, PCI-A3

- PIIX4(e) PCI-to-ISA bridge, IDE controller, USB controller, and power management

- PCI video controller, Cirrus Logic CL-GD5480

- PCI narrow SCSI controller, Symbios 5353C810AE

- Programmable Interrupt Device (Intel ASIC; contains I/O APIC)

Each device under the PCI host bridge has its IDSEL signal connected to one bit out of AD[31:11], which acts as a chip select on the PCI bus segment. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for PCI-A devices, and corresponding device number. Refer to "Accessing Configuration Space" in Chapter 3 for more information.

Table 1.1: PCI-A Configuration IDs

IDSEL Value	Device
22	PCI Slot PCI-A1
23	PCI Slot PCI-A2
24	PCI Narrow SCSI
25	PCI Slot PCI-A3
26	PCI Video
27	Programmable Interrupt Device
28	PIIX4(e)

1.5.1 PCI-A Arbitration

PCI-A supports seven PCI masters (slots PCI-A1 through PCI-A3, PID, PIIX4(e), Narrow SCSI, and the PXB). All PCI masters must arbitrate for PCI access, using resources supplied by the PXB. The host bridge PCI interface arbitration lines REQx_L and GNTx_L are a special case in that they are internal to the host bridge. PIIX4(e) arbitration signals are also a special case so that access time capability for ISA masters is guaranteed. The following table defines the arbitration connections:

Table 1.2: PCI-A Arbitration Connections

Baseboard Signals	Device
PA_PHOLD_L/P_PHLDA_L	PIIX4(e)
PA_REQ0_L/P_GNT0_L	PCI-A Slot PCI-A1
PA_REQ1_L/P_GNT1_L	PCI-A Slot PCI-A2
PA_REQ2_L/P_GNT2_L	PCI-A Slot PCI-A3
PA_REQ3_L/P_GNT3_L	Video GD5480
PA_REQ4_L/P_GNT4_L	Narrow SCSI
PA_REQ5_L/P_GNT5_L	PID

1.5.2 PCI-to-ISA/IDE/USB Controller PIIX4(e)

The PIIX4(e), is a multi-function PCI device, providing 4 PCI functions in a single package: PCI-to-ISA bridge, PCI IDE interface, PCI USB controller, and power management controller. Each function within the PIIX4(e) has its own set of configuration registers and once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

The PIIX4(e) fully implements a 32-bit PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Rev. 2.1*. The PCI interface operates at 33 MHz, using the 5V-signaling environment. The PIIX4(e) provides an ISA bus interface, operating at 8.33 MHz that supports a single ISA connector, Flash memory, server management interface, and the SuperI/O controller.

The Fast IDE controller in the PIIX4(e) supports programmed I/O transfers up to 14MB/s and bus master IDE transfers up to 33MB/s.

The PIIX4(e) contains a USB controller and two port USB hub. The USB controller moves data between main memory and up to two devices each connected on either the external or internal USB header. The S450NX MP Server baseboard provides a single external USB connector interface for the back panel, and a special internal header to be used with device bay expansion. The external USB port, logically Port B, is defined by the *USB Specification, Revision 1.0*, with the pin-out shown in table 1.3.

Table 1.3: USB Connector Pin-out

Pin	Name	Comment
1	VCC	CABLE POWER
2	DATA-	Data (differential pair negative)
3	DATA+	Data (differential pair positive)
4	GND	CABLE GROUND

The internal USB header has been defined to work with device bay; it is logically Port A. Power is not supplied by the baseboard for this port. The header pin-out is shown in table 1.4.

Table 1.4: USB Header Pin-out

Pin	Name	Comment
1		nc
2	DATA-	Data (differential pair negative)
3	DATA+	Data (differential pair positive)
4	GND	CABLE GROUND

1.6   PCI-A Narrow SCSI

The PCI-A bus provides an embedded narrow SCSI host adapter: Symbios SYM53C810AE. The SYM53C810AE contains a high-performance SCSI core capable of Fast 8-bit SCSI transfers in single-ended mode. The high-performance SCSI core, PCI bus master DMA, and internal SCRIPTS* processor meets SCSI-1 and SCSI-2 standards. This part provides programmable active negation, PCI zero wait-state bursts of faster than 110MB/s at 33MHz and SCSI transfers rates from 5MB/s to 10MB/s.

1.6.1 SYM53C810AE PCI Signals

The SYM53C810AE supports all of the required 32-bit PCI signals including the PERR_L and SERR_L functions. Full PCI parity is maintained on the entire data path through the component. The device also takes advantage of a PCI interrupt resource to operate. The 53C810AE does not support the CLKRUN_L, LOCK_L, SBO_L, SDONE_L, INTB/C/D_L, TCK, TDI, TDO, TMS, and TRST_L signals. The SYM53C810AE interrupt request signal connects to P_INTC_L on the S450NX MP Server baseboard.

```
SYM53C810            ◄────────►  AD[31::0]

                     ◄────────►  C/BE[3::0]_L
                     ◄────────►  PAR
                     ◄────────►  FRAME_L
                     ◄────────►  TRDY_L
                     ◄────────►  IRDY_L
                     ◄────────►  STOP_L
                     ◄────────►  DEVSEL_L
                     ◄─────────  IDSEL
                     ─────────►  REQ_L
                     ◄─────────  GNT_L
                     ◄─────────  PCI_CLK
                     ◄─────────  RST_L
                     ◄────────►  PERR_L
                     ◄────────►  SERR_L
                     ─────────►  PCIP_INTC_L
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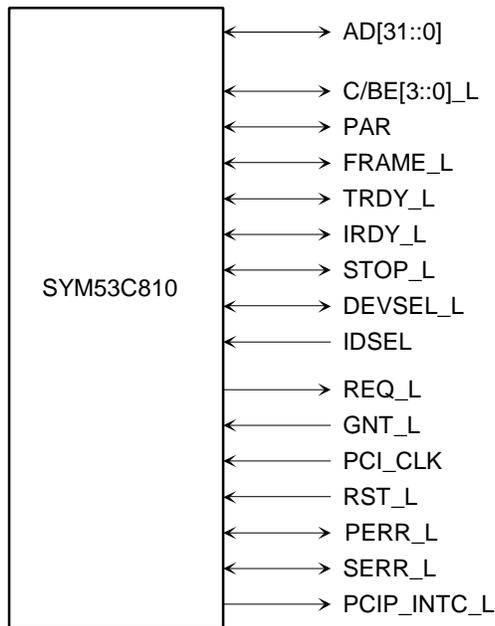
Figure 1.4: Embedded Narrow SCSI PCI Signals

1.7   PCI-A Video

The S450NX MP Server baseboard integrates a Cirrus Logic CL-GD5480 video controller, along with video SGRAM and support circuitry for an embedded SVGA video sub-system. The CL-GD5480 64-bit VGA Graphics Accelerator component contains an SVGA video controller, clock generator, Bit BLT engine, and RAMDAC. Two 256K x 32 SGRAM components provide 2 MB of 10ns video memory. The SVGA sub-system supports a variety of modes: up to 1600 x 1200 resolution, and up to 16.7 M colors. It also supports analog VGA monitors, single- and multi-frequency, interlaced and non-interlaced, up to 100Hz vertical retrace frequency. The S450NX MP Server baseboard also provides a standard 15-pin VGA connector, and external video blanking logic for server management support.

1.7.1 Video Component PCI Signals
The CL-GD5480 is a 32-bit PCI device with PCI master capability. Below is a diagram of the PCI signals used.
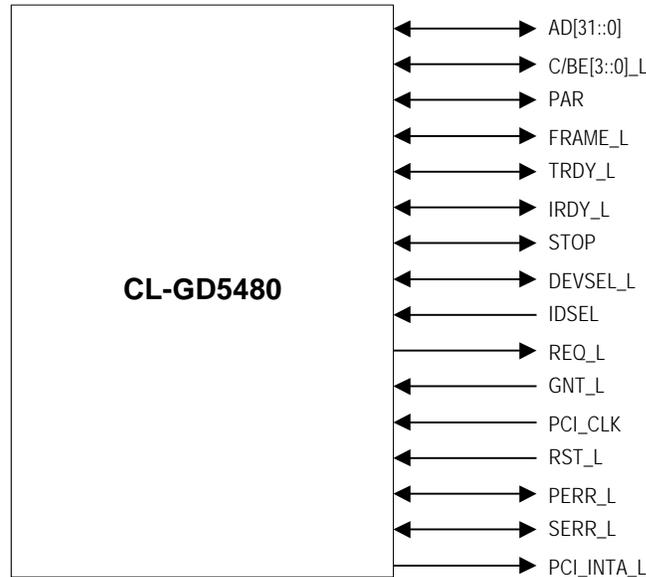
Figure 1.5: Video Controller PCI Signals

1.7.2 Video Controller PCI Commands

The CL-GD5480 supports the following PCI commands:

Table 1.5: Video Component Supported PCI Commands

C/BE[3::0]_L	Command Type	GD5480 Support	
		Target	Master
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	No
0111	Memory Write	Yes	No
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No	No
1101	Dual Address Cycle	No	No
1110	Memory Read Line	No	No
1111	Memory Write and Invalidate	No	No

1.7.3 Video Modes

The CL-GD5480 supports all standard IBM VGA modes. Using 2MB of SGRAM, the S450NX MP Server supports special Cirrus Logic extended modes. The following tables show the standard and extended modes that this implementation supports, including the number of colors and palette size (e.g., 16 colors out of 256 K colors), resolution, pixel frequency, and scan frequencies.

Table 1.6: Standard VGA Modes

Mode(s) in Hex	Colors (number /palette size)	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	16/256K	360 X 400	14	31.5	70
2, 3	16/256K	720 X 400	28	31.5	70
4, 5	4/256K	320 X 200	12.5	31.5	70
6	2/256K	640 X 200	25	31.5	70
7	Mono	720 X 400	28	31.5	70
D	16/256K	320 X 200	12.5	31.5	70
E	16/256K	640 X 200	25	31.5	70
F	Mono	640 X 350	25	31.5	70
10	16/256K	640 X 350	25	31.5	70
11	2/256K	640 X 480	25	31.5	60
12	16/256K	640 X 480	25	31.5	60
12+	16/256K	640 X 480	31.5	37.5	75
13	256/256K	320 X 200	12.5	31.5	70

Table 1.7: Extended VGA Modes

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
58, 6A	16/256K	800 X 600	36	35.2	56
58, 6A	16/256K	800 X 600	40	37.8	60
58, 6A	16/256K	800 X 600	50	48.1	72
58, 6A	16/256K	800 X 600	49.5	46.9	75
5C	256/256K	800 X 600	36	35.2	56
5C	256/256K	800 X 600	40	37.9	60
5C	256/256K	800 X 600	50	48.1	72
5C	256/256K	800 X 600	49.5	46.9	75
5C	256/256K	800 X 600	56.25	53.7	85
5C	256/256K	800 X 600	68.2	63.6	100
5D	16/256K (interlaced)	1024 X 768	44.9	35.5	43
5D	16/256K	1024 X 768	65	48.3	60
5D	16/256K	1024 X 768	75	56	70
5D	16/256K	1024 X 768	78.7	60	75
5E	256/256K	640 X 400	25	31.5	70
5F	256/256K	640 X 480	25	31.5	60
5F	256/256K	640 X 480	31.5	37.9	72
5F	256/256K	640 X 480	31.5	37.5	75
5F	256/256K	640 X 480	36	43.3	85
5F	256/256K	640 X 480	43.2	50.9	100
60	256/256K (interlaced)	1024 X 768	44.9	35.5	43
60	256/256K	1024 X 768	65	48.3	60
60	256/256K	1024 X 768	75	56	70
60	256/256K	1024 X 768	78.7	60	75
60	256/256K	1024 X 768	94.5	68.3	85
60	256/256K	1024 X 768	113.3	81.4	100
64	64K	640 X 480	25	31.5	60
64	64K	640 X 480	31.5	37.9	72
64	64K	640 X 480	31.5	37.5	75

Table 1.7: Extended VGA Modes (cont.)

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
64	64K	640 X 480	36	43.3	85
64	64K	640 X 480	43.2	50.9	100
65	64K	800 X 600	36	35.2	56
65	64K	800 X 600	40	37.8	60
65	64K	800 X 600	50	48.1	72
65	64K	800 X 600	49.5	46.9	75
65	64K	800 X 600	56.25	53.7	85
65	64K	800 X 600	68.2	63.6	100
66	32K	640 X 480	25	31.5	60
66	32K	640 X 480	31.5	37.9	72
66	32K	640 X 480	31.5	37.5	75
66	32K	640 X 480	36	43.3	85
66	32K	640 X 480	43.2	50.9	100
67	32K	800 X 600	36	35.2	56
67	32K	800 X 600	40	37.8	60
67	32K	800 X 600	50	48.1	72
67	32K	800 X 600	49.5	46.9	75
67	32K	800 X 600	56.25	53.7	85
67	32K	800 X 600	68.2	63.6	100
68	32K (interlaced)	1024 X 768	44.9	35.5	43
68	32K	1024 X 768	65	48.3	60
68	32K	1024 X 768	75	56	70
68	32K	1024 X 768	78.7	60	75
68	32K	1024 X 768	94.5	68.3	85
68	32K	1024 X 768	113.3	81.4	100
6C	16/256K (interlaced)	1280 X 1024	75	48	43
6D	256/256K (interlaced)	1280 X 1024	75	48	43
6D	256/256K	1280 X 1024	108	65	60
6D	256/256K	1280 X 1024	135	80	75
6D	256/256K	1280 X 1024	157.5	91	85
6E	32K	1152 X 864	94.5	63.9	70
6E	32K	1152 X 864	108	67.5	75
6E	32K	1152 X 864	121.5	76.7	85
6E	32K	1152 X 864	143.5	91.5	100
71	16M	640 X 480	25	31.5	60
71	16M	640 X 480	31.5	37.9	72
71	16M	640 X 480	31.5	37.5	75
71	16M	640 X 480	36	43.3	85
71	16M	640 X 480	43.2	50.9	100
74	64K (interlaced)	1024 X 768	44.9	35.5	43
74	64K	1024 X 768	65	48.3	60
74	64K	1024 X 768	75	56	70
74	64K	1024 X 768	78.7	60	75
74	64K	1024 X 768	94.5	68.3	85
74	64K	1024 X 768	113.3	81.4	100
78	32K	800 X 600	36	35.2	56

Table 1.7: Extended VGA Modes (cont.)

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
78	16M	800 X 600	40	37.8	60
78	16M	800 X 600	50	48.1	72
78	16M	800 X 600	49.5	46.9	75
78	16M	800 X 600	56.25	53.7	85
78	16M	800 X 600	68.2	63.6	100
7B	256/256K (interlaced)	1600 X 1200	135	62.5	48
7B	256/256K	1600 X 1200	162	75	60
7C	256/256K	1152 X 864	94.5	63.9	70
7C	256/256K	1152 X 864	108	67.5	75
7C	256/256K	1152 X 864	121.5	76.7	85
7C	256/256K	1152 X 864	143.5	91.5	100
7D	64K	1152 X 864	94.5	63.9	70
7D	64K	1152 X 864	108	67.5	75
7D	64K	1152 X 864	121.5	76.7	85
7D	64K	1152 X 864	143.5	91.5	100

For more information refer to the Cirrus Logic GD5480 Technical Reference Manual.

1.7.4 VGA connector

The following table shows the pin-out of the VGA connector:

Table 1.8: Video Port Connector Pin-out

Pin	Signal	Description
1	RED	Analog color signal R
2	GREEN	Analog color signal G
3	BLUE	Analog color signal B
4	nc	No connect
5	GND	Video ground (shield)
6	GND	Video ground (shield)
7	GND	Video ground (shield)
8	GND	Video ground (shield)
9	nc	No connect
10	GND	Video ground
11	nc	No connect
12	DDCDAT	Monitor ID data
13	HSYNC	Horizontal Sync
14	VSYNC	Vertical Sync
15	DDCCLK	Monitor ID clock

For more information refer to the *Cirrus Logic GD5480 Technical Reference Manual*.

1.8   PCI-B I/O Sub-system

PCI segments A and B are non-hierarchical and exist at the same level. PCI-B supports the following embedded devices and connectors:

- One Symbios SYM53C896 dual-channel SCSI-3 Ultra2 SCSI controller.

- Four 120-pin, 32-bit PCI expansion slot connectors, numbered PCI-B1, PCI-B2, PCI-B3, PCI-B4. Slot PCI-B4 is shared with an ISA slot.

- Slot PCI-B3 also supports the optional I_2O RAID card.

The PCI IDSEL signal connections to PCI AD[31::11] lines for PCI-B devices are shown in the following table.

Table 1.9: PCI-B Configuration IDs

IDSEL Value	Device
17	PCI Slot PB1
18	PCI Slot PCI-B2
19	Wide SCSI Controller
20	PCI Slot PCI-B3
21	PCI Slot PCI-B4

1.8.1 PCI-B Arbitration

PCI-B supports six PCI masters: slots PCI-B1 through PCI-B4, the wide SCSI controller, and the PXB. All PCI masters must arbitrate for PCI access using resources supplied by the PXB. The PXB PCI-B interface arbitration connections are internal to the device. The following table defines the external arbitration connections:

Table 1.10: PCI-B Arbitration Connections

Baseboard Signals	Device
S_REQ0_L/S_GNT0_L	PCI Slot PCI-B1
S_REQ1_L/S_GNT1_L	PCI Slot PCI-B2
S_REQ2_L/S_GNT2_L	PCI Slot PCI-B3
S_REQ3_L/S_GNT3_L	PCI Slot PCI-B4
S_REQ4_L/S_GNT4_L	unused
S_REQ5_L/S_GNT5_L	Wide SCSI controller

1.9   PCI-B Wide SCSI

PCI-B provides an embedded Symbios SYM53C896 dual channel LVD/SE (Ultra2/Ultra) SCSI controller. The SYM53C896 supports SE mode with 8-bit (10 MB/s or 20 MB/s) or 16-bit (20 MB/s or 40 MB/s) transfers and LVD mode with 8-bit (40 MB/s) or 16-bit (80 MB/s) transfers. The SYM53C896 is a highly integrated PCI-to-SCSI solution containing a high-performance PCI bus interface, DMA controller, internal SCRIPTS* engine, and a high-performance SCSI bus interface. PCI performance features include bursts of up to 128 Dwords for data rates of greater than 110 MB/s. The SCRIPTS* engine is a special high-speed processor optimized for SCSI protocol. The SCRIPTS engine and 8 KB of internal RAM for instruction storage can execute complex SCSI bus sequences independently of the host processor. The internal DMA, in combination with the SCRIPTS engine, creates a tightly-coupled connection between PCI and SCSI bus interfaces for optimum performance.

1.9.1 SYM53C896 PCI Signals

The SYM53C896 is a 64-bit PCI device and is interfaced to the 32-bit PCI bus in the S450NX MP Server. It supports all of the required 32-bit PCI signals including PERR_L and SERR_L. Full PCI parity is maintained on the entire data path through the component. The device has two programmable interrupt outputs which are connected to the PID. Refer to "Interrupts and the PID" later in this chapter for more details on interrupt routing in the I/O sub-system. The SYM53C896 does not support the CLKRUN_L, LOCK_L, SBO_L, SDONE_L and TRST_L signals. Support for these signals is specified as optional under the PCI 2.1 Specification.
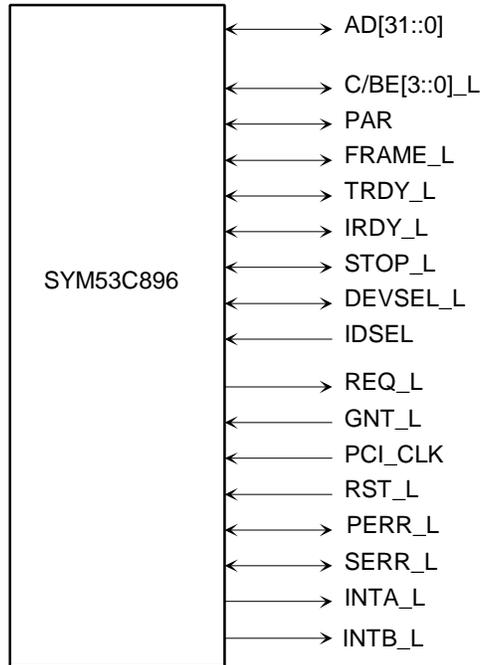
Figure 1.6: Embedded Wide SCSI PCI Signals

1.9.2 SCSI Interface

The SYM53C896 offers 8-bit or 16-bit SCSI operation at data transfer rates of 10, 20, 40, or 80 MB/s. The SYM53C896 uses Tolerant* technology for improved data integrity when running in the fastest SCSI transfer modes. Tolerant* technology includes active negation of SCSI signals when driving and programmable input signal filtering when receiving. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus avoiding indeterminate voltage levels and common-mode noise on long cable runs.

The SYM53C896 supports the SCSI 2, 8 or 16-bits wide bus with odd parity generated per byte. SCSI control signals are the same for either bus width. All SCSI signals are active low. SCSI P-connector cabling connects easily. During component power-down, all inputs are disabled to reduce power consumption.

```
SCLK  ────────▶ ┌──────────────┐ ◀────────▶ SD[15::0]_L
(40MHz)         │              │ ◀────────▶ SDP_L
                │              │ ◀────────▶ SDP1_L
                │              │ ◀────────▶ SC/D_L
                │              │ ◀────────▶ SI/O_L
                │              │ ◀────────▶ SMSG_L
                │   SYM53C896  │ ◀────────▶ SREQ_L
                │              │ ◀────────▶ SACK_L
                │              │ ◀────────▶ SRST_L
                │              │ ◀────────▶ SSEL_L
                │              │ ◀────────▶ SBSY_L
                │              │ ◀────────▶ SATN_L
                │              │ ─────────▶ GPIO0_L (LED_L)
                └──────────────┘
```
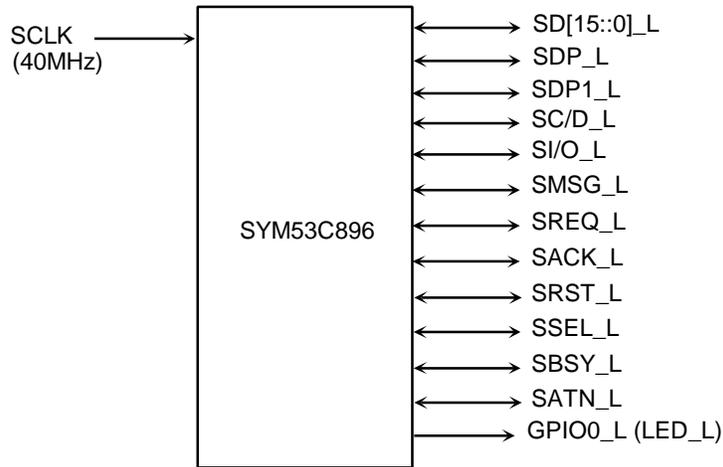
Figure 1.7: Wide SCSI Bus Signals

1.10   ISA I/O Sub-system

On the S450NX MP Server, the PIIX4(e) provides a bridge to an ISA I/O sub-system that supports the following connectors and devices:

- 1 ISA connector slot which supports slave only cards (**bus master cards are not supported**) and is physically shared with PCI slot PCI-B4.

  ISA Slot Length Restriction: **If wide SCSI channel B is used, only half length ISA cards are supported.**

- Flash memory for BIOS ROM and extensions.

- Baseboard Management Controller (BMC).

- PC87309 SuperI/O component, which supports the following:
    - ⇒ 2 PC-compatible serial ports
    - ⇒ Enhanced parallel port
    - ⇒ Floppy controller
    - ⇒ Keyboard/Mouse ports

The ISA interrupts are handled by either the PIIX4(e) or the PID. The PID handles interrupts in an MP environment. Refer to "Interrupts and the PID" later in this chapter for more information on these devices and how they are used in the S450NX MP Server interrupt structure.

1.10.1 I/O Controller Sub-system

The National 87309 SuperI/O device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. The S450NX MP Server provides the connector interface for each. Upon reset, the National 87309 reads the values on 3 GPO pins to determine its boot-up configuration. The S450NX MP Server baseboard configures the SuperI/O into Plug and Play baseboard and 2 UART modes.

1.10.2 Serial Ports

Two 9-pin connectors are provided in one stacked 9-pin D-Sub housing for Serial port A and Serial port B. By default port A is physically the top connector, port B is on the bottom. Both ports are compatible with 16550A and 16450 modes and are re-locatable. Each serial port can be set to 1 of 4 different COM ports and can be enabled separately. When enabled, each port can be programmed to generate edge or level sensitive interrupts. When disabled, serial port interrupts are available to add-in cards. Pin-out is shown below:

Table 1.11: Serial Port Connector Pin-out

Pin	Name	Description
1	DCD	Data Carrier Detected
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Request to Send
8	CTS	Clear to Send
9	RIA	Ring Indication Active

1.10.3 Parallel Port

The 25/15 pin connector stacks the parallel port connector over the VGA connector. BIOS programming of the National 87309 registers enable the parallel port, and determine the port address and interrupt. When disabled, the interrupt is available to add-in cards. Pin-out is shown below:

Table 1.12: Parallel Port Connector Pin-out

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

1.10.4 Floppy Disk Controller

The FDC in the National 87309 is functionally compatible with floppy disk controllers in the DP8473 and N82077. The baseboard provides the 24MHz clock, termination resistors, and chip selects. All other FDC functions are integrated into the National 87309 including analog data separator and 16-byte FIFO. The floppy connector on the baseboard has the pin-out shown in table 1.13.

Table 1.13: Floppy Port Connector Pin-out

Pin	Name	Pin	Name
1	GND	18	FD_DIR_L
2	FD_DENSEL	19	GND
3	GND	20	FD_STEP_L
4	n/c	21	GND
5	Key	22	FD_WDATA_L
6	FD_DRATE0	23	GND
7	GND	24	FD_WGATE_L
8	FD_INDEX_L	25	GND
9	GND	26	FD_TRK0_L
10	FD_MTR0_L	27	FD_MSEN0
11	GND	28	FD_WPROT_L
12	FD_DR1_L	29	GND
13	GND	30	FD_RDATA_L
14	FD_DR0_L	31	GND
15	GND	32	FD_HDSEL_L
16	FD_MTR1_L	33	GND
17	FD_MSEN1	34	FD_DSKCHG_L

1.10.5 Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single stacked housing. The mouse connector is stacked over the keyboard connector. External to the board they appear as two connectors. The keyboard controller is functionally compatible with the 8042A. The keyboard and mouse connectors are PS/2 compatible, with pin-outs shown in tables 1.14 and 1.15.

Table 1.14: Keyboard Connector Pin-out

Pin	Signal	Description
1	KEYDAT	Keyboard Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	KEYCLK	Keyboard Clock
6	(NC)	

Table 1.15: Mouse Connector Pin-out

Pin	Signal	Description
1	MSEDAT	Mouse Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	MSECLK	Mouse Clock
6	(NC)	

1.11   System Reset Control

Reset circuitry on the S450NX MP Server baseboard looks at resets from the front panel, PIIX4(e), I/O controller, and processor sub-system to determine proper reset sequencing for all types of reset. The reset logic is designed to accommodate a variety of ways to reset the system, which can be divided into the following categories:

- Power-up reset

- Hard reset

- Soft (programmed) reset

1.11.1 Power-up Reset

When the system is disconnected from power, all logic on the baseboard is not powered. When proper AC line voltage is provided to the power supply, 5 Volt standby power will be applied to the baseboard. A power monitor circuit on 5 Volt standby will assert RST_BMC, causing the Baseboard Management Controller (BMC) to reset. The BMC is powered by 5 Volt standby and monitors and controls key events in the system related to reset and power control.

1.11.2 Hard Reset

Hard reset may be initiated by software, by the user resetting the system through the front panel switch, or through the Server Management Module. For a software initiated reset, the MIOC Reset Control (RC) register should be used. The BMC is not reset by a hard reset. It may be reset at power-up.

1.11.3 Soft Reset

Soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers. Soft resets may be generated by the keyboard controller located in the 87309 SIO, by the PIIX4(e), or by the MIOC. The output of the 87309 is input to the PIIX4(e), and combined with its internal sources to drive the PIIX4(e). Both the PIIX4(e) and MIOC are open collector signals and are wire ORed on baseboard and connected to the Slot 2 connectors.

1.11.4 Reset Diagram

Reset flows throughout the S450NX MP Server baseboard as shown in the following figure.
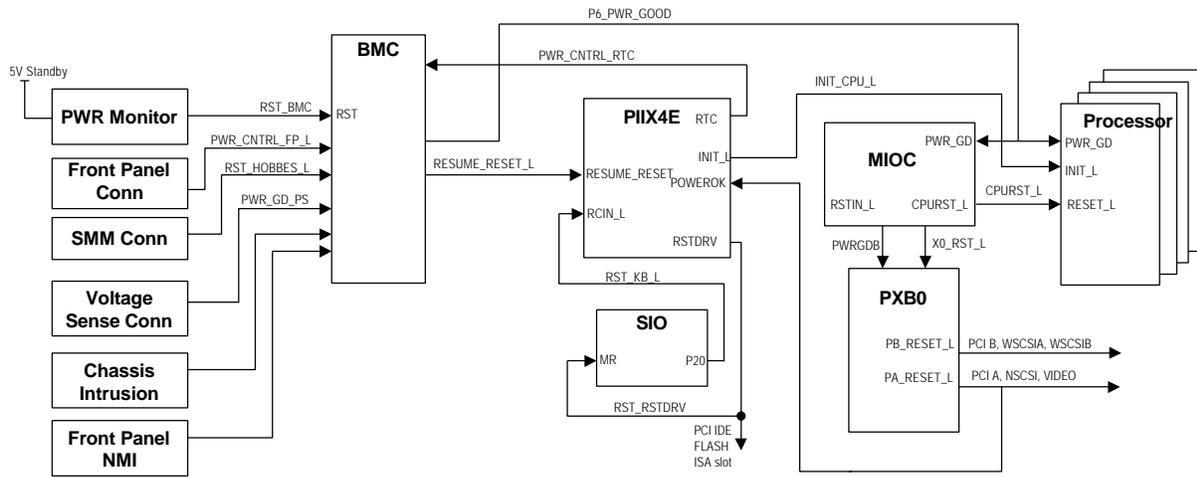
Figure 1.8: Reset Flow Diagram

1.12 Clock Generation and Distribution

There are three clock sources used on the S450NX MP Server baseboard. The 100MHz host clocks are generated from a 1:12 clock distribution component. The MIOC generates the 100MHz clock for the two F16 busses to the PXBs. The PXB generates two 33.3MHz PCI reference clocks for the two PCI busses. A clock generator on the baseboard generates two 48MHz clocks (USB and SuperI/O), two 40MHz clocks (Wide and Narrow SCSI controllers), and three 14.318MHz clocks (PIIX4(e), Video, and ISA slot). Since the BMC runs off of 5V standby, the BMC has its own crystal providing a 22.1184MHz time reference. The baseboard also has a low skew clock buffer to distribute the PCI reference clock to all the embedded PCI devices and to all PCI slots. The baseboard also divides a host clock by 4 for five 25MHz APIC clocks (PROC4-PROC1 and PID). The following figure illustrates clock generation and distribution on the S450NX MP Server baseboard.
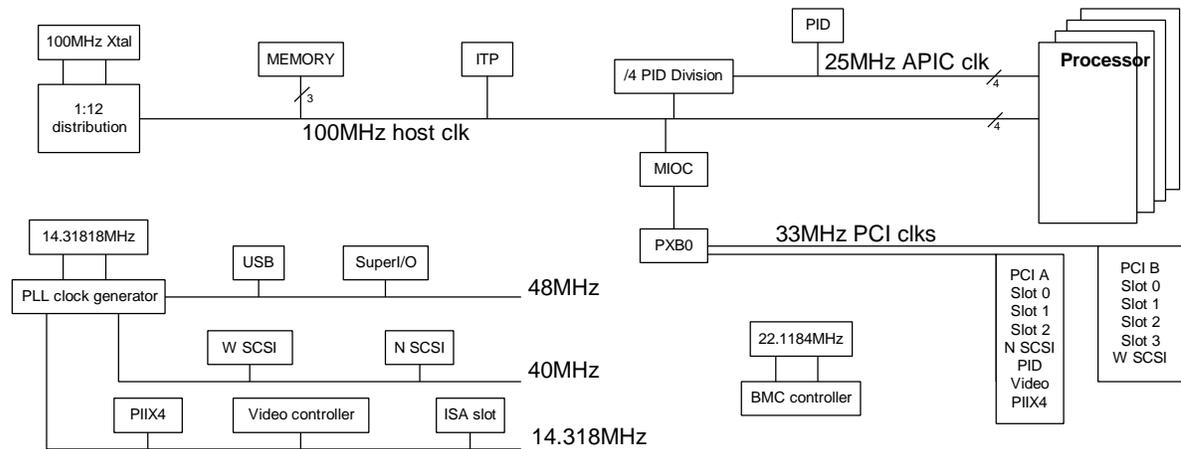
Figure 1.9: S450NX MP Server Baseboard Clock Distribution

1.13   Interrupts and the PID

The S450NX MP Server interrupt architecture accommodates both PC-compatible PIC mode, and APIC mode interrupts through use of the Programmable Interrupt Device (PID).

1.13.1 PIIX4(e) Compatibility Interrupt Controller

For PC-compatible mode, the PIIX4(e) provides two 82C59-compatible interrupt controllers embedded in the device. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The PIIX4(e) and 87309VUL contain configuration registers that define which interrupt source logically maps to I/O APIC INTx pins.

1.13.2 Intel PID

For APIC mode, the S450NX MP Server interrupt architecture incorporates the Intel PID device, to manage and broadcast interrupts to local APICs in each processor. The PID monitors each interrupt on each PCI device including PCI slots in addition to the compatible interrupts IRQ(0-15) , and on occurrence of an interrupt sends a message corresponding to the interrupt across a three wire serial interface to the local APICs. The APIC bus minimizes interrupt latency time for compatibility interrupt sources. The PID can also supply greater than 16 interrupt levels to the processor(s). This APIC bus consists of an APIC clock, and two bi-directional data lines. The PXB1 expansion slot has reserved signals for four PCI interrupts.
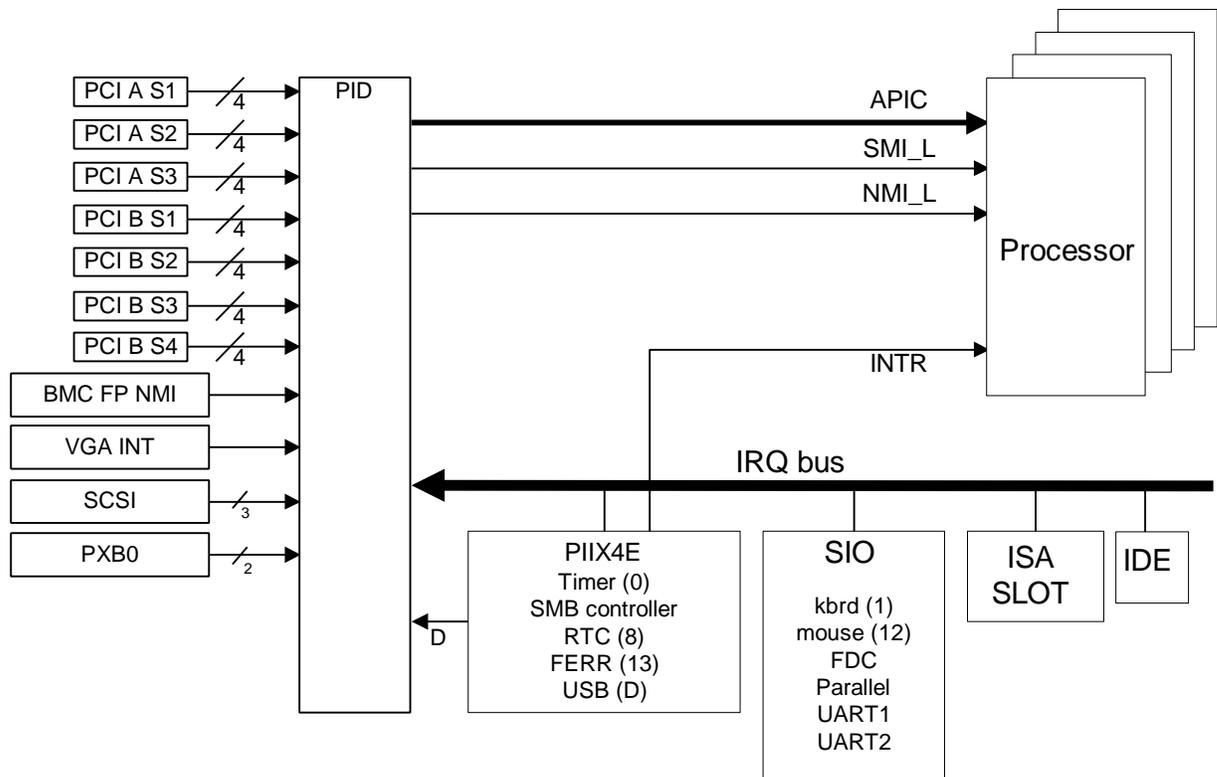
Figure 1.10: S450NX MP Server Baseboard Interrupt Diagram

1.13.3 Interrupt Routing

Interrupts, both PCI and IRQ types, are handled by the PID. The PID then translates these to the APIC bus.

1.13.4 Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on the S450NX MP Server baseboard. The actual interrupt map is defined using configuration registers in the PIIX4(e) and the PID.

Table 1.16: Interrupt Definitions

Interrupt	I/O APIC level	Description
INTR	INT0	Processor interrupt.
NMI		NMI from PID to processor.
IRQ1	INT1	Keyboard interrupt.
Cascade	INT2	Interrupt signal from second 8259 in PIIX4(e).
IRQ3	INT3	Serial port A or B interrupt from SIO device, user-configurable.
IRQ4	INT4	Serial port A or B interrupt from SIO device, user-configurable.
IRQ5	INT5	Parallel port.
IRQ6	INT6	Floppy disk.
IRQ7	INT7	Parallel port.
IRQ8_L	INT8	RTC interrupt.
IRQ9	INT9	
IRQ10	INT10	
IRQ11	INT11	
IRQ12	INT12	Mouse interrupt.
	INT13	
IRQ14	INT14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1.
IRQ15	INT15	
SMI_L		System Management Interrupt. General purpose indicator sourced by the PIIX4(e) and BMC through the PID to the processors.

1.14 System Board Jumpers

One 11-pin single inline header provides a total of three 3-pin jumper blocks that control various configuration options, as shown in figure 1.11. The shaded areas show default jumper placement for each configurable option.

J6J1

CMOS:
- BMC Control
- Protect (no jumper)
- Clear

Password:
- Protect
- Clear

BOOT Option:
- Normal Boot
- Recovery Boot
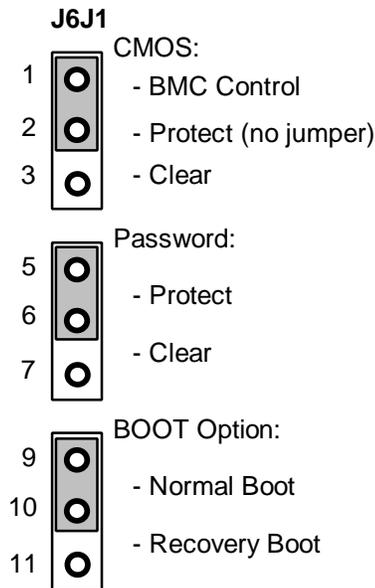
Figure 1.11: Configuration Jumpers

The following table details the baseboard jumper functions.

Table 1.17: Board Jumper description

Function	Pins (default in bold)	What it does at system reset
CMOS clear	**1-2, Protect**	Preserves the contents of NVRAM.
	2-3, Erase	Replaces the contents of NVRAM with the Intel manufacturing default settings.
Password clear	**5-6, Protect**	Maintains the current system password.
	6-7, Erase	Clears the password.
BOOT Option	**9-10, Normal**	System attempts to boot using the BIOS stored in flash memory.
	10-11, Recovery	BIOS attempts a recovery boot, loading BIOS code from a floppy diskette into the flash device. This is typically used when the BIOS code has been corrupted.

1.15 RAID Configuration

Certain PCI RAID solutions require mapping of interrupts from the SCSI controller to the PCI RAID controller. Slot 3 of PCI bus B supports this function. Normally the TDI pin of this slot is high and all four PCI interrupts act as on any other slot. If a PCI RAID card is used, TDI goes low and indicates to the PID to re-route the two wide SCSI interrupts to the I_2O outputs of the PID. This allows the PCI RAID card access to the SCSI controller interrupts on slot interrupts C and D and maintain normal card interrupts on A and B.
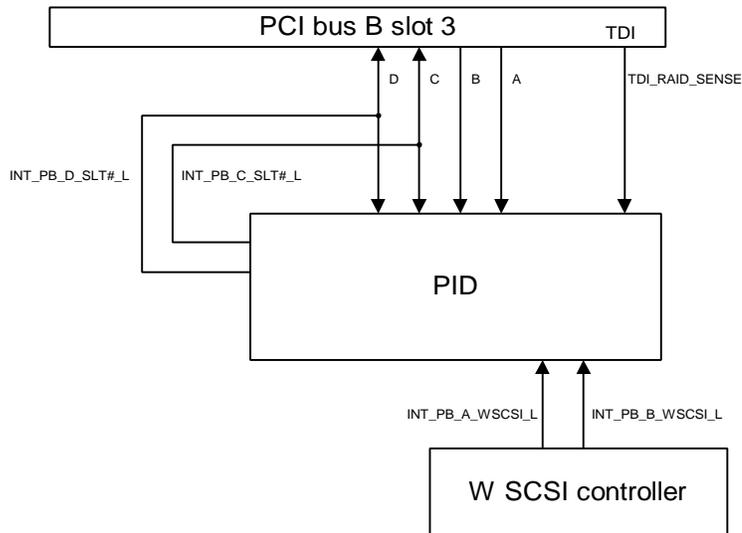
Figure 1.12: RAID configuration

2. Server Management

S450NX MP Server Management features are implemented using a Dallas 80CH10 controller.

The following diagram illustrates S450NX MP Server Management architecture. A description of the hardware architecture follows.
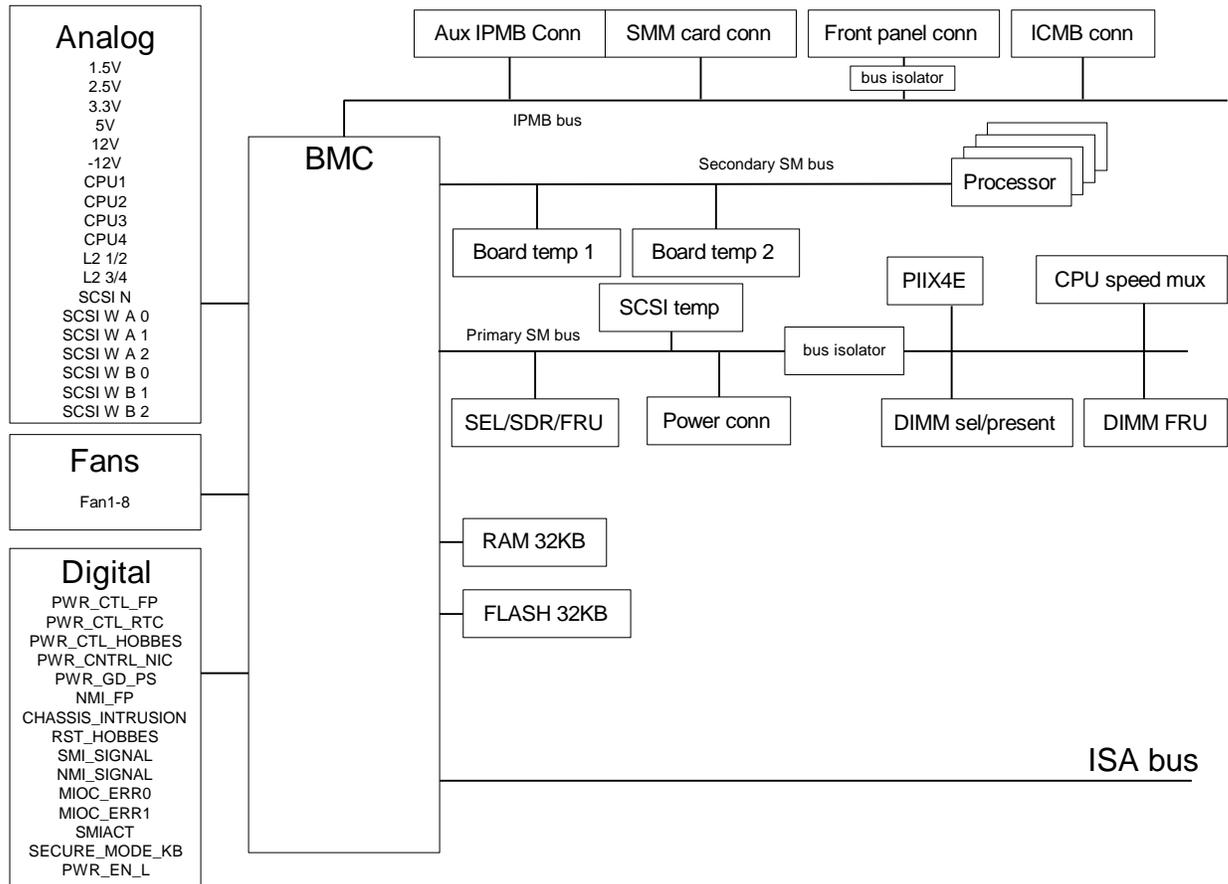
Figure 2.1: S450NX MP Server Management Block Diagram

2.1   Intelligent Management Bus

Management controllers (and sensors) communicate on the Intelligent Platform Management Bus. A bit protocol defined by the IPMB specification and a byte-level protocol defined by the *Intelligent Management Bus Communications Protocol Specification*, provide an independent interconnect for all devices operating on the IPMB bus. The IPMB extends throughout the baseboard and system chassis. An additional layer in the protocol supports transactions between multiple servers on interchassis IPMB bus segments.

The IPMB connects to various devices external to the baseboard. The IPMB connectors outside of the baseboard (Aux IPMB, SMM card, and ICMB) cannot load the bus without power, as this would prevent bus communication.

2.2   Baseboard Management Controller (BMC)

The BMC is an 8051-compatible microcontroller located on the baseboard. The BMC monitors baseboard power supply and SCSI termination voltages using an external Analog to Digital Converter (ADC), and checks the status of the fan failure indicators. The BMC also monitors system temperature sensors on the IPMB and on the BMC private IPMB buses. When any monitored parameter is outside defined thresholds, the BMC generates SMI_L. The BMC also provides general-purpose I/O (GPIO) functions, and acts as the primary communications gateway by providing support routines for IPMB and ISA communications.

2.3   Front Panel Connector

A 30-pin header is provided that attaches to the system front panel, which contains reset, NMI, sleep, power control switches, LED indicators, and IPMB connection.

2.3.1 Baseboard / Front Panel Interface

Table 2.1: Baseboard / Front Panel Interface

Pin #	I/O	Description
1	I	5V pulse speaker input
2		GND
3	O	TTL High True = chassis intrusion
4	I	TTL Low true = hard disk activity
5		5V VCC
6	O	TTL Low True = toggle ACPI sleep/service
7	I	TTL Low True = fan failed condition
8	I	TTL Low True = system power on condition TTL pulse = system in sleep mode
9	I	TTL Low True = power fault condition
10		GND
11	I/O	IPMB - SDA
12	O	TTL Low True = NMI to CPU
13	I/O	IPMB - SCL
14	O	TTL Low True = reset system
15		5V VCC Standby
16	O	TTL Low True = toggle system power
17		Reserved
18		GND
19	O	Open Collector pulse = fan 1 speed
20	O	Open Collector pulse = fan 2 speed
21	O	Open Collector pulse = fan 3 speed
22	O	Open Collector pulse = fan 4 speed
23	O	Open Collector pulse = fan 5 speed
24	O	Open Collector pulse = fan 6 speed
25	O	Open Collector pulse = fan 7 speed
26	O	Open Collector pulse = fan 8 speed
27	I	TTL Low True = electronics bay power on condition TTL pulse = electronics bay power off condition
28		NC

Table 2.1: Baseboard / Front Panel Interface (continued)

Pin #	I/O	Description
29		NC
30		NC

2.3.2 Hot Swap Backplane / Front Panel Interface

Table 2.2: Hot Swap Backplane / Front Panel Interface

Pin #	I/O	Description
1	I/O	IPMB - SDA
2	PWR	GND
3		NC
4	I/O	IPMB - SCL
5	I	TTL Low True = Disk drive 1 fault
6	I	TTL Low True = Disk drive 0 fault
7	I	TTL Low True = Disk drive 3 fault
8	I	TTL Low True = Disk drive 2 fault
9	I	TTL Low True = Disk drive 5 fault
10	I	TTL Low True = Disk drive 4 fault

2.3.3 Chassis Intrusion Switch Connector / Front Panel Interface

Table 2.3: Chassis Intrusion Switch Connector / Front Panel Interface

Pin #	I/O	Description
1	O	TTL High True = Chassis switch
2	PWR	Chassis switch return (GND or output of next chassis switch connector)
3	O	TTL High True = Chassis switch

2.3.4 Fan Power Connector / Front Panel Interface

Table 2.4: Fan Power Connector / Front Panel Interface

Pin #	I/O	Description
1	PWR	+12V
2	PWR	GND

2.3.5 Fan Connector /Front Panel Interface

Table 2.5: Fan Connector / Front Panel Interface

Pin #	I/O	Description
1	PWR	GND
2	I	Open Collector pulse = fan speed
3	PWR	+12V

2.4   Fault Resilient Booting

The BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If the default boot strap processor (BSP) fails to complete the boot process, FRB attempts to boot using an alternate processor.

- FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.

- FRB level 2 is for recovery from a Watchdog timeout during POST. The Watchdog timer for FRB level 2 detection is implemented in the BMC.

- FRB level 3 is for recovery from a Watchdog timeout on Hard Reset / Power-up. Hardware functionality for this level of FRB is provided by the BMC.

FRB-3 is managed by the BMC, which controls the ability to boot using either processor in the event of a catastrophic processor failure. On power up, a timer starts that can only be stopped by a healthy processor using the GPIO bit, FRB_TMRHLT_L, on the PIIX4(e) component. If processor 0 fails to halt the FRB timer before timeout, the controller asserts P6_0_STOP_L to the processor and resets the system. When the system comes out of reset, processor 0 is unable to act as the boot processor allowing the other processor to take over the boot process.

2.5   Auxiliary IPMB Connector

A 3 pin auxiliary IPMB connector is provided for access to the IPMB.

Table 2.6: Auxiliary IPMB Connector Pin-out

Pin	Signal
1	Local IPMB SCL
2	GND
3	Local IPMB SDA

Warning! A shorted IPMB connection at the auxiliary IPMB connector will prevent restoration of main power since the BMC needs the bus to boot the server from standby power.

2.6   ICMB Connector

A 6 pin edge connector is used to interface with the ICMB module. Listed below is the ICMB connector pin-out.

Pin	Signal	Type	Description
1	SDA	In/out	IPMB Data
2	+5V	Pwr	+5V Power Supply
3	GROUND	Pwr	Ground

2.7   Server Monitor Module Connector

The Server Monitor Module feature connector is supported on the baseboard. The pin-out of the 20-pin baseboard connector is shown in the following table. Type (in/out) is from the perspective of the baseboard. Note that pins 1, 9, 15, and 17 are connected on the S450NX MP Server baseboard to SMI_L, NMI, SECURE_MODE, and CHASSIS_INTRUSION, but these signals are not monitored on any existing or planned SM module.

Table 2.7: Server Monitor Module Connector Pin out

Pin	Signal	Type	Description/S450NX MP Server Implementation
1	SMI_L	out	System Management Interrupt: *not supported on SMM*
2	IPMB_SCL	in	IPMB clock line
3	CONP_L	out	Connector Present - tied to ground on the baseboard
4	Key		no connect on baseboard
5	PWR_CNTL_L	in	Power supply on/off control - allows SMM to control system power
6	IPMB_SDA	in/out	IPMB serial data line
7	5VSTNDBY	out	+5V standby - monitored by SMM to determine if AC power is applied
8	Reserved		no connect on baseboard
9	NMI	out	Non-maskable interrupt: *not supported on SMM*
10	HOST_AUX	out	Baseboard voltage monitored by SMM card - connected to 3.3V
11	RESET_L	in	Baseboard reset signal from Server Monitor Module
12	GND		Ground
13	GND		Ground
14	Key		no connect on baseboard
15	SECURE_MODE	out	Secure mode indication: *not supported on SMM*
16	GND		Ground
17	CHASSIS_INTRUSION	out	Chassis intrusion indication: *not supported on SMM*
18	Reserved		Reserved pin - NC on baseboard
19	Reserved		Reserved pin - NC on baseboard
20	GND		Ground

2.8   System Fan Interface

The S450NX MP Server baseboard monitors up to eight fans. All of the fans are equipped with a sensor that indicates whether the fan is operating (tachometer fan). The sensor pins for these fans are routed to the BMC through the front panel for failure monitoring. When the BMC senses a failure on any of the dual speed fans, it sends a command to the power share controller (PSC) which asserts the FAN_SPEED_CTL signal to increase the speed of the remaining fans.

3. Memory and Other Resource Mappings

This chapter describes the initial programming environment for S450NX MP Server, including memory and I/O maps, and provides an overview of related software and required firmware. During initialization and run-time, BIOS, operating system, and application software operate in an environment which is defined by memory and I/O mapping.

3.1   Memory Space

At the highest level, the Pentium II® Xeon™ processor address space is divided into three major regions, as shown in the following figure. Each region is divided into sub-regions, as described in following sections. Attributes can be independently assigned to regions and sub-regions using Intel 82450NX PCIset configuration registers.

Extended Pentium II Xeon Processor Region. Unused on S450NX.

Extended Memory Region

DOS Compatibility Region

64 GB

4 GB
(Top of Physical DRAM)

512 MB

Optional Fixed Memory Hole

16 MB

15 MB

1 MB

640 KB

512 KB

0
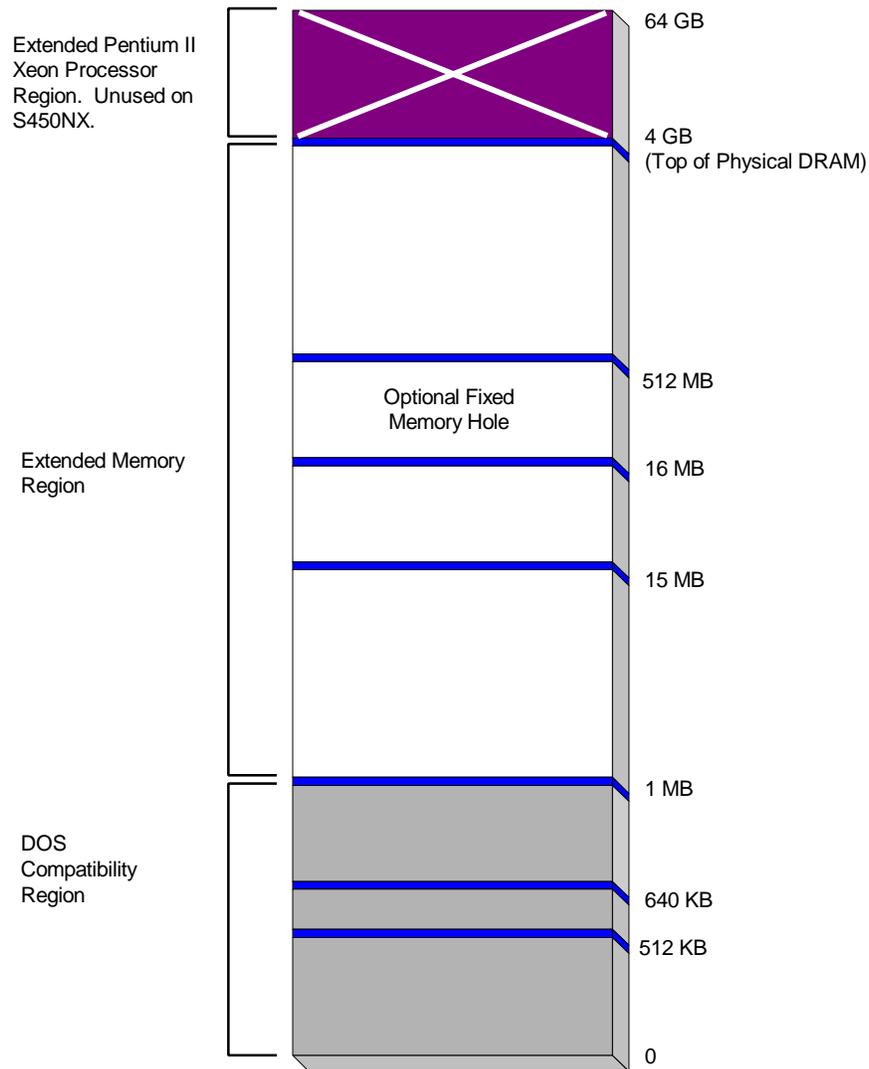
Figure 3.1: Pentium II® Xeon™ Slot 2 processor memory address space

3.1.1 DOS Compatibility Region

The DOS Compatibility Region spans the first 1MB address range (0h to FFFFFh). This was the first memory region defined for early server systems, and is maintained for backward compatibility. This region is divided into sub-regions as shown in the following figure.
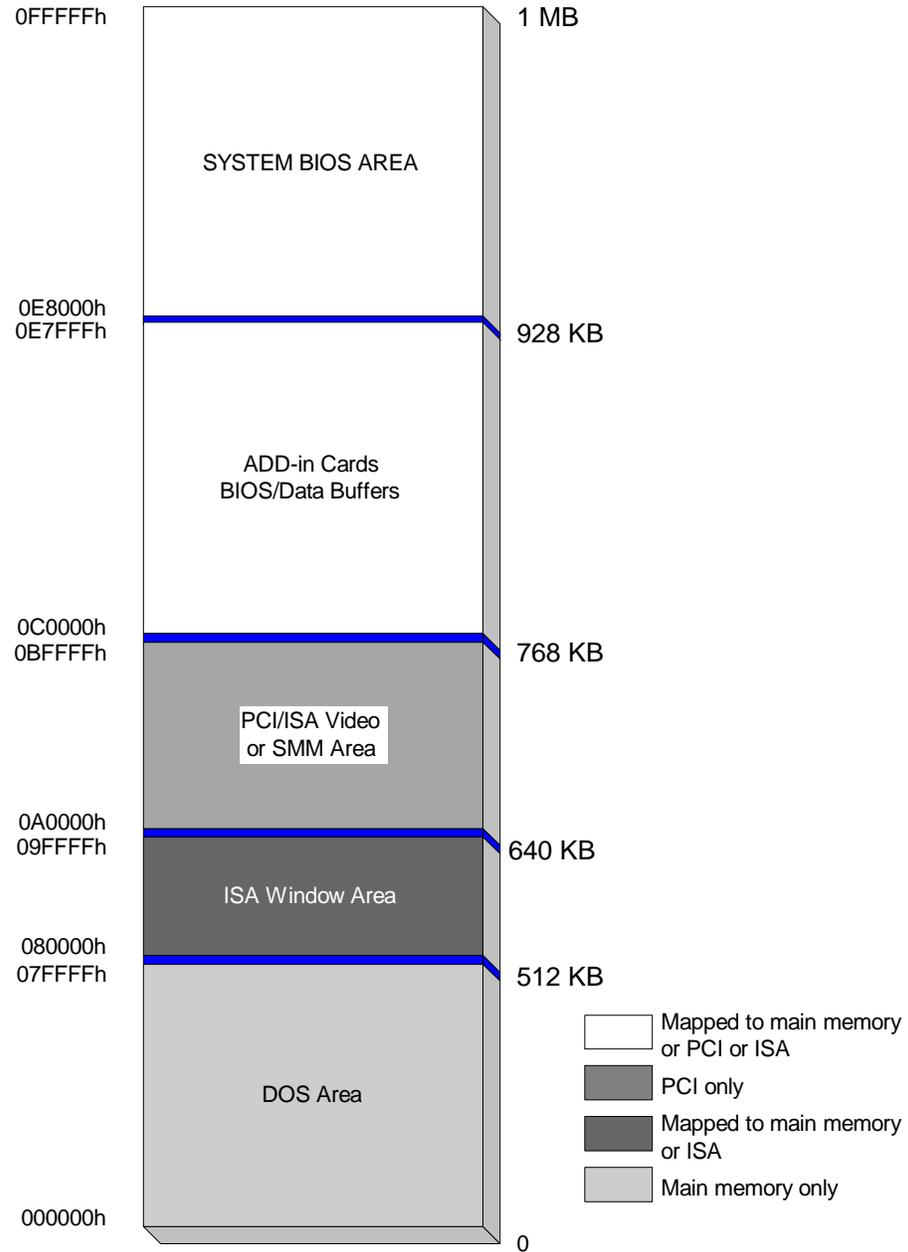
Figure 3.2: DOS Compatibility Region

3.1.2 DOS Area

The DOS region is 512KB in the address range 0 to 07FFFFh. This region is fixed and all accesses go to main memory.

3.1.3 ISA Window Memory

The ISA Window Memory is 128KB between the addresses of 080000h to 09FFFFh. This region can be mapped to main memory in the Intel 82450NX PCIset or to PCI memory on the compatibility bus.

3.1.4 Video or SMM Memory

The 128 KB Graphics Adapter Memory area at 0A0000H to 0BFFFFh is mapped to a VGA video controller on the compatibility PCI bus, PCI Bus A. This area is also the default region for SMM space. The SMM region can be remapped by programming the SMM RAM Control Register in the MIOC configuration space.

3.1.5 Add-in Card BIOS and Buffer Area

The memory region from 0C0000h to 0C7FFFh contains the VGA BIOS for a video card in the ISA expansion area. The remaining space, up to 0DFFFFh, is divided into 16KB segments with programmable attributes. This area can be used for shadowed or unshadowed option ROM code and data buffers for add-in cards.

3.1.6 System BIOS

The first 64 KB region from E0000h to EFFFFh is divided into four 16KB blocks and may be mapped either to main memory or the compatibility PCI bus. Each 16KB block has individual read/write attribute enables defined in the MAR register. These may be used to direct accesses to PCI memory or shadowed main memory. Typically, this area is used for Extended System Configuration Data (ESCD) and system BIOS code. The 64KB region from 0F0000h to 0FFFFFh is treated as a single block. Read/write attribute enables defined in the MAR registers may be used to direct accesses to the compatibility PCI bus or shadowed main memory. After power-on reset, the Intel 82450NX PCIset has this area configured to direct accesses to PCI memory, allowing fetches from the boot ROM during system initialization.

3.1.7 Extended Memory

Extended Memory on S450NX MP Server is defined as all address space greater than 1MB. This memory region covers 4GB from addresses 0100000h to FFFFFFFFh, as shown in the following figure.
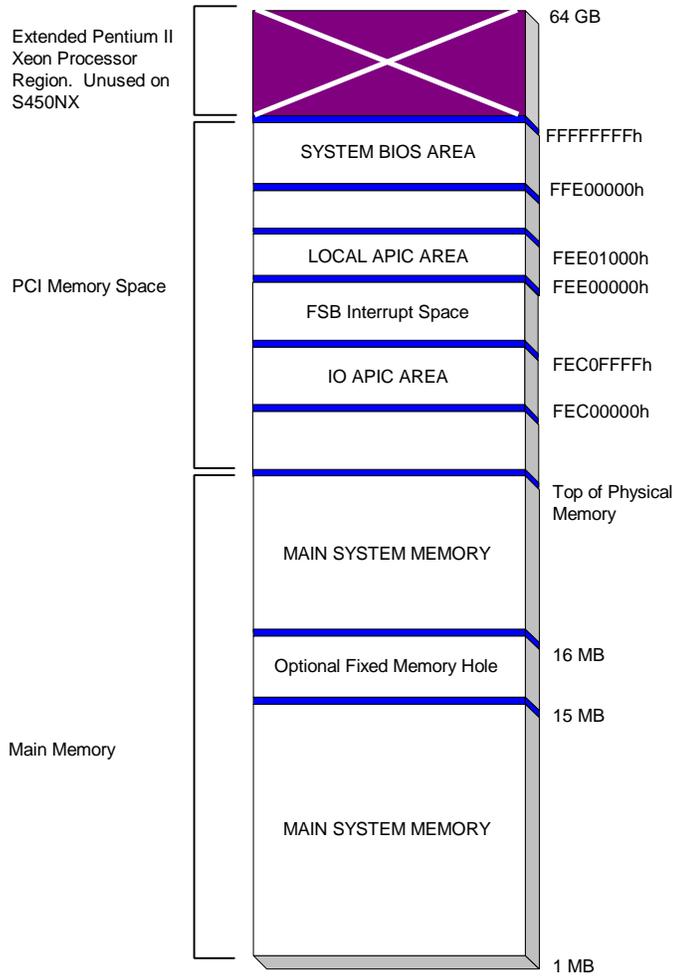
Figure 3.3: Extended Memory Map

3.1.8 Main Memory

All installed DRAM greater than 1MB is mapped to local main memory, up to the top of physical memory. Memory in this area up to 15MB is considered to be standard extended memory. 1MB of memory starting at 15MB can be optionally mapped to PCI memory space. The remainder of this space, up to the top of physical DRAM, is always mapped to main memory.

3.1.9 PCI Memory Space

The PCI Memory Region spans 20MB immediately below the 4GB address boundary (address range FEC00000h to FFFFFFFFh). This region supports pre-defined structured areas for compatibility with server-based systems. The PCI Memory region is divided into four sub-regions: High BIOS, Local APIC Configuration Space, FSB Interrupt Space, and General-purpose PCI Memory. The General-purpose PCI Memory area is typically used for memory-mapped I/O to PCI devices. The memory address space for each device is set using PCI configuration registers.

3.1.10 High BIOS

This is a 2MB space that spans the 4GB minus 2M to 4GB address range (FFFE0000h to FFFFFFFFh). The Pentium II® Xeon™ Processor will begin execution from this region after reset. Following power-on, Intel 82450NX PCIset has this space enabled. When enabled, accesses to this space will be directed to the compatibility PCI bus. This area is then aliased by the ISA bridge (PIIX4(e)) to the top of the ISA address range (14-16MB). Only 512KB of this area is actually required by the BIOS, but 2MB is required by Pentium II Xeon processor Slot 2 MTRR programming.

3.1.11 Local APIC Space

The local APIC resident inside the processor is mapped to address FEE00000h to FEE01000h. Accesses to this region will not be claimed by the Intel 82450NX PCIset.

3.1.12 FSB Interrupt Space

This 1MB block is reserved for use by future processor generations as a Front-Side Bus (FSB) interrupt delivery space. No external resources should be mapped to this region.

3.1.13 I/O APIC Configuration Space

This 1MB block, from address 0FEC00000h(4 GB minus 20 MB) to 0FEC0FFFFh, is reserved for the APIC configuration space, which includes the default I/O APIC configuration space. The Programmable Interrupt Device (PID) is used for this function. Up to sixteen APICs can be supported. The I/O APIC units are located beginning at a base address determined by subtracting 013FFFF0 from the reset vector. The first I/O APIC is located at FEC00000h. Each I/O APIC unit is located at FECx0000h where 'x' is the I/O APIC unit (0 through F).

3.1.14 Extended Pentium II Xeon Slot 2 Region (above 4GB)

A Pentium II Xeon Slot 2 system can have up to 64GB of addressable memory. However, S450NX MP Server system only supports up to maximum of 4GB of addressable memory. All accesses to the region from 4GB to 64GB are claimed by the Intel 82450NX PCIset and terminated. Write data is dropped and zeroes are returned on reads.

3.1.15 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be "shadowed" into main memory. Typically, this allows ROM code to execute more rapidly out of RAM. ROM is designated read-only during the copy process while RAM, at the same address, is designated write-only. After copying, the RAM is designated read-only and the ROM is designated write-only (shadowed). Processor bus transactions are routed accordingly. Transactions originated from PCI or ISA masters and targeted at shadowed memory blocks are unseen by the processor bus.

3.1.16 SMM Mode Handling

A Pentium II® Xeon™ processor asserts SMMEM_L (A7_L) in the second clock of the request phase if it is operating in System Management Mode (SMM). SM code resides in SMRAM. SMRAM can overlap with memory residing on the Pentium II Xeon processor bus or memory normally residing on the PCI bus. The Intel 82450NX PCIset determines where SMRAM space is located through the value of the SMM RAM Control Register. The SMRAM Enable bit in the SMM RAM Control Register determines how SM accesses are handled by the Intel 82450NX PCIset. When the SMRAM Enable bit is zero (SMRAM disabled), accesses to the SMM Range with SMMEM_L asserted are ignored by the Intel 82450NX PCIset. When the SMRAM Enable bit is one (SMRAM enabled), accesses to the SMM range with SMMEM_L asserted are claimed by the Intel 82450NX PCIset. If the SMMEM_L signal is not asserted, the SMM Range is not decoded regardless of the state of the SMRAM Enable bit. This allows SMRAM to overlap with memory normally residing on the processor bus.

In summary, when the SMMEM_L signal is asserted, the SMM Range is similar to a Memory Space Gap, where the SMM Enable bit either enables or disables the memory gap. The SMI_L signal may be asserted in the Response Phase by a device in SMM power-down mode.

3.2   I/O Map

The Intel 82450NX PCIset allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including the PIIX4(e), have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On the S450NX MP Server, the PIIX4(e) provides the bridge to ISA functions.

The following components contain registers that are accessible through either PCI configuration space or local I/O space. Refer to each component for specifics on the addresses and register set supported by each device. The programming of each of these components affects the global I/O map as numerous registers can be relocated or even disabled.

- Intel 82450NX PCIset

- PCI ISA IDE Xcelerator 4 (PIIX4(e))

- Symbios SYM53C810AE Narrow Fast SCSI Controller

- Cirrus Logic GD5480 Video Component

- Symbios SYM53C896 Ultra / Ultra II SCSI Controller

- Intel Programmable Interrupt Device (PID)

- National 87309 SuperI/O Component (SIO)

- Baseboard Management Controller (BMC)

3.3   Accessing Configuration Space

All PCI devices contain PCI configuration space, accessed using mechanism #1 defined in the *PCI Local Bus Specification*. The PIIX4(e) is a multi-function PCI device with 3 sets of configuration registers. If multiple processors are used, only the processor designated as the bootstrap processor (BSP) should perform PCI configuration space accesses as defined here. Precautions should be taken to guarantee that only one processor is accessing configuration space at a time. Two Dword I/O registers in the Intel 82450NX PCIset are used for the configuration space register access:

- CONFIG_ADDRESS (I/O address 0CF8h)

- CONFIG_DATA (I/O address 0CFCh)

When CONFIG_ADDRESS is written with a 32-bit value selecting the bus number, device on the bus, and specific configuration register in the device, a subsequent read or write of CONFIG_DATA initiates the data transfer to/from the selected configuration register. Byte enables are valid during accesses to CONFIG_DATA; they determine whether the configuration register is being accessed or not. Only full Dword reads and writes to CONFIG_ADDRESS are recognized as a configuration access by the Intel 82450NX PCIset. All other I/O accesses to CONFIG_ADDRESS are treated as normal I/O transactions.

3.3.1 CONFIG_ADDRESS Register

CONFIG_ADDRESS is 32 bits wide and contains the field format shown in the following figure. Bits [23::16] choose a specific bus in the system. Bits [15::11] choose a specific device on the selected bus. Bits [10::8] choose a specific function in a multi-function device. Bits [7::2] select a specific register in the configuration space of the selected device or function on the bus.

31 30		24 23		16 15		11 10	8 7		2 1	0
	Reserved		Bus Number		Device		Function	Register		0	0

Enable bit ('1' = enabled. '0' = disabled)

Figure 3.4: CONFIG_ADDRESS Register

3.3.2 Device Number and IDSEL Mapping

Each device under a PCI bridge has its IDSEL input connected to one bit out of the PCI bus address/data signals AD[31::11] for the primary bus, AD[31::16] for the secondary bus. Each IDSEL-mapped AD bit acts as a chip select for each device on PCI-A and PCI-B. The host bridge and PCI-to-PCI bridge respond to a unique PCI device ID value, that along with the bus number, cause the assertion of IDSEL for a particular device during configuration cycles. The following table shows the correspondence between IDSEL values and PCI device numbers for both PCI buses. The lower 5-bits of the device number are used in CONFIG_ADDRESS bits [15::11].

Table 3.1: PCI Configuration IDs and Device Numbers

IDSEL	PCI-A Bus Device #	PCI-A Bus Device	PCI-B Bus Device #	PCI-B Bus Device
31	01111b		01111b	
31	01111b		01111b	
30	01110b		01110b	
29	01101b		01101b	
28	01100b	PIIX4(e)	01100b	
27	01011b	PID	01011b	
26	01010b	GD5480 Video Controller	01010b	
25	01001b	PCI-A Slot 3	01001b	
24	01000b	Narrow SCSI (SYM53C810AE)	01000b	
23	00111b	PCI-A Slot 2	00111b	
22	00110b	PCI-A Slot 1	00110b	
21	00101b		00101b	PCI-B Slot 4
20	00100b		00100b	PCI-B Slot 3
19	00011b		00011b	Wide SCSI A/B (SYM53C896)
18	00010b		00010b	PCI-B Slot 2
17	00001b		00001b	PCI-B Slot 1
16	00000b		00000b	

3.4   Error Handling

The S450NX MP Server is designed to report these types of system errors: ISA bus, PCI bus, ECC memory, and system limit. Errors are reported using SMI_L. SMI is used for server management and advanced error processing. All errors can be intercepted by SMI for preprocessing (if SMI_L is enabled), or handled directly by NMI handlers. Some errors have to generate an NMI even if they are intercepted by the SMI because the traditional way to handle errors in server architecture is via the NMI. The S450NX MP Server emulates non-ISA errors as ISA-compatible using NMI and SMI_L.

Three error handlers are required: BIOS NMI handler, Operating System NMI handler, and SMI handler. The SMI has the highest priority to process the errors and is OS-transparent. The OS NMI handler can process all errors, even when the SMI is disabled. In this case, some errors are SMI resources which can be routed to the NMI. The BIOS NMI handler processes the ISA-compatible errors and disables the NMI only.

Enabling and disabling SMI_L sources is done by the PID.

3.5   Hardware Initialization and Configuration

This section describes the following:
- System initialization
- Programming considerations for various portions of the I/O system

3.5.1 System Initialization Sequence

A Pentium II® Xeon™ Processor system based on the Intel 82450NX PCIset is initialized and configured in the following manner.

1. System power is applied. The power supply initiates the reset sequence using the PWR_GD_PS signal. PCI reset (RST_P_RST_L) is asserted to tristate the PCI bus in order to prevent PCI output buffers from short circuiting when the PCI power rails are not within the specified tolerances. The Intel 82450NX PCIset asserts CPURST_L to reset the processor(s).

2. The Intel 82450NX PCIset is initialized with its internal registers set to default values.

3. Before CPURST_L is deasserted, the Intel 82450NX PCIset asserts BREQ0_L. Processor(s) in the system determine which host bus agents there are, Agent 0 or Agent 1, according to whether their BREQ0_L or BREQ1_L is asserted. This determines bus arbitration priority and order.

4. The processor(s) in the system determines which processor will be the Bootstrap Processor (BSP) by issuing Bootstrap Interprocessor Interrupts (BIPI) on the APIC data bus. The non-BSP processor becomes an application processor and idles, waiting for a Startup Interprocessor Interrupt (SIPI).

5. The BSP begins by fetching the first instruction from the reset vector.

6. DRAM is sized and initialized, Intel 82450NX PCIset registers are updated to reflect memory configuration.

7. All PCI and ISA I/O sub-systems are initialized and prepared for booting.

3.6   Server Management Programming Interface

Communication between BIOS and the Board Management Controller (BMC) is done using the ISA bus. After the BMC has started the power initialization sequence, BIOS can access BMC resources and records.

3.7   PCI Interrupt to IRQ Routing Control

The PID controls routing of interrupts from the IRQs, PCI buses and PXB expansion and is configured by BIOS. The PID also controls routing of SMI and NMI sources.
Refer to "Interrupts and the PID" in chapter 1, section 1.13 for more information.

4. BIOS, Setup and SSU

4.1   BIOS Overview

BIOS, as used in the context of this document, refers to the system BIOS, BIOS setup and option ROMs for onboard peripheral devices that are contained in the system flash. System BIOS controls basic system functionality using stored configuration values. BIOS setup refers to Flash ROM-resident setup utility that provides user control of configuration values stored in battery-backed CMOS configuration RAM. The System Setup Utility (SSU) has replaced the SCU. BIOS setup is closely tied with the system BIOS and is considered a part of BIOS. The Flash Memory Update utility (IFLASH) loads predefined areas of Flash ROM with setup, BIOS, and other code/data. Configuration utility (CU) is used to refer to both BIOS setup and SSU.

The following figure shows the relationship between BIOS components and register spaces. Unshaded areas are loaded into Flash using IFLASH.
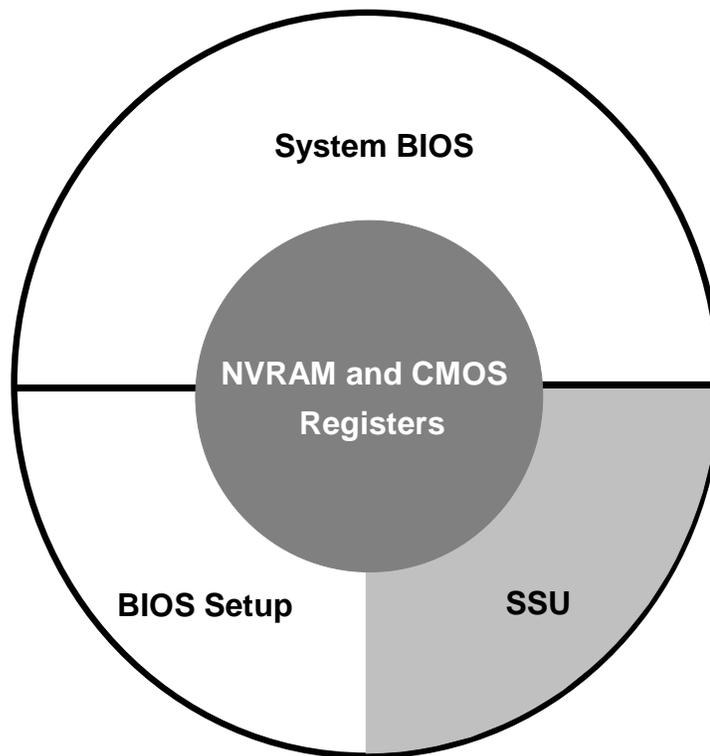
Figure 4.1: S450NX MP Server BIOS Architecture

4.2   System BIOS

The system BIOS is the core of the Flash ROM-resident portion of the BIOS. The system BIOS provides standard Server BIOS services and support for some new industry standards, such as I_2O, ACPI, and Wired For Management. In addition, the system BIOS supports certain features that are common across all the Intel Servers. These include security, MP specification support, server management and error handling, CMOS configuration RAM management, OEM customization, PCI and PnP BIOS interface, console redirection and resource allocation support. BIOS setup is embedded in Flash ROM and provides the means to configure onboard hardware devices and add-in cards.

The BIOS Setup and System Setup Utility (SSU) are discussed in detail in the S450NX MP Server Product Guide.

4.3   Revision History Format

The BIOS Revision Identification is used to track board, OEM, and build revision information for any given BIOS. This identifier can be a maximum of 32 characters. The first 28 characters have been defined using the following format:

The figure below illustrates a standard 32-byte BIOS ID.

BoardID&BoardRev.OEMID.BuildID.BuildType.Date&Time

Four byte:
HHMM

Six byte:
YYMMDD

One to three byte:
   D = development
   A = alpha
   B = beta
   Pxx = production

Four byte:
Increment
on each build

Three byte:
   86B = Intel ESG,

One byte:
start with zero

Six byte ID:
S450NX
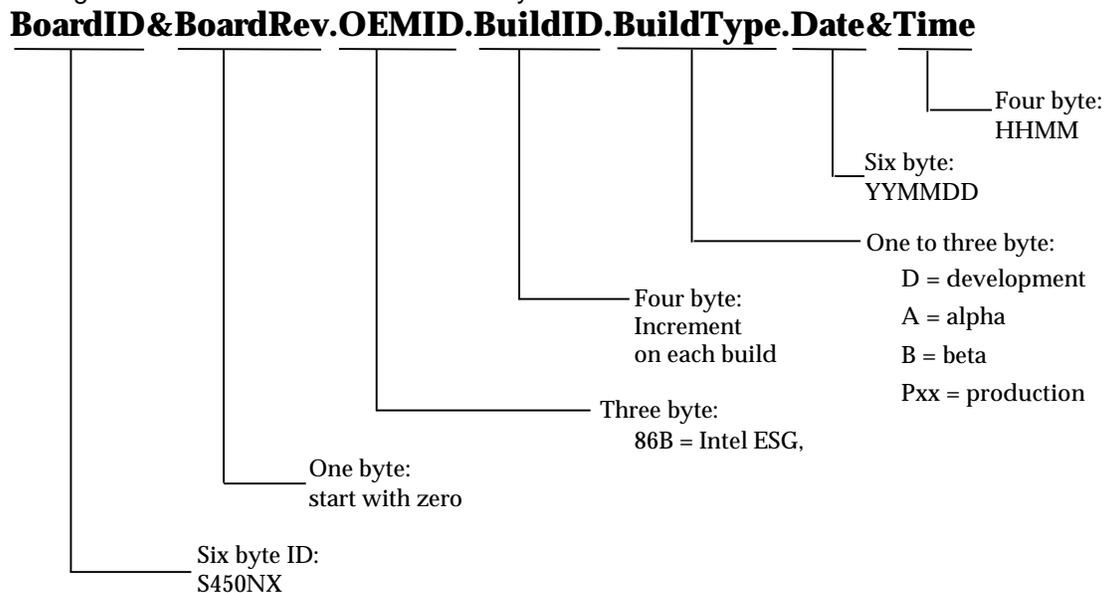
Figure 4.2: Standard 32-byte BIOS ID

5. Board Set Specifications

This chapter specifies the operational parameters and physical characteristics for S450NX. This is a board-level specification only. System specifications are beyond the scope of this document.

5.1   Absolute Maximum Ratings

Operation of the S450NX MP Server at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 5.1: Absolute Maximum Conditions

Operating Temperature	0°C to +55°C *
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V **
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V
12V Supply Voltage with Respect to ground	-0.3 to +12.6V
-12V Supply Voltage with Respect to ground	-13.2 to +0.3V

- *Chassis design must provide proper airflow to avoid exceeding Pentium II® Xeon™ Slot 2 maximum case temperature.
- ** V_{DD} means supply voltage for the device.

Further topics in this chapter specify normal operating conditions for the S450NX MP Server.

5.2   Electrical Specifications

DC specifications for the S450NX MP Server power connectors and module power budgets are summarized here. Electrical characteristics for major connector interfaces (including DC and AC specifications) can be obtained from other documents:
- PCI Connectors -- *PCI Local Bus Specification Rev. 2.1*
- ISA slots -- *EISA Bus Specification*

5.2.1 Power Connection

Main power supply connection is obtained using 2 - 20-pin connectors which attach to the power supply via 16 AWG wire of the colors shown in the table below. The 20-pin connector reference designators are J9B1 (Primary PROCs 1&2) and J9D2 (Secondary PROCs 3&4).

Table 5.2: 20-pin Main Power Connectors Pin-out

Pin	Signal	Color	Pin	Signal	Color
1	+3.3 Vdc	Orange	11	+3.3 Vdc	Orange
2	+3.3 Vdc	Orange	12	+3.3 Vdc	Orange
3	+3.3 Vdc	Orange	13	+3.3 Vdc	Orange
4	COM	Black	14	COM	Black
5	COM	Black	15	COM	Black
6	COM	Black	16	COM	Black
7	COM	Black	17	+5V Standby	Purple
8	+12 Vdc	Yellow	18	+5 Vdc	Red
9	+12 Vdc	Yellow	19	+5 Vdc	Red
10	+12 Vdc	Yellow	20	+5 Vdc	Red

There is also a 14-pin auxiliary power connector which handles the power supply voltage sense lines, the server management bus, and power good signals. It is connected to the power supply via a ribbon cable. Its reference designator is J9E4.

Table 5.3: 14-Pin Auxiliary Power Connector Pin-out

Pin	Signal	Pin	Signal
1	COM	2	+5V Sense
3	+3.3V Sense	4	Fan Speed Ctrl
5	IPMB Clock 5V	6	IPMB Data 5V
7	COM	8	Power Good
9	Power On	10	COM
11	-12 Vdc	12	*[Keying Pin]*
13	+12V Sense	14	COM

5.2.2 Power Consumption

The following table shows the power consumed on each supply line for a S450NX MP Server baseboard with 4 processors, 16 DIMMs, and 7 PCI slots or 6 PCI slots and 1 ISA slot load.

NOTE:

The following numbers are provided as an example. Actual power consumption will vary depending on the exact S450NX MP Server configuration.

Table 5.4: S450NX MP Server Power Consumption

Device(s)	3.3V	+5V	Combined 3.3 and 5V	+12V1 (primary)	+12V (secondary)	-12V	5VSB	total
Processors				10.3	10.3			
Memory	17.85							
GTL		3						
Baseboard	6.04	2.34		0.07		0.4	0.96	
Fans		9.67						
Keyboard		0.25						
PCI / ISA slots	31.82	21		1.5				
Power Share				0.75			0.04	
Total Current	55.71	36.26		11.87	10.3	0.4	0.96	115.5
Total Power	183.843	181.3	260.143	142.44	123.6	4.8	4.8	795.92
Power Sub-system	231	230	373.4	216	192	12	15	800
Board Power	183.843	181.3	260.143	142.44	123.6	4.8	4.8	535.783
Power Available	47.157	48.7	113.257	73.56	68.4	7.2	10.2	368.474

Power on combined 3.3V and 5V channels shall not exceed: 373.4

5.2.3 Power Supply Specifications

This section provides power supply design guidelines for a S450NX MP Server based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 5.5: S450NX MP Server Power Supply Voltage Specification

PARAMETER	Min	Nom	Max	Units	Tolerance
+3.3V	+3.135	+3.30	+3.465	V	± 5%
+5V	+4.75	+5.00	+5.25	V	± 5%
+12V	+11.40	+12.00	+12.60	V	± 5%
-12V	-10.80	-12.00	-13.20	V	± 10%
+5Vstdby	+4.75	+5.00	+5.25	V	± 5%

Table 5.6: Transient and Remote Sense/Sink Currents

Item	Min	Nom	Max	Units
Transient Currents				
di/dt				
3.3V			0.5	A/μsec.
5V			0.5	A/μsec.
12V			0.5	A/μsec.
Step Amplitude				
3.3V	22			A
5V	8			A
12V	5			A
Remote Sense				
trace resistance				
3.3V		0.659		ohms
5V		1.25		ohms
12V		0.407		ohms
Sink Current Off Voltage				
3.3V		0.007		V
5V		0.113		V
12V		0.061		V

Table 5.7: Ramp Rate / Ramp Shape / Sequencing / Power Good & Power On Signals

Item	Min	Nom	Max	Units	Comments
Ramp Rate(On):					
5 Volts	5		70	ms	to within 10%
3.3 Volts	5		70	ms	to within 10%
+12 Volts	5		70	ms	to within 10%
-12 Volts	5		70	ms	to within 10%
-5 Volts	5		70	ms	to within 10%
5 Volts Standby	5		70	ms	to within 10%
Ramp "Shape"(On & Off):					monotonic
Sequencing:(with respect to 5 Volts)					
3.3 Volts	simultaneous				
+12 Volts	simultaneous				
5 Volts Standby	constant voltage				
Power Good Signal					
Vil			0.6	V	
Vih	3.5			V	
Iil	-1		1	μA	
Iih					
Timing requirements					
Power On Signal					
Vol			0.8	V	
Voh	3.5			V	
Iol	10			mA	
Ioh	1.5			mA	
Timing requirements					
etc.					

5.2.4 Voltage Recovery Timing Specifications

The power supply must conform to the following specifications for voltage recovery timing under load changes:

1. Voltage shall remain within +/- 5% of the nominal set voltage on the +5V, +12V and 3.3V outputs, and +/- 5% of the nominal set voltage on the -5V and -12V outputs, during instantaneous changes in +5V and +12V load up to 8 Amps, and +3.3V load steps of 5 Amps.
2. Voltage regulation limits shall be maintained over the entire AC input range and any steady state temperature and operating conditions specified.
3. Voltages shall be stable as determined by bode plot and transient response. The combined error of peak overshoot, set point, regulation, and undershoot voltage shall be less than or equal to +/-5% of the output voltage setting. The transient response measurements shall be made with a load changing repetition rate of 50Hz to 5kHz. The load slew rate shall not be greater than 0.2A/μs.

5.2.5 Voltage Sequencing and Power Good Signal Characteristics

The following figures show the dynamic behavior of power signals when system power is switched on.
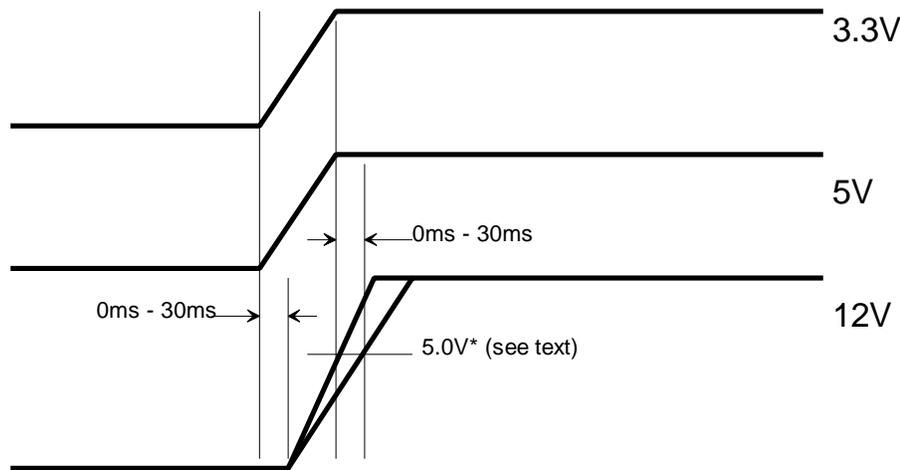
Figure 5.1: DC Voltage Sequencing

Note that the +3.3V and +5V supply voltages must begin their power-up ramp at the same time, and that +12V must start at the same time, or slightly after, the +5V supply. Additionally, the +12V must reach 5.0V at the same time, or slightly after, the +5V supply reaches 5.0V. All supply voltages must have a monotonic ramp up.
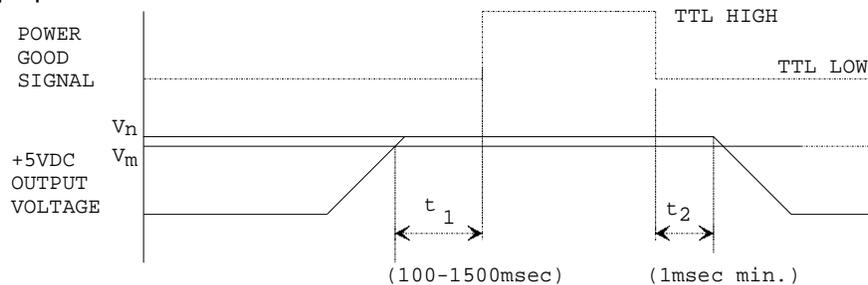
V_n Nominal Output Voltage +5 VDC
V_m Minimum Output Voltage +4.75 VDC
t1 Delay Turn-on (100-1500msec)
t2 Delay Turn-off(1msec min)

Figure 5.2: Power Good Signal Characteristics

5.2.6 Ripple Voltage

Ripple voltage was measured from 10Hz to 30MHz.

Table 5.8: Ripple Voltage Measurements

Voltage	Ripple Voltage Measurement (peak to peak)
+3.3V	1.5%
+5V	1.0%
+12V	1.0%
-12V	1.0%
+24V	1.0%
+5V STDBY	1.0%

5.3　Mechanical Specifications

The following diagrams show the mechanical specifications of the S450NX MP Server baseboard. All dimensions are given in inches, as per ANSI Y15.4M. Maximum primary-side component height is .550" unless otherwise noted. Connectors are dimensioned to pin 1. Refer to "Connector Specifications" after the diagrams for more information.

Figure 5.3: Baseboard Mechanical Diagram

Table 5.9: Baseboard Connectors

1	ISA Conn.	6	Serial A	11	PS Ctrl Conn.	16	Floppy Conn.
2	PCI Conn.	7	Parallel Conn.	12	Main Power Conn.	17	IDE Conn.
3	NIC Conn.	8	Secondary Proc.	13	Front Panel Conn.	18	Wide SCSI Conn.
4	Serial B	9	SDRAM DIMM	14	ITP Conn.	19	SMM Conn.
5	VGA Conn.	10	KeyB/Mouse	15	Battery	20	ATX Power Conn.

5.3.1 Connector Specifications

The following table shows the quantity and manufacturer part numbers for connectors on the baseboard.
Item numbers reference the circled numbers on the mechanical drawing. Refer to manufacturers'
documentation for more information on connector mechanical specifications.

Table 5.10: Baseboard Connector Specifications

Item	Qty.	Mfr(s). and Part #	Description
1	4	Molex 71109-5005	330-pin Slot 2 Processor connector
2	7	AMP 176139-2	98-pin ISA bus add-in card connector
3	1	AMP 646255-1	120-pin PCI add-in card connector
4	1	Molex 71796-0005	242-pin Memory card connectors
5	1	Molex 87256-3456	34-pin Floppy connector
6	1	Fox Conn 87256-4056	40-pin IDE connector
7	1	Molex 702-47-5001	50-pin Narrow SCSI connector
8	1	Molex 87256-30	30-pin Front panel connector
9	1	Foxconn/HonHai QA01343-P4	68-pin straight SCSI connector
10	6	BERG 95798-001	40-pin VRM Sockets
11	1	Foxconn/Hon Hai DM11396-68	15-pin VGA Video / 25-pin Parallel port connector
12	1	AMP 787904-1	Dual 9 Pin D-sub Serial port connector
13	1	Fox Conn MH11062-D2	Keyboard and mouse conn.
14	1	Fox Conn/Hon Hai	4-pin Single USB connector
15	2	Molex 39-29-9202	20-pin Power connector
16	1	AMP 111950-2	14-pin Auxiliary Power connector (pin 12 removed)
17	1	AMP 111970-6	26-pin Server Monitor Module feature conn.
18	1	Honda PCS-68LFDK	68-pin right angle SCSI connector
19	N/A	Not used	N/A
20	1	FoxConn ESO 03006	6-pin ICMB connector
21	1	AMP 104068-3	30-pin ITP conn.
22	1	AMP 1-146218-2	11-pin Jumper Header
23	2	AMP 104450-3	4-pin SIP header (Internal USB, HD Activity)
24	1	AMP 147015-1	4-pin Speaker conn.
25	1	Foxconn HB1903G	3-pin Write Protect for BMC Flush
26	2	Molex 22-44-7031	3-pin External IPMB and SMBus Expansion
27	1	FoxConn HF57030-C1	3-pin External WOL Connection

5.3.2 PCI and ISA Connectors

The baseboard PCI and ISA connectors adhere to the requirements in the *PCI 2.1 Local Bus
Specification* and *ISA Specification*. Refer to these documents for connector specifications.

5.4　Mean Time between Failures (MTBF) Data

5.4.1　S450NX MP Server Baseboard MTBF

The S450NX MP Server baseboard Mean Time between Failures (MTBF) data is calculated from predicted Failure in Time (FIT) data. The MTBF of the S450NX MP Server baseboard is calculated as 117,241 hours.

5.4.2　SC450NX MP Server System MTBF

The SC450NX MP Server System (S450NX MP Server baseboard with Cabrillo chassis) Mean Time between Failures (MTBF) data is calculated from predicted Failure in Time (FIT) data. The MTBF of the SC450NX MP Server system is calculated as 18,804 hours.

6. Power Share Backplane

6.1   Features

- Distributed load among 1, 2 or 3 power supplies (Power Share)
- Management Features:
    - IPMB bus
        - Report currents on all supplies and outputs.
        - Report fan pre-fail.
        - Current usage report.
        - Number of supplies installed.
        - Redundant mode determination.
        - Report FRU information from individual power supplies.
        - Report FRU information from the Power Share Board.
- Clustering Support

6.2   Electrical Connections

Interfacing is provided by the following connectors: power supply, baseboard power, baseboard auxiliary, and peripherals.

6.2.1 Power Supply

Table 6.1: Power Supply Connector Pin-out

PIN	SIGNAL	PIN	SIGNAL
1	GND	21	GND
2	GND	22	GND
3	GND	23	GND
4	GND	24	GND
5	5VCC	25	GND
6	5VCC	26	5VCC
7	3.3VCC	27	5VCC
8	3.3VCC	28	3.3VCC
9	3.3VCC	29	3.3VCC
10	12VCC	30	3.3VCC
11	12VCC	31	12VCC
12	12VCC	32	12VCC
13	NC	33	NC
14	24VCC	34	3.3_RS
15	-12VCC	35	RTN_RS
16	NC	36	5V_RS
17	PS_ON	37	12V_RS
18	P_GOOD	38	VCC_STDBY
19	GND	39	FAN_SEN
20	IPMBSDA	40	12CSCL

The Power Supply connectors, J1A1, J4A1, and J7A1, subscribe to the above format. More information about these signals can be found in the Power Supply Specification (Document order number 681374-002).

6.2.2 Baseboard Power

Table 6.2: Baseboard Power Connector Pin-out

PIN	SIGNAL	PIN	SIGNAL
1	3.3VCC	11	3.3VCC
2	3.3VCC	12	3.3VCC
3	3.3VCC	13	3.3VCC
4	GND	14	GND
5	GND	15	GND
6	GND	16	GND
7	GND	17	VCC_SDTBY
8	12VCC	18	5VCC
9	12VCC	19	5VCC
10	12VCC	20	5VCC

The Baseboard Power connectors, J5G1 and J8G1, subscribe to the above format and are labeled PRIMARY and SECONDARY.

6.2.3 Baseboard Auxiliary

Table 6.3: Baseboard Auxiliary Connector Pin-out

PIN	SIGNAL	PIN	SIGNAL
1	RTN_RS	2	5V_RS
3	3.3V_RS	4	FAN_SPEED
5	IPMBSCL	6	IPMBSDA
7	GND	8	SYS_PGOOD
9	PS_ON	10	GND
11	-12VCC	12	KEY
13	12V_RS	14	GND

The Baseboard Auxillary connector, J7G1, subscribes to the above format.

6.2.4 Peripherals

Table 6.4: Peripheral Connector Pin-out

PIN	SIGNAL	PIN	SIGNAL
1	GND	8	FAN_V
2	5VCC	9	12VCC
3	GND	10	GND
4	5VCC	11	12VCC
5	GND	12	GND
6	5VCC	13	12VCC
7	GND	14	GND

The Peripherals connector, J7G1, subscribes to the above format. Another high current connection to provide power to system peripherals. The 5VCC is monitored separately from the baseboard 5VCC. This allows current monitoring to check for 240VA violations.

6.3 Power Supplies and Sharing Circuits

The Cabrillo Power Share Backplane is designed to provide a reliable redundant power system for power hungry servers. This backplane can be used with one, two or three power supplies, providing power to the baseboard and peripherals. The load current will be balanced between the supplies. If there are three supplies, you will have redundant power and the unit will remain functional if one supply fails.

6.4 Clustering Support

Inexpensive clustering is supported through the use of the baseboard power switch. The peripherals can remain powered while the baseboard is disengaged from the power system. This switch is controlled through a microcontroller IPMB bus command. Each power form is handled in a slightly different way, providing an optimal power sharing solution for the Cabrillo chassis.

The following table describes the current capabilities of each power form.

Table 6.5: Power Form Current Capabilities

Form	Tolerance	Max. Current	Min. Current
+3.3V	+5/-4%	70	0.5
+5V	+5/-4%	46	0.8
+5V_stdby	+5/-4%	3	0
+12V	+5/-4%	34	0.53
-12V	±10%	1	0

6.4.1 3.3V Power Form

This is the easiest of the load sharing voltages. The current is monitored going into the PSB and the total output is monitored before going through the baseboard power switch.

6.4.2 VCC_STDBY Power Form

This provides current for running the server management system. VCC_SDTBY is available when any power supply is plugged into the AC power. This is the only power going to the baseboard that is not switched by the baseboard switch.

6.4.3 5V Power Form

This current is monitored as it enters from each supply and is then monitored going to the peripheral circuits. The current going to the baseboard is calculated by subtracting the peripheral current from the total.

6.4.4 12V Power Form

Three separate circuits are provided for +12V power. This allows monitoring for UL 240VA violations, while providing full power. There are two circuits going to the baseboard and one going to the peripherals. The peripheral circuit current can be calculated by subtracting the total baseboard current from the total incoming current. Two monitoring circuits are provided after the baseboard power switch for this purpose.

6.4.5 -12V Power Form

This low current negative voltage is provided from any and all supplies in the system through a simple "diode OR-ing" solution. This supply is also provided with a baseboard power switch. This voltage is provided through the baseboard auxiliary connector.

6.4.6 Micro-controller

The load sharing is accomplished through analog circuitry. The digital section is there only to communicate the status of the PSB. This includes the transmission of FRU information for both the supplies and the PSB itself and the analog currents that the power system is supplying. The control for the supplies actually lies with the baseboard management controller (BMC). All the PSC does is report the information and act upon the control commands from the BMC. The only PSC output controls the baseboard power switch.

7. LVD/SE SCSI Backplane

7.1 Overview

The backplane is an LVD/SE SCSI design which provides support for new SCSI devices using Low Voltage Differential Signaling (Ultra 2) as well as older SE SCSI devices (Ultra and older). The single backplane has a single SCSI channel with a SAF-TE controller and microcontroller. The backplane supports hot swapping SCA-2 style drives when mounted in the docking drive carrier. The backplane uses the SCA-2 PressFit connector.

7.2 Functional Description

The following figure shows the functional blocks of the LVD/SE SCSI Backplane. The function of the other SCSI channel is the same. An overview of each block follows.
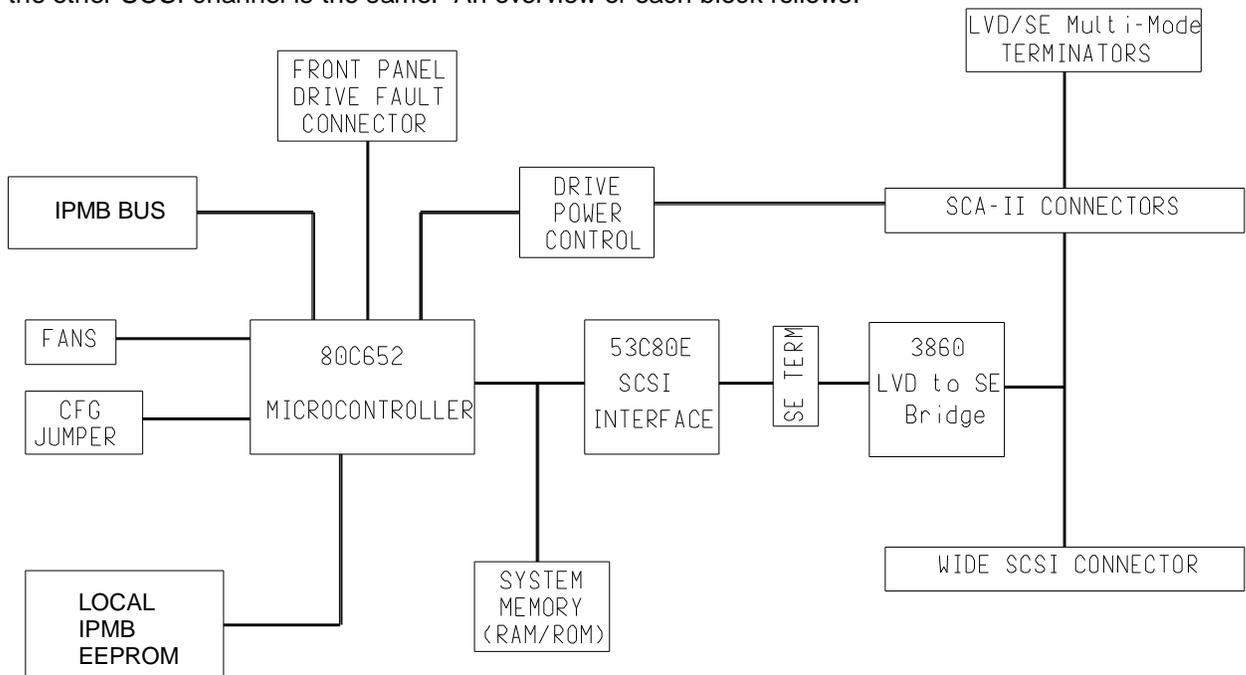
Figure 7.1: Functional Block Diagram

7.2.1 Wide SCSI Connector
SCSI input from Host SCSI Controller (baseboard or RAID card).

7.2.2 SCA-2 Connectors
The SC450NX MP Server LVD/SE SCSI backplane provides 6 SCA-2 PressFit connectors, which provide power and SCSI signals using a single connector. Each connector has control signals that enable the backplane to provide SCSI ID assignments as well as drive motor spin-up configuration. Each SCSI drive attaches to the backplane using one of these connectors.

7.2.3 SCSI Multi-Mode Termination

The Multi-Mode terminators provide SCSI-3 SPI-2 compliant termination for the backplane. These terminators provide termination in SE modes as well as LVD mode.

7.2.4 SCSI Interface

The SCSI interface on the SC450NX MP Server LVD/SE SCSI backplane provides the link between the SCSI bus and the microcontroller (containing the intelligence for the SC450NX MP Server LVD/SE SCSI backplane). This interface allows the microcontroller to respond as a SCSI target to implement the SAF-TE protocol. This is implemented using a Symbios logic 53C80S SCSI Interface Controller (or equivalent).

7.2.5 Power Control

Power control on the SC450NX MP Server LVD/SE SCSI backplane supports the following features:

Spin-down of a drive when failure is detected and reported (using enclosure services messages) via the SCSI bus. An application or RAID controller detects a drive related problem that indicates a data risk. In response it takes the drive out of service and sends a spin down SCSI command to the drive. This decreases the likelihood that the drive is damaged during removal from the hot-swap drive bay. When a new drive is inserted, the power control waits a small amount of time for the drive to be fully seated, and then applies power with a controlled power ramp.

If system power is on, the LVD/SE SCSI backplane immediately powers off a drive slot when it detects that a drive has been removed. This prevents possible damage to the drive when it is partially removed and re-inserted while full power is available and disruption of the entire SCSI array from possible sags in supply voltage and resultant current spikes.

7.2.6 FET short protection

The FET short protection circuit is useful to protect both 12 volt and 5 volt power control FETs located on LVD/SE SCSI backplane.

7.2.7 Microcontroller

The microcontroller provides all the intelligence for the LVD/SE SCSI backplane. It is an 80C652 microcontroller, with a built-in IPMB interface. The 80C652 microcontroller uses Flash for program code storage and Static RAM for program variables and buffers.

7.2.8 Hard Drive Fault LED

The Hot-Swap controller is responsible for turning the drive fault LEDs on or off according to the states specified via commands received via SAF-TE and the IPMB. The drive fault LEDs are yellow and serve to indicate failure status for each drive. The LEDs are physically located on the LVD/SE SCSI backplane and are driven from the backplane. During initialization, the microcontroller flashes the LEDs for two seconds to signal POST completion is successful.

7.2.9 IPMB (IPMB bus)

The IPMB bus is a system-wide server management bus. It provides a way for various system components to communicate independently of the standard system interfaces (e.g., PCI bus or processor/memory bus). The IPMB bus controller is integrated into the microcontroller.

7.2.10 Fan

The LVD/SE SCSI backplane supports up to 9 tachometer fans with a digital output that can be used by the microcontroller to assess the fans' operating condition before total failure (which may result in collateral hardware damage). The fans' digital outputs are connected via two multiplexers to the input of each microcontroller. Six fans are connected to the primary microcontroller and three fans to the secondary microcontroller. The microcontroller is responsible for monitoring the fans' speed (fan speed is directly controlled from backplane), and reporting of fans' condition via IPMB bus. It is the responsibility of the HSC to report fan speed. The speed of the fans is sensed by the HSC and compared against a 'low speed' threshold. The HSC issues a message on the IPMB when the fan speed falls below this threshold. Once a fan is dead it should be replaced, since the backplane does not detect second fan failure.

7.2.11 Serial EEPROM

The AT24C02N provides 256 bytes of non-volatile storage. This is used to hold the serial number, part number, and other FRU inventory information and miscellaneous application code used by firmware about the SC450NX MP Server LVD/SE SCSI backplane.

7.3   Board Functions

7.3.1 Microcontroller

The Philips P80C652FBB microcontroller operates at 12MHz and is a derivative of the 80C51 8-bit CMOS microcontroller.

7.3.2 SCSI Controller

The SYM53C80S controller is an 8-bit low performance part chosen for its low cost. Device selection is memory mapped at address FB00-FC00. It is reset on power-up and when reset is asserted to the backplane. The SYM53C80S controller access slows down the bus, it is recommended to query SAF-TE infrequently. SAF_TE command processing is 2-10ms.

7.3.3 Multi-Mode SCSI Termination

The SCSI-2 and SCSI-3 standards recommend the use of active termination at both ends of every cable segment in a SCSI system with single-ended drivers and receivers. Three Dallas DS21S07AE devices are used for active termination of the wide SCSI bus in each channel.

7.4   Memory Map

The following figure shows the memory map viewed from the perspective of the microcontroller. Description of each memory block are provided, showing their purpose and function as determined by microcontroller programming. These functions may also be controlled by system software using SCSI commands defined in the SAF-TE specification.

|		
256B	FAN MUX REGISTER ACCESS REGION	FE00h - FEFFh
256B	DIAGNOSTIC TRIGGER ACCESS REGION	FD00h - FDFFh
256B	SCSI DACK ACCESS REGION	FC00h - FCFFh
256B	SCSI TARGET ACCESS REGION	FB00h - FBFFh
256B	DRIVE PRESENCE REGION	FA00h - FAFFh
256B	DRIVE POWER ENABLE REGION	F900h - F9FFh
256B	DRIVE FAULT STATUS REGION	F800h - F8FFh
		F7FFh
32 KB	STATIC RAM REGION	
		8000h
		7FFFh
32 KB	FLASH MEMORY REGION	
		1000h
	BOOT BLOCK	0000h - 0FFFh

Figure 7.2: Microcontroller Memory map

7.4.1 Flash Memory Region (0x0000 - 0x7FFF)

The Atmel 27C257 device or equivalent Flash EPROM is accessible as either a Data or Program Memory read. Writes to flash are also allowed in order to support field-upgradeable code. The lower 4KB (0x0000 - 0x0fff) are not writable unless the boot block write protect jumper is moved.

7.4.2 Static RAM Region (0x8000 - 0xF7FF)

The static RAM is accessible as either Data or Program accesses. It is possible to load executable code into the Static RAM and execute directly from RAM.

7.4.3 Memory Mapped Registers (0xF800 - 0xFFFF)

The upper 2KB of the controller address space are mapped to eight regions of 256 bytes for memory-mapped registers and miscellaneous functions. For each of the regions listed, the actual function occupies less than the full 256 bytes of its address decode. Unless specifically stated, each region is a single address. Thus, aliases will occur on byte boundaries throughout the remainder of the region decoded for that function. Note that the eighth region from 0xFF00 - 0xFFFF is not used.

In register bit descriptions listed below, five fields are shown: the data bit number(s), the name of the field, how the bit(s) respond to a reset, whether the bits are readable and/or writable, and a description of the field. RO indicates read-only, WO indicates write-only, and RW indicates readable and writable. Any fields that are marked as reserved should be ignored when read, and should be set to zero when written.

7.4.4 Drive Fault Status Region (0xF800 - 0xF8FF)

The drive fault LEDs are controlled by this register. Writing a '1' to a bit turns the corresponding LED on. Reading the register returns the current state of the LEDs. A warm or cold reset clears all register bits to zero. The upper two bits are undefined.

Table 7.1: Drive Fault Status Byte Format

Bit(s)	Name	Reset Action	R/W	Description
7:6	Reserved	N/A	N/A	Reserved bits.
5::0	FLT[5::0]	Clear	RW	Drive fault LED enable. 0=LED off, 1=LED on. Bit 0 corresponds to drive ID 0.

7.4.5 Drive Power Enable Region (0xF900 - 0xF9FF)

Power is applied to a drive when its corresponding power-enable bit is set to '1' in this register. Following a cold reset, each drive that is present will have its power-enable bit turned on. A warm reset has no effect on this register.

Table 7.2: Drive Power Enable Byte Format

Bit(s)	Name	Reset Action	R/W	Description
7:6	Reserved	N/A	N/A	Reserved bits.
5::0	DRVPWR[5::0]	(see text)	RW	Drive power enable. 0=power off, 1=power on. Bit 0 corresponds to drive ID 0.

7.4.6 Drive Present Status Region (0xFA00 - 0xFAFF)

The absence or presence of each drive is detected by the state of pin 44 on that drive's SCA connector. A drive that is present will have its corresponding bit set to '1' in this register.

Table 7.3: Drive Present Status Byte Format

Bit(s)	Name	Reset Action	R/W	Description
7:6	Reserved	N/A	N/A	Reserved bits.

| 5::0 | DRVPRES[5::0] | N/A | | RO | Drive present sense. 0=drive absent, 1=drive present. Bit 0 corresponds to drive ID 0. |

7.4.7 SCSI Target Access Region (0xFB00 - 0xFBFF)

The Symbios 53C80 SCSI target appears to the controller as a set of eight registers at sequential addresses. For details, refer to the Symbios SYM53C80E/S Data Manual.

7.4.8 SCSI DACK Access Region (0xFC00 - 0xFCFF)

When the SCSI target is in DMA mode, data bytes may be read from or written to the 53C80S by reading or writing the DACK access region. This asserts the DACK_L input of the 53C80S instead of the CS_L input.

7.4.9 Diagnostic Trigger Access Region (0xFD00 - 0xFDFF)

A hole pattern exists on each channel of the backplane for a scope or logic-analyzer trigger and ground. When a write access is done to this address region, a positive pulse is generated on the trigger pin.

7.4.10 Fan Mux Register Access Region (0xFE00 - 0xFEFF)

Several miscellaneous control and status bits exist in this register as shown in the table below.

Table 7.4: Fan Mux Register Byte Format

Bit(s)	Name	Reset Action	R/W	Description
7	Reserved	N/A		Reserved bit.
6	FAN12V_L	Set	RW	Set the fan-voltage control signal to the BMC to run the fans at a higher voltage. 0=fans at 12V, 1=fans at 10V. This signal from the primary and secondary controllers are wire-ORed such that if either controller writes a 0 to this bit, the signal going to the BMC goes low.
5	Reserved	N/A		Reserved bit.
4	SEC_PRI_L	N/A	RO	Reading this bit indicates whether this is the primary or secondary controller. 0=primary, 1=secondary.
3	FRC_UPD_L	N/A	RO	Reads the state of the Force Update jumper. 0=force update jumper installed, 1=force update jumper not installed.
2::0	MUX[2::0]	Clear	RW	Selects which fan tach sensor is multiplexed to the microcontroller T1 input. The primary controller has 6 fans, the secondary controller has 3. Out of range values for the MUX bits select the highest numbered fan for that channel.

7.5   I/O Ports

80C652 architecture provides 4 memory-mapped I/O ports: [P0:P3].

7.5.1 P0

Since the firmware for the microcontroller is located in a Flash memory device (for ease of debugging and for possible field-upgradeability), and all memory and memory-mapped I/O are located outside the microcontroller, P0 is used as a time-multiplexed low-order address and data bus. It is not used for general I/O purposes.

7.5.2 P1

P1 has two dedicated-function signals and six implementation-specific control signals, as shown in the following table.

Table 7.5: P1 Functions

Bit	Name	I/O	Fixed*	Function
7	SDA	I/O	Y	IPMB Serial Data signal for the IPMB.
6	SCL	I/O	Y	IPMB Serial clock signal for the IPMB.
5	Reserved	-	N	Reserved for future use.
4	SCSI _reset_L	O	N	Reset SCSI controller. If 0, places the 53C80S SCSI controller into reset. If 1, the SCSI interface controller comes out of reset and operates normally.
3	SCSI_DRQ	I	N	SCSI DMA Request. Connected to the DRQ signal of the 53C80S SCSI component. Allows the microcontroller to use the DMA transfer capabilities of the SCSI interface component, which results in higher performance.
2	Reserved	-	N	Reserved for future use.
1	SDA_Local	I/O	N	Serial Data for private IPMB connection to temperature sensor
0	SCL_Local	O	N	Serial Clock for private IPMB connection to temperature sensor

* "Fixed" indicates whether the function/pin is defined by the microcontroller pin-out (fixed) or implementation-specific (not fixed)

7.5.3 P2

P2 is the high-order address and data bus for external device access. It is not used for general I/O purposes.

7.5.4 P3

P3 provides 4 dedicated-function signals and 4 implementation-specific control signals, as shown in the following table.

Table 7.6: P3 Functions

| Bit	Name	I/O	Fixed*	Function
7	RD_L	O	Y	Read strobe. Indication from the microcontroller that the current bus cycle is a read operation.
6	WR_L	O	Y	Write strobe. Indication from the microcontroller that the current bus cycle is a write operation.
5	Fan	I	N	Fan tachometer input.
4	Reserved	-	N	Reserved for future use.
3	INT1_L	I	Y	Interrupt 1. Connected to the SCSI bus reset signal RST_L.
2	INT0_L	I	Y	Interrupt 0. Connected to the 53C80S SCSI component interrupt.
1	Reserved	-	N	Reserved for future use.
0	Reserved	-	N	Reserved for future use.

7.6   Mechanical Specifications
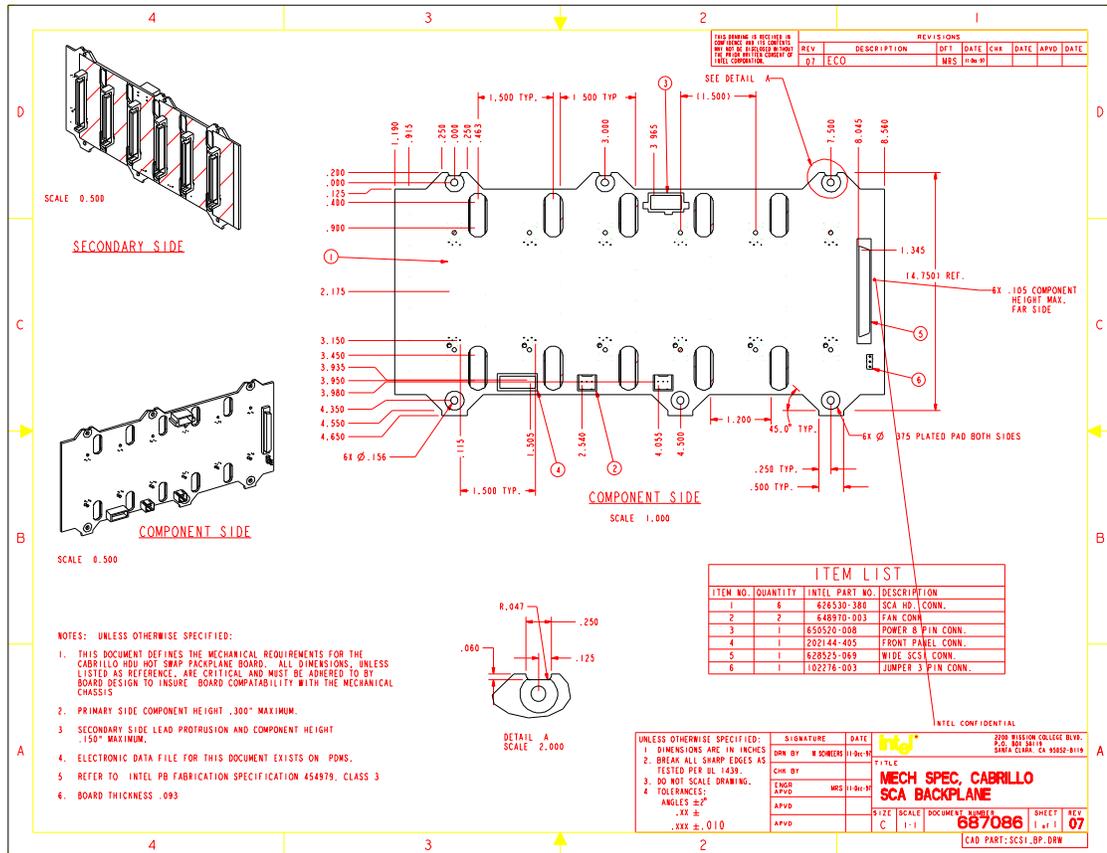
Figure 7.3: Mechanical drawing

8. Memory Module

8.1 Block Diagram

The figure below shows the main architectural features of the S450NX MP Server Memory Module.
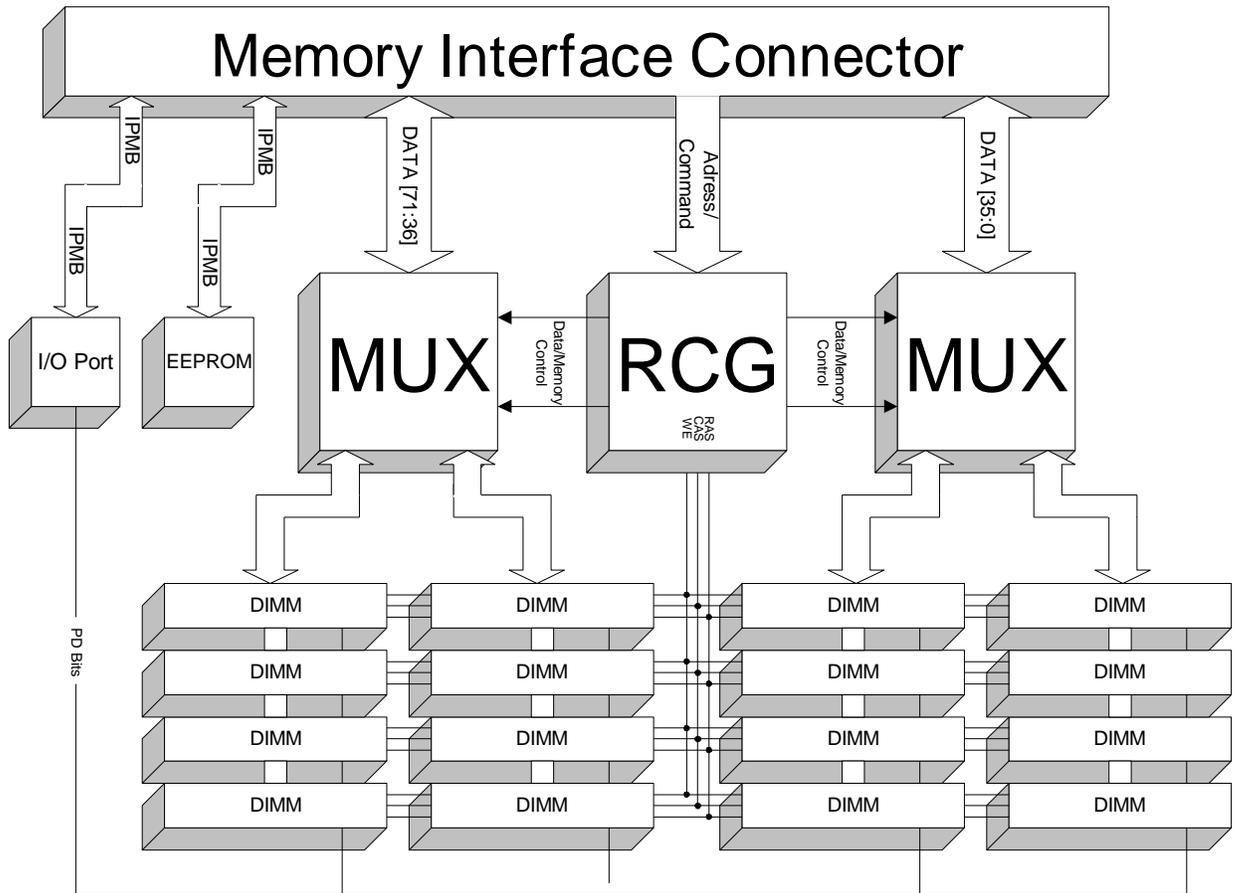

Figure 8.1: S450NX MP Server Memory Module Block Diagram

8.2   Overview

The memory module's main components are as follows:

- DRAM Array consisting of 16 DIMM sockets which accept 3.3V Buffered ECC DIMMs.
- One Intel 82450NX PCIset RAS-CAS Generator (RCG) which drives RAS, CAS, Address, and WE to the DRAM array.
- Two Intel 82450NX PCIset Data Path Multiplexers (MUXes) which drive and receive data to and from the DRAM array.

- Server Management support with onboard EEPROM plus accessibility of all Presence Detect (PD) and ID bits from all DIMMs. PD bits relate information regarding module configuration, page mode, and access timing. ID bits relate to the modules refresh control and data width.

8.3   EDO DRAM Array

The memory array on the S450NX MP Server memory module consists of 16 72-bit (64-bit data plus 8 ECC bits) DIMM sockets. These sockets are divided into four banks, of four sockets labeled A through D. These banks support 4:1 interleaving only. With 4:1 interleaving, all four DIMMs in the bank are populated and a single DRAM transaction is required to retrieve a full cache line. The four DIMMs are organized as follows, using the reference designators for a 4:1 interleaved Bank A as an example:

J1   Interleaves 0 and 1, Low Data (35:0)
J2   Interleaves 2 and 3, Low Data (35:0)
J3   Interleaves 0 and 1, High Data (71:36)
J4   Interleaves 2, and 3, High Data (71:36)

Each interleave provides access to 72 bits of data, thus 4:1 interleaving yields 288-bits (32 bytes) per transaction, which is one cache line for the Pentium II® Xeon™ processor. One Memory Module in a system can complete DRAM transactions at a maximum rate of once every 40 ns for a maximum data rate of 800 MB/s.

There are several different DIMMs available; table 8.1 shows which permutations of normal DIMM options can be used in the S450NX MP Server memory module.

Table 8.1: Memory Module DIMM Types

| Category	Supported DIMM Variety
Speed	50 ns, 60 ns
Capacity/ Organization/ Refresh	32 MB: 16Mbit, 4Mx4 DRAM;2K or 4K Refresh*
	64 MB: 64 Mbit, 8Mx8 DRAM; 4K Refresh*
	128 MB: 64 Mbit, 16Mx4 DRAM; 4K or 8K Refresh*
	256 MB: Double-high; 64 Mbit, 16Mx4 DRAM; 4K or 8K Refresh*
Voltage	3.3 V
Data Width	x72 (ECC)
Page Mode	EDO
Buffered/Non	Buffered
Maximum Height	2.1 inches
DRAM Package	TSSOP

* The S450NX MP Server memory module supports CAS-before-RAS refresh only.

When selecting a module, make sure that the target refresh number corresponds to CBR refresh.

All DIMMs within a given bank should be identical. From bank to bank, the Intel 82450NX PCIset supports different varieties of DIMM size, manufacturer, and speed, but only a limited subset will be validated at the system level. The validated configurations are still to be determined.

During POST, the BIOS should scan the presence detect bits of all DIMMs. If all DIMMs are found to contain 50-ns devices, then BIOS should change value of the DR50H# pin at the RCG. The default on this pin is a high voltage level, which corresponds to 60-ns timings; changing the value to a low voltage level will place the RCG in 50-ns mode. This signal is controlled by one of the 8-bit IPMB I/O ports on the memory module (see section 2.3, Table 2-4). A change of value on this pin must therefore be effected by software and must be done in a very controlled manner. After changing the value of the bit, BIOS will immediately perform a soft reset; no accesses to main memory can occur between the bit change and the reset. While changing this bit will not increase the maximum bandwidth, it will decrease initial latency of DRAM reads by one clock and will increase bandwidth of consecutive page misses.

If fewer than 16 DIMMs are installed, there is a preferred order for populating the DIMM sites to maintain optimal signal integrity. Supported DIMM configurations are shown in the following figures.
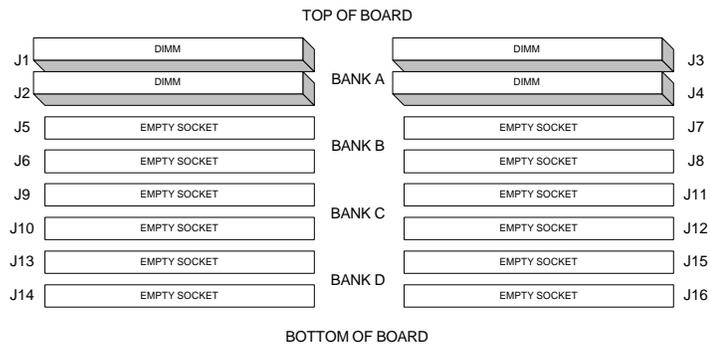

Figure 8.2: 4:1 Interleave with 4 DIMMS
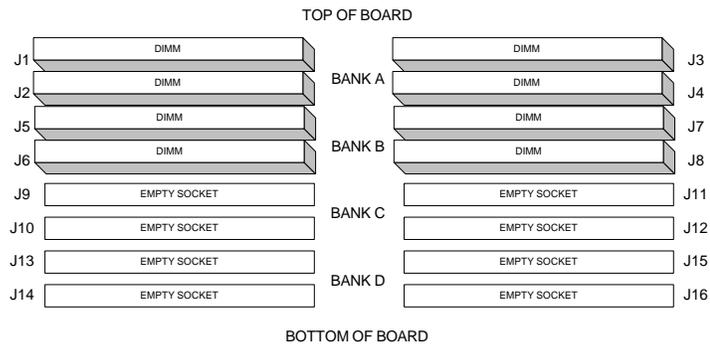
Figure 8.3: 4:1 Interleave with 8 DIMMS

J1	DIMM		DIMM	J3
J2	DIMM	BANK A	DIMM	J4
J5	DIMM		DIMM	J7
J6	DIMM	BANK B	DIMM	J8
J9	DIMM		DIMM	J11
J10	DIMM	BANK C	DIMM	J12
J13	DIMM		DIMM	J15
J14	DIMM	BANK D	DIMM	J16

BOTTOM OF BOARD
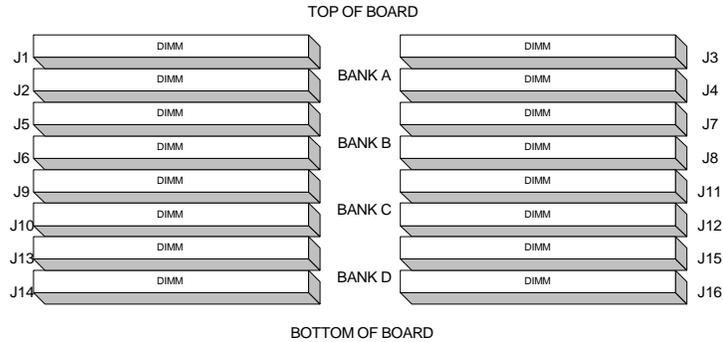
Figure 8.4: 4:1 Interleave with 16 DIMMS

TOP OF BOARD

| J1	DIMM		DIMM	J3
J2	DIMM	BANK A	DIMM	J4
J5	DIMM		DIMM	J7
J6	DIMM	BANK B	DIMM	J8
J9	DIMM		DIMM	J11
J10	DIMM	BANK C	DIMM	J12
J13	EMPTY SOCKET		EMPTY SOCKET	J15
J14	EMPTY SOCKET	BANK D	EMPTY SOCKET	J16

BOTTOM OF BOARD
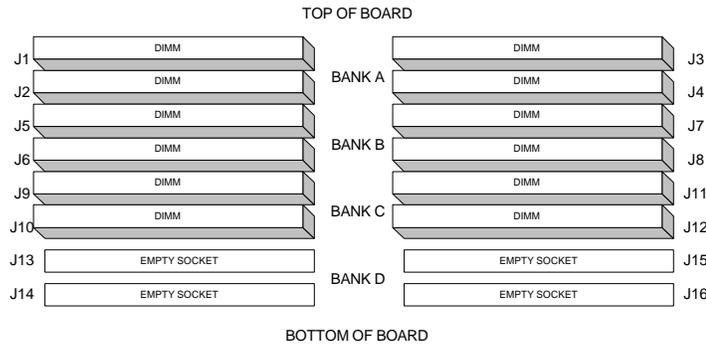
Figure 8.5: 4:1 Interleave with 12 DIMMS

With the memory module installed in a system, any combination of the above figures (8.2 through 8.5) should function correctly.

8.4   The Intel 82450NX PCIset

8.4.1 MUX

The purpose of the MUX is to provide the data path from the DRAM array to the MIOC. The MUX takes no action by itself but is controlled either by the MIOC or RCG. Each MUX contains four 36-bit data I/O paths (quad words) to the DRAM array and a single 36-bit data I/O path to the MIOC. The respective quad words from each MUX are combined for the full 72-bits required for the MD (Memory Data) bus. Quad word order is determined by the MIOC and sent via the DOFF[1:0]# signals to the MUX. The result is that the critical chunk is accessed first and the remaining chunks are accessed in Intel "toggle" order. The MUX acts not only as a multiplexer but also as a buffer. It takes in all 288-bits of data from the DRAM array and then multiplexes it out in four 72-bit bursts.

8.4.2 RCG

The RCG's primary purpose is to generate the signals to control accesses to the DRAM array. Once the data has been retrieved from the DRAM array the RCG is responsible for controlling the MUXes to get the data out onto the MD bus. The RCG responds to three types of requests from the MIOC: read, write, and refresh. Once one of these three commands has been received from the MIOC, the RCG will assert the appropriate DRAM control signals (RAS#, CAS#, Address and WE#) to carry out that transaction. Each RCG contains four RAS/CAS control units (RCCUs), each one is dedicated to one bank of DRAM. The RCG is also responsible for tracking requests from the MIOC and monitoring request completion via the CSTB#, RCMPLT#, and DCMPLT# signals.

8.4.3 System Management Interface

The S450NX MP Server memory module provides System Management software with information about DIMM configuration in addition to Field Replacement Unit (FRU) information about the memory module itself.

This data comes from three devices that reside on the IPMB bus. FRU data is provided by EEPROM connected to the IPMB bus. DIMM configuration data (presence, organization, size, speed, etc.) can be accessed via two 8-bit I/O Ports. The IPMB addresses of the three devices are listed in the table below.

Table 8.2: Memory Board IPMB Address Map

Device	IPMB Address
Board EEPROM	0xAA (Write)
I/O Port 0	0x70 (Write)
I/O Port 1	0x72 (Write)

The FRU data contained in the EEPROM consists of board serial number, part number, revision number, and other data as outlined in the following table.

Table 8.3: Memory Module EEPROM Byte Map

Address	Length	Description	Default Value
0x00	1	Common Header Format Version	0x01
0x01	1	Internal Use Area Offset (8-byte multiples)	0x01
0x02	1	Chassis Information Area Offset (8-byte multiples)	0x00 (area not present)
0x03	1	Board Information Area Offset (8-byte multiples)	0x0A
0x04	1	Product Information Area Offset (8-byte multiples)	0x00 (area not present)
0x05	2	Zero Padding	0x0000
0x07	1	Common Header Checksum	0xF4
0x08	72	Internal Use Area	
0x50	1	Board Information Area Format Version	0x01
0x51	1	Board Information Area Length (8-byte multiples)	0x08
0x52	1	Unicode Country Base	0x00
0x53	3	Manufacture Date/Time	
0x56	1	Board Manufacturer Type/Length Byte	0xC5
0x57	5	Board Manufacturer (ASCII)	'INTEL'
0x5C	1	Product Name Type/Length Byte	0xCD
0x5D	13	Product Name	' '
0x6A	1	Board Serial Number Type/Length Byte	0xCA
0x6B	10	Board Serial Number	
0x75	1	Board Part Number Type/Length Byte	0xCC
0x76	12	Board Part Number	
0x82	1	No More Fields Flag	0xC1

EEPROM data may be accessed via IPMB commands to the EEPROM device.

The DRAM configuration data is provided by two 8-bit I/O ports, also on the IPMB bus. These ports allow for the reading of the PD bits and ID bits of each DIMM, which contain information on module speed. The individual bits of this port are defined as follows:

Table 8.4: IPMB I/O Port Pin Definition

Port	Bit	Description
Port 0	P0	PDE Address bit 0 (output only)
Port 0	P1	PDE Address bit 1 (output only)
Port 0	P2	PDE Address bit 2 (output only)
Port 0	P3	PDE Address bit 3 (output only)
Port 0	P4	Reserved
Port 0	P5	DR50H pin on RCG (input only)
Port 0	P6	DIMM ID bit 0 (input only)
Port 0	P7	DIMM ID bit 1 (input only)
Port 1	P0	DIMM PD bit 1 (input only)
Port 1	P1	DIMM PD bit 2 (input only)
Port 1	P2	DIMM PD bit 3 (input only)
Port 1	P3	DIMM PD bit 4 (input only)
Port 1	P4	DIMM PD bit 5 (input only)
Port 1	P5	DIMM PD bit 6 (input only)
Port 1	P6	DIMM PD bit 7 (input only)
Port 1	P7	DIMM PD bit 8 (input only)

To read a particular DIMM's ID and PD bits, software must first write a 4-bit address to bits P0-P3 of Port 0. Once the write has taken place, software may then read the ID bits from P6-P7 of Port 0 and PD bits from P0-P7 of Port 1. The following table shows the mapping of PDE address to individual DIMMs.

Table 8.5: PDE Address Map

DIMM	Address	DIMM	Address
Bank A, Interleaves 0 & 1, Low Data (J1)	0x0	Bank A, Interleaves 0 & 1, High Data (J3)	0x8
Bank A, Interleaves 2 & 3, Low Data (J2)	0x1	Bank A, Interleaves 2 & 3, High Data (J4)	0x9
Bank B, Interleaves 0 & 1, Low Data (J5)	0x2	Bank B, Interleaves 0 & 1, High Data (J7)	0xA
Bank B, Interleaves 2 & 3, Low Data (J6)	0x3	Bank B, Interleaves 2 & 3, High Data (J8)	0xB
Bank C, Interleaves 0 & 1, Low Data (J9)	0x4	Bank C, Interleaves 0 & 1, High Data (J11)	0xC
Bank C, Interleaves 2 & 3, Low Data (J10)	0x5	Bank C, Interleaves 2 & 3, High Data (J12)	0xD
Bank D, Interleaves 0 & 1, Low Data (J13)	0x6	Bank D, Interleaves 0 & 1, High Data (J15)	0xE
Bank D, Interleaves 2 & 3, Low Data (J14)	0x7	Bank D, Interleaves 2 & 3, High Data (J16)	0xF

DIMM ID and PD bit definitions are available in JEDEC Standard #21-C, figure 4-13C, and are reprinted here.

Table 8.6: PD and ID Bit Definition

PD Bits 4 3 2 1	Module Configuration	DRAM Organization	DRAM ROW ADDR.	DRAM COL. ADDR.	Avg. Refresh Interval Normal / Slow (ms)
1 1 1 1	NO MODULE				
0 0 0 0	256Kx64/72,72	256Kx16/18	9	9	15.6 / 125
0 0 0 1	512Kx64/72,72	256Kx16/18	9	9	15.6 / 125
0 0 1 0	512Kx64/72, 72/80	512Kx8/9	10	9	15.6 / 125
0 0 1 1	1Mx64/72, 72/80	512Kx8/9	10	9	15.6 / 125
0 1 0 0	1Mx64/72, 72/80	1Mx1/4/16/18	10	10#	15.6 / 125
0 1 0 1	2Mx64/72, 72/80	1Mx1/4/16/18	10	10#	15.6 / 125
0 1 1 0	1Mx64/72, 72	1Mx16/18	12	8	15.6 / 31.2
1 0 0 0	2Mx64/72, 72	1Mx16/18	12	8	15.6 / 31.2

PD Bits 4 3 2 1	Module Configuration	DRAM Organization	DRAM ROW ADDR.	DRAM COL. ADDR.	Avg. Refresh Interval Normal / Slow (ms)
1 0 0 1	2Mx64/72, 72/80	2Mx8/9	11	10	15.6 / 62.5

Table 8.6: PD and ID Bit Definition

PD Bits 4 3 2 1	Module Configuration	DRAM Organization	DRAM ROW ADDR.	DRAM COL. ADDR.	Avg. Refresh Interval Normal / Slow (ms)
1 0 1 0	4Mx64/72, 72/80	2Mx8/9	11	10	15.6 / 62.5
1 0 1 1	4Mx72	4Mx1/4/8	12**	11**	15.6 / 31.2
1 0 1 1	4Mx64, 72/80	4Mx4/16	12/11	10/11	15.6 / (31.2/62.5)
1 1 0 0	8Mx64/72, 72	4Mx16/18	12/11	10/11	15.6 / (31.2/62.5)
1 1 0 1	8Mx64/72, 72/80	8Mx8/9	12	11	15.6 / 31.2
1 1 1 0	16Mx64/72, 72/80	8Mx8/9	12	11	15.6 / 31.2
1 1 1 1	16Mx64/72, 72/80	16Mx4	13/12	11/12	15.6 / (TBD/31.2)
0 0 0 0	16Mx72, 72	16Mx16/18	13/12	11/12	15.6 / (TBD/31.2)
0 0 0 1	32Mx72, 72	16Mx16/18	13/12	11/12	15.6 / (TBD/31.2)
0 0 1 0	32Mx64/72, 72/80	32Mx8/9	14/13	11/12	(7.8/15.6) / TBD*
0 0 1 1	64Mx64/72, 72/80	32Mx8/9	14/13	11/12	(7.8/15.6) / TBD*
0 1 0 0	64Mx64, 72/80	64Mx4	14/13	12/13	(7.8/15.6) / TBD*
0 1 1 1	EXPANSION				

Note 1) * These modules using 256M devices are for reference only and will be further defined in the future.

Note 2) 1 = Logic high ; 0 = Logic low; In Table Information.

Note 3) ** This addressing includes a redundant address to allow mixing of 12/10(X4) and 11/11(X1) DRAMs

Note 4) # 1M X 16/18 DRAMS with 10/10 addressing may dissipate excessive power in many applications. Care must be taken to ensure device thermal limits are not exceeded. 12/8 addressing is provided as a lower power option.

PD Note: PD & ID terminals must each be pulled up through a resistor to VDD at the next higher level assembly. PDs will either be open or driven to VOH or driven to VOL via on–board buffer circuits.

ID Note: IDs will either be open (NC) or connected directly to VSS without a buffer.

Table 8.7: Related Information

Speed	PD7	PD6
80 ns	0	1
70 ns	1	0
60 ns	1	1
50 ns	0	0
40 ns	0	1
PD SPEED TABLE		

Config	PD8	ID0
x64	1	0
x72 Parity	1	1
x72 ECC	0	0
x80 ECC	0	1
DATA CONFIGURATION		

Refresh Mode	ID1
Normal	0
Self-refresh	1

Data Access Mode	PD5
Fast Page	
FP W/EDO	
EDO DETECTION	

8.4.4 JTAG Scan

The S450NX MP Server memory module supports JTAG scanning its Intel 82450NX PCIset components, the RCG and MUXes. JTAG Test Access Ports on both the RCG and the MUXes provide access to both boundary scan and internal configuration and status registers.

The following diagram illustrates the scan chain on the memory module. Note that TDI from the connector is pulled up, while TDO to the connector is not.
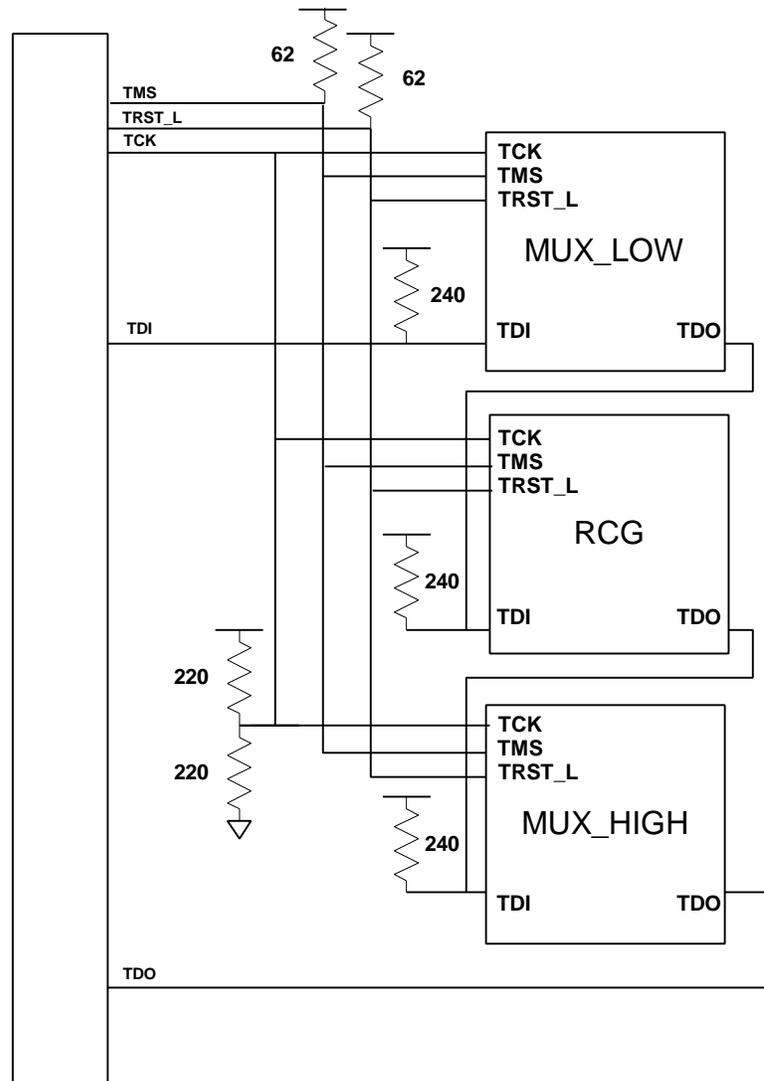
Figure 8.6: JTAG Scan Chain

8.5 Signal Descriptions

8.5.1 Memory Interface Bus Signals

Following is a summary of memory signal pins, including the signal mnemonic, electrical type, full name, and brief description. The electrical types are as follows:

Table 8.8: Electrical Types

Type	Description
in	Input is a standard input-only signal.
out	Totem Pole Output is a standard active driver.
o/d	Open Drain allows multiple devices to share signals as a wired-OR.

The memory interface signals supported are listed in the following table.

Table 8.9: Memory Interface Connector Signal Summary

Signal(s)	Type	Name and Description
MA[13:0]#	in	Memory Address Bus. These signals define the address of the location to be accessed in the DRAM. The signals are driven on two successive clock cycles to provide up to 28-bits of effective memory address.
CSTB#	in	Command Strobe. This strobe, when active indicates the initiation of an access.
ROW#	in	Row Select. This signal, when validated with CSTB#, indicate which row in the selected memory bank will receive this access.
BANK[2:0]#	in	Bank Selects. These signals, when validated with CSTB#, indicates which memory bank will service this access.
CARD#	in	Card Select. This signal, when validated with CSTB#, indicates which memory card will service this access.
CMND[1:0]#	in	Access Command. These signals, when validated with CSTB#, encode the command of the current operation. The command encodings follow: 00 Memory read operation 01 Memory write operation 10 Memory refresh operation 11 Reserved
RCMPLT#	out	This signal, which is driven by the device selected by RCARD/BANK/ROW signals, indicates the completion of a request in the memory array.
GRCMPLT#	in/out	A global version of RCMPLT#, connecting all RCGs across both cards, but not to the MIOC. Asserted coincident with RCMPLT#, and by the same agent, this signal allows all RCGs to monitor each request completion without placing undue loading on the RCMPLT# signals.
MRESET#	in	Memory Sub-system Reset. This signal represents a hard reset of the memory sub-system. It is asserted following PWRGD or upon the MIOC issuing a CPU RESET due to software invocation. All state relating to pending operations is cleared, returning the memory sub-system to an idle condition. All configuration and status registers are also returned to a default state.
PHIT# RHIT#	in	These signals, which are driven at the same time as RCMPLT# by the device selected by the CARD/BANK/ROW signals, gives an indication of what, if any, resource delayed the initiation of a read. PHIT RHIT 0 0 Bank was idle 0 1 Had to wait for Row precharge 1 0 Other side of DIMM was using address lines 1 1 Page was open, could skip Row Address Select
WDEVT#	in	Delay Event. This signal is issued by the MIOC to inhibit the response to the earliest memory request issued on this interface.
DSTBP[3:0] DSTBN[3:0]	in/out	Data Strobes (Differential Pair). This set of four differential pair signals are strobes which qualify the validity of the Qword data transfer between the MUX and MIOC. Each strobe pair qualifies 18 bits, as follows: DSTB[0]# qualifies MD[17:0]# DSTB[1]# qualifies MD[35:18]# DSTB[2]# qualifies MD[53:36]# DSTB[3]# qualifies MD[71:54]# In a 4:1 interleaved system, with 2 MUXs per card, DSTB[1:0]# strobes the low MUX and DSTB[3:2]# strobes the high MUX.
MD[71:36]# MD[35:0]#	in/out	Memory Data. These signals are connected to the external datapath of the MUXs. The MUX is connected between the MIOC and the DRAM. Each MUX provides 36 bits of the 72-bit datapath to the MIOC.

Signal(s)	Type	Name and Description
DCMPLT#	out	Data Transfer Complete. This signal is driven by the source of the data transfer during valid DSEL[1:0]# activation (by the MIOC for writes, the MUX for reads). DCMPLT# active indicates that the data transfer is complete. This signal is activated one clock before the last data transfer clock on the MD bus.
GDCMPLT#	in/out	Global DCMPLT#. a global version of DCMPLT#, connecting all MUXs across both cards, but not connected to the MIOC. Asserted coincident with DCMPLT#, and by the same agent, this signal allows all MUXs to monitor each data completion without placing undue loading on the DCMPLT# signals.
DOFF[1:0]#	in	Data Offset. These two bits define the initial Qword access order for the data transfer. The result is that the critical chunk is accessed first and the remaining chunks are accessed in Intel 'Toggle' order.
DSEL#	in	Data Card Select. This signal selects which card the memory transfer is coming from or destined towards.
DVALID#	in	Data Transfer Complete. This signal indicates that the signals on the DSEL# are valid. DVALID# is activated, at the minimum, in the second clock after DSEL# is active. The fastest DVALID# repetition rate is once every two clocks.
RCGCLK, MUXCLK0, MUXCLK1	in	Host Clock In for the RCG and the MUXes. These are buffered versions of the host clock.
SCL	in/out	IPMB Clock. Clock reference for the IPMB interface.
SDA	in/out	IPMB Data. Serial data transfer for the IPMB interface.
TCK	in	Test Clock. Test clock is used to clock state information and data into and out of the device during boundary scan.
TDI	in	Test Data Input. Test Input is used to serially shift data and instructions into the TAP. This signal is pulled up to 3.3 V through a 150 ohm resistor on the memory module.
TDO	o/d	Test Output. Test Output is used to shift data out of the device. This signal is not pulled up on the memory module.
TMS	in	Test Mode Select. Test Mode Select is used to control the state of the TAP controller.
TRST#	in	Test Reset. Test Reset is used to reset the TAP controller logic.

8.5.2 DRAM Interface Signals

Following is a summary of DRAM Interface signal pins, including the signal mnemonic, name, and brief description. These signals go between the RCG and DRAM.

Table 8.10: DRAM Interface Signal Summary

Signal(s)	Name and Description
RAS#	Row Address Strobe.
CAS#	Column Address Strobe.
WE#	Write Enable.
ADDR[13:0]	Address.
Q1D[35:0]	Quad Word #1.
Q2D[35:0]	Quad Word #2.
Q3D[35:0]	Quad Word #3.
Q4D[35:0]	Quad Word #4.
ID[1:0]	Identification Bits.
PD[8:0]	Presence Detect.
PDE#	Presence Detect Enable.

8.5.3 Other Signals

Following is a summary of other signals, including the signal mnemonic, name, and brief description. These signals go between Intel 82450NX PCIset components.

Table 8.11: Other Signal Summary

Signal(s)	Name and Description
ACWD#	Accept Write Data. Enables the MUX array to accept a write data transfer. RCG → MUX.
AVWP#	Advance MUX Write Path Pointers. Advances the read pointer in the MUX's write path FIFO. RCG → MUX.
LRD#	Load Read Data. This signal loads read data from the DRAM into the MUX. RCG → MUX.
LDSTB#	Load Data Strobe. This signal controls a latch in the MUXes to precisely control when read data is latched from the DRAM data bus. RCG → MUX.
DR50H	50ns DRAM Here. This strapping pin selects between 60ns and 50ns DRAM timings for the RCG. If asserted, 50ns timings will be used.
DR50T	50ns DRAM There. This strapping pin selects between 60ns and 50ns DRAM timings for a hypothetical second RCG on the card. Since there is only one RCG on the board, this signal is always deasserted.

8.6   Mechanical Specifications

The following diagram shows the mechanical specifications of the S450NX MP Server Memory Module. All dimensions are given in inches.

Figure 8.7: Memory Module Mechanical Specification

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Appendix A.   Supported Environments

The S450NX MP Server is being validated with leading network operating systems.

Operating Systems Under Validation

- Level 1   Heavy testing done in Intel's Server Validation Lab.
- Level 2   Testing done in Intel's Server Compatibility Lab.

Table A-1: Validated Operating Systems

Level	Operating System	Version	UP/MP	Comments
1	Intranetware*	1	SMP	With the most up to date service pack.
1	SCO UnixWare*	7	SMP	Gemini (UnixWare 7) FCS 1/98. Fall back is Unixware 2.1.2.
1	Win NT* Server Enterprise	4.0	SMP	With the most up to date service pack.
2	Intranetware* (Japanese)	1	SMP	
2	IntraNetware	2	SMP	Will be validated when available. Beta now.
2	Win NT* Server Enterprise (Japanese)	4.0	SMP	Should be available Q198, but will be validated when available.
2	Win NT* Workstation	4.0	SMP	
2	Win NT* Server	5.0	SMP	Will be validated when available. Beta now.
2	Win NT* Server (Japanese)	5.0	SMP	Will be validated when available. Beta now.
2	IBM OS/2* Warp Server SMP	4.0	SMP	
2	MS DOS	6.22	UP	
2	SCO UnixWare*	2.1.2	SMP	
2	Solaris*	2.6	SMP	
2	SCO OpenServer	ODT 5.0.4	SMP	

A document is available which describes the add-in cards used and the driver version tested. It is beyond the scope of this document to provide here. Contact your Intel Representative for availability.

Appendix B.   Product Codes/Spares

Product Codes

Table B-1: S450NX MP Board Product Codes

Description	Product code
S450NX Baseboard	SKBBS450NXB
S450NX Termination Assembly - Term Card, Housing, and Latches to support four processors	SKTERMASSY
S450NX Memory Module	SKMEM
S450NX Front Panel	SKFP
S450NX SCSI Backplane	SKSCSIBP
S450NX ICMB Board	SKICMB
S450NX Power Distribution Board 1 (Supports only 1 P/S)	SKPDB1
S450NX Power Distribution Board 2 (Supports only 2 P/S)	SKPDB2
S450NX Power Share Board (Supports 1, 2, or 3 P/S)	SKPSB

Table B-2: S450NX MP Server System Product Codes

Description	Product code
Base Redundant System - 0 Processors, PSB, 2 400W P/S, SCSI Backplane, 3 E-bay Fans, 2 HD Fans, 2 VRM's, 1 Mem Mod	SKCB000NP0RD
Base System - 0 Processors, PDB 1, 1 P/S, 1 SCSI Cable, 3 E-bay Fans, 0 HD Fans, 2 VRM's, 1 Mem Mod	SKCB000NP0EN
Redundant System w/processors - 2 400/512, PSB, 2 400W P/S, SCSI Backplane, 3 E-bay Fans, 2 HD Fans, 2 VRM's, 1 Mem Mod	SKCB4002P0RD

Spares/Accessories

Table B-3: Spares/Accessories List

Description	Product Code
S450NX Termination Card	SKTERM
400/512 Processor Kit - 1 400/512k Pentium® II Xeon™ processor with attached Heatsink	SL2400512KIT
400/1M Processor Kit - 1 400/1M Pentium® II Xeon™ processor with attached Heatsink	SL24001MKIT
450/512 Processor Kit - 1 450/512k Pentium® II Xeon™ processor with attached Heatsink	SL2450512KIT
450/1M Processor Kit - 1 450/1M Pentium® II Xeon™ processor with attached Heatsink	SL24501MKIT
450/2M Processor Kit - 1 450/2M Pentium® II Xeon™ processor with attached Heatsink	SL24502MKIT
Slot 2 Retention Module - Housing, Bracket, and Latches	SKCBRETENTION
Slot 2 Heatsink	SLOT2HEATSNK
Slot 2 Voltage Regulation Module (12V)	SLOT2VRMMOD
Slot 2 Voltage Regulation Module 10-pack (12V)	SLOT2VRMPKG

Appendix C.   Customer Support

FAXBack

- Product descriptions and technical data sent to any fax machine from a touch-tone phone
- Information on End-of-Life products
- Available worldwide through direct dial

U.S. Toll Free   800-628-2283
Americas: 916-356-3105
Europe: 44-793-496646

Intel Application Support
Contact Your Local Technical Representative

The customer's number one asset is the local representative. For all technical issues, first contact your Field Application Engineer.

Hotline

A direct link to highly qualified and well trained technical personnel.

- Toll-free access to Intel support engineers for problem resolution
- Responses within 24 hours Monday-Friday
- Expert assistance geared to the special needs of OEMs and VARs

1-800-628-8686

Internet

A full service World Wide Web location with product information and more will be available at release time.

⇒   Available worldwide through:

http://www.intel.com/
ftp.intel.com
http://www.intel.com/procs/ppro/server/compdir/

- FLASH BIOS upgrade files
- Server Configuration Utility (SCU) upgrade files

Year 2000 Capable

The S450NX MP Server Baseboard is Year 2000 capable. For more information with regard to the Year 2000 issue, please refer to the Intel web site at http://support.intel.com/sites/support/index.htm.

Reference Documents

The following documents are available to provide further information. Please contact your Intel representative for more information.

Power Supply, 400W, 5 Output, with PFC

Cabrillo Chassis Technical Product Specification

S450NX MP Server Product Guide

MTA Testview User's Guide

Supported O/S & Adapters