Intel B440FX DP Server Server Board Set

Technical Product Specification

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The B440FX DP Server baseboard may contain design defects or errors known as errata. Characterized errata that may cause the B440FX DP Server baseboard's behavior to deviate from published specifications are documented in the B440FX DP Server Specification Update.

Revision History

Revision	Revision History	Date
Rev 0.9-2.6	Preliminary releases of the B440FX DP Server Technical Product Specification	7/96
Rev 2.7	Preliminary release of the B440FX DP Server Technical Product Specification	10/96

This product specification applies only to standard B440FX DP Server board with BIOS identifier DA0. Information in this version of the summary applies to the BIOS 1.00.03 DA0. Different versions of the BIOS may look and behave differently.

Changes to this specification will be published in the B440FX DP Server Board Specification Update before being incorporated as a revision to this document.

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1. PRODUCT OVERVIEW

The B440FX DP Server is a high performance dual Pentium® Pro processor server as well as a high-reliability corporate desktop machine. The baseboard system architecture is based on the Pentium Pro processor and the Intel 82440FX PCIset. The system is partitioned into two modules: a dual Pentium Pro processor/Memory/PCI bridge subsystem (all contained on a processor board) and a baseboard that contains the I/O system and a connection to the processor board. Partitioning the server in this way places all high-speed interconnects on the same board, eliminating the need for connectors. The B440FX DP Server includes the following features:

- Volume server or desktop platform able to support one or two Pentium Pro processors. The system is fully MPS 1.4 compliant with appropriate Pentium Pro extensions. In addition, support (e.g., PCI interrupt to ISA IRQ rerouting) is provided for MP operating systems that may not be fully MPS 1.4 compliant.
- Modular processor/memory card that quickly adapts to processor and memory technology changes.
- System design based on Intel 82440FX PCIset and I/O APIC.
- Support for up to 1GB of memory using 72-bit buffered dual inline memory module (DIMM) devices.
- Primary and secondary PCI segments. The primary PCI bus is compliant with revision 2.1 of the PCI specification. The primary PCI bus, with four expansion slots (one shared with ISA), is provided via the host bridge. The secondary segment, with two slots, is provided via the PCI-to-PCI bridge.
- Three ISA slots (one shared with PCI) and PC Compatibility I/O (serial, parallel, mouse, and keyboard).
- Onboard PCI I/O, including SCSI, IDE, Video, and LAN controllers.
- Server management features, including thermal/voltage and ECC monitoring.
- Flash BIOS support for all of the above.

1.1 Related Documentation

Balboa Chassis Technical Product Specification

Columbus II Chassis Technical Product Specification

B440FX DP Server Performance Report

B440FX DP Server Product Guide

Adaptec AIC-7880 SCSI Software Guide

BB440FX DP Server system Data Sheet

LANDesk Server Manager 2.52 TPS

B440FX DP Server Board Specification Update

2. BOARD SET DESCRIPTION

2.1 Functional Architecture

This section provides an overview of the B440FX DP Server, explaining the functional blocks and their relationships to each another. The following diagram shows the functional architecture of the server and the system architecture that it supports. The dotted lines surround the major functional blocks. The top half of the diagram shows the processor board, and the bottom half shows the baseboard.

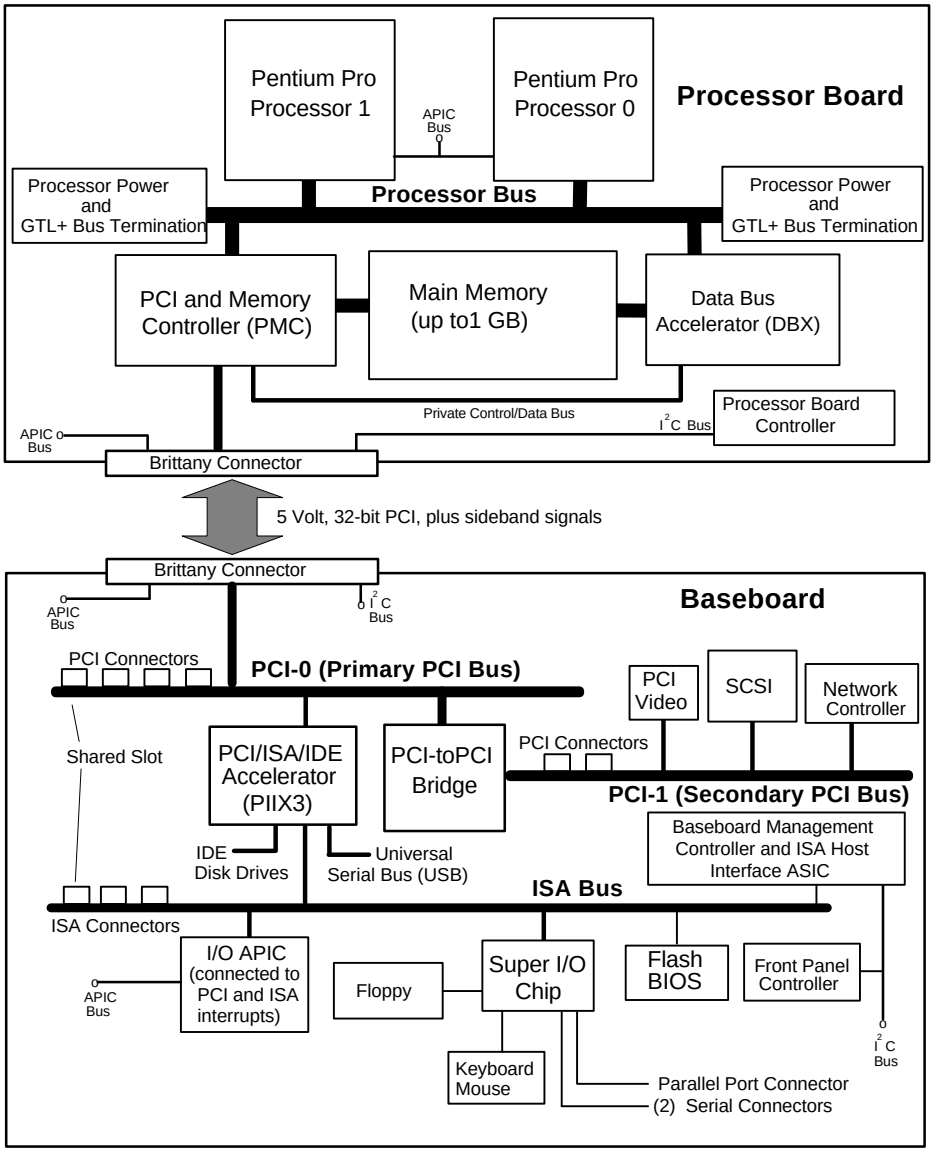


Figure 2-1 B440FX DP Server Functional Block Architecture

2.2 Processor Board

The dual processor module for the B440FX DP Server system consists of two devices: the PCI and Memory Controller (PMC) and the Data Bus Accelerator (DBX). The processor board connects to the baseboard on an interface known as the Brittany connector.

2.2.1 PMC and DBX

Two devices from the Intel 82440FX PCIset, PMC and DBX, form the core of the processor board design. These devices implement the host bridge function between the Pentium Pro processors and PCI I/O system. As the host bridge, they maintain proper ordering of operations by trapping synchronization events and flushing buffers appropriately. The PMC and DBX provide the 32-bit address/64-bit data processor bus interface, which operates at 66MHz (or 60MHz, depending on processor frequency) in the GTL+ signaling environment. The PMC provides a 32-bit PCI interface which operates synchronously in a 5V signaling environment at half the processor bus frequency.

The PMC also acts as memory controller for the system, and the DBX provides the data path to memory. They communicate with each other by using a private control and data bus, which operates independently of transactions on the processor bus and PCI bus. This memory controller supports up to 1GB of ECC memory, using Fast Page Mode (FPM) or Extended Data Out (EDO) DRAMs. ECC can detect and correct single-bit errors and can detect multiple-bit errors.

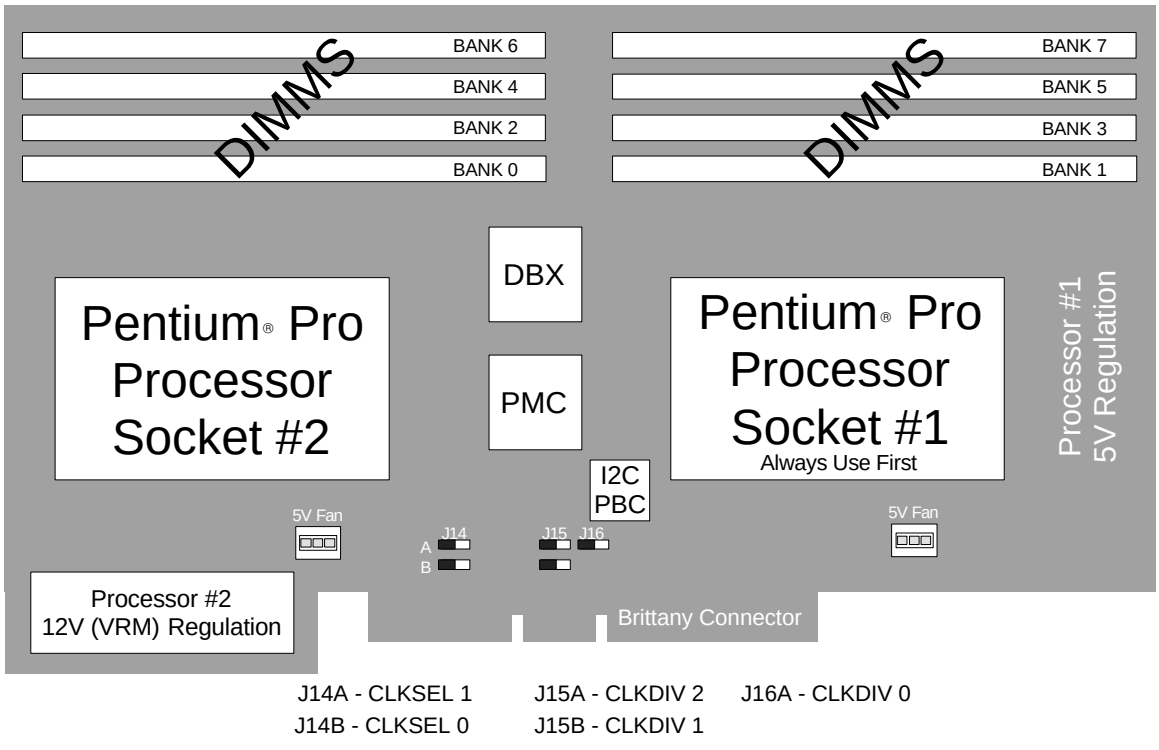


Figure 2-2 B440FX DP Server Processor Board Layout

2.3 Processor Subsystem

The Processor subsystem resides on the plug-in module. It contains the following:

- Dual Pentium Pro processor sockets
- Pentium Pro processor bus, with GTL+ termination and term. power supply
- APIC bus
- Clock generation
- Plug-in 12V DC-to-DC converter for secondary processor (processor 1) Vccp power
- Onboard 5V DC-to-DC converter for the primary processor (processor 0) Vccp power
- Processor board management microcontroller, and I^2C-based thermal monitor

NOTE: *If you are using only a single processor, the primary processor must be installed first. When you install the second processor, you must also install a Vccp power module. Both processors must be of the same revision and have identical clock frequencies.*

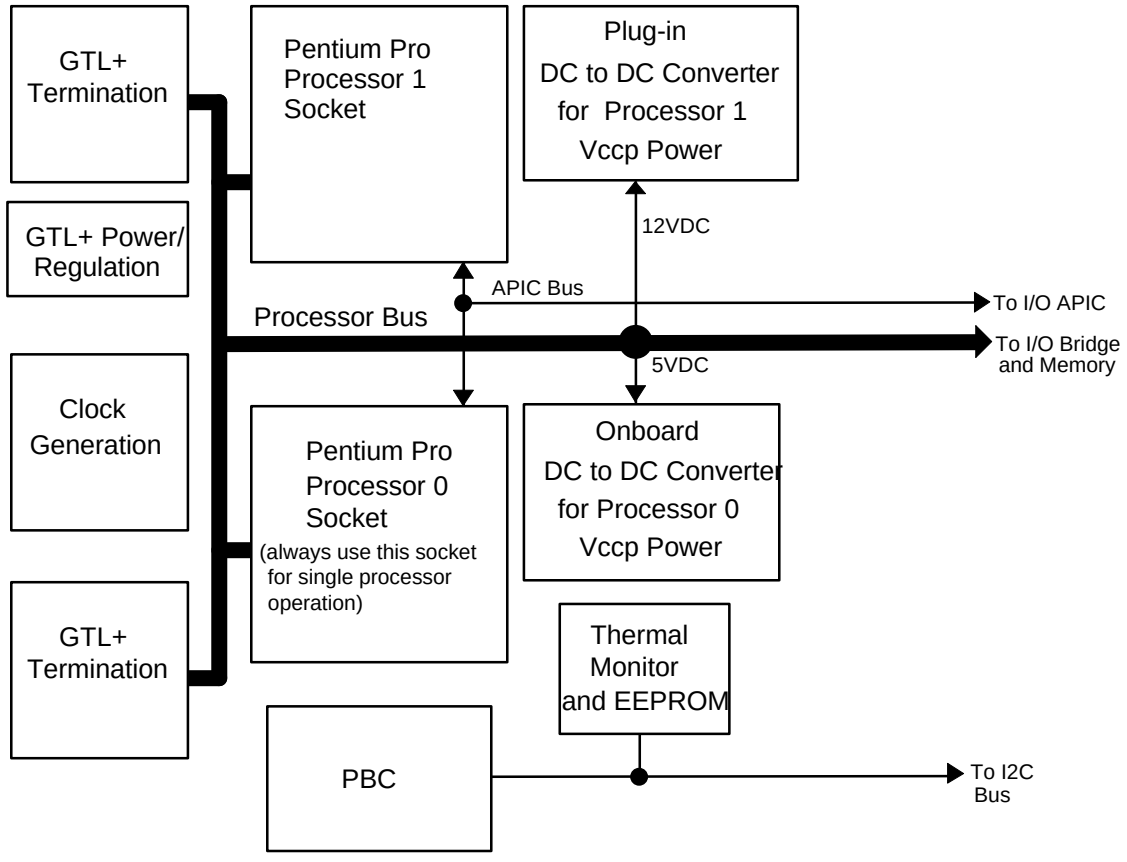


Figure 2-3 Processor Subsystem Block Diagram

2.3.1 Pentium Pro processor

The Pentium Pro processor, housed in a 387-pin dual-cavity PGA package, is the next generation Intel architecture microprocessor. Currently, the package contains two devices: a 5.5 million transistor CPU core with 8KB primary cache, and 15.5 million transistor 256KB secondary cache that communicates with the CPU using a dedicated internal bus. The Pentium Pro external interface is designed to be MP ready. Each processor contains a local APIC section for interrupt handling in the multi-processor and uni-processor environments.

2.3.2 Processor Bus Termination/Regulation/Power

The dual Pentium Pro processors connect to the processor bus. The processors are socketed, allowing the option to install one processor on shipment and upgrades supplied later. The termination circuitry, required by the processor bus (GTL+) signaling environment, has 1.5V termination power.

2.3.3 Processor Vccp Power

DC-to-DC converters provide Vccp power for each processor. Processor 0 Vccp power (14A) is derived from the 5V supply using onboard circuitry. Processor 1 power is derived from the 12V supply using a plug-in module. Refer to the latest revision of the *VRM 8 Data Sheet* for more information.

2.3.4 APIC Bus

Interrupt notification and generation for the Pentium Pro processors is done using an independent path between local APICs in each processor and an I/O APIC located on the baseboard. This simple bus consists of two data bits and a clock line. Refer to “I/O APIC” later in this chapter for more information.

2.3.5 Processor and PCI Clock Generation

All buses on the B440FX DP Server operate using synchronous clocks. The processor bus (66MHz or 60MHz) and the PCI bus (33MHz or 30MHz) clocks are synthesized by circuitry from the processor module from a master clock on the baseboard. The PCI bus clock is sent back to the baseboard for replication and distribution. One copy of the PCI clock is returned to the processor board for use by the PMC.

Two frequency select signals, CLK_SEL[1::0], control the frequency of the master host clock. To minimize the skew between the various host and PCI clocks, multiple copies of tightly controlled host clocks and PCI clocks are generated on the processor board. In the B440FX DP Server implementation, one copy of the PCI clock is sent to the baseboard for replication by a phase lock loop clock buffer chip, with feedback to the processor module for the PMC. This scheme gives multiple tightly controlled host and PCI clocks with a controlled skew between the host and PCI clocks.

2.3.6 Processor Board Controller

A microcontroller directly monitors voltages and error signals on the processor(s). The I^2C interface on the controller supports two onboard thermal monitor devices, one of which contains an EEPROM for non-volatile storage of vital information.

2.4 PCI Bridge and Memory Subsystem

All high-speed interconnections between the processor bus, PCI host bridge, and system memory are contained on the processor board. The PCI host bridge, the memory controller, and DIMM sites are all found in this subsystem.

2.4.1 PCI Host Bridge

The PCI host bridge consists of two of the 208-pin PQFP devices in the Intel 82440FX PCIset:: the PMC (control part) and the DBX (data part). These two devices coordinate operations over an independent private bus. The PCI host bridge supports one or two Pentium Pro processors at a processor bus frequency of up to 66 MHz, with 32-bit addressing, optimized 4-deep in-order and request queue (IOQ), multi-processing support, dynamic deferred transaction support, and USWC support. The host bridge translates address and data operations from the GTL+ signaling environment on the processor bus to a PCI Rev. 2.1 compliant, 5V signaling environment.

The PCI interface provides greater than 100 MB/s data streamlining for PCI to DRAM accesses, while supporting concurrent Pentium Pro and PCI transactions to main memory. This is accomplished using extensive data buffering with processor-to-DRAM and PCI-to-DRAM write data buffering and write-combining support for processor-to-PCI burst writes. In addition to the host and PCI to ISA bridge functions, five PCI masters can be supported.

2.4.2 Memory Controller

The PMC performs the function of memory controller for the B440FX DP Server. Total memory from 16MB to 1GB of DIMM DRAM is supported, with the DBX providing a 72-bit non-interleaved pathway to main memory. The memory controller supports FPM and EDO DRAMs.

ECC can detect and correct single-bit errors (SED/SEC), detect all double-bit errors, and detect some multiple-bit errors (DED). Only memory ECC is supported; the B440FX DP Server does not support ECC on processor signals or parity checking. On power-up, ECC is disabled.

2.4.3 DRAM Array

The memory controller can automatically detect and initialize the memory array, depending upon the type, size, and speed of installed DIMM devices. 8, 16, 32, 64, and 128 MB DIMMs are supported. Memory is partitioned as eight banks of DRAM, one bank per installed DIMM, each providing 72 bits of non-interleaved memory (64-bit main memory plus ECC). The PMC provides a row address strobe (RASx_L) for each bank, and column address strobes (CASx_L) for all data bits. DIMM sockets should be populated in sequence (DIMM-0 is first and DIMM-7 is last). Installed memory is automatically sized and allocated by the PMC. The following figure shows the correspondence between installed DIMMs, PMC RASn_L signals, and DRAM row boundary (DRB) register values.

NOTE: *If 4 or fewer DIMMs are installed, faster memory timing is available: x-2-2-2 for EDO devices, x-3-3-3 for FPM devices. With 5 to 8 DIMMs, memory timing is x-3-3-3 for EDO and x-4-4-4 for FPM.*

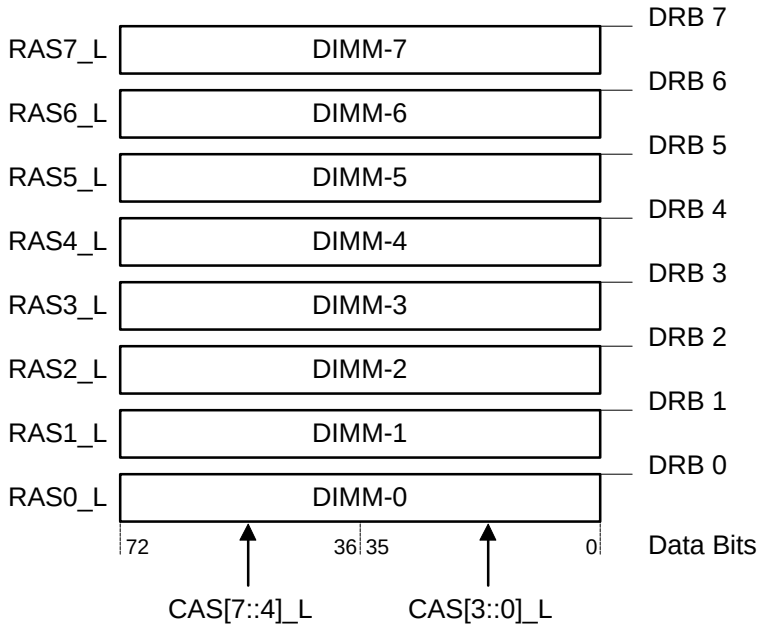


Figure 2-4 DIMMs and DRAM Row Boundaries

2.5 Brittany Connector Interface

The Brittany connector interface connects the processor board to the baseboard. It operates as a standard 5V PCI connection, and it works with the Pentium Pro host bus at half frequency. The interface is a modified 33MHz 5V PCI implementation, with sideband signals specific to the B440FX DP Server (or subsequent) baseboard designs. Included among the sideband signals are I/O APIC and I^2C buses. The I/O APIC bus minimizes interrupt latency time by providing a direct pathway from the I/O APIC device on the baseboard to the local APIC(s) in the processor(s). The I^2C bus provides an independent communications path for onboard diagnostics and server management.

The edge connector resembles a 64-bit PCI card.

2.6 Baseboard

The baseboard contains a PCI and ISA I/O system with several embedded devices for video, network, and disk control. It provides server management, hardware support monitoring, interrupt control (I/O APIC and standard PC), and it connects to the processor board via the Brittany connector.

The baseboard consists of the following major components:

2.6.1 PCI I/O Subsystem

PCI is the primary I/O bus for The B440FX DP Server . There are two PCI bus segments, PCI-0 and PCI-1; they are compliant with revision 2.1 of the PCI specification and operate at up to 33 MHz. PCI-0 is the primary PCI segment, lying directly beneath the PMC. The PCI-1 connects to the PCI-0 using a PCI-to-PCI bridge in a hierarchical bus structure. Unlike previous Intel SSPD server designs that have provided the two PCI segments as peers of each other, the B440FX DP Server uses independent arbitration and data buffering to run the two hierarchical PCI segments concurrently with the processor bus and with each other. However, there are functional differences in the way PCI configuration cycles are handled. According to PCI architecture, the PCI-to-PCI bridge effectively extends the electrical capacity of PCI-0, providing an extensive amount of embedded functionality on a single PCI bus.

2.6.2 ISA I/O Subsystem

The ISA I/O subsystem on the B440FX DP Server provides three ISA slots. The ISA bus supports an embedded I/O APIC and Flash BIOS. A National Semiconductor Super I/O† chip resides on the ISA bus and supports direct connection of the keyboard, mouse, floppy drive, and standard parallel and serial ports.

2.6.3 Server Management Subsystem

The B440FX DP Server system offers server management features that are implemented using three separate microcontrollers and one ASIC.

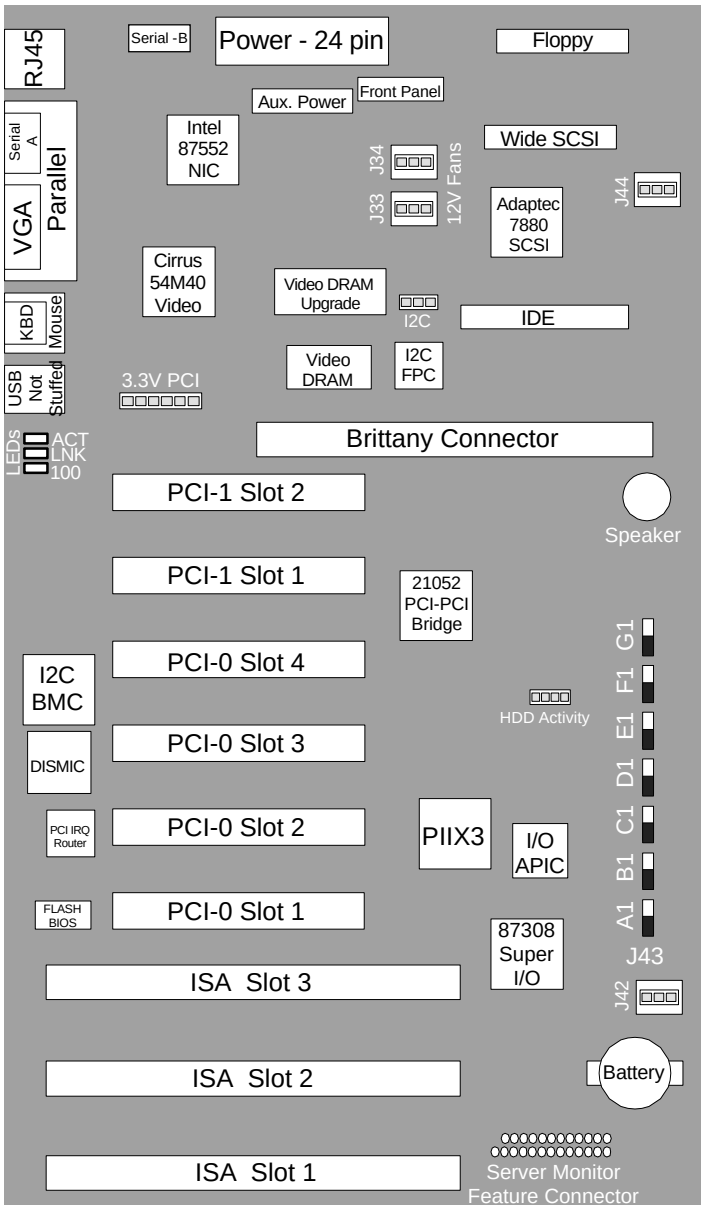


Figure 2-5 B440FX DP Server Baseboard Layout

2.6.4 Primary PCI I/O Subsystem (PCI-0)

All I/O for the B440FX DP Server, including PCI and PC-compatible, is directed through PCI-0. Unlike other Intel SSPD server products, which provide two PCI segments as peers in the PCI hierarchy, the B440FX DP Server architecture defines PCI-0 as the primary PCI segment and uses PCI-1 as its secondary (subordinate) PCI bus.

In addition to the PCI-to-PCI bridge device (described later), PCI-0 supports the following embedded devices and connectors:

Four 120-pin PCI expansion slot connectors (one physically shared with an ISA slot)

PIIX3 PCI-to-ISA bridge and IDE controller subsystem

Each device under a PCI bridge has its IDSEL signal connected to one bit out of AD[31::16], which acts as a chip select on the PCI bus segment. This determines a unique PCI device ID value for use in configuration cycles.

2.6.5 PCI-0 Arbitration

PCI-0 supports six PCI masters (slots 1 - 4, PIIX3, and PCI-to-PCI bridge). These six PCI masters use resources supplied by the PMC to arbitrate for PCI access.

Table 2-1 PCI-0 Arbitration Connections

PMC Signals	Device
PHOLD_L / PHLDA_L	PIIX3
REQ4_L / GNT4_L	PCI-to-PCI Bridge
REQ3_L / GNT3_L	PCI-0 Slot 4
REQ2_L / GNT2_L	PCI-0 Slot 3
REQ1_L / GNT1_L	PCI-0 Slot 2
REQ0_L / GNT0_L	PCI-0 Slot 1

2.6.6 PCI-to-ISA/IDE Subsystem

The PCI/ISA/IDE Accelerator, also known as PIIX3, is a multi-function PCI device integrated into the Intel 82440FX PCIset. There are three distinct PCI controllers on the PIIX3: PCI-to-ISA bridge, and PCI-based fast IDE interface. Each function within the PIIX3 has its own set of registers, which when configured, appear to the system as distinct hardware controllers sharing the same PCI bus interface.

This 208-pin QFP device provides the gateway to all PC-compatible I/O devices and features. The B440FX DP Server architecture uses the following PIIX3 functional blocks:

- PCI interface
- ISA bus interface
- IDE interface
- Universal Serial Bus (USB) interface (not currently implemented on the B440FX DP Server).
- System reset control
- ISA-compatible interrupt control and PCI interrupt steering
- PC-compatible timer/counters and DMA controllers
- Baseboard plug and play support
- System power management features

Following are descriptions of five of these functional blocks.

2.6.6.1 PCI Interface

The PIIX3 fully implements a 32-bit PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Rev. 2.1*. On the B440FX DP Server, the PCI interface operates at up to 33 MHz, using the 5V signaling environment.

2.6.6.2 ISA Interface

Operating at up to 8.33 MHz, the PIIX3 provides an ISA bus interface that supports three ISA connectors, Flash memory, the National Super I/O chip, and baseboard management microcontroller ISA interface ASIC.

2.6.6.3 IDE Interface

The PIIX3 acts as a PCI-based fast IDE controller. It supports PIO and bus master IDE operations, Mode 4 timings, transfer rates to 22MB/s, buffering for PCI/IDE burst transfers, and master/slave IDE mode. The PIIX3 also supports two IDE channels (primary and secondary) that support two drives each (drives 0 and 1). The B440FX DP Server supports only the primary IDE channel, providing one 40 pin (2 x 20) IDE connector. For the pinout, see Chapter 8.

For proper IDE operation, cable length is specified as shown in the following figure. If no drives are present on an IDE channel, the cable must be removed. If only one drive is installed, it must appear at the end of the cable.

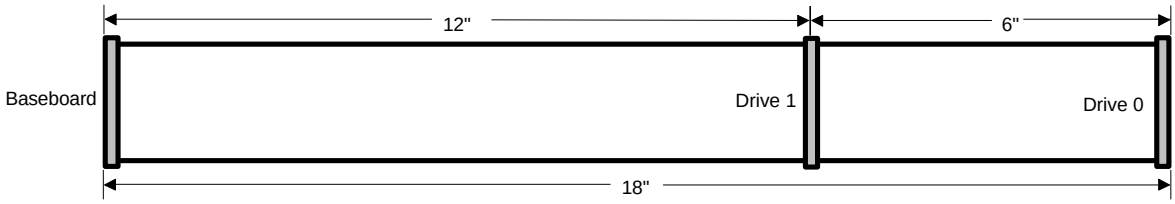


Figure 2-6 IDE Cable Requirements

2.6.6.4 USB Interface

The PIIX3 contains a USB controller with two USB ports. The USB controller moves data between main memory and two devices hooked to the USB connector. An interrupt signal is internally ORed with a PCI interrupt (PCI_INTA) for use in USB transactions. Software is required to manage the USB interface. The B440FX DP Server provides a stacked dual-USB connector interface on the baseboard, as defined by the *USB Specification, Revision 0.9*. However, the B440FX DP Server does not currently support USB.

2.6.6.5 Compatibility Interrupt Control

The PIIX3 provides the functionality of two 82C59 PIC devices for ISA-compatible interrupt handling. The PIIX3 also supports PCI interrupt steering to the I/O APIC, which is controlled using PCI configuration registers. For a complete discussion of interrupt handling on the B440FX DP Server, refer to “I/O APIC” later in this chapter.

2.6.6.6 ISA I/O Subsystem

The ISA bus interface on the PIIX3 device supports the following connectors and devices:

- Three ISA connector slots, one physically shared with PCI-0 slot 4
- Flash memory for BIOS ROM and extensions
- Intel I/O APIC
- National 87308VUL Super I/O Super I/O chip, for which the B440FX DP Server supports the following:
    - Two PC-compatible serial ports
    - Enhanced parallel port
    - Floppy controller
    - Keyboard/mouse port
    - Plug and Play features
    - Real-time Clock (RTC)
    - General Purpose I/O (GPIO) bits used in server management and miscellaneous functions

2.6.6.7 ISA Connectors

The B440FX DP Server provides three ISA expansion slots that follow the pinout shown in Chapter 8. The ISA slot 3 is shared physically with PCI-0 slot 1.

2.6.6.8 Flash ROM

An 8-bit flash memory (Intel 28F004BV) provides 512K x 8 of BIOS and non-volatile storage space, partitioned as shown in the following figure. The Flash device is directly addressed as 8-bit ISA memory.

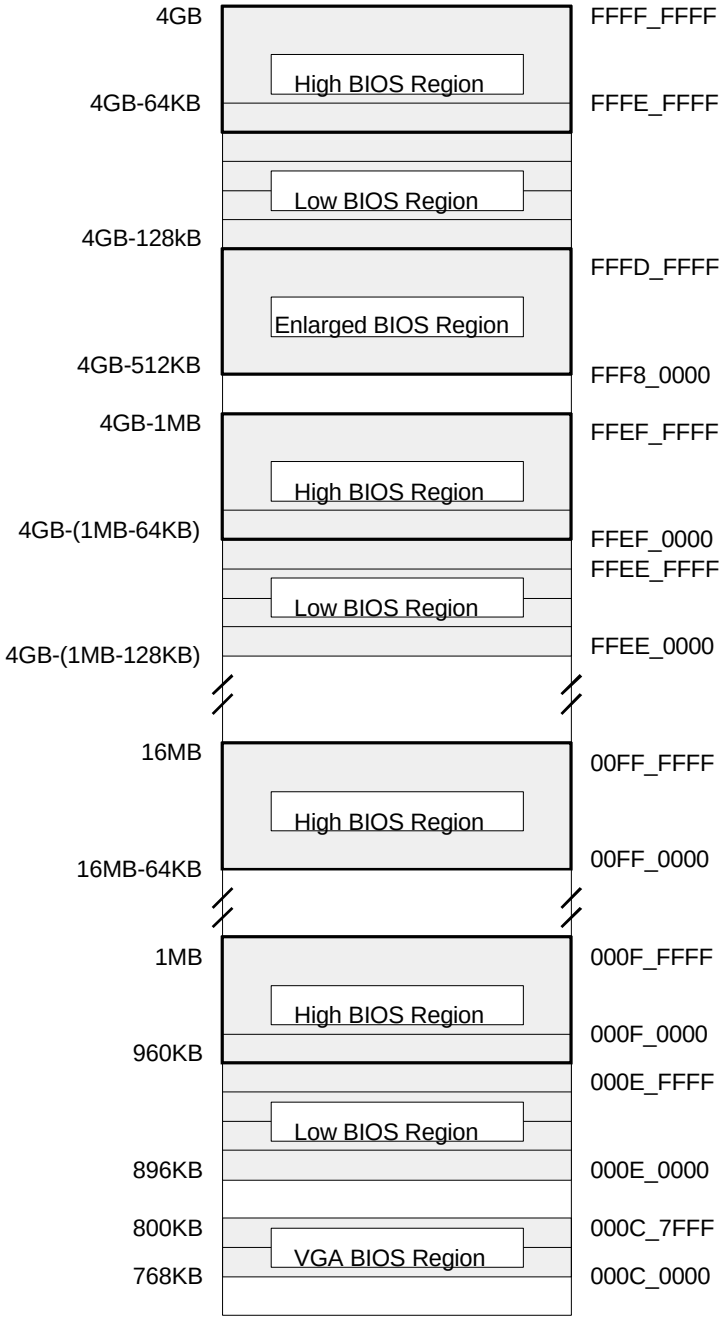


Figure-2-7 Flash Memory Map

2.6.6.9 Flash Update Utility Requirements

You may load flash memory from a floppy disk; a Flash update utility is required (FMUP.EXE).

2.6.7 I/O APIC and Interrupt Mapping

The PIIX3 provides compatibility interrupt control and PCI interrupt steering, which is sufficient for uni-processor PC-compatible operation. However, the B440FX DP Server provides the Intel 82093AA I/O APIC device for interrupt handling when using an operating system that supports multi-processing operation. An APIC bus from the I/O APIC to local APICs in each Pentium Pro processor and APIC support built into the PIIX3 minimizes interrupt latency time from compatibility interrupt sources in single and dual processor operation.

***NOTE**: An ISA IRQ for any PCI device is still allocated, so that an operating system can boot from the device. The multi-processing operating systems will switch the IRQ routing from the PIC to IOAPIC after the HAL / MP kernel is loaded.*

2.6.7.1 PCI Interrupt Routing

Many multi-processing operating systems are unable to handle interrupts from PCI slots and devices as pure PCI interrupts (via inputs 16-23 of the I/O APIC). Instead, they expect PCI interrupts to be delivered as ISA IRQs. In some cases, multi-processing operating systems want some interrupts delivered by the PC-compatible PIC in the PIIX3, and others by the I/O APIC (mixed mode). Some device drivers check whether the device is operating using one of the traditional IRQ interrupts, and if not (when the PCI interrupt is connected directly to the I/O APIC), the driver fails to install or run properly. The PIIX3 performs internal PCI to IRQ interrupt steering so that PCI interrupts can be delivered to the PIC. However, the PCI interrupt steering feature is unidirectional, which means that it cannot be used to redirect PCI interrupts to the I/O APIC inputs.

For these reasons, the B440FX DP Server provides an external PCI to IRQ rerouter that can either be programmed to pass PCI interrupts to inputs 16-19 of the I/O APIC, or can be programmed to deliver a specific PCI interrupt to an ISA IRQ. A PCI interrupt (PCI_INTA_L, PCI_INTB_L, PCI_INTC_L, or PCI_INTD_L) can be individually rerouted to one of these IRQ lines: IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, or IRQ15.

2.6.7.1.1 PCI Interrupt Sharing (Slot Routing)

The PIIX3 has four PCI interrupts, INTA through INTD. The table and figure that follow depict the routing of these interrupts to the various PCI devices and slots within the B440FX DP Server baseboard. This information is supplied in the event that a non-PCI 2.1 compliant adapter is used which exhibits problems sharing interrupts.

Table 2-2 PCI Interrupt Sharing

	PIIX3 PCI_INTA	PIIX3 PCI_INTB	PIIX3 PCI_INTC	PIIX3 PCI_INTD
PCI-1 Slot 2	INTD	INTA	INTB	INTC
PCI-1 Slot 1	INTA	INTB	INTC	INTD
PCI-0 Slot 4	INTB	INTC	INTD	INTA
PCI-0 Slot 3	INTC	INTD	INTA	INTB
PCI-0 Slot 2	INTD	INTA	INTB	INTC
PCI-0 Slot 1	INTA	INTB	INTC	INTD
Onboard USB	X			
Onboard SCSI		X		
Onboard LAN			X	

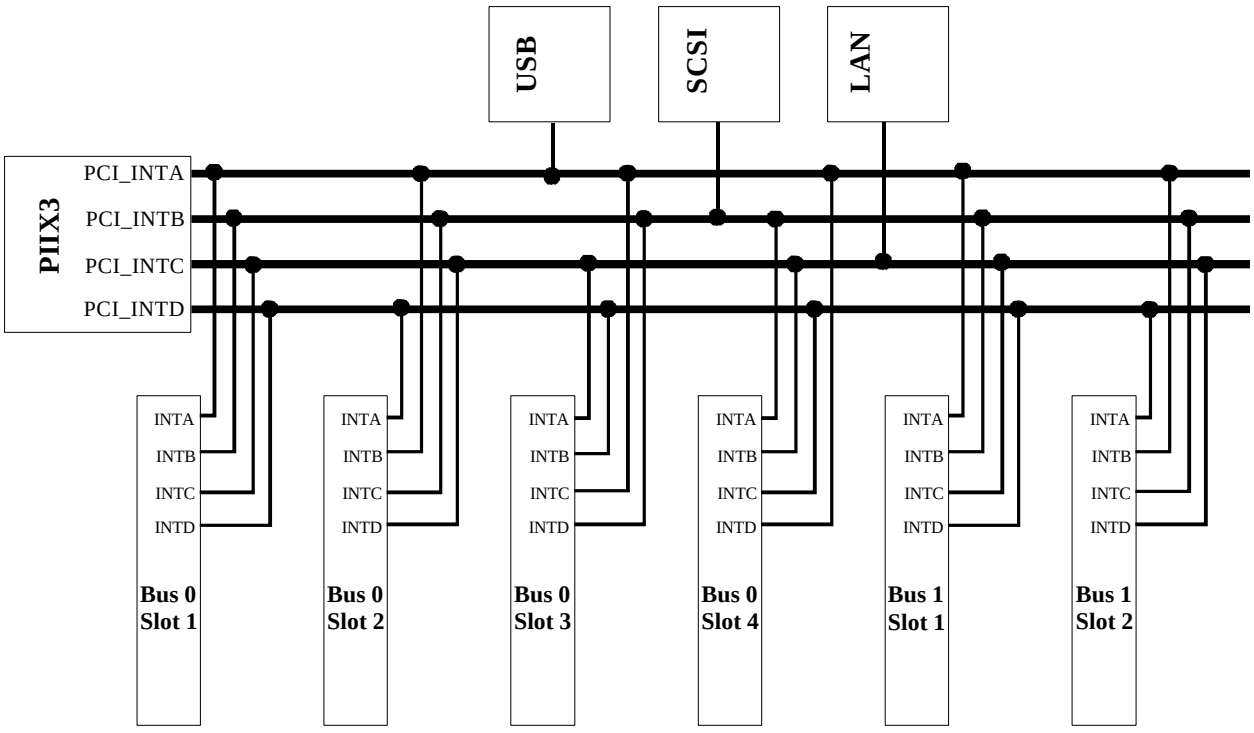


Figure 2-8 PCI Interrupt Routing

2.6.7.2 Compatibility Interrupt Mapping

The PIIX3 and National 87308VUL Super I/O contain configuration registers that determine which interrupt source will map to a specific IRQ line. The PIIX3 controls INTx to IRQ mapping, and the National 87308VUL Super I/O controls which embedded function or device will map to an IRQ.

2.6.7.3 NMI and SMI_L Control

The Server Management SMI_L control logic presents error signals from various sources on the B440FX DP Server that normally produce an NMI to the I/O APIC as SMI_L. This logic is contained in the ASIC that provides the ISA interface for the baseboard server management controller. That logic, in combination with baseboard server management features, controls how NMI and SMI_L are asserted under various fatal error conditions.

2.6.7.4 APIC Bus

The APIC bus that connects the I/O APIC with local APIC(s) in the Pentium Pro processor(s) consists of an APIC clock and two bi-directional data signals (PICD[1::0]). Interrupts are broadcast on the APIC bus as messages conforming to an APIC protocol defined by the register interface embedded in each processor. Multi-processor tables in APIC memory space determine how messages and associated interrupt events are defined to the processors.

2.6.7.5 Interrupt Connections

The following figure illustrates the interrupt connections on the B440FX DP Server between the PIIX3, National 87308VUL Super I/O, and I/O APIC devices.

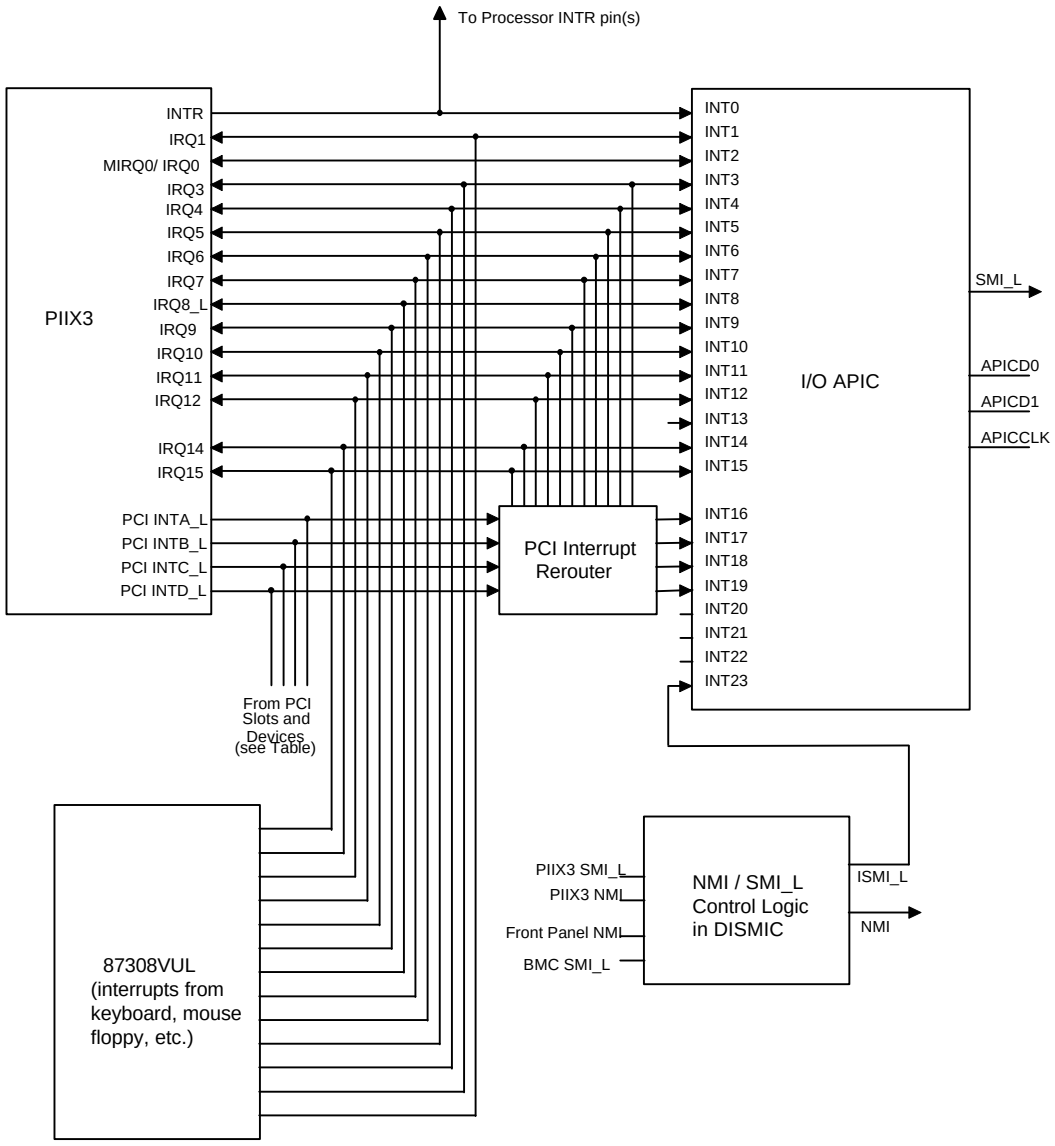


Figure 2-9 Interrupt Connections

2.6.7.6 Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on the B440FX DP Server. The actual interrupt map is defined using configuration registers in the PIIX3 and National 87308VUL Super I/O. The I/O redirection registers in the I/O APIC are provided for each interrupt signal, which define hardware interrupt signal characteristics for APIC messages sent to local APIC(s). The information in this table can be used to determine how to program each interrupt.

Table 2-3 Interrupt Definitions

Interrupt	Description
INTR	Processor interrupt
NMI	NMI from DISMIC to processor
IRQ0/ MIRQ0	Baseboard interrupt request 0, connected to input 2 of the I/O APIC. NOTE: For proper operation, the BIOS must set the “IRQ0 enable” bit in PIIX3 register 70h during initialization.
IRQ1	Keyboard
IRQ3	Serial port A or B interrupt from National 87308VUL Super I/O device, user-configurable.
IRQ4	Serial port A or B interrupt from National 87308VUL Super I/O device, user-configurable.
IRQ5	Parallel port
IRQ6	Floppy disk
IRQ7	Parallel port
IRQ8_L	RTC
IRQ9	
IRQ10	
IRQ11	
IRQ12	Mouse interrupt from National 87308VUL Super I/O
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	
MIRQ1	Additional IDE interrupt from secondary channel IDE devices 0 and 1 (no secondary IDE channel on B440FX DP Server)
PCI_INTA_L	PCI Interrupt signal A from PIIX3. Wired to PCI-0 slot 1 INTA_L, PCI-0 slot 2 INTD_L, PCI-0 slot 3 INTC_L, PCI-0 slot 4 INTB_L, PCI-1 slot 1 INTA_L, and PCI-1 slot 2 INTD_L. This interrupt is also used by the USB controller.

PCI_INTB_L	PCI Interrupt signal B from PIIX3. Wired to PCI-0 slot 1 INTB_L, PCI-0 slot 2 INTA_L, PCI-0 slot 3 INTD_L, PCI-0 slot 4 INTC_L, PCI-1 slot 1 INTB_L, and PCI-1 slot 2 INTA_L. This interrupt is also used by the SCSI controller.
PCI_INTC_L	PCI Interrupt signal C from PIIX3. Wired to PCI-0 slot 1 INTC_L, PCI-0 slot 2 INTB_L, PCI-0 slot 3 INTA_L, PCI-0 slot 4 INTD_L, PCI-1 slot 1 INTC_L, and PCI-1 slot 2 INTB_L. This interrupt is also used by the Network controller.
PCI_INTD_L	PCI Interrupt signal D from PIIX3. Wired to PCI-0 slot 1 INTD_L, PCI-0 slot 2 INTC_L, PCI-0 slot 3 INTB_L, PCI-0 slot 4 INTA_L, PCI-1 slot 1 INTD_L, PCI-1 slot 2 INTC_L.
SMI_L	System Management Interrupt. General-purpose error indicator from a control PAL that provides an SMI_L from non-traditional error sources (PERR_L, SERR_L, and others).

2.6.8 Super I/O Subsystem

The National Semiconductor 87308VUL Super I/O device contains all of the necessary circuitry to control two serial ports, one IEEE 1284-compatible parallel port, a floppy disk, and a PS/2-compatible keyboard and mouse. The B440FX DP Server provides connector interfaces for all of the above. The B440FX DP Server employs a configuration of the 87308VUL Super I/O chip referred to as Plug and Play (PnP) baseboard mode, which provides an appropriate set of default values for all registers on power-up, at a base address that differs from full ISA PnP compliance. Hardware strapping of the 87308VUL signal pins, pulled high or low on the baseboard, determines the operating mode and base address of the device on power-up, as shown in the following table. The 87308VUL Super I/O also provides general-purpose I/O (GPIO) bits that power up as inputs. Some of these bits are used by server management hardware, and must be properly configured by the BIOS.

2.6.8.1 Serial Ports

One of the two 9-pin D-Sub connectors (Serial port A), along with the VGA connector (described later in this chapter), is stacked under the parallel port connector. The Serial port B connector, which is an optional item, appears as bulkhead mounted. The baseboard supplies a 10 pin header for cabling serial B to the bulkhead.

Each serial port can be set to one of four different COMx ports, and can be enabled separately. When enabled, each port can be programmed to generate edge or level sensitive interrupts. When disabled, serial port interrupts are available to add-in cards.

2.6.8.2 Parallel Port

The National 87308VUL Super I/O provides one IEEE 1284-compatible (ECP/EPP) 25-pin bi-directional parallel port. Hardware strapping enables the parallel port, and sets the port address and interrupt. When disabled, the interrupt is available to add-in cards.

The 25/15 pin connector stacks the parallel port connector over the VGA and Serial A connectors. The pinout is shown in Chapter 8.

2.6.8.3 Floppy Port

The FDC on the National 87308VUL Super I/O is functionally compatible with 82077SL, 82077AA, and 8272A floppy disk controllers. The baseboard provides the 24 MHz clock and termination resistor package. All other FDC functions are integrated into the National 87308VUL Super I/O chip including PLL separator and 16-byte FIFO. The pinout for floppy connector on the baseboard can be found in Chapter 8.

2.6.8.4 Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single housing. Both connectors are functionally equivalent and the system will recognize the keyboard or the mouse regardless of the connector.

2.7 Secondary PCI Subsystem (PCI-1)

The DECchip 21152 PCI-to-PCI bridge device extends the electrical capacity of PCI-0 to form a secondary PCI segment referred to as PCI-1. All PCI transactions on PCI-0 that fall within specified address ranges are forwarded to PCI-1 by the 21152. The 21152 is a 3.3V CMOS, 160-pin, PQFP. For a complete functional specification of the PCI-to-PCI bridge device, refer to the *DECchip 21152 PCI-to-PCI Bridge Data Sheet*

PCI-1 contains the following embedded devices and PCI expansion connectors:

- Adaptec 7880† SCSI host adapter
- Intel 82557 PCI Fast Ethernet controller
- Cirrus Logic CL-GD54M40† VGA controller
- Two PCI expansion slots

2.7.1 PCI-1 Arbitration

PCI-1 supports four PCI masters: slot 1, slot 2, SCSI chip, and network controller. The video chip is a PCI slave which never requires bus mastering, it therefore does not need to arbitrate for PCI-1 access. The four PCI masters, however, must arbitrate for PCI access using resources supplied by the PCI-to-PCI bridge.

Table 2-4 PCI-1 Arbitration Connections

DEC 21052 Arbiter Signals	Device
REQ3_L / GNT3_L	82557 chip
REQ2_L / GNT2_L	SCSI
REQ1_L / GNT1_L	PCI-1 Slot 2
REQ0_L / GNT0_L	PCI-1 Slot 1

2.7.2 SCSI Subsystem

The PCI-1 provides an embedded Adaptec AIC-7880 SCSI host adapter. The AIC-7880 contains a double-speed SCSI controller and full-featured PCI bus master interface in a 160-pin PQFP. The AIC-7880 can support 8- or 16-bit Fast SCSI, providing 10MB/s or 20MB/s throughput, or double-speed SCSI that can burst data at 20MB/s or 40MB/s. Sustained throughput may vary depending upon the number and type of SCSI devices connected to the SCSI bus. As a PCI 2.0 bus master, the AIC-7880 supports burst data transfers on PCI up to the maximum rate of 133MB/s using the on-chip 256 byte FIFO.

2.7.2.1 Adaptec 7880 PCI Signals

The Adaptec AIC-7880 supports all of the required PCI 2.0 32-bit PCI signals including the PERR_L and SERR_L functions. Full PCI parity is maintained on the entire data path through the chip. The device also takes

advantage of PCI interrupt signaling capability, which is hardwired to PCI_INTB_L on the B440FX DP Server. The figure below shows the PCI signals supported by the AIC-7880.

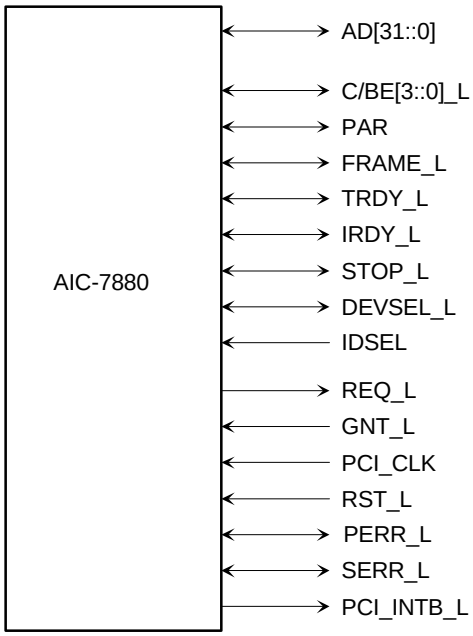


Figure 2-10 Embedded SCSI PCI Signals

2.7.2.2 Adaptec AIC-7880 Supported PCI Commands

The AIC-7880 supports the PCI commands listed in the following table:

Table 2-5 Embedded SCSI Supported PCI Commands

		AIC-7880 Support	
C/BE [3:0] _L	**Command Type**	**Target**	**Master**
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0110	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	Yes

0111	Memory Write	Yes	Yes
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	**	Yes
1101	Dual Address Cycle	No	Yes
1110	Memory Read Line	**	Yes
1111	Memory *Write and Invalidate	*	Yes

* Defaults to Memory Write
** Defaults to Memory Read

The extensions to memory commands (Memory Read Multiple, Memory Read Line, and Memory Write and Invalidate) work with the cache line size register to give the cache controller advance knowledge of the minimum amount of data to expect. The decision to use either the Memory Read Line or Memory Read Multiple command is determined by a bit in the configuration space command register for this device.

2.7.2.3 SCSI Interface

The AIC-7880 offers 8-bit or 16-bit SCSI operation at data transfer rates of 10, 20, or 40MB/s (although sustained transfer rates may vary depending on the number and type of SCSI devices connected to the SCSI bus). It also offers active negation outputs, controls for external differential transceivers, a disk activity output, and a SCSI terminator power-down control. Active negation outputs reduce the chance of data errors by driving both polarities of the SCSI bus, avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48 mA single-ended SCSI bus with no additional drivers. Synchronous SCSI can handle up to 15 REQs.

2.7.2.3.1 SCSI Bus

The SCSI data bus is 8- or 16-bits wide with odd parity generated per byte. Its control signals are the same for either width. To accommodate 8-bit devices on a 16-bit wide SCSI bus, the AIC-7880 assigns the highest arbitration priority to the low byte of the 16-bit word. This way, 16-bit targets can be mixed with 8-bit if the 8-bit devices are placed on the low data byte. For 8-bit mode, the unused high data byte is self-terminated and need not be connected. During chip power-down, all inputs are disabled to reduce power consumption.

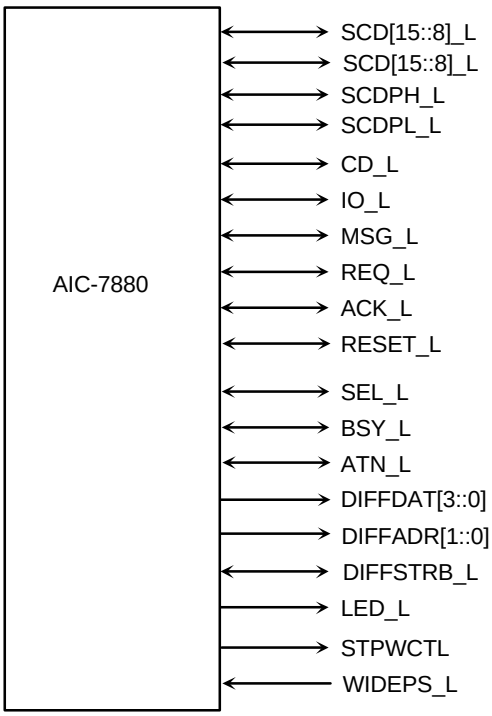


Figure 2-11 SCSI Bus Signals

For more information on the functional architecture of this device, refer to the *Adaptec AIC-7880 PCI Bus Master Single-chip SCSI Host Adapter Data Book* For the pinout, see Chapter 8.

2.7.3 PCI Video

The B440FX DP Server uses the next generation of integrated video controller and support circuitry: Cirrus Logic CL-GD54M40 32-bit VGA Graphics Accelerator chip containing an SVGA video controller, Clock Generator, and 80 MHz RAMDAC in a 160-pin PQFP. One 256K x 16 DRAM chip provides 512KB of 60ns video memory, and can be expanded to 1MB for improved performance and more video modes. The CL-GD54M40 supports up to 1280 x 1024 resolution and up to 64K colors.

This SVGA subsystem supports analog VGA monitors, single and multi-frequency, interlaced and non-interlaced, up to 87 Hz vertical retrace frequency. The connector is a standard 15-pin VGA connector.

The CL-GD54M40 supports the following PCI commands:

Table 2-6 Video Chip Supported PCI Commands

		CL-GD54M40 Support	
C/BE_L[3:0]	**Command Type**	**Target**	**Master**
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0110	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	No
0111	Memory Write	Yes	No
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No	No
1101	Dual Address Cycle	No	No
1110	Memory Read Line	No	No
1111	Memory Write and Invalidate	No	No

2.7.3.1 Video Modes

TheCL-GD54M40 provides all standard IBM VGA modes. With 512KB of video memory, the standard B440FX DP Server goes beyond standard VGA support. The following tables show all supported video modes using 512KB and 1MB of video memory. An additional 512KB is user-installable. The tables also show the standard and extended modes that the chip supports, including the number of colors, palette size (e.g., 16 colors out of 256K colors), resolution, pixel frequency, and scan frequencies.

Table 2-7 Standard VGA Modes

Mode(s) in Hex	Bits Per Pixel	Colors (number /palette size)	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	4	16/256K	360 X 400	14	31.5	70
2, 3	4	16/256K	720 X 400	28	31.5	70
4, 5	4	4/256K	320 X 200	12.5	31.5	70
6	4	2/256K	640 X 200	25	31.5	70
7	4	Mono	720 X 400	28	31.5	70
D	4	16/256K	320 X 200	12.5	31.5	70
E	4	16/256K	640 X 200	25	31.5	70
F	4	Mono	640 X 350	25	31.5	70
10	4	16/256K	640 X 350	25	31.5	70
11	4	2/256K	640 X 480	25	31.5	60
12	4	16/256K	640 X 480	25	31.5	60
12+	4	16/256K	640 X 480	31.5	37.5	75
13	8	256/256K	320 X 200	12.5	31.5	70

Table 2-8 Extended VGA Modes

Mode(s) in Hex	BPP	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
14, 55	8	16/256K	1056 X 400	41.5	31.5	70
54	8	16/256K	1056 X 350	41.5	31.5	70
58, 6A	8	16/256K	800 X 600	40	37.8	60
58, 6A	8	16/256K	800 X 600	49.5	46.9	75
5C	8	256/256K	800 X 600	36	35.2	56
5C	8	256/256K	800 X 600	40	37.9	60
5C	8	256/256K	800 X 600	49.5	46.9	75
5D	8	16/256K (interlaced)	1024 X 768	44.9	35.5	87
5D	8	16/256K	1024 X 768	65	48.3	60
5D	8	16/256K	1024 X 768	75	56	70
5D	8	16/256K	1024 X 768	78.7	60	75
5F	8	256/256K	640 X 480	25	31.5	60
5F	8	256/256K	640 X 480	31.5	37.5	75
60*	8	256/256K (interlaced)	1024 X 768	44.9	35.5	87
60*	8	256/256K	1024 X 768	65	48.3	60
60*	8	256/256K	1024 X 768	75	56	70
60*	8	256/256K	1024 X 768	78.7	60	75
64*	16	64K	640 X 480	25	31.5	60
64*	16	64K	640 X 480	31.5	37.5	75
65*	16	64K	800 X 600	36	35.2	56
65*	16	64K	800 X 600	40	37.8	60
65*	16	64K	800 X 600	49.5	46.9	75
66*	16	32K Direct/256 Mixed	640 X 480	25	31.5	60
66*	16	32K Direct/256 Mixed	640 X 480	31.5	37.5	75

67*	16	32K Direct/256 Mixed	800 X 600	40	37.8	60
67*	16	32K Direct/256 Mixed	800 X 600	49.5	46.9	75
6C*	16	16/256K (interlaced)	1280 X 1024	75	48	87

* Requires 1MB video memory option.

2.7.4 Network Interface Controller (NIC)

The baseboard supports a 10Base-T/100Base-TX network subsystem based on the Intel 82557™ Fast Ethernet PCI bus controller. The National DP838040† and DP83223† devices, along with other discrete components, provide the physical layer interface. The following diagram illustrates the architecture of the network controller subsystem:

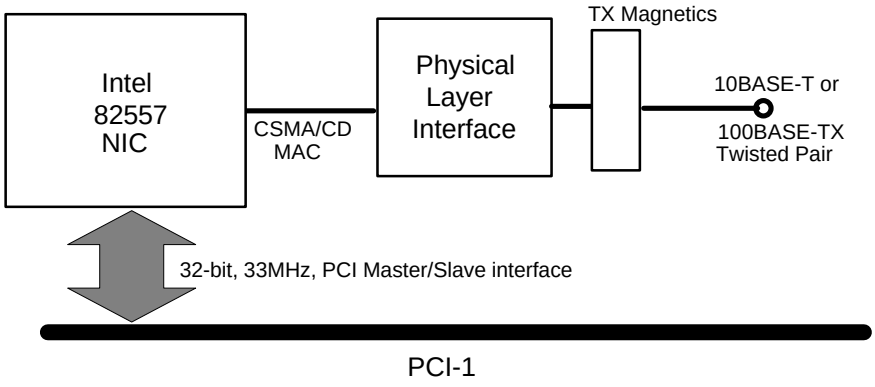


Figure 2-12 Network Controller Subsystem

The 82557 is a highly integrated PCI LAN controller in a 160-pin QFP package for 10 or 100Mbps fast ethernet networks. As a PCI bus master, the 82557 can burst data at up to 132MB/s. This high-performance bus master interface can eliminate the intermediate copy step in receive and transmit frame copies, resulting in faster frame processing. The network operating system communicates with the 82557 using a memory-mapped I/O interface, PCI_INTC_L, and two large receive and transmit FIFOs. These prevent data overruns or underruns while waiting for access to the PCI bus, and enable back-to-back frame transmission within the minimum 960ns inter-frame spacing. The following figure shows the PCI signals supported by the 82557.

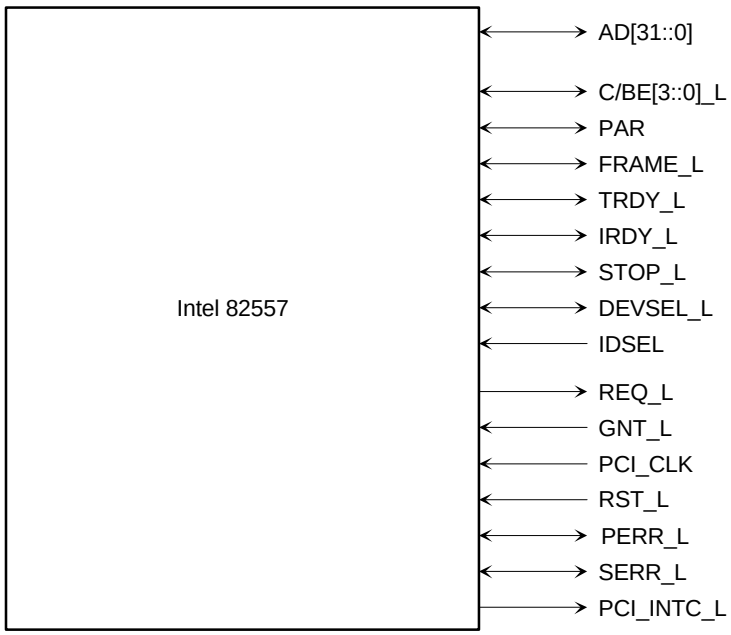


Figure 2-13 Embedded NIC PCI Signals

2.7.4.1 Supported Network Features

The 82557 contains an IEEE MII compliant interface to the components necessary to implement a IEEE 802.3 100Base-TX network connection. The B440FX DP Server supports the following features of the 82557 controller:

- Glueless 32-bit PCI bus master interface (direct drive of bus), compatible with PCI Bus Specification, revision 2.1
- Chained memory structure similar to the Intel 82596™, with improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- On-chip counters for network management
- Autodetect and autoswitching for 10Mbps or 100Mbps network speeds
- Support for both 10Mbps and 100Mbps networks, full or half duplex-capable, with back-to-back transmit at 100Mbps

The 82557 connects to the National DP83840 and DP83223 components which provide the physical layer for the LAN controller. In addition, a magnetic component is provided that terminates to the 100Base-TX connector interface. Also included is support to enable the National DP83840 to switch between 10Mbps and 100Mbps operation. A flash device stores the network ID.

2.7.4.2 NIC Status LEDs

The National DP83840 drives LEDs to indicate the transmit/receive activity on the LAN, a valid link to the LAN, and 10/100Mbps operation. The location and function of each LED is shown in the following figure.

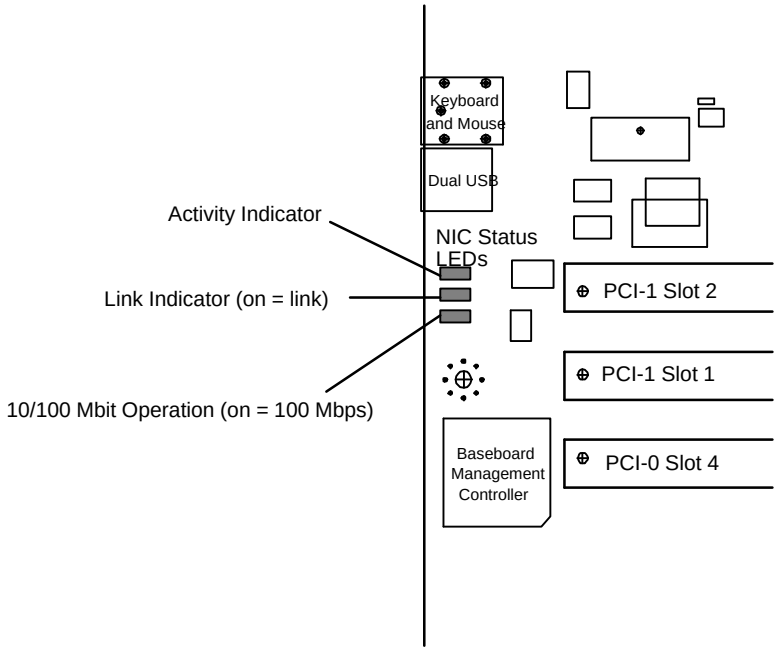


Figure 2-14 NIC Status LEDs

2.8 Server Management

The B440FX DP Server Management features are implemented using the following three microcontrollers and one ASIC:

- Baseboard Management Microcontroller (BMC)
- Front Panel Microcontroller (FPC)
- Processor Board Controller (PBC)
- Distributed Integrated Server Management Interface Chip (DISMIC)

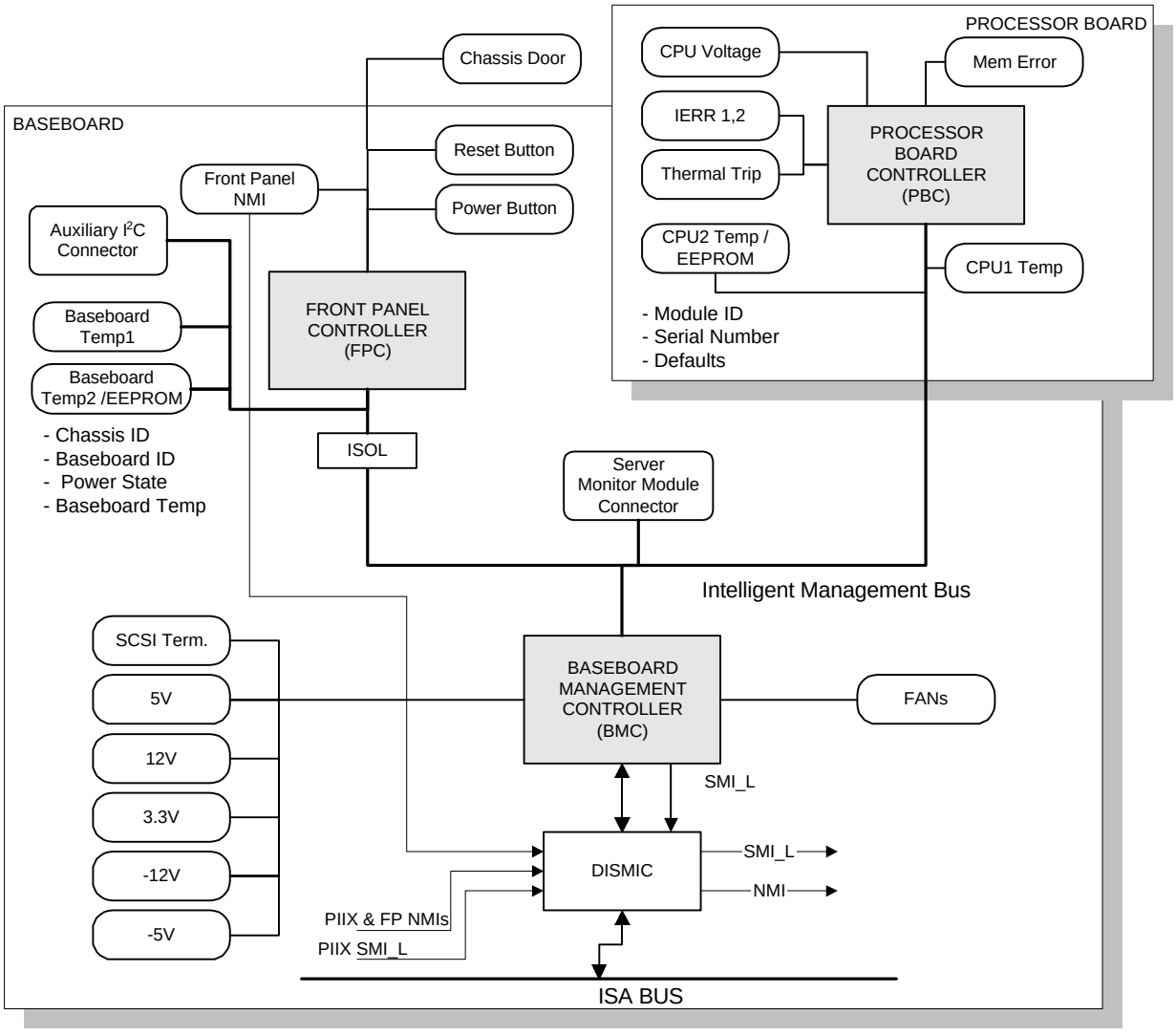


Figure 2-15 B440FX DP Server Management Architecture

2.8.1 Baseboard Management Microcontroller (BMC)

The BMC is an 8051-compatible microcontroller located on the baseboard. It monitors baseboard power supply and SCSI termination voltages by using an onboard Analog to Digital Converter (ADC). It checks the status of the fan failure and the front panel NMI request and monitors system temperature sensors using the I^2C-based intelligent management bus. When any monitored parameter is outside defined thresholds, the BMC generates SMI_L. The BMC also provides general-purpose I/O (GPIO) functions, and acts as the primary communications gateway to the FPC, PBC, and DISMIC by providing support routines for I^2C and ISA communications.

An EEROM associated with the secondary baseboard temperature sensor contains the Chassis ID, Baseboard ID, Power State, and Baseboard Temperature during power-off conditions. These values are managed by the BMC via I^2C.

2.8.2 Front Panel Microcontroller (FPC)

The FPC, located on the baseboard, manages system power on/off control, system reset, chassis intrusion monitoring, and an external I^2C interface. The device is powered from the +5V standby power supply, enabling it to stay alive when system power is off. The FPC controls main power to the baseboard and processor board, and is responsible for monitoring all sources of power control both on and off the baseboard, including the Front Panel, Server Manager module, PIIX3, and RTC power control signals.

2.8.3 I^2C Isolation Buffers

Isolation buffers, between the temperature sensors on the baseboard and the rest of the I^2C bus, keep the bus alive even though the main +5V power supply is unavailable. This allows the FPC to communicate with its I^2C EEROM (in the secondary baseboard temperature sensor) at all times.

2.8.4 Processor Board Management Microcontroller (PBC)

The PBC monitors processor voltage levels, determines DIMM configuration, monitors processor thermal trip and internal error signals, and manages two I^2C thermal sensors located near each processor.

Fault Resilient Booting (FRB) is managed by the PBC, which controls the ability to boot using either processor in the event of a catastrophic processor failure. On power-up, a timer starts within the PBC that can only be stopped by a healthy processor using the GPIO bit, FRB_TMRHLT_L, on the 87308VUL Super I/O chip. If processor 0 fails to halt the FRB timer before time-out, the microcontroller asserts STOP_FLUSH to the processor and asserts FRB_RST_L for 10ms. When the system comes out of reset, processor 0 is unable to act as the boot processor allowing the other processor to take over the boot process.

The PBC uses the I^2C bus for communication with the baseboard, indicating status and error information using a semaphore protocol defined in the *Intelligent Management Bus V1.0 Communications Protocol Specification.* The PBC manages the EEROM associated with the secondary temperature sensor on the processor board which contains the Module ID, Serial Number, and other information that remains intact during power-off.

2.8.5 Distributed Integrated Server Management Interface Chip (DISMIC)

The three controllers communicate with each other on the intelligent management bus. Communication between this distributed controller network, the SMI handler, and the Systems Management Software (SMS) is done with the ISA host interface provided by the DISMIC. The DISMIC and BMC act as a bridge between the host server and devices on the intelligent management bus. In addition, the DISMIC provides a mailbox register interface designed to work with SMS and SMI_L handler code across the ISA interface. The DISMIC also gates and redirects SMI_L and NMI to generate SERR_L, and performs other miscellaneous logic functions (e.g. logic control).

2.9 System Reset Control

The PIIX3 asserts reset to the host PCI bridge, which propagates reset to the I/O system. The PMC and PIIX3 provide software-controlled reset capability. The FPC, which monitors and controls system power supplies, provides a signal that indicates when power is stable to the system. The reset architecture is designed to accommodate three ways to reset the system:

- Power-up (system) reset
- Programmed (warm) reset
- Soft (keyboard) reset

2.9.1 Power-up Reset

Power-up reset occurs on the initial application of power to the system. The FPC manages a P6_PWR_GOOD signal that indicates stable power-up reset conditions to the Pentium Pro processor(s). The PBC is held in reset until the P6_POWER_GOOD assertion, when processor clocks are started. On power-up reset, all processors in the system perform their internal BIST. A timer begins to run in the FPC that supports a Fault Resilient Booting (FRB) mechanism allowing the system to boot if one processor fails. After successful processor initialization, the PMC is reset, and reset propagates throughout the I/O system, which allows the system to start.

2.9.2 Programmed Reset

Programmed Reset may be initiated by software. Reset control is provided by registers in the PMC and PIIX3. Reset may also be initiated by the FPC and PBC, but this is not recommended. For this implementation, the 82440FX PCIset documentation recommends that you use the PIIX3 reset control register for programmed resets.

2.9.3 Soft Reset

Soft resets may be generated by the keyboard controller in the 87308VUL Super I/O chip, the PMC, and the PIIX3 to the reset PLD. Soft resets preserve all cache contents but reset the bus and processors.

2.9.4 Reset Signal Flow

Reset propagates throughout the system as shown in the following figure:

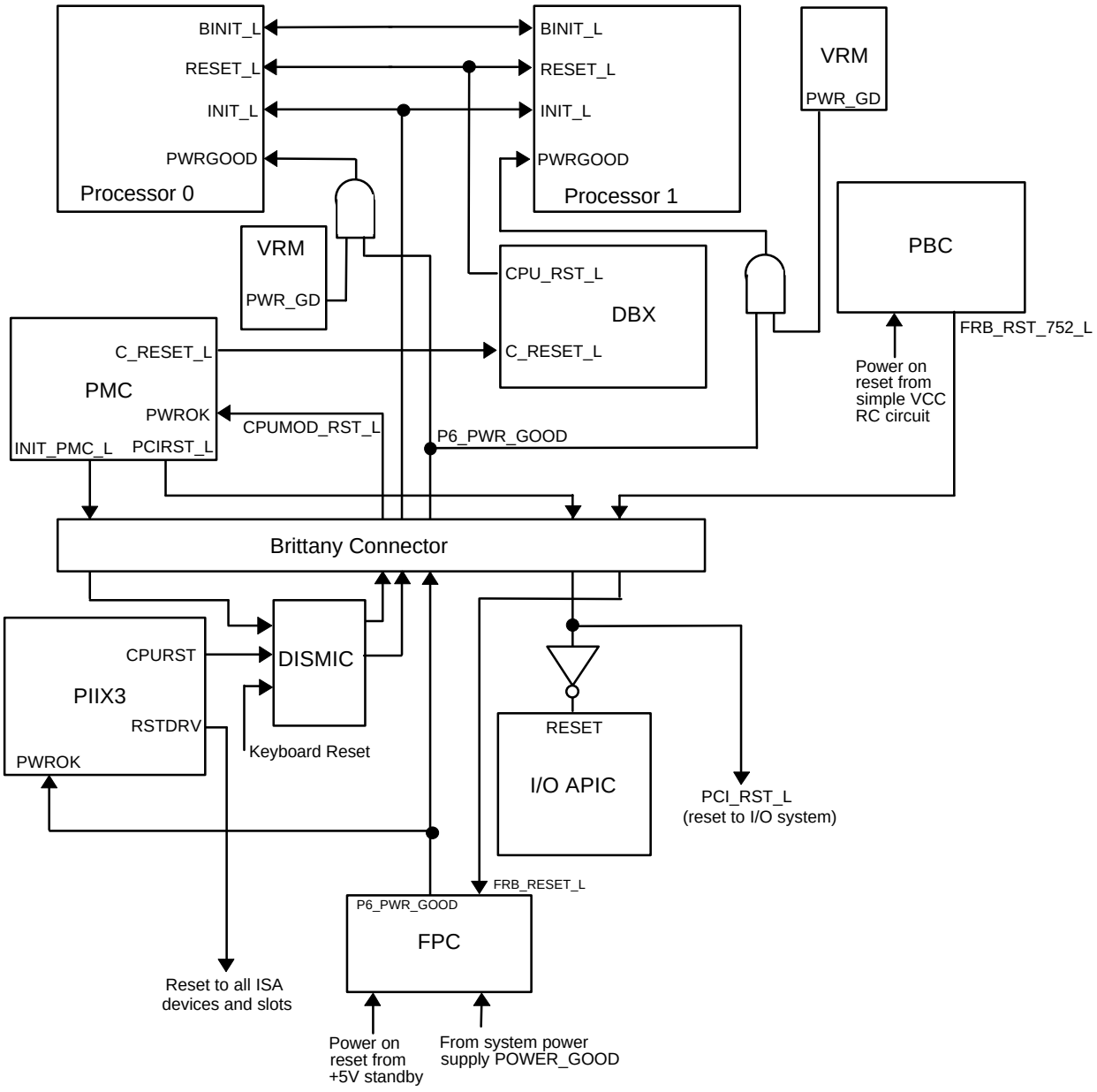


Figure 2-16 System Reset Flow

3. MEMORY AND OTHER RESOURCE MAPPINGS

3.1 Memory Maps

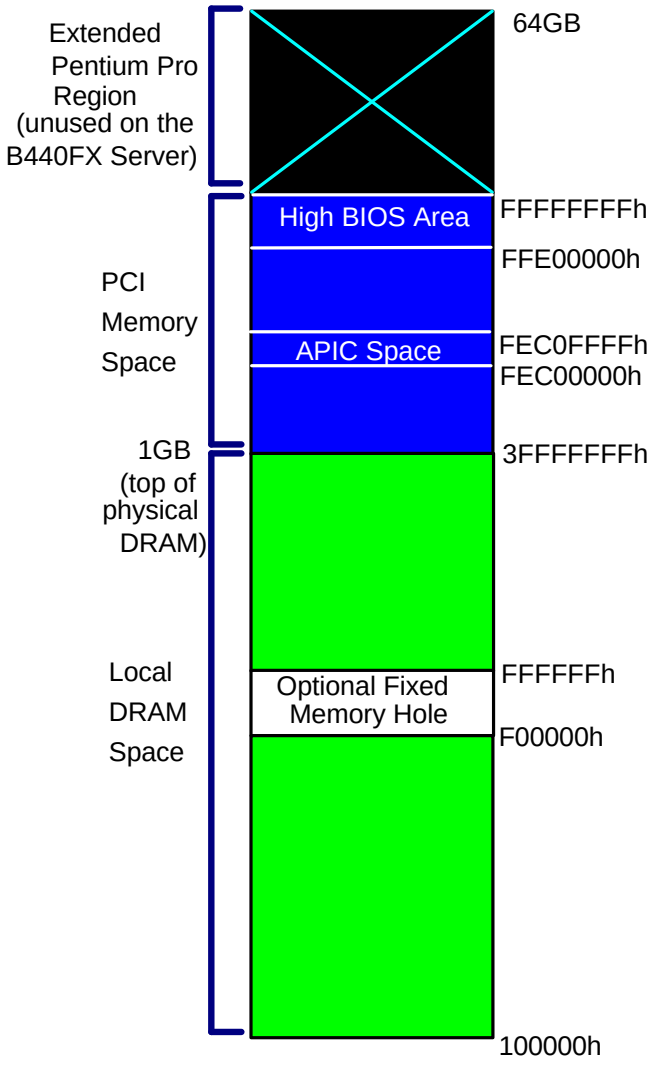


Figure 3-1 Extended Memory Map

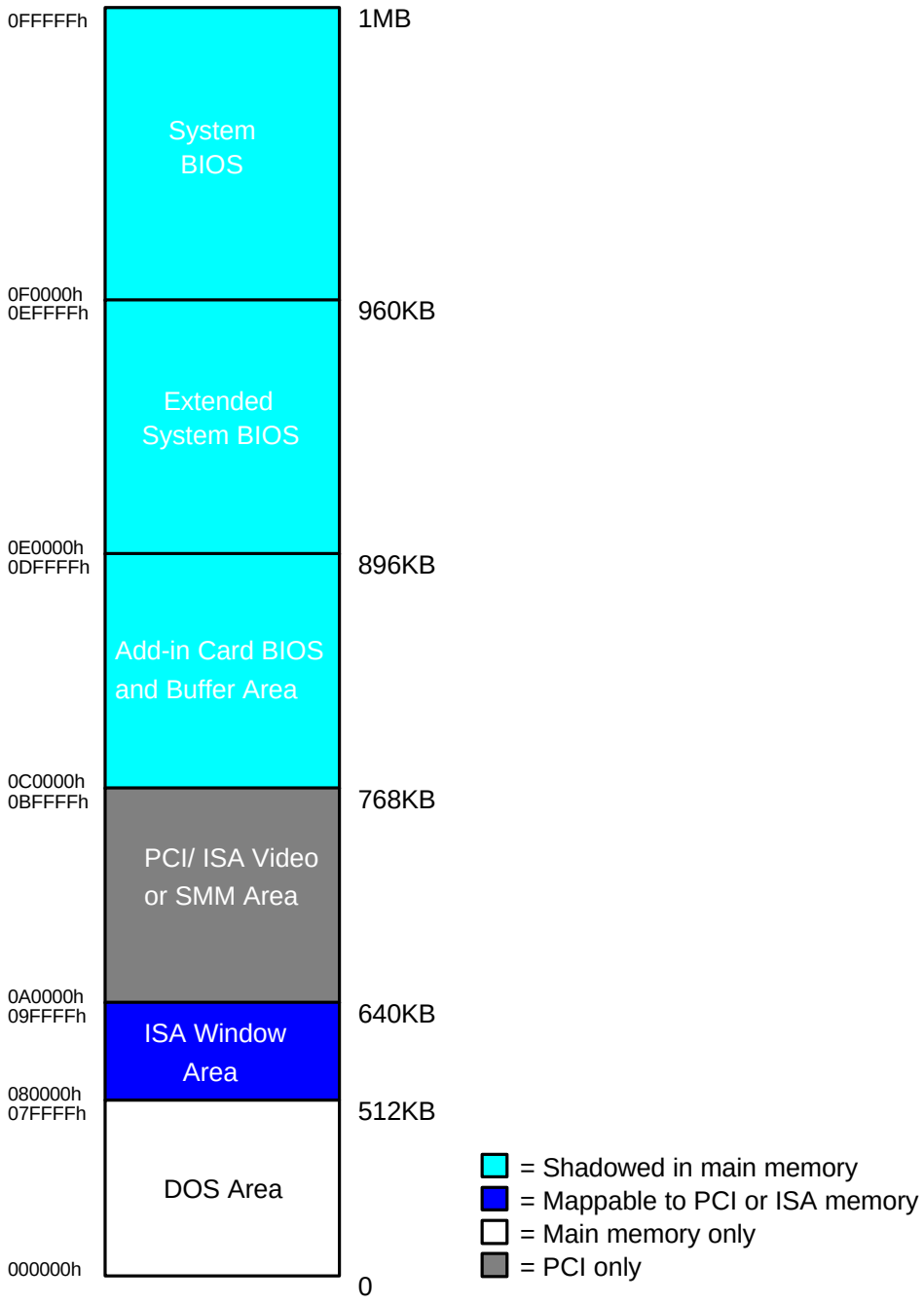


Figure 3-2 DOS Compatible Memory Regions

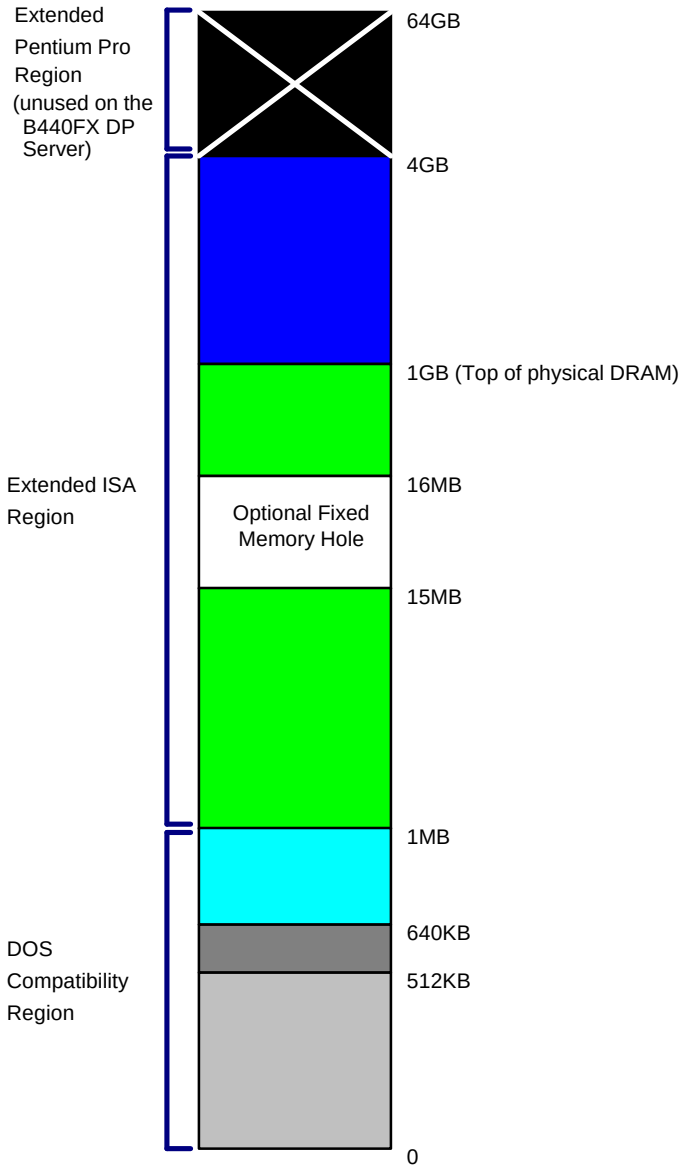


Figure 3-3 Pentium Pro Processor Memory Address Space

3.2 I/O Map

Table 3-1 I/O Map

ADDRESS(ES)	RESOURCE	NOTES
0000h - 000Fh	DMA Controller 1	PIIX3
0020h - 0021h	Interrupt Controller 1	PIIX3
002Eh - 002Fh	Super I/O Index and Data Ports	
0040h - 0043h	Programmable Timer	PIIX3
0060h, 0064h	Keyboard Controller	Keyboard chip select from National 87308VUL Super I/O
0061h	NMI Status & Control Register	PIIX3
0070h	NMI Mask (bit 7) & RTC Address (bits 6:0)	Write Only.
0071h	Real Time Clock (RTC)	RTC chip select from National 87308VUL Super I/O
0080h - 0081h	BIOS Timer	
0080h - 008Fh	DMA Low Page Register	PIIX3
0092h	System Control Port A (PC-AT control Port)	PIIX3 does not alias this port in DMA range.
0094h	Video Display Controller	
00A0h - 00BFh	Interrupt Controller 2	PIIX3
00C0h - 00DFh	DMA Controller 2	PIIX3
00F0h	Clear NPX error	Resets IRQ13
00F8h - 00FFh	x87 Numeric Coprocessor	
0102h	Video Display Controller	
0170h - 0177h	Secondary Fixed Disk Controller (IDE)	
01F0h - 01F7h	Primary Fixed Disk Controller (IDE)	
0200h - 0207h	Game I/O Port	Not used
0220h - 022Fh	Serial Port A	
0238h - 023Fh	Serial Port B	

0278h - 027Fh	Parallel Port 3	
02E8h - 02EFh	Serial Port B	
02F8h - 02FFh	Serial Port B	
0338h - 033Fh	Serial Port B	
0370h - 0375h	Secondary Floppy	
0378h - 037Fh	Parallel Port 2	
03B4h - 03BAh	Monochrome Display Port	
03BCh - 03BFh	Parallel Port 1 (Primary)	
03C0h - 03CFh	Video Display Controller	
03D4h - 03DAh	Color Graphics Controller	
03E8h - 03EFh	Serial Port A	
03F0h - 03F5h	Floppy Disk Controller	
03F6h - 03F7h	Primary IDE - Sec. Floppy	
03F8h - 03FFh	Serial Port A (Primary)	
0400h - 043Fh	DMA Controller 1, Extended Mode Registers.	PIIX3
0461h	Extended NMI / Reset Control	PIIX3
0462h	Software NMI	PIIX3
0480h - 048Fh	DMA High Page Register.	PIIX3
04C0h - 04CFh	DMA Controller 2, High Base Register.	
04D0h - 04D1h	Interrupt Controllers 1 and 2 Control Register.	
04D4h - 04D7h	DMA Controller 2, Extended Mode Register.	
04D8h - 04DFh	Reserved	
04E0h - 04FFh	DMA Channel Stop Registers	
0678h - 067Ah	Parallel Port (ECP)	
0778h - 077Ah	Parallel Port (ECP)	
07BCh - 07BEh	Parallel Port (ECP)	

0800h - 08FFh	NVRAM	
0CA4	PCI to IRQ rerouter control	PCI_INTB (upper nibble), PCI_INTA (lower nibble)
0CA5	PCI to IRQ rerouter control	PCI_INTD (upper nibble), PCI_INTC (lower nibble)
0CA6h - 0CA7h	Reserved	
0CA9h	DISMIC Data Register	Server management mailbox registers.
0CAAh	DISMIC Control/Status Register	
0CABh	DISMIC Flags Register	
0C84h	Board Revision Register	
0C85h - 0C86h	BIOS Function Control	
	PCI Interrupt Rerouter Control	
0CF8h	PCI CONFIG_ADDRESS Register	Located in PMC
0CF9h	PMC Turbo and Reset control	PIIX3
0CFCh	PCI CONFIG_DATA Register	Located in PMC
46E8h	Video Display Controller	
xx00 - xx1F*	SCSI registers	Refer to SCSI chip doc.

3.3 PCI Map

Table 3-2 PCI Configuration IDs and Device Numbers

IDSEL	PMC DEVICE #	PCI-0 DEVICE	21152 DEVICE #	PCI-1 DEVICE
31	10100b	21152 PCI-to-PCI Bridge	01111b	CL-GD54M40 Video chip
30	10011b		01110b	
29	10010b	PIIX3	01101b	
28	10001b		01100b	
27	10000b	PCI-0 Slot 4	01011b	PCI-1 Slot 2
26	01111b	PCI-0 Slot 3	01010b	82557 Network chip
25	01110b	PCI-0 Slot 2	01001b	
24	01101b	PCI-0 Slot 1	01000b	PCI-1 Slot 1
23	01100b		00111b	
22	01011b		00110b	
21	01010b		00101b	AIC-7880 SCSI chip
20	01001b		00100b	
19	01000b		00011b	
18	00111b		00010b	
17	00110b		00001b	
16	00101b		00000b	
15	00100b		n/a	
14	00011b		n/a	
13	00010b		n/a	
12	00001b		n/a	
11	00000b	Hardwired internally to PMC	n/a	

3.4 DMA Channels

Table 3-3 DMA Channel Mapping

CHANNEL	FUNCTION
0	available for add-in board
1	available for add-in board
2	On-Board Floppy Controller
3	available for add-in board
4	DMA Controller
5	available for add-in board
6	available for add-in board
7	ISA IDE DMA Transfers

3.5 Interrupts

Table 3-4 Interrupt Mapping

INTERRUPT	DESCRIPTION
INTR	Processor interrupt
NMI	NMI from DISMIC to processor
IRQ0/ MIRQ0	Motherboard interrupt request 0, connected to input 2 of the I/O APIC. NOTE: For proper operation, the BIOS must set the “IRQ0 enable” bit in PIIX3 register 70h during initialization.
IRQ1	Keyboard
IRQ3	Serial port A or B interrupt from National 87308VUL Super I/O device, user-configurable.
IRQ4	Serial port A or B interrupt from National 87308VUL Super I/O device, user-configurable.
IRQ5	Parallel port
IRQ6	Floppy disk
IRQ7	Parallel port
IRQ8	RTC
IRQ9	

continued

INTERRUPT	DESCRIPTION
IRQ10	
IRQ11	
IRQ12	Keyboard/mouse interrupt from National 87308VUL Super I/O
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	
PCI_INTA	PCI Interrupt signal A from PIIX3. Wired to PCI-0 slot 1 INTA, PCI-0 slot 2 INTD, PCI-0 slot 3 INTC, PCI-0 slot 4 INTB, PCI-1 slot 1 INTA, and PCI-1 slot 2 INTD. This interrupt is also used by the USB controller.
PCI_INTB	PCI Interrupt signal B from PIIX3. Wired to PCI-0 slot 1 INTB, PCI-0 slot 2 INTA, PCI-0 slot 3 INTD, PCI-0 slot 4 INTC, PCI-1 slot 1 INTB, and PCI-1 slot 2 INTA. This interrupt is also used by the SCSI controller.
PCI_INTC	PCI Interrupt signal C from PIIX3. Wired to PCI-0 slot 1 INTC, PCI-0 slot 2 INTB, PCI-0 slot 3 INTA, PCI-0 slot 4 INTD, PCI-1 slot 1 INTC, and PCI-1 slot 2 INTB. This interrupt is also used by the Network controller.
PCI_INTD	PCI Interrupt signal D from PIIX3. Wired to PCI-0 slot 1 INTD, PCI-0 slot 2 INTC, PCI-0 slot 3 INTB, PCI-0 slot 4 INTA, PCI-1 slot 1 INTD, PCI-1 slot 2 INTC.
SMI	System Management Interrupt. General-purpose error indicator from a control PAL that provides an SMI from non-traditional error sources (PERR, SERR, and others).

3.6 BIOS Map

Table 3-5 Flash Map Summary

Length	Base Address	Usage
04000h	*0FFFEC000h	Recovery BIOS
10000h	0FFFF0000h	BIOS block
10000h	0FFFD0000h	BIOS block
10000h	0FFFC0000h	BIOS block
10000h	0FFFA0000h	Language block
10000h	0FFFB0000h	BIOS block
08000h	0FFFE0000h	BIOS block
02000h	*0FFFEA000h	ESCD , DMI-GPNV and SCSI storage area
02000h	*0FFFE8000h	Event Logs
02000h	0FFF80000h	User Binary (Shadowed @ 0EE000h in runtime)
0E000h	0FFF82000h	Reserved
10000h	0FFF90000h	Reserved

* These block base addresses are always visible to programs both at the physical address shown, as well as the corresponding address below 1MB.

3.7 CMOS Map

Table 3-6 CMOS Map Summary

LOCATION(S)	DESCRIPTION
10h	Floppy Drive A: and B: Type
11h	Run time Info
12h	Hard Disk C: and D: Type (Filled In By POST)
13h	Typematic rate programming
14h	Equipment information
15h - 16h	Low and High Bytes Of Base Memory In KB
17h - 18h	IBM-compatible Low and High Bytes Of Extended Memory In KB
19h	Hard Disk C: - F: Auto-configure
1Ah	Hard Disk C: - F: Initialization Time-out
1Bh	Hard Disk C: - F: Multiple Sector Setting
1Ch	Hard Disk C: - F: Enhanced IDE and DMA Support
1Dh	Hard Disk C: - F: Translation Mode
1Eh	IDE Boot History, system base memory size Hard Disk Predelay
1Fh	Hot Key Valid Flag and Scan Code
20h	Language
21h -27h	Reserved
28h - 29h	Product-dependent Shadow Control Bytes 1 and 2
2Ah - 2Dh	Product-dependent CPU Data Bytes 1 - 4
2Eh - 2Fh	Standard CMOS Checksum High and Low Bytes
30h - 31h	IBM-compatible Extended Mem Low and High Bytes (Post) In KB

continued

LOCATION(S)	DESCRIPTION
32h	Hard Disk Reset Flag, and Century Byte
33h	Miscellaneous functions
34h	Low and High Bytes Of Extended Memory (Post) In 64KB
36h	Clear CMOS on boot, User Defined Bit #2, Override Watchdog Timer
37h	Reserved for OEMs
38h - 3Fh	Reserved for Intel
40h - 47h	Reserved for Intel
48h -4Fh	Reserved
50h - 5Fh	User-defined Drive Type C: - F: parameters
60h - 64h	I/O Peripheral Bytes 1 - 5
65h -6Ah	Reserved
6Bh	Product-dependent Extra Peripheral CMOS byte
6Ch - 6Fh	Product-dependent Chipset Bytes 1 - 4
70h	Processor Options
71h - 75h	Product-dependent PCI Control Bytes 1 - 5
76h -77h	Reserved
78h - 7Dh	Reserved for Power Management Bytes 1 - 6
7Eh - 7Fh	Extended CMOS Checksum High and Low Bytes

3.8 NVRAM Map

Table 3-7 NVRAM Map

START	END	DESCRIPTION
0000	1E7F	ESCD data (EISA (or ISA) and Plug-n-Play configuration data).
1E80	1EBF	64 byte blocks of 7880 SCSI configuration data for onboard device 1.
1EC0	1EFF	*N/A for Buckeye* - 64 byte blocks of 7880 SCSI configuration data for onboard device 2.
1F20	1F27	System fatal upper limits.
1F28	1F2F	System warning upper limits.
1F30	1F37	System fatal lower limits.
1F38	1F3F	System warning lower limits.
1F40	1F7F	OEM-specific usage.
1F80	1FFE	Reserved
1FFF	1FFF	Checksum for 1F00-1FFEh

4. BIOS & CONFIGURATION

The Basic Input Output System, or BIOS, is embedded software that resides in flash memory. It contains standard PC-compatible basic I/O services as well as system-specific hardware configuration routines and register defaults that are embedded in flash memory.

The term “BIOS” refers to the following:

- System BIOS. This is the system that controls basic system functionality using stored configuration values.
- Flash Memory Update utility (FMUP). This is what loads pre-defined areas of Flash memory with Setup, BIOS, and other code or data.
- Configuration Utility (CU) consisting of Flash ROM-resident setup utility and system memory-resident System Configuration utility (SCU). They provide user control of configuration values stored in NVRAM.

The following figure shows the relationship between BIOS components and register spaces. Unshaded areas are loaded into flash using FMUP.

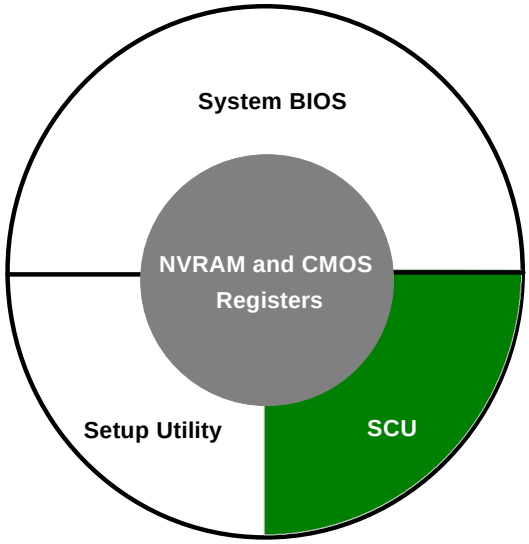


Figure 4-1 B440FX DP Server BIOS Architecture

4.1 System BIOS

The system BIOS, which provides standard PC BIOS services, is the core of the flash memory-resident portion of the BIOS. In addition, the system BIOS provides support for these specific features: security, multiple speed processor (mixing processor speeds within the same configuration is not allowed), SMP, fault resilient booting (FRB), logging of critical events, server management, I^2C, CMOS configuration RAM defaults, multiple language, defective DIMM detection and remapping, automatic detection of video adapters, greater than 16MB memory support, PCI BIOS interface, option ROM shadowing, cache state on boot, system information reporting, ECC, SMI, user-supplied BIOS, L2 cache, ISA, memory sizing, boot drive sequencing, and resource allocation.

4.1.1 Security Features

The B440FX DP Server BIOS provides a number of security features.

Table 4-1 Security Features Operating Model

MODE	ENTRY METHOD/ EVENT	ENTRY CRITERIA /QUALIFIER	BEHAVIOR	EXIT CRITERIA	AFTER EXIT
Secure mode	Keyboard Inactivity Timer, Secure Mode Button, Programming of KBC Hot-Key	User Password KBC inactivity timer (set by CU)	Screen goes blank (if enabled in Setup). Floppy writes are disabled (if selected in setup). Power and Reset switches on the front panel are disabled. No mouse or keyboard input is accepted.	User Password	Video is restored. Floppy writes are enabled. Power and Reset switches are enabled. Keyboard and mouse inputs are accepted.
Secure boot	Power On/Reset	User Password Secure Boot Enabled in SCU	Boots drive C if drive A is empty, prompts for Password; if not empty, Video is blanked (if enabled in Setup). Floppy writes are disabled (if enabled in setup). Power and Reset switches on the front panel are disabled. No mouse or keyboard input is accepted. However, the Mouse driver is allowed to load before a password is required.	User Password	Floppy writes are enabled. Power and Reset switches are enabled. Keyboard and mouse inputs are accepted. System attempts to boot from drive A.
User Password boot (AT style)	Power On/Reset	User Password Secure Boot Disabled in SCU	System halts for User Password before booting. Video is blanked (if enabled in setup). Floppy writes are allowed (if enabled by CU). Power and Reset switches on the front panel are disabled. No mouse or keyboard input is accepted.	User Password	Power and Reset - switches are enabled. Keyboard and mouse inputs are accepted. Boot sequence: drive A. then drive C
Power and Reset Switch Lockout	Same as “Secure Mode” above	User-programmed bit (using FMUP)	Power and reset buttons are disabled on front panel.	User clears the bit	Power and reset switches enabled.

4.1.1.1 Password Protection

Passwords prevent unauthorized tampering with the system. Once secure mode is enacted, access to the system is allowed only after the correct password(s) have been entered. Passwords for both the user and administrator can be created during system configuration using the CU.

If a user password is set without an administrative password, this password is the only one required to boot the machine or run the CU. If both passwords are enabled, either password can be used to boot the machine or enable the keyboard and/or mouse, but only the administrative password allows the system configuration to be changed using the CU.

The user password only allows viewing of the system configuration settings, while the administrative password is provided as a means to access basic system configuration independently from other access controls. For example, system hardware configuration can be controlled by an administrator, while the user password can control access to the machine's file system.

Once set, a password can be disabled by changing it to a null string.

4.1.1.1.1 Inactivity Timer

If the inactivity timer function is enabled, and no keyboard or mouse actions have occurred for the specified timeout period, the following occurs until the user password is entered:

1. Keyboard and mouse input is inhibited
2. Video is blanked
3. Floppy drive is write protected (if enabled)
4. A timeout period of 1 to 128 minutes may be specified with the CU, in 1 minute increments.

4.1.1.1.2 Hot key activation

A hot-key can activate secure mode immediately, rather than having to wait for the inactivity timeout to expire. The hot-key combination is set using the CU.

4.1.1.1.3 Password Clear Jumper

The BIOS reads the GPIO port, to determine if the password clear switch (located on the baseboard configuration jumper) is set. If set, any passwords are cleared from CMOS and password protection is disabled.

4.1.1.2 Boot Sequence Control

Security features in the BIOS determine the boot devices and the boot sequence, and control the disabling of writes to the floppy drive in secure mode. The CU is used to select one of the following:

- First boot device.
- Second boot device.
- Third boot device.
- Fourth boot device.

Floppy, hard disk, CD-ROM and network can be selected for each boot device. The default boot sequence is: floppy, hard disk and CD-ROM.

NOTE: *In addition to BIOS boot device type, the system bus is also considered when determining from which device the system will boot. The ISA bus is scanned first (Onboard IDE, lowest enabled BIOS ROM - "D000"), then the primary PCI slots (Bus 0, slots 1-4) and finally the secondary PCI slots and devices (Bus 1, , onboard SCSI, slots 1-2 last in this chain).*

4.1.1.3 Boot Without Keyboard

The system can boot with or without a keyboard. Before booting, the BIOS displays whether it has detected a keyboard. There is no entry in the CU for keyboard enable/disable. The presence of the keyboard is detected automatically during POST, and the keyboard is tested if present.

4.1.1.4 Floppy Write Protection

If enabled by the CU, floppy disk writes are disabled when the system is in secure mode. Floppy write protection is only in effect while the system is in secure mode. Otherwise, write protection is disabled.

4.1.1.5 Power Switch and Reset Button Lock

If enabled by the CU, the power switch and reset button are disabled when in secure mode.

4.1.1.6 Secure Boot Mode

Secure Boot mode allows the system to boot and run the OS, but no mouse or keyboard input is accepted until the user password is entered. The CU is used to place the system into secure boot mode. In secure boot mode, if the BIOS detects a floppy disk in the A drive at boot time, it prompts the user for a password. When the password is entered, the system can boot from the floppy and secure mode is disabled. Any one of the secure mode triggers will cause the system to go back into secure mode. If there is no disk in drive A, the system boots from the C drive and is placed in secure mode automatically. All of the secure mode features (that are enabled) go into effect at boot time.

4.1.2 Auto-configuration Features

The B440FX DP Server BIOS provides support for auto-configuration of the following:

- Processor speed
- SMP initialization
- Memory sizing including greater than 16MB memory support
- Boot drive selection
- Video controller auto-detection
- PCI and ISA add-in devices
- Resource allocation
- User-supplied BIOS code

The B440FX DP Server BIOS does not support auto-detection of floppy.

4.1.3 Reliability Features

The B440FX DP Server BIOS supports several reliability features, including the following:

- ECC memory and defective DIMM handling
- Fault resilient booting
- Logging of critical events
- CMOS default override

4.1.4 Multiple Language Support

Any number of languages can be supported in the BIOS. FMUP is used to load language support that replaces the text strings for POST. The FMUP also loads general error messages with text strings translated into a particular language.

Intel provides specifications for all BIOS/SCU text strings, so that any OEM (Original Equipment Manufacturer) can have them translated and prepared for updating with FMUP. By default, FMUP provides language support for English, Spanish, French, German, and Italian, which can all be selected using the SCU.

4.1.5 I^2C Diagnostic Bus

The I^2C interface on the baseboard provides an independent interconnect between various devices in the system (e.g., memory board, processor boards, etc.), for diagnostic or other purposes normally unavailable to the system. The base address register of the I^2C interface on the server is 0CA0h.

Each device on the I^2C bus has a controller that responds to a unique ID.

4.1.6 Intel MPS 1.4 Support

The B440FX DP Server BIOS is required to be compliant with the Intel MPS Specification, revision 1.4. The server features:

- Intel Multi-Processor Specification (MPS)
- Selection of the BootStrap Processor (BSP)
- Responsibilities of the BSP and Application Processor (AP) during POST
- Reset and initialization
- MPS configuration table

4.1.7 Flash Update Utility

The system BIOS, setup utility, and configuration files are housed in partitioned Flash ROM. The device is in-circuit reprogrammable, except for the recovery boot block, which is electrically protected from erasure. A jumper on the baseboard can enable writing to this region.

The Flash Memory Update utility (FMUP) loads a fresh copy of the BIOS into Flash ROM. The loaded code and data include the following:

- Onboard Video BIOS and SCSI BIOS
- Setup and SCSISelect* utilities
- User-definable Flash area (User Binary Area)
- Language file

When running FMUP in interactive mode, any particular flash area can be saved, updated, or verified. Saving a flash area takes a mirror image of the specified Flash area and copies it to a file (or series of files) on hard or floppy disk. Updating a flash area takes a file (or series of files) from hard or floppy disk, and loads it in the specified area of Flash ROM. Verifying a flash area compares an existing flash area against a file (or series of files) on hard or floppy disk.

NOTE: *FMUP must be run without the presence of a 386 control program (such as Windows or EMM386). FMUP uses the processor's flat addressing mode to update the flash part.*

4.1.7.1 User Binary Area

The B440FX Server includes an 8K area in Flash for implementation-specific OEM add-ons. The user binary area can be saved and updated exactly as described in the BIOS section. Only one file is needed. The valid extension for user files is .USR.

4.1.7.2 User-supplied BIOS Code Support

An 8KB block of Flash is available for general use, and FMUP can update this area with user-supplied code or data. The User Binary Area may (enabled using the CU) be scanned for custom BIOS code during POST, and if found, it can be initialized in the same manner as any other adapter BIOS ROM.

To accommodate a range of uses, the User Binary Area can call user programs at various points in the BIOS execution. User-supplied BIOS code must adhere to the following requirements:

- Custom BIOS code must be recognizable to the system BIOS (for proper execution) and other applications (e.g., DOS memory managers) so that they are protected after DOS boots.
- The system BIOS performs a scan of the User Binary Area at a number of points during POST. It is necessary for the system BIOS to selectively execute a scanned BIOS based on which scan is being performed. Furthermore, it is possible that a particular scanned BIOS might require execution at more than one scan. The BIOS extensions accommodate this by providing the scanned BIOS information about which scan is being performed.
- System state must be defined for each scan point.
- Some system resources (RAM, CMOS) may be required by the scanned BIOS.

At each scan point in POST, the system BIOS looks for the value AA55h in the User Binary area. When this signature is discovered at any 2K boundary within the area, the system BIOS examines byte 3. If byte 3 is not 0CBh (RETF), the scanned code is ignored (until the normal user scan just prior to boot). Otherwise, if the RETF is found, the scanned code is considered a new part of the BIOS, and the system BIOS must determine if this is the correct scan point to transfer control. This is done by comparing the bitmap identified by the following byte (byte 4) to the current mask bit (which has been determined/defined by the scan point). If the bitmap has the appropriate bit set, then the mask is placed in AL and execution is passed to the address computed by (ADR(Byte 5)+5*scan sequence #). In addition, the user BIOS is granted access to 16 bytes of BIOS Data Area Ram (40:D0h - 40:DFh) and a bit 5 (mask 20h) of CMOS byte 33 (unchecksummed). Coordination of these resources between scanned BIOS code is the responsibility of the user.

The following code fragment shows how to prepare custom BIOS code for scanning:

```
                db      55h, 0AAh, 10h  ; 8K USER Area


MyCodePROC      FAR             ; MUST be a FAR procedure
                RETF            ; This byte (3rd, 4th in the file) is the
                                ; transfer address in a standard scanned BIOS.
                                ; It is a RETF for backward compatibility, and
                                ; acts as a flag to distinguish this as User
                                ; Binary Area BIOS code
                db      04h     ; Bit map to define call points, a 1 in any bit
                                ; specifies that the BIOS is called at that scan
                                ; point in POST (scan points TBD)
                JMP     ErrRet  ; This is a list of 8 transfer addresses, one
                db      0,0     ; for each bit in the bitmap.  In all likelihood
                JMP     ErrRet  ; only one of these is used, earlier entries
                db      0,0     ; must be present, later can be omitted if
                JMP     Start   ; desired.
                db      0,0
                JMP     ErrRet
                db      0,0
                JMP     ErrRet
                db      0,0
                JMP     ErrRet
                db      0,0
                JMP     ErrRet
                db      0,0
```

```
Start:
                {code}

ErrRet:
                RETF

MyCodeendp
```

4.1.7.3 Scan Point Definitions

The following table defines the bitmap for each scan point, indicating when the scan point occurs and which resources are available (RAM, Stack, Binary Data Area, Video, Keyboard).

Table 4-2 User Binary Area Scan Point Definitions

Scan Point	Mask	RAM/Stack/BDA	Video/Keyboard
This scan occurs immediately before video initialization	08h	Yes	No
This scan occurs immediately after video initialization.	04h	Yes	Yes.
This scan occurs immediately before the normal external ROM scan. This is just before boot but prior to the scan for external ROMs and the scan for conventional BIOS in User Binary.	40h	Yes	Yes,
This scan occurs immediately following the "normal" User Binary area scan.	80h	Yes	Yes
This is the final scan, it occurs immediately prior to the INT 19 for normal boot and allows you to completely circumvent the normal INT 19 boot if desired.	20h	Yes	Yes
This scan only occurs as a result of an SMI (during SMM). It is the last SMM detection routine to run. New log messages entered during this SMM interval (if any) are copied verbatim into SMRAM at A900:40. This log fragment can be traversed in exactly the same manner as the "real" log and will always include the final 0FFh as a "last record" flag. If no log messages were added, the byte at 0a900:40 is 0FFh. The USER_CMOS_BIT_1 (Byte 33 Bit 6) is copied into SMRAM at 0A900:0021 bit 0 and USER_CMOS_BIT_2 (Byte 36 bit 1) is copied to SMRAM at 0A900:0021 bit 1.	02h	A stack is assured, in addition, 128 bytes of SMRAM is available to the user binary from SMRAM address 0A900:0080-0A900:00FF. Remember, this is SMRAM and only accessible when in SMM. It will persist between SMM invocations (but not across resets or power-downs). The processor is in real mode at this point.	Video memory and INT 10h services are not accessible since SMRAM is mapped over the top of where video RAM usually is. Keyboard services are not available through BIOS, although port accesses to the keyboard is possible.
This scan occurs just before boot to provide User Binary an option to alter status of any POST error messages; for instance, a message status can be changed from warning to fatal, display or not display on the video etc.	10h	Yes	Yes

4.1.7.4 Language Area

The system BIOS language area can be updated without having to update the entire BIOS. English, Spanish, French, German, and Italian are the languages that are selectable using the SCU. When additional language

files (*.LNG) are made available, they can be loaded into the system BIOS using FMUP (in interactive mode as described above), in the same manner as updating the system BIOS and the user binaries.

4.1.7.5 Recovery Mode

In the case of a corrupt .bIx image or an unsuccessful update of the system BIOS, the B440FX DP Server can boot in recovery mode. To place the B440FX DP Server into recovery mode, move jumper J47 to connect pins 2 and 3 (recovery BIOS). The jumper connects pins 1 and 2 (normal BIOS) by default.

Recovery mode requires at least 4MB of RAM, and that drive A: be setup to support a 3.5" 1.44MB floppy drive. This is a last resort, to be used only when the main system BIOS will not come up. In recovery mode operation, FMUP (in non-interactive mode only) automatically updates only the main system BIOS. FMUP senses that the B440FX DP Server is in recovery mode and automatically attempts to update the system BIOS.

Before powering up the B440FX DP Server, obtain a bootable MS-DOS diskette that contains a copy of the BIOS release. Boot the system from the A: drive using this diskette, which executes a special AUTOEXEC.BAT file from the BIOS release. The batch file invokes FMUP, which updates the flash ROM with the BIOS found on the diskette.

NOTE: *During recovery mode, video will not be initialized. One high pitched beep announces the beginning of the recovery process. The entire process takes between 2 and 4 minutes and a successful update ends with two high pitched beeps. Failure is indicated by a low buzz.*

If a failure occurs, it is most likely that one or more of the system BIOS FMUP files is corrupt or missing.

After a successful update, power down the system and move the J47 jumper back to pins 1 and 2. Power up the system and verify that the BIOS version number matches the version of the entire BIOS that you originally attempted to update. CMOS is not cleared when the system BIOS is updated. Remember that any additional or different languages that were present before updating will need to be reloaded to Flash.

4.2 Configuration Utilities

The Configuration Utilities (CU) configure onboard hardware resources and add-in cards. The CU is provided in three forms:

1. **Standard PC-AT Setup ability, or Setup.** Embedded in the Flash ROM, this configures onboard resources. Configuration of onboard devices can be done using a subset of the CU embedded in Flash ROM known as the Setup utility. Setup provides enough configuration functionality to boot a system diskette, shipped with the hardware, that contains the SCU. The booted SCU is required for configuration of PCI and ISA add-in cards.

2. **System Configuration Utility (SCU).** This configures add-in cards and ROM-resident Setup utilities. It must be run from a boot diskette (shipped with the system). The SCU is PCI-aware and conforms to the ISA Plug-N-Play Specification version 1.1. The SCU works with any compliant CFG or OVL files supplied by the peripheral device manufacturer, although Intel supplies only the OVL and CFG files for the system baseboard.

3. **SCSISelect used to configure the onboard Adaptec AIC-7880 SCSI device.** The CU modifies the ISA CMOS RAM and NVRAM, under direction of the user. The actual hardware configuration is accomplished by the BIOS Power-On-Self-Test (POST) routines and the Plug-N-Play Auto-configuration Manager. The CU always updates a checksum for both areas, so that any potential data corruption is detectable by the BIOS before actual hardware configuration takes place. If the data is corrupted, the BIOS requests that you configure the system before the system is rebooted. If the disk-based SCU is used, a customer-supplied logo is automatically displayed before the SCU is executed. Localization of the SCU is accomplished by a new copy of the SCU provided on diskette.

4.2.1 Configurable Options

The following table defines most of the Configurable options, although more options may also be supported. The BIOS detects the state of the “CMOS default” switch (configuration DIP switch on the baseboard). If set prior to power-on or hard reset, the BIOS changes CMOS and NVRAM settings to a default state with no exceptions, which guarantees the system’s ability to boot from floppy (CMOS clear). After CMOS clears default values, shown in **bold** below, they are copied into CMOS.

Buckeye OVL Options

When you select SCU step 3, Change Configuration Settings, there are many menus and options available under that heading. This section about the SCU shows the screen information that displays **after you select the System Board from the Change Configuration Settings screen.**

- Default values are in **bold** type.
- Select an option and press <Enter> to display the menu for an option.
- Some items are displayed only, with no selection available here.

Some of the option choices are described below the grouping. Not all of them are described because a few are not user-selectable but are displayed for information purposes and because many of the option choices are relatively self-explanatory.

Note: *Record your SCU settings on the worksheets in Chapter 9. If the default values ever need to be restored (after a CMOS-clear, for example), you must run the SCU to reconfigure your system. Referring to the worksheets could make your task easier.*

Table 4-3 Configuration options (System group)

Systems Group	
System Identification and Version Information	
System Identification String	Displays System Identification String
Config and Overlay Version	Displays overlay version number
BIOS Version String	Displays BIOS version
MP Spec Version:	**MP Spec V1.1** MP Spec V1.4
System Processor Module	
Processor 1 in Slot 1	Displays Pentium Pro Processor at {XXX} MHz (or Not Present)
Processor 2 in Slot 1	Displays **Pentium Pro Processor at {XXX} MHz** (or Not Present)
System Processor Status	
Processor 1 in Slot 1	Displays “Failures Detected” or “**No Failures Detected**”
Processor 2 in Slot 1	Displays “Failures Detected” or “**No Failures Detected**”
System Performance	
Power-on Speed Option	**Processor Speed=Fast** Processor Speed=Slow
Direct PCI Interrupts to I/O APIC	**Enable** Disable

Table 4-4 Configuration options (Memory group)

Memory Subsystem Group	
Base Memory Options	**640KB Base Memory** 512KB Base Memory
Shadowing ISA ROMs Options	Press <Enter> to modify the shadowing options
Extended Memory Options (Cache, 1MB ISA Hole)	XXX MB Extended Memory / 256KB Cache (WB)

Table 4-5 Configuration options (onboard disk)

Onboard Disk Controllers	
Onboard Floppy Controller	**Enable** Disable
Onboard IDE Controller	**Enable** Disable

Table 4-6 Configuration options (onboard comm.)

Onboard Communication Devices	
Serial Port 1 Configuration	**Port:3F8h IRQ:4 (COM 1)** Port:2F8h IRQ:3 (COM 2) Port:3E8h IRQ:4 (COM 3) Port:2E8h IRQ:3 (COM 4) Port 1 Disable
Serial Port 2 Configuration	**Port:2F8h IRQ:3 (COM 2)** Port:3F8h IRQ:4 (COM 1) Port:3E8h IRQ:4 (COM 3) Port:2E8h IRQ:3 (COM 4) Port 2 Disable
Parallel Port Configuration	**Port:378h IRQ:7 (LPT 1)** Port:278h IRQ:5 (LPT 2) Port:3BCh IRQ:7 (LPT 3) Parallel Port Disable
Parallel Port Mode	**Parallel Port Mode ISA-Compatible** Parallel Port Mode PS/2 Parallel Port Mode Extended (Not valid with LPT3) Parallel Port Mode ECP on LPT1 with DMA 1 Parallel Port Mode ECP on LPT1 with DMA 3 Parallel Port Mode ECP on LPT2 with DMA 1 Parallel Port Mode ECP on LPT2 with DMA 3

Table 4-7 Configuration options (Floppy)

Floppy Drive Subsystems Group	
Floppy Drive A Options	**3.5 inch 1.44/1.25 MB drive** 5.25 inch 360 KB drive 5.25 inch 1.2 MB drive 3.5 inch 720 KB drive 3.5 inch 2.88 MB drive Disable or Not Installed
Floppy Drive B Options	**Disable or Not Installed** 3.5 inch 1.44/1.25 MB drive 5.25 inch 360 KB drive 5.25 inch 1.2 MB drive 3.5 inch 720 KB drive 3.5 inch 2.88 MB drive

Table 4-8 Configuration options (IDE)

IDE Subsystem Group	
ISA IDE DMA Transfers	**Auto Configured** Disable
IDE Configuration - Primary Master	**{Drive Name} /** {No Drive Detected} **Auto** Customize Disable
IDE Drive Options - Primary Master	
Multi-sector Transfer	**Auto Configured** 4 Sector/Block 8 Sector/Block Disable
Translation Mode	**Auto Configured** Standard CHS Logical Block Addressing Extended CHS
Enhanced IDE Mode	**Auto Configured** Disable
IDE Configuration - Primary Slave	**{Drive Name} /** {No Drive Detected} **Auto** Customize Disable
IDE Drive Options - Primary Slave	
Multi-sector Transfer	**Auto Configured** 4 Sector/Block 8 Sector/Block Disable
Translation Mode	**Auto Configured** Standard CHS Logical Block Addressing Extended CHS
Enhanced IDE Mode	**Auto Configured** Disable
IDE Configuration - Secondary Master	**{Drive Name} /** {No Drive Detected} **Auto** Customize Disable

continued

IDE Subsystem Group (con't)	
IDE Drive Options - Secondary Master	
Multi-sector Transfer	**Auto Configured** 4 Sector/Block 8 Sector/Block Disable
Translation Mode	**Auto Configured** Standard CHS Logical Block Addressing Extended CHS
Enhanced IDE Mode	**Auto Configured** Disable
IDE Configuration - Secondary Slave	{Drive Name} / {No Drive Detected} **Auto** Customize Disable
IDE Drive Options - Secondary Slave	
Multi-sector Transfer	**Auto Configured** 4 Sector/Block 8 Sector/Block Disable
Translation Mode	**Auto Configured** Standard CHS Logical Block Addressing Extended CHS
Enhanced IDE Mode	**Auto Configured** Disable

Table 4-9 Configuration options (BIOS)

BIOS Language Support Group	
BIOS Language Support Options	
Current BIOS Language	**English (US)** {more options are listed if available}

Table 4-10 Configuration options (Input devices)

Keyboard (KB) and Mouse Subsystem Group	
Keyboard and Mouse Options	
Num Lock Options	**Off at Boot** On at Boot
Typematic Speed	**Auto** Fast (7 char/sec) Medium (4 char/sec) Slow (1 char/sec)
Mouse Control Option	**Mouse Auto detected**

Table 4-11 Configuration options (Console)

Console Redirection	
Console Redirection Control	
COM Port for Redirection	**Disable** Enable Redirection on COM1 @ E4000 Enable Redirection on COM2 @ E4000
Serial Port Baud Rate	2400 Baud 9600 Baud 19.2K Baud **115.2K Baud**
Hardware Flow Control	None **CTS/RTS** CTS/RTS & Xoff/Xon
Select Terminal Type	**ANSI**

Table 4-12 Configuration options (Security)

Security Subsystems Group	
Administrative Password Option	**Disable/**Enabled (Press <Enter> to display the Password Menu. After entering a new password, <Tab> down to verify the password.) New Password Enter Password XXXXXXX Verify Password XXXXXXX
User Password Option	**Disable/**Enabled Press <Enter> to display the Password Menu. After entering a new password, <Tab> down to verify the password. New Password Enter Password XXXXXXX Verify Password XXXXXXX
Hot Key Option	**Disable/**{Ctrl-Alt-?} Press <Enter> to display menu: **Disable** Enable <Tab> down to Enable, and then <Tab> to Enter New Hot Key. Type one character, either a letter or number.
Lockout Timer	**Disable/**{1-127 Minutes} Press <Enter> to display menu: Value in minutes: (0 = Disable, 127 = Maximum)
Secure Boot Mode	**Disable** Enable
Video Blanking	**Disable** Enable
Floppy Writes	**Enable** Disable

Table 4-13 Configuration options (Boot)

Boot Subsystem Group	
Boot Options	
First Boot Device	**Boot Floppy** Boot Hard Disk Boot IDE CD-ROM Floppy Image Boot IDE CD-ROM Hard Drive Image Boot Network
Second Boot Device	Boot Disabled Boot Floppy **Boot Hard Disk** Boot Network
Third Boot Device	**Boot Disabled** Boot Floppy Boot Hard Disk Boot Network
Fourth Boot Device	**Boot Disabled** Boot Floppy Boot Hard Disk Boot Network
Display '<F1> for Setup' Message during POST	**Enable** Disable
Require User Interaction on POST Errors	**Enable** Disable

Table 4-14 Configuration options (SCSI BIOS)

SCSI ROM BIOS Options Group	
SCSI-A ROM BIOS Scan	**Enable** Disable (if disabled, the SCSI-A channel is fully configured, but the ROM scan is skipped)

Table 4-15 Configuration options (SMM)

Management Subsystem Group	
System Sensor Control	Press <Enter> to modify the System Sensors.
Speaker Options	**Enable** Disable
Scan User Flash Area	**Disable** Enable
System Management Options	
System Management Mode	**Disable** Enable
Event Logging	**Disable** Enable (controls onboard event logging.)
PCI System Error Detection	**Disable** Enable

4.3 Error Sources and Types

Server management must be able to correctly and consistently handle system errors. System errors on the B440FX DP Server which can be disabled and enabled individually or as a group, are categorized as follows:

- ISA bus
- PCI bus
- Processor bus (or internal)
- Memory bus (or DIMM)
- System limit

ISA and PCI bus errors can be further classified as 'standard bus' errors, which have a standard register interface across all platforms. All other errors, like Processor bus and ECC errors, are referred to as 'product-specific' errors, which require special consideration depending upon the system configuration. Product-specific errors can be emulated as standard bus errors, if specific routing of certain hardware signals (as documented in this chapter) is followed. This emulation is important to both OS and BIOS NMI handlers, which have no knowledge of product-specific errors, but need to recover and shut down the system gracefully.

Three types of the system errors can occur on the B440FX DP Server : Fatal, Warning, and Trivial.

- Fatal errors are logged by an error handler before they are reported to the OS, which performs fatal error post-processing, and causes a halt or reset of the system.
- Warning errors are logged by an error handler before they are reported to the OS, which can then display an informative message.
- Trivial errors are only logged by an error handler and are not reported to the OS.

Errors are reported using NMI (non-maskable interrupt) and SMI (system management interrupt). SMI is used for server management error pre-processing. All errors can be intercepted by SMI (if enabled in Setup). Otherwise, all errors can be processed by NMI handlers. Some errors must use NMI even if they are intercepted by SMI, because the traditional way to handle these errors is by NMI.

4.3.1 Error Handlers

Three error handlers are required: BIOS NMI handler, OS NMI handler, and SMI handler.

- BIOS NMI handler is the default error handler. As such it processes the standard bus (ISA, PCI) errors and disables NMI (if the source is unknown). In general, it is not product-specific, but can be customized in special cases. This handler is part of the BIOS but can be overridden or intercepted by the OS NMI handler.
- OS NMI handler is OS-based and not product-specific. It shuts down the system when an NMI occurs, and may override or intercept the BIOS NMI handler. It resides in the OS kernel and cannot be customized,

even via an OS device driver.

- SMI handler has the highest priority for error processing, and processes all system errors. If SMI is disabled (using a Setup option), errors that normally belong to the SMI resource can be routed to the BIOS NMI handler. The SMI handler is product-specific and OS-transparent. It logs and preprocesses all system errors. It emulates product-specific fatal system errors as standard bus errors. It is loaded by the BIOS and can be enabled and disabled using a Setup option.

There are two modes in which the BIOS NMI and SMI handlers work together:

1. SMI handler disabled. In this mode, the NMI handler can only process standard bus errors (which have been enabled by the BIOS). All of the product-specific errors are not recognized and must be disabled, or emulated in hardware. These product specific errors need to be initialized for other applications, such as, OS device driver.

2. SMI handler enabled. In this mode, the SMI handler processes all system errors. The BIOS enables all of the system errors and routes the NMI errors to SMI for preprocessing. The SMI handler only passes the standard bus errors to the NMI handler. The SMI handler can emulate the standard bus system errors for compatibility if the error are properly routed in hardware. If the system NMI handler only processes some of the standard bus errors (e.g., ISA-only), the SMI handler must be consistent with the BIOS NMI handler, and pass those system errors only to the BIOS NMI handler instead of other standard bus errors which cannot be handled by the BIOS NMI handler.

4.4 BIOS Setup

This section describes the BIOS Setup options. The Setup utility stores configuration values in flash memory and in the battery-backed memory of the real-time clock (RTC). Values you enter in Setup are overwritten when you run the SCU.

For a number of options, the settings are made by using the SCU, not Setup. The values are simply displayed in the Setup screens. To see the descriptions of such options, refer to the SCU section later in this chapter.

Setup has four major menus and several sub-menus. To move between the major menus, use the ← → keys. To display the sub-menus, press <Enter> when the prompt is displayed beside an option name.

4.4.1 When to Run Setup

You should run setup if:

- the boot-time prompt says to do so
- it is needed in order to enable or properly configure your diskette drive.
- there is no access to a diskette drive.

Much of the system configuration is done through the SCU, not Setup. Because the SCU is provided on diskette, a diskette drive needs to be connected and enabled. After configuring the system, you may prefer to secure it against casual or unauthorized access by someone using diskettes. Therefore, you can:

- run Setup to enable the diskette drive
- then use Setup or the SCU to configure the system
- run Setup again to disable the diskette drive for security

4.4.2 What can be changed

System Date and System Time—to change, type in the correct date and time and press <Enter>.

Floppy Options—displays a menu that lists the type of diskette drive connected. If one is not connected, you will see the word “Disabled.”

NOTE: *You can use the Floppy Options menu to limit access to a drive.Use this menu to specify whether access to the diskette drive is Read/Write or Read Only.*

Primary IDE Master—a separate menu screen appears for EACH of the IDE devices. For each IDE drive, if the system has already been configured, you will see the name of the device or the phrase “Not installed.”

Language—step through the language choices available for the BIOS prompts. If you change the default (English), you will not see any change until you exit the SCU and enter Setup. Only the BIOS prompts and menus appear in the selected language. The SCU screens remain in English.

Boot Options—a separate menu screen appears.

Video Mode—displays the mode selected in the SCU.

Mouse—displays the mode selected in the SCU.

Memory—displays the amount of base and extended memory detected.

The most stable system will be achieved if you use the recommended default settings, although you are free to try other options. Keep the settings for the primary and secondary IDE masters and slaves.

4.5 Setup Utility Operation

The Setup utility configures only onboard devices. Configuration of added PCI or ISA cards requires the use of the diskette-loadable SCU. The Setup Utility provides these 4 major menus of configurable options:

- Main Menu
- Advanced Menu
- Security Menu
- Exit Menu

Each menu occupies the left and center sections of the screen. Selecting certain fields within a major menu drops you into sub-menus. On the right side of the screen is a Command screen; the following section describes each command.

4.5.1 Setup Command Screen

The right side of the Setup screen provides a list of commands for interacting with the Setup Utility. These commands are displayed at all times, for every menu and sub-menu.

4.5.1.1.1 F1 Help

Help is provided for most of the fields. It cannot be invoked when parameter options are being displayed.

4.5.1.1.2 ESC Back

The ESC key provides a mechanism for backing out of any field. When the ESC key is hit while editing any field, the field options cease to be displayed. When the ESC key is hit in any sub-menu, the parent menu is re-entered. When the ESC key is hit in any major menu the following screen is displayed:

Exit Discarding Changes?
Press Enter to Continue **Press ESC to Abort**

At this point pressing the Enter key will cause Setup to exit without saving any changes that may have made. Pressing the ESC key brings you back to the top level of the current menu.

4.5.1.1.3 Enter Select

The Enter key is used to activate sub-menus, change parameters and select parameter options.

4.5.1.1.4 ↑ Previous Item

The up arrow is used to move to the menu item above the current item..

4.5.1.1.5 ↓ Next Item

The down arrow is used to move to the menu item below the current item.

4.5.1.1.6 ↔ Select Menu

The left and right arrow keys are used to move between the 4 major menus.

4.5.1.1.7 F5 Setup Defaults

Pressing F5 cause the following to appear:

Load Setup Defaults?
Press Enter to Continue Press ESC to Abort

If the Enter key is hit, all Setup fields are set to their default values. If ESC is hit, then you are returned to where you were before F5 was pressed, without affecting any existing field values.

4.5.1.1.8 F6 Previous Values

Pressing F6 causes the following message to appear:

Discard Changes?
Press Enter to Continue Press ESC to Abort

If the Enter key is hit, all Setup fields are returned to their original values, i.e., those in effect before Setup was entered. If the ESC key is hit, you are returned to where you were before F6 was pressed, without affecting any existing values.

4.5.1.1.9 F10 Save & Exit

Pressing F10 causes the following message to appear:

Exit Saving Changes?
Press Enter to Continue Press ESC to Abort

If the Enter key is hit, the Setup Utility is exited with all parameters set to their current values. If the ESC key is hit, then you are returned to where you were before F10 was pressed.

4.5.2 Menu Navigation

Each menu contains a number of parameter fields. You can change most parameters, except those for informative purposes only. Editable parameters are displayed in black, information-only parameters are displayed in blue. Depending on the security option chosen and in effect (via password), a parameter can be changeable or not. If a parameter is non-changeable due to insufficient security privilege (or other reasons), it is grayed out. Parameters that have no effect based on the value of other parameters are not displayed.

4.5.2.1 Saving the configuration

When exiting Setup, if you have changed any parameters, you are asked to save the configuration in CMOS. If you have pressed the ESC key to exit from the main menu, you are prompted with the following message.

Exit Discarding Changes?
Press Enter to Continue Press ESC to Abort

If the Enter key is hit, the Setup Utility is exited with all parameters set to their current values and the system is rebooted. If the ESC key is hit, you are returned to where you were in Setup without effecting any change.

4.6 System Configuration Utility (SCU)

The system configuration utility (SCU) is the main tool to configure the system or to check or change the configuration. Most system settings can be entered from either the SCU or Setup, but the SCU provides conflict resolution as well as access to information about ISA, ISA Plug-N-Play, EISA, and PCI adapters.

NOTE: *Because the SCU is provided on a diskette, the system must have a diskette drive. If a drive is present but is disabled or improperly configured, use the BIOS Setup utility to enable or configure the diskette drive. Then make a bootable SCU diskette and use the SCU to configure the system.*

4.6.1 When to Run the SCU

The SCU should be run:

- when the system is first set up and configured
- if there is a configuration error message at power-on
- each time an ISA add-in board is added, removed, or moved
- each time memory is added or removed

Running the SCU is also recommended for Plug-N-Play and PCI add-in boards.

4.6.2 Where the SCU Gets Information

Information comes from	Description
Configuration (.CFG) *or* overlay (.OVL) files	For the baseboard, we provide these files. For some ISA add-in boards, each comes with a diskette that contains a .CFG file (and an optional .OVL file) supplied by the device manufacturer. The file describes the board's characteristics and the system resources it requires.
Configuration registers	The configuration registers on PCI and Plug-N-Play add-in boards contain the same type of information that an ISA .CFG file does. The SCU is PCI and Plug-N-Play aware, and it complies with the ISA Plug-N-Play Specification (version 1.1).
Your option selections	The SCU stores your information by modifying ISA CMOS and EISA nonvolatile RAM (NVRAM). It stores most of the values in the battery-maintained memory of the real-time clock (RTC); it stores the rest of the values in flash memory.

4.6.3 Checking the Configuration at Power-on

At power-on or rebooting, the BIOS POST routines and the Plug-N-Play Auto Configuration Manager checks and configures the hardware. POST checks the values that have been stored against the actual hardware configuration; if the values do not agree, an error message will sound. The SCU must be run to correct the configuration before the system boots.

4.6.4 How to Use the SCU

1. Copy the file HIMEM.SYS onto a DOS bootable diskette.

2. Turn on the video display monitor and system.

3. There are three ways to start and run the SCU:

   - From diskette: insert the System Configuration Disk in drive A, and then press the reset button or type <Ctrl+Alt+Del> to reboot the system.
   - From a DOS directory on the hard drive, type SCU. Press <Enter>. If this method is used, HIMEM.SYS needs to be loaded into the AUTOEXEC.BAT and CONFIG.SYS files.
   - From diskette in drive A: change to drive A and type SCU at the MS-DOS † prompt. Press <Enter>.

   The ability ot use the second or third method depends on how much main memory is used by drivers that are loaded onto the system.

4. The SCU has four major configuration menus and several sub-menus. From the main menu, select "Step 1: About System Configuration" for information about setting up the computer.

To navigate the screens	Press key...	...or use mouse
Change between major menus	← or →	
From main menu, press up or down arrow to highlight an item	↑ or ↓	Point to item
Select an item	<Enter>	Double-click left button
Get help	<F1>	Point to help on toolbar
Enter numbers and symbols	numeric keypad keys	
To change options	Enter Administrator password if this is enabled	

NOTE: *To run the SCU faster on a DOS-based system, copy to a directory onto the hard drive and run it from there. The SCU may not run properly unless HIMEM.SYS is loaded and there is approximately 600 KB of conventional system memory available.*

4.6.5 Configuring the System

There are six steps, accessible from the main menu, to configure the system:

1. About System Configuration
2. Add and Remove Boards
3. Change Configuration Settings
4. Save Configuration
5. View Switch/Jumper Settings
6. Exit

The SCU has three major menus and multiple sub-menus. Follow the screen prompts to move between the major menus, display sub-menus, and make selections.

4.6.5.1 About System Configuration

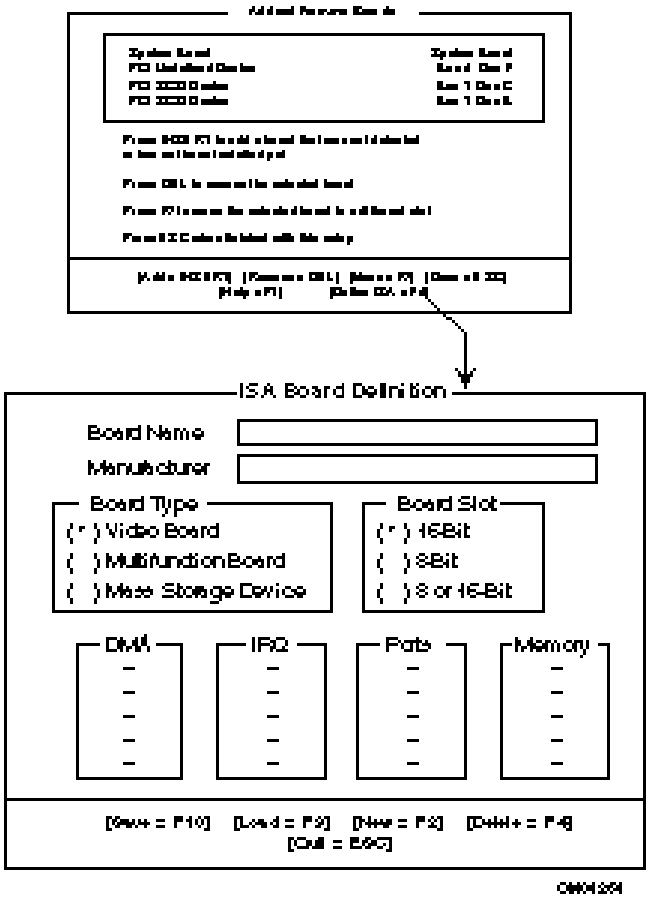
This step provides basic information for configuring expansion devices. More experienced users can skip this step.

4.6.5.2 Add and Remove Boards

Use this step to add, delete, or move boards. Most boards are automatically detected and added by the SCU once you enter this step. However, if the SCU did not detect a board, you can add a board manually.

4.6.5.3 Define an ISA Board

To define an ISA board that has no .CFG file, press F6 while viewing the Add and Remove Boards screen. The ISA Board Definition dialog box will appear. It is necessary to define a board to prevent other boards in the system from using the same IRQ levels, DMA channels, I/O addresses, or memory addresses as that of the ISA board.



To define an ISA board:

1. In the Board Name box, type a description of the board.
2. In the Manufacturer box, type the name of the board manufacturer.
3. From the Board Type box, choose the type of board.
4. From the Board Slot box, choose the type of slot.
5. In the DMA box, define up to four DMA channels. Press <Enter> to bring up a list of choices.
6. In the IRQ box, define up to seven IRQ levels. Press <Enter> to bring up a list of choices.
7. In the Ports box, define up to eight ranges of I/O ports.
8. In the Memory box, define up to eight memory address ranges.
9. Press F10 to save the ISA board definition.

A previously defined ISA board can be loaded in order to modify the board definition.

To load a previously defined ISA board: Press F9.

To delete an ISA board: Press F4, and confirm that you intend to delete the ISA definition.

4.6.5.4 Change Configuration Settings

Use this step to view or change the configuration settings for any board in the system. You can verify that the baseboard and adapter board resources are set properly.

To view or change the settings for a board:

1. Use the arrow keys to select the board.
2. Press Enter.
3. When you are satisfied with the current settings, press ESC to return to the Main Menu.

4.6.5.5 Advanced Options

The Advanced Options menu is intended for advanced users. These are the options available:

Use this option	To see this
Global resource map	A list of allocated resources (DMA, IRQ, ports, and memory)
Board details	Detailed information for individual boards
System details	Information on the entire system and the current configuration
Physical board ID map	IDs of boards present in the system

To view the Advanced Options menu: from the Change Configuration Settings dialog box, press F9.

4.6.5.6 Save Configuration

This step saves the configuration settings to nonvolatile RAM as well as to a backup file (.CMS file). Settings must be saved once they have been configured.

4.6.5.7 View Switch/Jumper Settings

Use this step to view manufacturer's instructions about setting dip switches and jumpers, and how to run utilities to ensure correct configuration of each adapter.

4.6.5.8 Exit

This step exits to the operating system. If any configuration settings were changed, you will be prompted to restart your system to see the changes.

4.7 SCSI*Select** Utility

The SCSI*Select* utility detects the number of SCSI-II AIC-78xx host adapters in your system. Use the utility to start, format, and verify SCSI drives or to explicitly configure the SCSI host adapter to settings other than defaults.

The utility is menu-driven. Follow the screen prompts and information about moving around through the menus and selecting options.

4.7.1 To Start up SCSI*Select*

1. Turn on or reboot the system. During the boot-up process, the following prompt is displayed at the time the SCSI BIOS is loaded:, select from the SCU menu.

   <<< Press <CTRL><A> for SCSISelect™ Utility! >>>

   To enter the SCSI*Select* utility, press <Ctrl-A> when you see the prompt.

2. When the utility appears, choose the bus:device that you want to configure; each bus accepts up to 15 devices.

5. ERROR MESSAGES AND BEEP CODES

The system BIOS displays error messages on the video screen. Prior to video initialization, beep codes inform you of errors. POST error codes are logged in NVRAM, as well as the Extended BIOS Data area (EBDA).

The BIOS displays POST error codes on the video monitor. The error codes are defined by Intel and whenever possible are backward-compatible with error codes used in the XXpress platform.

Following are definitions of POST error codes, POST beep codes, and system error messages.

5.1 BIOS Beep Codes

A beep code is a series of individual beeps on the PC speaker, each of equal length. The following table describes the error conditions associated with each beep code and the corresponding POST checkpoint code as seen by a ‘port 80h’ card.

Table 5-1 Beep Codes

Beep Count	Port 80 Codes	Error Condition
1	71h	Refresh failure
2	72h	Parity cannot be reset
3	73h	First 4MB memory failure
4	74h	Timer not operational
5	75h	Processor failure
6	76h	8042 Gate A20 is off (v_mode)
7	77h	Exception interrupt error
8	78h	Display memory R/W error
9	79h	ROM checksum error
10	7Ah	Shutdown reg. R/W error
11	7Bh	I2C Error

5.2 POST Codes and Countdown Codes

The BIOS indicates the current testing phase during POST after the video adapter has been successfully initialized by writing a 2-digit hex code to I/O location 80h. If a Port-80h card (POSTcard ™) is installed, it displays this 2-digit code on a pair of hex display LEDs. The current countdown code indicates how far into POST the error occurred. The countdown ranges from 900 to 000 (boot OS).

Table 5-2. Port-80h and Countdown Code Definition

Code	Meaning
CP	AMIBIOS check point (port-80) code
XX	Intel AMIBIOS BIOS countdown code

5.2.1 Recovery Port-80 Codes and Countdown Codes Displayed

The following table contains the port-80 codes and the POST countdown codes displayed during the recovery boot process. Recovery boot is enabled by moving the jumper at J47 from pins 1 and 2, to pins 2 and 3, and cold-booting the system. The system will boot from the floppy disk in drive A using a recovery BIOS image that is automatically installed.

During BIOS recovery, the diskette in drive A is booted, and a BIOS image is automatically installed.

Table 5-3 Recovery Port-80 Codes

Port 80 Code	Countdown Code	Reason
02h		Disable internal cache
08h		Disable DMA controller #1, #2, disable interrupt controller #1, #2, reset video display
13h		Initialize all chip set registers
15h	900	Initialize system timer
1Bh	800	Real mode base 64 KB test
20h	700	16 KB base RAM test
23h	650	Setup interrupt vectors
40h	600	Test memory in virtual mode
65h	500	Initialize 8237 DMA controller
67h	400	8259 interrupt controller test
80h	300	Unmask diskette, keyboard and timer interrupts
88h	200	Floppy unit initialization
A0h	100	Cache enable
00h	000	Boot OS

5.2.2 Standard Port-80 Codes and Countdown Codes Displayed

Table 5-4 Standard Port-80 Codes

Port 80 Code	Countdown Code	Reason
D0h		Early MP Initialization
D1h		Power On Initialization
D2h		Disable NMI
D3h		Reset video controller
D4h		Enter real mode
D5h		Checksum the 8 KB loader BIOS
D6h		Loader BIOS checksum good
D7h	900	Check if Keyboard Controller (KBC) buffers are free
D8h		Issue BAT (basic assurance test) command to KBC
D9h		Read BAT results
DAh		Check if keyboard controller passed BAT
DBh	820	Keyboard Initialization Passed
DDh		Disable keyboard and auxiliary devices
DFh		Disable both DMA controllers
E0h	780	Preliminary initialization of PICs
E1h		Enter real big mode and initialize chip set, size memory
E2h		Initialize timer 2 for speaker
E3h	760	Initialize timer channel 0 for system timer
E4h		Clear any pending parity errors
E6h	740	Test RAM from 0-640 KB
E7h		Test and initialize 2 MB memory

continued

Port 80 Code	Countdown Code	Reason
E8h		RAM failure, remap memory partitions and test again
E9h		RAM test complete, passed. Clear parity errors
EAh	730	Set up stack at 30:100, enable cache and shadow BIOS
EBh		Initialize code dispatcher
ECh		Make F000h DRAM R/W Enabled
EDh		Dispatch POST
23h	700	Initializations before setting up vector table
24h		Setup interrupt vector table
0Dh		Check CMOS clear jumper
0Eh	690	Check validity of CMOS
0Fh		Force CMOS defaults if required
10h		CMOS initialization complete
25h		Nothing
28h		Set monochrome mode
29h		Set color display
2ah		Clear parity status if any, initialize warm reset flag
2bh		Video auto-configuration and initialization
F0h		ISA Slot Initialization
F1h		Enable extended NMI sources
F2h		Test extended NMI sources
2ch	580	Conventional video option ROM search
2dh		Scan user binary in flash

continued

Port 80 Code	Countdown Code	Reason
2eh	570	Initialize monochrome display if no other video present
2fh	560	Test buffer memory for monochrome
30h		Check vertical and horizontal retrace
31h		Test for color display memory if no external video BIOS found
32h		Check vertical retrace
34h		Sign on message
36h		Initialize Messaging Services and clear screen
37h	500	Custom sign on display
80h	370	Keyboard/mouse port check
81h		Keyboard controller initialization and testing
83h		Check if keyboard is locked
F5h	330	Initialize mouse
39h		Keyboard, mouse and other sign-ons
3bh		Prepare for memory test
43h	290	Decide memory size from chip set
4Fh		Disable cache, test memory and display memory size on screen
52h		Initialize for the other processors in MP system, reset DMA controller
61h	250	DMA register tests
62h		DMA test OK
65h		Initialize 8237 DMA controller
66h		Clear DMA write request register and mask set/reset register
67h	220	8259 Interrupt controller test
F4h		Enable extended NMI sources
8Ch	140	Initialize remaining Plug-N-Play devices (i.e., other than video), initialize IPL, initialize IDE controller
8Fh	130	Floppy Initialization

92h		Set printer, RS-232 time-out
96h		Optional ROM scan and initialize above C800h
97h	080	Scan User binary flash and conventional option ROM scan
98h		Scan User binary flash area
9Ah		Clear soft reset flag, complete MP Table
9Dh	070	Timer data area initialization
A0h		Printer setup
A1h		RS-232 setup
A2h		Check for stuck key
ABh		Before NPX test and initialization
ACh	060	NPX test and initialization
ADh		Update coprocessor information in CMOS and recalculate checksum
Aeh		Set typematic rate
AFh	050	Keyboard read ID command
B0h		Wait for READ ID response
A3h		Display POST errors
A6h		Before Setup
A7h	030	Call Setup if required, prompt for password if enabled
B1h		Enable Cache for boot
B3h		Setup display mode set
B4H		Jump to pre-OS code
BBh	020	Initialize SMI code, prepare for boot
00h	000	Execute BOOT

5.3 POST Error Codes and Messages

The BIOS indicates errors as follows:

- By writing an error code to the PS/2-standard logging area in the Extended BIOS Data Area
- By displaying a POST Error Code and message on the screen.

Table 5-5 POST Error Codes

Number	Error message
0002	Primary Boot Device Not Found
0010	Cache Memory Failure, Do Not Enable Cache
0015	Primary Output Device Not Found
0016	Primary Input Device Not Found
0041	EISA ID Mismatch for Slot
0043	EISA Invalid Configuration for Slot
0044	EISA configuration NOT ASSURED!
0045	EISA Expansion Board Not Ready in Slot
0047	EISA CMOS Configuration Not Set
0048	EISA CMOS Checksum Failure
0049	EISA NVRAM Invalid
0060	Keyboard Is Locked ... Please Unlock It
0070	CMOS Time & Date Not Set
0080	Option ROM has bad checksum
0083	Shadow of PCI ROM Failed
0084	Shadow of EISA ROM Failed
0085	Shadow of ISA ROM Failed
0131	Floppy Drive A:

continued

Number	Error message
0132	Floppy Drive B:
0135	Floppy Disk Controller Failure
0140	Shadow of System BIOS Failed
0171	CPU Failure - Slot 1, CPU # 1
0172	CPU Failure - Slot 1, CPU # 2
0171	Previous CPU Failure - Slot 1, CPU # 1
0172	Previous CPU Failure - Slot 1, CPU # 2
0175	CPU modules are incompatible
0180	Attempting to boot with failed CPU
0191	CMOS Battery Failed
0195	CMOS System Options Not Set
0198	CMOS Checksum Invalid
0289	System Memory Size Mismatch
0295	Address Line Short Detected
0297	Memory Size Decreased
0299	ECC Error Correction failure
0301	ECC Single bit correction failed, Correction Disabled
0302	ECC Double bit Error
0370	Keyboard Controller Error
0373	Keyboard Stuck Key Detected
0375	Keyboard and Mouse Swapped
0380	ECC SIMM failure, Board in slot 1 SIMM #
0430	Timer Channel 2 Failure

continued

Number	Error message
0440	Gate-A20 Failure
0441	Unexpected Interrupt in Protected Mode
0445	Master Interrupt Controller Error
0446	Slave Interrupt Controller Error
0450	Master DMA Controller Error
0451	Slave DMA Controller Error
0452	DMA Controller Error
0460	Fail-safe Timer NMI Failure
0461	Software Port NMI Failure
0465	Bus Time-out NMI in Slot
0467	Expansion Board NMI in Slot
0501	PCI System Error
0510	PCI Parity Error
0710	System Board Device Resource Conflict
0711	Static Device Resource Conflict
0800	PCI I/O Port Conflict
0801	PCI Memory Conflict
0802	PCI IRQ Conflict
0803	PCI Error Log is Full
0810	Floppy Disk Controller Resource Conflict
0811	Primary IDE Controller Resource Conflict
0812	Secondary IDE Controller Resource Conflict
0815	Parallel Port Resource Conflict

continued

Number	Error message
0816	Serial Port 1 Resource Conflict
0817	Serial Port 2 Resource Conflict
0818	USB 1 …TBD
0819	USB 2 …TBD
0820	Expansion Board Disabled in Slot
0900	NVRAM Checksum Error, NVRAM Cleared
0903	NVRAM Data Invalid, NVRAM Cleared
0905	NVRAM Cleared By Jumper
0982	I/O Expansion Board NMI in Slot
0984	Expansion Board Disabled in Slot
0985	Fail-safe Timer NMI
0986	System Reset caused by Watchdog Timer
0987	Bus Time-out NMI in Slot

6. BOARD SET SPECIFICATIONS

This chapter specifies the operational parameters and physical characteristics for the B440FX DP Server. This is a board-level specification only. System specifications are beyond the scope of this document.

6.1 Absolute Maximum Ratings

Operation of the B440FX DP Server at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 6-1 Absolute Maximum Ratings

Operating Temperature	0°C to +55°C *
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V **
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V

* Chassis design must provide proper airflow to avoid exceeding Pentium Pro maximum case temperature.
** V_{DD} means supply voltage for the device.

Further topics in this chapter specify normal operating conditions for the B440FX DP Server.

6.2 Electrical Specifications

DC specifications for the B440FX DP Server power connectors and module power budgets, are summarized here. Electrical characteristics for major connector interfaces (including DC and AC specifications), can be obtained from other documents:

- PCI bus and Brittany Connectors -- *PCI Local Bus Specification Rev. 2.1*
- EISA slots -- *EISA Bus Specification*

6.2.1 Power Connection

Power supply connection uses two connectors: main and auxiliary. Each signal of the 24-pin main connector attaches to the power supply using 18 AWG wire. The 14-pin auxiliary power connector attaches using 24 AWG wire.

6.2.2 Power Consumption

The following table shows the power consumed on each supply line for a B440FX DP Server with two processors, 8 DIMMs, 6 PCI slot loads (2A @ 5V per slot), and two ISA slot loads (Server Monitor Module and terminal concentrator board).

NOTE: *The following numbers are provided as an example. Actual power consumption will vary depending on the exact B440FX DP Server configuration.*

Table 6-2 B440FX DP Server Power Consumption

Device(s)	3.3V	+5V	+12V	-12V
Processors		8.3 A	3.5 A	
Memory	2.0 A			
Termination	3.4 A			
PMC and DBX	1.0 A			
Baseboard		3 A	.5 A	.1 A
PCI slots		12 A		
ISA slots		1.9 A	2.0 A	.4 A
Total	6.4 A	25.2 A	6.0 A	.5 A

Table 6-3 Sample 330 Watt Power Supply Output Summary

DC Power	3.3VDC at 11A Max.
	+5 VDC at 32A Max.
	+12 VDC at 12 A with 16A/12 sec peak current
	-12 VDC at 0.5A
	-5 VDC at 0.25A.
	5V Standby 100 mA,
	Total combined output power of 3.3v and +5v shall not exceed 178W
AC Line voltage	100-120 VAC, 200-240 VAC, switch selectable
AC Line Frequency	50 / 60 Hz
AC Input Current	7A@ 110 VAC /3.5A@ 210 VAC

6.3 Mechanical Specifications

The following diagrams show the mechanical specifications of the processor board and baseboard. All dimensions are given in inches, as per ANSI Y15.4M. Maximum primary-side component height is .550" unless otherwise noted. Connectors are dimensioned to pin 1. Refer to "Connector Specifications" after the diagrams for more information.

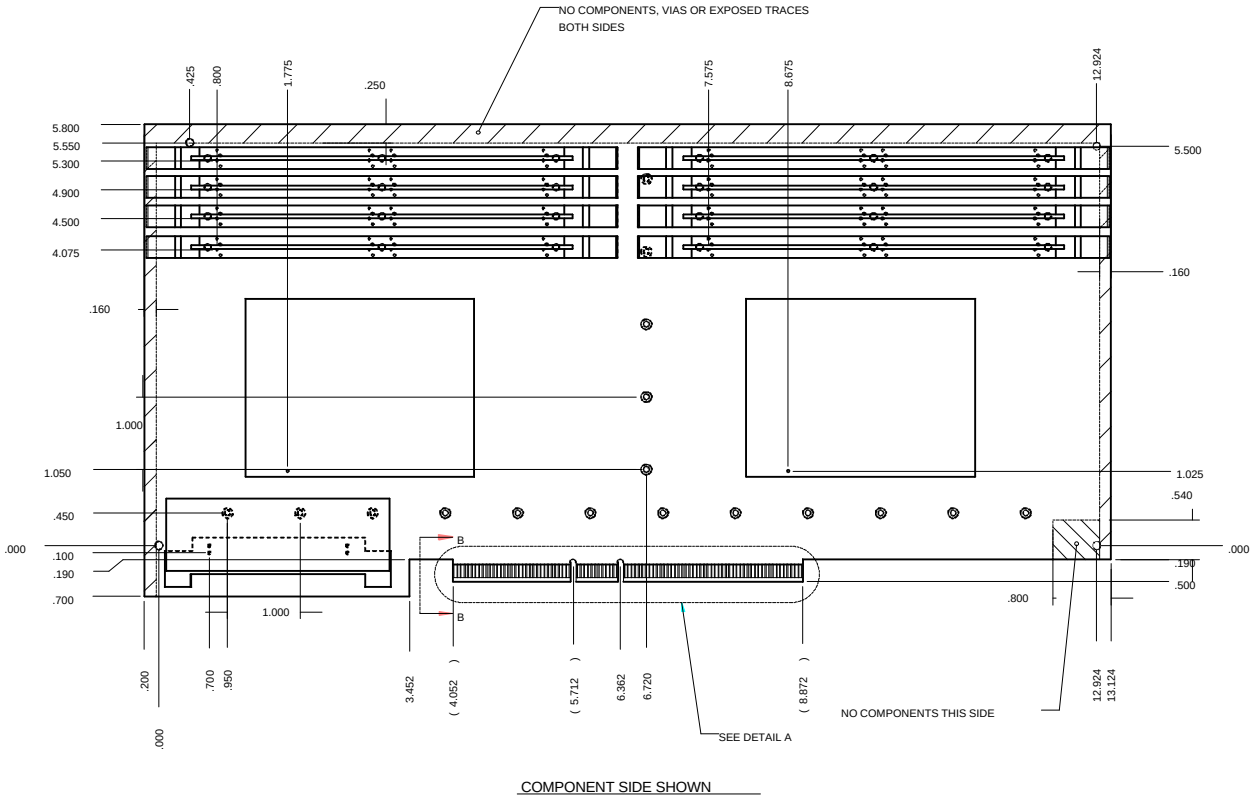


Figure 6-1Processor Board Mechanical Diagram

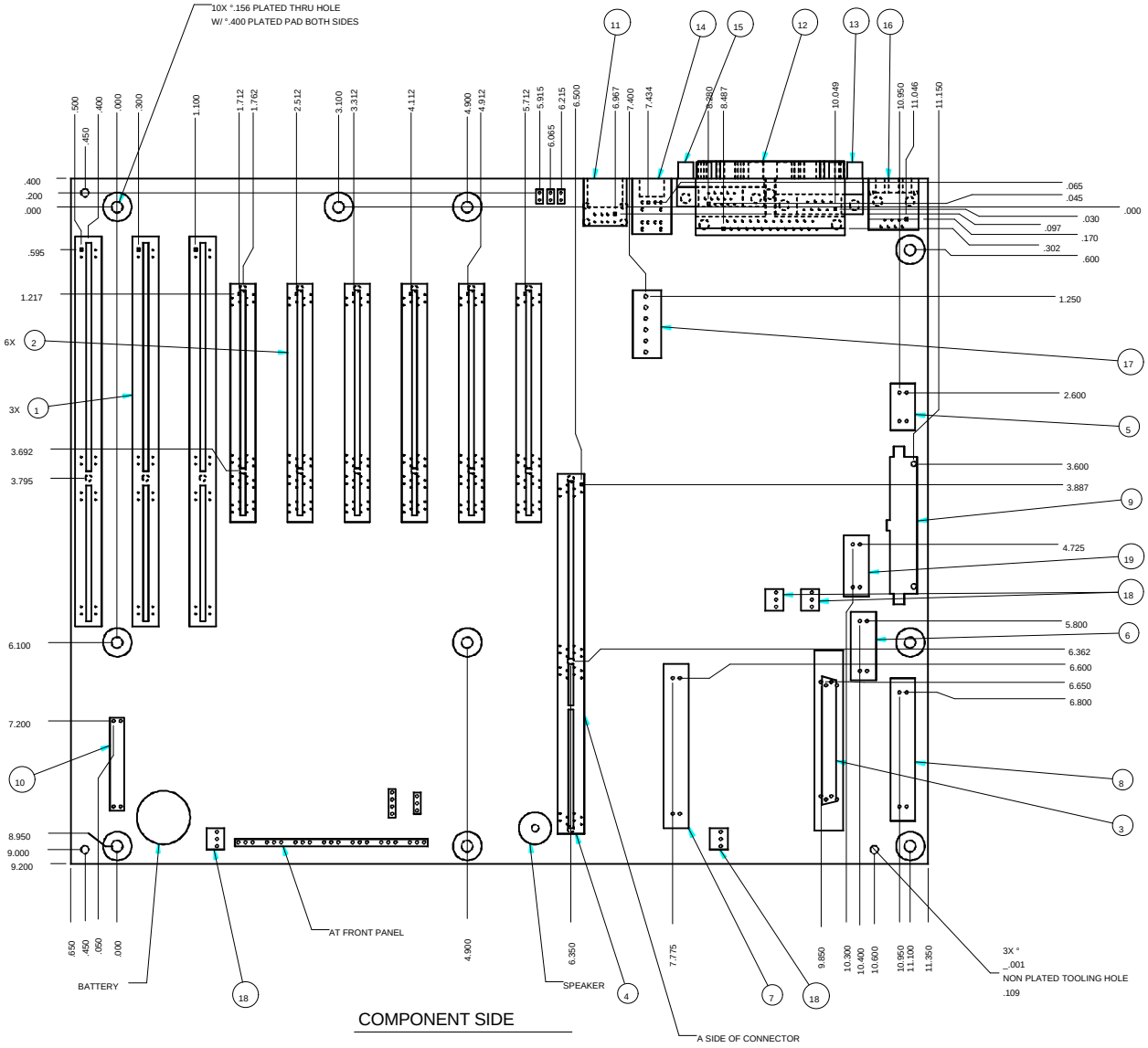


Figure 6-2Baseboard Mechanical Diagram

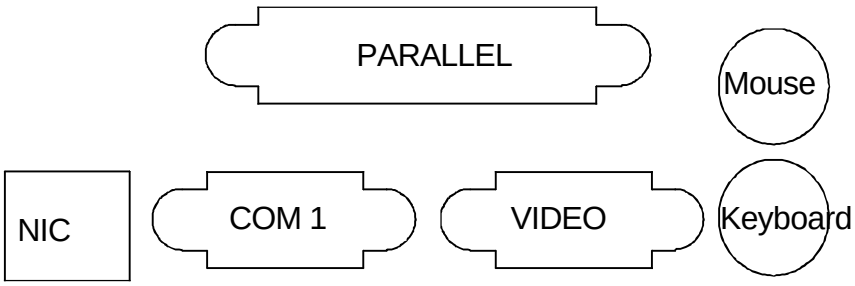


Figure 6-3 I/O Connector Map

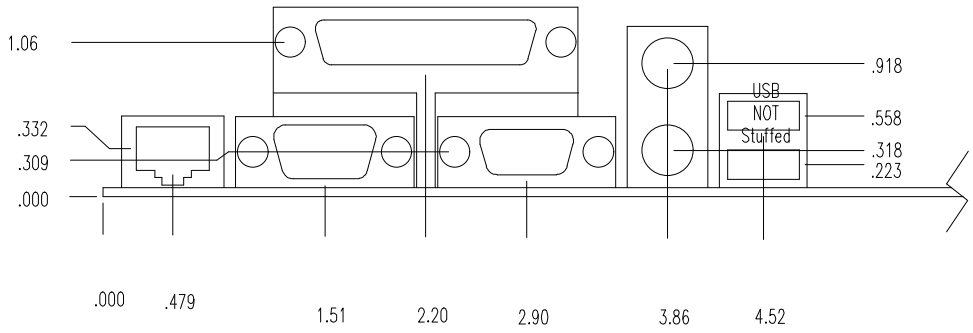


Figure 6-4I/O Connector Mechanical Diagram

6.3.1 PCI and ISA Connectors

The baseboard PCI and ISA connectors adhere to the requirements in the *PCI Local Bus Specification* and *ISA Specification*. Refer to these documents for connector specifications.

6.3.2 Brittany Connector

The baseboard Brittany connector adheres to the requirements in the *PCI Local Bus Specification*. Refer to this document for connector specifications. The following figure shows the details of the processor card edge connector (side A):

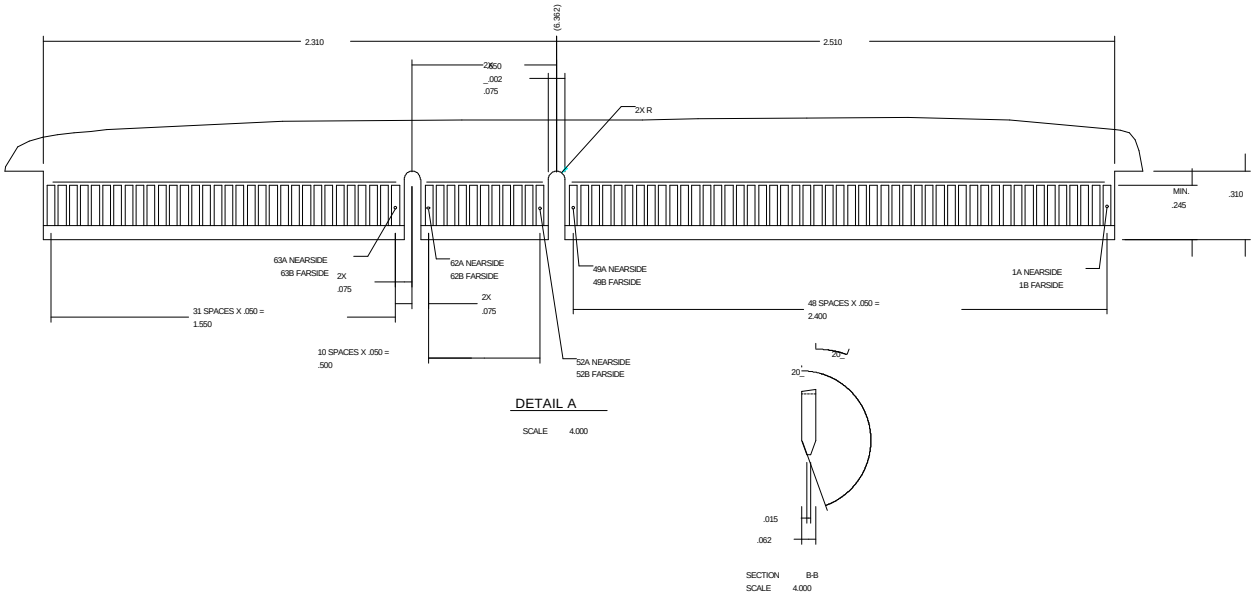


Figure 6-5Brittany Connector Edge Connector

6.4 Temperature Requirements

The system should be cooled adequately to insure that all components included in the system are operating within their rated temperature range. The Pentium Pro processor's operating case temperature range is 0°C to 85°C. Refer to Intel's application note on Thermal Measurements on the Pentium Pro Processor for further information on tools and thermal measurement techniques.

6.5 Shock and Vibration Requirements

The base board and processor board have been designed to withstand a 50g shock, trapezoidal wave with velocity change of 170 in./sec. The base board and processor board have been designed to meet non-operating random vibration of 0.01g2/Hz at 5Hz, sloping to 0.02g2/Hz at 20Hz, level to 0.02g2/Hz to 500Hz. The system should be designed to insure the boards do not exceed these specifications.

6.6 Reliability

6.6.1 Mean Time Between Failure - MTBF

The Mean-Time-Between-Failures (MTBF) data is calculated from predicted data.

Table 6-4 System MTBF

Sub Assembly Description	Calculated MTBF (in hours)
Baseboard (B440FX)	62,065
Processor / Memory board (B440FX)	152,088

6.7 Sample System Environmental Testing

These tests include:

- Temperature Operating and Non-Operating
- Humidity Non-Operating
- Shock Packaged and Unpackaged
- Vibration Packaged and Unpackaged
- AC Voltage, Freq.& Source Interrupt
- AC Surge
- Acoustics
- ESD
- EMC Radiated Investigation

7. SUPPORTED ENVIRONMENTS

NOTE: *This TPS has been published prior to final testing. All supported environments will be verified and periodic updates to this section will be available in the B440FX DP Server Board Set Specification Update.*

7.1 Supported Operating Systems

Explanation of Terms:

UP = Uniprocessor

MP = Multiprocessor

Level 1 = Operating system tested and verified in Intel's Server Validation Laboratory

Level 2 = Operating system tested in Intel's Compatibility Engineering Laboratory

Table 7-7-1 Supported Operating Systems

Level	Operating System	Version #	UP/MP
1	Win NT*	3.51 Server	UP & MP
1	NetWare*	4.11	UP & MP
1	SCO UnixWare*	2.1	UP & MP
1	OS/2*	2.11 SMP	UP & MP
2	Win NT*	4.0 Server	UP & MP
2	SCO UNIX	ODT 5.0	UP & MP
2	NetWare*	3.12	UP
2	NetWare*	4.1	UP
2	Solaris	2.4	UP
2	Solaris	2.5	UP & MP
2	Win NT*	3.51 Workstation	UP & MP
2	MS DOS*	6.22	UP
2	Windows 95*		UP

7.1.1 B440FX DP Server will not support NetWare 4.1 SMP

Novell announced in June 1996 that it had directed resources away from any support for NetWare 4.1 SMP in favor of NetWare 4.11 completion for Q4, 1996. Due to this position and the fact that open issues on 4.1 SMP were not reproducible on NetWare 4.11, Intel's B440FX DP Server team has determined not to support the older NetWare 4.1 SMP. Support for NetWare 4.11 commenced Q3, 1996.

7.2 Supported Adapters

The following is a list of adapter cards Intel plans to test in the B440FX DP Server system. The adapters have been broken down into categories based on their functionality. Within each category they are prioritized much like the O/S testing i.e. higher priority will be given to priority 1 adapters, lower priority to 2 and 3.

Note that testing of the adapter cards is very complex since they must be tested in different slots, with different O/S's, in combination with different adapter cards etc.. A matrix showing which adapter has passed with which O/S, driver version etc. will be provided at a later date and will be updated on a periodic basis.

One final note: All onboard devices are tested by default and are therefore not included in this list (SCSI & NIC)

Level 1 = Operating system tested and verified in Intel's Server Validation Laboratory

Level 2 = Operating system tested in Intel's Compatibility Engineering Laboratory

7.2.1 PCI Hard Disk Controllers

Table 7-2 PCI Hard Disk Controllers

Priority	MFGR	Model	Driver and O/S Tested
1	Adaptec	AHA-3940UW	TBD
1	Mylex	DAC 960PL-2A	TBD
1	DPT	DPT 3224XR-W	TBD
1	SYMBIOS	SYM8751SP	TBD
2	Adaptec	AHA-2940UW	TBD
2	Adaptec	AHA-2940W	TBD
2	Mylex	DAC 960PL	TBD

2	SYMBIOS	NCR8251S	TBD
2	Adaptec	AHA-2940	TBD
2	Adaptec	AHA-3940W	TBD
2	Mylex	DAC 960P	TBD
2	SYMBIOS	NCR8251D	TBD

7.2.2 ISA Hard Disk Controllers

Table 7-3 ISA Hard Disk Controllers

Priority	MFGR	Model	Driver and O/S Tested
1	Adaptec	AHA-1520B	TBD

7.2.3 PCI Network Interface Cards

Table 7-4 PCI Network Interface Cards

Priority	MFGR	Model	Driver and O/S Tested
1	3Com	3C595-TX	TBD
1	Intel	Pro/100B	TBD
1	SMC	SMC9332DST	TBD
1	RNS	2340-TX (2340-20)	TBD
2	Intel	Pro/100S	TBD
2	Cogent	EM964	TBD
2	AMD	PCNet/PCI	TBD
2	SMC	SMC8434	TBD

7.2.4 ISA Ethernet Network Interface Cards

Table 7-5 ISA Ethernet Network Interface Cards

Priority	MFGR	Model	Driver and O/S TestedComment
1	IBM	25H3501	TBD
2	Intel	Pro 10	TBD

7.2.5 PCI Token Ring Network Interface Cards

Table 7-6 PCI Token Ring Network Interface Cards

Priority	**MFGR**	**Model**	**Driver and O/S Tested**
2	IBM	IBM 3 Port PCI Token Ring	TBD

7.2.6 Server Management Cards

Table 7-7 Server Management Cards

Priority	**MFGR**	**Model**	**Driver and O/S Tested**
1	Intel	Server Monitor Module	TBD

7.2.7 PCI Video Adapters

Table 7-8 PCI Video Adapters

Priority	**MFGR**	**Model**	**Driver and O/S Tested**
2	ATI	GRAPHICS PRO TURBO VRAM (Mach 64)	TBD
2	#9	GXE64PRO 4MB	TBD
2	Diamond	Stealth 64 4MB VRAM (S3 86C964)	TBD

7.3 Supported Drivers

Table 7-9 Supported Drivers - Ships with Systems

	Video (Cirrus 54M40)	NIC (Intel 82557-Tx)	SCSI (Adaptec 7880)
Windows NT v3.51	X	X	X
NetWare 3.12		X	X
NetWare 4.1		X	X
UnixWare 2.1		X	X
SCO Unix ODT v 5.0			X
OS/2 2.11 SMP		X	X
Windows 95	X	X	X
DOS v 6.22	X		X

7.4 Memory and Processor Upgrades

7.4.1 Memory

Eight 168-pin gold leaded sockets on the processor/memory module will accept up to 1 GB of system memory using 60 ns fast page or EDO 3.3V buffered DIMMs of the following sizes: 1M x 72 (8 MB), 2M x 72 (16 MB), 4M x 72 (32 MB), 8M x 72 (64 MB), and 16M x 72 (128 MB) DIMMs. The minimum memory size is 16 MB and the maximum memory size, using eight 128 MB DIMMs, is 1 GB.

The eight DIMM sockets are arranged as eight banks (Bank 0 through 7) with each bank consisting of one socket. The DIMMs should be populated through succeeding banks until all eight banks are filled (E.G. Bank 0, then Bank 1, 2…and finally Bank 7). Separate banks may have different sizes and types of memory installed. In some instances, for electrical reasons only, it may be essential to populate Bank 0 first.

System memory begins at address 0 and is contiguous (flat addressing) up to the maximum amount of system memory installed. The only places where system memory is non-contiguous is in the ranges from 00080000 - 000FFFFF (the DOS compatibility region) and 00F00000 - 00FFFFFF (the system BIOS region). Memory holes at any other location may result in DRAM beyond that hole unusable.

Because of the constant changes in the memory market, Intel engineering continually analyzes DIMMs by comparing information in the DIMM vendor's data book with the required timings on the B440FX DP Server baseboard. Memory also is tested by either Intel or by respected OEM customers.

The following tables list DIMMs that are known to be compatible with the specified Intel platforms. DIMMs that are not listed also should function properly as long as their specifications are compatible with the devices listed below. Although Intel goes to great lengths to insure SIMM or DIMM compatibility in its systems, Intel makes no

claim that any SIMM or DIMM will work in all instances. In general, DIMM devices that are faster than those specified for a given platform will work although no extra performance will be realized. The DIMM devices shown are categorized according to the following level of qualification:

The following tables list DIMM devices known to be compatible with the specified Intel platforms. In general, DIMM devices which are faster than those specified for a given platform will work although no extra performance will be realized. The memory devices shown are categorized according to four levels of qualification:

1. **Intel Tested and Approved (on Intel's AML)**: The DIMM device has been electrically tested by Intel engineering and is known to be compatible with the server baseboard or associated memory module. Rigorous environmental testing, voltage margin, shock, and vibration testing were conducted on these DIMM devices. In addition, the vendor has met or exceeded Intel's product change, quality control, and availability requirements. The DIMM device is on the Intel Approved Manufacturing List (AML) and has an Intel part number associated with the device.

2. **Intel Tested (not on Intel's AML)**: The DIMM device has been electrically tested by Intel engineering and is known to be compatible with the server baseboard or associated memory module. Rigorous environmental testing, voltage margin, shock, and vibration testing were conducted on these DIMM devices. The vendor has met Intel's product change, quality control, and availability requirements. The DIMM device is not on the Intel Approved Manufacturing List, but maybe listed in the tables below.

3. **Paper Qualification**: The DIMM device have been analyzed by the data sheet and have been electrically tested. A small sample (normally 12 DIMMs) have been tested by either Intel engineering, OEM engineering or the DIMM manufacturer across voltage and temperature margins on the baseboard and/or memory modules. The DIMM devices are not on the Approved Manufacturing list and are not listed on the tables below.

4. **Customer Tested**: The DIMM has been electrically tested by an OEM customer and is reported to be compatible with the server platform system. The DIMM devices are not on the Approved Manufacturing list, and are not listed on the tables below.

Intel recommends that DIMMs listed as (1) *Intel Approved and Tested* or (2) *Intel Tested* be used to ensure reliable system operation. DIMM devices not listed or listed as (4) *Customer Tested* can be used; but, in the event of unreliable system operation, the DIMM devices should be replaced with DIMMs tested by Intel (1 or 2) to determine whether the DIMM devices are causing the problem.

Table 7-10 Qualified DIMM Memory

BB440FX DP Server System Intel Approved and Qualified DIMM Modules				
Manufacturer	**Part Number**	**Intel Part #**	**DIMM Type**	**Size**
Samsung	KMM372F124AJ-6	800061-060	1Mx72	8MB
IBM	IBM11M1730BBH-60	n/a	1Mx72	8MB
Simple Tech	I721007D1-6GVSASCA	n/a	1Mx72	8MB
Samsung	KMM372F213AJ-6	800062-060	2Mx72	16MB
Micron	MT9LD272G-60X	800062-060	2Mx72	16MB
IBM	IBM11M2735HBE-60	n/a	2Mx72	16MB
Micron	MT18LD472G-60X	800071-060	4Mx72	32MB
IBM	IBM11M4735CBE-60J	n/a	4Mx72	32MB
Samsung	KMM372V400AS-6	n/a	4Mx72	32MB
Samsung	KMM372F803AK-6	800072-060	8Mx72	64MB
Samsung	KMM372F1600AK-60	800091-060	16Mx72	128MB

CAUTION: *DIMM devices with gold contacts should NOT be placed into DIMM sockets with tin lead contacts or vice-versa. Mixing dissimilar metal contact types has been shown to result in unreliable memory operation. For more information, see FaxBack document 4229. Intel recommends similar manufacturer and similar speeds in each bank on the memory module. This document contains information which is the proprietary property of Intel Corporation. This document is received in confidence and its contents may not be disclosed or copied without the prior written consent of Intel Corporation. Nothing in this document constitutes a guaranty, warranty, or license, express or implied. Intel disclaims all liability for all such guaranties, warranties, and licenses, including but not limited to: Fitness for a particular purpose; merchantability; not infringement of intellectual property or other rights of any third party or of Intel; indemnity; and all others. The reader is advised that third parties may have intellectual property rights which may be relevant to this document and the technologies discussed herein, and is advised to seek the advice of competent legal counsel, without obligation of Intel. Intel retains the right to make changes to this document at any time, without notice. Intel makes no warranty for the use of this document and assumes no responsibility for any errors which may appear in the document nor does it make a commitment to update the information contained herein.*

7.4.2 Processors

Single-processor B440FX DP Server platforms can be upgraded by using a processor with a faster clock speed. The baseboard is designed to operate with 166, 180 or 200MHz Pentium® Pro processors. Dual-processor configurations must always have Pentium Pro processors with the same clock speed and processor stepping installed in the two Zero Insertion Force (ZIF) sockets. When upgrading processors, it is also important to ensure the processors Speed jumpers are set correctly. The second processor will require a heatsink compatible with the socket on the B440FX DP Server baseboard. In addition, a conductive compound should be used between the processor and the heatsink. This assembly (without the processor) can now be ordered from the factory:

Order code ABUC2NDCPUA (VRM included).

The second processor upgrade on the B440FX DP Server baseboard must match exactly the following characteristics of the primary processor: External Clock Speed and Internal Clock Speed. Use the following table when contacting your service provider for the second processor. To determine what processor to use in the secondary socket, match the Product code and S-Spec number on your installed processor to the secondary processor. The Product code / S-Spec number can be found on the under side of the processor.

Table 7-11 Supported Processors (Preliminary)

Processor	Part_number / S Spec	Stepping (Proc/Cache)
166/512	KB80521EX166512 S Y047	A-1/B-0
200/512	KB80521EX200512 S Y048	A-1/B-0
200/256	KB80521EX200256 S Y040	A-1/B-2
200/256	KB80521EX200256 S Y032	A-1/B-2

7.4.3 Video DRAM

Video DRAM memory can be upgraded using one 256K x 16, 60 ns, SOJ component. Unlike the system DRAM, we do not qualify video DRAM vendors. The examples below have been used and have no known issues with the B440FX DP Server baseboard.

Table 7-12 Video DRAM Vendors

Manufacturer	Part Number
Samsung	KM416C256AJ-6T
Micron Technology	MR4C1625DJ-6TR
Samsung	KM416C256BJ-6T
Siemens Corp.	HYB514171BJ-60
Hyundai	HY514260BJC-60
Oki Semiconductor	M514260BSL-60J

Contact your local sales office to obtain the latest specifications before placing your order.

8. CONNECTOR PINOUTS

Table 8-8-1 Brittany Connector Signal Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	5V	B1	5V	A49	GND	B49	spare
A2	5V	B2	5V	A50	key	B50	key
A3	spare	B3	5V	A51	key	B51	key
A4	ELOCK	B4	spare	A52	PA_AD26	B52	PA_AD27
A5	GND	B5	ESERR	A53	PA_AD28	B53	GND
A6	HOST_CLK	B6	GND	A54	3.3V	B54	PA_AD29
A7	5V	B7	P_CLK_SL1	A55	PA_AD30	B55	CPUMOD_RST_L
A8	REF_PCI_CLK	B8	5V	A56	PA_AD31	B56	3.3V
A9	GND	B9	P_CLK_SL2	A57	GND	B57	P_GNT_SLOT1_L
A10	CPU1_PIC_CLK	B10	GND	A58	P_REQ_SLOT1_L	B58	GND
A11	5V	B11	P_CLK_SL3	A59	3.3V	B59	P_GNT_SLOT2_L
A12	P_VGA_CLK	B12	5V	A60	P_REQ_SLOT2_L	B60	3.3V
A13	GND	B13	P_SCSI _CLK	A61	GND	B61	P_GNT_SLOT3_L
A14	P_PCEB_CLK	B14	GND	A62	P_REQ_SLOT3_L	B62	GND
A15	5V	B15	FRB_RST_L	Key		Key	
A16	UCTRLR12_CLK	B16	5V	Key		Key	
A17	GND	B17	P_GNT_SLOT0_L	A63	3.3V	B63	P_GNT_DEC_L
A18	P_REQ_SLOT0_L	B18	GND	A64	P_REQ_DEC_L	B64	3.3V
A19	GND	B19	CPU_INIT_L	A65	GND	B65	PA_PERR_L
A20	PA_AD00	B20	PA_AD01	A66	PA_SERR_L	B66	GND
A21	PA_AD02	B21	GND	A67	3.3V	B67	APIC_ACK2
A22	GND	B22	PA_AD03	A68	PIIX3_PHLDA_L	B68	3.3V
A23	PA_AD04	B23	PA_AD05	A69	GND	B69	PMC_PHOLD_L
A24	PA_AD06	B24	GND	A70	P_PCI_RST_L	B70	GND

A25	3.3V	B25	PA_AD07	A71	3.3V	B71	PMC_PCI_CLK
A26	PA_CBE0_L	B26	PA_AD08	A72	TEMP1	B72	3.3V
A27	PA_AD09	B27	3.3V	A73	TEMP2	B73	CPU_SMI_L
A28	GND	B28	PA_AD10	A74	GND	B74	SMI_REQ_L
A29	PA_AD11	B29	PA_AD12	A75	P6_PWR_GD	B75	GND
A30	PA_AD13	B30	GND	A76	INIT_PMC_L	B76	PICD0
A31	3.3V	B31	PA_AD14	A77	GND	B77	PICD1
A32	PA_AD15	B32	PA_CBE1_L	A78	LINT0_INTR	B78	GND
A33	PA_PAR	B33	3.3V	A79	LINT1_NMI	B79	A20GATE_L
A34	GND	B34	PA_PLOCK_L	A80	GND	B80	FERR_L
A35	PA_STOP_L	B35	GND	A81	IGNNE_L	B81	GND
A36	3.3V	B36	PA_DEVSEL_L	A82	spare	B82	P_IERR
A37	PA_TRDY_L	B37	3.3V	A83	GND	B83	GND
A38	GND	B38	PA_IRDY_L	A84	ID0_CPUMOD	B84	CLK_SEL0
A39	PA_FRAME_L	B39	GND	A85	ID1_CPUMOD	B85	CLK_SEL1
A40	3.3V	B40	PA_CBE2_L	A86	ID2_CPUMOD	B86	GND
A41	PA_AD16	B41	PA_AD17	A87	ID3_CPUMOD	B87	CPU0_PIC_CLK
A42	PA_AD18	B42	3.3V	A88	GND	B88	GND
A43	GND	B43	PA_AD19	A89	I2C_SDA	B89	I2C_SCL
A44	PA_AD20	B44	PA_AD21	A90	GND	B90	GND
A45	PA_AD22	B45	GND	A91	spare	B91	STOP_TIMER
A46	5V	B46	PA_AD23	A92	12V	B92	12V
A47	PA_AD24	B47	PA_CBE3_L	A93	12V	B93	12V
A48	PA_AD25	B48	5V	A94	12V	B94	12V

Table 8-8-2 PCI Connector Signal Descriptions

Type	Description
in	Input is a standard input-only signal.
Out	Totem Pole Output is a standard active driver.
T/s	Tri-State is a bi-directional, tri-state input/output pin.
S/t/s	Sustained Tri-State is an active low tri-state signal owned and driven by one and only one agent at a time, subject to specific timing restrictions.
O/d	Open Drain allows multiple devices to share signals as a wired-OR.

Signal	Type	Name and Description
AD[31::00]	t/s	Address and Data are multiplexed; during the first clock of a transaction (address phase) they contain a 32-bit physical address; during subsequent clocks, data. As address bits, AD0 and AD1 have no significance; instead, they are encoded to indicate the burst type.
C/BE[3::0]#	t/s	Bus Command and Byte Enable are multiplexed; during the address phase of a transaction, they define the bus command; during the data phase they determine which byte lanes carry valid data.
DEVSEL#	s/t/s	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, it indicates whether any device on the bus has been selected.
FRAME#	s/t/s	Cycle Frame is driven by the current master to indicate the beginning and duration of an access.
GNT#	in	Grant indicates to the agent that the arbiter has granted access to the bus. This is a point to point signal. Every master has its own GNT#.
IDSEL	in	Initialization Device Select is used as a chip select instead of the upper 24 address lines during configuration read and write transactions.
IRDY#	s/t/s	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. During a write, IRDY# indicates that valid data is present. During a read, it indicates the master is prepared to accept data.
INT[A-D]#	o/d	Interrupts are defined as "level sensitive" and asserted low using open drain output drivers. The assertion and deassertion of INT[A-D]# lines is asynchronous to CLK.
LOCK#	s/t/s	Lock indicates an atomic operation that may require multiple transactions to complete.
PAR	t/s	Indicates even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents.

Continued

PERR#	s/t/s	Parity Error reports a data parity error on all commands except Special Cycle.
PRSNT1# PRSNT2#	in	Present Lines indicate the presence of a PCI add-in board in the connector, and the power requirements of the add-in board.
REQ#	out	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ#.
RST#	in	Reset forces the PCI sequencer of each device to a known state.
SBO#	in/out	Snoop Backoff indicates whether the current memory access may proceed or is required to be retried.
SDONE	in/out	Snoop Done indicates the status of the snoop for the current cache access.
SERR#	o/d	System Error reports address parity errors, data parity errors on Special Cycle commands, or any other system error where the result will be catastrophic.
STOP#	s/t/s	Stop indicates the current target is requesting the Master to stop the current transaction.
TCK	in	Test Clock clocks state information and data into and out of the device during boundary scan. All of the test related pins conform to the Test Access Port (TAP) and Boundary Scan Architecture defined by IEEE Standard 1149.1
TDI	in	Test Input shifts data and instructions into the TAP in a serial manner.
TDO	out	Test Output shifts data out of the device. If an add-in card does not implement a TAP, TDI and TDO should be tied together.
TMS	in	Test Mode Select controls the state of the TAP controller.
TRDY#	s/t/s	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. During a read TRDY# indicates that valid data is present. During a write it indicates the target is prepared to accept data.
TRST#	in	Test Reset is used to force the TAP controller into a test logic reset state.

Table 8-3 PCI Connector Signal Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	-12V	A32	AD17	B1	TRST_L (p/d)	B32	AD16
A2	TCK (p/d)	A33	C/BE2_L	B2	+12V	B33	+3.3V
A3	GND	A34	GND	B3	TMS (p/u)	B34	FRAME_L
A4	TDO (n/c)	A35	IRDY_L	B4	TDI (p/u)	B35	GND
A5	+5V	A36	+3.3V	B5	+5V	B36	TRDY_L
A6	+5V	A37	DEVSEL_L	B6	INTA_L	B37	GND
A7	INTB_L	A38	GND	B7	INTC_L	B38	STOP_L
A8	INTD_L	A39	LOCK_L	B8	+5V	B39	+3.3V
A9	PRSNT1_L	A40	PERR_L	B9	Reserved	B40	SDONE (p/u)
A10	Reserved	A41	+3.3V	B10	+5V	B41	SBO_L (p/u)
A11	PRSNT2_L	A42	SERR_L	B11	Reserved	B42	GND
A12	GND	A43	+3.3V	B12	GND	B43	PAR
A13	GND	A44	C/BE1_L	B13	GND	B44	AD15
A14	Reserved	A45	AD14	B14	Reserved	B45	+3.3V
A15	GND	A46	GND	B15	RST_L	B46	AD13
A16	CLK	A47	AD12	B16	+5V	B47	AD11
A17	GND	A48	AD10	B17	GNT_L	B48	GND
A18	REQ_L	A49	GND	B18	GND	B49	AD9
A19	+5V	A50	key	B19	Reserved	B50	key
A20	AD31	A51	key	B20	AD30	B51	key
A21	AD29	A52	AD8	B21	+3.3V	B52	C/BE0_L
A22	GND	A53	AD7	B22	AD28	B53	+3.3V
A23	AD27	A54	+3.3V	B23	AD26	B54	AD6

continued

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A24	AD25	A55	AD5	B24	GND	B55	AD4
A25	+3.3V	A56	AD3	B25	AD24	B56	GND
A26	C/BE3_L	A57	GND	B26	IDSEL	B57	AD2
A27	AD23	A58	AD1	B27	+3.3V	B58	AD0
A28	GND	A59	+5V	B28	AD22	B59	+5V
A29	AD21	A60	ACK64_L (p/u)	B29	AD20	B60	REQ64_L (p/u)
A30	AD19	A61	+5V	B30	GND	B61	+5V
A31	+3.3V	A62	+5V	B31	AD18	B62	+5V

Table 8-4 PCI - Bus # Configuration IDs

PCI-0 Configuration IDs		PCI-1 Configuration IDs	
IDSEL Value	*Device*	*IDSEL Value*	*Device*
24	PCI-0 Slot 1	21	AIC-7880
25	PCI-0 Slot 2	24	PCI-1 Slot 1
26	PCI-0 Slot 3	26	i82557
27	PCI-0 Slot 4	27	PCI-1 Slot 2
29	PIIX3	31	CL-GD54M40
31	PCI-to-PCI Bridge		

Table 8-5 Add-in Hard Disk Controller Activity Connector Pinout

Pin	Name
1	N/C
2	+5V
3	+5V
4	N/C

Table 8-6 ISA Connector Signal Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	IOCHK_L	A26	SA5	B01	GND	B26	DACK2_L
A02	SD7	A27	SA4	B02	RESDRV	B27	TC
A03	SD6	A28	SA3	B03	+5V	B28	BALE
A04	SD5	A29	SA2	B04	IRQ9	B29	+5V
A05	SD4	A30	SA1	B05	-5V	B30	OSC
A06	SD3	A31	SA0	B06	DRQ2	B31	GND
A07	SD2	C01	SBHE_L	B07	-12V	D01	MEMCS16_L
A08	SD1	C02	LA23	B08	NOWS_L	D02	IOCS16_L
A09	SD0	C03	LA22	B09	+12V	D03	IRQ10
A10	IOCHRDY	C04	LA21	B10	GND	D04	IRQ11
A11	AEN	C05	LA20	B11	SMWTC_L	D05	IRQ12
A12	SA19	C06	LA19	B12	SMRDC_L	D06	IRQ15
A13	SA18	C07	LA18	B13	IOWC_L	D07	IRQ14
A14	SA17	C08	LA17	B14	IORC_L	D08	DACK0_L
A15	SA16	C09	MRDC_L	B15	DACK3_L	D09	DRQ0
A16	SA15	C10	MWTC_L	B16	DRQ3	D10	DACK5_L
A17	SA14	C11	SD8	B17	DACK1_L	D11	DRQ5
A18	SA13	C12	SD9	B18	DRQ1	D12	DACK6_L
A19	SA12	C13	SD10	B19	REFRESH_L	D13	DRQ6
A20	SA11	C14	SD11	B20	BCLK	D14	DACK7_L
A21	SA10	C15	SD12	B21	IRQ7	D15	DRQ7
A22	SA9	C16	SD13	B22	IRQ6	D16	+5V
A23	SA8	C17	SD14	B23	IRQ5	D17	MASTER16_L
A24	SA7	C18	SD15	B24	IRQ4	D18	GND
A25	SA6	--	--	B25	IRQ3	--	--

Table 8-7 Video Port Connector Pinout

Pin	Signal	Description
1	RED	Analog color signal R
2	GREEN	Analog color signal G
3	BLUE	Analog color signal B
4	n/c	No connect
5	GND	Video ground (shield)
6	GND	Video ground (shield)
7	GND	Video ground (shield)
8	GND	Video ground (shield)
9	n/c	No connect
10	GND	Video ground
11	n/c	No connect
12	DDCDAT	Monitor power control
13	HSYNC	Horizontal Sync
14	VSYNC	Vertical Sync
15	DDCCLK	Monitor power control

Table 8-8 IDE Connector Pinout

Pin	Function	Pin	Function
1	IDERST_L	21	IDEDRQ
2	GND	22	GND
3	ID7	23	DIOW_L
4	ID8	24	GND
5	ID6	25	DIOR_L
6	ID9	26	GND
7	ID5	27	IORDY
8	ID10	28	SPSYNC (0Ω to GND)
9	ID4	29	IDEDACK_L
10	ID11	30	GND
11	ID3	31	IDEIRQ14
12	ID12	32	IDEIO16_L
13	ID2	33	IDESA1
14	ID13	34	PDIAG_L
15	ID1	35	IDESA0
16	ID14	36	IDESA2
17	ID0	37	IDECS0_L
18	ID15	38	IDECS1_L
19	GND	39	IDEHDACT_L / DRVPRES_L
20	Keyed	40	GND

For proper IDE operation, cable length is specified as shown in the following figure. If no drives are present on an IDE channel, the cable must be removed. If only one drive is installed, it must appear at the end of the cable.

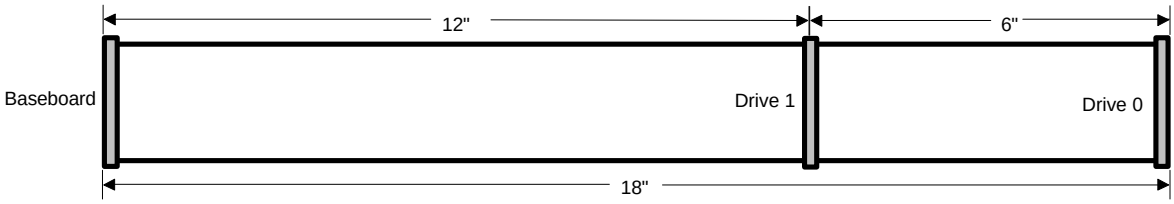


Figure 8-1 IDE Cable Requirements

Table 8-9 Keyboard Connector Pinout

Pin	Signal	Description
1	KEYDAT	Keyboard Data
2	(NC)	
3	GND	
4	FUSED_VCC	
5	KEYCLK	Keyboard Clock
6	(NC)	

Table 8-10 Wide SCSI Connector Pinout

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	18	TERMPWR	35	DAT_12	52	TERMPWR
2	GND	19	N/C	36	DAT_13	53	N/C
3	GND	20	GND	37	DAT_14	54	GND
4	GND	21	GND	38	DAT_15	55	ATN
5	GND	22	GND	39	CDPH	56	GND
6	GND	23	GND	40	DAT_0	57	BSY
7	GND	24	GND	41	DAT_1	58	ACK
8	GND	25	GND	42	DAT_2	59	RESET
9	GND	26	GND	43	DAT_3	60	MSG
10	GND	27	GND	44	DAT_4	61	SEL
11	GND	28	GND	45	DAT_5	62	CD
12	GND	29	GND	46	DAT_6	63	REQ
13	GND	30	GND	47	DAT_7	64	I/O
14	GND	31	GND	48	CDPL	65	DAT_8
15	GND	32	GND	49	GND	66	DAT_9
16	GND	33	GND	50	GND	67	DAT_10
17	TERMPWR	34	GND	51	TERMPWR	68	DAT_11

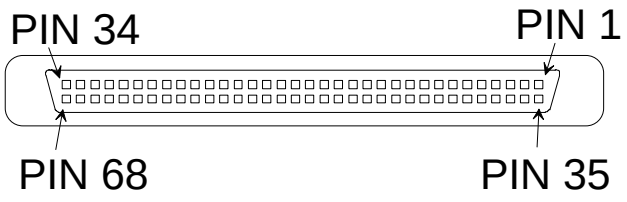


Figure 8-2Wide SCSI Connector

Table 8-11 Serial Port Connector Pinout

Pin	Name	Description
1	DCD	Data Carrier Detected
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Return to Send
8	CTS	Clear to Send
9	RIA	Ring Indication Active
10	key	Keying pin (Serial B header only)

Table 8-12 Parallel Port Connector Pinout

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

Table 8-13 Floppy Port Connector Pinout

Pin	Name	Pin	Name
1	GND	18	FD_DIR_L
2	FD_DENSEL	19	GND
3	GND	20	FD_STEP_L
4	n/c	21	GND
5	Key	22	FD_WDATA_L
6	FD_DRATE0	23	GND
7	GND	24	FD_WGATE_L
8	FD_INDEX_L	25	GND
9	GND	26	FD_TRK0_L
10	FD_MTR0_L	27	FD_MSEN0
11	GND	28	FD_WPROT_L
12	FD_DR1_L	29	GND
13	GND	30	FD_RDATA_L
14	FD_DR0_L	31	GND
15	GND	32	FD_HDSEL_L
16	FD_MTR1_L	33	GND
17	FD_MSEN1	34	FD_DSKCHG_L

Table 8-14 Mouse Connector Pinout

Pin	Signal	Description
7	MSEDAT	Mouse Data
8	(NC)	
9	GND	
10	FUSED_VCC	
11	MSECLK	Mouse Clock
12	(NC)	

*Table 8-15 Server Monitor Module (SMM) Feature Connector Signal Descriptions**

Pin	Signal	Type	Description
1	SMI#	Input	System management interrupt
2	I2C_CLK	Output	I^2C clock (8 MHz)
3	GND	Power	Ground
4	Reserved		No connection
5	PWROFF#	Output	Power supply off (active low)
6	I2CDATA	I/O	I^2C data signal
7	LPOK	Input	Host line power okay
8	KEYUNLK#	Input	Keyboard unlock
9	NMI	Input	Nonmaskable interrupt
10	3.3 V	Input	3.3 V power
11	RESET#	Output	Reset system board
12	GND	Power	Ground
13	GND	Power	Ground
14	Reserved		No connection
15	SECURE	Input	Host in secure mode
16	GND	Power	Ground
17	INTRUD	Input	Chassis is open
18	Reserved		No connection (reserved for future use)
19	Reserved		No connection
20	GND	Power	Ground
21	Reserved		No connection
22	Reserved		No connection
23	POWERGD		Power to system is within specification
24	Reserved		No connection
25	Reserved		No connection, pin missing
26	Reserved		No connection

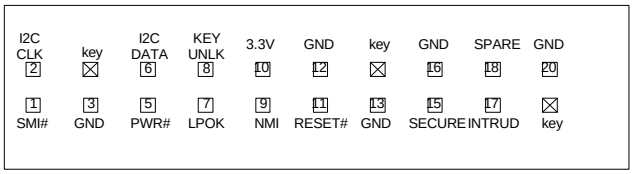


Figure 8-3 SMM Feature Connector Layout

Table 8-16 12V Fan Pinout

Pin	Signal	Description
1	+12V	
2	Sense	Fan Rotation Sense, pulse output, frequency directly proportional to RPM of the Fan
3	GND	

Table 8-17 5V Fan Pinout

Pin	Signal	Description
1	+5V	
2	N/C	
3	GND	

Table 8-18 RJ-45 Network Connector Pinout

(Standard Ethernet 10Base-T ,100Base-TX)

Pin	Signal	Description
1	TXP	
2	TXM	
3	RXP	
4	TERM1	
5	TERM1	
6	RXM	
7	TERM2	
8	TERM2	

Table 8-19 Universal Serial Bus Connector Pinout

(As of July 1996 - NOT STUFFED)

Pin	Signal	Description
1	5VCC	
2	USB_P0_NR	
3	USB_P0_PR	
4	GND	
5	5VCC	
6	USB_P1_NR	
7	USB_P1_PR	
8	GND	

Table 8-20 14-pin Auxiliary Power Connector Pinout

Pin	Signal	Pin	Signal
1	Remote Sense return	8	Power Good
2	5V Remote Sense	9	PS on
3	3.3V remote sense	10	COM
4	COM	11	5VSB
5	N/C	12	KEY (Amp 87077-2)
6	N/C	13	24vdc
7	COM	14	24vdc Return

Table 8-21 24-pin Main Power Connector Pinout

Pin	Signal	Pin	Signal
1	+5 Vdc	13	+5 Vdc
2	+5 Vdc	14	+5 Vdc
3	-5 Vdc	15	+5 Vdc
4	-12Vdc	16	+5 Vdc
5	COM	17	COM
6	COM	18	COM
7	COM	19	COM
8	COM	20	COM
9	COM	21	COM
10	+3.3Vdc	22	+3.3Vdc
11	+12Vdc	23	+3.3Vdc
12	+12Vdc	24	+12Vdc

*Table 8-22 PCI Compliant 3.3V Connector Pinout**

Pin	Signal
1	GND
2	GND
3	GND
4	PCI 3.3V
5	PCI 3.3V
6	PCI 3.3V

*Power supplies shipped with Intel's SSPD systems do not supply power to this connector.

Table 8-23 I^2C Connector Pinout

Pin	Name
1	Local I^2C SCL
2	GND
3	Local I^2C SDA

Table 8-24 Front Panel Connector Pinout

Pin	Name	Description
1	GND	0V
2	Hard Drive-Activity	TTL Low true = hard disk activity, requires series R for LED
3	Reset	TTL Low True = reset system
4	Power-Control	TTL Low True = toggle system power
5	VCC	+5V
6	N/C	Spare
7	NMI	TTL Low True = NMI to CPU
8	VCC	+5V
9	Fan-Failed	TTL Low True = fan failed, requires series R for LED
10	Chassis - Intrusion	TTL High True = chassis intrusion, This signal comes from the chassis
11	Power-Fault	TTL Low True = power fault condition, requires series R for LED
12	+5V-STBY	+5V-Standby
13	I^2C-SDA	I^2C - SDA (Serial Data)
14	GND	0V
15	I^2C-SCL	I^2C - SCL (Serial Clock)
16	GND	0V

Table 8-25 Connector Specifications

Item	Qty.	Mfr(s). and Part #	Description
1	3	AMP 176139-2	ISA bus add-in card connector
2	6	AMP 646255-1	PCI add-in card connector
3	1	AMP 74931-7	68-pin SCSI connector
4	1	AMP 145169-4	Brittany Connector
5	1	AMP111950-1	Second Serial Port Header
6	1	AMP 111950-3	Front panel connector
7	1	3M 2450-60Y2UB or G	IDE connector
8	1	3M 2534-60V2UG	Floppy connector
9	1	Molex 39-01-2240	24-pin power connector onboard
10	1	Molex 39-01-2204	24-pin power connector from supply
11	1	Fox Conn/Hon Haj HC11131-KD6	Server Monitor Module feature conn.
12	1	AMP 787745-2	Dual USB connector (Not stuffed as of 7/96)
13	1	Fox Conn SKTC-0704-95 R7/95	25-pin Parallel port connector
14	1	AMP 787650-4	9-pin Serial port D-sub connector
15	1	Fox Conn MH11063-D0	Keyboard and mouse conn.
16	1	Fox Conn DZ11A39-R9	15-pin VGA connector
17	1	AMP 555153-1	RJ45 Network connector
18	1	Fox Conn HZ-50060-E3	6-pin 3.3V PCI power conn.
19	4	AMP640456-3	3-pin System/CPU Fan Conn.
20	1	Amp 11959-2	Auxiliary Power Connector onboard
21	1	Amp 102387-2	Auxiliary Power Connector from supply

Table 8-26 Baseboard Module Jumpers

Jumper - Name	Pins (default in bold)	Description
J43G - Chassis Intrusion Detection	1-2 Enable	Activates alarm switches used to detect removal of chassis covers.
	2-3 Disable	Bypasses the chassis intrusion switch
J43F - Boot Option	1-2 Normal Boot	Inverts address A16 so that the normal BIOS does not reside at the top of flash memory where the write-protected Recovery BIOS region is located
	2-3 Recovery Boot	Prevents inverting A16. Allows system to boot from the Recovery BIOS when the normal BIOS gets corrupted—if you are unable to reload a fresh copy from floppy diskette
J43E - Flash	1-2 Erase/Program	Applies +12V power to the VPP pin on the Flash memory device, and enables erasing or programming of Flash memory.
	2-3 Protect	Protects the contents of Flash memory
J43D - Boot Block	1-2 Protect	Prevents writing to the BIOS boot block
	2-3 Erase/Program	Permits boot block erasing and programming
		CAUTION Programming the boot block incorrectly will prevent the system from booting.

continued

Jumper - Name	Pins (default in bold)	Description
J43C - FRB (Fault Resilient Boot Timer)	1-2 Enable 2-3 Disable	Allows the system to boot from processor 1 if processor 0 fails. Lets the system boot from only processor 0.
J43B - Password	1-2 Protect 2-3 Erase	Maintains the current system password. Clears the password.
J43A - CMOS Clear	1-2 Protect 2-3 Erase	Preserves the contents of NVRAM. Replaces the contents of NVRAM with the manufacturing default settings.

Table 8-27 Processor/Memory Module Jumpers

Processor/ Bus Speed	J14A CLKSEL 1	J14B CLKSEL 0	J15A CLKDEV 2	J15B CLKDEV 1	J16A CLKDIV 0
150/60	1-2	2-3	2-3	1-2	1-2
166/66	2-3	1-2	2-3	1-2	1-2
180/60	1-2	2-3	1-2	2-3	1-2
200/66	2-3	1-2	1-2	2-3	1-2

9. APPENDIX A - PRODUCT CODES

9.1 Boards

Table 9-1 Board Product Codes

Product Code	Description
Baseboard Only	
BBUC04A	B440FX baseboard with NIC and SCSI, Production
Processor Modules	
MBUCCPU10A	1 X 200/512, 32 MB memory, Production
MBUCCPU12A	1 X 166/512, 32 MB memory, Production
MBUCCPU13A	No CPU, 0 MB memory, Production
MBUCCPU16A	1x200/256, 32 MB memory, Production
MBUCCPU20A	2x200/256, 0 MB memory, 12V VRM, Production
MBUCCPU21A	1x200/256, 0 MB memory, Production
MBUCCPUD25A	2x200/512, 32MB memory, 12V VRM, Production
B440FX Accessories	
ABUC2NDCPUA	Second processor upgrade kit includes instructions, heat sink, VRM, clips, grease, NO processor

9.2 System

Table 9-2 System Product Codes

Balboa	
SBALBUCSTD15A	1x power supply, single disk array support, non-redundant cooling (3 fans not including power supply fans), Baseboard
SBALBUCSTD24A	2x power supply, single disk array support, redundant cooling (5 fans not including power supply fans), Baseboard
Balboa Accessories	
ABALBUCRCOOLA	Redundant fan kit for Balboa includes 2x fans, housing, 2x adapters, instructions
ABALBUCRPWRA	Redundant power supply upgrade kit for Balboa includes power share board, cover, cables, manual, (US) AC cord, AC warning label, NO power supply
ABALBUCPS1A	Balboa power supply includes 1x 330 W power supply and instructions. ABALBUCRPWRA must be purchased separately to add as additional supply
ABALBUC2NDHDA	Second hard drive array for Balboa includes 5x drive trays, EMI clips, wide SCSI cable, instructions, SCSI backplane

9.2.1 Packing lists (Balboa Systems)

SBALBUCSTD24A - Basic Redundant

Main Components:

	Notes
Balboa Chassis	
B440FX Baseboard	
Front Panel Board	
Hot Swap SCSI Back Plane	1
Power Share Board	
Cooling Fans	5
330W Power Supply	2
Country Kit on CD-ROM	(October ’96 revision includes SCU & NIC Floppies)
LANDesk Server Manager v2.52	CD-ROM

Peripheral Components:

	Notes
3-1/2” Floppy Drive	
CD-ROM Drive (4X SCSI)	
Plastic Hard Drive Carrier Trays	5-1” HDD supported per backplane

Cable Assemblies:

	Notes
Main Power Harness	
Auxiliary Power Harness	
Peripheral Power Harness	
Floppy Cable	
Wide SCSI cable	
Front Panel Board Cable	
Hot Swap Management Cable	
Chassis Intrusion Switch	2
Hot Swap Intrusion Switch	

Miscellaneous:

	Notes
5.25” Drive Bay Rails	4
SCSI Converter	2 - Wide Cable to Narrow Device, One used by CD-ROM
Power Cord	2

Paper Documentation:

	Notes
Quick Start Guide	
Management S/W Installation Guide	
Intel End User Software License Agreement	

SBALBUCSTD15A - Basic Redundant

Main Components:

	Notes
Balboa Chassis	
B440FX Baseboard	
Front Panel Board	
Hot Swap SCSI Back Plane	1
Cooling Fans	3
330W Power Supply	
Country Kit on CD-ROM	(October '96 revision includes SCU & NIC Floppies)
LANDesk Server Manager v2.52	CD-ROM

Peripheral Components:

	Notes
3-1/2" Floppy Drive	
CD-ROM Drive (4X SCSI)	
Plastic Hard Drive Carrier Trays	5-1" HDD supported per backplane

Cable Assemblies:

	Notes
Main / Peripheral Power Harness	
Floppy Cable	
Wide SCSI cable	
Front Panel Board Cable	
Hot Swap Management Cable	
Chassis Intrusion Switch	2
Hot Swap Intrusion Switch	

Miscellaneous:

	Notes
5.25” Drive Bay Rails	4
SCSI Converter	2 - Wide Cable to Narrow Device, One used by CD-ROM
Power Cord	

Paper Documentation:

	Notes
Quick Start Guide	
Management S/W Installation Guide	
Intel End User Software License Agreement	

10. APPENDIX B - CUSTOMER SUPPORT

10.1 Faxback

- Product descriptions and technical data sent to any fax machine from a touch-tone phone
- Information on End-of-Life products
- Available worldwide through direct dial

U.S. 800-525-3019

Americas 916-356-3105

Europe 44-793-496646

10.2 Windows Help Files

- Monthly Product updates available to qualified users on the bulletin board
- Official notification of engineering changes and technical data
- Easy information retrieval using Windows Help file format
- Intel platform system, board, and BIOS revision histories
- Hardware and software compatibility notes
- Documentation updates, spare parts and order information
- Errata

10.3 Intel Application Support

Contact your local technical representative; the customer's primary asset is the local representative. For all technical issues, first contact your Field Application Engineer.

10.3.1 Hotline

1-800-628-8686

A direct link to highly qualified and well trained technical personnel.

- ♦ Toll-free access to Intel support engineers for problem resolution
- ♦ Responses within 24 hours Monday-Friday
- ♦ Expert assistance geared to the special needs of OEMs and VARs

10.3.2 BBS

A full service bulletin board with product information and more.

- **Americas 503-264-7999**
- **Europe 44-793-496340**
- FLASH BIOS upgrade files
- Modem set at no parity, 8 data bits, 1 stop bit.
- Master BBS file list and FaxBack catalog available at 800-897-2536.

10.3.3 Internet

A full service World Wide Web location with product information and more.

Available worldwide through:

http://www.intel.com/TBD

ftp.intel.com/TBD

- FLASH BIOS upgrade files
- Configuration Utility (SCU) upgrade files