OC440LX Motherboard

Technical Product Specification

August 1998

Order Number 702586-001

The OC440LX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the OC440LX Motherboard Specification Update.

Revision History

Revision	Revision History	Date
-001	First review draft of the OC440LX Motherboard Technical Product Specification	August 1998

This product specification applies only to standard OC440LX motherboards with BIOS identifier 4O4CL0X0.15A**.**

Changes to this specification will be published in the OC440LX Motherboard Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the OC440LX motherboard. It describes the standard motherboard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the motherboard and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically not intended for general audiences.

What this Document Contains

Chapter	Description
1	A description of the hardware used on this board
2	A map of the resources of the board
3	Features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes
6	A listing of where to find information about specifications supported by the motherboard

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

A note calls attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions which, if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn is the relative coordinates of its location on the motherboard, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. There is only one such connector at that location.
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
GB	Gigabyte (1,073,741,824 bytes)
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.

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1 Motherboard Description

1.1 Overview

The OC440LX motherboard has the following features:

microATX form factor of 8.8 x 9.6 inches

Microprocessor:

- Support for a single Pentium® II or Intel® Celeron™ processor
- 66 MHz host bus speed
- Slot 1 connector

Main memory:

- Two 168-pin dual inline memory module (DIMM) sockets
- Supports up to 512 MB of synchronous DRAM (SDRAM)

Intel® 82440LX AGPset and PCI/IDE Interface:

- Intel® 82443LX PCI/AGP controller (PAC)
  - Integrated PCI bus mastering controller
  - Integrated Accelerated Graphics Port (AGP) interface
- Intel® 82371EB PCI ISA IDE Xcelerator (PIIX4E)
  - Multifunction PCI-to-ISA bridge
  - Universal Serial Bus (USB) and DMA controllers
  - Two fast IDE interfaces that support up to four IDE drives or devices
  - Power management logic
  - Real-time clock

I/O features:

- SMC FDC37M707QFP I/O controller
- Two USB ports

Three expansion slots:

- Two PCI slots
- One shared (ISA/PCI) slot

AC ‘97 audio subsystem:

- Creative Labs ES1371 AC ‘97 V1.03 digital controller
- Crystal Semiconductor CS4297 AC ‘97 V1.03 analog codec

Graphics subsystem

- ATI Rage† Pro Turbo AGP 2X graphics controller
- 4 MB SGRAM (graphics memory)
- DDC2B Compliant

Other features:

- Intel/Phoenix BIOS (2 Mbit flash memory)
- Plug and Play compatible
- Single-jumper configuration
- Advanced Power Management (APM) 1.2 support
- Advanced Configuration and Power Interface (ACPI) 1.0 support
- Wake on Ring connector
- ATI Media Channel (AMC) connector

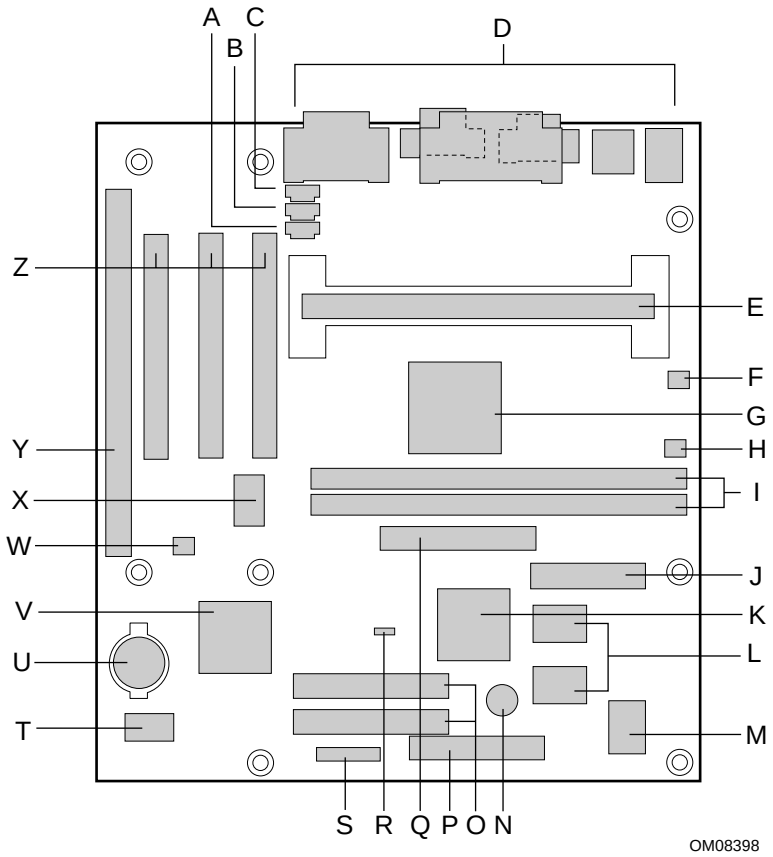
Software drivers and utilities are available from Intel.

1.2 Manufacturing Options

The following are manufacturing options. Not all manufacturing options are available in all marketing channels. Please contact your Intel representative to determine what manufacturing options are available to you.

- Wake on LAN† technology connector

1.3 Motherboard Components



A	ATAPI CD-ROM connector	N	Piezoelectric speaker
B	TV Audio Line In connector (ATAPI-style)	O	IDE connectors
C	Telephony connector (ATAPI-style)	P	Diskette drive connector
D	Back panel connectors	Q	ATI Media Channel (AMC) connector
E	Slot 1 connector	R	Configuration jumper block
F	Fan 2 connector (for a variable speed fan)	S	Front panel connector
G	Intel 82443LX PCI/AGP controller	T	Flash memory
H	Fan 3 connector (for an “always on” fan)	U	Battery
I	DIMM sockets	V	Intel 82371EB PCI ISA IDE Xcelerator (PIIX4E)
J	Power supply connector	W	Wake on Ring connector
K	ATI Rage Pro Turbo AGP 2X graphics controller	X	Creative Labs ES1371 AC ’97 digital controller
L	Graphics memory	Y	ISA slot
M	SMC FDC37M707QFP I/O controller	Z	PCI slots

Figure 1. Motherboard Components

1.4 Microprocessor

The motherboard supports a single Pentium II or Celeron processor with a 66 MHz host bus. The processor's VID pins automatically program the voltage regulator on the motherboard to the required processor voltage. The processor connects to the motherboard through the Slot 1 connector, a 242-pin edge connector. The processor must be secured by a retention mechanism attached to the motherboard.

NOTE

Information regarding the specific retention mechanism for the processor to be installed in the computer is available from Intel.

The motherboard supports the following processor configurations:

Processor Type	Processor Speed	Cache Size	Package Type
Pentium II	333 MHz 300 MHz 266 MHz 233 MHz	512 KB 512 KB 512 KB 512 KB	S.E.C. cartridge
Celeron	333 MHz 300A MHz 300 MHz 266 MHz	128 KB 128 KB None None	S.E.P. package

1.4.1 Second Level Cache

The second level cache for the Pentium II processor is located on the substrate of the S.E.C. cartridge. The cache includes 512 KB of synchronous pipelined burst static RAM (PBSRAM) and tag RAM. All supported onboard memory can be cached.

The Celeron 300A and 333 MHz processors include an integrated 128 KB second level cache subsystem, implemented on the processor die. All supported onboard memory can be cached.

The Celeron processors operating at 266 and 300 MHz do not have second level cache.

1.4.2 Microprocessor Upgrades

The motherboard can be upgraded with processors that run at higher speeds. When upgrading the processor, use the configure mode to change the processor speed (see Section 1.13).

1.5 Main Memory

The motherboard has two DIMM sockets. SDRAM can be installed in one or both sockets. The motherboard supports only DIMMs with serial presence detect (SPD) data structures.

Using the SPD data structure, programmed into an E^2PROM on the DIMM, the BIOS can determine the SDRAM's size and speed. Minimum memory size is 16 MB; maximum memory size is 512 MB. Memory size can vary between sockets.

The motherboard supports the following memory features:

- 168-pin DIMMs with gold-plated contacts
- 66 MHz, 4 Clock SDRAM
- 64-bit memory (non-error checking and correcting)
- 3.3 V memory only
- Unbuffered single- or double-sided DIMMs in the following sizes:

DIMM Size	Configuration
16 MB	2 Mbit x 64
32 MB	4 Mbit x 64
64 MB	8 Mbit x 64
128 MB	16 Mbit x 64
256 MB	32 Mbit x 64

NOTE

All memory components and DIMMs used with the OC440LX motherboard must comply with the PC SDRAM specifications. These include the PC SDRAM Specification (memory component specific) and the PC Unbuffered DIMM Specification. When using a DIMM with the SPD data structure, the DIMM must comply with the PC Serial Presence Detect Specification. You can access these documents through the Internet at:
http://www.intel.com/design/pcisets/memory/

See Section 6.2 for information about these specifications.

1.6 Chipset

The Intel® 440LX AGPset includes a Host-PCI bridge integrated with both an optimized DRAM controller and an AGP interface. The I/O subsystem of the 440LX is based on the PIIX4E, which is a highly integrated PCI-ISA/IDE Accelerator Bridge. This chipset consists of the Intel 82443LX PAC and the Intel 82371EB PIIX4E bridge chip.

1.6.1 Intel® 82443LX PAC

The Intel 82443LX PAC provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, PCI bus, the AGP, and main memory. The PAC features:

- Processor interface control
  - — Processor host bus speed up to 66 MHz
  - — 32-bit addressing
  - — GTL+ compliant host bus
- Integrated DRAM controller
  - — Support for synchronous DRAM (SDRAM)
  - — 64-bit path-to-memory
  - — Auto detection of memory type
  - — Support for 4-, 16-, 64-Mbit DRAM devices
  - — Symmetrical and asymmetrical DRAM addressing
  - — Support for 3.3 V DRAMs
- Accelerated Graphics Port Interface
  - — Compliance with A.G.P. specification (see Section 6.2 for specification information)
  - — Support for 3.3 V A.G.P. devices with data transfer rates up to 133 MHz
  - — Synchronous coupling to the host-bus frequency
- Fully-synchronous PCI bus interface
  - — Compliance with PCI specification (see Section 6.2 for specification information)
  - — PCI-to-DRAM access greater than 100 MB/sec
  - — Support for five PCI bus masters in addition to the host and PCI-to-ISA I/O bridge
  - — Delayed transactions
  - — PCI parity checking and generation support
- Data Buffering
  - — Host-to-DRAM, PCI-to-DRAM, and A.G.P.-to-DRAM write-data buffering
  - — Write-combining for host-to-PCI burst writes
  - — Supports concurrent host, PCI, and A.G.P. transactions to main memory
- Support for system management mode (SMM)

1.6.2 Intel® 82371EB PIIX4E

The Intel 82371EB PIIX4E is a multifunction PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, USB host/hub functionality, and enhanced power management. The PIIX4E features:

- Multifunction PCI-to-ISA bridge
  - Support for the PCI bus at 33 MHz
  - Complies with the PCI specification (see Section 6.2 for specification information)
  - ISA bus support
- USB controller
  - Two USB ports (see Section 6.2 for specification information)
  - Support for legacy keyboard and mouse
  - Support for UHCI interface
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 16 MB/sec
  - Support for Ultra DMA/33 synchronous DMA mode transfers at up to 33 MB/sec
  - Bus master mode with an 8 x 32-bit buffer for bus master PCI IDE burst transfers
- Enhanced DMA controller
  - Two 8237-based DMA controllers
  - Support for PCI DMA with three PC/PCI channels and distributed DMA protocols
- Interrupt controller based on 82C59
  - Support for 15 interrupts
  - Programmable for edge/level sensitivity
- Power management logic
  - Sleep/resume logic
  - Support for Wake on Ring, Wake on LAN technology, and Wake on PCI power management enabled (PME)
  - Support for ACPI (see Section 6.2 for specification information)
- Real-Time Clock
  - 256-byte battery-backed CMOS SRAM
  - Includes date alarm
- 16-bit counters/timers based on 82C54

1.6.3 USB

The motherboard has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The motherboard fully supports the universal host controller interface (UHCI) and uses UHCI-compatible software drivers. See Section 6.2 for information about the USB specification. USB features include:

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

1.6.4 IDE Support

The motherboard has two independent bus-mastering PCI IDE interfaces. These interfaces support:

- ATAPI devices (such as CD-ROM drives)
- ATA devices using these transfer modes
  - PIO Mode 3
  - PIO Mode 4
  - Ultra DMA/33 synchronous-DMA mode

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The BIOS automatically detects the IDE device transfer rate and translation mode.

The motherboard also supports laser servo (LS-120) drives. LS-120 technology allows the user to perform read/write operations to LS-120 (120 MB) and conventional 1.44 MB and 720 KB diskettes. An optical servo system is used to precisely position a dual-gap head to access the diskette's 2,490 tracks per inch (tpi) containing up to 120 MB of data storage. A conventional diskette uses 135 tpi for 1.44 MB of data storage.

LS-120 drives are ATAPI-compatible and connect to the motherboard's IDE interface. (LS-120 drives are also available with SCSI and parallel port interfaces.) Some versions of Windows† 95, Windows 98, and Windows NT† operating systems recognize the LS-120 drive as a bootable device in both 120 MB and 1.44 MB mode.

Connection of an LS-120 drive and a standard 3.5-inch diskette drive is allowed. The LS-120 drive can be configured as a boot device if selected as Drive A in the BIOS setup program.

NOTE

If you connect an LS-120 drive to an IDE connector and configure it as the "boot" drive and configure a standard 3.5-inch diskette drive as a "B" drive, the standard diskette drive is not seen by the operating system. When the LS-120 drive is configured as the "boot" device, the system will recognize it as both the A and B drive.

1.6.5 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program.

NOTE

The recommended method of accessing the date in systems with Intel motherboards is indirectly from the Real Time Clock (RTC) via the BIOS. The BIOS on Intel motherboards and baseboards contains a century checking and maintenance feature that checks the least two significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

For more information on proper date access in systems with Intel motherboards please see http://support.intel.com/support/year2000/

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 V applied.

1.7 I/O Interface Controller

The motherboard uses the SMC FDC37M707QFP I/O controller which features:

- Single diskette drive interface
- ISA Plug-and-Play compatible register set
- One serial port
- FIFO support on both serial and floppy interfaces
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- PS/2† style mouse and keyboard interfaces
- Intelligent auto power management, including:
  - — Shadowed write-only registers for ACPI compliance
  - — Programmable wake-up event interface

The BIOS Setup program provides configuration options for the I/O controller.

1.7.1 Serial Port

The motherboard has one 9-pin D-Sub serial port connector located on the back panel. The serial port's NS16C550-compatible UARTs support data transfers at speeds up to 115.2 Kbits/sec with BIOS support. The serial port can be assigned as COM1 (3F8), COM2 (2F8), COM3 (3E8), or COM4 (2E8).

1.7.2 Parallel Port

The connector for the multimode bi-directional parallel port is a 25-pin D-Sub connector located on the back panel of the motherboard. In the Setup program, there are four options for parallel port operation:

- Compatible (standard mode)
- Bi-directional (PS/2 compatible)
- Bi-directional EPP. A driver from the peripheral manufacturer is required for operation. See Section 6.2 for EPP compatibility.
- Bi-directional high-speed ECP

1.7.3 Diskette Drive Controller

The I/O controller is software compatible with the 82077 diskette drive controller and supports a single diskette drive in both PC-AT† and PS/2 modes. In the Setup program, the diskette drive interface can be configured for the following diskette drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch (driver required)
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

1.7.4 PS/2 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel of the motherboard. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an over-current condition is removed.

NOTE

The mouse and keyboard can be plugged into either PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains code which provides the traditional keyboard and mouse control functions, and also supports Power On/Reset password protection. A Power On/Reset password can be specified in the BIOS Setup program.

1.8 Audio Subsystem

The OC440LX motherboard includes an Audio Codec ’97 (AC ’97) compatible audio subsystem, the features of which include:

- Split digital/analog architecture for improved S/N (signal-to-noise) ratio: ≥ 80 dB - measured at line out, from any analog input, including line in, CD-ROM, auxiliary line in, and video (stereo audio from a video source)
- Ensoniq 3D positional audio support
- Power management support for APM 1.2, ACPI 1.0, and PCI 2.1
- Audio inputs:
  - Two analog line-level stereo inputs for connection from line in and CD-ROM audio
  - One analog line-level input for telephony (speakerphone input)
  - One mono microphone input (Mic)
- Audio outputs:
  - Stereo line-level output
  - Mono output for speakerphone

The audio subsystem consists of these devices:

- Creative Labs ES1371 AC ’97 V1.03 digital controller
- Crystal Semiconductor CS4297 AC ’97 V1.03 analog codec

1.8.1 Creative Labs ES1371 AC ’97 V1.03 Digital Controller

- PCI 2.1 compliant
- PCI bus master for PCI audio
- 64 voice software wavetable
- Aureal A3D† API, Sound Blaster Pro†, Roland MPU 401 MIDI, joystick compatible
- Ensoniq 3D positional audio and Microsoft DirectSound† 3D support

1.8.2 Crystal Semiconductor CS4297 AC ’97 V1.03 Analog Codec

- 18 bit stereo full-duplex codec
- Fixed 48 kHz sampling rate

1.8.3 Audio Connectors

The audio connectors include the following:

- Back panel connectors: stereo line-level output (line out), stereo line-level input (line in), and Mic In
- ATAPI CD-ROM audio connector (black)
- Telephony connector (green)
- TV audio line in connector (natural / off-white)

See Section 1.12 for the location and pinouts of the audio connectors.

1.8.3.1 CD-ROM Audio Connector

A 1 x 4-pin ATAPI-style connector (J2C2) can be used to connect an internal CD-ROM drive to the audio mixer.

1.8.3.2 Telephony Connector

A 1 x 4-pin ATAPI-style connector (J1C1) connects the monaural audio signals of an internal telephony device to the audio subsystem. A monaural audio-in and audio-out signal interface is necessary for telephony applications such as speakerphones, faxmodems, and answering machines.

1.8.3.3 TV Audio Line In Connector

A 1 x 4-pin ATAPI-style line in connector (J2C1) connects the left and right channel signals of an internal audio device to the audio subsystem. An audio-in signal interface of this type is necessary for applications such as TV tuners.

1.8.4 Audio Drivers and Utilities

Audio software and utilities are available from Intel's World Wide Web site (see Section 6.1).

1.9 Graphics Subsystem

The graphics subsystem features the ATI Rage Pro Turbo AGP 2X. Graphics drivers are available from Intel's World Wide Web site (see Section 6.1).

1.9.1 Graphics Controller

The ATI Rage Pro Turbo 2X provides the following features:

- Support for AGP operating at 66 MHz (up to 533 MB/s throughput or data transfer rate)
- Multistream video for video conferencing
- Filtered scaling that enhances playback quality
- Enhanced line buffer allows vertical filtering of native MPEG-2 size (720 x 480) images
- DVD/MPEG-2 decode assist
- Filter circuitry that eliminates video artifacts caused by displaying interlaced video on noninterlaced displays
- Bi-directional bus mastering engine with planar YUV-to-packed format converter

- YUV to RGB color space converter with support for both packed and planar YUV:
  - YUV 4:2:2, YUV 4:1:0, and YUV 4:2:0
  - RGB 32, RGB 16/15, RGB 8, and monochrome
- Triple 8-bit palette DAC with gamma correction. Pixel rates up to 230 MHz
- Supports DDC1 and DDC2B+ for Plug and Play monitors
- 4 MB of 100 MHz SGRAM on the motherboard

Table 1 shows the relationship between video resolutions, color depth, and refresh rates.

Table 1. Video Resolutions, Color Depth, and Refresh Rate

	Maximum Refresh Rate (Hz) At:	
Resolution	**64K colors (4 MB local SGRAM)**	**16.7M colors (4 MB local SGRAM)**
640 x 480	200	200
800 x 600	200	150
1024 x 768	150	120
1152 x 864	120	85
1280 x 1024	100	85
1600 x 1200	85	

1.9.2 ATI Multimedia Channel (AMC) 2.0 Interface

The graphics subsystem includes a 40-pin AMC shrouded stake pin connector for interfacing add-in graphics/video cards with the AGP controller.

AMC 2.0 is a 16-bit bi-directional video port that enables direct connection to video upgrades such as:

- Video capture/video conferencing capability
- Hardware MPEG-2/DVD player
- TV tuner with Intercast† support
- An interface for the ATI ImpacTV chip

1.10 Wake on LAN Technology (Optional)

Wake on LAN technology enables remote wakeup of the computer through a network. Wake on LAN technology requires a PCI add-in network interface card (NIC) with remote wakeup capabilities. The remote wakeup connector on the NIC must be connected to the onboard Wake on LAN technology connector. The NIC monitors network traffic at the MII interface; upon detecting a Magic Packet†, the NIC asserts a wakeup signal that powers up the computer. To access this feature use the Wake on LAN technology connector, which is a 1 x 3-pin connector located at J4A1 on the motherboard. See Section 1.12 for the location and pinouts of the Wake on LAN technology connector.

⚠ CAUTION

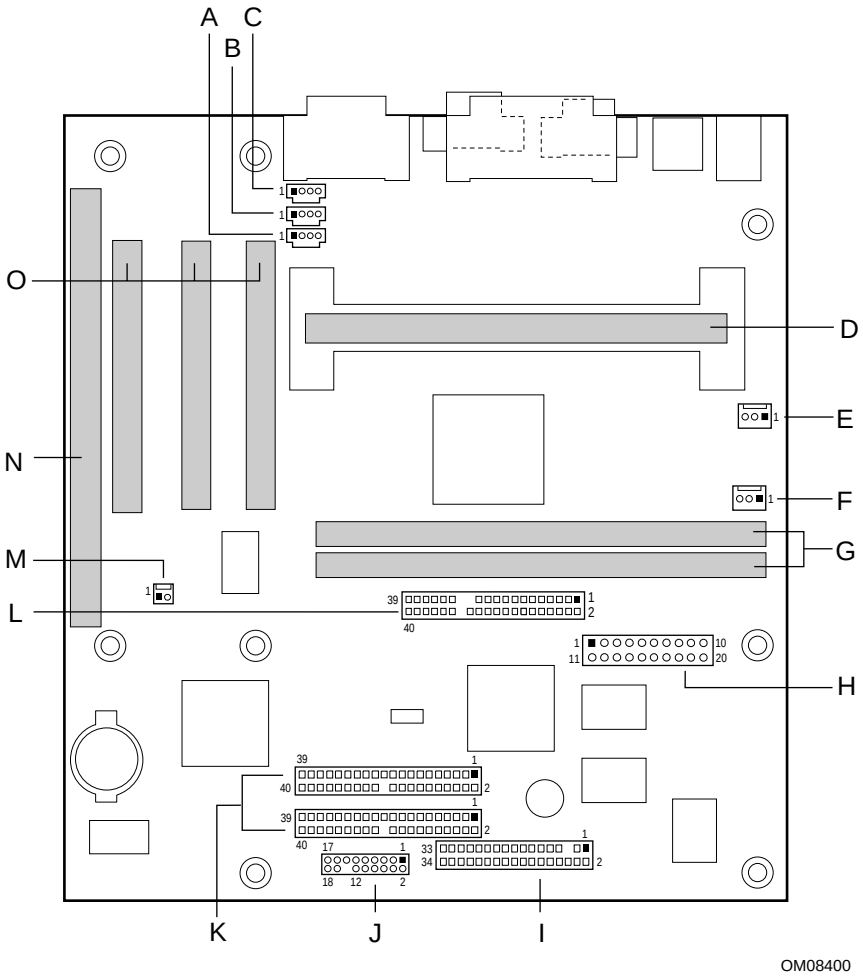
For Wake on LAN, the 5-V standby line for the power supply must be capable of delivering +5 V± 5 % at 720 mA. Failure to provide adequate standby current when implementing Wake on LAN, can damage the power supply.

1.11 Wake on Ring

Wake on Ring enables the computer to wake from sleep or soft-off mode when a call is received on a telephony device, such as a faxmodem, configured for operation on COM1. The first incoming call powers up the computer. A second call must be made to access the computer. To access this feature use the Wake on Ring connector, which is a 1 x 2-pin connector located at J3A2 on the motherboard. See Section 1.12 for the location and pinouts of the Wake on Ring connector.

1.12 Motherboard Connectors

Figure 2 shows the location of the motherboard connectors.



A	ATAPI CD-ROM (J2C2)	I	Diskette drive (J10F1)
B	TV Audio Line In (ATAPI-style) (J2C1)	J	Front panel (J10D1)
C	Telephony (ATAPI-style) (J1C1)	K	Primary and secondary IDE (J9D1, J9D2)
D	Slot 1 (J4F1)	L	AMC (J7F1)
E	Fan 2 (J4J1)	M	Wake on Ring (J3A2)
F	Fan 3 (J5J1)	N	ISA slot (J4A2)
G	DIMMs (J6F1, J6F2)	O	PCI slots (J4C1, J4B1, J4A3)
H	Power supply (J7H1)		

Figure 2. Motherboard Connectors

Table 2. ATAPI CD-ROM Connector (J2C2)

Pin	Signal Name
1	CD_IN-Left
2	Ground
3	Ground
4	CD_IN-Right

Table 3. TV Audio Line In Connector (ATAPI-style) (J2C1)

Pin	Signal Name
1	Left Line In
2	Ground
3	Ground
4	Right Line In (monaural)

Table 4. Telephony Connector (ATAPI-style) (J1C1)

Pin	Signal Name
1	Audio In (monaural)
2	Ground
3	Ground
4	Mic pre-amp out (to modem)

Table 5. Fan 2 Connector (J4J1)

Pin	Signal Name
1	Ground
2	FAN_CTRL (+12 V)
3	No connect

Table 6. Fan 3 Connector (J5J1)

Pin	Signal Name
1	Ground
2	+12 V
3	Ground

Table 7. Diskette Drive Connector (J10F1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	No Connect
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	No connect
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	No connect
17	No Connect	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	No Connect	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 8. PCI IDE Connectors (J9D1, J9D2)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Ground
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	Address 1	34	Reserved
35	Address 0	36	Address 2
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

NOTE: Signal names in brackets ([ ]) are for the secondary IDE connector.

Table 9. AMC Connector (J7F1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	VFC_D0
3	Ground	4	VFC_D1
5	Ground	6	VFC_D2
7	EVIDEO	8	VFC_D3
9	ESYNC	10	VFC_D4
11	EDCLK	12	VFC_D5
13	SDA	14	VFC_D6
15	Ground	16	VFC_D7
17	Ground	18	DCLK
19	Ground	20	BLANK #
21	VFCSNS #	22	HSYNC
23	SCL	24	VSYNC
25	Key	26	Ground
27	Key	28	Key
29	+5V	30	SAD3
31	RST #	32	SAD7
33	SAD6	34	SAD5
35	SAD4	36	AMCREV
37	Ground	38	+12V
39	N/C	40	N/C

Table 10. Wake on LAN Technology Connector (J4A1) (Optional)

Pin	Signal Name
1	+5 VSB
2	Ground
3	WOL

Table 11. Wake on Ring Connector (J3A2)

Pin	Signal Name
1	Ground
2	RINGA#

1.12.1 Power Supply Connector

When used with an ATX-compliant power supply that supports remote power on/off, the motherboard can turn off the system power through software control. See Section 6.2 for information about the ATX specification.

To enable soft-off control in software, advanced power management must be enabled in the Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

If power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

In addition, the motherboard supports the use of small form factor SFX power supplies. An SFX power supply uses the same connector as an ATX power supply, but does not provide -5 V to the motherboard. For more information about the SFX specification, see Section 6.2.

Table 12. Power Supply Connector (J7H1)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off control)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	-5 V
9	+5 VSB	19	+5 V
10	+12 V	20	+5 V

1.12.2 Front Panel Connectors

The front panel connectors includes connections for the following:

- Reset switch
- Power LED
- Hard drive activity LED
- Power switch
- Infrared module

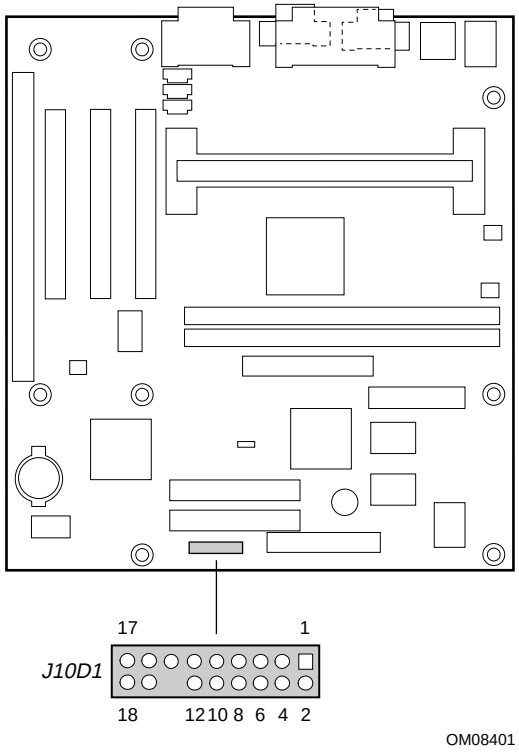


Figure 3. Front Panel I/O Connectors

Table 13 lists the signal name and corresponding description of the front panel connector pins.

Table 13. Front Panel I/O Connectors (J10D1)

Pin	Signal Name	In/Out	Description	Pin	Signal Name	In/Out	Description
1	HD_PWR	Out	Hard disk LED pullup (330 Ω) to +5 V	2	HDR_BLNK_ GRN	Out	Front panel green LED
3	HAD#	Out	Hard disk active LED	4	HDR_BLNK_ YEL	Out	Front panel yellow LED
5	GND		Ground	6	SW_ON#	In	Front panel On/Off button
7	FP_RESET#	In	Front panel Reset button	8	GND		Ground
9	+5 V	Out		10	FPSLP#	In	Front panel Sleep button
11	IRRX	In	IrDA† serial input	12	GND		Ground
13	GND		Ground	14	(pin removed)		Not connected
15	IRTX	Out	IRDA serial output	16	+5 V	Out	IR power
17	N/C		Not connected	18	N/C		Not connected

1.12.2.1 Hard Drive LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard hard drive controller.

1.12.2.2 Power LED Connector

Pins 2 and 4 can be connected to a dual colored LED that will light when the computer is powered on. Table 14 shows the possible states for this LED.

Table 14. Power LED

LED State	Description
Off	Off
Steady Green	Running
Blinking Green	Running or message waiting (Note)
Steady Yellow	Sleeping
Blinking Yellow	Sleeping or message waiting (Note)

Note: To utilize the message waiting function, an OnNow / Instantly Available aware message capturing software application must be invoked.

1.12.2.3 Power Switch Connector

Pins 6 and 8 can be connected to a front panel power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. At least two seconds must pass before the power supply will recognize another on/off signal. (The time requirements are due to internal debounce circuitry on the motherboard.)

1.12.2.4 Reset Switch Connector

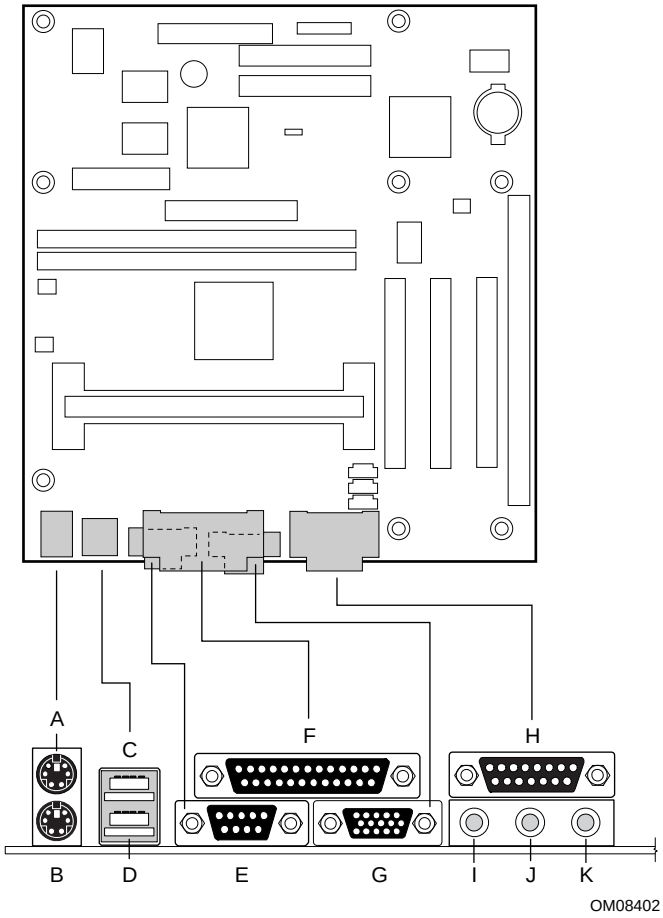
Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the motherboard resets and runs the POST.

1.12.2.5 Infrared Module Connector

Pins 11 - 16 can be connected to an IrDA module. After the IrDA interface is configured, files can be transferred to or from portable devices such as laptops, PDAs, and printers using application software.

1.12.3 Back Panel Connectors

Figure 4 shows the location of the back panel I/O connectors.



A	PS/2 keyboard or mouse	G	Video
B	PS/2 keyboard or mouse	H	MIDI/Game Port
C	USB Port 1	I	Audio Line Out
D	USB Port 0	J	Audio Line In
E	Serial Port	K	Audio Mic In
F	Parallel Port		

Figure 4. Back Panel I/O Connectors

Table 15. PS/2 Keyboard/Mouse Connectors

Pin	Signal Name
1	Data
2	No connect
3	Ground
4	+5 V (fused)
5	Clock
6	No connect

Table 16. Stacked USB Connectors

Pin	Signal Name
1	Power
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

Signal names in brackets ([ ]) are for USB Port 1.

Table 17. Serial Port Connector

Pin	Signal Name	Pin	Signal Name
1	DCD	6	DSR
2	Serial In #	7	RTS
3	Serial Out #	8	CTS
4	DTR#	9	RI
5	Ground		

Table 18. Video Connector

Pin	Signal Name
1	RED
2	GREEN
3	BLUE
4	No Connect
5	Ground
6	Ground
7	Ground
8	Ground
9	Fused VCC
10	Ground
11	No Connect
12	MONID1
13	HSYNC
14	VSYNC
15	MONID2

Table 19. Parallel Port Connector

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data bit 0	15	Fault#
3	Data bit 1	16	INIT#
4	Data bit 2	17	SLCT IN#
5	Data bit 3	18	Ground
6	Data bit 4	19	Ground
7	Data bit 5	20	Ground
8	Data bit 6	21	Ground
9	Data bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Error	25	Ground
13	Select		

Table 20. MIDI/Game Port Connector

Pin	Signal Name	Pin	Signal Name
1	+5 V (fused)	9	+5 V (fused)
2	GP4 (JSBUTO)	10	GP6 (JSBUT2)
3	GP0 (JSX1R)	11	GP2 (JSX2R)
4	Ground	12	MIDI-OUTR
5	Ground	13	GP3 (JSY2R)
6	GP1 (JSY1R)	14	GP7 (JSBUT3)
7	GP5 (JSBUT1)	15	MIDI-INR
8	+5 V (fused)		

Table 21. Audio Line Out Connector

Pin	Signal Name
Sleeve	Ground
Tip	Audio Left Out
Ring	Audio Right Out

Table 22. Audio Line In Connector

Pin	Signal Name
Sleeve	Ground
Tip	Audio Left In
Ring	Audio Right In

Table 23. Audio Mic In Connector

Pin	Signal Name
Sleeve	Ground
Tip	Mono In
Ring	Electret Bias Voltage

1.12.4 Add-in Board Expansion Connectors

There are three expansion slots on the motherboard: two PCI slots and one shared (ISA/PCI) slot. The PCI bus supports up to three additional bus masters through the three PCI connectors (see Section 6.2 for information about compliance with the PCI specification).

Table 24. PCI Bus Connectors

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	no connect (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	no connect (PRSNT1#)*	A40	+5 V (SDONE)*	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	+5 V (SBO#)*	B41	+3.3 V
A11	Reserved	B11	no connect (PRSNT2#)*	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

Table 25. ISA Bus Connector

Pin	Signal Name *	Pin	Signal Name *
B1	Ground	A1	IOCHK# (IOCHCK#)
B2	RESET (RESDRV)	A2	SD7
B3	+5 V	A3	SD6
B4	IRQ9	A4	SD5
B5	-5 V **	A5	SD4
B6	DRQ2	A6	SD3
B7	-12 V	A7	SD2
B8	SRDY# (NOWS#)	A8	SD1
B9	+12 V	A9	SD0
B10	Ground	A10	IOCHRDY (CHRDY)
B11	SMEMW# (SMWTC#)	A11	AEN
B12	SMEMR# (SMRDC#)	A12	SA19
B13	IOW# (IOWC#)	A13	SA18
B14	IOR# (IORC#)	A14	SA17
B15	DACK3#	A15	SA16
B16	DRQ3	A16	SA15
B17	DACK1#	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH#	A19	SA12
B20	BCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DACK2#	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	+5 V	A29	SA2
B30	OSC	A30	SA1
B31	Ground	A31	SA0
Key		Key	
D1	MEMCS16# (M16#)	C1	SBHE#
D2	IOCS16# (IO16#)	C2	LA23
D3	IRQ10	C3	LA22

continued

Table 25. ISA Bus Connector (continued)

Pin	Signal Name	Pin	Signal Name
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0#	C8	LA17
D9	DRQ0	C9	MEMR# (MRDC#)
D10	DACK5#	C10	MEMW# (MWTC#)
D11	DRQ5	C11	SD8
D12	DACK6#	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5 V	C16	SD13
D17	Master16# (MASTER#)	C17	SD14
D18	Ground	C18	SD15

* Items in parentheses are alternate versions of signal names.

** If an SFX power supply is installed in your computer, -5 V will not be present at pin B5 of the ISA bus connector.

1.13 Jumper Settings

The motherboard has a single jumper block at location J8E1. The 3-pin jumper block enables all motherboard configuration to be done in Setup. Figure 5 shows the location of the configuration jumper block. Table 26 describes the jumper settings for normal, configure, and recovery modes.

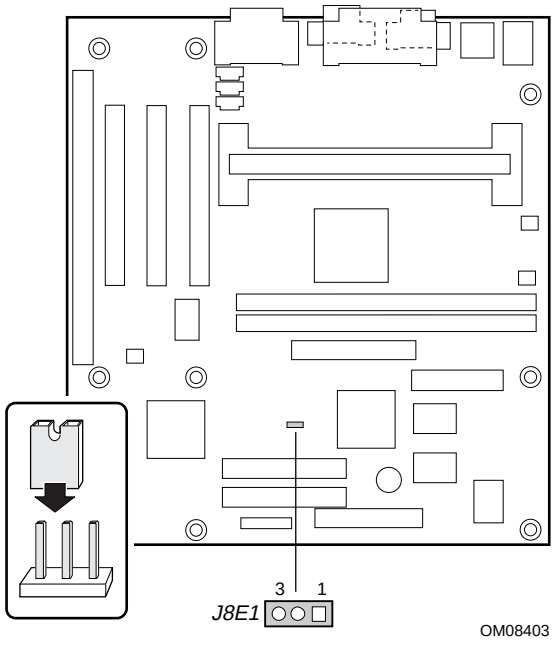


Figure 5. Location of the Configuration Jumper Block

Table 26. Configuration Jumper Settings

Function	Jumper J8E1	Configuration
Normal	1-2	The BIOS uses current configuration information and passwords for booting.
Configure	2-3	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	none	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

⚠ CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing the jumper.

1.14 Mechanical Considerations

1.14.1 Form Factor

The motherboard is designed to fit into a microATX form-factor chassis. The outer dimensions are 8.8 x 9.6 inches. (The maximum dimensions for a microATX form factor are 9.6 x 9.6 inches.) Figure **6** shows that the mechanical form factor, the I/O connector locations, and the mounting hole locations are in compliance with the microATX specification (see Section 6.2 for information about the microATX specification).

NOTE

One additional support point (mounting hole) is required in a standard ATX chassis for the OC440LX motherboard to be fully microATX compatible. See Section 6.2 for information about the microATX specification.

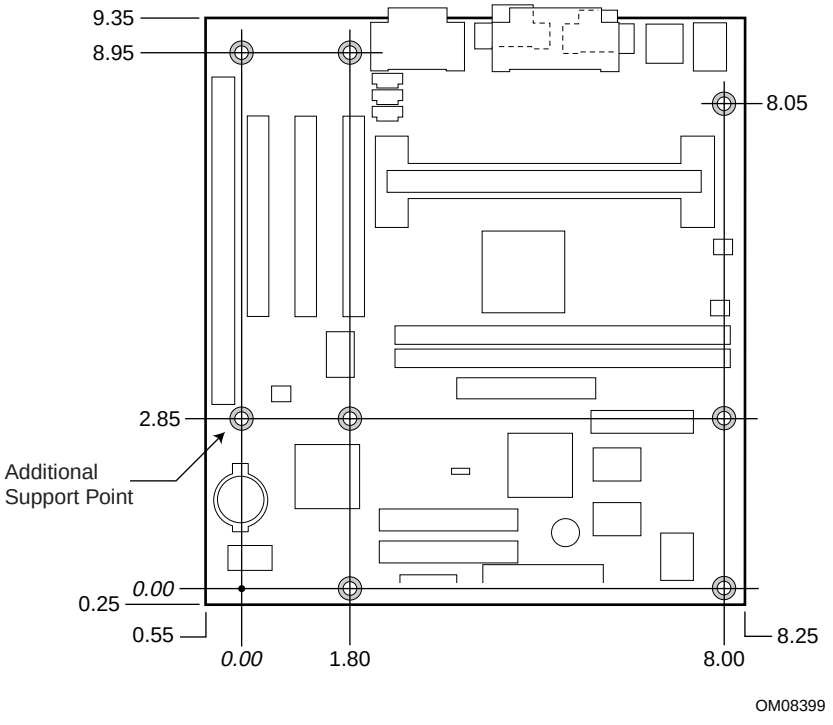


Figure 6. Motherboard Dimensions

1.14.2 I/O Shield

The back panel I/O shield for the motherboard must meet specific dimension and material requirements. Systems based on this motherboard need the back panel I/O shield to pass certification testing. Figure 7 shows the critical dimensions of the chassis-dependent I/O shield. Figure 8 shows the critical dimensions of the chassis-independent I/O shield. Both figures indicate the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the microATX specification. The dimensions of the back panel I/O shield for a microATX form factor are identical to the dimensions for an ATX form factor. See Section 6.2 for information about the microATX specification.

NOTE

An I/O shield specifically designed for the Intel® microATX chassis is available from Intel.

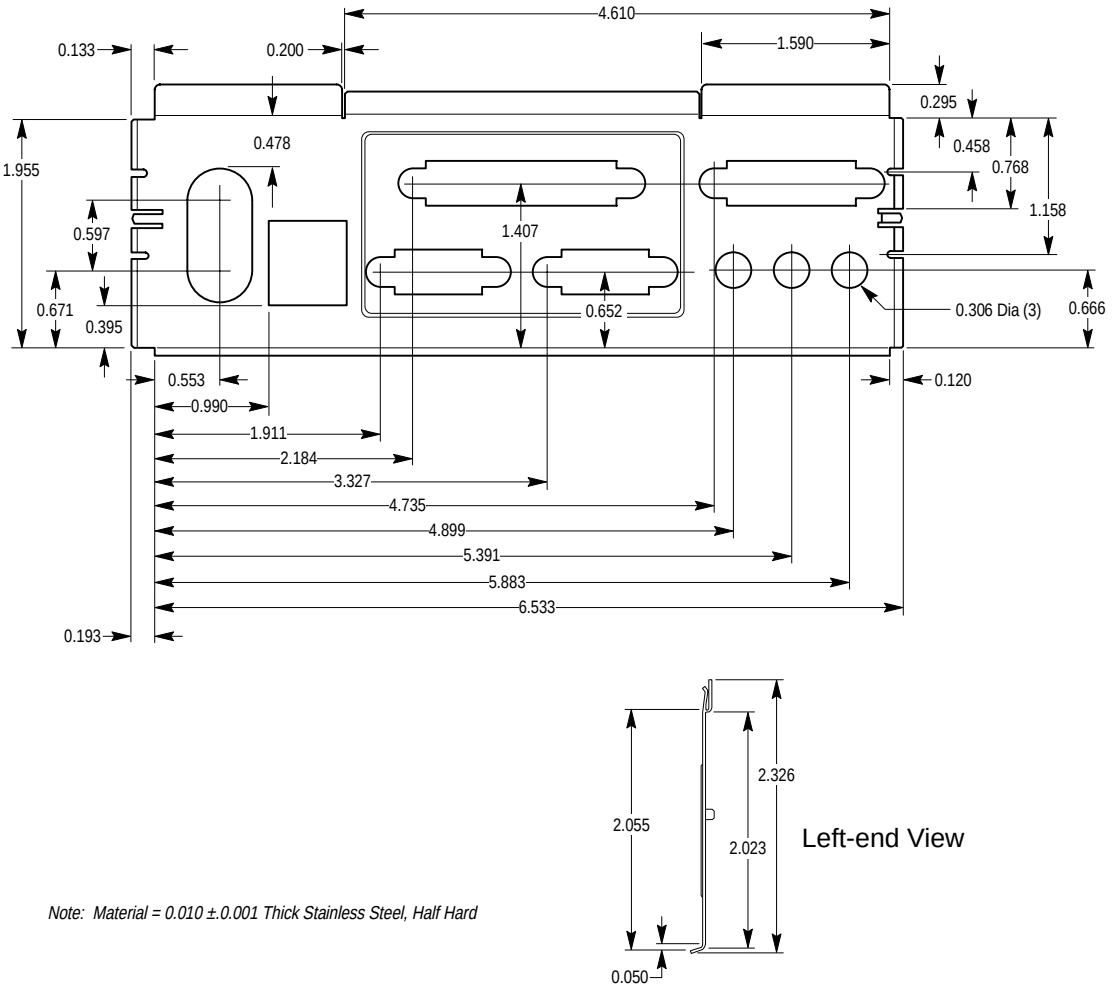


Figure 7. Back Panel I/O Shield Dimensions (microATX Chassis-Dependent)

NOTE

A chassis-independent I/O shield designed to be compliant with the microATX chassis specification 2.01 is available from Intel.

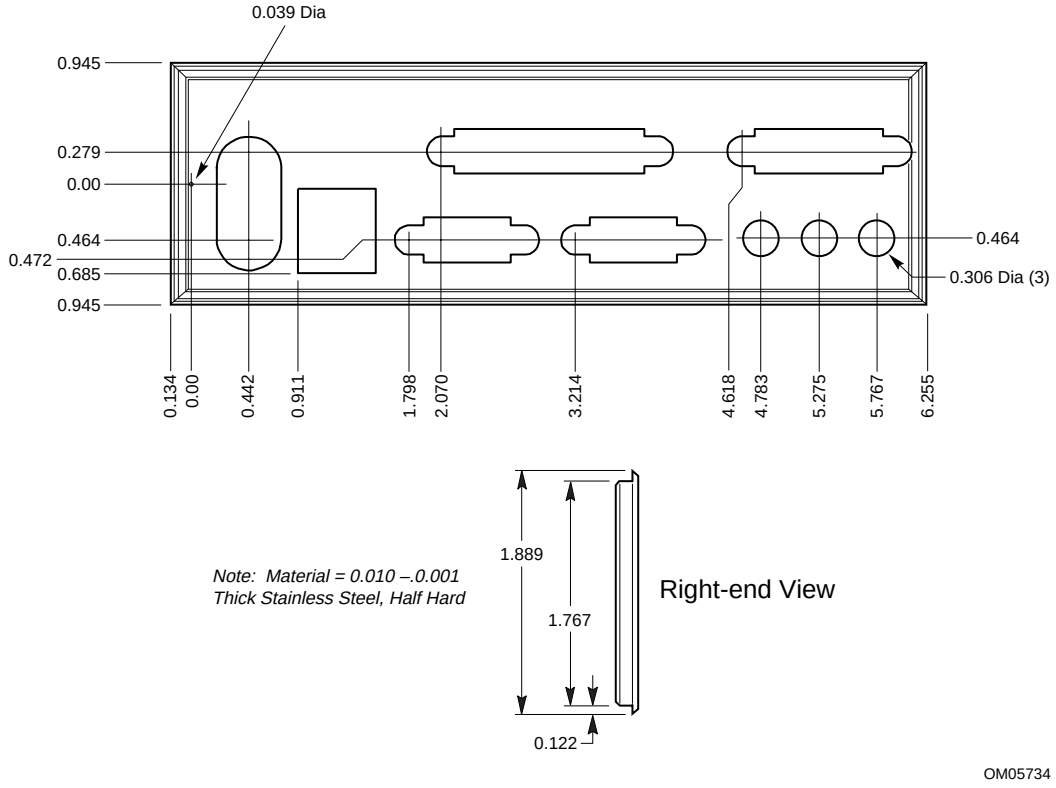


Figure 8. Back Panel I/O Shield Dimensions (microATX Chassis-Independent)

1.15 Electrical Considerations

1.15.1 Power Consumption

Table 27 lists the power usage for a computer that contains a motherboard with a 266 MHz Celeron processor, 32 MB SDRAM, 3.5-inch floppy drive, 2.5 GB IDE hard drive, 8X IDE CD-ROM, integrated Rage Pro Turbo 2X with 4 MB of video memory, and integrated Creative Labs ES1371 AC ’97 digital controller. This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 95 desktop mode were measured at 65K colors and 75 Hz refresh rate. AC watts are measured with a typical 200 W supply, nominal input voltage and frequency, with true RMS wattmeter at the line input.

Table 27. Power Usage

Mode	AC (watts) Out of 110 VAC Wall Outlet
DOS prompt, APM disabled	37 W
Windows 95 desktop, APM disabled	39 W
Windows 95 desktop, APM enabled, in SMM	28 W

1.15.2 Power Supply Considerations

System integrators should refer to the power usage values listed in Table 27 when selecting a power supply for use with this motherboard. The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification (see Section 6.2).

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

1.15.3 SFX Power Supply Support

The motherboard supports the use of small form factor SFX power supplies. An SFX power supply uses the same connector as an ATX power supply, but does not provide -5 V to the motherboard. For more information about the SFX specification, see Section 6.2.

1.16 Thermal Considerations

Table 28 lists maximum component case temperatures for motherboard components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the motherboard.

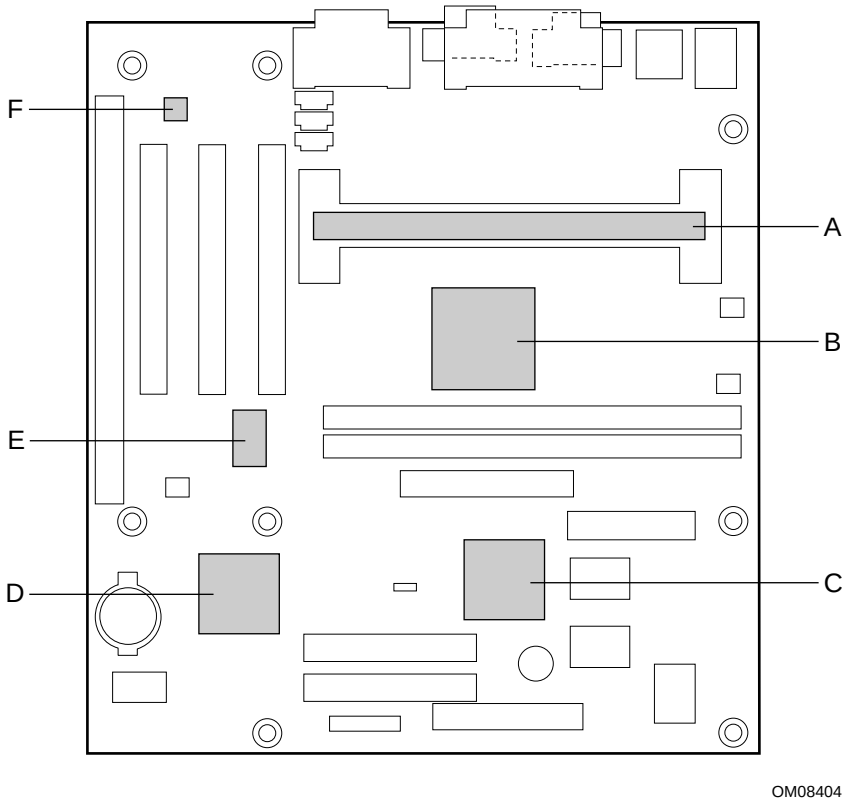
⚠ CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 °C to 10 °C might cause components to exceed their maximum case temperature. For information about the maximum operating temperature, see the environmental specifications in Section 1.18.

Table 28. Thermal Considerations for Components

Component	Maximum Case Temperature		Motherboard Location
Pentium II processor	233 MHz 266 MHz 300 MHz 333 MHz	75 °C (thermal plate) 75 °C (thermal plate) 72 °C (thermal plate) 65 °C (thermal plate)	J4F1 (Slot 1 connector)
Celeron processor	266 MHz	85 °C	J4F1 (Slot 1 connector)
Intel 82443LX (PAC)	85 °C		U5F1
ATI Rage Pro Turbo 2X	80 °C		U8F1
Intel 82371EB (PIIX4E)	85 °C		U8B4
Crystal Semiconductor CS4297 AC '97	85 °C		U2A1

Figure 9 shows motherboard components that may be sensitive to thermal changes.



A Processor (in Slot 1 connector)
B Intel 82443LX (PAC)
C ATI Rage Pro Turbo 2X
D Intel 82371EB (PIIX4E)
E Creative Labs ES1371 AC ’97
F Crystal Semiconductor CS4297 AC ’97

Figure 9. Thermally-Sensitive Components

1.17 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is for estimating repair rates and spare parts requirements.

MTBF data is calculated from predicted data @ 55 °C.

The MTBF prediction for the motherboard is 163,242 hours.

1.18 Environmental Specifications

Table 29. Environmental Specifications

Parameter	Specification		
Temperature			
Nonoperating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 G trapezoidal waveform		
	Velocity change of 170 inches/sec		
Packaged	Half sine 2 millisecond		
	Product Weight (lbs)	**Free Fall (inches)**	**Velocity Change (inches/sec)**
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz : 0.02g² Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015g² Hz (flat)		
	40 Hz to 500 Hz : 0.015g² Hz sloping down to 0.00015 g² Hz		
Humidity			
Nonoperating	noncondensing		
Operating	95% relative humidity at 30 °C, noncondensing		

1.19 Regulatory Compliance

This motherboard complies with the following safety and EMC regulations when correctly installed in a compatible host system.

Table 30. Safety Regulations

Regulation	Title
UL 1950 - CSA 950-95, 3rd edition, Dated 07-28-95	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60 950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60 950. (Norway, Sweden, Denmark, and Finland)

Table 31. EMC Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22, 2nd Edition, 1993	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
EN 55 022, 1994	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN 50 082-1 (1992)	Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)
VCCI Class B (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
ICES-003, Issue 2	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

1.19.1 Product Certification Markings

This motherboard has the following product certification markings:

- European CE Marking: Consists of a marking on the board and shipping container.
- UL Recognition Mark: Consists of a stylized backward UR on component side of the board, the UL File No. E139761 on the component side of the board, and the PB No. on the solder side of the board. Board material flammability is 94V-0.
- Canadian Compliance: Consists of small c followed by a stylized backward UR on component side of the board.

2 Resource Mapping

2.1 Memory Map

Table 32. Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 524288 K	100000 - 20000000	511 MB	Extended memory
928 K - 1024 K	E8000 - FFFFF	96 KB	System BIOS
896 K - 928 K	E0000 - E7FFF	32 KB	System BIOS (Available as UMB)
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to ISA and PCI buses)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
0 K - 640 K	00000 - 9FFFF	640 KB	Conventional memory

2.2 DMA Channels

Table 33. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Audio
1	8- or 16-bits	Audio/parallel port
2	8- or 16-bits	Diskette drive
3	8- or 16-bits	Parallel port (for ECP)/audio
4		Reserved - cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.3 I/O Map

Table 34. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA controller 1
0020 - 0021	2 bytes	Interrupt controller 1
002E - 002F	2 bytes	Super I/O controller configuration registers
0040 - 0043	4 bytes	Counter/Timer 1
0048 - 004B	4 bytes	Counter/Timer 2
0060	1 byte	Keyboard controller
0061	1 byte	NMI, speaker control
0064	1 byte	Keyboard controller
0070 - 0071	2 bytes	Real time clock controller
0080 - 008F	16 bytes	DMA page registers
00A0 - 00A1	2 bytes	Interrupt controller 2
00B2 - 00B3	2 bytes	APM control
00C0 - 00DE	31 bytes	DMA controller 2
00F0 - 00FF	16 bytes	Numeric processor
0170 - 0177	8 bytes	Secondary IDE controller
01F0 - 01F7	8 bytes	Primary IDE controller
0200 - 0207	8 bytes	Audio / game port / joy stick
0220 - 022F	16 bytes	Audio (Sound Blaster† compatible)
0228 - 022F	8 bytes	LPT3
0278 - 027F	8 bytes	LPT2
02E8 - 02EF	8 bytes	COM4/Video (8514A)
02F8 - 02FF	8 bytes	COM2
0330 - 0331	2 bytes	MPU-401 (MIDI)
0376 - 0377	2 bytes	Secondary IDE controller
0120 - 0127	8 bytes	Audio controller
0274 - 0277	4 bytes	I/O read data port for ISA Plug and Play enumerator
0378 - 037F	8 bytes	LPT1
0388- 038D	6 bytes	AdLib† (FM synthesizer)
03B0 - 03BB	12 bytes	Video (monochrome)
03C0 - 03DF	32 bytes	Video (VGA†)
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5, 03F7	7 bytes	Diskette controller
03F6	1 byte	Primary IDE controller
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0530 - 0537	8 bytes	Windows Sound System
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + 400h
0CF8 - 0CFF*	8 bytes	PCI configuration registers
0CF9**	1 byte	Turbo and reset control register

* DWORD access only

** Byte access only

2.4 PCI Configuration Space Map

Table 35. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82443LX (PAC)
00	01	00	Intel 82443LX (PAC) AGP bus
00	07	00	Intel 82371EB (PIIX4E) PCI/ISA bridge
00	07	01	Intel 82371EB (PIIX4E) IDE bus master
00	07	02	Intel 82371EB (PIIX4E) USB
00	07	03	Intel 82371EB (PIIX4E) power management
00	0B	00	PCI audio controller
00	0D	00	PCI expansion slot 1 (J4C1)
00	0E	00	PCI expansion slot 2 (J4B1)
TBD	TBD	TBD	PCI expansion slot 3 (J4A3)

2.5 Interrupts

Table 36. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard controller
2	Reserved, cascade interrupt from slave PIC
3	COM2*
4	COM1*
5	LPT2 (Plug and Play option)/audio/user available
6	Diskette drive controller
7	LPT1*
8	Real time clock
9	Reserved
10	USB/user available
11	Windows Sound System* / user available
12	PS/2 mouse port (if present, else user available)
13	Reserved, numeric processor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

2.6 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI expansion slots and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in board.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in boards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in boards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in boards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4E PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in board) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt. Table 37 lists the PIRQ signals and shows how the signals are connected to the onboard PCI interrupt sources.

Table 37. PCI Interrupt Routing Map

PIIX4E PIRQ Signal	First PCI Expansion Slot: J4C1	Second PCI Expansion Slot: J4B1	Third PCI Expansion Slot: J4A3	AGP Video	PCI Audio	USB	Power Management
PIRQA	INTA	INTB	INTC			INTA	INTA
PIRQB	INTB	INTC	INTD				
PIRQC	INTC	INTD	INTA		INTC		
PIRQD	INTD	INTA	INTB	INTD			

For example, assume an add-in board has one interrupt (group INTA) and is plugged into the second PCI slot. In this slot, an interrupt source from group INTA connects to the PIRQB signal. This add-in board will not share an interrupt.

Now, however, plug an add-in board that has one interrupt (group INTA) into the first PCI slot. Plug a second add-in board that has two interrupts (groups INTA and INTB) into the second PCI slot. INTA in the first slot is connected to signal PIRQA. INTA in the second slot is connected to signal PIRQB, and INTB is connected to signal PIRQC, which is already connected to the onboard audio. The second interrupt source on the add-in board in the second PCI slot will share an interrupt with the onboard audio.

NOTE

The PIIX4E can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 11, 14, 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

3 Overview of BIOS Features

3.1 Introduction

The motherboard uses an Intel/Phoenix BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the Setup program, POST, APM, the PCI auto-configuration utility, and Windows 95-ready Plug and Play. See Section 6.2 for the supported versions of these specifications.

This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as 4O4CL0X0.15A.

3.2 BIOS Flash Memory Organization

The Intel 28F002 2-Mbit flash component is organized as 256 KB x 8 bits and is divided into areas as described in Table 38. The table shows the addresses in the ROM image in normal mode (the addresses change in BIOS Recovery Mode).

Table 38. Flash Memory Organization

Address (Hex)	Size	Description
FFFFC000 - FFFFFFFF	16 KB	Boot Block
FFFFA000 - FFFFBFFF	8 KB	Vital Product Data (VPD) Extended System Configuration Data (ESCD) (DMI configuration data / Plug and Play data)
FFFF9000 - FFFF9FFF	4 KB	Used by BIOS (e.g., for Event Logging)
FFFF8000 - FFFF8FFF	4 KB	OEM logo or Scan Flash Area
FFFC0000 - FFFF7FFF	224 KB	Main BIOS Block

3.3 Resource Configuration

3.3.1 Plug and Play: PCI Autoconfiguration

The BIOS can automatically configure PCI devices and Plug and Play devices. PCI devices may be onboard or add-in cards. Plug and Play devices are ISA devices built to meet the Plug and Play specification. Autoconfiguration lets a user insert or remove PCI or Plug and Play cards without having to configure the system. When a user turns on the system after adding a PCI or Plug and Play card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is nondeterministic.

PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by this BIOS, see Section 6.2.

3.3.2 ISA Plug and Play

If Plug and Play operating system (see Section 4.3) is selected in Setup, the BIOS autoconfigures only ISA Plug and Play cards that are required for booting (IPL devices). If Plug and Play operating system is not selected in Setup, the BIOS autoconfigures all Plug and Play ISA cards. Since ISA legacy devices are not autoconfigurable, the resources for them must be reserved in BIOS Setup.

3.3.3 PCI IDE Support

If you select Auto in Setup, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to PIO Mode 4 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 6.2 for the supported version of ATAPI). Add-in ISA IDE controllers are not supported. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in Setup.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device.

3.4 Desktop Management Interface (DMI)

DMI is a method for managing computers in a managed network. See Section 6.2 for information about the latest DMI specification.

The main component of DMI is the management information format (MIF) database, which contains information about the computing system and its components. Using DMI, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use DMI. The BIOS stores and reports the following DMI information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Intel can provide system manufacturers with a utility that programs system and chassis-related information into the DMI space in flash memory. The utility is used to program the BIOS during system manufacturing, so that the BIOS can later report this information. Once written, this information cannot be overwritten.

DMI does not work directly under non-Plug and Play operating systems (such as Windows NT). However, the BIOS supports a DMI table interface for such operating systems. Using this support, a DMI service-level application running on a non-Plug and Play OS can access the DMI BIOS information.

3.5 Power Management

The BIOS supports both APM and ACPI. If the board is used with an ACPI-aware operating system, the BIOS provides ACPI support. Otherwise, it defaults to APM support.

3.5.1 Advanced Power Management (APM)

See Section 6.2 for the version of the APM specification that is supported. The energy saving standby mode can be initiated in the following ways:

- Time-out period specified in Setup
- Suspend/resume switch connected to the front panel sleep connector
- From the operating system, such as the Suspend menu item in Windows 95

In standby mode, the motherboard can reduce power consumption by spinning down hard drives, and reducing power to or turning off VESA† DPMS-compliant monitors. Power-management mode can be enabled or disabled in Setup (see Section 4.5).

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power-management features to work. For example, Windows 95 supports the power-management features upon detecting that APM is enabled in the BIOS.

3.5.2 Advanced Configuration and Power Interface (ACPI)

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. ACPI requires an ACPI-aware operating system. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM functionality normally contained in the BIOS
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the Power On Suspend sleeping state, and less than 5-watt system operation in the Suspend to Disk sleeping state
- A Soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 41)
- Support for a front panel power and sleep mode switch. Table 39 describes the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system

Table 39. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off	Less than four seconds	Power on
On	Less than four seconds	Soft off/Suspend
On	More than four seconds	Fail safe power off
Sleep	Less than four seconds	Wake up

3.5.2.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 40 lists the power states supported by the motherboard along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 40. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power *
G0 - working state	S0 - working	C0 - working	D0 - working state	Full power > 60 W
G1 - sleeping state	S1 - CPU stopped	C1 - stop grant	D1, D2, D3- device specification specific.	5 W < power < 30 W
G2/S5	S5 - Soft off. Context not saved. Cold boot is required.	No power	D3 - no power except for wake up logic.	Power < 5 W **
G3 - mechanical off. AC power is disconnected from the computer.	No power to the system.	No power	D3 - no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

* Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.

** Dependent on the standby power consumption of wake-up devices used in the system.

3.5.2.2 Wake Up Devices and Events

The table below describes which devices or specific events can wake the computer from specific states.

Table 41. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S5
LAN	S5
Modem	S5
USB	S1

3.5.2.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure motherboard devices that do not have other hardware standards for enumeration and configuration. PCI devices on the motherboard, for example, are not enumerated by ACPI.

3.6 BIOS Upgrades

A new version of the BIOS can be upgraded from a diskette using the Intel® Flash Memory Update utility that is available from Intel. This utility supports the following BIOS maintenance functions:

- Update the flash BIOS from a file on a diskette
- Change the language section of the BIOS
- Verify that the upgrade BIOS matches the target system to prevent accidentally installing an incompatible BIOS

BIOS upgrades and the Intel Flash Memory Update utility are available from Intel through the Intel World Wide Web site. See Section 6.1 for information about this site.

NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

3.6.1 Language Support

The Setup program and help messages can be supported in 32 languages. Five languages are available: American English, German, Italian, French, and Spanish. The default language is American English, which is present unless another language is programmed into the BIOS using the flash memory update utility. See Section 3.6 for information about the BIOS update utility.

The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

3.6.2 OEM Logo or Scan Area

A 4 KB flash-memory user area at memory location FFFF8000h-FFFF8FFFh is for displaying a custom OEM logo during POST. A utility is available from Intel to assist with installing a logo into the flash memory. Information about this capability is available on the Intel Support world wide web site. See Section 6.1 for more information about this site.

3.7 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode (see Section 1.13, beginning on page 39). When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the nonerasable boot block area, there is no video support. The procedure can only be monitored by listening to the speaker and looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.

- A single beep indicates the beginning of the BIOS recovery process.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Upgrade utility are available from the Intel Support world wide web site. See Section 6.1 for more information about this site.

NOTE

If the computer is configured to boot from an LS-120 diskette (see Section 4.6.2), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

3.8 Boot Options

In the Setup program, the user can choose to boot from a diskette drive, hard drive, CD-ROM, the network, or any BIOS boot specification (BBS) compliant device. The default setting is for the diskette drive to be the primary boot device and the hard drive to be the secondary boot device. By default the third and fourth devices are disabled.

3.8.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. See Section 6.2 for information about the El Torito specification. Under the Boot menu in the Setup program, CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device.

The network can be selected as a boot device. This selection allows booting from a network add-in card with a remote boot ROM installed.

3.8.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if no video adapter, keyboard, or mouse is attached. During POST, the board will beep three times to indicate that no video adapter was detected, but this is not a fatal error.

With regard to standard settings and custom default settings in the BIOS, if custom defaults have been set, the battery has failed, and AC power has failed, custom defaults will be loaded back into CMOS RAM at power on. If no custom defaults have been set, the standard defaults will be loaded back into CMOS RAM at power on.

3.9 USB Legacy Support

USB legacy support enables USB keyboards and mice to be used even when no operating system USB drivers are in place. By default, USB legacy support is disabled. USB legacy support is only intended to be used in accessing BIOS Setup and installing an operating system that supports USB.

This sequence describes how USB legacy support operates in the default (disabled) mode.

1. When you power up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is temporarily enabled by the BIOS. This allows you to use a USB keyboard to enter the Setup program or the maintenance mode.
4. POST completes and disables USB legacy support (unless it was set to Enabled while in Setup).
5. The operating system loads. While the operating system is loading, USB keyboards and mice are not recognized. After the operating system loads the USB drivers, the USB devices are recognized.

To install an operating system that supports USB, enable USB Legacy support in BIOS Setup and follow the operating system's installation instructions. Once the operating system is installed and the USB drivers configured, USB legacy support is no longer used. USB Legacy Support can be left enabled in BIOS Setup if needed.

Notes on using USB legacy support:

- If USB legacy support is enabled, don't mix USB and PS/2 keyboards and mice. For example, do not use a PS/2 keyboard with a USB mouse, or a USB keyboard and a PS/2 mouse.
- Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non-USB aware operating system.
- USB legacy support is for keyboards and mice only. Hubs and other USB devices are not supported.

3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the Setup program. This is supervisor mode.
- The user password gives restricted access to view and change Setup options in the Setup program. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 42 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 42. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options *	Can change all options *	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

* If no password is set, any user can change all Setup options.

See Section 4.4 for information about setting user and supervisor passwords.

4 BIOS Setup Program

The Setup program is for viewing and changing the BIOS settings for a computer. Setup is accessed by pressing the <F2> key after the Power-On Self Test (POST) memory test begins and before the operating system boot begins.

Table 43 shows the menus available from the menu bar at the top of the Setup screen.

Table 43. Setup Menu Bar

Setup Menu Screen	Description
Maintenance	Specifies the processor speed and clears the Setup passwords. This menu is only available in configure mode. Refer to Section 1.13 for information about configure mode.
Main	Allocates resources for hardware components.
Advanced	Specifies advanced features available through the chipset.
Security	Specifies passwords and security features.
Power	Specifies power management features.
Boot	Specifies boot options and power supply controls.
Exit	Saves or discards changes to the Setup program options.

Table 44 shows the function keys available for menu screens.

Table 44. Setup Function Keys

Setup Key	Description
<F1> or <Alt-H>	Brings up a help screen for the current item.
<Esc>	Exits the menu.
<←> or <→>	Selects a different menu screen.
<↑> or <↓>	Moves cursor up or down.
<Home> or <End>	Moves cursor to top or bottom of the window.
<PgUp> or <PgDn>	Moves cursor to top or bottom of the window.
<F5> or <->	Selects the previous value for a field.
<F6> or <+> or <Space>	Selects the next value for a field.
<F9>	Load the default configuration values for the current menu.
<F10>	Save the current values and exit Setup.
<Enter>	Executes command or selects the submenu.

4.1 Maintenance Menu

This menu is for setting the processor speed and clearing the Setup passwords. Setup only displays this menu in configure mode. See Section 1.13 for information about using configure mode.

Table 45. Maintenance Menu

Feature	Options	Description
Processor Speed	• 233 • 266 • 300 • 333	Specifies the processor speed in megahertz. This setup screen will only show speeds up to and including the maximum speed of the processor installed on the motherboard.
Clear All Passwords	No options	Clears the user and supervisor passwords.

4.2 Main Menu

This menu reports processor and memory information and is for configuring the system date and system time.

Table 46. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays the processor type.
Processor Speed	No options	Displays the processor speed.
Cache RAM	No options	Displays the size of the second-level cache.
System Memory	No options	Displays the total amount of RAM on the motherboard.
Memory Bank 0 Memory Bank 1	No options	Displays the size and type of DIMM installed in each memory bank.
Language	• **English (US) (default)** • Italian • Francais • Deutsch • Espanol	Displays the language used by the BIOS.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Month, day, and year	Specifies the current date.

4.3 Advanced Menu

This menu is for setting advanced features that are available through the chipset.

Table 47. Advanced Menu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if a Plug and Play operating system is being used. *No* lets the BIOS configure all devices. *Yes* lets the operating system configure Plug and Play devices. Not required with a Plug and Play operating system.
Reset Configuration Data	• **No (default)** • Yes	Clears the BIOS configuration data on the next boot.
Numlock	• Auto • **On (default)** • Off	Specifies the power on state of the Num Lock feature on the numeric keypad of the keyboard.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	No options	Specifies type of connected IDE device.
Floppy Options	No options	When selected, displays the Floppy Options submenu.
DMI Event Logging	No options	Configures DMI Events Logging. When selected, displays the DMI Events Logging submenu.
Video Configuration	No options	Configures video features. When selected, displays the Video Configuration submenu.
Resource Configuration	No options	Configures memory blocks and IRQs for legacy ISA devices. When selected, displays the Resource Configuration submenu.

4.3.1 Peripheral Configuration Submenu

This submenu is for the configuring the computer peripherals.

Table 48. Peripheral Configuration Submenu

Feature	Options	Description
Serial port	• Disabled • **Enabled (default)** • Auto	Configures the serial port. *Auto* assigns the first free COM port, normally COM1, the address 3F8h and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address** for the serial port.
Interrupt	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for the serial port.
IR port	• **Disabled (default)** • Enabled • Auto	Configures IR port. *Auto* assigns the first free COM port, normally COM1, the address 3F8h and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• **IrDA (default)** • ASK-IR	Specifies the IR mode.
Base I/O address	• 3F8 • **2F8 (default)** • 3E8 • 2E8	Specifies the base I/O address** for the IR port.
Interrupt	• **IRQ 3 (default)** • IRQ 4	Specifies the interrupt for the IR port.

** If either the serial port or the IR port address is set, that address will not appear in the list of options for the other port. If an ATI *mach32*† or an ATI *mach64*† video controller is active as an add-in board, the COM4, 2E8h address will not appear in the list of options for either the serial port or the IR port.

continued

Table 48. Peripheral Configuration Submenu (continued)

Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. *Output Only* operates in AT†-compatible mode. *Bi-directional* operates in bi-directional PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address	• **378 (default)** • 278 • 228	Specifies the base I/O address for the parallel port.
Interrupt	• IRQ 5 • **IRQ 7 (default)**	Specifies the interrupt for the parallel port.
Audio	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
Legacy USB Support	• **Disabled (default)** • Enabled	Enables or disables legacy USB support.

4.3.2 IDE Configuration

Table 49. IDE Configuration

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the Primary IDE Controller. *Secondary* enables only the Secondary IDE Controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	• Disabled • 3 Seconds • **6 Seconds (default)** • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.3.3 IDE Configuration Submenus

This submenu is for configuring IDE devices, including:

- Primary IDE master
- Primary IDE slave
- Secondary IDE master
- Secondary IDE slave

Table 50. IDE Configuration Submenus

Feature	Options	Description
Type	• None • ATAPI Removable • Other ATAPI • CD-ROM • User • IDE Removable • **Auto (default)**	Specifies the IDE configuration mode for IDE devices. *User* allows the cylinders, heads, and sectors fields to be changed. *Auto* automatically fills in the values for the cylinders, heads, and sectors fields.
Maximum Capacity	No options	Reports the maximum capacity for the hard disk.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • 16 Sectors	Specifies number of sectors per block for transfers from the hard drive to memory. Check the hard drive's specifications for optimum setting.
LBA Mode Control	• Disabled • Enabled	Enables or disables the LBA mode control.
Transfer Mode	• Standard • Fast PIO 1 • Fast PIO 2 • Fast PIO 3 • Fast PIO 4 • FPIO 3 / DMA 1 • FPIO 4 / DMA 2	Specifies the method for moving data to/from the drive.
Ultra DMA	• Disabled • Mode 0 • Mode 1 • Mode 2	Specifies the Ultra DMA mode for the drive.

4.3.4 Floppy Options Submenu

This submenu is for configuring the diskette drive interface.

Table 51. Floppy Options Submenu

Feature	Options	Description
Floppy Disk Controller	• Disabled • **Enabled (default)** • Auto	Disables or enables the integrated diskette drive controller.
Diskette A:	• Disabled • 360 KB, 5¼″ • 1.2 MB, 5¼″ • 720 KB, 3½″ • **1.44/1.25 MB, 3½″ (default)** • 2.88 MB, 3½″	Specifies the capacity and physical size of diskette drive A.
Floppy Write Protect	• **Disabled (default)** • Enabled	Disables or enables write protect for diskette drive A.

4.3.5 DMI Event Logging

This submenu is for configuring the DMI event logging features.

Table 52. DMI Event Logging Submenu

Feature	Options	Description
Event log capacity	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View DMI event log	No options	Enables viewing of DMI event log.
Clear all DMI event logs	• **No (default)** • Yes	Clears the DMI event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of DMI events.
Mark DMI events as read	No options	Marks all DMI events as read.

4.3.6 Video Configuration Submenu

This submenu is for configuring video features.

Table 53. Video Configuration Submenu

Feature	Options	Description
Palette Snooping	• **Disabled (default)** • Enabled	Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card.
AGP Aperture Size	• **64 MB (default)** • 256 MB	Specifies the aperture size for the AGP video controller.

4.3.7 Resource Configuration Submenu

This submenu is for configuring the memory and interrupts.

Table 54. Resource Configuration Submenu

Feature	Options	Description
Memory Reservation	• C800 - CBFF **Available (default)** | Reserved • CC00- CFFF **Available (default)** | Reserved • D000 - D3FF **Available (default)** | Reserved • D400 - D7FF **Available (default)** | Reserved • D800 - DBFF **Available (default)** | Reserved • DC00 - DFFF **Available (default)** | Reserved	Reserves specific upper memory blocks for use by legacy ISA devices.
IRQ Reservation	• IRQ3 **Available (default)** | Reserved • IRQ4 **Available (default)** | Reserved • IRQ5 **Available (default)** | Reserved • IRQ7 **Available (default)** | Reserved • IRQ10 **Available (default)** | Reserved • IRQ11 **Available (default)** | Reserved	Reserves specific IRQs for use by legacy ISA devices. An * (asterisk) displayed next to an IRQ indicates an IRQ conflict.

4.4 Security Menu

This menu is for setting passwords and security features.

Table 55. Security Menu

Feature	Options	Description
User Password Is	No options	Reports if there is a user password set.
Supervisor Password Is	No options	Reports if there is a supervisor password set.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Clear User Password	No Options	Clears the user password.
User Setup Access	• Name • **View Only (default)** • Limited Access • Full	Specifies the type of user access.
Unattended Start	• **Disabled (default)** • Enabled	Enables the unattended start feature. When enabled, the computer boots, but the keyboard is locked. The user must enter a password to unlock the computer or boot from a floppy diskette.

4.5 Power Menu

This menu is for setting power management features.

Table 56. Power Menu

Feature	Options	Description
Power Management Support	• Disabled • **Enabled (default)**	Enables or disables the BIOS power management feature.
Inactivity Timer	• **Off (default)** • 1 Minute • 5 Minutes • 10 Minutes • 20 Minutes • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	• Disabled • **Enabled (default)**	Enables power management for hard disks during standby and suspend modes.
VESA Video Power Down	• Disabled • **Standby (default)** • Suspend • Sleep	Specifies power management for video during standby and suspend modes.
Power Button Behavior	• **On/Off (default)** • Sleep/Wake	Specifies the function of the power button.

4.6 Boot Menu

This menu is for setting the boot features and the boot sequence.

Table 57. Boot Menu

Feature	Options	Description
Boot-time Diagnostic Screen	• **Disabled (default)** • Enabled	Displays the diagnostic screen during boot.
Quick Boot Mode	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Stay Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC/Power loss occurs. *Power On* restores power to the computer. *Stay Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred.

continued

Table 57. Boot Menu (continued)

On Modem Ring	• Stay Off • **Power On (default)**	Specifies how the computer responds to an incoming call on an installed modem when the power is off.
On LAN	• Stay Off • **Power On (default)**	Specifies how the computer responds to a LAN wakeup event when the power is off.
On PME	• **Stay Off (default)** • Power On	Specifies how the computer responds to a PME wakeup event when the power is off.
First Boot Device Second Boot Device Third Boot Device Fourth Boot Device	• Removable devices • Hard Drive • ATAPI CD-ROM Drive • Network Boot	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering.
Hard Drive	No options	Lists available hard drives. When selected, displays the Hard Drive submenu.
Removable Devices	No options	Lists available removable devices. When selected, displays the Removable Devices submenu.

4.6.1 Hard Drive Submenu

This submenu is for configuring the boot sequence for hard drives.

Table 58. Hard Drive Submenu

Options	Description
Bootable Add in Card	Specifies the boot sequence for the hard drives attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.6.2 Removable Devices Submenu

This submenu is for configuring the boot sequence for removable devices.

Table 59. Removable Devices Submenu

Options	Description
Legacy Floppy Drives	Specifies the boot sequence for the removable devices attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.7 Exit Menu

This menu is for exiting the Setup program, saving changes, and loading and saving defaults.

Table 60. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS RAM.
Exit Discarding Changes	Exits without saving any changes made in Setup.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

5.1 BIOS Error Messages

Table 61. BIOS Error Messages

Error Message	Explanation
Diskette drive A error	Drive A is present but fails the POST diskette tests. Check that the drive is defined with the proper diskette type in Setup and that the diskette drive is installed correctly.
Extended RAM Failed at offset: *nnnn*	Extended memory not working or not configured properly at offset *nnnn*.
Failing Bits: *nnnn*	The hexadecimal number *nnnn* is a map of the bits at the RAM address (System, Extended, or Shadow memory) that failed the memory test. Each 1 in the map indicates a failed bit.
Fixed Disk 0 Failure or Fixed Disk 1 Failure or Fixed Disk Controller Failure	Fixed disk is not working or not configured properly. Check to see if fixed disk is installed properly. Run Setup be sure the fixed-disk type is correctly identified.
Incorrect Drive A type - run SETUP	Type of diskette drive for drive A not correctly identified in Setup.
Invalid NVRAM media type	Problem with NVRAM (CMOS) access.
Keyboard controller error	The keyboard controller failed test. Try replacing the keyboard.
Keyboard error	Keyboard not working.
Keyboard error nn	BIOS discovered a stuck key and displays the scan code nn for the stuck key.
Keyboard locked - Unlock key switch	Unlock the system to proceed.
Monitor type does not match CMOS - Run SETUP	Monitor type not correctly identified in Setup.
Operating system not found	Operating system cannot be located on either drive A or drive C. Enter Setup and see if fixed disk and drive A are properly identified.
Parity Check 1	Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Parity Check 2	Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Press <F1> to resume, <F2> to Setup	Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change any settings.
Real time clock error	Real-time clock fails BIOS test. May require motherboard repair.

continued

Table 61. BIOS Error Messages (continued)

Error Message	Explanation
Shadow RAM Failed at offset: *nnnn*	Shadow RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System battery is dead - Replace and run SETUP	The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system.
System cache error - Cache disabled	RAM cache failed the BIOS test. BIOS disabled the cache.
System CMOS checksum bad - run SETUP	System CMOS RAM has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. Run Setup and reconfigure the system either by getting the default values and/or making your own selections.
System RAM Failed at offset: *nnnn*	System RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System timer error	The timer test failed. Requires repair of system motherboard.

nnnn = hexadecimal number

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

Table 62 provides the POST codes that can be generated by the BIOS. Some codes are repeated in the table because that code applies to more than one operation.

Table 62. Port 80h Codes

Code	Description of POST Operation
02h	Verify real mode
03h	Disable nonmaskable interrupt (NMI)
04h	Get processor type
06h	Initialize system hardware
08h	Initialize chipset with initial POST values
09h	Set IN POST flag
0Ah	Initialize CPU registers
0Bh	Enable CPU cache
0Ch	Initialize caches to initial POST values
0Eh	Initialize I/O component
0Fh	Initialize the local bus IDE
10h	Initialize power management
11h	Load alternate registers with initial POST *valuesnew*
12h	Restore CPU control word during warm boot
13h	Initialize PCI bus mastering devices
14h	Initialize keyboard controller
16h	BIOS ROM checksum
17h	Initialize cache before memory autosize
18h	8254 timer initialization
1Ah	8237 DMA controller initialization
1Ch	Reset programmable interrupt controller
20h	Test DRAM refresh
22h	Test keyboard controller
24h	Set ES segment register to 4 GB
26h	Enable A20 line
28h	Autosize DRAM
29h	Initialize POST memory manager

continued

Table 62. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
2Ah	Clear 512 KB base RAM
2Ch	RAM failure on address line *xxxx**
2Eh	RAM failure on data bits *xxxx** of low byte of memory bus
2Fh	Enable cache before system BIOS shadow
30h	RAM failure on data bits *xxxx** of high byte of memory bus
32h	Test CPU bus-clock frequency
33h	Initialize POST dispatch manager
34h	Test CMOS RAM
35h	Initialize alternate chipset registers
36h	Warm start shut down
37h	Reinitialize the chipset (motherboard only)
38h	Shadow system BIOS ROM
39h	Reinitialize the cache (motherboard only)
3Ah	Autosize cache
3Ch	Configure advanced chipset registers
3Dh	Load alternate registers with CMOS *valuesnew*
40h	Set Initial CPU speed new
42h	Initialize interrupt vectors
44h	Initialize BIOS interrupts
45h	POST device initialization
46h	Check ROM copyright notice
47h	Initialize manager for PCI option ROMs
48h	Check video configuration against CMOS RAM data
49h	Initialize PCI bus and devices
4Ah	Initialize all video adapters in system
4Bh	Display QuietBoot screen
4Ch	Shadow video BIOS ROM
4Eh	Display BIOS copyright notice
50h	Display CPU type and speed
51h	Initialize EISA motherboard
52h	Test keyboard
54h	Set key click if enabled
56h	Enable keyboard
58h	Test for unexpected interrupts
59h	Initialize POST display service
5Ah	Display prompt "Press F2 to enter SETUP"
5Bh	Disable CPU cache

continued

Table 62. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
5Ch	Test RAM between 512 and 640 KB
60h	Test extended memory
62h	Test extended memory address lines
64h	Jump to UserPatch1
66h	Configure advanced cache registers
67h	Initialize multiprocessor APIC
68h	Enable external and processor caches
69h	Setup System Management Mode (SMM) area
6Ah	Display external L2 cache size
6Ch	Display shadow-area message
6Eh	Display possible high address for UMB recovery
70h	Display error messages
72h	Check for configuration errors
74h	Test real-time clock
76h	Check for keyboard errors
7Ah	Test for key lock on
7Ch	Set up hardware interrupt vectors
7Eh	Initialize coprocessor if present
80h	Disable onboard Super I/O ports and IRQs
81h	Late POST device initialization
82h	Detect and install external RS232 ports
83h	Configure non-MCD IDE controllers
84h	Detect and install external parallel ports
85h	Initialize PC-compatible PnP ISA devices
86h	Re-initialize onboard I/O ports
87h	Configure motherboard configurable devices
88h	Initialize BIOS Data Area
89h	Enable nonmaskable Interrupts (NMIs)
8Ah	Initialize extended BIOS data area
8Bh	Test and initialize PS/2 mouse
8Ch	Initialize diskette controller
8Fh	Determine number of ATA drives
90h	Initialize hard-disk controllers
91h	Initialize local-bus hard-disk controllers
92h	Jump to UserPatch2
93h	Build MPTABLE for multiprocessor boards
94h	Disable A20 address line (Rel. 5.1 and earlier)
95h	Install CD-ROM for boot

continued

Table 62. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
96h	Clear huge ES segment register
97h	Fix up multiprocessor table
98h	Search for option ROMs
99h	Check for SMART Drive
9Ah	Shadow option ROMs
9Ch	Set up power management
9Eh	Enable hardware interrupts
9Fh	Determine number of ATA and SCSI drives
A0h	Set time of day
A2h	Check key lock
A4h	Initialize typematic rate
A8h	Erase F2 prompt
Aah	Scan for F2 key stroke
Ach	Enter SETUP
Aeh	Clear IN POST flag
B0h	Check for errors
B2h	POST done - prepare to boot operating system
B4h	One short beep before boot
B5h	Terminate QuietBoot
B6h	Check password (optional)
B8h	Clear global descriptor table
B9h	Clean up all graphics
Bah	Initialize DMI parameters
BBh	Initialize PnP Option ROMs
BCh	Clear parity checkers
BDh	Display MultiBoot menu
Beh	Clear screen (optional)
BFh	Check virus and backup reminders
C0h	Try to boot with INT 19h
C1h	Initialize POST Error Manager (PEM)
C2h	Initialize error logging
C3h	Initialize error display function
C4h	Initialize system error handler

continued

Table 62. Port 80h Codes (continued)

Code	Description of POST Operation (The following are for boot block in flash ROM)
E0h	Initialize the chipset
E1h	Initialize the bridge
E2h	Initialize the processor
E3h	Initialize system timer
E4h	Initialize system I/O
E5h	Check force recovery boot
E6h	Checksum BIOS ROM
E7h	Go to BIOS
E8h	Set huge segment
E9h	Initialize multiprocessor
Eah	Initialize OEM special code
Ebh	Initialize PIC and DMA
Ech	Initialize memory type
Edh	Initialize memory size
Eeh	Shadow boot block
Efh	System memory test
F0h	Initialize interrupt vectors
F1h	Initialize runtime clock
F2h	Initialize video
F3h	Initialize beeper
F4h	Initialize boot
F5h	Clear huge segment
F6h	Boot to mini-DOS
F7h	Boot to full DOS

* If the BIOS detects error 2Ch, 2Eh, or 30h (base 512 K RAM error), it displays an additional word-bitmap (xxxx) indicating the address line or bits that failed. For example, "2C 0002" means address line 1 (bit one set) has failed. "2E 1020" means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. The BIOS also sends the bitmap to the port-80 LED display. It first displays the check point code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.

5.3 BIOS Beep Codes

Whenever a recoverable error occurs during Power-On Self Test (POST), the BIOS displays an error message describing the problem. The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero.

An external ROM module (e.g., video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST Terminal Error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 63. Beep Codes

Beeps	Port 80h Code	Explanation
1-2-2-3	16h	BIOS ROM checksum
1-3-1-1	20h	Test DRAM refresh
1-3-1-3	22h	Test keyboard controller
1-3-3-1	28h	Autosize DRAM
1-3-3-2	29h	Initialize POST memory manager
1-3-3-3	2Ah	Clear 512 KB base RAM
1-3-4-1	2Ch	RAM failure on address line xxxx
1-3-4-3	2Eh	RAM failure on data bits xxxx of low byte of memory bus
1-4-1-1	30h	RAM failure on data bits xxxx of high byte of memory bus
2-1-2-2	45h	POST device initialization
2-1-2-3	46h	Check ROM copyright notice
2-2-3-1	58h	Test for unexpected interrupts
2-2-4-1	5Ch	Test RAM between 512 and 640 KB
1-2	98h	Search for option ROMs. One long, two short beeps on checksum failure

6 Specifications and Customer Support

6.1 Online Support

Find information about Intel motherboard at this World Wide Web site:

http://support.intel.com/

6.2 Specifications

The motherboard complies with the following specifications:

Table 64. Compliance with Specifications

Specification	Description	Revision Level
AGP	Accelerated Graphics Port Interface Specification	Revision 1.0, July, 1996, Intel Corporation. The specification is available through the Accelerated Graphics Implementers Forum at: http://www.agpforum.org/.
APM	Advanced Power Management BIOS interface specification	Revision 1.2, February, 1996 Intel Corporation, Microsoft Corporation
ACPI	Advanced Configuration and Power Interface specification	Revision 1.0, December 22, 1996 Intel Corporation, Microsoft Corporation, and Toshiba Corporation
ATA-3	Information Technology - AT Attachment-3 Interface	X3T10/2008D Revision 6 ATA Anonymous FTP Site: fission.dt.wdc.com
ATAPI	ATA Packet Interface for CD-ROMs	SFF-8020i Revision 2.5 (SFF) Fax Access: (408) 741-1600
ATX	ATX form factor specification	Revision 2.01, February 1997 Intel Corporation, The specification is available at: http://www.intel.com/
microATX	microATX form factor specification SFX Power Supply Design Guide	Version 1.0, December, 1997 Intel Corporation Version 1.0, December, 1997 Intel Corporation
DMI	Desktop Management Interface BIOS specification	Version 2.0, October 16, 1995 American Megatrends Inc., Award Software International Inc., Dell Computer Corporation, Intel Corporation, Phoenix Technologies Ltd., SystemSoft Corporation
El Torito	Bootable CD-ROM format specification	Version 1.0, January 25, 1995 Phoenix Technologies Ltd., IBM Corporation. The El Torito specification is available on the Phoenix Web site http://www.ptltd.com/techs/specs.html.

continued

Table 64. Compliance with Specifications (continued)

Specification	Description	Revision Level
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2], v1.7
PCI	PCI Local Bus specification	Revision 2.1, June 1, 1995, PCI Special Interest Group
Phoenix BIOS	Phoenix BIOS	Revision 4.0, February 27, 1997, Phoenix Technologies Ltd.
Plug and Play	Plug and Play BIOS specification	Version 1.0a, May 5, 1994 Compaq Computer Corporation, Phoenix Technologies Ltd., Intel Corporation
SDRAM DIMMs (64-and 72-bit)	PC SDRAM Unbuffered DIMM specification	Revision 0.9, October 22, 1997, Intel Corporation
USB	Universal serial bus specification	Revision 1.0, January 15, 1996 Compaq Computer Corporation, Digital Equipment Corporation, IBM PC Company, Intel Corporation, Microsoft Corporation, NEC, Northern Telecom