# Intel® Desktop Board VC820
## Technical Product Specification

*November 1999*

*Order Number 737611-001*

The Intel Desktop Board VC820 may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board VC820 Specification Update.

# Revision History

| Revision | Revision History | Date |
|---|---|---|
| -001 | Released Version | November 1999 |

This product specification applies only to standard VC820 desktop boards with BIOS identifier VC82010A.86A.

Changes to this specification will be published in the Intel Desktop Board VC820 Specification Update before being incorporated into a revision of this document.

# Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel Desktop Board VC820. It describes the standard VC820 board product.

## Intended Audience

The TPS is intended to provide detailed, technical information about the VC820 board and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

## What This Document Contains

| Chapter | Description |
|---|---|
| 1 | A description of the hardware used on this board |
| 2 | A map of the resources of the board |
| 3 | The features supported by the BIOS Setup program |
| 4 | The contents of the BIOS Setup program's menus and submenus |
| 5 | A description of the BIOS error messages, beep codes, POST codes, and enhanced diagnostics |

## Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

### Notes, Cautions, and Warnings

**NOTE**

*Notes call attention to important information.*

**CAUTION**

*Cautions are included to help you avoid damaging hardware or losing data.*

**WARNING**

*Warnings indicate conditions, which if not observed, can cause personal injury.*

## Other Common Notation

| | |
|---|---|
| # | Used after a signal name to identify an active-low signal (such as USBP0#) |
| (NxnX) | When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the board, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area. |
| KB | Kilobyte (1024 bytes) |
| Kbit | Kilobit (1024 bits) |
| MB | Megabyte (1,048,576 bytes) |
| Mbit | Megabit (1,048,576 bits) |
| GB | Gigabyte (1,073,741,824 bytes) |
| xxh | An address or data value ending with a lowercase h indicates a hexadecimal value. |
| x.x V | Volts. All voltages are DC unless otherwise specified. |
| † | This symbol is used to indicate third-party brands and names that are the property of their respective owners. |

# Contents

## 5 Error Messages and Beep Codes



## Figures

## Tables

# 1 Product Description

## What This Chapter Contains

# 1.1 Overview

## 1.1.1 Feature Summary

Table 1 summarizes the VC820 board's major features.

**Table 1. Feature Summary**

| | |
|---|---|
| **Form Factor** | ATX (12.0 inches by 8.2 inches) |
| **Processor** | Support for Intel® Pentium® III and Pentium II processors |
| **Memory** | • Two 168-pin RIMM† sockets<br>• Support for up to 512 MB |
| **Chipset** | Intel® 82820, consisting of:<br>• Intel 82820 Memory Controller Hub (MCH) with AHA (Accelerated Hub Architecture) bus<br>• Intel® 82801AA I/O Controller Hub (ICH) with AHA bus<br>• Intel® 82802AB 4 Mbit Firmware Hub (FWH) |
| **I/O Control** | LPC47M102 SIO low pin count (LPC) interface I/O controller |
| **Accelerated Graphics Port (AGP) Video** | AGP universal connector supporting 1X, 2X, and 4X AGP boards |
| **Peripheral Interfaces** | • Two serial ports<br>• Two Universal Serial Bus (USB) ports<br>• One parallel port<br>• Two IDE interfaces with Ultra DMA and ATA-66 support<br>• One diskette drive interface<br>• Game Port<br>• PS/2 keyboard and mouse |
| **Expansion Capabilities** | Seven add-in board expansion slots:<br>• Five PCI bus add-in board connectors (SMBus routed to PCI connector – slot 2)<br>• One AGP universal connector<br>• AMR (Audio/Modem Riser) connector |
| **BIOS** | • Intel/AMI BIOS<br>• Intel® 4 Mbit symmetrical flash memory<br>• Support for Advanced Power Management (APM), Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS. |
| **Enhanced Diagnostics** | Four dual-color LEDs on back panel |
| **Hardware Monitor Subsystem** | • Two fan sense inputs used to monitor fan activity<br>• Two pin header security feature for intrusion detection<br>• Remote diode temperature sense<br>• Voltage sense to detect out of range values<br>• Hardware monitor component |

continued

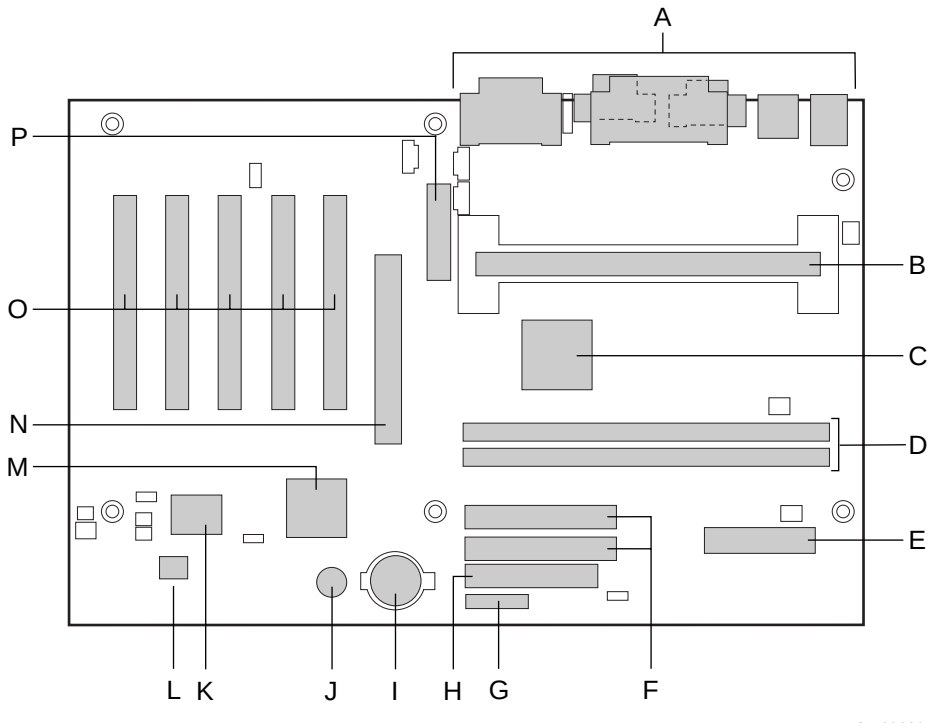
**Table 1. Feature Summary** (continued)

| | |
|---|---|
| **Instantly Available PC** | • Support for *PCI Local Bus Specification Revision 2.2*<br>• Suspend to RAM support<br>• Wake on PS/2 keyboard and USB ports |
| **Audio** | Audio Codec ’97 V 1.03 (VC ’97) compliant features including ICH and AMR with enhanced PCI audio supported by the Creative Labs ES1373 AC ’97 Digital Controller with Crystal Semiconductor CS4297 (A) Stereo Audio Codec |
| **Wake on LAN† Technology Connector** | Support for system wake up using an add-in network interface board with remote wake up capability |
| **Wake on Ring Connector** | Support for system wake up using an add-in telephony device, such as a modem |
| **SCSI LED Connector** | Allows add-in SCSI controllers to use the same LED as the onboard I/O controller |

| For information about | Refer to |
|---|---|
| The VC820 board’s compliance level with APM, ACPI, Plug and Play, and SMBIOS | Section 1.3, page 16 |

## 1.1.2 VC820 Desktop Board Layout

Figure 1 shows the location of the major components on the VC820 board.




| | | | |
|---|---|---|---|
| A | Back panel connectors | I | Battery |
| B | 242-contact slot connector | J | Speaker |
| C | Intel 82820 Memory Controller Hub (MCH) | K | SMSC LPC47M102 I/O Controller |
| D | RIMM sockets | L | Intel 82802AB 4 Mbit Firmware Hub (FWH) |
| E | Power connector | M | Intel 82801AA I/O Controller Hub (ICH) |
| F | IDE connectors | N | AGP universal connector |
| G | Front panel connector | O | PCI bus add-in board connectors |
| H | Diskette drive connector | P | Audio/Modem Riser (AMR) connector |

**Figure 1. VC820 Board Components**

## 1.1.3 Block Diagram

Figure 2 is a block diagram of the major functional areas of the VC820 board.

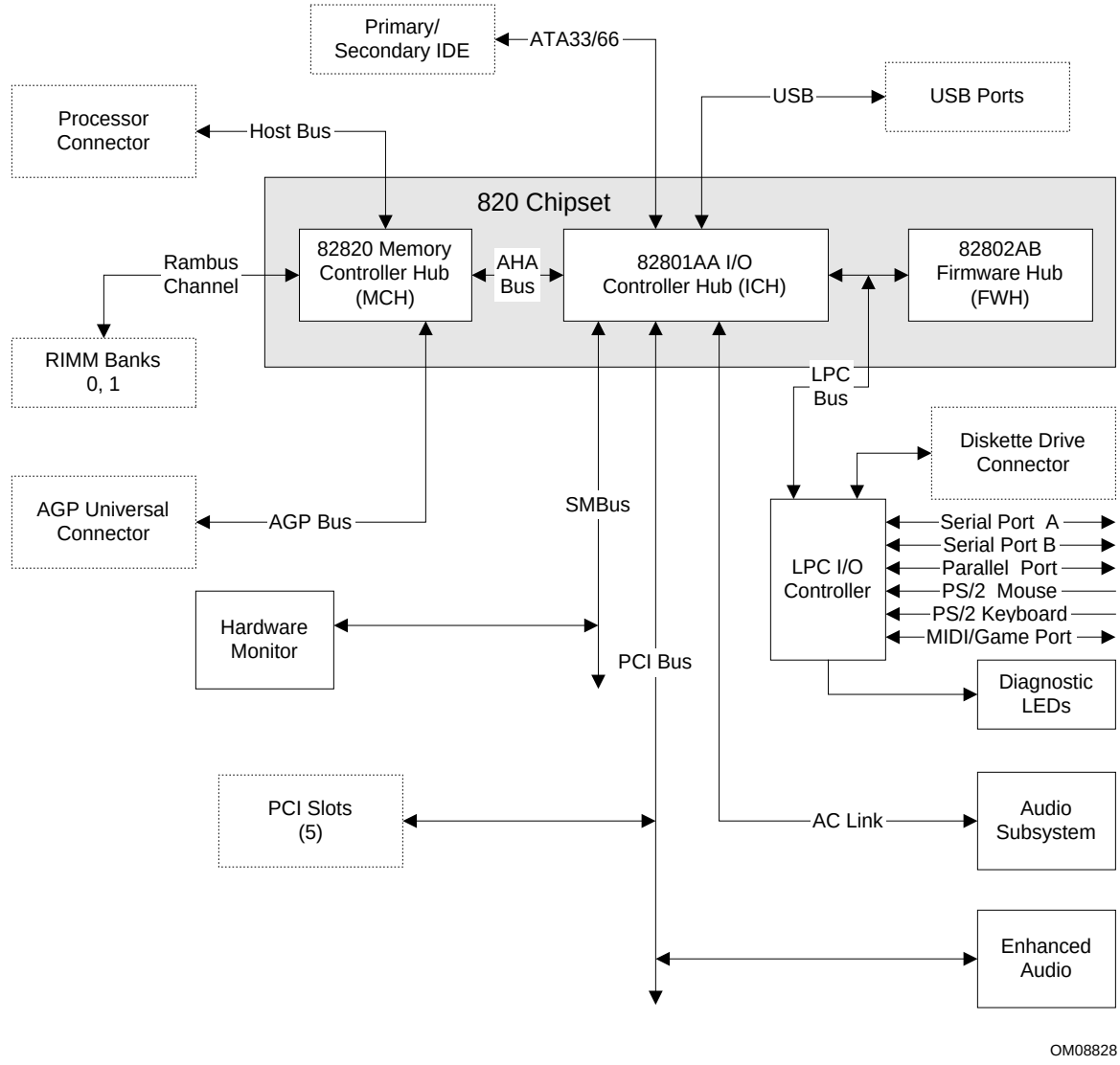



**Figure 2. Block Diagram**

## 1.2 Online Support

Find information about Intel desktop boards under “Product Info” or “Customer Support” at these World Wide Web sites:

http://www.intel.com/design/motherbd
http://support.intel.com/support/motherboards/desktop

Find “Processor Data Sheets” or information about “Proper Date Access in Systems with Intel Motherboards” at these World Wide Web sites:

http://www.intel.com/design/litcentr
http://support.intel.com/support/year2000

Find information about the ICH addressing at this World Wide Web site:
http://developer.intel.com/design/chipsets/datashts/

## 1.3 Design Specifications

Table 2 lists the specifications applicable to the VC820 board.

**Table 2. Specifications**

| Reference Name | Specification Title | Version, Revision Date, and Ownership | The information is available from… |
|---|---|---|---|
| AC ‘97 | *Audio Codec ‘97* | Version 2.1,<br>May 1998,<br>Intel Corporation. | ftp://download.intel.com/<br>pc-supp/platform/ac97 |
| ACPI | *Advanced Configuration and Power Interface Specification* | Version 1.0b,<br>February 2, 1999,<br>Intel Corporation,<br>Microsoft Corporation,<br>and Toshiba Corporation. | http://www.teleport.com/~acpi/ |
| AGP | *Accelerated Graphics Port Interface Specification* | Version 2.0,<br>May 4, 1998,<br>Intel Corporation. | the Accelerated Graphics Implementers Forum at:<br>http://www.agpforum.org/ |
| AMI BIOS | *American Megatrends BIOS Specification* | AMIBIOS 99,<br>1999<br>American Megatrends, Inc. | http://www.amibios.com, or<br>http://www.ami.com/download/<br>amibios99.pdf |
| AMR | *Audio/Modem Riser Specification* | Version 1.01,<br>September 10, 1998,<br>Intel Corporation. | ftp://download.intel.com/<br>pc-supp/platform/ac97/<br>amr101.pdf |
| APM | *Advanced Power Management BIOS Interface Specification* | Version 1.2,<br>February 1996,<br>Intel Corporation,<br>Microsoft Corporation. | http://www.microsoft.com/<br>hwdev/busbios/amp_12.htm |

continued

**Table 2. Specifications** (continued)

| Description | Specification Title | Version, Revision Date and Ownership | The information is available from… |
|---|---|---|---|
| ATA-3 | *Information Technology - AT Attachment-3 Interface, X3T10/2008D* | Version 6, October 1995, ASC X3T10 Technical Committee | http://www.t13.org/ |
| ATAPI | *Information Technology AT Attachment with Packet Interface Extensions T13/1153D* | Version 18, August 19, 1998, Contact: T13 Chair, Seagate Technology | http://www.t13.org |
| ATX | *ATX Specification* | Version 2.01, February 1997, Intel Corporation. | http://developer.intel.com/design/motherbd/atx.htm |
| EPP | *Enhanced Parallel Port IEEE std 1284.1-1997* | Version 1.7, 1997, Institute of Electrical and Electronic Engineers | http://standards.ieee.org/catalog/bus.html |
| El Torito | *Bootable CD-ROM format specification* | Version 1.0, January 25, 1995, Phoenix Technologies Ltd., and IBM Corporation. | the Phoenix Web site at: http://www.ptltd.com/techs/specs.html |
| IrDA† | *Serial Infrared Physical Layer Link specification* | Version 1.1, October 17, 1995, Infrared Data Association. | http://www.irda.org/standards/pubs/IrData.zip |
| LPC | *Low Pin Count Interface Specification* | Version 1.0, September 29, 1997, Intel Corporation. | http://www.intel.com/design/chipsets/industry/lpc.htm |
| PCI | *PCI Local Bus Specification* | Version 2.2, December 18, 1998, PCI Special Interest Group. | http://www.pcisig.com/ |
| | *PCI Bus Power Management Interface Specification* | Version 1.1, December 18, 1998' PCI Special Interest Group. | http://www.pcisig.com/ |
| Plug and Play | *Plug and Play BIOS specification* | Version 1.0a, May 5, 1994, Compaq Computer Corp., Phoenix Technologies Ltd., and Intel Corporation. | http://www.microsoft.com/hwdev/respec/pnpspecs.htm |
| RIMM | *Rambus Serial Presence Detect (SPD) Specification* | Version 1.0, March 1999, Rambus Corp. | http://www.rambus.com/developer/support_rimm.html |
| | *Rambus RIMM specification* | Version 1.0 February 1999 Rambus Corp. | http://www.rambus.com/developer/development_support.html |

continued

**Table 2. Specifications** (continued)

| Description | Specification Title | Version, Revision Date and Ownership | The information is available from… |
|---|---|---|---|
| SMBIOS | *System Management BIOS* | Version 2.3,<br>August 12, 1998,<br>Award Software International Inc.,<br>Dell Computer Corporation,<br>Hewlett-Packard Company,<br>Intel Corporation,<br>International Business Machines Corporation,<br>Phoenix Technologies Limited,<br>American Megatrends Inc.,<br>and SystemSoft Corporation. | http://developer.intel.com/ial/wfm/design/smbios |
| UHCI | *Universal Host Controller Interface Design Guide* | Version 1.1,<br>March 1996,<br>Intel Corporation. | http://developer.intel.com/design/USB/UHCI11D.htm |
| USB | *Universal Serial Bus Specification* | Version 1.1,<br>September 23, 1998,<br>Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC. | http://www.usb.org/developers |
| WfM | *Wired for Management Baseline* | Version 2.0,<br>December 18, 1998,<br>Intel Corporation | http://developer.intel.com/ial/WfM/wfmspecs.htm |

# 1.4 Processor

### ⚠ CAUTION

*The VC820 desktop board supports processors that have a 19.3 A maximum current draw (2 V core), or a 22.0 A maximum current draw (1.6 V core). Using a processor not in compliance with these guidelines can damage the processor, the board, and the power supply. See the processor's data sheet for current usage requirements.*

### ⚠ CAUTION

*Before installing or removing the processor, make sure that AC power has been removed by unplugging the power cord from the computer (the standby power indicator LED should not be lit). Failure to do so could damage the processor and the board. See Figure 6, page 40 for the location of the standby power indicator LED.*

### NOTE

*66 MHz host bus frequency processors are not supported in this product. A hardware lockout is provided so that if such a processor is installed, the VC820 board will not power-up.*

The VC820 desktop board supports either a single Pentium III processor at host bus frequencies of 100 or 133 MHz, or a single Pentium II processor at a host bus frequency of 100 MHz. Host bus frequencies for all processors are automatically selected.

The VC820 board supports up to 512 KB L2 cache. All supported onboard memory can be cached up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

The VC820 board supports the 242-contact slot type processors listed in Table 3. The processor must be secured by a retention mechanism attached to the board.

**Table 3. Supported Processors**

| Processor Type | Processor Designation (MHz) | Host Bus Frequency (MHz) | L2 Cache Size (KB) |
|---|---|---|---|
| Pentium III processor | 450, 500, 550, and 600 | 100 | 512 |
| | 550E, 600E, 650, and 700 | 100 | 256 |
| | 533B and 600B | 133 | 512 |
| | 533EB, 600EB, 667, and 733 | 133 | 256 |
| Pentium II processor | 350, 400, and 450 | 100 | 512 |

| For information about | Refer to |
|---|---|
| Processor support for the VC820 boards | Section 1.2, page 16 |
| Processor data sheets | Section 1.2, page 16 |

# 1.5 System Memory

**CAUTION**

*Incorrect insertion of RIMM modules or continuity RIMM modules in the RIMM connectors can damage the VC820 board.*

**CAUTION**

*Before installing or removing RIMM modules, make sure that AC power has been removed by unplugging the power cord from the computer (the standby power indicator LED should not be lit). Failure to do so could damage the memory and the board. See Figure 6, page 40 for the location of the standby power indicator LED.*

## 1.5.1 RDRAM Terminology

The VC820 desktop board uses RDRAM technology. For clarity, some RDRAM terms and definitions are included in the list below.

- The terms Direct Rambus† and Direct RDRAM are simplified to Rambus and RDRAM.
- The Rambus Memory System includes the Memory Controller, which in turn includes the Rambus interface, the Rambus Channel, and the DRAMs with the Rambus interface.
- The Rambus Memory Module for desktop systems is referred to as the RIMM module. The RIMM connector supports a RIMM module.
- The RIMM module and RIMM connector use a form factor similar to the DIMM module and connector. They do not, however, work interchangeably.

## 1.5.2 Memory Features

The Intel 82820 Memory Controller Hub (MCH) integrates a single Rambus channel as an electrically pipelined serial bus (16 data bits in width) with uniform impedance of 28 ohms and single ended termination. This Rambus channel is capable of providing a processor-to-memory bandwidth up to 1.6 GB/sec.

The board supports the following memory features:

- Up to two 2.5 V, 168-pin, RIMM modules
- Single- or double-sided RIMM module configurations
- Serial Presence Detect (SPD) memory only
- Non-ECC memory with 16-bit components (128 Mbit technology)
- ECC memory with 18-bit components (144 Mbit technology)
- 512 MB maximum onboard capacity using 128/144 Mbit technology

| For information about | Refer to |
|---|---|
| The *Rambus RIMM Specification* | Section 1.3, page 16 |
| The *Direct Rambus Serial Presence Detect (SPD) Specification* | Section 1.3, page 16 |

### 1.5.3 Continuity RIMM Modules

All RIMM connectors must be populated to achieve continuity for termination at the Rambus interface. Continuity RIMMs (or "pass-through" modules) must be installed in any unused RIMM connectors.

### 1.5.4 RDRAM Memory Configuration

**CAUTION**

*The board supports combinations of no more than 32 RDRAM components across the installed RIMM modules. If the total number of RDRAM components installed in RIMM connectors exceeds 32, the computer will not boot.*

Table 4 gives examples of RDRAM component-counts for various RIMM modules. Component counts can be identified on the RIMM label.

**Table 4. Typical RIMM Module Configurations**

| Rambus Technology | 4 RDRAM components per RIMM | 6 RDRAM components per RIMM | 8 RDRAM components per RIMM | 12 RDRAM components per RIMM | 16 RDRAM components per RIMM |
|---|---|---|---|---|---|
| 128/144 Mbit | 64 MB | 96 MB | 128 MB | 192 MB | 256 MB |

**NOTE**

*To obtain best memory bus loading characteristics, RIMM modules should be installed in Bank 0 first and then in Bank 1. (Bank 0 is closest to the processor.) A Continuity RIMM module must be installed in Bank 1 if unused.*

## 1.5.5 Memory Bus Frequencies

The BIOS automatically selects the memory bus frequency from the Serial Presence Detect (SPD) information in the RIMM module. The VC820 platform supports only Serial Presence Detect (SPD) memory. Serial Presence Detect (SPD) information is required to properly configure the Rambus interface. Table 5 describes the memory frequencies supported with standard configurations of the board. The BIOS configures the Rambus interface to the speed of the slowest RIMM module installed.

### ⟹ NOTE

Intel recommends using only tested memory. For a list of tested memory, see the User-Installable Upgrades Web page at: http://developer.intel.com/design/motherbd/vc/vc_user.htm

**Table 5. Memory Bus Frequency with DRCG (Rambus Clock Generator)**

| | PC600 | PC700 | PC800 |
|---|---|---|---|
| Host Bus frequency: 100 MHz | 300 MHz | See footnote* | 400 MHz |
| Host Bus frequency: 133 MHz | 266 MHz | 356 MHz | 400 MHz |

* The BIOS configures the Rambus interface to a memory bus frequency of 300 MHz for PC700 memory when configured with a host bus speed of 100 MHz. This is equivalent to PC600 performance.

## 1.5.6 ECC Memory

ECC memory detects multiple-bit errors and corrects single-bit errors. When ECC memory is installed, the BIOS will support both ECC and non-ECC mode. The BIOS automatically detects if ECC memory is installed and provides the Setup option for selecting ECC mode. ECC mode must be enabled in the Setup program; the default setting is disabled. If any non-ECC memory is installed, ECC operation is not available.

Table 6 describes the effect of using Setup to put each memory type in each supported mode.

**Table 6. Memory Error Detection Mode Established in Setup Program**

| Memory Type | ECC Disabled | ECC Enabled |
|---|---|---|
| Non-ECC RIMM | No error detection | N/A |
| ECC RIMM | No error detection | Single-bit error correction, multiple-bit error detection |

### ⟹ NOTE

*Whenever ECC mode is selected in Setup, some performance loss may occur.*

# 1.6 Intel® 820 Chipset

The Intel® 820 chipset consists of the following devices:

- 82820 Memory Controller Hub (MCH) with Accelerated Hub Architecture (AHA) bus
- 82801AA I/O Controller Hub (ICH) with AHA bus
- 82802AB Firmware Hub (FWH)

The chipset provides the host, memory, AGP, and I/O interfaces shown in Figure 3.

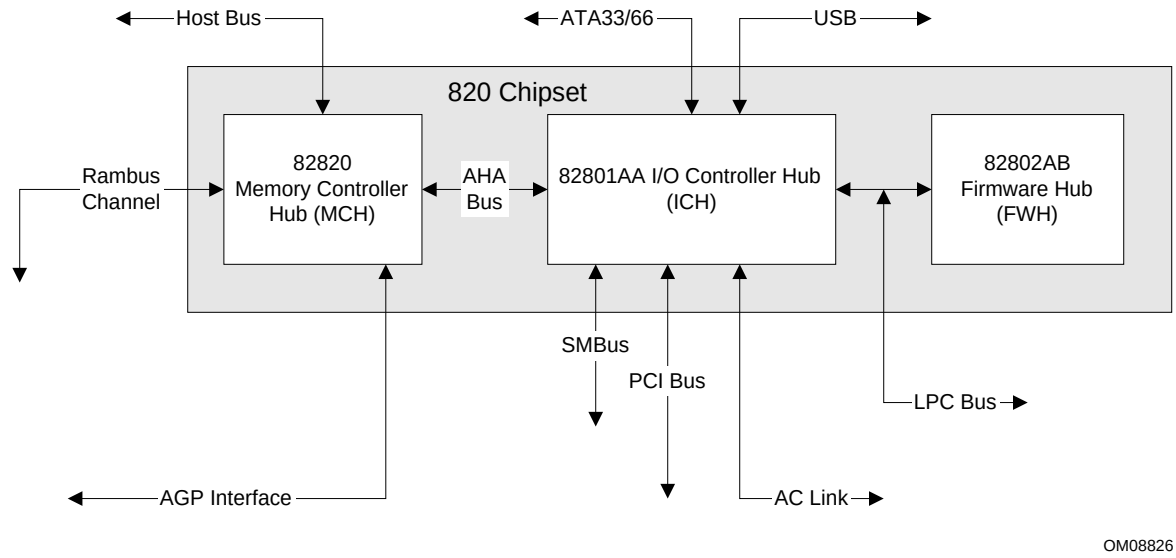



**Figure 3. Intel 820 Chipset Block Diagram**

| For information about | Refer to |
|---|---|
| The Intel 820 chipset | http://developer.intel.com |
| The resources used by the chipset | Chapter 2 |
| The chipset's compliance with ACPI, APM, AC '97 | Section 1.3, page 16 |

### 1.6.1 AGP

The VC820 board supports 1x, 2x, and 4x AGP boards. AGP is a high-performance bus for graphics-intensive applications, such as 3-D applications. AGP, while based on the *PCI Local Bus Specification*, Rev. 2.1, is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amounts of graphics data with the following features:

- Pipelined memory Read and Write operations that hide memory access latency
- De-multiplexing of address and data in the bus for nearly 100 percent bus efficiency

| For information about | Refer to |
|---|---|
| Obtaining the *Accelerated Graphics Port Interface Specification* | Section 1.3, page 16 |

### 1.6.2 USB

The VC820 board has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The two USB ports are implemented with stacked back panel connectors. The VC820 board fully supports UHCI and uses UHCI-compatible software drivers. USB features include:

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

**NOTE**

*Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.*

| For information about | Refer to |
|---|---|
| The location of the USB connectors on the back panel | Figure 8, page 50 |
| The signal names of the USB connectors | Table 18, page 51 |
| The USB specification and UHCI | Section 1.3, page 16 |

## 1.6.3 IDE Support

### 1.6.3.1 IDE Interfaces

The VC820 board has two independent bus-mastering IDE interfaces. These interfaces support:

- ATAPI devices (such as CD-ROM drives)
- ATA devices using the transfer modes listed in Table 68 on page 103

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The VC820 board supports laser servo (LS-120) diskette technology through its IDE interfaces. The LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

| For information about | Refer to |
|---|---|
| The location of the IDE connectors | Figure 10, page 57 |
| The signal names of the IDE connectors | Table 31, page 58 |
| BIOS Setup program's Boot menu | Table 74, page 109 |
| Ultra ATA/66 | Section 3.3.2, page 85 |

### 1.6.3.2 SCSI Hard Drive Activity LED Connector

The SCSI hard drive activity LED connector is a 1 x 2-pin connector that allows add-in SCSI controller to use the same LED as the IDE controller. This connector can be attached to the LED output of the add-in controller board. The LED will indicate when data is being read or written using the add-in controller.

| For information about | Refer to |
|---|---|
| The location of the SCSI hard drive activity LED connector | Figure 10, page 57 |
| The signal names of the SCSI hard drive activity LED connector | Table 30, page 58 |

## 1.6.4 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multi-century calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

**NOTE**

*If the battery and AC power fail, standard defaults, not custom defaults, will be loaded into CMOS RAM at power-on.*

**NOTE**

*The recommended method of accessing the date in systems with VC820 boards is indirectly from the Real-Time Clock (RTC) via the BIOS. The BIOS on VC820 boards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.*

| For information about | Refer to |
|---|---|
| Proper date access in systems with VC820 boards | Paragraph 1.2, page 16 |

# 1.7 I/O Controller

The SMSC LPC47M102 I/O Controller provides the following features:

- Low pin count (LPC) interface
- 3.3V operation
- Two serial ports
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.2 MB, 1.44 MB, or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake up event interface
- PME (Power Management Event) Interface
- IrDA† 1.0 compliant
- Fan control:
  - Two fan control outputs
  - Two fan tachometer inputs

The BIOS Setup program provides configuration options for the I/O controller.

| For information about | Refer to |
|---|---|
| SMSC LPC47M102 I/O controller | http://www.smsc.com |

### 1.7.1 Serial Ports

The VC820 board has two 9-pin D-Sub serial port connectors located on the back panel. The serial ports' NS16C550-compatible UARTs support data transfers at speeds up to 115.2 kbits/sec with BIOS support. The serial ports can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

| For information about | Refer to |
|---|---|
| The location of the serial port connectors | Figure 8, page 50 |
| The signal names of the serial port connectors | Table 20, page 52 |

### 1.7.2 Infrared Support

On the front panel connector, there are four pins that support Hewlett Packard HSDL-1000 compatible infrared (IR) transmitters and receivers. In the BIOS Setup program, Serial Port B can be directed to a connected IR device. (In this case, the serial port B connector on the back panel cannot be used.) The IR connection can be used to transfer files to or from portable devices like laptops, PDAs, and printers. The Infrared Data Association (IrDA) specification supports data transfers of 115 Kbits/sec at a distance of 1 meter.

| For information about | Refer to |
|---|---|
| The infrared port connector | Table 43, page 68 |
| Configuring serial port B for infrared applications | Section 4.4.3, page 100 |
| The IrDA specification | Section 1.3, page 16 |

### 1.7.3 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel. In the BIOS Setup program, the parallel port can be configured for the following:

- Output only (PC AT† -compatible mode)
- Bi-directional (PS/2 compatible)
- EPP
- ECP

| For information about | Refer to |
|---|---|
| The location of the parallel port connector | Figure 8, page 50 |
| The signal names of the parallel port connector | Table 19, page 52 |

## 1.7.4 Diskette Drive Controller

The I/O controller supports one diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT and PS/2 modes.

### NOTE

*The I/O controller also supports a 1.2 MB, 3.5-inch diskette drive. A special driver is required for this configuration however.*

| For information about | Refer to |
|---|---|
| The location of the diskette drive connector | Figure 10, page 57 |
| The signal names of the diskette drive connector | Table 32, page 59 |
| The supported diskette drive capacities and sizes | Table 69, page 104 |

## 1.7.5 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

### NOTE

*The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.*

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del> for a software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the power-on self-test (POST).

| For information about | Refer to |
|---|---|
| The location of the keyboard and mouse connectors | Figure 8, page 50 |
| The signal names of the keyboard and mouse connectors | Table 17, page 51 |

# 1.8 Audio

The VC820 desktop board offers an enhanced PCI audio system consisting of:

- Intel 82801AA I/O Controller Hub (ICH)
- AMR connector
- Creative Labs' PCI-128 capable ES1373 digital controller with Crystal Semiconductor CS4297 (A) codec

The ICH and AMR support these features:

- Split digital/analog architecture for improved S/N (signal-to-noise) ratio: ≥ 85 dB
- Power management support for APM 1.2 and ACPI 1.0 (driver dependant)
- 3-D stereo enhancement

The enhanced PCI audio subsystem has additional features described below.

## 1.8.1 Enhanced PCI Audio Subsystem

The VC820 board offers an AC '97 V 1.03 compliant audio feature-set supported by the Creative Labs ES1373 digital controller with Crystal Semiconductor CS4297 (A) codec (see Figure 4 below). AC '97 uses a five-wire digital serial interface between the PCI digital controller and the audio codec splitting the digital and analog architecture for improved S/N ratio. This approach supports downloadable wavetables utilizing system memory, eliminating the requirement for a hardware wavetable ROM.

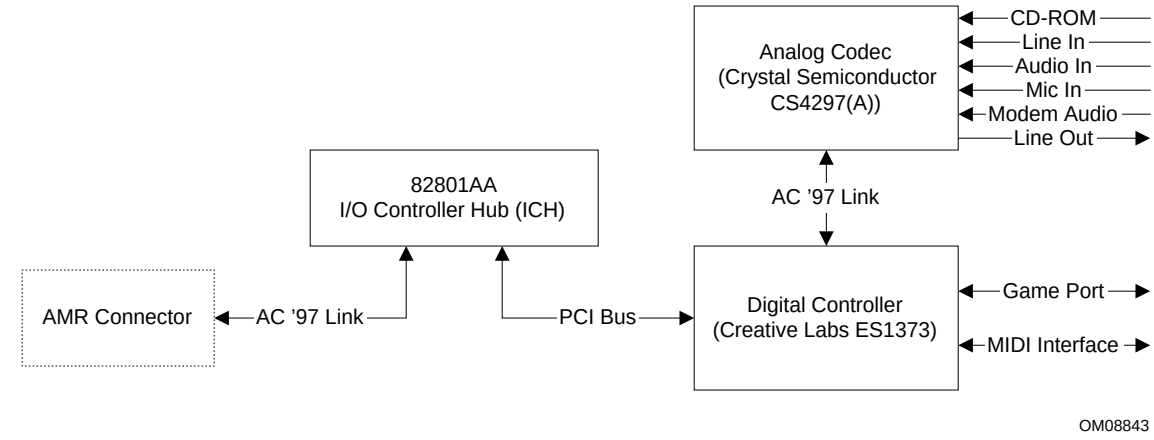



**Figure 4. Block Diagram of AC '97 V 1.03 Compatible Audio Subsystem with Creative Labs ES1373 Controller and AMR Connector**

The enhanced PCI audio subsystem supports the following audio connectors:

- Audio inputs:
  - Three analog line-level stereo inputs for connection from the back-panel; line in, CD and auxiliary line in
  - One analog line-level input for speakerphone (telephony)
  - One mono microphone input
- Audio outputs:
  - Stereo line-level output
  - Mono output for speakerphone (telephony)

The Creative Labs ES1373 digital controller with the Crystal Semiconductor CS4297 (A) codec support the following features:

- Creative Labs ES1373 AC ’97 V1.03 Digital Controller:
  - PCI 2.1 compliant
  - PCI bus master for PCI audio
  - 128-voice wavetable synthesizer
  - Aureal A3D† API, Sound Blaster Pro†, Roland MPU-401 MIDI, joystick compatible
  - Ensoniq 3D positional audio and Microsoft DirectSound† 3D support
- Crystal Semiconductor CS4297 (A) Stereo Audio Codec:
  - High performance 18-bit stereo full-duplex audio codec with up to 48 kHz sampling rate
  - Connects to the ES1373 digital controller using a five-wire digital interface.

| For information about | Refer to |
|---|---|
| Obtaining audio software and utilities | Paragraph 1.2, page 16 |

## 1.8.2 Audio Connectors

The audio connectors include the following:

- CD-ROM (legacy-style 2-mm connector)
- ATAPI-style connectors:
  - CD-ROM
  - Telephony
  - Auxiliary line in
- Back panel audio connectors:
  - MIDI/Game Port
  - Line out
  - Line in
  - Mic in
- Audio/Modem Riser (AMR)

| For information about | Refer to |
|---|---|
| The back panel audio connectors | Section 2.8.1, page 50 |

### 1.8.2.1 CD-ROM (Legacy-style 2 -mm) Connector

A 1 x 4-pin legacy-style 2-mm connector connects an internal CD-ROM drive to the audio mixer.

| For information about | Refer to |
|---|---|
| The location of the legacy-style 2-mm connector | Figure 9, page 55 |
| The signal names of the legacy-style 2 mm connector | Table 25, page 56 |

### 1.8.2.2 ATAPI CD-ROM Audio Connector

A 1 x 4-pin ATAPI-style connector connects an internal ATAPI CD-ROM drive to the audio mixer.

| For information about | Refer to |
|---|---|
| The location of the ATAPI CD-ROM connector | Figure 9, page 55 |
| The signal names of the ATAPI CD-ROM connector | Table 26, page 56 |

### 1.8.2.3 Telephony Connector

A 1 x 4-pin ATAPI-style connector connects the monoaural audio signals of an internal telephony device to the audio subsystem. A monaural audio-in and audio-out signal interface is necessary for telephony applications such as speakerphones, fax/modems, and answering machines.

| For information about | Refer to |
|---|---|
| The location of the telephony connector | Figure 9, page 55 |
| The signal names of the telephony connector | Table 27, page 56 |

### 1.8.2.4 Auxiliary Line In Connector

A 1 x 4-pin ATAPI-style connector connects the left and right channel signals of an internal audio device to the audio subsystem.

| For information about | Refer to |
|---|---|
| The location of the auxiliary line in connector | Figure 9, page 55 |
| The signal names of the auxiliary line in connector | Table 28, page 56 |

### 1.8.2.5 Audio/Modem Riser (AMR) Connector

The AMR is a 46-pin riser connector that supports adding modems and/or audio risers to VC820 boards. The AMR interface, utilizing an AC ’97 2.1 link, includes support for audio codec, modem codec, and audio/modem codec devices.

| For information about | Refer to |
|---|---|
| The location of the Audio/Modem Riser connector | Figure 12, page 63 |
| The signal names of the Audio/Modem Riser connector | Table 42, page 66 |
| The AMR specification | Section 1.3, page 16 |

# 1.9 Hardware Management Features

The hardware management features enable the VC820 board to be compatible with the Wired for Management (WfM) specification. The VC820 board has several hardware management features, including the following:

- Hardware monitor component
- Chassis intrusion detection
- Fan control and monitoring (implemented on the SMSC LPC47M102 I/O controller)

| For information about | Refer to |
|---|---|
| The WfM specification | Table 2, page 16 |
| Fan control functions of the SMSC LPC47M102 I/O controller | Section 1.7, page 26 |

## 1.9.1 Hardware Monitor Component

The hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing
- Remote thermal diode sensing for direct monitoring of processor temperature (if supported in the processor)
- Power supply monitoring (+12, +5, +3.3, +2.5, 3.3 VSB, $V_{CCP}$) to detect levels above or below acceptable values
- SMBus interface

## 1.9.2 Chassis Intrusion Detect Connector

The VC820 board supports a chassis security feature that detects if the chassis cover is removed. For the chassis intrusion circuit to function, the chassis' power supply must be connected to AC power. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion detect connector. The mechanical switch is closed for normal computer operation.

| For information about | Refer to |
|---|---|
| The location of the chassis intrusion detect connector | Figure 11, page 60 |
| The signal names of the chassis intrusion detect connector | Table 39, page 62 |

# 1.10 Power Management Features

Power management is implemented at several levels, including:

- Software support:
  - Advanced Power Management (APM)
  - Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - Wake on LAN technology
  - Instantly Available technology
  - Wake on Ring
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 keyboard
  - PME# wakeup support

## 1.10.1 Software Support

The software support for power management includes:

- APM
- ACPI

If the VC820 board is used with an ACPI-aware operating system, the BIOS can provide ACPI support. Otherwise, it defaults to APM support.

### 1.10.1.1 APM

APM makes it possible for the computer to enter an energy-saving standby mode. The standby mode can be initiated in the following ways:

- Time-out period specified in the BIOS Setup program
- From the operating system, such as the Standby menu item in Windows† 98

In standby mode, the VC820 board can reduce power consumption by spinning down hard drives, and reducing power to, or turning off of, VESA† DPMS-compliant monitors. Power management mode can be enabled or disabled in the BIOS Setup program

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power management features to work. For example, Windows 98 supports the power management features upon detecting that APM is enabled in the BIOS.

| For information about | Refer to |
|---|---|
| Enabling or disabling power management in the BIOS Setup program | Section 4.6, page 107 |
| The VC820 board's compliance level with APM | Table 2, page 16 |

### 1.10.1.2 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the VC820 board requires an operating system that supports ACPI. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM support normally contained in the BIOS
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 9 on page 37)
- Support for a front panel power and sleep mode switch. Table 7 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

**Table 7. Effects of Pressing the Power Switch**

| If the system is in this state… | …and the power switch is pressed for… | …the system enters this state |
|---|---|---|
| Off (ACPI G2/S5 – Soft off) | Less than four seconds | Power-on (ACPI G0 – working state) |
| On (ACPI G0 – working state) | Less than four seconds | Soft-off/Standby (ACPI G1 – sleeping state) |
| On (ACPI G0 – working state) | More than four seconds | Fail safe power-off (ACPI G2/S5 – Soft off) |
| Sleep (ACPI G1–sleeping state) | Less than four seconds | Wake up (ACPI G0 – working state) |
| Sleep (ACPI G1–sleeping state) | More than four seconds | Power-off (ACPI G2/S5 – Soft off) |

| For information about | Refer to |
|---|---|
| The VC820 board's compliance level with ACPI | Section 1.3, page 16 |

#### 1.10.1.2.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 8 lists the power states supported by the VC820 board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

**Table 8. Power States and Targeted System Power**

| Global States | Sleeping States | CPU States | Device States | Targeted System Power* |
|---|---|---|---|---|
| G0 – working state | S0 – working | C0 – working | D0 – working state | Full power > 60 W |
| G1 – sleeping state | S1 – CPU stopped | C1 – stop grant | D1, D2, D3 – device specification specific. | 5 W < power < 30 W |
| G1 – sleeping state | S3 – Suspend to RAM. Context saved to RAM. | No power | D3 – no power except for wake up logic. | Power < 5 W ** |
| G2/S5 | S5 – Soft off. Context not saved. Cold boot is required. | No power | D3 – no power except for wake up logic. | Power < 5 W ** |
| G3 – mechanical off.<br>AC power is disconnected from the computer. | No power to the system. | No power | D3 – no power for wake up logic, except when provided by battery or external source. | No power to the system so that service can be performed. |

* Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.

** Dependent on the standby power consumption of wake-up devices used in the system.

#### 1.10.1.2.2 Wake Up Devices and Events

Table 9 lists the devices or specific events that can wake the computer from specific states.

**Table 9. Wake Up Devices and Events**

| These devices/events can wake up the computer… | …from this state |
|---|---|
| Power switch | S1, S3, S5 |
| RTC alarm | S1, S3, S5 |
| PME# (including PCI 2.2 compliant add-in boards) | S1, S3, S5* |
| LAN (through Wake on LAN technology connector) | S5* |
| Modem (through COM port connector) | S1, S3 |
| IR command | S1, S3 |
| USB | S1, S3 |
| PS/2 keyboard | S1, S3 |

* S5 with jumper J4A2 pins 1 and 2 connected, see Table 47)

#### 1.10.1.2.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure VC820 board devices that do not have other hardware standards for enumeration and configuration. PCI devices on the VC820 board, for example, are not enumerated by ACPI.

### 1.10.2 Hardware Support

**⚠ CAUTION**

*If the Wake on LAN, Wake from USB and Instantly Available technology features are used, ensure that the power supply provides adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported. Refer to Section 2.11.3 on page 75 for additional information.*

The VC820 board provides several hardware features that support power management, including:

- Power connector
- Fan connectors
- Wake on LAN technology
- Instantly Available technology
- Wake on Ring
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# wakeup support

Both Wake on LAN technology and Instantly Available technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Wake on Ring and Resume on Ring enable telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the power management mode being used (APM or ACPI).

**NOTE**

*The use of Wake on Ring, Wake from USB, and Resume on Ring technologies from an ACPI state requires an operating system that provides full ACPI support.*

### 1.10.2.1 Power Connector

When used with an ATX-compliant power supply that supports remote power-on/ -off, the VC820 board can turn off the system power through software control. To enable soft-off control in software, power management must be enabled in the BIOS Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

| For information about | Refer to |
|---|---|
| The location of the power connector | Figure 11, page 60 |
| The signal names of the power connector | Table 35, page 61 |
| The ATX specification | Section 1.3, page 16 |

### 1.10.2.2 Fan Connectors

The VC820 board has three fan connectors. The functions of these connectors are described in Table 10.

**Table 10. Fan Connector Descriptions**

| Connector | Function |
|---|---|
| System fan (Fan 1) | Provides +12 V DC for a system or chassis fan. The fan voltage can be switched on or off, depending on the power management state of the computer. A tachometer feedback connection is also provided. |
| Power supply fan control (Fan 2) | Provides +12 V DC for a system or chassis fan. The fan voltage can be switched on or off, depending on the power management state of the computer. A tachometer feedback connection is also provided. |
| Processor fan (Fan 3) | Provides +12 V DC for a processor fan or active fan heatsink |

| For information about | Refer to |
|---|---|
| The location of the fan connectors | Figure 11, page 60 |
| The signal names of the fan connectors | Section 2.8.2.3, page 60 |

### 1.10.2.3 Wake on LAN Technology

**CAUTION**

*For Wake on LAN technology, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Wake on LAN technology can damage the power supply. Refer to Section 2.11.3 on page 75 for additional information.*

Wake on LAN technology enables remote wakeup of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet† frame, the LAN subsystem asserts a wakeup signal that powers up the computer. Depending on the LAN implementation, the VC820 board supports Wake on LAN technology in one of two ways:

- Through the Wake on LAN technology connector (APM or ACPI S5 only)
- Through the PCI bus PME# signal (for PCI 2.2 compliant LAN designs)

The Wake on LAN technology connector can be used with PCI bus network adapters that have a remote wake up connector, as shown in Figure 5. Network adapters that are PCI 2.2 compliant assert the wakeup signal through the PCI bus signal PME# (pin A19 on the PCI bus connectors).

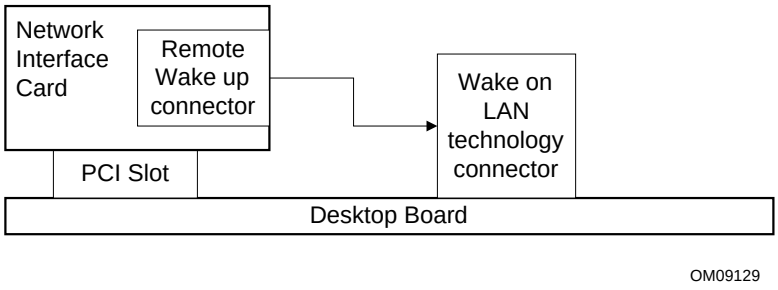



**Figure 5. Using the Wake on LAN Technology Connector**

| For information about | Refer to |
|---|---|
| The location of the Wake on LAN technology connector | Figure 11, page 60 |
| The signal names of the Wake on LAN technology connector | Table 37, page 62 |

### 1.10.2.4 Instantly Available Technology

**CAUTION**

*For Instantly Available Technology, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available technology can damage the power supply. Refer to Section 2.11.3 on page 75 for additional information.*

Instantly Available technology enables the VC820 board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, the fans are off, and the front panel LED is amber if dual-color, or off if single-color.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 9 on page 37 lists the devices and events that can wake the computer from the S3 state.

The VC820 board supports the *PCI Bus Power Management Interface Specification*. For information on the versions of this specification, see Section 1.3. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available technology requires operating system support and PCI 2.2 compliant add-in boards and drivers.

The standby power indicator LED (located between the AGP universal connector and the RIMM Bank 0 connector) provides an indication that power is still present to the RIMM modules and PCI bus connectors, even when the computer appears to be off. Figure 6 shows the location of the standby power indicator LED.

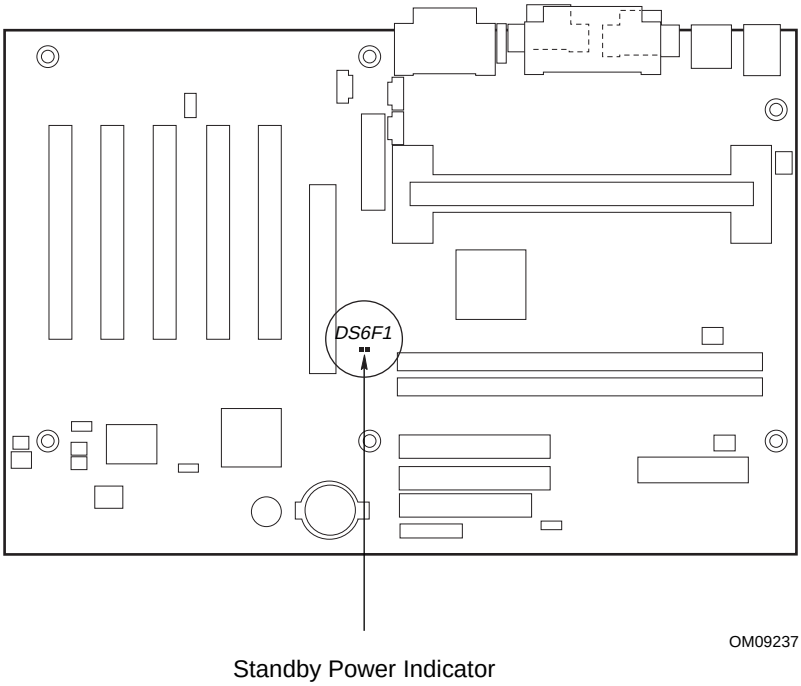



**Figure 6. Location of Standby Power Indicator LED**

### 1.10.2.5 Wake on Ring

The operation of Wake on Ring can be summarized as follows:

- Powers up the computer from the APM soft-off mode.
- Requires two calls to access the computer:
  - First call restores the computer
  - Second call enables access (when supporting software is installed)
- Detects incoming call differently for external as opposed to internal modems:
  - For external modems, VC820 board hardware monitors the ring indicate (RI) input of serial port A (serial port B does not support this feature)
  - For internal modems that do not support PME#, a cable must be routed from the modem to the Wake on Ring connector

| For information about | Refer to |
|---|---|
| The location of the Wake on Ring connector | Figure 11, page 62 |
| The signal names of the Wake on Ring connector | Table 38, page 61 |

### 1.10.2.6 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from either the APM sleep mode or the ACPI S1 state
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems; does not use the Wake on Ring connector
- Requires modem interrupt be unmasked for correct operation

### 1.10.2.7 Wake from USB

USB bus activity wakes the computer from an ACPI S1 or S3 state.

**NOTE**

*Wake from USB requires the use of a USB peripheral that supports Wake from USB.*

### 1.10.2.8 Wake from PS/2 Keyboard

PS/2 keyboard activity wakes the computer from ACPI S1 or S3 states.

### 1.10.2.9 PME# Wakeup Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1 or S3 state.

# 2 Technical Reference

## What This Chapter Contains



## 2.1 Introduction

Sections 2.2 - 2.6 contain several standalone tables. Table 11 describes the System Memory Map, Table 12 shows the I/O Map, Table 13 lists the DMA Channels, Table 14 defines the PCI Configuration Space Map, and Table 15 describes the Interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

## 2.2 Memory Map

**Table 11. System Memory Map**

| Address Range (decimal) | Address Range (hex) | Size | Description |
|---|---|---|---|
| 1024 K - 524288 K | 100000 - 1FFFFFFF | 511 MB | Extended memory |
| 960 K - 1024 K | F0000 - FFFFF | 64 KB | Runtime BIOS |
| 896 K - 960 K | E0000 - EFFFF | 64 KB | Reserved |
| 800 K - 896 K | C8000 - DFFFF | 96 KB | Available high DOS memory |
| 640 K - 800 K | A0000 - C7FFF | 160 KB | Video memory and BIOS |
| 639 K - 640 K | 9FC00 - 9FFFF | 1 KB | Extended BIOS data (movable by memory manager software) |
| 512 K - 639 K | 80000 - 9FBFF | 127 KB | Extended conventional memory |
| 0 K - 512 K | 00000 - 7FFFF | 512 K | Conventional memory |

# 2.3 I/O Map

**Table 12. I/O Map**

| Address (hex) | Size | Description |
|---|---|---|
| 0000 - 000F | 16 bytes | DMA controller |
| 0020 - 0021 | 2 bytes | Programmable Interrupt Control (PIC) |
| 0040 - 0043 | 4 bytes | System timer |
| 0060 | 1 byte | Keyboard controller byte—reset IRQ |
| 0061 | 1 byte | System speaker |
| 0064 | 1 byte | Keyboard controller, CMD/STAT byte |
| 0070 - 0071 | 2 bytes | System CMOS/Real Time Clock |
| 0072 - 0073 | 2 bytes | System CMOS |
| 0080 - 008F | 16 bytes | DMA controller |
| 0092 | 1 byte | Fast A20 and PIC |
| 00A0 - 00A1 | 2 bytes | PIC |
| 00B2 - 00B3 | 2 bytes | APM control |
| 00C0 - 00DF | 32 bytes | DMA |
| 00F0 | 1 byte | Numeric data processor |
| 0170 - 0177 | 8 bytes | Secondary IDE channel |
| 01F0 - 01F7 | 8 bytes | Primary IDE channel |
| One of these ranges:<br>0200 - 0207<br>0208 - 020F<br>0210 - 0217<br>0218 - 021F | Can vary from 1 byte to 8 bytes | Audio/game port |
| One of these ranges: | | Audio (Sound Blaster Pro-compatible) |
| 0220 - 022F | 16 bytes | |
| 0240 - 024F | 16 bytes | |
| 0228 - 022F* | 8 bytes | LPT3 |
| 0278 - 027F* | 8 bytes | LPT2 |
| 02E8 - 02EF* | 8 bytes | COM4/video (8514A) |
| 02F8 - 02FF* | 8 bytes | COM2 |
| One of these ranges:<br>0320 - 0327<br>0330 - 0337<br>0340 - 0347<br>0350 - 0357 | 8 bytes | MPU-401 (MIDI) |
| 0376 | 1 byte | Secondary IDE channel command port |
| 0377, bits 6:0 | 7 bits | Secondary IDE channel status port |
| 0378 - 037F | 8 bytes | LPT1 |
| 0388- 038B | 6 bytes | AdLib† (FM synthesizer) |
| 03B0 - 03BB | 12 bytes | Intel 82820 - Memory Controller Hub (MCH) |
| 03C0 - 03DF | 32 bytes | Intel 82820 - Memory Controller Hub (MCH) |
| 03E8 - 03EF | 8 bytes | COM3 |

continued

**Table 12. I/O Map** (continued)

| Address (hex) | Size | Description |
|---|---|---|
| 03F0 - 03F5 | 6 bytes | Diskette channel 1 |
| 03F6 | 1 byte | Primary IDE channel command port |
| 03F8 - 03FF | 8 bytes | COM1 |
| 04D0 - 04D1 | 2 bytes | Edge/level triggered PIC |
| One of these ranges:<br>0530 - 0537<br>0E80 - 0E87<br>0F40 - 0F47 | 8 bytes | Windows Sound System |
| LPTn + 400h | 8 bytes | ECP port, LPTn base address + 400h |
| 0CF8 - 0CFB** | 4 bytes | PCI configuration address register |
| 0CF9*** | 1 byte | Turbo and reset control register |
| 0CFC - 0CFF | 4 bytes | PCI configuration data register |
| FFA0 - FFA7 | 8 bytes | Primary bus master IDE registers |
| FFA8 - FFAF | 8 bytes | Secondary bus master IDE registers |
| 96 contiguous bytes starting on a 128-byte divisible boundary | | ICH (ACPI + TCO) |
| 64 contiguous bytes starting on a 64-byte divisible boundary | | VC820 board resource |
| 64 contiguous bytes starting on a 64-byte divisible boundary | | ICH Audio Bus Master |
| 256 contiguous bytes starting on a 256 byte divisible boundary | | ICH Audio Mixer |
| 256 contiguous bytes starting on a 256 byte divisible boundary | | ICH Modem Mixer |
| 32 contiguous bytes starting on a 32-byte divisible boundary | | ICH (USB) |
| 16 contiguous bytes starting on a 16-byte divisible boundary | | ICH (SMBus) |
| 4096 contiguous bytes starting on a 4096-byte divisible boundary | | Intel 82801AA PCI bridge |

* Default, but can be changed to another address range.

** Dword access only

*** Byte access only

## NOTE

*Some additional I/O addresses are not available due to ICH address aliassing. For information about the ICH addressing, refer to Section 1.2 on page 16.*

## 2.4 DMA Channels

**Table 13. DMA Channels**

| DMA Channel Number | Data Width | System Resource |
|---|---|---|
| 0 | 8- or 16-bits | Audio |
| 1 | 8- or 16-bits | Audio / parallel port |
| 2 | 8- or 16-bits | Diskette Drive |
| 3 | 8- or 16-bits | Parallel port (for ECP or EPP) / audio |
| 4 | 8- or 16-bits | DMA controller |
| 5 | 16-bits | Open |
| 6 | 16-bits | Open |
| 7 | 16-bits | Open |

## 2.5 PCI Configuration Space Map

**Table 14. PCI Configuration Space Map**

| Bus Number (hex) | Device Number (hex) | Function Number (hex) | Description |
|---|---|---|---|
| 00 | 00 | 00 | Memory controller (of Intel 82820 component) |
| 00 | 01 | 00 | PCI to AGP bridge |
| 00 | 1E | 00 | Link to PCI bridge |
| 00 | 1F | 00 | PCI-to-LPC bridge |
| 00 | 1F | 01 | IDE controller |
| 00 | 1F | 02 | USB controller |
| 00 | 1F | 03 | SMBus controller |
| 00 | 1F | 04 | Reserved |
| 00 | 1F | 05 | AC ’97 audio controller |
| 00 | 1F | 06 | AC ’97 modem controller |
| 01 | 00 | 00 | AGP connector |
| 02 | 07 | 00 | PCI accelerated audio (ES1373) |
| 02 | 08 | 00 | PCI slot 1 |
| 02 | 09 | 00 | PCI slot 2 |
| 02 | 0A | 00 | PCI slot 3 |
| 02 | 0B | 00 | PCI slot 4 |
| 02 | 0C | 00 | PCI slot 5 |

# 2.6 Interrupts

**Table 15. Interrupts**

| IRQ | System Resource |
|---|---|
| NMI | I/O channel check |
| 0 | Reserved, interval timer |
| 1 | Reserved, keyboard buffer full |
| 2 | Reserved, cascade interrupt from slave PIC |
| 3 | COM2 (if enabled, else user available) |
| 4 | COM1 (if enabled, else user available) |
| 5 | LPT2 (Plug and Play option) / Audio / User available |
| 6 | Diskette drive |
| 7 | LPT1 (if enabled, else user available) |
| 8 | Real-time clock |
| 9 | Reserved for ICH system management bus |
| 10 | User available |
| 11 | User available |
| 12 | Onboard mouse port (if present, else user available) |
| 13 | Reserved, math coprocessor |
| 14 | Primary IDE (if present, else user available) |
| 15 | Secondary IDE (if present, else user available) |

# 2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification defines how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in board.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in boards that require only one interrupt are in this category. For almost all boards that require more than one interrupt, the first interrupt on the board is also classified as INTA.
- INTB: Generally, the second interrupt on add-in boards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in boards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH PCI-to-LPC bridge has four programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in board connect to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are electrically tied together on the VC820 board and therefore share the same interrupt.

For example, using Table 16 as a reference, assume an add-in board using INTA is plugged into PCI Bus Connector 4. In PCI Bus Connector 4, INTA is connected to PIRQD. Since PIRQD is already connected to PCI Audio and the ICH USB Controller, the add-in board now shares interrupts with these onboard interrupt sources.

Table 16 lists the PIRQ signals used on the VC820 board shows how the signals are connected to the PCI bus connectors and to the onboard PCI interrupt sources.

**Table 16. PCI Interrupt Routing Map**

| PCI Interrupt Source | ICH PIRQ Signal Name | | | |
|---|---|---|---|---|
| | **PIRQA** | **PIRQB** | **PIRQC** | **PIRQD** |
| AGP Connector | INTA | INTB | | |
| ICH Audio Controller | | INTB | | |
| ICH Modem Controller | | INTB | | |
| ICH USB Controller | | | | INTD |
| PCI Audio | | | | INTD |
| PCI Bus Connector 1 (J4E1) | INTA | INTB | INTC | INTD |
| PCI Bus Connector 2 (J4D1) | INTD | INTA | INTB | INTC |
| PCI Bus Connector 3 (J4C1) | INTC | INTD | INTA | INTB |
| PCI Bus Connector 4 (J4B1) | INTB | INTC | INTD | INTA |
| PCI Bus Connector 5 (J4A1) | INTC | INTD | INTA | INTB |

## NOTE

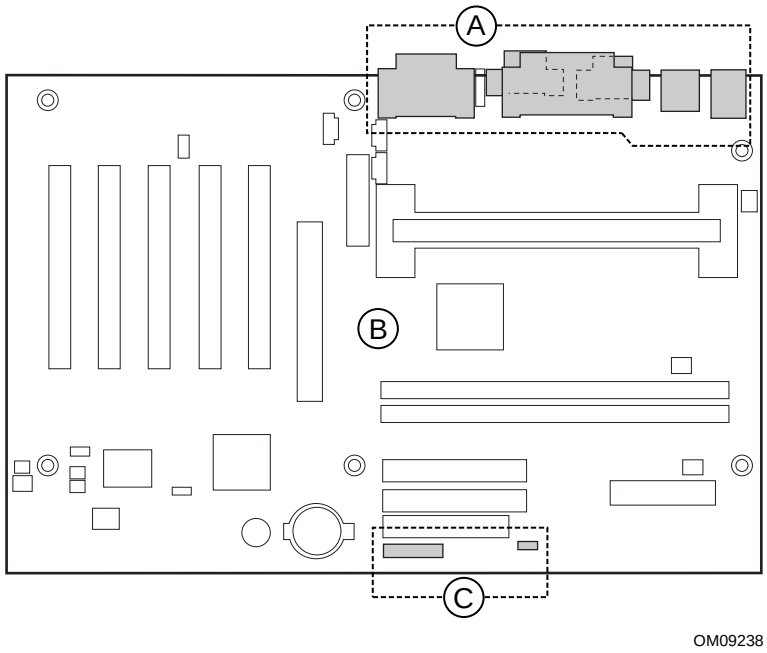
*The ICH can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 10, 11, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.*

# 2.8 Connectors

**CAUTION**

*Only the back panel connectors of this VC820 board have overcurrent protection. The internal VC820 board connectors are not overcurrent protected, and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.*

This section describes the VC820 board's connectors. The connectors can be divided into three groups, as shown in Figure 7.




**A. Back panel connectors (see page 50)**

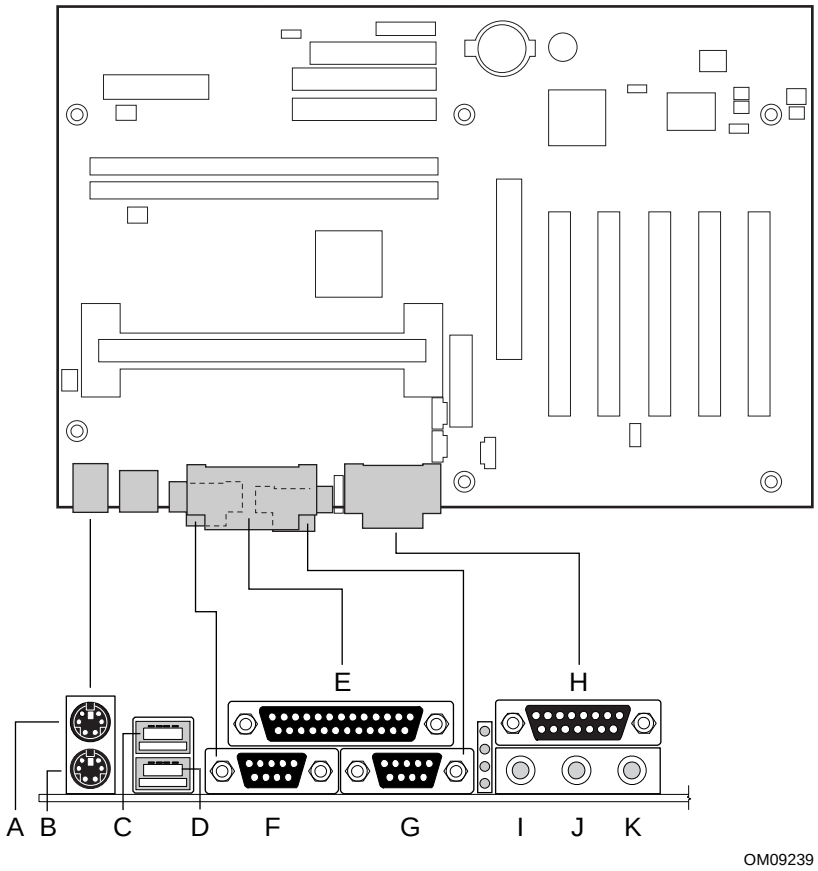
**B. Midboard connectors (see page 54)**

**C. Front panel connectors (see page 67)**

**Figure 7. Connector Groups**

## 2.8.1 Back Panel Connectors

Figure 8 shows the location of the back panel connectors. The back panel connectors are color-coded in compliance with PC 99 recommendations. The figure legend below lists the colors used.




| Item | Description | Color | For more information see: |
|---|---|---|---|
| A | PS/2 mouse port | Green | Table 17 |
| B | PS/2 keyboard port | Purple | Table 17 |
| C | USB port 0 | Black | Table 18 |
| D | USB port 1 | Black | Table 18 |
| E | Parallel port | Burgundy | Table 19 |
| F | Serial port A | Teal | Table 20 |
| G | Serial port B | Teal | Table 20 |
| H | MIDI/Game port | Gold | Table 21 |
| I | Audio line out | Lime green | Table 22 |
| J | Audio line in | Light blue | Table 23 |
| K | Mic in | Pink | Table 24 |

**Figure 8. Back Panel Connectors**

## NOTE

*The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.*

**Table 17. PS/2 Keyboard/Mouse Connectors**

| Pin | Signal Name |
|---|---|
| 1 | Data |
| 2 | Not connected |
| 3 | Ground |
| 4 | Fused +5 V |
| 5 | Clock |
| 6 | Not connected |

**Table 18. USB Connectors**

| Pin | Signal Name |
|---|---|
| 1 | +5 V (fused) |
| 2 | USBP0# [USBP1#] |
| 3 | USBP0 [USBP1] |
| 4 | Ground |

Signal names in brackets ([ ]) are for USB port 1.

**Table 19. Parallel Port Connector**

| Pin | Standard Signal Name | ECP Signal Name | EPP Signal Name |
|---|---|---|---|
| 1 | STROBE# | STROBE# | WRITE# |
| 2 | PD0 | PD0 | PD0 |
| 3 | PD1 | PD1 | PD1 |
| 4 | PD2 | PD2 | PD2 |
| 5 | PD3 | PD3 | PD3 |
| 6 | PD4 | PD4 | PD4 |
| 7 | PD5 | PD5 | PD5 |
| 8 | PD6 | PD6 | PD6 |
| 9 | PD7 | PD7 | PD7 |
| 10 | ACK# | ACK# | INTR |
| 11 | BUSY | BUSY#, PERIPHACK | WAIT# |
| 12 | PERROR | PE, ACKREVERSE# | PE |
| 13 | SELECT | SELECT | SELECT |
| 14 | AUDOFD# | AUDOFD#, HOSTACK | DATASTB# |
| 15 | FAULT# | FAULT#, PERIPHREQST# | FAULT# |
| 16 | INIT# | INIT#, REVERSERQST# | RESET# |
| 17 | SLCTIN# | SLCTIN# | ADDRSTB# |
| 18 - 25 | GND | GND | GND |

**Table 20. Serial Port Connectors**

| Pin | Signal Name |
|---|---|
| 1 | DCD (Data Carrier Detect) |
| 2 | SIN# (Serial Data In) |
| 3 | SOUT# (Serial Data Out) |
| 4 | DTR (Data Terminal Ready) |
| 5 | Ground |
| 6 | DSR (Data Set Ready) |
| 7 | RTS (Request to Send) |
| 8 | CTS (Clear to Send) |
| 9 | RI (Ring Indicator) |

**Table 21. MIDI/Game Port Connector**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | +5 V (fused) | 9 | +5 V (fused) |
| 2 | JOY4 | 10 | JOY6 |
| 3 | JOYTIME0 | 11 | JOYTIME2 |
| 4 | Ground | 12 | MIDI-OUT |
| 5 | Ground | 13 | JOYTIME3 |
| 6 | JOYTIME1 | 14 | JOY7 |
| 7 | JOY5 | 15 | MIDI-IN |
| 8 | +5 V (fused) | | |

**Table 22. Audio Line Out Connector**

| Pin | Signal Name |
|---|---|
| Tip | Audio left out |
| Ring | Audio right out |
| Sleeve | Ground |

**Table 23. Audio Line In Connector**

| Pin | Signal Name |
|---|---|
| Tip | Audio left in |
| Ring | Audio right in |
| Sleeve | Ground |

**Table 24. Mic In Connector**

| Pin | Signal Name |
|---|---|
| Tip | Mono in |
| Ring | Mic bias voltage |
| Sleeve | Ground |

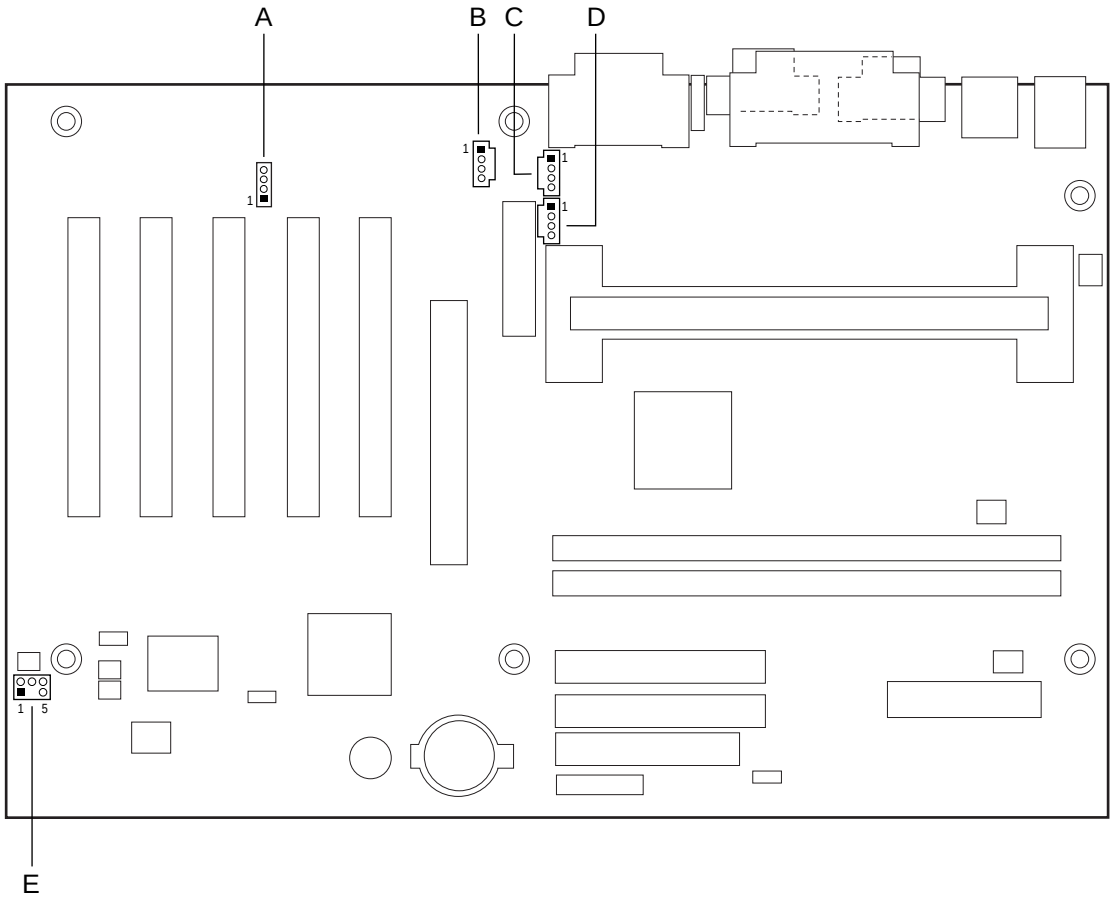
## 2.8.2 Midboard Connectors

The midboard connectors are divided into the following functional groups:

- Audio (see page 55)
  - CD-ROM (legacy style 2 mm connector)
  - AMR (Audio/Modem Riser)
  - ATAPI CD-ROM
  - Telephony
  - Auxiliary line in
  - PC/PCI
- Peripheral interfaces and indicators (see page 57)
  - SCSI LED
  - Secondary IDE
  - Primary IDE
  - Diskette drive
- Hardware control (see page 60)
  - Power supply fan control (Fan 2)
  - Processor fan (Fan 3)
  - Power
  - System fan (Fan 1)
  - Wake on LAN technology
  - Wake on Ring
  - Chassis intrusion
- Add-in boards (see page 63)
  - PCI bus (5)
  - AGP

### 2.8.2.1 Audio

Figure 9 shows the location of the audio connectors.




| Item | Description | Color | Style | Reference Designator |
|---|---|---|---|---|
| A | CD-ROM (see Table 25) | N/A | Legacy-style, 2 mm | J2C1 |
| B | CD-ROM (see Table 26) | Black | ATAPI | J1F1 |
| C | Telephony (see Table 27) | Green | ATAPI | J2F1 |
| D | Auxiliary line in (see Table 28) | Tan | ATAPI | J2F2 |
| E | PC/PCI (see Table 29) | N/A | 2x3 | J7A2 |

**Figure 9. Audio Connectors**

**Table 25. CD-ROM Legacy Style Connector (J2C1)**

| Pin | Signal Name |
|---|---|
| 1 | CD_Ground |
| 2 | CD_IN-Left |
| 3 | CD_Ground |
| 4 | CD_IN-Right |

**Table 26. ATAPI CD-ROM Connector (J1F1)**

| Pin | Signal Name |
|---|---|
| 1 | Left audio input from CD-ROM |
| 2 | CD audio differential ground |
| 3 | CD audio differential ground |
| 4 | Right audio input from CD-ROM |

**Table 27. Telephony Connector (J2F1)**

| Pin | Signal Name |
|---|---|
| 1 | Analog audio mono input |
| 2 | Ground |
| 3 | Ground |
| 4 | Analog audio mono output |

**Table 28. Auxiliary Line In Connector (J2F2)**

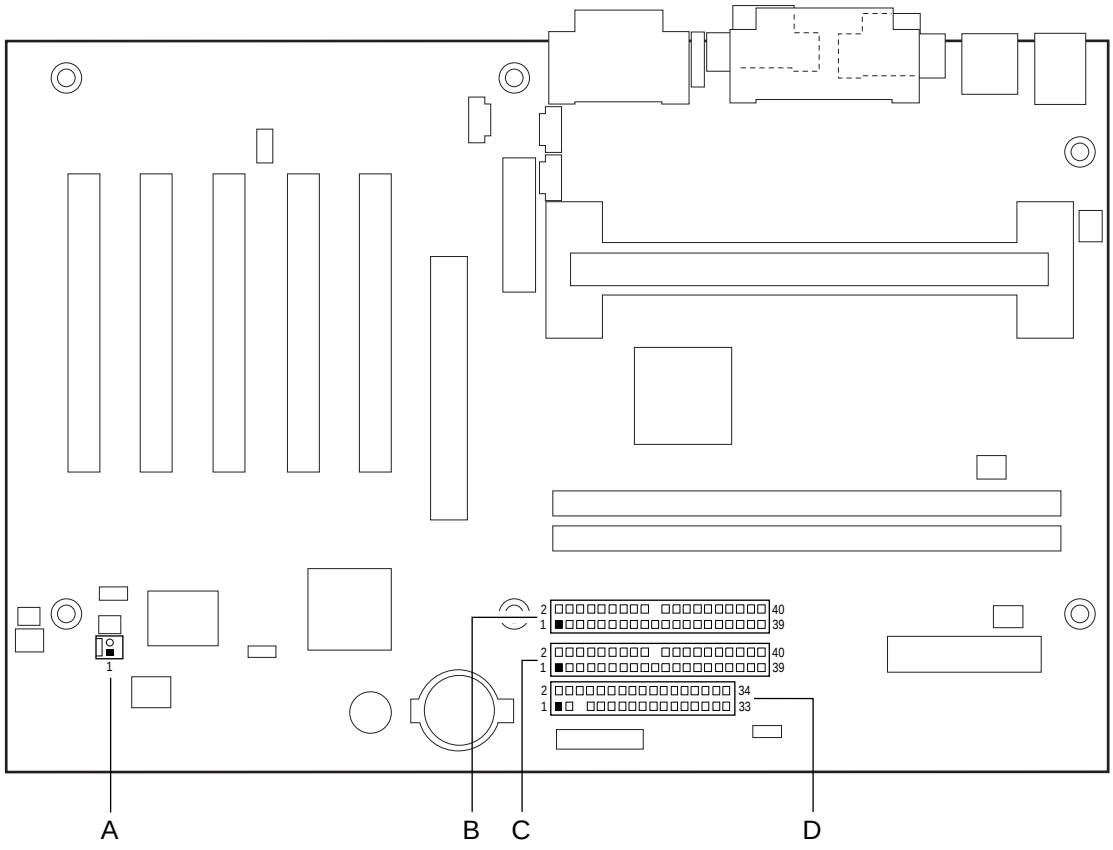
| Pin | Signal Name |
|---|---|
| 1 | Left auxiliary line in |
| 2 | Ground |
| 3 | Ground |
| 4 | Right auxiliary line in |

**Table 29. PC/PCI Connector (J7A2)**

| Pin | Signal Name |
|---|---|
| 1 | P_PCIGNTA In |
| 2 | Ground |
| 3 | No connection |
| 4 | P_PCIREQA Out |
| 5 | Ground |
| 6 | SER_IRQ Out |

### 2.8.2.2 Peripheral Interfaces and Indicators

Figure 10 shows the location of the peripheral interface and indicator connectors.




| Item | Description | Reference Designator |
|---|---|---|
| A | SCSI LED (see Table 30) | J7B3 |
| B | Secondary IDE (see Table 31) | J7H1 |
| C | Primary IDE (see Table 31) | J8H1 |
| D | Diskette drive (see Table 32) | J8G1 |

**Figure 10. Peripheral Interface and Indicator Connectors**

**Table 30. SCSI LED Connector (J7B3)**

| Pin | Signal Name |
|---|---|
| 1 | SCSI activity |
| 2 | Not connected |

**Table 31. PCI IDE Connectors (J8H1, Primary and J7H1, Secondary)**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | Reset IDE | 2 | Ground |
| 3 | Data 7 | 4 | Data 8 |
| 5 | Data 6 | 6 | Data 9 |
| 7 | Data 5 | 8 | Data 10 |
| 9 | Data 4 | 10 | Data 11 |
| 11 | Data 3 | 12 | Data 12 |
| 13 | Data 2 | 14 | Data 13 |
| 15 | Data 1 | 16 | Data 14 |
| 17 | Data 0 | 18 | Data 15 |
| 19 | Ground | 20 | Key |
| 21 | DDRQ0 [DDRQ1] | 22 | Ground |
| 23 | I/O Write# | 24 | Ground |
| 25 | I/O Read# | 26 | Ground |
| 27 | IOCHRDY | 28 | P_ALE (Cable Select Pullup) |
| 29 | DDACK0# [DDACK1#] | 30 | Ground |
| 31 | IRQ 14 [IRQ 15] | 32 | Reserved |
| 33 | DAG1 (Address 1) | 34 | GPIO_DMA66_Detect_Pri (GPIO_DMA66_Detect_Sec) |
| 35 | DAG0 (Address 0) | 36 | DAG2Address 2 |
| 37 | Chip Select 1P# [Chip Select 1S#] | 38 | Chip Select 3P# [Chip Select 3S#] |
| 39 | Activity# | 40 | Ground |

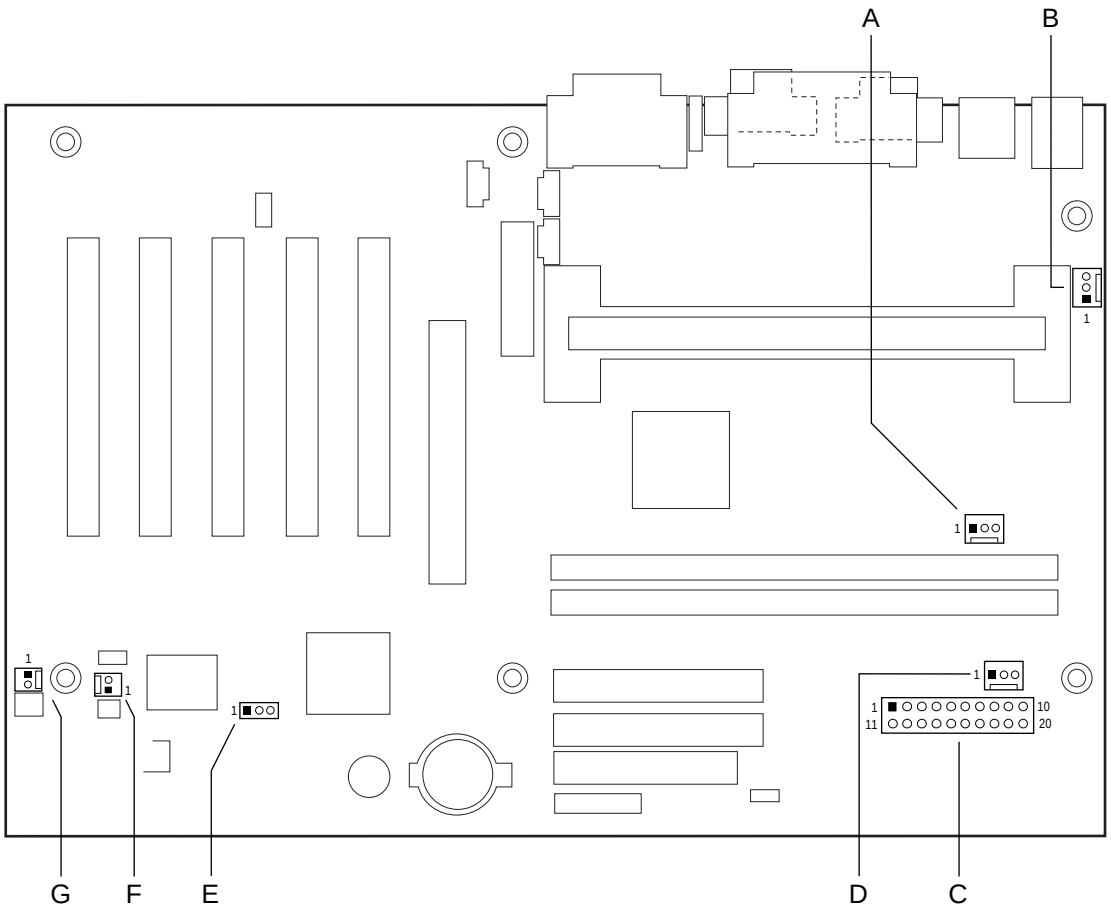
Note: Signal names in brackets ([ ]) are for the secondary IDE connector.

**Table 32. Diskette Drive Connector (J8G1)**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | Ground | 2 | DENSEL |
| 3 | Ground | 4 | Reserved |
| 5 | Key | 6 | FDEDIN |
| 7 | Ground | 8 | FDINDX# (Index) |
| 9 | Ground | 10 | FDM00# (Motor Enable A) |
| 11 | Ground | 12 | No connect |
| 13 | Ground | 14 | FDDS0# (Drive Select A) |
| 15 | Ground | 16 | No connect |
| 17 | No connect | 18 | FDDIR# (Stepper Motor Direction) |
| 19 | Ground | 20 | FDSTEP# (Step Pulse) |
| 21 | Ground | 22 | FDWD# (Write Data) |
| 23 | Ground | 24 | FDWE# (Write Enable) |
| 25 | Ground | 26 | FDTRK0# (Track 0) |
| 27 | No connect | 28 | FDWPD# (Write Protect) |
| 29 | Ground | 30 | FDRDATA# (Read Data) |
| 31 | Ground | 32 | FDHEAD# (Side 1 Select) |
| 33 | Ground | 34 | DSKCHG# (Diskette Change) |

### 2.8.2.3 Hardware Control and Power

Figure 11 shows the location of the hardware control and power connectors.




| Item | Description | Reference Designator |
|---|---|---|
| A | Power supply fan control (Fan 2) (see Table 33) | J5L1 |
| B | Processor fan (Fan 3) (see Table 34) | J2M1 |
| C | Power (see Table 35) | J7L2 |
| D | System fan (Fan 1) (see Table 36) | J7L1 |
| E | Wake on LAN technology (see Table 37) | J7C1 |
| F | Wake on Ring (see Table 38) | J7B2 |
| G | Chassis intrusion (see Table 39) | J7A1 |

**Figure 11. Hardware Control and Power Connectors**

| For information about | Refer to |
|---|---|
| The power connector | Section 1.10.2.1, page 38 |
| The functions of the fan connectors | Section 1.10.2.2, page 38 |
| Wake on LAN technology | Section 1.10.2.3, page 39 |
| Wake on Ring technology | Section 1.10.2.5, page 41 |

**Table 33. Power Supply Fan Control Connector (J5L1)**

| Pin | Signal Name |
|---|---|
| 1 | Ground |
| 2 | +12 V |
| 3 | FAN2_TACH |

**Table 34. Processor Fan Connector (J2M1)**

| Pin | Signal Name |
|---|---|
| 1 | Ground |
| 2 | +12 V |
| 3 | FAN3_CPU_HDR_GND_R |

**Table 35. Power Connector (J7L2)**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | +3.3 V | 11 | +3.3 V |
| 2 | +3.3 V | 12 | -12 V |
| 3 | Ground | 13 | Ground |
| 4 | +5 V | 14 | PS-ON# (power supply remote on/off) |
| 5 | Ground | 15 | Ground |
| 6 | +5 V | 16 | Ground |
| 7 | Ground | 17 | Ground |
| 8 | PWRGD (Power Good) | 18 | -5 V |
| 9 | +5 V (Standby) | 19 | +5 V |
| 10 | +12 V | 20 | +5 V |

**Table 36. System Fan Connector (J7L1)**

| Pin | Signal Name |
|---|---|
| 1 | Ground |
| 2 | +12 V |
| 3 | FAN1-TACH |

**Table 37. Wake on LAN Technology Connector (J7C1)**

| Pin | Signal Name |
|---|---|
| 1 | +5 VSB |
| 2 | Ground |
| 3 | WOL |

**Table 38. Wake on Ring Connector (J7B2)**

| Pin | Signal Name |
|---|---|
| 1 | Ground |
| 2 | RINGA# |

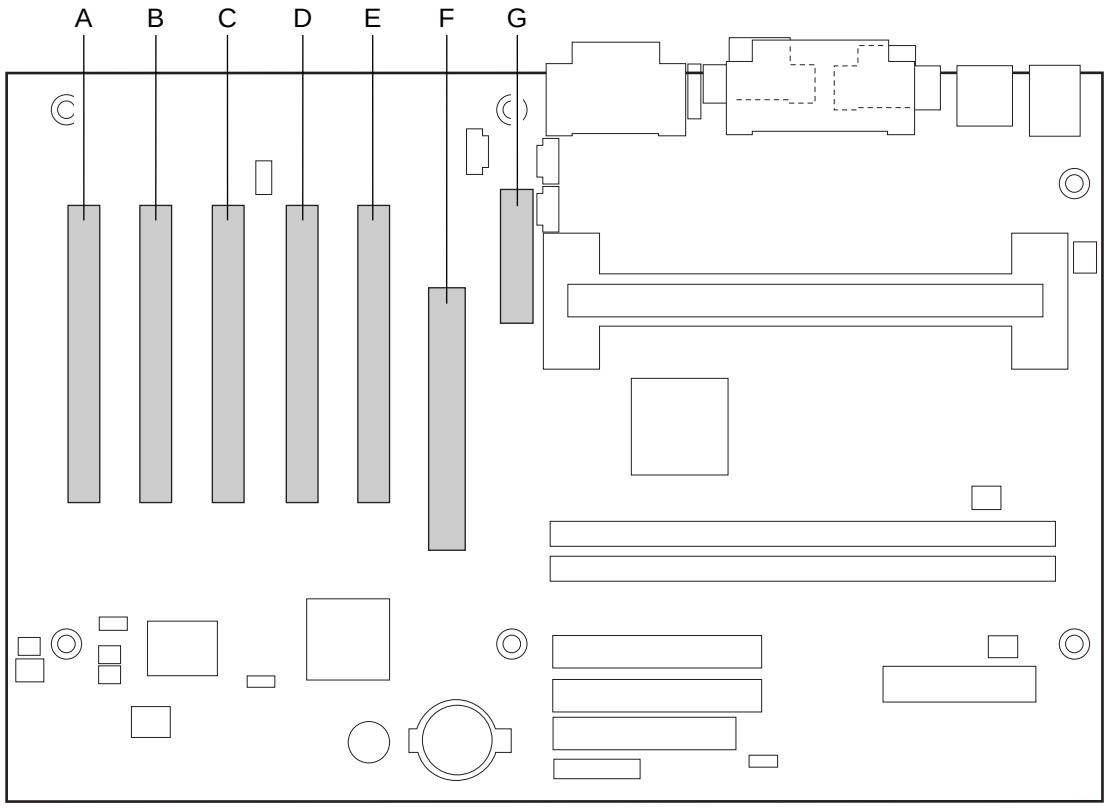
**Table 39. Chassis Intrusion Connector (J7A1)**

| Pin | Signal Name |
|---|---|
| 1 | INTRUDER# |
| 2 | Ground |

### 2.8.2.4 Add-In Boards

Figure 12 shows the location of the add-in board connectors. Note the following considerations for the PCI bus connectors:

- All of the PCI bus connectors are bus master capable.
- PCI bus connector 2 has SMBus signals routed to it. This enables PCI bus add-in boards with SMBus support to access sensor data on the VC820 board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40
  - The SMBus data line is connected to pin A41




| Item | Description | Reference Designator |
|---|---|---|
| A | PCI bus connector 5 (see Table 40) | J4A1 |
| B | PCI bus connector 4 (see Table 40) | J4B1 |
| C | PCI bus connector 3 (see Table 40) | J4C1 |
| D | PCI bus connector 2 (see Table 40) | J4D1 |
| E | PCI bus connector 1 (see Table 40) | J4E1 |
| F | AGP universal connector (see Table 41) | J5E1 |
| G | AMR (Audio/Modem Riser) connector (see Table 42) | J3F1 |

**Figure 12. Add-In Board Connectors**

**Table 40. PCI Bus Connectors (J4A1, J4B1, J4C1, J4D1, J4E1)**

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|---|---|---|---|
| A1 | Ground (TRST#)* | B1 | -12 V | A32 | AD16 | B32 | AD17 |
| A2 | +12 V | B2 | Ground (TCK)* | A33 | +3.3 V | B33 | C/BE2# |
| A3 | +5 V (TMS)* | B3 | Ground | A34 | FRAME# | B34 | Ground |
| A4 | +5 V (TDI)* | B4 | no connect (TDO)* | A35 | Ground | B35 | IRDY# |
| A5 | +5 V | B5 | +5 V | A36 | TRDY# | B36 | +3.3 V |
| A6 | INTA# | B6 | +5 V | A37 | Ground | B37 | DEVSEL# |
| A7 | INTC# | B7 | INTB# | A38 | STOP# | B38 | Ground |
| A8 | +5 V | B8 | INTD# | A39 | +3.3 V | B39 | LOCK# |
| A9 | Reserved | B9 | no connect (PRSNT1#)* | A40 | Reserved ** | B40 | PERR# |
| A10 | +5 V (I/O) | B10 | Reserved | A41 | Reserved *** | B41 | +3.3 V |
| A11 | Reserved | B11 | no connect (PRSNT2#)* | A42 | Ground | B42 | SERR# |
| A12 | Ground | B12 | Ground | A43 | PAR | B43 | +3.3 V |
| A13 | Ground | B13 | Ground | A44 | AD15 | B44 | C/BE1# |
| A14 | +3.3 V Aux | B14 | Reserved | A45 | +3.3 V | B45 | AD14 |
| A15 | RST# | B15 | Ground | A46 | AD13 | B46 | Ground |
| A16 | +5 V (I/O) | B16 | CLK | A47 | AD11 | B47 | AD12 |
| A17 | GNT# | B17 | Ground | A48 | Ground | B48 | AD10 |
| A18 | Ground | B18 | REQ# | A49 | AD09 | B49 | Ground |
| A19 | PME# | B19 | +5 V (I/O) | A50 | Key | B50 | Key |
| A20 | AD30 | B20 | AD31 | A51 | Key | B51 | Key |
| A21 | +3.3 V | B21 | AD29 | A52 | C/BE0# | B52 | AD08 |
| A22 | AD28 | B22 | Ground | A53 | +3.3 V | B53 | AD07 |
| A23 | AD26 | B23 | AD27 | A54 | AD06 | B54 | +3.3 V |
| A24 | Ground | B24 | AD25 | A55 | AD04 | B55 | AD05 |
| A25 | AD24 | B25 | +3.3 V | A56 | Ground | B56 | AD03 |
| A26 | IDSEL | B26 | C/BE3# | A57 | AD02 | B57 | Ground |
| A27 | +3.3 V | B27 | AD23 | A58 | AD00 | B58 | AD01 |
| A28 | AD22 | B28 | Ground | A59 | +5 V (I/O) | B59 | +5 V (I/O) |
| A29 | AD20 | B29 | AD21 | A60 | REQ64C# | B60 | ACK64C# |
| A30 | Ground | B30 | AD19 | A61 | +5 V | B61 | +5 V |
| A31 | AD18 | B31 | +3.3 V | A62 | +5 V | B62 | +5 V |

* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

** On PCI bus connector 2, this pin is connected to the SMBus clock line.

*** On PCI bus connector 2, this pin is connected to the SMBus data line.

**Table 41. AGP Bus Connector (J5E1)**

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|---|---|---|---|
| A1 | +12V | B1 | No Connect | A34 | Vcc3.3 | B34 | Vcc3.3 |
| A2 | TYPEDET# | B2 | Vcc | A35 | AD22 | B35 | AD21 |
| A3 | Reserved | B3 | Vcc | A36 | AD20 | B36 | AD19 |
| A4 | No Connect | B4 | No Connect | A37 | Ground | B37 | Ground |
| A5 | Ground | B5 | Ground | A38 | AD18 | B38 | AD17 |
| A6 | INTA# | B6 | INTB# | A39 | AD16 | B39 | C/BE2# |
| A7 | RST# | B7 | CLK | A40 | Vcc3.3 | B40 | Vcc3.3 |
| A8 | GNT1# | B8 | REQ# | A41 | FRAME# | B41 | IRDY# |
| A9 | Vcc3.3 | B9 | Vcc3.3 | A42 | Reserved | B42 | +3.3 V Aux |
| A10 | ST1 | B10 | ST0 | A43 | Ground | B43 | Ground |
| A11 | Reserved | B11 | ST2 | A44 | Reserved | B44 | Reserved |
| A12 | PIPE# | B12 | RBF# | A45 | Vcc3.3 | B45 | Vcc3.3 |
| A13 | Ground | B13 | Ground | A46 | TRDY# | B46 | DEVSEL# |
| A14 | WBF# | B14 | No Connect | A47 | STOP# | B47 | Vcc3.3 |
| A15 | SBA1 | B15 | SBA0 | A48 | PME# | B48 | PERR# |
| A16 | Vcc3.3 | B16 | Vcc3.3 | A49 | Ground | B49 | Ground |
| A17 | SBA3 | B17 | SBA2 | A50 | PAR | B50 | SERR# |
| A18 | SBSTB# | B18 | SB_STB | A51 | AD15 | B51 | C/BE1# |
| A19 | Ground | B19 | Ground | A52 | Vcc3.3 | B52 | Vcc3.3 |
| A20 | SBA5 | B20 | SBA4 | A53 | AD13 | B53 | AD14 |
| A21 | SBA7 | B21 | SBA6 | A54 | AD11 | B54 | AD12 |
| A22 | Key | B22 | Key | A55 | Ground | B55 | Ground |
| A23 | Key | B23 | Key | A56 | AD9 | B56 | AD10 |
| A24 | Key | B24 | +3.3 V Aux | A57 | C/BE0# | B57 | AD8 |
| A25 | Key | B25 | Key | A58 | Vcc3.3 | B58 | Vcc3.3 |
| A26 | AD30 | B26 | AD31 | A59 | AD_STB0# | B59 | AD_STB0 |
| A27 | AD28 | B27 | AD29 | A60 | AD6 | B60 | AD7 |
| A28 | Vcc3.3 | B28 | Vcc3.3 | A61 | Ground | B61 | Ground |
| A29 | AD26 | B29 | AD27 | A62 | AD4 | B62 | AD5 |
| A30 | AD24 | B30 | AD25 | A63 | AD2 | B63 | AD3 |
| A31 | Ground | B31 | Ground | A64 | Vcc3.3 | B64 | Vcc3.3 |
| A32 | AD_STB1# | B32 | AD_STB1 | A65 | AD0 | B65 | AD1 |
| A33 | C/BE3# | B33 | AD23 | A66 | VRREFG_C | B66 | VREFC_G |

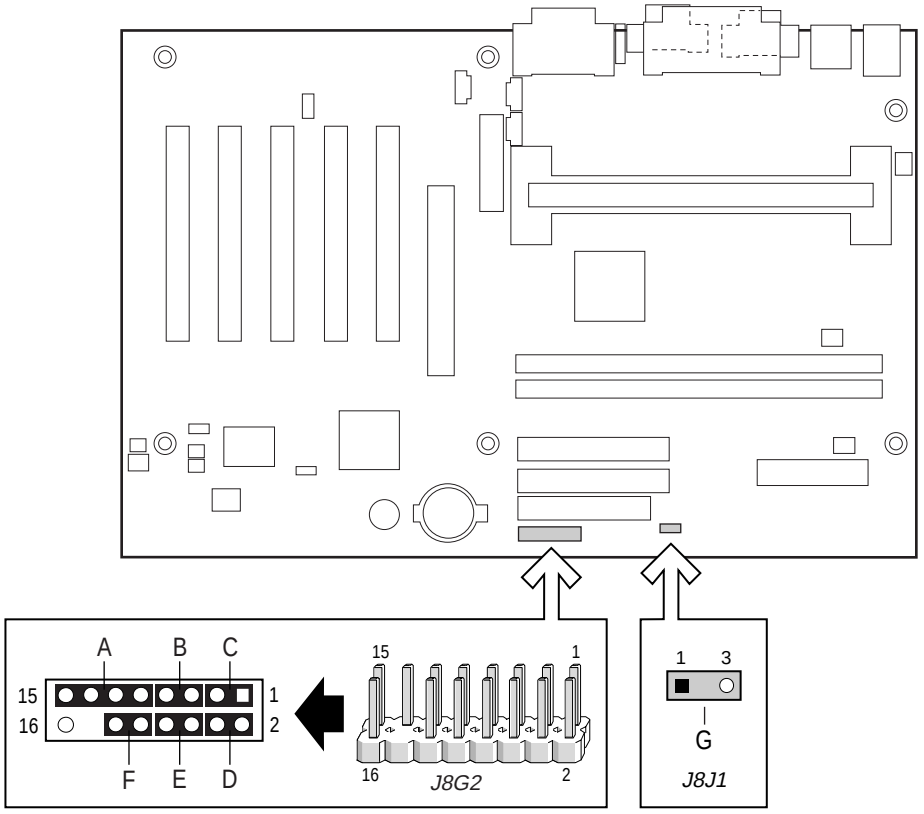
**Table 42. Audio/Modem Riser Connector (J3F1)**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| A1 | AUDIO_PWRDN | B1 | AUDIO_MUTE |
| A2 | MONO_PHONE | B2 | GND |
| A3 | RESERVED | B3 | MONO_OUT/PB_BEEP |
| A4 | RESERVED | B4 | RESERVED |
| A5 | RESERVED | B5 | RESERVED |
| A6 | GND | B6 | PRIMARY_DN |
| A7 | +5VDUAL/+5VVSB | B7 | -12V |
| A8 | USB_OC | B8 | GND |
| A9 | GND | B9 | +12V |
| A10 | USB+ | B10 | GND |
| A11 | USB- | B11 | +5VD |
| A12 | GND | B12 | GND |
| A13 | S/P_DIF_IN | B13 | RESERVED |
| A14 | GND | B14 | RESERVED |
| A15 | +3.3VDUAL/+3.3VSB | B15 | +3.3VD |
| A16 | GND | B16 | GND |
| A17 | AC97_SYNC | B17 | AC97_SDATA_IN0 |
| A18 | GND | B18 | AC97_RESET |
| A19 | AC97_SDATA_IN1 | B19 | AC97_SDATA_IN1 |
| A20 | GND | B20 | GND |
| A21 | AC97_SDATA_IN0 | B21 | AC97_SDATA_IN2 |
| A22 | GND | B22 | GND |
| A23 | AC97_BITCLK | B23 | AC97_MSTRCLK |

| For information about | Refer to |
|---|---|
| The Audio/Modem Riser | Section 1.8.2.5, page 32 |

## 2.8.3 Front Panel Connectors

Figure 13 shows the location of the front panel connectors.




| | Item | Pins | Description |
|---|---|---|---|
| Front Panel Connector (see Table 43) | A | 9, 11, 13, and 15 | Infrared port |
| | B | 5 and 7 | Reset switch |
| | C | 1 and 3 | Hard drive activity LED |
| | D | 2 and 4 | Power / Sleep / Message waiting LED |
| | E | 6 and 8 | Power switch |
| | F | 10 and 12 | No connect |
| Auxiliary Front Panel Power LED Connector (see Table 46) | G | 1 and 3 | Auxiliary Power LED connector (Pin 2 keyed) |

**Figure 13. Front Panel Connectors**

**Table 43. Front Panel Connector (J8G2)**

| Pin | Signal | In/Out | Description | Pin | Signal | In/Out | Description |
|---|---|---|---|---|---|---|---|
| 1 | HD_PWR | Out | Hard disk LED pullup (330 Ω) to +5 V | 2 | HDR_BLNK_ GRN | Out | Front panel green LED |
| 3 | HDA# | Out | Hard disk active LED | 4 | HDR_BLNK_ YEL | Out | Front panel yellow LED |
| 5 | GND | | Ground | 6 | FPBUT_IN | In | Power switch |
| 7 | FP_RESET# | In | Reset switch | 8 | GND | | Ground |
| 9 | +5 V | Out | IR Power | 10 | N/C | | |
| 11 | IRRX | In | IrDA serial input | 12 | GND | | Ground |
| 13 | GND | | Ground | 14 | (pin removed) | | Not connected |
| 15 | IRTX | Out | IrDA serial output | 16 | +5 V | Out | Power |

### 2.8.3.1 Infrared Port Connector

Serial Port B can be configured to support an IrDA module connected to pins 9, 11, 13, and 15.

| For information about | Refer to |
|---|---|
| Infrared support | Section 1.7.2, page 27 |
| Configuring serial port B for infrared applications | Section 4.4.3, page 100 |

### 2.8.3.2 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the VC820 board resets and runs POST.

### 2.8.3.3 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface. The LED will also show activity for devices connected to the SCSI hard drive activity LED connector.

| For information about | Refer to |
|---|---|
| The SCSI hard drive activity LED connector | Section 1.6.3.2, page 25 |

### 2.8.3.4 Power / Sleep / Message Waiting LED Connector

Pins 2 and 4 can be connected to a single- or dual-colored LED. Table 44 shows the possible states for a single-colored LED.

Table 45 shows the possible states for a dual-colored LED.

**Table 44. States for a Single-colored Power LED**

| LED State | Description |
|---|---|
| Off | Power off/sleeping |
| Steady Green | Running |
| Blinking Green | Running/message waiting |

**Table 45. States for a Dual-colored Power LED**

| LED State | Description |
|---|---|
| Off | Power off |
| Steady Green | Running |
| Blinking Green | Running/message waiting |
| Steady Yellow | Sleeping |
| Blinking Yellow | Sleeping/message waiting |

**NOTE**

*To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.*

### 2.8.3.5 Power Switch Connector

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the VC820 board.) At least two seconds must pass before the power supply will recognize another on/off signal.

### 2.8.3.6 Auxiliary Front Panel Power LED Connector

This connector duplicates the signals on pins 2 and 4 of the front panel connector.

**Table 46. Auxiliary Front Panel Power LED Connector (J8J1)**

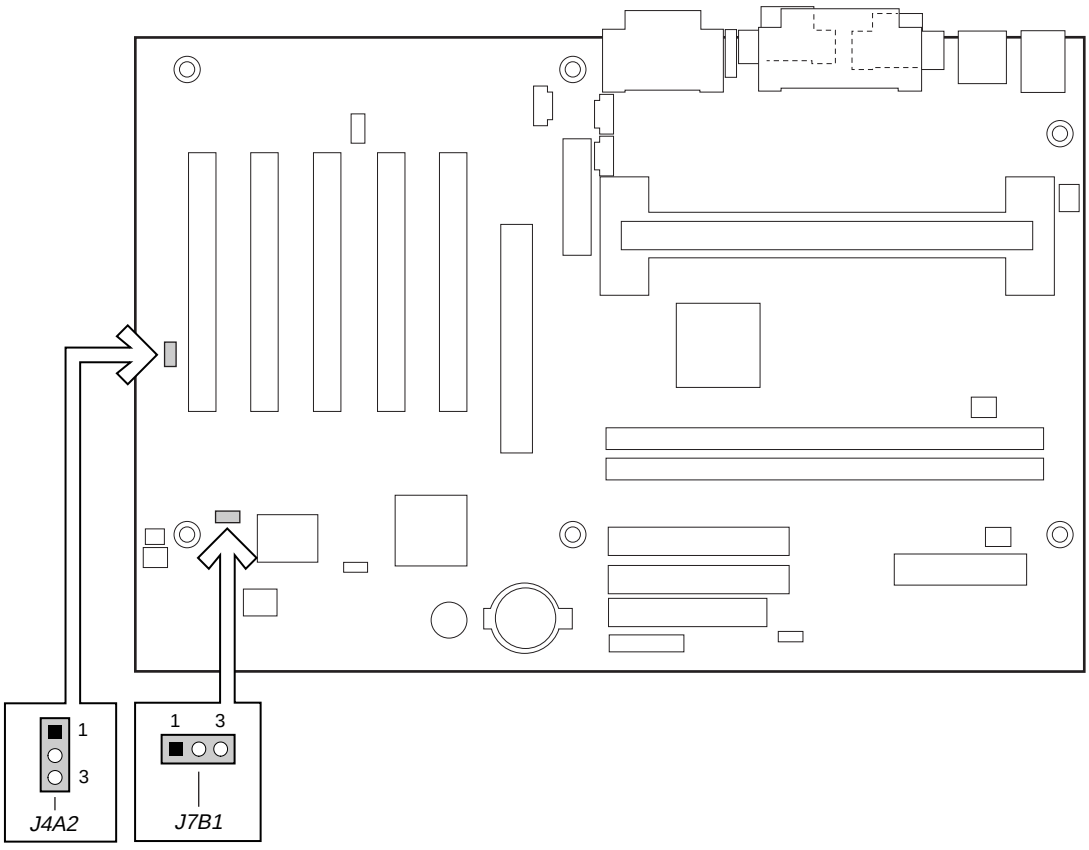
| Pin | Signal Name | In/Out | Description |
|---|---|---|---|
| 1 | HDR_BLNK_GRN | Out | Front panel green LED |
| 2 | No connect | | |
| 3 | HDR_BLNK_YEL | Out | Front panel yellow LED |

# 2.9 Jumper Blocks

**CAUTION**

*Do not move any jumper with the power ON. Always turn the power off and unplug the power cord from the computer before changing a jumper setting. Otherwise, damage to the VC820 board could occur.*

The VC820 board has two jumper blocks the locations of which are shown in Figure 14.




| Description | Reference Designator |
|---|---|
| S5 remote control jumper block | J4A2 |
| BIOS setup configuration jumper block | J7B1 |

**Figure 14. Location of the Jumper Blocks**

Table 47 describes jumper block J4A2 that provides user-control over system wake events. If the jumper is set to connect pins 1-2 (default), the system resumes from an S5 state when a PME# or Wake on LAN technology event is asserted. If the jumper is set to connect pins 2-3, the system will no longer resume from an S5 state. This feature is useful if, for example, the user does not wish their dial-up modem to wake their previously powered-off computer whenever the telephone rings. The jumper setting does not effect S3 resume events.

**Table 47. S5 Remote Control Jumper Settings (J4A2)**

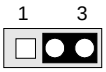
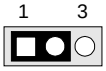
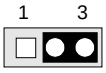
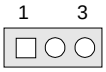
| Function/Mode | Jumper Setting | | Configuration |
|---|---|---|---|
| Enable S5 wake events. | 1-2 |  *(Default)* | System will resume from an S5 state when a PME# or Wake on LAN technology event is asserted. |
| Disable S5 wake events. | 2-3 |  | System will NOT resume from an S5 state when a PME# or Wake on LAN technology event is asserted. |

Table 48 describes the jumper settings for the three BIOS setup configuration modes: normal, configure, and recovery. This 3-pin jumper block determines the BIOS Setup program's mode.

**Table 48. BIOS Setup Configuration Jumper Settings (J7B1)**

| Function/Mode | Jumper Setting | | Configuration |
|---|---|---|---|
| Normal | 1-2 |  | The BIOS uses current configuration information and passwords for booting. |
| Configure | 2-3 |  | After the POST runs, Setup runs automatically. The maintenance menu is displayed. |
| Recovery | None |  | The BIOS attempts to recover the BIOS configuration. A recovery diskette is required. |

| For information about | Refer to |
|---|---|
| How to access the BIOS Setup program | Section 4.1, page 93 |
| The maintenance menu of the BIOS Setup program | Section 4.2, page 94 |
| BIOS recovery | Section 3.6, page 88 |

# 2.10 Mechanical Considerations

## 2.10.1 Form Factor

The VC820 board is designed to fit into an ATX-form-factor chassis. Figure 15 illustrates the mechanical form factor for the VC820 board. Dimensions are given in inches. The outer dimensions are 8.20 inches by 12.00 inches. Location of the I/O connectors and mounting holes are in compliance with the ATX specification (see Section 1.3).

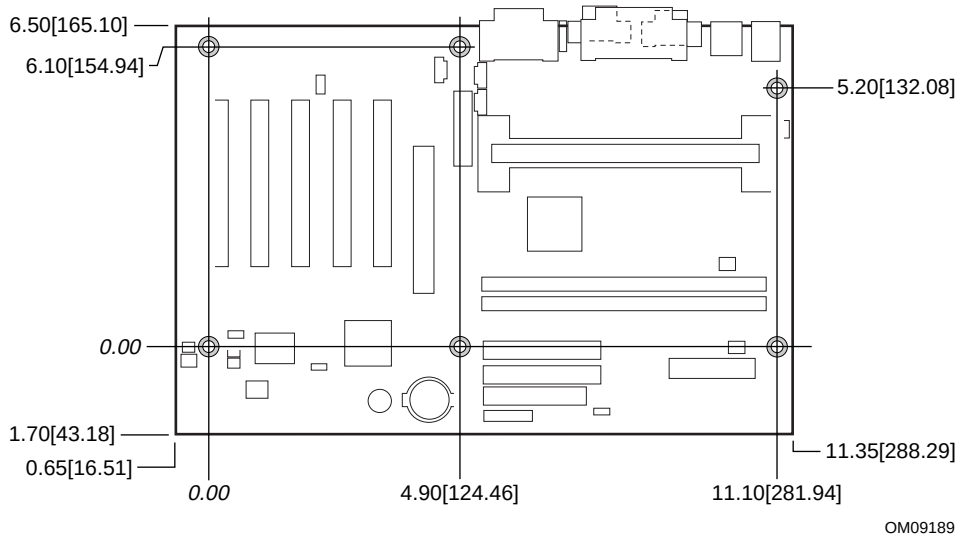



**Figure 15. VC820 Board Dimensions**

## 2.10.2 I/O Shield

The back panel I/O shield for the VC820 board must meet specific dimension and material requirements. Systems based on this VC820 board need the back panel I/O shield to pass certification testing. Figure 16 shows the critical dimensions of the I/O shield. Dimensions are given in inches. For dimensions given to two decimal places, (X.XX) the tolerance is ±0.02 inches. The figure also indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 1.3 for information about the ATX specification.

**NOTE**

*An I/O shield compliant with the ATX chassis specification 2.01 is available from Intel.*

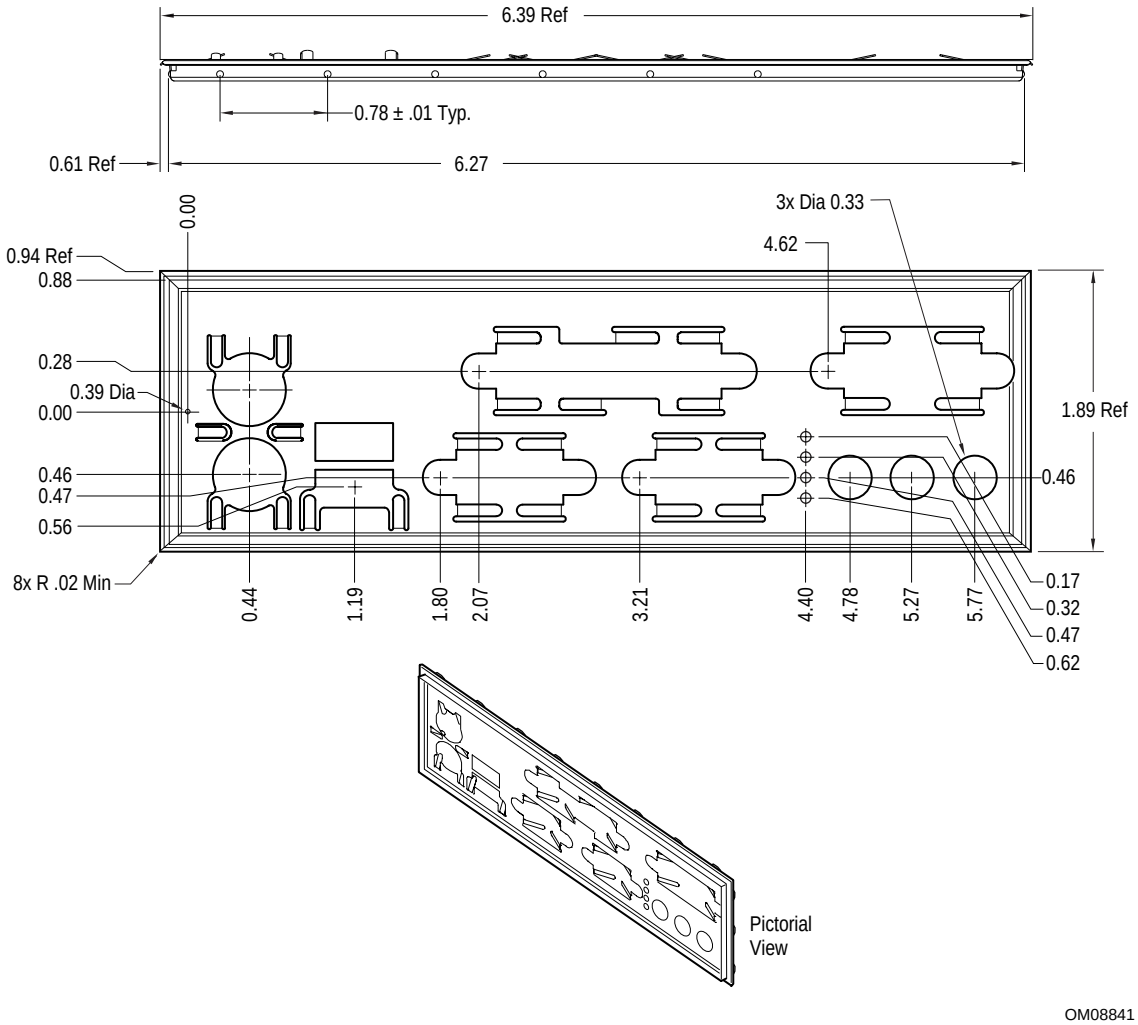



**Figure 16. I/O Shield Dimensions**

# 2.11 Electrical Considerations

## 2.11.1 Power Consumption

Table 49 lists typical power usage measurements for a desktop computer that contains the VC820 board and the following:

- 533 MHz Intel Pentium III processor with a 512 KB cache
- 128 MB RDRAM
- 3.5-inch diskette drive
- 1.6 GB IDE hard disk drive
- 32X IDE CD-ROM drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 98 desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with a typical 250 W power supply meeting ATX version 2.01 specifications, nominal input voltage and frequency, and using a true RMS wattmeter at the line input.

**NOTE**

*Actual system power consumption depends upon system configuration. The power supply should comply with the recommendations found in the ATX Form Factor Specification document (see Table 2 on page 16 for specification information).*

**Table 49. Typical Power Usage**

| Power Management Mode | Windows 98 APM Full on (idle) | Windows 98 APM Suspend | Windows 98 ACPI S0 Idle | Windows 98 ACPI S1 | Windows 98 ACPI S3 | Windows 98 ACPI S5 |
|---|---|---|---|---|---|---|
| **AC Watts** | 43.3 W | 29 W | 44 W | 27 W | 3 W | 2.8 W |

All measurements were made at nominal input voltage and frequency with a true RMS wattmeter connected to the power supply's line input.

Table 50 lists the maximum current required for each power supply voltage. Although not seen continuously, these peak values may occur during normal operation. Power supplies chosen for the VC820 board should be able to meet the maximum power supply current requirements, plus any additional system and add-in board requirements.

**Table 50. Maximum Power Supply Current Requirements**

| DC Voltage | +3.3 V | +5 V | +12 V | -12 V | +5 VSB |
|---|---|---|---|---|---|
| **Maximum Current** | 8.51 A | 11.2 A | 1.4 A | 0.05 A | 1.38 A |

## 2.11.2 Add-in Board Considerations

The VC820 board has seven slots for add-in boards: five PCI slots, one AGP slot, and one AMR (Audio/Modem Riser) slot. The maximum power used by any PCI slot (from all voltage sources) should not exceed 25 W. The total current load for all slots should not to exceed 14 A. Table 51 lists the maximum current load for PCI add-boards from all voltage sources.

**Table 51. Maximum PCI Add-in Board Current Load**

| Power Rail | +3.3 V | +5 V | +12 V | -12 V |
|---|---|---|---|---|
| Maximum Current | 7.6 A | 5.0 A | 500 mA | 100 mA |

## 2.11.3 Standby Current Requirements

### ⚠ CAUTION

*If the standby current necessary to support multiple wake events from the PCI and/or USB buses exceeds power supply capacity, the VC820 board may lose register settings stored in memory, etc. Calculate the standby current requirements using the steps described below.*

To support the Instantly Available (ACPI S3 sleep state) configuration as outlined in Table 52, power supplies used with the VC820 desktop board must provide enough standby current.

Approximate values can be determined by specifications such as PCI 2.2. Actual measured values may vary.

To estimate the amount of standby current required for a particular system configuration, standby current requirements of all installed components must be added to determine the total standby current requirement. Refer to the descriptions in Table 52 and review the following steps:

1. Note the total VC820 desktop board standby current requirement.
2. Add to that the total PS/2 port standby current requirement if a wake enabled device is attached to the bottom PS/2 connector.
3. Add, from the PCI 2.2 slots (wake enabled) row, the total number of wake enabled devices installed (PCI and AGP) and multiply by the standby current requirement.
4. Add, from the PCI 2.2 slots (non-wake enabled) row, the total number of non-wake enabled devices installed (PCI and AGP) and multiply by the standby current requirement.
5. Add all additional wake enabled devices' and non-wake enabled devices' standby current requirements as applicable.
6. Add all the required current totals from steps 1 through 5 to determine the total estimated standby current power supply requirement.

**Table 52. Standby Current Requirements**

| Instantly Available Current Support (Estimated for integrated board components) | Description | Standby Current Requirements (mA) |
|---|---|---|
| | Total for the VC820 board | 200 |
| **Instantly Available Stand-by Current Support**<br>• **Estimated for add-on components**<br>• **Add to Instantly Available total current requirement**<br>**(See instructions above)** | PS/2 Ports* | 345 |
| | PCI 2.2 slots (wake enabled) | 375 |
| | PCI 2.2 slots (non-wake enabled) | 20 |
| | WOL header | 225 |
| | AMR* | 150 |
| | USB Ports* | 507.5 (maximum for both ports) |

***** Dependent upon system configuration

**NOTE**

*IBM PS/2 Port Specification (Sept 1991) states*

- *275 mA for keyboard*
- *70 mA for the mouse (not wake-enable device)*

*PCI/AGP requirements are calculated by totaling the following:*

- *One wake enabled device @ 375 mA, plus*
- *Non-wake enabled devices @ 20 mA each, plus*

*USB requirements are calculated as:*

- *One USB wake enabled device @ 500 mA*
- *Three USB non-wake enabled devices @ 2.5 mA each*

**NOTE**

*Both USB ports are capable of providing up to 500 mA during normal G0/S0 operation. Only one USB port will support up to 500 mA of stand-by-current (wake enabled device) during G1/S3 suspended operation. The other port may provide up to 7.5 mA (three non-wake enabled devices only) during G1/S3 suspended operation.*

### 2.11.4 Fan Power Requirements

The VC820 Desktop Board is capable of supplying 250 mA per fan connector (maximum).

## 2.11.5 Power Supply Considerations

### ⚠ CAUTION

*The 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported. Refer to Section 2.11.3 on page 75 for additional information.*

System integrators should refer to the power usage values listed in Table 49 and Table 50 when selecting a power supply for use with this VC820 board.

Measurements account only for current sourced by the VC820 board while running in idle modes of the started operating systems.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

| For information about | Refer to |
|---|---|
| The ATX form factor specification | Section 1.3, page 16 |

## 2.12 Thermal Considerations

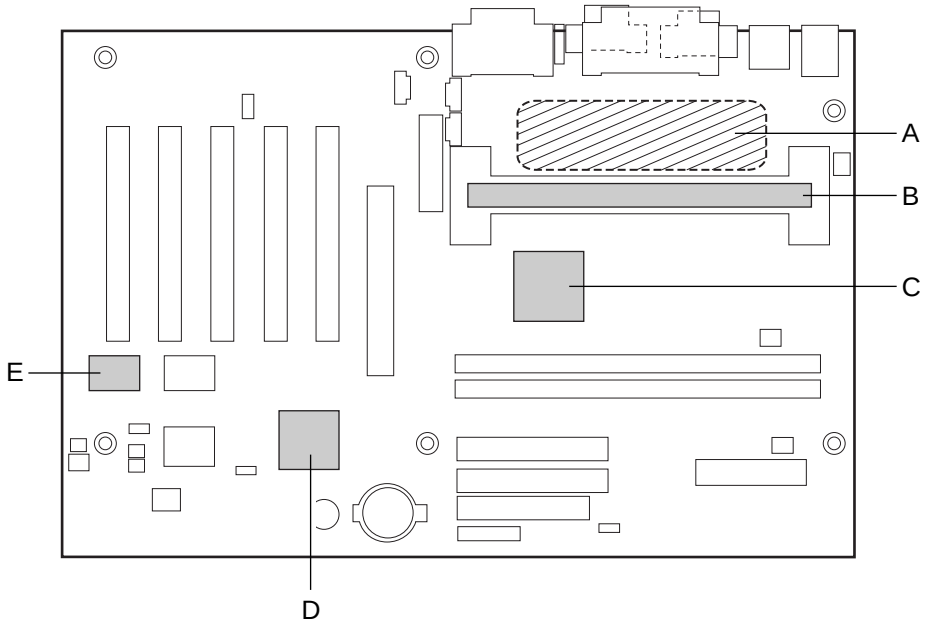
### ⚠ CAUTION

*An ambient temperature that exceeds the VC820 board's maximum operating temperature by 5 °C to 10°C could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.*

### ⚠ CAUTION

*System integrators should ensure that proper airflow is maintained in the voltage regulator circuit. The voltage regulator area can reach a temperature of up to 85 °C in an open chassis (item A in Figure 17). Failure to do so may result in damage to the voltage regulator circuit.*

Figure 17 shows the locations of the thermally sensitive components.




| | |
|---|---|
| A | Processor voltage regulator area |
| B | Processor |
| C | Intel 82820 MCH |
| D | Intel 82801AA ICH |
| E | ES1373 digital controller |

**Figure 17. Thermally-sensitive Components**

Table 53 provides maximum case temperatures for VC820 board components that are sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the VC820 board.

**Table 53. Thermal Considerations for Components**

| Processor Type | Processor / Host Bus Frequency | Maximum Processor Temperature | |
|---|---|---|---|
| | | **SECC** | **SECC2** |
| Pentium III processor | 450 / 100 MHz | N/A | 85º C (max thermal junction) |
| | 500 / 100 MHz | N/A | 85º C (max thermal junction) |
| | 550 / 100 MHz | N/A | 85º C (max thermal junction) |
| | 600 / 100 MHz | N/A | 85º C (max thermal junction) |
| | 550E / 100 MHz | NA | 82º C (max thermal junction) |
| | 600E / 100 MHz | NA | 82º C (max thermal junction) |
| | 650 / 100 MHz | NA | 82º C (max thermal junction) |
| | 700 / 100 MHz | NA | 80º C (max thermal junction) |
| | 533B / 133 MHz | N/A | 90º C (max thermal junction) |
| | 600B / 133 MHz | N/A | 85º C (max thermal junction) |
| | 533EB / 133 MHz | NA | 82º C (max thermal junction) |
| | 600EB / 133 MHz | NA | 82º C (max thermal junction) |
| | 667 / 133 MHz | NA | 82º C (max thermal junction) |
| | 733 / 133 MHz | NA | 80º C (max thermal junction) |
| Pentium II processor | 350 / 100 MHz | 75º C (max thermal plate) | NA |
| | 400 / 100 MHz | 75º C (max thermal plate) | NA |
| | 450 / 100 MHz | 75º C (max thermal plate) | 80º C (max thermal junction) |
| **Component Type** | **Maximum Component Temperature** | | |
| Intel 82820 MCH | 110 °C | | |
| Intel 82801AA ICH | 100 °C | | |
| ES 1373 | 70 °C | | |

## 2.13 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 55 ºC.

VC820 board MTBF: 208270.85 hours

## 2.14 Environmental

Table 54 lists the environmental specifications for the VC820 board.

**Table 54. VC820 Board Environmental Specifications**

| Parameter | Specification | | |
|---|---|---|---|
| **Temperature** | | | |
| Non-Operating | -40 °C to +70 °C | | |
| Operating | 0 °C to +55 °C | | |
| **Shock** | | | |
| Unpackaged | 30 g trapezoidal waveform | | |
| | Velocity change of 170 inches/second | | |
| Packaged | Half sine 2 millisecond | | |
| | Product Weight (pounds) | Free Fall (inches) | Velocity Change (inches/sec) |
| | <20 | 36 | 167 |
| | 21-40 | 30 | 152 |
| | 41-80 | 24 | 136 |
| | 81-100 | 18 | 118 |
| **Vibration** | | | |
| Unpackaged | 5 Hz to 20 Hz : 0.01 $g^2$ Hz sloping up to 0.02 $g^2$ Hz | | |
| | 20 Hz to 500 Hz : 0.02 $g^2$ Hz (flat) | | |
| Packaged | 10 Hz to 40 Hz : 0.015 $g^2$ Hz (flat) | | |
| | 40 Hz to 500 Hz : 0.015 $g^2$ Hz sloping down to 0.00015 $g^2$ Hz | | |

# 2.15 Regulatory Compliance

This section describes the VC820 board's compliance with safety and EMC regulations.

## 2.15.1 Safety Regulations

Table 55 lists the safety regulations with which the VC820 board complies when it is correctly installed in a compatible host system.

**Table 55. Safety Regulations**

| Regulation | Title |
|---|---|
| UL 1950/CSA950, 3rd edition, Dated 07-28-95 | Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada) |
| EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4) | The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Community) |
| IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4) | The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International) |
| EMKO-TSE (74-SEC) 207/94 | Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland) |

## 2.15.2 EMC Regulations

Table 56 lists the EMC regulations with which VC820 board complies with when it is correctly installed in a compatible host system.

**Table 56. EMC Regulations**

| Regulation | Title |
|---|---|
| FCC Class B | Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA) |
| CISPR 22, 2nd Edition, 1993 (Class B) | Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International) |
| VCCI Class B (ITE) | Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan) |
| EN55022 (1994) (Class B) | Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe) |
| EN50082-1 (1992) | Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe) |
| ICES-003 (1997) | Interference-Causing Equipment Standard, Digital Apparatus, Class B (Including CRC c.1374). (Canada) |
| AS/NZ 3548 | Australian Communications Authority (ACA), Standard for Electromagnetic Compatibility. |

### 2.15.3 Certification Markings

This printed circuit assembly has the following markings related to product certification:

- UL Joint Recognition Mark: Consists of small c followed by a stylized backward UR and followed by a small US (Component side)
- Manufacturer's recognition mark: Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (Solder side)
- UL File Number for VC820 boards: E139761 (Component side)
- PB Part Number: Intel bare circuit board part number (Solder side) PB726794-003
- Battery "+ Side Up" marking: located on the component side of the VC820 board in close proximity to the battery holder
- FCC Logo/Declaration: (Solder side)
- ACA (C-Tick) mark: Consists of a unique letter C, with a tick mark; followed by N-232. Located on the component side of the VC820 board and on the shipping container
- CE Mark: (Component side) The CE mark should also be on the shipping container

# 3 Overview of BIOS Features

## What This Chapter Contains



## 3.1 Introduction

The VC820 board uses an Intel/AMI BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the BIOS Setup program, POST, APM, the PCI auto-configuration utility, and Plug and Play support.

This VC820 board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST, identifying the type of BIOS and a revision code. The initial production BIOS is identified as VC82010A.86A.

| For information about | Refer to |
|---|---|
| The VC820 board's compliance level with APM and Plug and Play | Section 1.3, page 16 |

# 3.2 BIOS Flash Memory Organization

The Intel 82802AB Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable. Figure 18 shows the organization of the flash memory.

The last two 8 KB blocks of the fault tolerance area are the parameter blocks. These blocks contain data such as BIOS updates, vital product data (VPD), logo, System Management BIOS (SMBIOS) interface, and extended system configuration data (ESCD) information. The backup block contains a copy of the fault tolerance block.

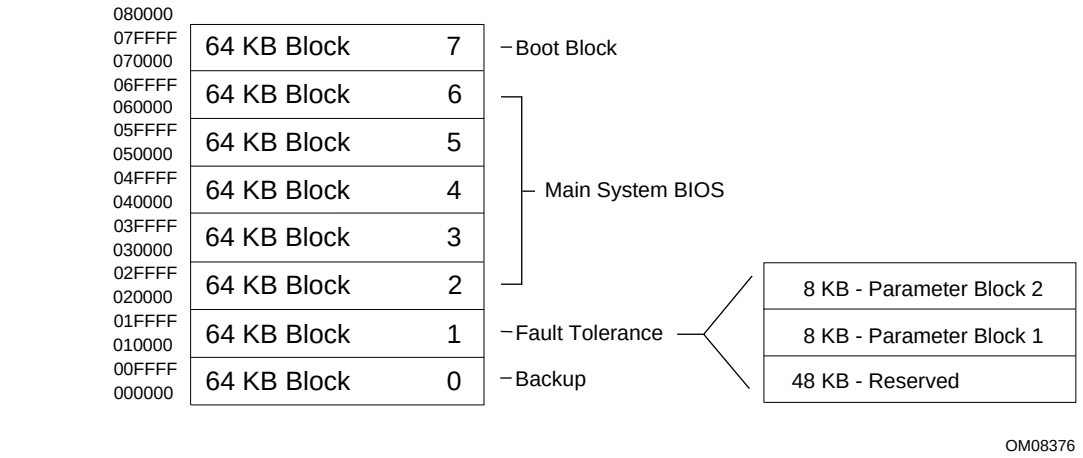



**Figure 18. Memory Map of the Flash Memory Device**

# 3.3 Resource Configuration

## 3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in boards. Autoconfiguration lets a user insert or remove PCI boards without having to configure the system. When a user turns on the system after adding a PCI board, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in board.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to system resources. The assignment of PCI interrupts to ISA IRQs is non-deterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 1.3.

### 3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to Ultra ATA/66 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.3 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance.

To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

**NOTE**

*Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.*

The VC820 board uses Host Detect to sense Ultra ATA/66 cables and hard drives. Additionally, this feature needs to be enabled in the operating system. (In Windows 98, for example, enable DMA in the Device Manager.)

To use Ultra ATA/66 features the following items are required:

- An Ultra ATA/66 peripheral device
- An Ultra ATA/66 compatible cable
- Operating system support for Ultra ATA/66
- Device driver support for Ultra ATA/66

**NOTE**

*Ultra ATA-66 compatible cables are backward compatible with drives using slower IDE transfer protocols.*

**NOTE**

*Some Ultra ATA/66 drivers do not support unique DMA speed settings for two hard drives connected to the same IDE interface (on the same cable). In this case, hard drives should be connected to different IDE interfaces through two separate cables to ensure the Ultra ATA/66 hard drives achieve maximum performance.*

# 3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor frequency
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT†, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

| For information about | Refer to |
|---|---|
| The VC820 board's compliance level with SMBIOS | Section 1.3, page 16 |

# 3.5 BIOS Upgrades

A new version of the BIOS can be upgraded from a diskette using the Intel® Flash Memory Update utility that is available from Intel. This utility supports the following BIOS maintenance functions:

- Update the flash BIOS from a file on a diskette
- Verify that the upgrade BIOS matches the target system to prevent accidentally installing an incompatible BIOS
- BIOS boot block update

BIOS upgrades and the Intel Flash Memory Update utility are available from Intel through the Intel World Wide Web site.

**NOTE**

*Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.*

| For information about | Refer to |
|---|---|
| The Intel World Wide Web site | Section 1.2, page 16 |

## 3.5.1 Language Support

The BIOS program and help messages are available in five languages from the BIOS: US English, German, Italian, French, and Spanish. The default language is US English unless another language is selected in the BIOS Setup program.

The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

## 3.5.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site. See Section 1.2 for more information about this site.

# 3.6 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is no video support. You can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- A single beep indicates the beginning of the BIOS recovery process.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Upgrade utility are available from Intel Customer Support through the Intel World Wide Web site.

### NOTE

*If the computer is configured to boot from an LS-120 diskette (in the Setup program's Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.*

| For information about | Refer to |
|---|---|
| The BIOS recovery mode jumper settings | Table 47, page 71 |
| The Boot menu in the BIOS Setup program | Section 4.7, page 109 |
| Contacting Intel customer support | Section 1.2, page 16 |

# 3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The default setting of the fourth device is disabled.

## 3.7.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device with bootable media.

The network can be selected as a boot device. This selection allows booting from a network add-in board with a remote boot ROM installed.

| For information about | Refer to |
|---|---|
| The El Torito specification | Section 1.3, page 16 |

## 3.7.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter (the BIOS will notify the user with one long and two short beeps)
- Keyboard
- Mouse

## 3.8 USB Legacy Support

USB legacy support enables USB devices such as keyboards, mice, and hubs to be used even when no operating system USB drivers are in place. USB legacy support is used in accessing the BIOS Setup program and installing an operating system that supports USB. By default, USB legacy support is set to Auto. The Auto setting enables USB legacy support if a supported USB device is connected to the USB port.

This sequence describes how USB legacy support operates in the Enabled (default) mode.

1. When you power up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is temporarily enabled by the BIOS. This allows you to use a USB keyboard to enter the BIOS Setup program or the maintenance mode.
4. POST completes and disables USB legacy support.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are not recognized. After the operating system loads the USB drivers, the USB devices are recognized by the operating system.

To install an operating system that supports USB, enable USB Legacy support or set it to Auto in the BIOS Setup program and follow the operating system's installation instructions. Once the operating system is installed and the USB drivers have been configured, USB legacy support is no longer used. USB Legacy support can be left enabled or set to Auto in the BIOS Setup program if needed.

Notes on using USB legacy support:

- Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non-USB aware operating system.
- USB legacy support is for keyboards, mice, and hubs only. Other USB devices are not supported.

# 3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. The user's access privileges are determined in the supervisor mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered. The user's access privileges are determined in the supervisor mode.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 57 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

**Table 57. Supervisor and User Password Functions**

| Password Set | Supervisor Mode | User Mode | Setup Options | Password to Enter Setup | Password During Boot |
|---|---|---|---|---|---|
| Neither | Can change all options * | Can change all options * | None | None | None |
| Supervisor only | Can change all options | Can change a limited number of options with the access level determined by supervisor. | Supervisor Password | Supervisor | None |
| User only | N/A | Can change all options | Enter Password Clear User Password | User | User |
| Supervisor and user set | Can change all options | Can change a limited number of options with the access level determined by supervisor. | Supervisor Password Enter Password | Supervisor or user | Supervisor or user |

* If no password is set, any user can change all Setup options.

| For information about | Refer to |
|---|---|
| Setting user and supervisor passwords | Section 4.5, page 107 |

# 4 BIOS Setup Program

## What This Chapter Contains



## 4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

| Maintenance | Main | Advanced | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

Table 58 lists the BIOS Setup program menu functions.

**Table 58. BIOS Setup Program Menu Bar**

| Maintenance | Main | Advanced | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|
| Clears passwords and enables extended configuration mode | Allocates resources for hardware components | Configures advanced features available through the chipset | Sets passwords and security features | Configures power management features | Selects boot options and power supply controls | Saves or discards changes to Setup program options |

**NOTE**

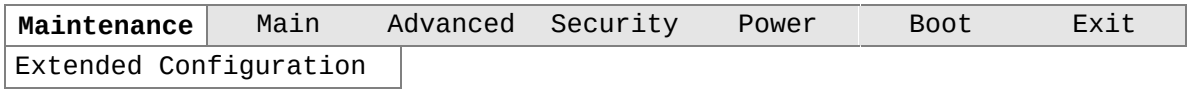
*In this chapter, all examples of the BIOS Setup Program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the board is in configuration mode. Section 2.9 on page 70 tells how to put the board in configuration mode.*

Table 59 lists the function keys available for menu screens.

**Table 59. BIOS Setup Program Function Keys**

| BIOS Setup Program Function Key | Description |
|---|---|
| <←> or <→> | Selects a different menu screen (Moves the cursor left or right) |
| <↑> or <↓> | Selects an item (Moves the cursor up or down) |
| <Tab> | Selects a field (Not implemented) |
| <Enter> | Executes command or selects the submenu |
| <F9> | Load the default configuration values for the current menu |
| <F10> | Save the current values and exits the BIOS Setup program |
| <Esc> | Exits the menu |

# 4.2 Maintenance Menu




The menu shown in Table 60 is for clearing Setup passwords and enabling extended configuration mode. Setup only displays this menu in configuration mode. See Section 2.9 on page 70 for configuration mode setting information.

**Table 60. Maintenance Menu**

| Feature | Options | Description |
|---|---|---|
| Clear All Passwords | No options | Clears the user and administrative passwords. |
| Extended Configuration | • **Default (default)**<br>• User-Defined | User Defined allows setting system control and video memory cache mode. If selected here, will also display in the Advanced Menu as: "Extended Menu: *Used*." |
| CPU Information | No options | Displays CPU Information. |
| CPU Stepping Signature | No options | Displays CPU's Stepping Signature. |
| CPU Microcode Update Revision | No options | Displays CPU's Microcode Update Revision. |

## 4.2.1 Extended Configuration Submenu

| Maintenance | Main | Advanced | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|
| Extended Configuration | | | | | | |

The submenu represented by Table 61 is for setting system control and video memory cache mode. This submenu becomes available when User Defined is selected under Extended Configuration.

**Table 61. Extended Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| System Control: Video Memory Cache Mode | • USWC | Selects Uncacheable Speculative Write-Combining (USWC) video memory cache mode. Full 32 byte contents of the Write Combining buffer are written to memory as required. Cache lookups are not performed. Both the video driver and the application must support Write Combining. |
| | • **UC (default)** | Selects Uncacheable (UC) video memory cache mode. This setting identifies the video memory range as uncacheable by the processor. Memory writes are performed in program order. Cache lookups are not performed. Well suited for applications not supporting Write Combining. |

# 4.3 Main Menu

| Maintenance | **Main** | Advanced | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

Table 62 describes the Main Menu. This menu reports processor and memory information and is for configuring the system date and system time.

**Table 62. Main Menu**

| Feature | Options | Description |
|---|---|---|
| BIOS Version | No options | Displays the version of the BIOS. |
| Processor Type | No options | Displays processor type. |
| Processor Speed | No options | Displays processor operating frequency. |
| System Bus Frequency | No options | Displays the of the system front side bus frequency. |
| Cache RAM | No options | Displays the size of second-level cache and whether it is ECC-capable. |
| Total Memory | No options | Displays the total amount of RAM. |
| Memory Bank 0<br>Memory Bank 1 | No options | Displays type of RIMM installed in each memory bank. |
| Language | • **English (US) (default)**<br>• German<br>• French<br>• Italian<br>• Spanish | Selects the default language used by the BIOS. |
| Processor Serial Number | • **Disabled (default)**<br>• Enabled | Enables and disables the processor serial number. |
| Memory Configuration | • Enabled<br>• **Disabled (default)** | Allows selection of ECC-mode memory operation if ECC-type memory is installed. |
| System Time | Hour, minute, and second | Specifies the current time. |
| System Date | Month, day, and year | Specifies the current date. |

# 4.4 Advanced Menu

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |

Table 63 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

**Table 63. Advanced Menu**

| Feature | Options | Description |
|---|---|---|
| Extended Configuration | Used<br>**Not Used (default)** | If *Used* is highlighted, *User-Defined* has been selected in Extended Configuration under the Maintenance Menu. |
| PCI Configuration | No options | Configures individual PCI slot's IRQ priority. When selected, displays the PCI Configuration submenu. |
| Boot Configuration | No options | Configures Plug and Play and the Numlock key, and resets configuration data. When selected, displays the Boot Configuration submenu. |
| Peripheral Configuration | No options | Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu. |
| IDE Configuration | No options | Specifies type of connected IDE device. |
| Diskette Configuration | No options | When selected, displays the Floppy Options submenu. |
| Event Log Configuration | No options | Configures Event Logging. When selected, displays the Event Log Configuration submenu. |
| Video Configuration | No options | Configures video features. When selected, displays the Video Configuration submenu. |

## 4.4.1 PCI Configuration Submenu

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| **PCI Configuration** |
|---|
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |

The submenu represented by Table 64 is for configuring the IRQ priority of PCI slots individually.

**Table 64. PCI Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| PCI Slot 1 IRQ Priority | • **Auto (default)**<br>9<br>10<br>11 | Allows selection of IRQ priority. |
| PCI Slot 2 IRQ Priority | • **Auto (default)**<br>9<br>10<br>11 | Allows selection of IRQ priority. |
| PCI Slot 3 IRQ Priority | • **Auto (default)**<br>9<br>10<br>11 | Allows selection of IRQ priority. IRQ Priority selections for PCI slots 3 and 5 are linked. Selections made to PCI Slot 3 IRQ Priority are repeated in PCI Slot 5 IRQ Priority. |
| PCI Slot 4 IRQ Priority | • **Auto (default)**<br>9<br>10<br>11 | Allows selection of IRQ priority. |
| PCI Slot 5 IRQ Priority | • Whatever is selected in slot 3 | No selections can be made to PCI Slot 5 IRQ Priority. Selections made to PCI Slot 3 repeat in PCI Slot 5. |

## 4.4.2 Boot Configuration Submenu

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| **Boot Configuration** |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |

The submenu represented by Table 65 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

**Table 65. Boot Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Plug & Play O/S | • **No (default)**<br>• Yes | Specifies if a Plug and Play operating system is being used.<br>*No* lets the BIOS configure all devices.<br>*Yes* lets the operating system configure Plug and Play devices. Not required with a Plug and Play operating system. |
| Reset Config Data | • **No (default)**<br>• Yes | Clears the BIOS configuration data on the next boot. |
| Numlock | • Off<br>• **On (default)** | Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard. |

## 4.4.3 Peripheral Configuration Submenu

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| **Peripheral Configuration** |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |

The submenu represented in Table 66 is used for enabling the onboard audio and LAN devices and legacy USB support.

**Table 66. Peripheral Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Serial port A | • Disabled<br>• Enabled<br>• **Auto (default)** | Configures Serial port A.<br>*Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4.<br>An * (asterisk) displayed next to an address indicates a conflict with another device. |
| Base I/O address<br>(Visible only if Enabled selected in Serial port A) | • **3F8 (default)**<br>• 2F8<br>• 3E8<br>• 2E8 | Specifies the base I/O address for Serial port A, if Serial port A is Enabled. |
| Interrupt<br>(Visible only if Enabled selected in Serial port A) | • IRQ 3<br>• **IRQ 4 (default)** | Specifies the interrupt for Serial port A, if Serial port A is Enabled. |
| Serial port B | • Disabled<br>• Enabled<br>• **Auto (default)** | Configures serial port B.<br>*Auto* assigns the first free COM port, normally COM2, the address 2F8h, and the interrupt IRQ3.<br>An * (asterisk) displayed next to an address indicates a conflict with another device.<br>If either serial port address is set, that address will not appear in the list of options for the other serial port. |
| Mode | • **Normal (default)**<br>• IrDA SIR-A<br>• ASK_IR | Specifies the mode for Serial port B for normal (COM 2) or infrared applications. This option is not available if Serial port B has been disabled. |

continued

**Table 64. Peripheral Configuration Submenu** (continued)

| Feature | Options | Description |
|---|---|---|
| Base I/O address<br>(Visible only if Enabled selected in Serial port B) | • 3F8<br>• **2F8 (default)**<br>• 3E8<br>• 2E8 | Specifies the base I/O address for Serial port B. |
| Interrupt<br>(Visible only if Enabled selected in Serial port B) | • **IRQ 3 (default)**<br>• IRQ 4 | Specifies the interrupt for Serial port B. |
| Parallel port | • Disabled<br>• Enabled<br>• **Auto (default)** | Configures the parallel port.<br>*Auto* assigns LPT1 the address 378h and the interrupt IRQ7.<br>An * (asterisk) displayed next to an address indicates a conflict with another device. |
| Mode | • Output Only<br>• **Bi-directional (default)**<br>• EPP<br>• ECP | Selects the mode for the parallel port. Not available if the parallel port is disabled.<br>*Output Only* operates in AT†-compatible mode.<br>*Bi-directional* operates in PS/2-compatible mode.<br>*EPP* is Extended Parallel Port mode, a high-speed bi-directional mode.<br>*ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode. |
| Base I/O address<br>(Visible only if Enabled selected in Parallel port) | • **378 (default)**<br>• 278<br>• 228 | Specifies the base I/O address for the parallel port. |
| Interrupt<br>(Visible only if Enabled selected in Parallel port) | • IRQ 5<br>• **IRQ 7(default)** | Specifies the interrupt for the parallel port. |
| Audio Device | • Disabled<br>• **Enabled (default)** | Enables or disables the onboard audio subsystem. |
| Legacy USB Support | • Disabled<br>• **Enabled (default)** | Enables or disables USB legacy support.<br>(See Section 3.8 on page 90 for more information.) |

## 4.4.4 IDE Configuration Submenu

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| **IDE Configuration** |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |

The submenu represented in Table 67 is used to configure IDE device options.

**Table 67. IDE Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| IDE Controller | • Disabled<br>• Primary<br>• Secondary<br>• **Both (default)** | Specifies the integrated IDE controller.<br>*Primary* enables only the primary IDE controller.<br>*Secondary* enables only the secondary IDE controller.<br>*Both* enables both IDE controllers. |
| Hard Disk Pre-Delay | • **Disabled (default)**<br>• 3 Seconds<br>• 6 Seconds<br>• 9 Seconds<br>• 12 Seconds<br>• 15 Seconds<br>• 21 Seconds<br>• 30 Seconds | Specifies the hard disk drive pre-delay. |
| Primary IDE Master | No options | Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu. |
| Primary IDE Slave | No options | Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu. |
| Secondary IDE Master | No options | Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu. |
| Secondary IDE Slave | No options | Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu. |

### 4.4.4.1 IDE Configuration Sub-Submenus

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| **IDE Configuration**<br>**Primary IDE Master**<br>**Primary IDE Slave**<br>**Secondary IDE Master**<br>**Secondary IDE Slave** |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |

The sub-submenus represented in Table 68 are used to configure IDE devices.

**Table 68. IDE Configuration Sub-Submenus**

| Feature | Options | Description |
|---|---|---|
| Type | • None<br>• User<br>• **Auto (default)**<br>• CD-ROM<br>• ATAPI Removable<br>• Other ATAPI<br>• IDE Removable | Specifies the IDE configuration mode for IDE devices.<br>*User* allows the cylinders, heads, and sectors fields to be changed.<br>*Auto* automatically fills in the values for the cylinders, heads, and sectors fields. |
| LBA Mode Control | • Disabled<br>• **Enabled (default)** | Enables or disables LBA Mode Control. |
| Multi-Sector Transfers | • Disabled<br>• 2 Sectors<br>• 4 Sectors<br>• 8 Sectors<br>• **16 Sectors (default)** | Specifies number of sectors per block for transfers from the hard disk drive to memory.<br>Check the hard disk drive's specifications for optimum setting. |
| Transfer Mode | • **Auto (default)**<br>• Fast 0<br>• Fast 1<br>• Fast 2<br>• Fast 3<br>• Fast 4 | Specifies the transfer mode. |

continued

**Table 67. IDE Configuration Sub-Submenus** (continued)

| Feature | Options | Description |
|---|---|---|
| Ultra DMA | • **Disabled (default)**<br>• Mode 0<br>• Mode 1<br>• Mode 2<br>• Mode 3<br>• Mode 4 | Specifies the Ultra DMA mode for the drive.<br>Note that when Auto is selected in Transfer Mode, the BIOS sets Ultra DMA to the fastest speed supported. If the drive doesn't support Ultra DMA, the BIOS sets Ultra DMA to disabled and the fastest supported PIO mode will be used instead. |

## 4.4.5 Diskette Configuration Submenu

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| **Diskette Configuration** |
| Event Log Configuration |
| Video Configuration |

The submenu represented by Table 69 is used for configuring the diskette drive.

**Table 69. Diskette Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Diskette Controller | • Disabled<br>• **Enabled (default)** | Disables or enables the integrated diskette controller. |
| Floppy A | • Not Installed<br>• 360 KB 5¼<br>• 1.2 MB 5¼<br>• 720 KB 3½<br>• **1.44/1.25 MB 3½ (default)**<br>• 2.88 MB 3½ | Specifies the capacity and physical size of diskette drive A. |
| Diskette Write Protect | • **Disabled (default)**<br>• Enabled | Disables or enables write-protect for the diskette drive. |

## 4.4.6 Event Log Configuration Submenu

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| **Event Log Configuration** |
| Video Configuration |

The submenu represented by Table 70 is used to configure the event logging features.

**Table 70. Event Log Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Event log | No options | Indicates if there is space available in the event log. |
| Event log validity | No options | Indicates if the contents of the event log are valid. |
| View event log | [Enter] | Displays the event log. |
| Clear all event logs | • **No (default)**<br>• Yes | Clears the event log after rebooting. |
| Event Logging | • Disabled<br>• **Enabled (default)** | Enables logging of events. |
| ECC Event Logging | • Disabled<br>• **Enabled (default)** | Enables logging of ECC events. |
| Mark events as read | [Enter] | Marks all events as read. |

## 4.4.7 Video Configuration Submenu

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| **Video Configuration** |

The submenu represented in Table 71 is for configuring the video features.

**Table 71. Video Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| AGP Aperture Size | • **64 MB (default)**<br>• 256 MB | Specifies the aperture size for the AGP video controller. |
| Primary Video Adapter | • **AGP (default)**<br>• PCI | Selects primary video adapter to be used during boot. |

# 4.5 Security Menu

| Maintenance | Main | Advanced | **Security** | Power | Boot | Exit |
|---|---|---|---|---|---|---|

The menu represented by Table 72 is for setting passwords and security features.

**Table 72. Security Menu**

| **If no password entered previously:** | | |
|---|---|---|
| **Feature** | **Options** | **Description** |
| Supervisor Password Is | No options | Reports if there is a supervisor password set. |
| User Password Is | No options | Reports if there is a user password set. |
| Set Supervisor Password | Password can be up to seven alphanumeric characters. | Specifies the supervisor password. |
| Set User Password | Password can be up to seven alphanumeric characters. | Specifies the user password. |
| **If password entered previously:** | | |
| **Feature** | **Options** | **Description** |
| Clear User Password (Supervisor only) | • Yes<br>• No | Allows removal of a previously entered password. |
| User Access Level (Supervisor only) | • Limited<br>• No access<br>• View Only<br>• **Full (default)** | Specifies user's access privileges. |
| Unattended Start | • Enabled<br>• **Disabled (default)** | When enabled, the computer boots, but the keyboard is locked. The user must enter a password to unlock the computer or boot from a diskette. |

# 4.6 Power Menu

| Maintenance | Main | Advanced | Security | **Power** | Boot | Exit |
|---|---|---|---|---|---|---|

The menu represented in Table 73 is for setting the power management features.

**Table 73. Power Menu**

| Feature | Options | Description |
|---|---|---|
| Power Management | • Disabled<br>• **Enabled (default)** | Enables or disables the BIOS power management feature. |
| Inactivity Timer | • Off<br>• 1 Minute<br>• 5 Minutes<br>• 10 Minutes<br>• **20 Minutes (default)**<br>• 30 Minutes<br>• 60 Minutes<br>• 120 Minutes | Specifies the amount of time before the computer enters standby mode. |
| Hard Drive | • Disabled<br>• **Enabled (default)** | Enables power management for hard disks during standby modes. |
| Video Power-Down | • Disabled<br>• Standby<br>• **Suspend (default)**<br>• Sleep | Specifies power management for video during standby modes. |
| ACPI Suspend State | • **S1 State (default)**<br>• S3 State | Specifies the ACPI suspend state. |

**NOTE**

*When an ACPI capable operating system is configured for ACPI, only the ACPI Suspend State option effects power management. The ACPI Suspend State is not supported if the system is configured for APM.*

# 4.7 Boot Menu

| Maintenance | Main | Advanced | Security | Power | **Boot** | Exit |
|---|---|---|---|---|---|---|
| | | | | | IDE Drive Configuration | |

The menu represented in Table 74 is used to set the boot features and the boot sequence.

**Table 74. Boot Menu**

| Feature | Options | Description |
|---|---|---|
| Quiet Boot | • Disabled<br>• **Enabled (default)** | *Disabled* displays normal POST messages.<br>*Enabled* displays OEM graphic instead of POST messages. |
| Quick Boot | • Disabled<br>• **Enabled (default)** | Enables the computer to boot without running certain POST tests. |
| Scan User Flash Area | • **Disabled (default)**<br>• Enabled | Enables the BIOS to scan the flash memory for user binary files that are executed at boot time. |
| After Power Failure | • Stays Off<br>• **Last State (default)**<br>• Power-On | Specifies the mode of operation if an AC/Power loss occurs. *Power-On* restores power to the computer.<br>*Stay-Off* keeps the power off until the power button is pressed.<br>*Last State* restores the previous power state before power loss occurred. |
| On Modem Ring | • **Stay-Off (default)**<br>• Power-On | Specifies how the computer responds to an incoming call on an installed modem when the power is off. This soft-off mode applies to Wake on Ring technology. This feature applies only to systems configured in APM mode. |
| 1st Boot Device<br>2nd Boot Device<br>3rd Boot Device<br>4th Boot Device<br>(This list varies in length with the number of devices selected up to 8.) | • Floppy<br>• ARMD-FDD (Note 1)<br>• ARMD-HDD (Note 2)<br>• IDE-HDD (Note 3)<br>• ATAPI CDROM<br>• Disabled | Specifies the boot sequence from the available devices. To specify boot sequence:<br>1. Select the boot device with <↑> or <↓>.<br>2. Press <Enter> to set the selection as the intended boot device.<br>The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering.<br>Not all of the devices in this list are available as second, third, and fourth boot devices. The default settings for the first through fourth boot devices are, respectively:<br>• Floppy<br>• 1st IDE-HDD<br>• ATAPI CDROM<br>• Disabled |
| IDE Drive Configuration | No Options | Configures IDE drives. When selected, displays the IDE Drive Configuration submenu. |

Notes:

1 ARMD-FDD = ATAPI removable device - floppy disk drive

2 ARMD-HDD = ATAPI removable device - hard disk drive

3 HDD = Hard Disk Drive.

### 4.7.1 IDE Drive Configuration Submenu

| Maintenance | Main | Advanced | Security | Power | **Boot** | Exit |
|---|---|---|---|---|---|---|
| | | | | | **IDE Drive Configuration** | |

The submenu represented in Table 75 is used to set the order in which the IDE drives boot. Changing the boot-order of a given drive causes the boot-order for the other drives to change automatically to accommodate your selection.

**Table 75. IDE Drive Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Primary Master IDE | **1st IDE (default)**<br>1 through 4 | Allows you to select the order in which the Primary Master IDE drive boots. |
| Primary Slave IDE | **2nd IDE (default)**<br>1 through 4 | Allows you to select the order in which the Primary Slave IDE drive boots. |
| Secondary Master IDE | **3rd IDE (default)**<br>1 through 4 | Allows you to select the order in which the Secondary Master IDE drive boots. |
| Secondary Slave IDE | **4th IDE (default)**<br>1 through 4 | Allows you to select the order in which the Secondary Slave IDE drive boots. |

## 4.8 Exit Menu

| Maintenance | Main | Advanced | Security | Power | Boot | **Exit** |
|---|---|---|---|---|---|---|

The menu represented in Table 76 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

**Table 76. Exit Menu**

| Feature | Description |
|---|---|
| Exit Saving Changes | Exits and saves the changes in CMOS SRAM. |
| Exit Discarding Changes | Exits without saving any changes made in the BIOS Setup program. |
| Load Setup Defaults | Loads the factory default values for all the Setup options. |
| Load Custom Defaults | Loads the custom defaults for Setup options. |
| Save Custom Defaults | Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults. |
| Discard Changes | Discards changes without exiting Setup. The option values present when the computer was turned on are used. |

# 5 Error Messages and Beep Codes

## What This Chapter Contains



## 5.1 BIOS Error Messages

Table 77 lists the error messages and provides a brief description of each.

**Table 77. BIOS Error Messages**

| Error Message | Explanation |
|---|---|
| GA20 Error | An error occurred with Gate A20 when switching to protected mode during the memory test. |
| Pri Master HDD Error<br>Pri Slave HDD Error<br>Sec Master HDD Error<br>Sec Slave HDD Error | Could not read sector from corresponding drive. |
| Pri Master Drive - ATAPI Incompatible<br>Pri Slave Drive - ATAPI Incompatible<br>Sec Master Drive - ATAPI Incompatible<br>Sec Slave Drive - ATAPI Incompatible | Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly. |
| A: Drive Error<br>B: Drive Error | No response from diskette drive. |
| Cache Memory Bad | An error occurred when testing L2 cache. Cache memory may be bad. |
| CMOS Battery Low | The battery may be losing power. Replace the battery soon. |
| CMOS Display Type Wrong | The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct. |
| CMOS Checksum Bad | The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values. |
| CMOS Settings Wrong | CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed. |
| CMOS Date/Time Not Set | The time and/or date values stored in CMOS are invalid. Run Setup to set correct values. |
| DMA Error | Error during read/write test of DMA controller. |
| FDC Failure | Error occurred trying to access diskette drive controller. |
| HDC Failure | Error occurred trying to access hard disk controller. |

continued

**Table 77. BIOS Error Messages** (continued)

| Error Message | Explanation |
|---|---|
| Checking NVRAM..... | NVRAM is being checked to see if it is valid. |
| Update OK! | NVRAM was invalid and has been updated. |
| Updated Failed | NVRAM was invalid but was unable to be updated. |
| Keyboard Is Locked | The system keyboard lock is engaged. The system must be unlocked to continue to boot. |
| Keyboard Error | Error in the keyboard connection. Make sure keyboard is connected properly. |
| KB/Interface Error | Keyboard interface test failed. |
| Memory Size Decreased | Memory size has decreased since the last boot. If no memory was removed then memory may be bad. |
| Memory Size Increased | Memory size has increased since the last boot. If no memory was added there may be a problem with the system. |
| Memory Size Changed | Memory size has changed since the last boot. If no memory was added or removed then memory may be bad. |
| No Boot Device Available | System did not find a device to boot. |
| Off Board Parity Error | A parity error occurred on an off-board card. This error is followed by an address. |
| On Board Parity Error | A parity error occurred in onboard memory. This error is followed by an address. |
| Parity Error | A parity error occurred in onboard memory at an unknown address. |
| NVRAM / CMOS / PASSWORD cleared by Jumper | NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed. |
| <CTRL_N> Pressed | CMOS is ignored and NVRAM is cleared. User must enter Setup. |

## 5.2 Port 80h POST Codes

During the POST the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires an add-in board (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 78 defines the Uncompressed INIT Code Checkpoints, Table 79 describes the Boot Block Recovery Code Checkpoints, and Table 80 lists the Runtime Code Uncompressed in F000 Shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

**Table 78. Uncompressed INIT Code Checkpoints**

| Code | Description of POST Operation |
|---|---|
| D0 | NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting. |
| D1 | Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode. |
| D3 | Perform necessary chipset initialization, start memory refresh, perform Memory sizing. |
| D4 | Verify base memory. |
| D5 | Init code to be copied to segment 0 and control to be transferred to segment 0. |
| D6 | Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS. |
| D7 | Find Main BIOS module in ROM image. |
| D8 | Uncompress the main BIOS module. |
| D9 | Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM. |

**Table 79. Boot Block Recovery Code Checkpoints**

| Code | Description of POST Operation |
|---|---|
| E0 | Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller. |
| E8 | Initialize extra (Intel Recovery) Module. |
| E9 | Initialize floppy drive. |
| EA | Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code. |
| EB | Booting from floppy failed, look for ATAPI (LS120, Zip) devices. |
| EC | Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code. |
| EF | Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9). |

**Table 80. Runtime Code Uncompressed in F000 Shadow RAM**

| Code | Description of POST Operation |
|---|---|
| 03 | NMI is Disabled. To check soft reset/power-on. |
| 05 | BIOS stack set. Going to disable cache if any. |
| 06 | POST code to be uncompressed. |
| 07 | CPU init and CPU data area init to be done. |
| 08 | CMOS checksum calculation to be done next. |
| 0B | Any initialization before keyboard BAT to be done next. |
| 0C | KB controller I/B free. To issue the BAT command to keyboard controller. |
| 0E | Any initialization after KB controller BAT to be done next. |
| 0F | Keyboard command byte to be written. |
| 10 | Going to issue Pin-23,24 blocking/unblocking command. |
| 11 | Going to check pressing of <INS>, <END> key during power-on. |
| 12 | To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers. |
| 13 | Video display is disabled and port-B is initialized. Chipset init about to begin. |
| 14 | 8254 timer test about to start. |
| 19 | About to start memory refresh test. |
| 1A | Memory Refresh line is toggling. Going to check 15 µs ON/OFF time. |
| 23 | To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable. |
| 24 | To do any setup before Int vector init. |
| 25 | Interrupt vector initialization to begin. To clear password if necessary. |
| 27 | Any initialization before setting video mode to be done. |
| 28 | Going for monochrome mode and color mode setting. |
| 2A | Different buses init (system, static, and output devices) to start if present. (See Section 5.3 for details of different buses.) |
| 2B | To give control for any setup required before optional video ROM check. |
| 2C | To look for optional video ROM and give control. |
| 2D | To give control to do any processing after video ROM returns control. |
| 2E | If EGA/VGA not found then do display memory R/W test. |
| 2F | EGA/VGA not found. Display memory R/W test about to begin. |
| 30 | Display memory R/W test passed. About to look for the retrace checking. |
| 31 | Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test. |
| 32 | Alternate Display memory R/W test passed. To look for the alternate display retrace checking. |
| 34 | Video display checking over. Display mode to be set next. |
| 37 | Display mode set. Going to display the power-on message. |
| 38 | Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.) |
| 39 | Display different buses initialization error messages. (See Section 5.3 for details of different buses.) |
| 3A | New cursor position read and saved. To display the Hit <DEL> message. |

continued

**Table 80. Runtime Code Uncompressed in F000 Shadow RAM** (continued)

| Code | Description of POST Operation |
|---|---|
| 40 | To prepare the descriptor tables. |
| 42 | To enter in virtual mode for memory test. |
| 43 | To enable interrupts for diagnostics mode. |
| 44 | To initialize data to check memory wrap around at 0:0. |
| 45 | Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size. |
| 46 | Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory. |
| 47 | Pattern to be tested written in extended memory. Going to write patterns in base 640k memory. |
| 48 | Patterns written in base memory. Going to find out amount of memory below 1M memory. |
| 49 | Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory. |
| 4B | Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh). |
| 4C | Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M. |
| 4D | Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h). |
| 4E | Memory test started. (NOT SOFT RESET) About to display the first 64k memory size. |
| 4F | Memory size display started. This will be updated during memory test. Going for sequential and random memory test. |
| 50 | Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/ shadow. |
| 51 | Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow. |
| 52 | Memory testing/initialization above 1M complete. Going to save memory size information. |
| 53 | Memory size information is saved. CPU registers are saved. Going to enter in real mode. |
| 54 | Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI. |
| 57 | A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow. |
| 58 | Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message. |
| 59 | Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test. |
| 60 | DMA page register test passed. To do DMA#1 base register test. |
| 62 | DMA#1 base register test passed. To do DMA#2 base register test. |
| 65 | DMA#2 base register test passed. To program DMA unit 1 and 2. |
| 66 | DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller. |
| 7F | Extended NMI sources enabling is in progress. |
| 80 | Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command. |
| 81 | Keyboard reset error/stuck key found. To issue keyboard controller interface test command. |
| 82 | Keyboard controller interface test over. To write command byte and init circular buffer. |
| 83 | Command byte written, global data init done. To check for lock-key. |

continued

**Table 80. Runtime Code Uncompressed in F000 Shadow RAM** (continued)

| Code | Description of POST Operation |
|---|---|
| 84 | Lock-key checking over. To check for memory size mismatch with CMOS. |
| 85 | Memory size check done. To display soft error and check for password or bypass setup. |
| 86 | Password checked. About to do programming before setup. |
| 87 | Programming before setup complete. To uncompress SETUP code and execute CMOS setup. |
| 88 | Returned from CMOS setup program and screen is cleared. About to do programming after setup. |
| 89 | Programming after setup complete. Going to display power-on screen message. |
| 8B | First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done. |
| 8C | Setup options programming after CMOS setup about to start. |
| 8D | Going for hard disk controller reset. |
| 8F | Hard disk controller reset done. Floppy setup to be done next. |
| 91 | Floppy setup complete. Hard disk setup to be done next. |
| 95 | Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.) |
| 96 | Going to do any init before C800 optional ROM control. |
| 97 | Any init before C800 optional ROM control is over. Optional ROM check and control will be done next. |
| 98 | Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache. |
| 99 | Any initialization required after optional ROM test over. Going to setup timer data area and printer base address. |
| 9A | Return after setting timer and printer base address. Going to set the RS-232 base address. |
| 9B | Returned after RS-232 base address. Going to do any initialization before Coprocessor test. |
| 9C | Required initialization before Coprocessor is over. Going to initialize the Coprocessor next. |
| 9D | Coprocessor initialized. Going to do any initialization after Coprocessor test. |
| 9E | Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and Numlock. |
| A2 | Going to display any soft errors. |
| A3 | Soft error display complete. Going to set keyboard typematic rate. |
| A4 | Keyboard typematic rate set. To program memory wait states. |
| A5 | Going to enable parity/NMI. |
| A7 | NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000. |
| A8 | Initialization before E000 ROM control over. E000 ROM to get control next. |
| A9 | Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control. |
| AA | Initialization after E000 optional ROM control is over. Going to display the system configuration. |
| AB | Put INT13 module runtime image to shadow. |
| AC | Generate MP for multiprocessor support (if present). |
| AD | Put CGA INT10 module (if present) in Shadow. |

continued

**Table 80. Runtime Code Uncompressed in F000 Shadow RAM** (continued)

| Code | Description of POST Operation |
|---|---|
| AE | Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow. |
| B1 | Going to copy any code to specific area. |
| 00 | Copying of code to specific area done. Going to give control to INT-19 boot loader. |

## 5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 81 describes the bus initialization checkpoints.

**Table 81. Bus Initialization Checkpoints**

| Checkpoint | Description |
|---|---|
| 2A | Different buses init (system, static, and output devices) to start if present. |
| 38 | Different buses init (input, IPL, and general devices) to start if present. |
| 39 | Display different buses initialization error messages. |
| 95 | Init of different buses optional ROMs from C800 to start. |

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 82 describes the upper nibble of the high byte and indicates the function that is being executed.

**Table 82. Upper Nibble High Byte Functions**

| Value | Description |
|---|---|
| 0 | func#0, disable all devices on the bus concerned. |
| 1 | func#1, static devices init on the bus concerned. |
| 2 | func#2, output device init on the bus concerned. |
| 3 | func#3, input device init on the bus concerned. |
| 4 | func#4, IPL device init on the bus concerned. |
| 5 | func#5, general device init on the bus concerned. |
| 6 | func#6, error reporting for the bus concerned. |
| 7 | func#7, add-on ROM init for all buses. |

Table 83 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

**Table 83. Lower Nibble High Byte Functions**

| Value | Description |
|---|---|
| 0 | Generic DIM (Device Initialization Manager) |
| 1 | On-board System devices |
| 2 | ISA devices |
| 3 | EISA devices |
| 4 | ISA PnP devices |
| 5 | PCI devices |

# 5.4 Speaker

A 47 Ω inductive speaker is mounted on the VC820 board. The speaker provides audible error code (beep code) information during POST.

| For information about | Refer to |
|---|---|
| The location of the onboard speaker | Figure 1, page 14 |

## 5.5 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 84). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video board or no board installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

**Table 84. Beep Codes**

| Beep | Description |
|---|---|
| 1 | Refresh failure |
| 2 | Parity cannot be reset |
| 3 | Memory failure |
| 4 | Timer not operational |
| 5 | Not used |
| 6 | 8042 GateA20 cannot be toggled |
| 7 | Exception interrupt error |
| 8 | Display memory R/W error |
| 9 | Not used |
| 10 | CMOS Shutdown register test error |
| 11 | Invalid BIOS (e.g. POST module not found, etc.) |

# 5.6 Enhanced Diagnostics

The enhanced diagnostics feature consists of a hardware decoder and four LEDs located between the audio connectors and the serial port B connector on the back panel. This feature requires no modifications to the chassis (other than I/O back panel shield) or cabling.

Figure 19 shows the location of the diagnostic LEDs. Table 85 lists the diagnostic codes displayed by the LEDs.

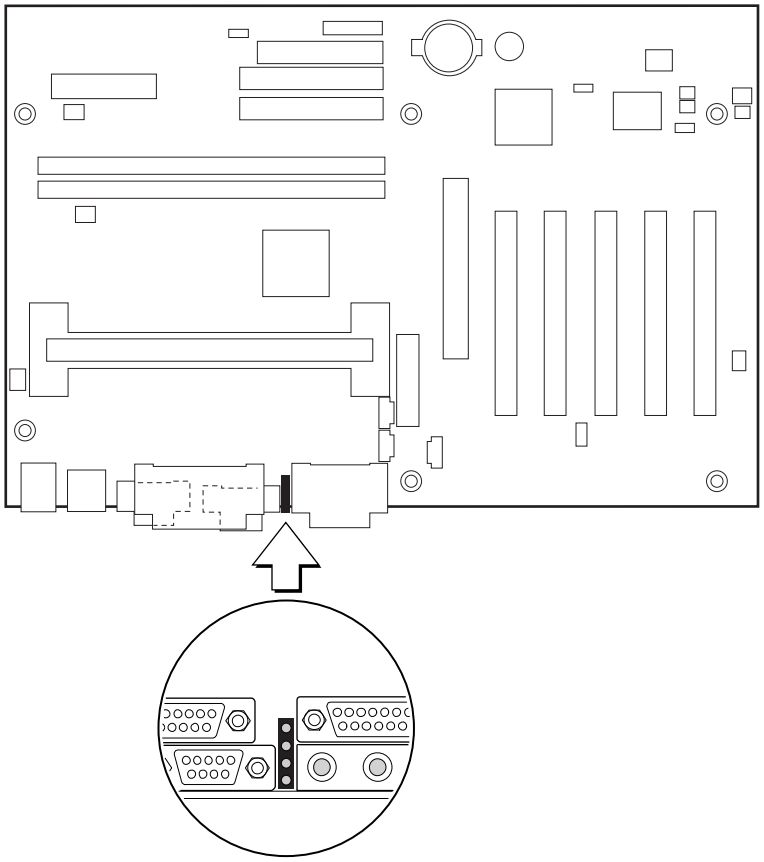
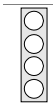
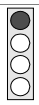
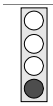
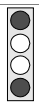
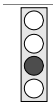
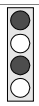
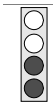
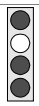
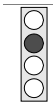
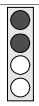
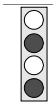
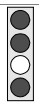
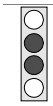
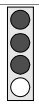
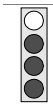
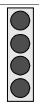



**Figure 19. Enhanced Diagnostic LEDs**

**Table 85. Diagnostic LED Codes**

| Display | BIOS Operation | Display | BIOS Operation |
|---|---|---|---|
|  Amber Amber Amber Amber | Power-on, starting BIOS |  Green Amber Amber Amber | Undefined |
|  Amber Amber Amber Green | Recovery mode |  Green Amber Amber Green | Undefined |
|  Amber Amber Green Amber | Processor, cache, etc. |  Green Amber Green Amber | Undefined |
|  Amber Amber Green Green | Memory, auto-size, shadow, etc. |  Green Amber Green Green | Undefined |
|  Amber Green Amber Amber | PCI bus initialization |  Green Green Amber Amber | Undefined |
|  Amber Green Amber Green | Video |  Green Green Amber Green | Undefined |
|  Amber Green Green Amber | IDE bus initialization |  Green Green Green Amber | Reserved |
|  Amber Green Green Green | USB initialization |  Green Green Green Green | Booting operating system |

Note: Undefined states are reserved for future use.