PF222-04

SED9420C$_{AC}$

CMOS DATA SEPARATOR FOR FDD

- **Built-in Terminals for Switching between $5\frac{1}{4}$-inch and 8-inch Floppy Disks and between Double Density and Single Density**
- **For Filter Switching System Only**

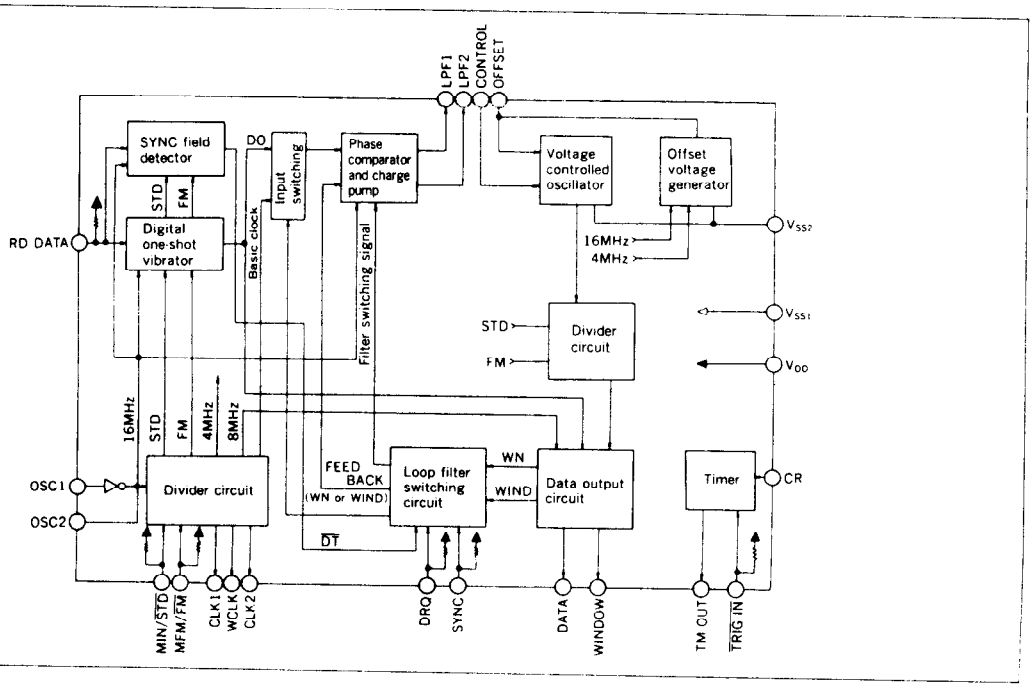
DESCRIPTION

The SED9420C$_{AC}$ is a CMOS VFO data separator LSI for use in floppy disk interfaces. Equipped with its own SYNC field detection, loop filter switching, and timer functions, the IC allows construction of a one-chip VFO circuit with just a few external components. Floppy disk controllers which can be used with this IC are the μPD765, μPD765A, FD1791-02, FD1793-02, MB8876A, MB8877A.

FEATURES

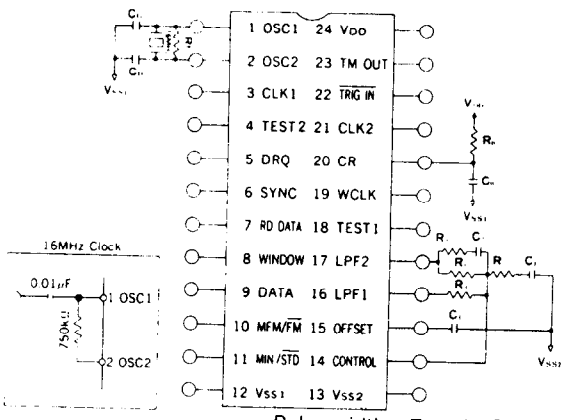
- Data separation function using the VFO system (a phase locked loop)
- Switchable between 8-inch and $5\frac{1}{4}$-inch floppy disk drives (FDDs)
- Recording can be switched between double density and single density
- Requires no adjustment and few external circuits
- Compatible with the IBM Format
- Clock output for floppy disk controllers ·····to be connected with μPD765series, MB8877series or FD179Xseries
- Single 5V power supply
- TTL-compatible I/O pins (excluding OSC1 and OSC2)
- Built-in timer circuit (with external C-R)
- Package·····DIP-24pin (plastic)

BLOCK DIAGRAM



■PIN CONFIGURATION AND AN EXAMPLE OF EXTERNAL CIRCUITS

○ SED9420C AC



Pulse width $Tw = 1.42 \times C_0R_0$

$R_0 > 5k\Omega$

[Reference value of external circuits]

FDD	$5\frac{1}{4}$-inch/8-inch
R_1	33kΩ
R_2	2.4kΩ
R_3	7.5kΩ
R_4	100Ω
C_1	0.01μF
C_2	3,300pF
C_3	0.01 to 0.1μF
C_D	10pF
C_G	10pF
R_F	1 MΩ
f_0	16MHz ± 0.5%

Accuracy of resistor ±5%, Accuracy of capacitor ±10%

■PIN DESCRIPTION

Pin Name	Pin No.	Function
OSC1	1	(1) Gate input terminal for the inverted amplifier of the crystal oscillator circuit. (2) Clock input terminal when using an external 16MHz clock.
OSC2	2	Drain output terminal for the crystal oscillator circuit's inverted amplifier.
CLK1	3	FDC clock output terminal (for the μPD765) • f = 8MHz for 8-inch floppy disk • f = 4MHz for $5\frac{1}{4}$-inch floppy disk
TEST2*	4	Test terminal for testing functions (with pull-up resistor)
DRQ*	5	Input signal for FDC data transfer signal (with pull-up resistor)
SYNC*	6	FDC control signal input terminal for GAP area and SYNC area detection (with pull-up resistor).
RD DATA*	7	Input terminal for the read data signal from the floppy disk drive (FDD) (with pull-up resistor).
WINDOW	8	Output terminal for the data window signal used to separate data pulses in the DATA signal from clock pulses.
DATA	9	Output terminal for the read data signal produced from the RD DATA signal. Sent to the FDC together with the WINDOW signal, and is then separated into clock and data pulses.
MFM/$\overline{FM}$*	10	Terminal for switching between double density and single density (with pull-up resistor) HIGH selects double density (MFM), LOW selects single density (FM).
MIN/$\overline{STD}$*	11	Terminal for switching between $5\frac{1}{4}$-inch and 8-inch floppy disks (with pull-up resistor). HIGH selects $5\frac{1}{4}$-inch floppies LOW selects 8-inch floppies.

Pin Name	Pin No.	Function
Vss1	12	Ground terminal for the digital system.
Vss2	13	Ground terminal for the analog system. (VCO ground)
CONTROL	14	Input terminal for the VCO (voltage controlled oscillator) control voltage.
OFFSET	15	Input terminal for offset voltage for VCO center frequency correction. An external capacitor tied to this pin generates offset voltage.
LPF1	16	Terminal for connecting the PLL system's loop filter. Selected when sync field is detected for frequency lock-in.
LPF2	17	Terminal for connecting the PLL system's loop filter. Selected when ID and DATA fields are detected after frequency lock-in.
TEST1	18	Test terminal fo testing functions (ordinarily not connected).
WCLK	19	Write clock for the μPD765 FDC. • 8-inch MFM : Interval T = 1 μs • 8-inch FM : Interval T = 2 μs • $5\frac{1}{4}$-inch MFM : Interval T = 2 μs • $5\frac{1}{4}$-inch FM : Interval T = 4 μs
CR	20	CR connection terminal for the timer circuit.
CLK2	21	FDC clock output terminal (for the MB8877 and FD1791). • f = 2MHz for 8-inch floppy disk • f = 1MHz for $5\frac{1}{4}$-inch floppy disk
$\overline{TRIG\ IN}$*	22	Trigger input terminal for the timer circuit (with pull-up resistor).
TM OUT	23	Retriggerable oneshot timer output terminal (Timer for head-load timing or motor-on signal, etc.)
VDD	24	+5V power supply terminal

NOTE : *Input terminals with pull-up resistors are pulled up through a standard resistance of 100K ohms. Since susceptibility to noise is increased by leaving terminals open, it is recommended that terminals which are to be kept HIGH be connected directly to VDD.

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5 to V_{DD}+0.3	V
Output voltage	V_O		
Operating temperature	T_{opr}	−10 to 60	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{SS}=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating supply voltage	V_{DD}	—	4.75	5.0	5.25	V
High level input voltage	V_{IH}	—	2.0	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}	—	−0.3	—	0.8	V
High level output voltage	V_{OH}	I_{OH}=−200μA	2.4	—	V_{DD}	V
Low level output voltage	V_{OL}	I_{OL}=2.0mA	0	—	0.4	V
High level input current*1	I_{IH1}	V_{IH}=V_{DD}	—	—	2.0	μA
Low level input current*2	I_{IL1}	V_{IL}=V_{SS} V_{DD}=5V	−100	−50	−10	μA
High level output current*3	I_{OH1}	V_{OH}=2.4V	—	—	−200	μA
Low level output current*4	I_{OL1}	V_{OL}=0.4V	2.0	—	—	mA
Current consumption	I_{DD}	Output open, V_{DD}=5V, 16MHz oscillation	—	—	10	mA

*1 HIGH input current for pins with pull-up resistors
*2 LOW input current for pins with pull-up resistors
*3 HIGH output current for driver output terminals
*4 LOW output current for driver output terminals

●AC Electrical Characteristics

(Standard frequency ; f_0=16MHz)

Parameter	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
Frequency	f_{CLK1}	CLK1	MIN/$\overline{STD}$=Low	—	8.0	—	MHz
			MIN/$\overline{STD}$=High	—	4.0	—	MHz
	f_{CLK2}	CLK2	MIN/$\overline{STD}$=Low	—	2.0	—	MHz
			MIN/$\overline{STD}$=High	—	1.0	—	MHz
Cycle time and Window width	t_{CYWCL} and t_{WHWIND}	WCLK and WINDOW	MIN/$\overline{STD}$=Low MFM/$\overline{FM}$=Low	—	2	—	μs
			MIN/$\overline{STD}$=High MFM/$\overline{FM}$=Low	—	4	—	μs
			MIN/$\overline{STD}$=Low MFM/$\overline{FM}$=High	—	1	—	μs
			MIN/$\overline{STD}$=High MFM/$\overline{FM}$=High	—	2	—	μs
High level width	t_{WHDT}	DATA	C_L=15pF	110	125	140	ns
High level width	t_{WHRD}	RD DATA	—	150	—	—	ns
VCO Oscillation frequency	f_{VCO}	—	CONTROL terminal=V_{DD}/2 External capacitance (0.1μF) connected to OFFSET terminal	3.8	4.0	4.3	MHz
VCO control voltage coefficient	K_V	—	|V_{DD}/2-CONTROL voltage|≦0.5V	1.0	1.2	1.4	MHz/V
Supply voltage rise time	V_R	—	Time for voltage to rise from 10% level to 90%	5	—	—	ms