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The Intel Processor Roadmap

Intel will make significant changes to its product roadmap in the next two years. New 32-bit processors will dramatically increase processor performance, and Intel will introduce the first 64-bit Intel Architecture (IA-64) processor coded-named Merced. This paper details some of the more important changes coming in 1999 and beyond that will affect industry-standard servers.

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The Intel Processor Roadmap
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INTRODUCTION

In 1998, Intel introduced the Deschutes processor core and migrated systems to a 100-MHz system bus. Several similar changes are targeted for 1999. Intel plans to continue segmenting the processor market, with different processor offerings for basic PC, performance PC, workstation/server, and mobile products. In 1999, Intel will launch a new 32-bit Intel Architecture (IA-32) processor core code-named Katmai. The Katmai core is based on the current Deschutes core, with added multimedia instructions and a 133-MHz system bus. Katmai processors will come in different variations for different market segments. The Katmai processors intended for high-end workstation and server users are code-named Tanner and Cascades. In addition to Katmai, Intel is continuing work on the Merced 64-bit (IA-64) processor.

Intel is also introducing new production processes in 1999. Current Pentium II and Pentium II Xeon processors use a 0.25-micron production process. The Cascades processor will be fabricated using a 0.18-micron technology. This technology will allow Intel to pack more circuits into each square millimeter of die size. One outcome of this technology advancement will be the ability to move the level-two (L2) cache memory back into the processor die.

.25 micron - refers to the smallest feature size on a solid state substrate. In general, the smaller the size, the faster the device can operate.

Figure 1 shows the current Intel roadmap. The roadmap shows that Intel intends to carry the IA-32 product line well into the next decade in parallel with the IA-64 line of processors.

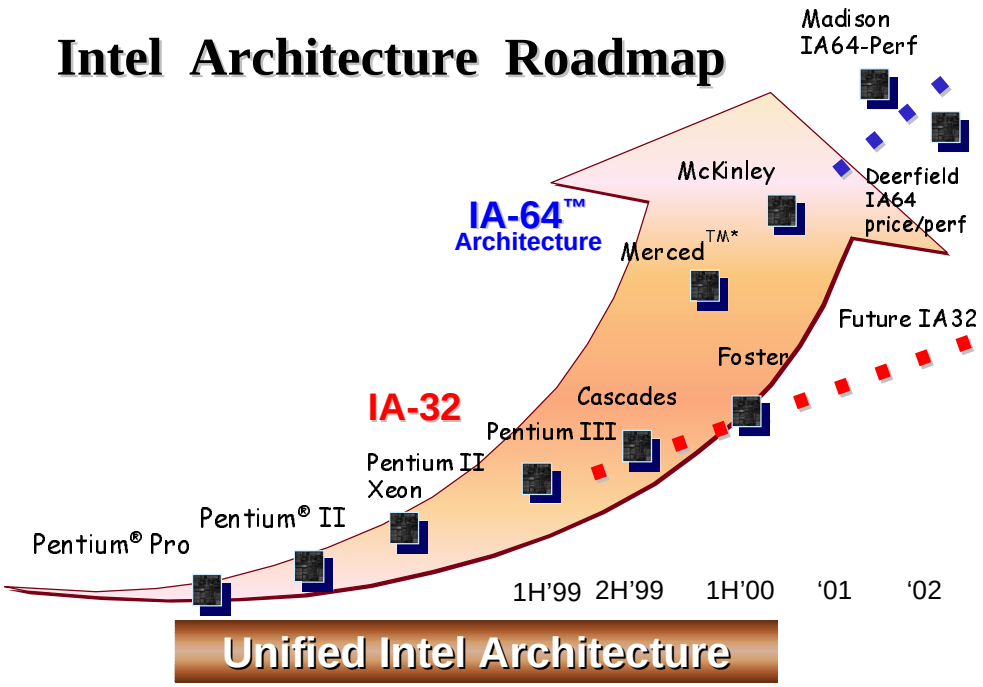

Figure 1. The Intel product roadmap through 2001. Intel will continue to develop IA-32 processors in parallel with IA-64 processors.

IA-32 PROCESSORS

The Pentium II Xeon processor is the current IA-32 standard for high-end workstations and enterprise-class servers. The Pentium II Xeon processor contains the Deschutes processor core and a 100-MHz system bus. The latest announcement from Intel is a 450-MHz version of the Pentium II Xeon with a 2-MB L2 cache.

Tanner/Cascades

In February 1999, Intel announced the Pentium III Xeon processor, code-named Tanner. The Tanner processor will have the following characteristics:

- 100-MHz system bus
- Full-speed cache on module
- 512K, 1M, and 2M L2 cache (not all cache sizes may be available at the product launch)
- 500 MHz core frequency
- Katmai New Instructions (KNI)
- 330-contact slot connector form factor (formerly called Slot 2)

Tanner will provide a Slot 2 upgrade path for the current Pentium II Xeon processor, with higher core speeds and a larger L2 cache size (2MB). Aside from speed and cache size increases, the main difference between the Pentium II and Pentium III Xeon processors will be the migration from the Deschutes core logic to the Katmai core logic.

Cascades will be a "shrink" of the Tanner circuitry, migrating from the current 0.25-micron process technology to 0.18-micron technology. This migration will allow Intel to move the L2 cache memory back onto the processor chip. The initial Cascades processors will have a full-speed 256-KB L2 cache and will use a faster 133-MHz system bus. Current Pentium II Xeon processors use a 100-MHz system bus. Because of the system bus speed increase, Cascades will not be a drop-in replacement for Pentium II Xeon or Tanner processors in most cases. System boards for Cascades products will be redesigned to accommodate the higher bus speeds.

Katmai Core Logic

Tanner and Cascades will have the new Katmai core logic. The Katmai core logic adds the following enhancement features to the existing Deschutes core:

- Memory Streaming
- Concurrent Single Instruction Multiple Data – Floating Point (SIMD-FP)
- 70 new multimedia instructions (KNI)

Memory Streaming

Memory streaming is a set of techniques that increase the utilization of the memory bus during memory reads and writes. Currently, processors must frequently wait for data to be retrieved from system memory. Because the system bus connecting the memory to the processor is slower than the processor's core speed, this results in a performance bottleneck. Katmai's memory streaming enables the processor to pre-fetch data from system memory into cache memory. To use this feature, software programmers must rewrite their code to take advantage of these new instructions.

During writes to memory, other new instructions can tell the processor to write data back directly to memory, bypassing the L2 cache. Bypassing the L2 cache frees up more room in the cache for additional data. This technique would be useful in the case when the software programmer knows in advance that the data will not be reaccessed in the near future. As with pre-fetching, software must be rewritten to take advantage of this instruction.

Concurrent SIMD-FP

Concurrent SIMD-FP applies the same architecture used by MMX for integer operations to floating-point numbers. Floating-point numbers are used extensively in 3D graphics and scientific computations. Katmai processors have eight new registers that can each hold 4 single-precision floating-point numbers. Once the registers are filled, a single instruction can be used to add, subtract or do other operations between the registers. For example, eight floating-point numbers could be added together using one instruction call.

KNI

KNI refers to the addition of 70 new instructions to the MMX instruction set. The new instructions primarily refer to the new SIMD-FP registers, but some new integer instructions also have been added. The new instructions are particularly useful for multimedia applications, such as 3D rendering and video encoding and decoding.

Foster

Xeon and Katmai provide extensions and improvements to the existing sixth-generation IA-32 architecture. In the second half of 2000, Intel is scheduled to launch their seventh-generation architecture. Code-named Willamette, the new architecture will have increased performance over Katmai processors at the same clock speed. Willamette will have

- 512-KB, 1-MB, and 2-MB L2 caches
- A 64-bit data bus capable of providing 3.2 GB/s of bandwidth

Willamette processors will appear in desktops, servers and workstations. The server version has the code name Foster.

IA-64 PROCESSORS

Intel is currently working on a 64-bit architecture to complement their 32-bit architecture. The following sections describe the IA-64 processors now under development.

Merced

EPIC – Explicitly Parallel Instruction Computing

RISC – Reduced Instruction Set Computing

VLIM – Very Long Instruction Word

The first 64-bit processor, code-named Merced, is scheduled for production in the second half of 2000. The Merced processor uses the EPIC architecture. The EPIC architecture is based on RISC and VLIW systems, but is significantly different from either of those two architectures. Current IA-32 processors use hardware within the processor to make decisions on which instructions can be executed simultaneously. EPIC-based processors rely primarily on software compilers to provide information needed to efficiently execute parallel instructions. However, the EPIC architecture will allow for some dynamic hardware-based speculation.

IA-64 is a combination of existing x86 instructions and new 64-bit instructions. Merced will translate the x86 instructions into native 64-bit instructions. Because the translation will create a performance penalty when running existing software, software will have to be recompiled to take advantage of any Merced performance improvements. Initially, the only performance advantage a Merced will have over a Foster processor will be on recompiled floating-point code.

Merced processors will also debut in a new mechanical form factor called Slot M. Slot M is designed to offer four times more bus bandwidth than the current Slot 2 design used in Pentium II Xeon processors.

McKinley

McKinley is the second generation IA-64 processor, currently scheduled to announce during the second half of 2001. McKinley processors are predicted to dramatically improve over the first generation of IA-64 processors. McKinley is projected to have twice the processing performance and three times the bus bandwidth of Merced.

CONCLUSION

The next two years will mark dramatic increases in the processing capability of Intel processors. Newer and more powerful 32-bit processors will provide additional horsepower to current Compaq industry-standard workstations and server products. The advent of IA-64 processors will accelerate the move to 64-bit computing which began in 1992 with Digital Equipment Corporation's Alpha processor.

Processor architecture is only one factor in the system performance equation – albeit an important one. Compaq delivers the best price/performance industry-standard workstations and servers by carefully designing its products to have the lowest total cost of ownership, highest system performance and best availability.