EMULOGIC™

68000

User's Guide Supplement

Additional system specifications and
details concerning the use and operation of
Emulogic equipment and software are included
in various technical manuals available
through local sales representatives.

This document supplements the ECL-3211 System User's Guide by providing operational information specific to the emulation of Motorola's 68000 and compatible microprocessors. This document describes special set-up procedures, conditions, and limitations to be noted when emulating the 68000. It is assumed here that the reader has read the User's Manual and is already familiar with the details of the 68000. Ready access to the technical literature is a plus.

This supplement covers five general areas.

*** INSTALLATION ***

System installation instructions will be found in the User's Manual.

Note that the 10 MHz 68000 requires a Dual Connector Card on the ECL-3211's High Speed Memory. Instructions for installation of the 10 MHz Dual Connector Card will be found in the System installation section in the User's Guide.

*** INITIALIZATION ***

Type on the keyboard "RUN L01200" to load the Emulation Software into the ECL-3211. Note that a user can use the Operating System's RENAME function to give the file a name the user would prefer. Additionally, a Command File can be created causing L01200 to run.

There are no special initialization instructions for the 68000.

SYSTEM DISPLAY

These are seen on the top half of the display when using the Emulation
Software. All of these registers and flags can be loaded with user prefered
values with the SET Command or ALTER mode as described in the User Manual or
HELP file.

***	*** DESCRIPTION ***	
D0 - D7	Data Registers 0-7	32 bits/8 hex digits
PC	Program Counter	24 bits/6 hex digits
A0 - A6	Address Registers 0-6	32 bits/8 hex digits
US	User Stack Pointer	32 bits/8 hex digits
SS	Supervisor Stack Pntr	32 bits/8 hex digits
T	Trace Mode Flag	bit 15
S	Supervisor/User Mode Flag	bit 13
I	Interrupt Mask	octal decode of bits 8,9,10
X	Extend Flag	bit 4
N	Negative	bit 3
Z	Zero	bit 2
V	Overflow	bit 1
C	Carry	bit 0
SR	Status Register	16 bits/4 hex digits

TRACE DISPLAY   Note: Low=0   High=1   Don't Care=X

                                "1" and "0" refer to ELECTRICAL,
                                NOT logical levels; though for
                                ECL-3211 functions logical and
                                electrical coincide.

These are seen when examining the Trace.

***   *** DESCRIPTION ***

F   Function Code;   FC0,FC1,FC2 decoded
C

B   BGACK-L; Bus Grant Acknowledge
A

B   BG-L; Bus Grant
G

B   BR-L; Bus Request
R

B   BERR-L; Bus Error
E

I   Interrupt Priority;   IPL0-L,IPL1-L,IPL2-L decoded
P

V   VMA-L; Valid Memory Address
M

V   VPA-L; Valid Peripheral Address
P

U   UDS-L; Upper Data Strobe
D

E   Enable

L   LDS-L; Lower Data Strobe
D

R   RESET-L
S

H   HALT-L
L

R   R/W-L; Read/Write
W

I   Instruction Fetch

BREAKPOINT DISPLAY   Note: Low=0   High=1   Don't care=X

These are seen when examining or setting Breakpoints.

E0-E7	Pod External Input 0-7
SW1	Logical Switch 1
	External Trigger 1
SW2	Logical Switch 2
	External Trigger 2
SW3	Logical Switch 3
SW4	Logical Switch 4

INS   Instruction Fetch; this is a signal generated by the
             Emulator. A "1" indicates the fetch of
             the first byte/word of an Op Code as a
             Breakpoint Condition.

ROM   ROM access; "1" means trigger on a read from an address
             designated as ROM.

CO1	Counter 1 expired (CO1=0)
CO2	Counter 2 expired (CO2=0)

ADDR	Address Bus; 24 bits (UDS is A0)
DATA	Data Bus; 16 bits
E	Enable (output)
FC0	Function Code 0
FC1	Function Code 1
FC2	Function Code 2
HALT	HALT-L
RESET	RESET-L

LDS	Lower Data Strobe-L
VMA	Valid Memory Address-L
VPA	Valid Peripheral Address-L
RW	Read/Write-L

IPL0	Interrupt Priority Level 0-L
IPL1	Interrupt Priority Level 1-L
IPL2	Interrupt Priority Level 2-L

BGACK	Bus Grant Acknowledge-L
BG	Bus Grant-L
BR	Bus Request-L
BERR	Bus Error-L

PH   Phantom Status; JUMP or CALL
             Note: this is a Breakpoint Action rather
             than a Breakpoint Condition.

L01200

The file name for the Emulation Software is L01200. It is accessed through the Operating System hosted by the ECL-3211's CPU.

MAX FREQ

The maximum specified frequency of operation without WAIT states in Maps 1-4 or Target memory is 8 MHz for the 8 MHz 68000 and 10 MHz for the 10 MHz 68000. (Map 0 must be off.)

For operation in Map 0 without WAIT states, the maximum frequency is 6 MHz for both 8 MHz and 10 MHz 68000 Pods.

Both 8 MHz and 10 MHz 68000 Pods must be clocked at 4 MHz to use DEC Internal Memory. There will be WAIT states using this bank of memory.

Minimum operating frequency for both products is 4 MHz.

RESET

The ECL-3211's RESET command resets the 68000 Pod only, and does not reset the Target. A Reset generated by the Target or the User's program has effect during emulation only.

HALT

Whether internally or externally generated, a HALT condition must be serviced by the user. The 68000 Pod has no facility for terminating a HALT condition, and if Emulation mode is left while the 68000 Pod is in a HALT condition, all register settings will be lost.

NO TARGET

Not having the 68000 Pod deployed in a target will not affect the operation of the Emulator in any way, assuming the user does not try to access resources in the Target.

TRACE DATA CAPTURE

If the Trace has been turned on, it takes a "snapshot" of conditions during each Machine Cycle when the conditions are valid. For example, the Data bus is sampled when it contains valid Data. Address information is sampled when there is a valid Address on the bus. Control signals are sampled at the same time as the Data unless they must be sampled at a different point in the Machine Cycle. (The Trace is turned on by defining a Breakpoint with conditions that will be met and an Action statement including Set Trace, as described in the User's Guide and HELP file.)

Instructions are disassembled in the Trace as they appeared on the Data bus when they were fetched.

In the event that a Branch or Jump instruction is executed, the word that was Prefetched will appear in the Trace. If the word is a complete instruction, it will be disassembled. If the word is the first word of a multi-word instruction, the Trace Incomplete notation, "--T.I.--", will appear.

Note that the External Inputs are not sampled simultaneously in a Machine Cycle. External Inputs 0-3 are sampled during the valid address time of a Machine Cycle and External Inputs 4-7 are sampled during valid data time.

BREAKPOINT ACTION

Defined Breakpoint conditions are tested and resolved at the end of the Machine Cycle. Any Breakpoint Actions for a Breakpoint with conditions that have been met in a Machine Cycle commence at the completion of that Machine Cycle. For the action of SET TRACE (ST), the Trace will not start to record activity until the next instruction fetch.

--E.C.--

In the Trace Buffer under the column titled "Instruction", there will be entries titled "--E.C.--". "EC" stands for Emulation Cycle and represents cycles used to purge the 68000's instruction pipeline when control is transfered back to the Emulator. This appears in the Trace Buffer when emulation is stopped due to user action from the keyboard, or when a valid and active Breakpoint has as a defined action a Pause or a Halt. It does not affect the timing of a program in any way.

CLOCK

The Emulator provides two sources (Emulator and Target) and three different modes of providing a clock signal to the 68000 Pod; External, Internal, Internal source with external drive (Internal Drive). Both modes of Internal clock have a guarantee for 100 Kilohertz resolution.

--- External ---

External Clock is the mode in which the Target Circuit (the circuit the Pod is deployed in) provides the clock. Since it is buffered in the Pod with TTL logic, the clock signal must be TTL driven or equivalent. Do not clock the Pod with a Crystal/RC Network circuit.

Type "FREQ EXT" to select this mode.

--- Internal ---

Internal Clock is the mode in which the 68000 Pod is clocked by the Emulator. No clocking signal is taken from or given to the Target. Pin 15 (CLK) on the Pod's Target Cable Plug is electrically disconnected.

Type "FREQ xxxx" to select the Internal Clock mode. "xxxx" is the value of the frequency in units of Kilohertz. There is no need to specify "Internal" at any point.

--- Internal Drive ---

Internal Drive is the mode in which the 68000 is receiving its clock from the Emulator (as in Internal) but the signal the Pod's 68000 is receiving is also connected to Pin 15 (CLK) on the Target Cable Plug for use by the Target circuit. In this way, other components can be driven from the same clock that drives the Pod's 68000 and thus the entire Target Circuit can be provided with a software controllable clock.

Type "FREQ xxxx IND" to select Internal Drive mode. "xxxx" is the value of the frequency in units of Kilohertz.

SET COMMAND

Register values can be altered to user preferred values prior to emulation when in Command mode. The format used is described in the User's Manual or the HELP file. The abbreviations used to refer to the 68000's registers are listed above in the section on Abbreviations under System Display. The Abbreviations on the screen representing the registers are basically those used to change the register's contents. Note that the ECL-3211 provides two ways of changing the contents of Registers or other parameters as discussed in the User's Guide: ALTER mode and the SET command. The later is discussed here.

To illustrate, consider the following examples:

a) Typing "SE D0=12345678" will change the contents of Data Register 0 to "12345678".

b) Typing "SE A0=12345678,A6=87654321" will change the contents of Address Register 0 to "12345678" and the contents of Address Register 6 to "87654321".

c) Typing "SE MEM 123=5555" will change the contents of Memory address 000123 to "5555".

d) Typing "SE MEM 1500=1111,2222,3333" will change the contents of Memory addresses 001500 to "1111", 001502 to "2222", 001504 to "3333".

e) Typing "SE MEM 0-7FE=AA" will change the contents of Memory addresses 00000000 through 0007FE inclusive with "00AA".

f) Typing "SE MEM 0-0=AA" will set only Memory address 000000.

BYTE/WORD

The ECL-3211 has two modes of transfering data to and from a Target, BYTE or WORD. This is relevant when using the SET or LOAD commands to write values to addresses that are physically present in the Target. Data can be read or written to the Target in bytes or words to provide compatibility with the I/O components in the Target. To illustrate, a Target using 6800 family I/O components should use BYTE mode. A Target with I/O components that are designed for a 16 bit Data Bus should use WORD mode.

The existing mode is indicated in the Switch display on the line labeled ".EXTERNAL FETCH/PUT". (To access the Switch display, type "SW" while in Command mode.) To select the mode of data transfers, type "WORDS" or "BYTES" when the Emulator is in Command mode. The HELP file sections can be accessed by typing "HE WO" for Word mode, or "HE BY" for Byte mode. The default is BYTE.

PHANTOMS

To branch to a Phantom code segment when a defined set of Breakpoint conditions are met, a user must 1) define Phantom as being a Breakpoint Action for the defined conditions and 2) select the mode of Phantom. The 68000 Emulator offers the user a choice as to the mode of Phantom to be employed; JUMP or CALL.

The choice is implemented when the Emulator is in Command Mode. Type "BR n CALL" or "BR n JMP" as appropriate, where "n" is the number identifying which Breakpoint is being defined. To illustrate, type "BR 3 JMP" to select JUMP mode for a Phantom defined in Breakpoint 3. Remember that to take a Phantom, a user must specify a Phantom as a Breakpoint Action.

The choice of CALL for one Breakpoint does not prevent a user from selecting JUMP for a different Breakpoint.

For a Phantom CALL, 1) the value of 6 should be subtracted from the the value pointed to by the Stack Pointer to adjust the stored PC to return to the address where the Phantom was inserted 2) the user code should be terminated with an RTS instruction. To illustrate, below is an example of the last instructions of a Phantom:

```
        .
        .
        .
    SUBQ.L #6,(SP)      /5D97
    RTS                 /4E75
```

DTACK (Rev 4+)

This section is for User's with Rev. 4.00 or later Emulation Software.

To ease product and software development, the 68000 Emulator offers three options for providing the 68000 with DTACK. There is also the option to choose the number of WAIT states (up to 14) the Emulator will delay its generation of DTACK to simulate memory banks of varying access times. Note that this feature is not available for Map 0.

The DTACK signal the 68000 Pod receives can be sourced:
    1) from the ECL-3211 alone
    2) from the Target alone
    3) from whichever DTACK is received later --the ECL-3211's or
         the Target's.

If the third option is selected, the 68000 Pod waits for both DTACKs to be present to create the effect that the one that is issued last is the one that is responded to by the 68000 Pod. This provides a margin of safety for "slow" RAM in the Target to prevent the premature termination of Read and Write operations.

Note that any reference to External (Target) Memory will automatically use the Target's DTACK for the duration of those references. The user's DTACK selection will be preserved.

When sourcing DTACK from the Target, a 5 microsecond timer will always be present on every machine cycle. If the Target does not generate the DTACK, the Watchdog Timer will.

The DTACK configuration is found in the Switch display (accessed while the Emulator is in Command mode). Changes are made while in Command mode.

Type "DTA ECL" to select the ECL-3211 as the source of DTACK.

Type "DTA TAR" to select the Target as the source of DTACK.

Type "DTA TAR,ECL" or "DTA ECL,TAR" to select the later of the Target's or the Emulator's DTACK.

Type "WAIT ON" to enable the Emulator's delay of DTACK when referencing the Emulator's High Speed Memory. Type "WAIT OFF" to disable this feature. This feature is normally disabled.

To select the number WAIT states (up to 14) the ECL-3211 will delay its DTACK, use the syntax "WAIT XX=YY" where XX is the Map Number and YY is the number of desired WAIT states. Type "WAIT 1=14" to select a delay of 14 WAIT states in DTACK generation for any access to user defined Map 1. (Note that this is the maximum number of WAIT states possible.) Type "WAIT 3=2" to select a delay of 2 WAIT states for any access to user defined Map 3. Note that Map 0 will not support the selectable WAIT state feature.

DTACK (Rev. 1, 2, and 3)

This section is for User's with Revisions 1.xx, 2.xx, or 3.xx of the Emulation Software.

To ease product and software development, the 68000 Emulator offers three options for providing the 68000 Pod with DTACK. There is also the option to choose the number of WAIT states (up to 14) the Emulator will delay its generation of DTACK to simulate memory banks of varying access times. Note that this feature is not available for Map 0.

The DTACK signal the 68000 receives can be sourced:
     1) from the ECL-3211 alone
     2) from the Target alone
     3) from whichever DTACK is received later --the ECL-3211's or
          the Target's.

If the third option is selected, the 68000 Pod waits for both DTACKs to be present to create the effect that the one that is issued last is the one that is responded to by the 68000 Pod. This provides a margin of safety for "slow" RAM in the Target to prevent the premature termination of Read and Write operations.

Note that any reference to External (Target) Memory will automatically use the Target's DTACK for the duration of those references. The user's DTACK selection will be preserved.

When sourcing DTACK from the Target, a 5 microsecond timer will always be present on every machine cycle. If the Target does not generate the DTACK, the Watchdog Timer will.

The DTACK configuration is found in the Switch display (accessed while the Emulator is in Command mode). Changes are made while in Command mode.

     SW A   Enables Target DTACK
     SW B   Disables ECL-3211 DTACK, enables Target DTACK
     SW C   Enables ECL-3211 programmed WAIT states to permit
               simulation of banks of RAM with varying Access Times

The allowed combinations of DTACK switch settings are:

*** SWITCH ***			*** DTACK ***
A	B	C	
0	0	0	-- ECL only
1	0	0	-- the later of ECL-3211 or Target
1	1	0	-- Target only
1	0	1	-- the later of (ECL-3211 + WAIT) or Target

To select the number of WAIT states (up to 14) the ECL-3211 will delay its DTACK, use the syntax "WAIT XX=YY" where XX is the Map Number and YY is the number of desired WAIT states. Type "WAIT 1=14" to select a delay of 14 WAIT states in DTACK generation for any access to user defined Map 1. (Note that this is the maximum number of WAIT states possible.) Type "WAIT 3=2" to select a delay of 2 WAIT states for any access to user defined Map 3. Note that Map 0 will not support the selectable WAIT state feature.

NOT EMULATING

When the Emulator is not in Emulation mode, a number of 68000 signals remain active. They are listed here:

A1-A23	(pins 29-48, 50-52)
R/W-L	(pin 9)
LDS-L	(pin 8)
UDS-L	(pin 7)
AS-L	(pin 6)
FC0,FC1,FC2	(pins 26-28)
E	(pin 20)
BG-L	(pin 11)
VMA-L	(pin 19)
VPA-L	(pin 21)
BR-L	(pin 13)
DTACK-L	(pin 10)
BGACK-L	(pin 12)

CLK (pin 15) will be generated when not in Emulation mode if Internal Drive is selected as the Clocking mode.

D0-D16 (pins 1-5, 54-64) will be Tri-Stated.

HALT-L (pin 17) and RESET-L (pin 18) will be open.

IPL0, IPL1, and IPL2 (pins 23-25) will be pulled High.

BERR-L (pin 22) will be pulled High.

*** ELECTRICAL (DC) CHARACTERISTICS ***

Signal	Buffer Type	Output Drive		Input Load		Delay, additional	Termination, pull-up R
	74xxx	High mA	Low mA	High mA	Low mA	nSec typical	ohms
A1-A23	LS245	-15.0	64.0	0.07	-1.0	7	--
D0-D16	LS245	-15.0	64.0	0.07	-1.0	7	--
R/W-L	LS245	-15.0	64.0	--	--	7	10K
LDS-L	LS245	-15.0	64.0	--	--	7	10K
UDS-L	LS245	-15.0	64.0	--	--	7	10K
AS-L	LS245	-15.0	64.0	--	--	7	10K
FC0	LS245	-15.0	64.0	--	--	7	10K
FC1	LS245	-15.0	64.0	--	--	7	10K
FC2	LS245	-15.0	64.0	--	--	7	10K
E	F241	-15.0	64.0	--	--	7	--
VMA-L	LS245	-15.0	64.0	--	--	7	--
BR-L	F241	--	--	0.02	-1.6	7	1K
DTACK-L	F08	--	--	0.02	-0.6	21	1K
IPL0-2	F32	--	--	0.02	-0.6	7	10K
VPA-L	F32	--	--	0.02	-0.6	7	10K
BERR-L	F32	--	--	0.02	-0.6	7	10K
BGACK-L	F241	--	--	0.02	-1.6	7	1K
Clock, Ext	F253	--	--	0.02	-0.6		1K
Clock, Int Dr	F253	-1.0	20.0	--	--		1K
BG-L	none; it is driven directly by the Pod's 68000						1K
HALT-L	CD4066 analog switch; negligible loading						1K
RESET-L	CD4066 analog switch; negligible loading						1K