

Peripheral Notes:

- 1. Within console.
- 2. Separate housing, power from console
- 3. Separate housing, separate power

Only one rigid disk can be connected at one time. SA4xxx kit cables directly into the Workstation w/connector.

PWBA Connector Notes:

Type	
P11	
P12	
P13	713W12720 (XEROX) 40 POS.
P14	20 PIN I.C. SOCKET
P15	713W12220 (XEROX) 10 POS.
P21	713W12720 (XEROX) 40 POS.
P22	713W12820 (XEROX) 50 POS.
P41	713W12220 (XEROX) 10 POS.
P42	
P43	

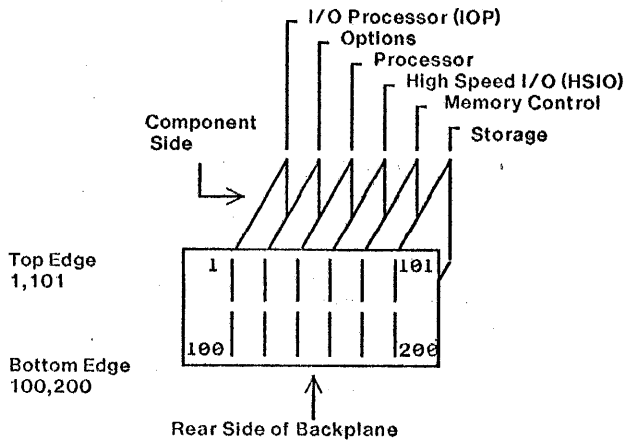
connector panel on rear of console

Connector Panel Notes:

- 1 D Series 25 Pin Socket
- 2 D Series 50 Pin Socket
- 3 D Series 25 Pin Socket
- 4 D Series 25 Pin Plug
- 5 D Series 25 Pin Socket
- 6 D Series 25 Pin Socket
- 7 D Series 25 Pin Socket
- 8 Kit

Dandelion Backplane

Physical arrangement



Files

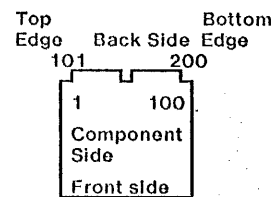
[Iris]<Workstation>Backplane>
Backplane-B.press
Backplane-B.dm

Backplane Signals

Card	IOP	Options	Central Processor	High Speed I/O	Memory Control	Storage	
Total Signal lines used	131	166	140	141	155	66	170 max per card
I/O Connectors on front of boards	Floppy Keyboard Printer MaintenanceP Alto umb.	LSEP/Ethernet RS232/RS366		SA4XXX SA100X Display			

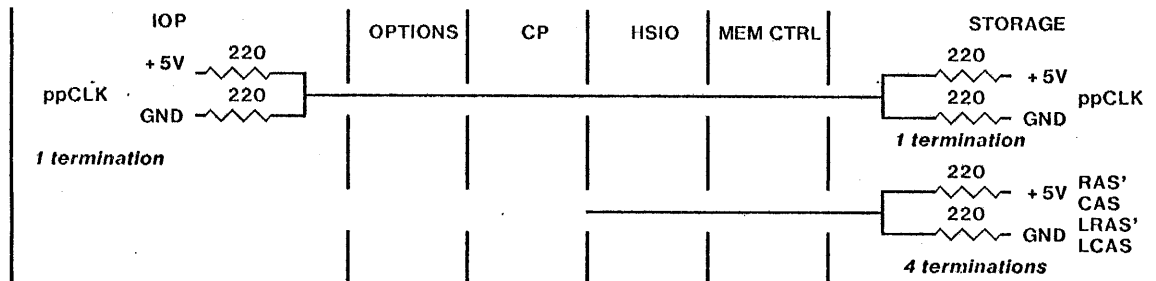
Power distribution

Backplane Power & Ground		30 lines total
Voltage	Backplane Pins	
+ 12 V	1,101	
+ 5 V	50,51,150,151	
Gnd	10,20,30,40,60,70,80,90,110,120,130,140,160,170,180,190	
- 5V	100,200	
- 12 V	98,198	
No Conn.	97,99,197,199	



2- 100 pin connectors
Pins on .1" centers
.6" between pins 50 & 51
AMP # 530826-3

Termination of clock signals



Terminations are placed on the IOP and STORAGE cards.

XEROX SDD	Project Dandelion	Backplane Description General Characteristics	File WSBackplane.sil	Designer Ogus	Rev B	Date 2/19/80
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IOP		OPTIONS		CP		HSIO		
02		02	Cycle.1'	02	Cycle1'	02	Cycle1'	02
03		03	Cycle.2'	03	Cycle2'	03	Cycle2'	03
04		04	Cycle.3'	04	Cycle3'	04	Cycle3'	04
05	Spare22	05	Spare22	05	Spare22	05	RAS'	05
06	IOPALE	06	IOPALE	06	IOPALE	06	CAS	06
07	Spare20	07	Spare20	07	Spare20	07	WPulse	07
08	Spare18	08	Spare18	08	Spare18	08	ppCLK	08
09	ppCLK	09	ppCLK	09	ppCLK	09	ppCLK	09
11	Spare16	11	Spare16	11	AllowWrite	11	AllowWrite	11
12	IOPClk	12	IOPClk	12		12		12
13	Spare14	13	Spare14	13	MAR←	13	MAR←	13
14	Spare12	14	Spare12	14	←MStatus'	14	←MStatus'	14
15	Spare10	15	Spare10	15	MapRef	15	MapRef	15
16	SelTroyMode	16	SelTroyMode	16	Refresh'	16	Refresh'	16
17	Wait	17	Wait	17	IOPReset'	17	Wait	17
18	TrIndex	18	TrIndex	18	Spare26	18	Spare26	18
19	TrReady	19	TrReady	19	Spare24	19	Spare24	19
21	IOPData←'	21	IOPData←'	21	IOPData←'	21	IOPData←'	21
22	TrTK00	22	TrDirIn	22	KData←'	22	KData←'	22
23	XData←'	23	XData←'	23	XData←'	23	XData←'	23
24	TrWrProt	24	TrWrGate	24	DCTlFifo←'	24	DCTlFifo←'	24
25	TrRdData	25	TrWrData	25	DBorder←'	25	DBorder←'	25
26	IOOutSp1←'	26	IOOutSp2←'	26	IOOutSp1←'	26	IOOutSp2←'	26
27	IOOutSp3←'	27	IOOutSp4←'	27	IOOutSp3←'	27	IOOutSp4←'	27
28	POData←'	28	PData←'	28	POData←'	28	POData←'	28
29	Spare6	29	Spare7	29	Spare6	29	Spare7	29
31	←XIData'	31	←XStatus'	31	←XIData'	31	←XStatus'	31
32	Spare4	32	Spare4	32	←KIData'	32	←KStatus'	32
33	←IOPIData'	33	←IOPStatus'	33	←PStatus'	33	←PStatus'	33
34	←IOInSp2'	34	←IOInSp2'	34	←IOPIData'	34	←IOPStatus'	34
35	Spare2	35	Spare2	35	←IOInSp2'	35	←IOInSp2'	35
36	CSParErr	36	EndLine'	36	ClrRefReq'	36	ClrRefReq'	36
37	IODisp.0	37	IODisp.0	37	Spare3	37	Spare3	37
38	YIODisp.0	38	YIODisp.0	38	CSParErr	38	EndLine'	38
39	X.0	39	X.1	39	IODisp.0	39	IODisp.0	39
41	X.0	41	X.1	41	YIODisp.0	41	YIODisp.0	41
42	X.2	42	X.3	42	X.0	42	X.1	42
43	X.4	43	X.5	43	X.2	43	X.3	43
44	X.6	44	X.7	44	X.4	44	X.5	44
45	X.8	45	X.9	45	X.6	45	X.7	45
46	X.10	46	X.11	46	X.8	46	X.9	46
47	X.12	47	X.13	47	X.10	47	X.11	47
48	X.14	48	X.15	48	X.12	48	X.13	48
49	Y.0	49	Y.1	49	X.14	49	X.15	49
					Y.0		Y.1	
52		52	Y.2	52	Y.2	52	Y.2	52
53		53	Y.4	53	Y.3	53	Y.3	53
54		54	Y.6	54	Y.4	54	Y.4	54
55		55	Y.8	55	Y.5	55	Y.5	55
56		56	Y.10	56	Y.6	56	Y.6	56
57		57	Y.12	57	Y.7	57	Y.7	57
58		58	Y.14	58	Y.8	58	Y.8	58
59	DmaReqC	59	DmaAckC	59	Y.9	59	Y.9	59
61	DmaReqA	61	DmaAckA	61	Y.10	61	Y.10	61
62	DmaReqB	62	DmaAckB	62	Y.11	62	Y.11	62
63	DmaCycle	63	ExtWaitReq'	63	Y.12	63	Y.12	63
64	IOPIntReq0	64	IOPIntReq1	64	Y.13	64	Y.13	64
65	IOPIntReq2	65	IOPIntReq3	65	Y.14	65	Y.14	65
66	IOPSel.0	66	IOPSel.1	66	Y.15	66	Y.15	66
67	IOPSel.2	67	IOPSel.3	67	YH.0	67	YH.0	67
68	IOPSel.4	68	IOPSel.5	68	YH.1	68	YH.1	68
69	IOPAddr.00	69	IOPAddr.01	69	YH.2	69	YH.2	69
71	IOPAddr.02	71	IOPAddr.03	71	YH.3	71	YH.3	71
72	IOPAddr.04	72	IOPAddr.05	72	YH.4	72	YH.4	72
73	IOPAddr.06	73	IOPAddr.07	73	YH.5	73	YH.5	73
74	IOPAddr.08	74	IOPAddr.09	74	YH.6	74	YH.6	74
75	IOPAddr.10	75	IOPAddr.11	75	YH.7	75	YH.7	75
76	IOPAddr.12	76	IOPAddr.13	76	Pt.0	76	Pt.0	76
77	IOPAddr.14	77	IOPAddr.15	77	Pt.1	77	Pt.1	77
78	Spare0	78	Spare1	78	Pt.2	78	Pt.2	78
79	IOPMemRd'	79	IOPMemRd'	79	Disp-Proc'	79	MemErr	79
81	CSWE.a'	81	CSWE.b'	81	Disp-Proc'	81	MemErr	81
82	CSWE.c'	82	CSWE.d'	82	DAddr.0	82	DAddr.0	82
83	CSWE.e'	83	CSWE.f'	83	DAddr.2	83	DAddr.1	83
84	IOPReq'	84	ClrIOPReq'	84	DAddr.4	84	DAddr.3	84
85		85	DPReq'	85	DAddr.6	85	DAddr.5	85
86		86	XReq'	86	DAddr.8	86	DAddr.7	86
87	IOPMemWr'	87	IOPMemWr'	87	DAddr.10	87	DAddr.9	87
88	RefReq'	88	ReadCSEn'	88	DAddr.12	88	DAddr.11	88
89	SpareReq'	89	IOPWait	89	DAddr.14	89	DAddr.13	89
91	WrTPCHigh'	91	WrTPCLow	91	DData.0	91	DData.1	91
92	IOPData.0	92	IOPData.1	92	DData.2	92	DData.2	92
93	IOPData.2	93	IOPData.3	93	DData.4	93	DData.3	93
94	IOPData.4	94	IOPData.5	94	DData.6	94	DData.4	94
95	IOPData.6	95	IOPData.7	95	DData.8	95	DData.5	95
96	SwTAddr	96	SwTAddr'	96	DData.10	96	DData.6	96

1-100 101-200 1-100 101-200 1-100 101-200 1-100 101-200

Above diagram is rear view (wiring side) of backplane.
ALL NUMBERS ARE IN DECIMAL.

Dandelion Backplane Signals - 1

Stamen1-4.sil in: [Iris]<Workstation>Backplane>Backplane-B.dm

Rev	B	2/19/80
Ogus		1:17 p

MEM CTRL

STORAGE

02	Cycle1'		02		02
03	Cycle2'		03		03
04	Cycle3'		04		04
05	RAS'	LRAS'	05	RAS'	LRAS'
06	CAS	LCAS	06	CAS	LCAS
07	WPulse	DR/C	07		
08			08		
09	ppCLK		09	ppCLK	
11	AllowWrite		11		
12	Bank0'		12	Bank0'	
13	MAR←	mem	13		
14		←MStatus'	14		
15	MapRef	Mctl←'	15		
16	Refresh'	CRefresh'	16	Refresh'	CRefresh'
17	Wait		17		
18	SDO.00	SDO.01	18	SDO.00	SDO.01
19	SDO.02	SDO.03	19	SDO.02	SDO.03
21	SDO.04	SDO.05	21	SDO.04	SDO.05
22	SDO.06	SDO.07	22	SDO.06	SDO.07
23	SDO.08	SDO.09	23	SDO.08	SDO.09
24	SDO.10	SDO.11	24	SDO.10	SDO.11
25	SDO.12	SDO.13	25	SDO.12	SDO.13
26	SDO.14	SDO.15	26	SDO.14	SDO.15
27	SDO.16	SDO.17	27	SDO.16	SDO.17
28	SDO.18	SDO.19	28	SDO.18	SDO.19
29	SDO.20	SDO.21	29	SDO.20	SDO.21
31			31		
32	SAddr.00	SAddr.01	32	SAddr.00	SAddr.01
33	SAddr.02	SAddr.03	33	SAddr.02	SAddr.03
34	SAddr.04	SAddr.05	34	SAddr.04	SAddr.05
35	SAddr.06	SAddr.07	35	SAddr.06	SAddr.07
36	Y1Latch	YOLatch	36	Y1Latch	YOLatch
37	Bank1'	Bank2'	37	Bank1'	Bank2'
38	MRef'	Write'	38	MRef'	Write'
39			39		
41	X.0	X.1	41		
42	X.2	X.3	42		
43	X.4	X.5	43		
44	X.6	X.7	44		
45	X.8	X.9	45		
46	X.10	X.11	46		
47	X.12	X.13	47		
48	X.14	X.15	48		
49	Y.0	Y.1	49		
52	Y.2	Y.3	52		
53	Y.4	Y.5	53		
54	Y.6	Y.7	54		
55	Y.8	Y.9	55		
56	Y.10	Y.11	56		
57	Y.12	Y.13	57		
58	Y.14	Y.15	58		
59	YH.0	YH.1	59		
61	YH.2	YH.3	61		
62	YH.4	YH.5	62		
63	YH.6	YH.7	63		
64	Pt.0	Pt.1	64		
65	Pt.2		65		
66	Disp-Proc'	MemErr	66		
67	DAddr.0	DAddr.1	67		
68	DAddr.2	DAddr.3	68		
69	DAddr.4	DAddr.5	69		
71	DAddr.6	DAddr.7	71		
72	DAddr.8	DAddr.9	72		
73	DAddr.10	DAddr.11	73		
74	DAddr.12	DAddr.13	74		
75	DAddr.14	DAddr.15	75		
76	DData.0	DData.1	76		
77	DData.2	DData.3	77		
78	DData.4	DData.5	78		
79	DData.6	DData.7	79		
81	DData.8	DData.9	81		
82	DData.10	DData.11	82		
83	DData.12	DData.13	83		
84	DData.14	DData.15	84		
85	SDI.20	SDI.21	85	SDI.20	SDI.21
86	SDI.18	SDI.19	86	SDI.18	SDI.19
87	SDI.16	SDI.17	87	SDI.16	SDI.17
88	SDI.14	SDI.15	88	SDI.14	SDI.15
89	SDI.12	SDI.13	89	SDI.12	SDI.13
91	SDI.10	SDI.11	91	SDI.10	SDI.11
92	SDI.08	SDI.09	92	SDI.08	SDI.09
93	SDI.06	SDI.07	93	SDI.06	SDI.07
94	SDI.04	SDI.05	94	SDI.04	SDI.05
95	SDI.02	SDI.03	95	SDI.02	SDI.03
96	SDI.00	SDI.01	96	SDI.00	SDI.01

1-100

101-200

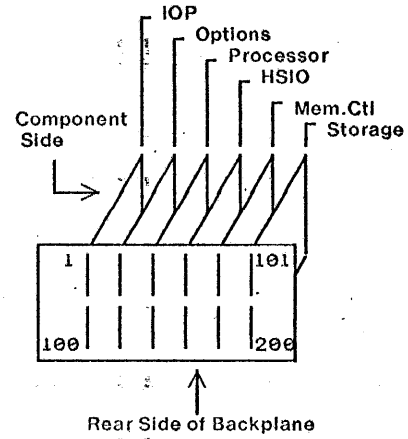
1-100

101-200

Dandelion Backplane - 2

Rev	B	2/19/80
Ogus		1:19 p

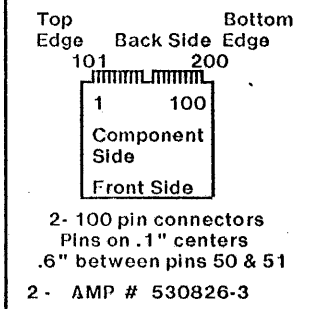
Physical arrangement of cards:



Power & Ground

Voltage	Pins
+12 V	1,101
+5 V	50,51,150,151
GND	10,20,30,40,60,70,80,90,110,120,130,140,160,170,180,190
-5 V	100,200
-12 V	98,198
No Conn	97,99,197,199

Card Edge Connector



Stamen5-6.sil In:

[Iris]<Workstation>Backplane>Backplane-B.dm

Above diagram is rear view (wiring side) of backplane. All numbers are in DECIMAL.

IOP			OPTIONS			CP			HSIO			
02			02	Cycle.1'	Click.0	02	Cycle1'	Click.0	02	Cycle1'	Click.0	02
03			03	Cycle.2'	Click.1	03	Cycle2'	Click.1	03	Cycle2'	Click.1	03
04			04	Cycle.3'	Click.2	04	Cycle3'	Click.2	04	Cycle3'	Click.2	04
05	Spare22	Spare23	05	Spare22	Spare23	05			05	RAS'	LRAS'	05
06	Spare2		06	Spare2		06			06	CAS	LCAS	06
07	Spare20	Spare21	07	Spare20	Spare21	07	Spare20	Spare21	07	WPulse	DR/C	07
08	Spare18	Spare19	08	Spare18	Spare19	08	Spare18	Spare19	08			08
09	ppCLK		09	ppCLK		09	ppCLK		09	ppCLK		09
11	Spare16	Spare17	11	Spare16	Spare17	11	AllowWrite		11	AllowWrite		11
12	IOPClk		12	IOPClk		12			12			12
13	Spare14	Spare15	13	Spare14	Spare15	13	MAR←	mem	13	MAR←	mem	13
14	Spare12	Spare13	14	Spare12	Spare13	14	←MStatus'		14	←MStatus'		14
15	IOPDataOut	BRCIk	15	IOPDataOut	BRCIk	15	MapRef	MCTl←'	15	MapRef	MCTl←'	15
16	SelTroyMode	Spare9	16	SelTroyMode	Spare9	16	Refresh'		16	Refresh'		16
17	Wait	IOPReset'	17	Wait	IOPReset'	17	Wait	IOPReset'	17	Wait	IOPReset'	17
18	TrIndex	TrHdLd	18	TrIndex	TrHdLd	18	Spare26	Spare27	18	Spare26	Spare27	18
19	TrReady	TrStep	19	TrReady	TrStep	19	Spare24	Spare25	19	Spare24	Spare25	19
21	IOPData←'	IOPCtl←'	21	IOPData←'	IOPCtl←'	21	IOPData←'	IOPCtl←'	21	IOPData←'	IOPCtl←'	21
22	TrTK00	TrDirIn	22	TrTK00	TrDirIn	22	KOData←'	KCtl←'	22	KOData←'	KCtl←'	22
23			23	EOData←'	EICtl←'	23	EOData←'	EICtl←'	23	EOData←'	EICtl←'	23
24	TrWrProt	TrWrGate	24	TrWrProt	TrWrGate	24	DCTlFifo←'	DCTl←'	24	DCTlFifo←'	DCTl←'	24
25	TrRdData	TrWrData	25	TrRdData	TrWrData	25	DBorder←'		25	DBorder←'		25
26	EWrite'	EOCtl←'	26	EWrite'	EOCtl←'	26	EWrite'	EOCtl←'	26	EWrite'	EOCtl←'	26
27	KCmd←'	IOOutSp4←'	27	KCmd←'	IOOutSp4←'	27	KCmd←'	IOOutSp4←'	27	KCmd←'	IOOutSp4←'	27
28			28	POData←'	PCtl←'	28	POData←'	PCtl←'	28	POData←'	PCtl←'	28
29	Spare6	Spare7	29	Spare6	Spare7	29	Spare6	Spare7	29	Spare6	Spare7	29
31			31	EIData'	EStatus'	31	EIData'	EStatus'	31	EIData'	EStatus'	31
32	Spare4	Spare5	32	Spare4	Spare5	32	←KIData'	←KStatus'	32	←KIData'	←KStatus'	32
33			33	KWrite'		33	←KTest'	KWrite'	33	←KTest'	KWrite'	33
34	←IOPIData'	←IOPStatus'	34	←IOPIData'	←IOPStatus'	34	←IOPIData'	←IOPStatus'	34	←IOPIData'	←IOPStatus'	34
35	←IOInSp2'		35	←IOInSp2'	PrtReq'	35	←IOInSp2'	PrtReq'	35	←IOInSp2'	PrtReq'	35
36	IOPALE	Spare3	36	IOPALE	Spare3	36	IOPALE	Spare3	36	IOPALE	Spare3	36
37	CSParErr	EndLine'	37	CSParErr	EndLine'	37	CSParErr	EndLine'	37	CSParErr	EndLine'	37
38	IODisp.0	IODisp.1	38	IODisp.0	IODisp.1	38	IODisp.0	IODisp.1	38	IODisp.0	IODisp.1	38
39	YIODisp.0	YIODisp.1	39	YIODisp.0	YIODisp.1	39	YIODisp.0	YIODisp.1	39	YIODisp.0	YIODisp.1	39
41	X.0	X.1	41	X.0	X.1	41	X.0	X.1	41	X.0	X.1	41
42	X.2	X.3	42	X.2	X.3	42	X.2	X.3	42	X.2	X.3	42
43	X.4	X.5	43	X.4	X.5	43	X.4	X.5	43	X.4	X.5	43
44	X.6	X.7	44	X.6	X.7	44	X.6	X.7	44	X.6	X.7	44
45	X.8	X.9	45	X.8	X.9	45	X.8	X.9	45	X.8	X.9	45
46	X.10	X.11	46	X.10	X.11	46	X.10	X.11	46	X.10	X.11	46
47	X.12	X.13	47	X.12	X.13	47	X.12	X.13	47	X.12	X.13	47
48	X.14	X.15	48	X.14	X.15	48	X.14	X.15	48	X.14	X.15	48
49			49	Y.0	Y.1	49	Y.0	Y.1	49	Y.0	Y.1	49
52			52	Y.2	Y.3	52	Y.2	Y.3	52	Y.2	Y.3	52
53			53	Y.4	Y.5	53	Y.4	Y.5	53	Y.4	Y.5	53
54			54	Y.6	Y.7	54	Y.6	Y.7	54	Y.6	Y.7	54
55			55	Y.8	Y.9	55	Y.8	Y.9	55	Y.8	Y.9	55
56			56	Y.10	Y.11	56	Y.10	Y.11	56	Y.10	Y.11	56
57			57	Y.12	Y.13	57	Y.12	Y.13	57	Y.12	Y.13	57
58			58	Y.14	Y.15	58	Y.14	Y.15	58	Y.14	Y.15	58
59	DmaReqC'	DmaAckC'	59	DmaReqC'	DmaAckC'	59	YH.0	YH.1	59	YH.0	YH.1	59
61	DmaReqA'	DmaAckA'	61	DmaReqA'	DmaAckA'	61	YH.2	YH.3	61	YH.2	YH.3	61
62	DmaReqB'	DmaAckB'	62	DmaReqB'	DmaAckB'	62	YH.4	YH.5	62	YH.4	YH.5	62
63	DmaCycle	ExtWaitReq'	63	DmaCycle	ExtWaitReq'	63	YH.6	YH.7	63	YH.6	YH.7	63
64	IOPIntReq0	IOPIntReq1	64	IOPIntReq0	IOPIntReq1	64	Pt.0	Pt.1	64	Pt.0	Pt.1	64
65	IOPIntReq2	IOPIntReq3	65	IOPIntReq2	IOPIntReq3	65	Pt.2		65	Pt.2		65
66	IOPSel.0'	IOPSel.1'	66	IOPSel.0'	IOPSel.1'	66	Disp-Proc'	MemErr	66	Disp-Proc'	MemErr	66
67	IOPSel.2'	IOPSel.3'	67	IOPSel.2'	IOPSel.3'	67	DAddr.0	DAddr.1	67	DAddr.0	DAddr.1	67
68	IOPSel.4'	IOPSel.5'	68	IOPSel.4'	IOPSel.5'	68	DAddr.2	DAddr.3	68	DAddr.2	DAddr.3	68
69	IOPAddr.00	IOPAddr.01	69	IOPAddr.00	IOPAddr.01	69	DAddr.4	DAddr.5	69	DAddr.4	DAddr.5	69
71	IOPAddr.02	IOPAddr.03	71	IOPAddr.02	IOPAddr.03	71			71	DAddr.6	DAddr.7	71
72	IOPAddr.04	IOPAddr.05	72	IOPAddr.04	IOPAddr.05	72			72	DAddr.8	DAddr.9	72
73	IOPAddr.06	IOPAddr.07	73	IOPAddr.06	IOPAddr.07	73			73	DAddr.10	DAddr.11	73
74	IOPAddr.08	IOPAddr.09	74	IOPAddr.08	IOPAddr.09	74			74	DAddr.12	DAddr.13	74
75	IOPAddr.10	IOPAddr.11	75	IOPAddr.10	IOPAddr.11	75			75	DAddr.14	DAddr.15	75
76	IOPAddr.12	IOPAddr.13	76	IOPAddr.12	IOPAddr.13	76	IOPAddr.12	IOPAddr.13	76	DData.0	DData.1	76
77	IOPAddr.14	IOPAddr.15	77	IOPAddr.14	IOPAddr.15	77	IOPAddr.14	IOPAddr.15	77	DData.2	DData.3	77
78	Spare0	Spare1	78	Spare0	Spare1	78	Spare0	Spare1	78	DData.4	DData.5	78
79	IOPMemRd'	IOP/ORd'	79	IOPMemRd'	IOP/ORd'	79			79	DData.6	DData.7	79
81	CSWE.a'	CSWE.b'	81	CSWE.a'	CSWE.b'	81	CSWE.a'	CSWE.b'	81	DData.8	DData.9	81
82	CSWE.c'	CSWE.d'	82	CSWE.c'	CSWE.d'	82	CSWE.c'	CSWE.d'	82	DData.10	DData.11	82
83	CSWE.e'	CSWE.f'	83	CSWE.e'	CSWE.f'	83	CSWE.e'	CSWE.f'	83	DData.12	DData.13	83
84	IOPReq'	ClrIOPReq'	84	IOPReq'	ClrIOPReq'	84	IOPReq'	ClrIOPReq'	84	DData.14	DData.15	84
85			85	DPReq'	ClrDPReq'	85	DPReq'	ClrDPReq'	85	DPReq'	ClrDPReq'	85
86			86	EReq'	ClrRefReq'	86	EReq'	ClrRefReq'	86	EReq'	ClrRefReq'	86
87	IOPMemWr'	IOP/ORw'	87	IOPMemWr'	IOP/ORw'	87	KReq'	ClrKFlags'	87	KReq'	ClrKFlags'	87
88	RefReq'	ReadCSEn'	88	RefReq'	ReadCSEn'	88	RefReq'	ReadCSEn'	88	RefReq'	ReadCSEn'	88
89	EORound	IOPWait	89	EORound	IOPWait	89	EORound	IOPWait	89	EORound	IOPWait	89
91	WrTPCHigh'	WrTPCLow	91	WrTPCHigh'	WrTPCLow	91	WrTPCHigh'	WrTPCLow	91			91
92	IOPData.0	IOPData.1	92	IOPData.0	IOPData.1	92	IOPData.0	IOPData.1	92			92
93	IOPData.2	IOPData.3	93	IOPData.2	IOPData.3	93	IOPData.2	IOPData.3	93			93
94	IOPData.4	IOPData.5	94	IOPData.4	IOPData.5	94	IOPData.4	IOPData.5	94			94
95	IOPData.6	IOPData.7	95	IOPData.6	IOPData.7	95	IOPData.6	IOPData.7	95			95
96	SwTAddr	SwTAddr'	96	SwTAddr	SwTAddr'	96	SwTAddr	SwTAddr'	96			96

1-100

101-200

1-100

101-200

1-100

101-200

1-100

101-200

Above diagram is rear view (wiring side) of backplane.
ALL NUMBERS ARE IN DECIMAL.

Dandelion Backplane Signals - 1

Stamen1-4.sil in:

[Iris]<Workstation>Backplane>Backplane-C.dm

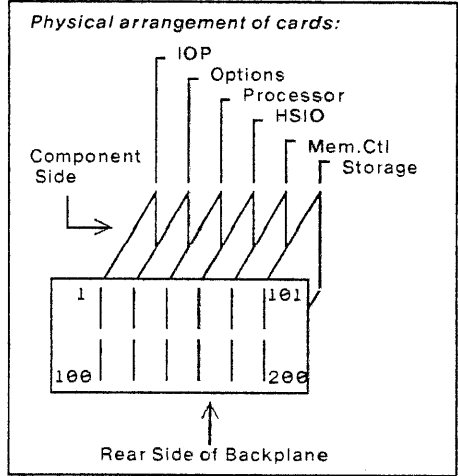
Rev	C	9/26/80
Ogus		

MEM CTRL				STORAGE			
02	Cycle1'			02			
03	Cycle2'			03			
04	Cycle3'			04			
05	RAS'	LRAS'		05	RAS'	LRAS'	
06	CAS	LCAS		06	CAS	LCAS	
07	WPulse	DR/C		07			
08				08			
09	ppCLK			09	ppCLK		
11	AllowWrite			11			
12	Bank0'			12	Bank0'		
13	MAR←	mem		13			
14		←MStatus'		14			
15	MapRef	MCTl←'		15			
16	Refresh'	CRrefresh'		16	Refresh'	CRrefresh'	
17	Wait			17			
18	SDO.00	SDO.01		18	SDO.00	SDO.01	
19	SDO.02	SDO.03		19	SDO.02	SDO.03	
21	SDO.04	SDO.05		21	SDO.04	SDO.05	
22	SDO.06	SDO.07		22	SDO.06	SDO.07	
23	SDO.08	SDO.09		23	SDO.08	SDO.09	
24	SDO.10	SDO.11		24	SDO.10	SDO.11	
25	SDO.12	SDO.13		25	SDO.12	SDO.13	
26	SDO.14	SDO.15		26	SDO.14	SDO.15	
27	SDO.16	SDO.17		27	SDO.16	SDO.17	
28	SDO.18	SDO.19		28	SDO.18	SDO.19	
29	SDO.20	SDO.21		29	SDO.20	SDO.21	
31				31			
32	SAddr.00	SAddr.01		32	SAddr.00	SAddr.01	
33	SAddr.02	SAddr.03		33	SAddr.02	SAddr.03	
34	SAddr.04	SAddr.05		34	SAddr.04	SAddr.05	
35	SAddr.06	SAddr.07		35	SAddr.06	SAddr.07	
36	Y1Latch	YOLatch		36	Y1Latch	YOLatch	
37	Bank1'	Bank2'		37	Bank1'	Bank2'	
38	MRef'	Write'		38	MRef'	Write'	
39				39			
41	X.0	X.1		41			
42	X.2	X.3		42			
43	X.4	X.5		43			
44	X.6	X.7		44			
45	X.8	X.9		45			
46	X.10	X.11		46			
47	X.12	X.13		47			
48	X.14	X.15		48			
49	Y.0	Y.1		49			
52	Y.2	Y.3		52			
53	Y.4	Y.5		53			
54	Y.6	Y.7		54			
55	Y.8	Y.9		55			
56	Y.10	Y.11		56			
57	Y.12	Y.13		57			
58	Y.14	Y.15		58			
59	YH.0	YH.1		59			
61	YH.2	YH.3		61			
62	YH.4	YH.5		62			
63	YH.6	YH.7		63			
64	Pt.0	Pt.1		64			
65	Pt.2			65			
66	Disp.Proc'	MemErr		66			
67	DAddr.0	DAddr.1		67			
68	DAddr.2	DAddr.3		68			
69	DAddr.4	DAddr.5		69			
71	DAddr.6	DAddr.7		71			
72	DAddr.8	DAddr.9		72			
73	DAddr.10	DAddr.11		73			
74	DAddr.12	DAddr.13		74			
75	DAddr.14	DAddr.15		75			
76	DData.0	DData.1		76			
77	DData.2	DData.3		77			
78	DData.4	DData.5		78			
79	DData.6	DData.7		79			
81	DData.8	DData.9		81			
82	DData.10	DData.11		82			
83	DData.12	DData.13		83			
84	DData.14	DData.15		84			
85	SDI.20	SDI.21		85	SDI.20	SDI.21	
86	SDI.18	SDI.19		86	SDI.18	SDI.19	
87	SDI.16	SDI.17		87	SDI.16	SDI.17	
88	SDI.14	SDI.15		88	SDI.14	SDI.15	
89	SDI.12	SDI.13		89	SDI.12	SDI.13	
91	SDI.10	SDI.11		91	SDI.10	SDI.11	
92	SDI.08	SDI.09		92	SDI.08	SDI.09	
93	SDI.06	SDI.07		93	SDI.06	SDI.07	
94	SDI.04	SDI.05		94	SDI.04	SDI.05	
95	SDI.02	SDI.03		95	SDI.02	SDI.03	
96	SDI.00	SDI.01		96	SDI.00	SDI.01	

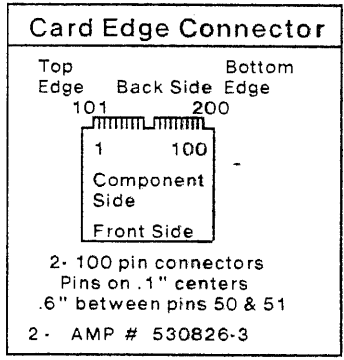
1-100 101-200 1-100 101-200

Above diagram is rear view (wiring side) of backplane.
All numbers are in DECIMAL.

Dandelion Backplane - 2	
Rev C	9/26/80
Ogus	



Power & Ground	
Voltage	Pins
+ 12 V	1,101
+ 5 V	50,51,150,151
GND	10,20,30,40,60 70,80,90,110,120, 130,140,160,170, 180,190
- 5 V	100,200
- 12 V	98,198
No Conn	97,99,197,199



Stamen5-6.sil in:

[Iris]<Workstation>Backplane>Backplane-C.dm

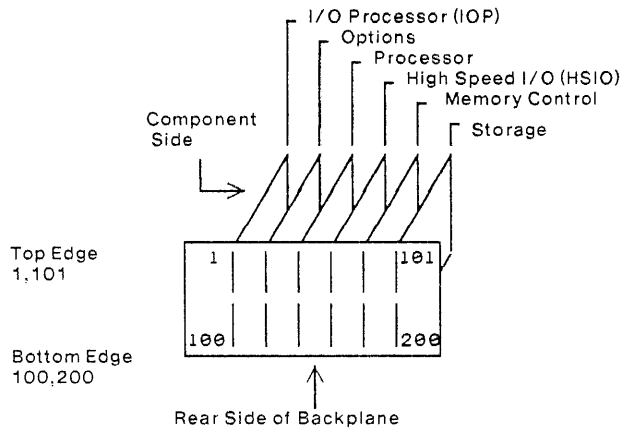
Revision B to Revision C

- Rename XOData←' to EOData←' (23)
- Rename XCtl←' to EICtl←' (123)
- Rename IOOutSp1←' to EWrite' (26)
- Rename IOOutSp2←' to EOCtl←' (126)
- Rename IOOutSp3←' to KCmd←' (27)
- Rename ←XIData' to EIData' (31)
- Rename ←XStatus' to EStatus' (131)
- Rename ←PStatus' to KWrite' (133)
- Rename XReq' to EReq' (86)
- Rename ClrXReq' to ClrRefReq' (186)
- Rename SpareReq' to EORound (89)
- Rename Spare10 to IOPDataOut (15)
- Rename Spare11 to BRCIk (115)
- Rename ClrRefReq' to PrtReq' (135)
- Rename Spare2 to IOPALE (36)
- Rename IOPALE to Spare2 (06)
- Rename DmaReqA to DmaReqA' (61)
- Rename DmaReqB to DmaReqB' (62)
- Rename DmaReqC to DmaReqC' (59)
- Rename DmaAckA to DmaAckA' (161)
- Rename DmaAckB to DmaAckB' (162)
- Rename DmaAckC to DmaAckC' (159)
- rename IOPSel.0 to IOIPSel.0' (66)
- rename IOPSel.1 to IOIPSel.1' (166)
- rename IOPSel.2 to IOIPSel.2' (67)
- rename IOPSel.3 to IOIPSel.3' (167)
- rename IOPSel.4 to IOIPSel.4' (68)
- rename IOPSel.5 to IOIPSel.5' (168)

XEROX SDD	Project Dandelion	Backplane Revision History	File StamenChanges1.si	Designer Ogus	Rev C	Date 9/26/80
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Dandelion Backplane

Physical arrangement



Files

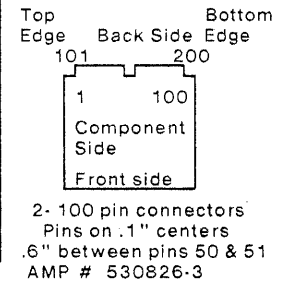
[Iris]<Workstation>Backplane>
Backplane-C.press
Backplane-C.dm

Backplane Signals

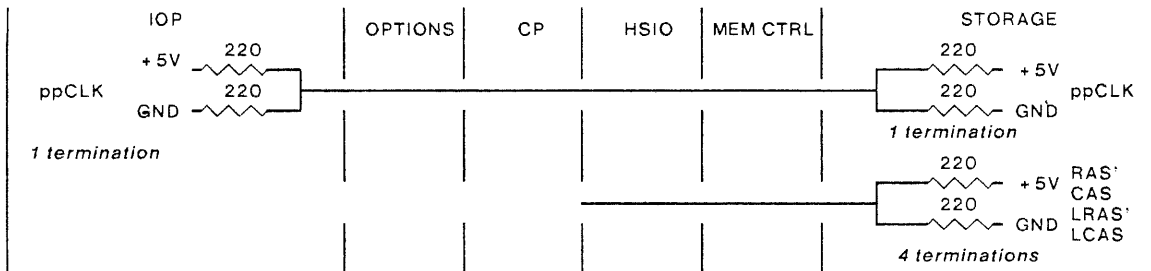
Card	IOP	Options	Central Processor	High Speed I/O	Memory Control	Storage	
Total Signal lines used	131	166	140	141	155	66	170 max. per card
I/O Connectors on front of boards	Floppy Keyboard Printer MaintenanceP Alto umb.	LSEP/Ethernet RS232/RS366		SA4XXX SA100X Display			

Power distribution

<i>Backplane Power & Ground</i>		<i>30 lines total</i>
Voltage	Backplane Pins	
+ 12 V	1,101	
+ 5 V	50,51,150,151	
Gnd	10,20,30,40,60,70,80,90,110,120,130,140,160,170,180,190	
- 5V	100,200	
- 12 V	98,198	
No Conn.	97,99,197,199	



Termination of clock signals



Terminations are placed on the IOP and STORAGE cards.

XEROX SDD	Project Dandelion	Backplane Description General Characteristics	File WSBackplane.sil	Designer Ogus	Rev C	Date 9/26/80
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