INTRODUCTION

The WD/9000 Microprocessor is a 16-bit MOS/LSI Chip Set that directly executes programs written in the Pascal programming language. The Chip Set consists of five LSI components:

Arithmetic Component (CP2151)

Control Processor (CP2161)

MICROMS (CP2171-1,CP2171-2,and CP2171-3)

DEVICE ADDRESSES AND BOOTSTRAPPING

Page 29 of the WD/90 Pascal MICROENGINEtm Reference Manual (Users' Manual Section) lists standard device addresses. A subset of these are used by the firmware, all are recognized by the Pascal Operating System. The subset which the firmware recognizes includes the floppy disk, DMA, specification switch for serial port A, system value of nil, and the reserved location which is part of the boot sequence. These device addresses are hard coded into the bootstrap sequence of the chip set. Two values cannot be changed anytime: the system value of nil and the reserved word device addresses FC6X. Under the optional bootstrap technique, other device addresses do not have to be reserved.

When the processor receives a RESET signal (automatically occurs when power is applied), the system will enter a restart sequence. After internal initialization the processor will read from reserved location FC6X which defines the bootstrap sequence. If the value of zero is returned, the internal firmware bootstrap is executed. It expects the floppy disk controller (FD1791) and the DMA controller (DM1883) to be installed at the device address FC3X. A value other than zero indicates the starting address of a Pascal bootstrap program with the appropriate task information block as the first 5 entries at that location. The processor will set up the environment and begin execution at the address pointed to by the task information block.

PROCESSOR CONTROL SIGNALS

Interfacing the chip set to a physical environment requires the use of processor control signals. There are five main

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control signals which establish this handshake:

SYNC indicates an I/O cycle; on the leading edge of SYNC an address is valid on DAL lines.

DIN and DOUT are control signals that define the direction of a transfer: DIN from the external environment to the processor and DOUT from the processor to an external environment.

REPLY synchronizes processor operation with external devices slower in response time than the chip set. Its function is to indicate that the addressed device is physically there and that the device is ready. If an address is presented and a REPLY signal is not received the chip set will loop indefinitely waiting for REPLY. The external environment should provide a time out or delay function to indicate that a non- existent location(memory or peripheral) was addressed.

WRITE/NOT READ can be used to indicate an early write cycle for use with slower memories. During an output phase it also indicates whether a byte or word is being transferred across the bus. When the WRITE/NOT READ line is true the upper byte written to the bus will be forced to zero. The processor will not present the zeros but will assume that with the signal being true, external hardware will zero the upper byte. THIS FUNCTION IS REQUIRED FOR PROPER EXECUTION OF THE INSTRUCTION SET.

It is recommended that the four interrupts and REPLY signal be synchronized to Phase II of the processor clock to assure that short cycles do not occur during I/O transfers. This will insure that a device generating a response will be intiated during an input phase of the chip set instruction. This can be accomplished by using a edge clocked latch, clocking on Phase II with the reply line from the external environment passing through this latch before connecting to the control chip.

INTERRUPT HANDLING

On Page 30, of the WD/90 Pascal MICROENGINEtm Reference Manual (Users' Manual Section) interrupts related to the standard devices on the WD90 board are listed from highest to lowest priority. All interface controllers must generate equivalent vector addresses. The 3.0 Operating System reserves a block of vector addresses from memory location 0 through 7F. Each block is 16 words long and supports a given device. During an interrupt sequence the processor responds to the interrupt with an interrupt acknowledge (IACK) signal. The interrupted device presents a vector address on the data lines. The value presented is used as the effective address, the semaphore contained in that address is used for the signal operation.

The interrupt structure is briefly described on page 29. There are 4 interrupt lines, each one representing a different

level of priority from I0 to I3. Any number of devices can be attached to a given interrupt level, all devices on a given level will have a daisy chain priority so that the physical location will reflect a relative priority on a given interrupt line. On the WD90 board, all devices are on the same interrupt level which is I0, the highest priority level. During an interrupt sequence a device requests an interrupt by signalling one of the four lines. In response to that, the chip set will present a 4 bit code (DATA bits 0-3) with one bit being an enable to external hardware defining the level which should respond.

There are two levels of priorities: the four levels recognized by the chip set and a priority on each level determined by daisy chaining an interrupt priority level through each device. Priority between the four levels is determined in firmware and the enable word which is sent out to inhibit all levels except for the one being serviced. If more than one level of interrupt is being used additional hardware is required to disable other levels. An addressable gate or an external latch is required to turn interrupts on and off under program control.

On the WD/90 board with all interrupts on I0 level, there is no mask required. The board uses a priority encoder to decode which device is interrupting and produce the interrupt vector in one operation. For the chip set to operate in an environment with all four interrupt levels, two external hardware elements are required: one is a mask register to enable and disable any priority level and the second is a control signal which effectively enables and disables interrupts.

I/O handling and response to interrupts are similar to programmed I/O except that an interrupt acknowledge signal indicates that the current I/O cycle is in response to an interrupt request rather than a programmed input or output.

During an interrupt acknowledge sequence, SYNC indicates the presence of a device address, DIN or DOUT determine the type of interrupt operation, and IACK is true indicating that the processor expects the interrupting device to present the vector address assigned to that device on the data line . The chip set executes an input I/O cycle to capture the address presented on the data line. This address is used to determine which interrupt service routine is to be executed.

DIRECT MEMORY ACCESS

The last mode of I/O handling is a DMA or a direct memory access request from a device where the processor removes all control, address, and data signals from the bus in order to allow another device or controller to take over the bus. Synchronization is required to support the DMA request to insure that the processor is not accessing the bus when it is

released. This synchronization is accomplished by the BUSY line which requests that the processor, at the completion of its current bus access, if one is underway, enter into a state where processor operations can continue to be executed until the bus is again needed. At this point the chip set will go into a wait state until the bus is available. A DMA request from a controller should be synchronized on a Phase II edge and provide a BUSY signal. On the following Phase II a bus grant must be generated. The bus grant must be qualified with an OR function of the DIN or the DOUT signal which will define that an bus access is not in process when the grant is provided. Once the bus grant signal is generated, the external controller should release the bus when its operation is complete. The chip set is not involved until that release.

DESIGN CONSIDERATIONS

It is recommended that capacitance of the MIB lines be approximately 33 to 47 picofarads. This may be achieved using ground planes as part of the layout or by installing 33 picofarad capacitors between each MIB line and ground.