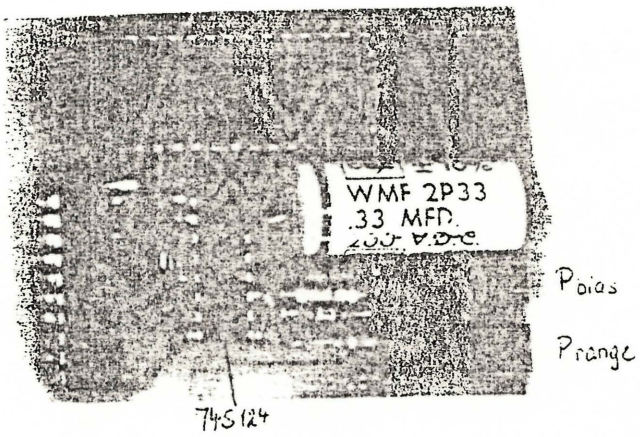
SE - 90

Abgleichanweisung für Piggy-Back-Platine

1. Flachbandkabel an beiden Laufwerken abziehen (! auf Berührung mit Netzteil!)
2. Voltmeter an 74S124, PIN 2. Mittels P-bias auf 1,4V einstellen.
3. Frequenzmesser am 74S124, PIN 7. Mittels P-range auf 4,0 MHz einstellen.
4. Flachbandkabel wieder anschließen



2.12.1980

Fehler war am 26.3.87: Boot, dann 'stop in' nicht mehr.
Ursache: Kondensator war ab (0,33µF)

NFORMATION IS CONFIDENTIAL AND
ILTARY TO WDC AND SHALL NOT BE
NUCED OR FURTHER DISCLOSED TO
E OTHER THAN WDC EMPLOYEES
UT WRITTEN AUTHORIZATION FROM
RN DIGITAL CORPORATION.

CHG	E.O. NO.	DATE	BY	CHKD

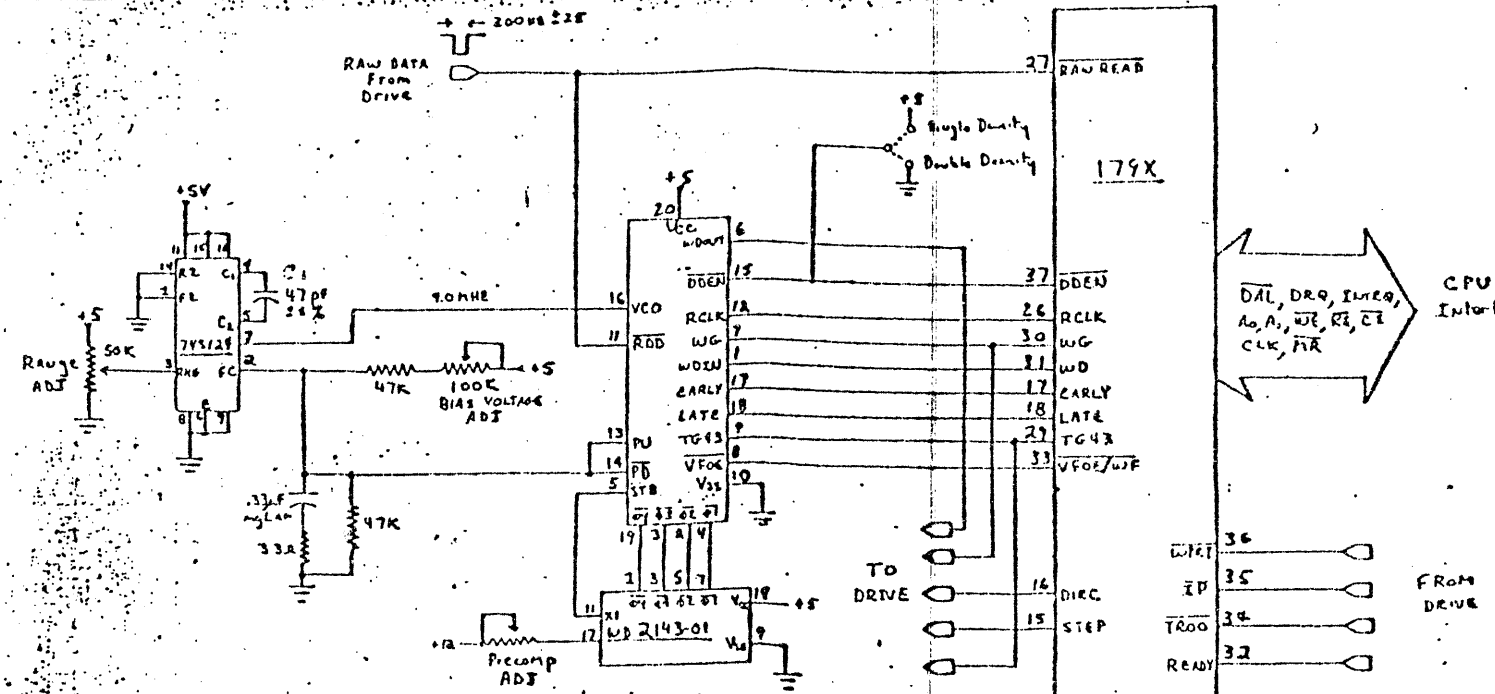


Fig. 1

8" Single/Double Density Floppy Interface

Notes:

1) All resistors ¼W ±5%

2) Specifications

Capture Range: ±20%

Lock-up Time: 25 µsec

(All one's pattern, MFM)

S: UNLESS OTHERWISE SPECIFIED.

DRAWN		WESTERN DIGITAL	TITLE 1691 – 179X Interface
CHECK			
DESIGN	JVJ		DWG NO. - REV
ENGR		ISSUE DATE 1/AY'80	SIZE B
OPER		SCALE	SHEET 1 OF 1

GRAPHICS/ACCUPRESS
FORM NO. A 6760

PRELIMINARY

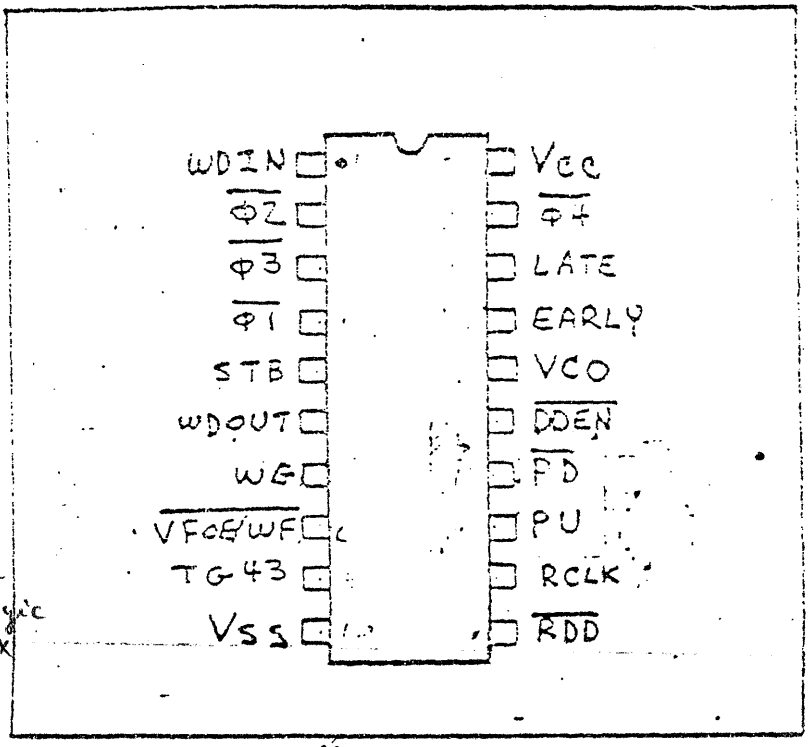
WESTERN DIGITAL

CORPORATION

691 FLOPPY SUPPORT LOGIC (F.S.L.)

EATURES

irect interface to the FD179X
liminates external FDC Logic
ata Separation/RCLK GENERATION
rite Precompensation Signals
FOE/WF Demultiplexing
rogrammable Density
" or 5.25" Drive Compatable
ll inputs and outputs TTL
Compatible
ingle +5V Supply

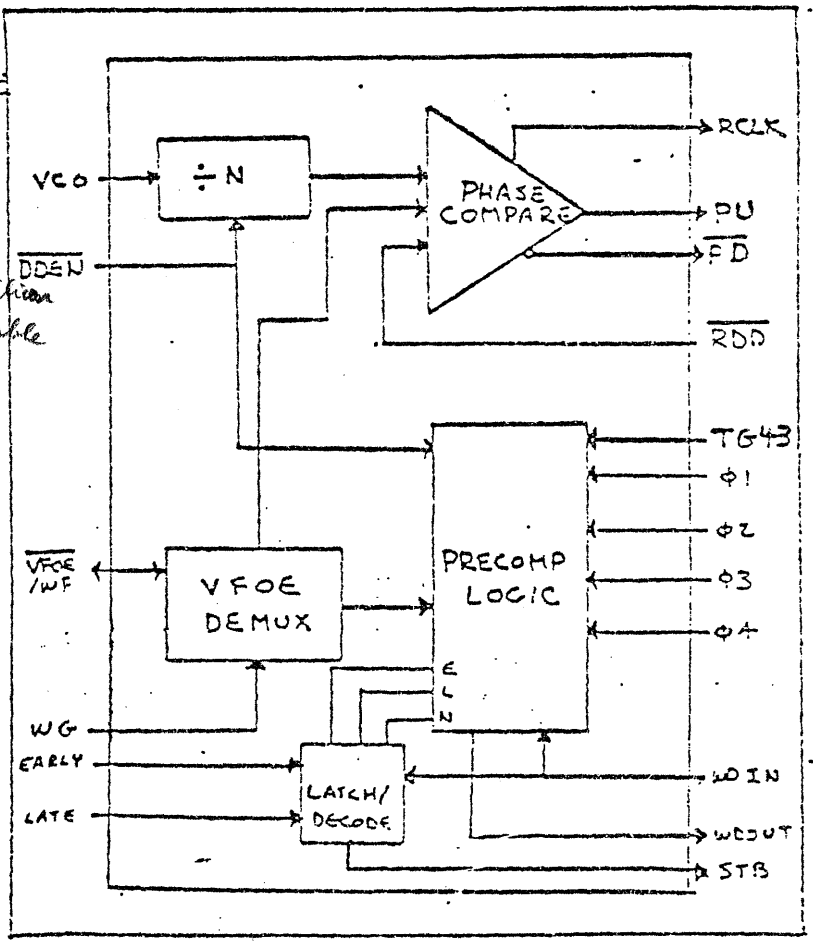


PIN CONNECTIONS

ENE L DESCRIPTION

he WD1691 F.S.L. has been designed esigned to minimize the external logic ogic required to interface the 179X 79X family of Floppy Disk controllers ontrollers to a drive. With the se of an external VCO, the WD1691 ill generate the RCLK signal for he 179X, while providing an djustment pulse (PUMP) to control he VCO frequency. VFOE/WF e-multiplexing is also accomplished nd Write Precompensation signals ave been included to interface irectly with the WD2143 Clock enerator.

he D1691 is implimented in N-MOS silicon gate technology and is available v lable in a plastic or ceramic 0 pin dual-in-line package.

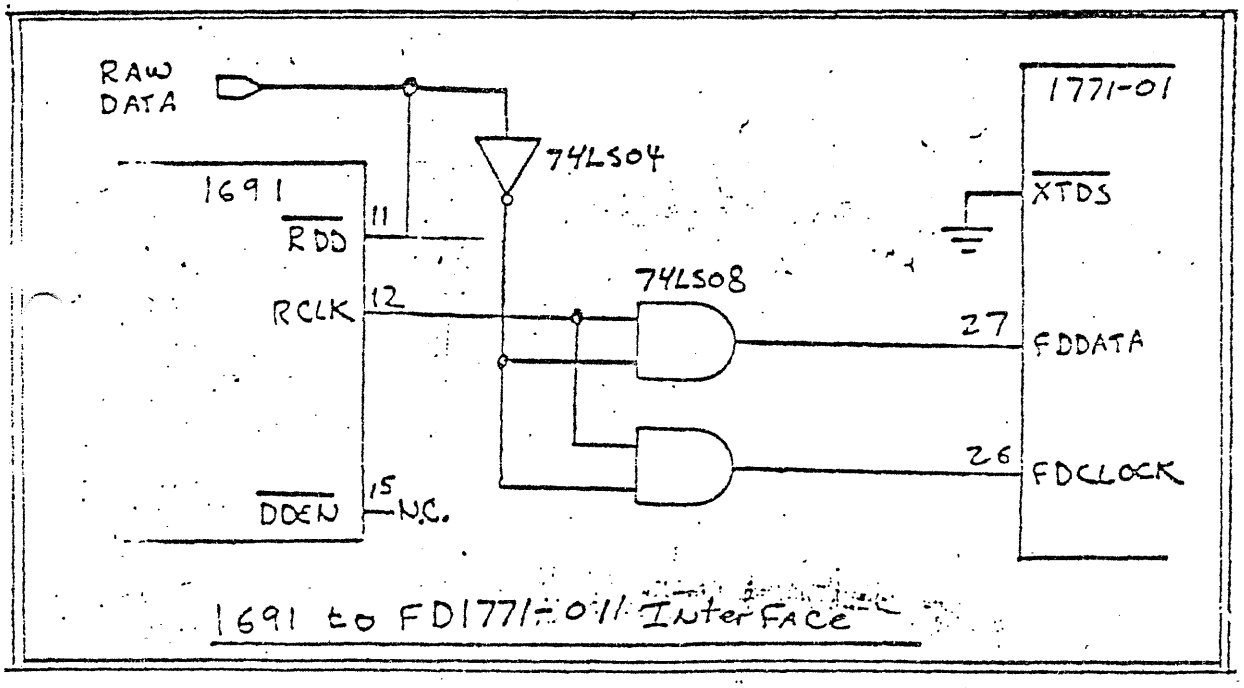


Typical Applications

Shown in Figure 1 is a Phase-Lock-Loop data separator and the support logic for a single and double-density 8" drive. The raw data (both clock and data bits) are fed to the 1691 and 179X. The 1691 outputs its PU or $\overline{PD}$ signal, which is integrated by the .33uf capacitor and 330hm resistor to form a control voltage for the 74S124 VCO device. The 4.0MHZ nominal output of the VCO then feeds back to the 1691 completing the loop. The WD2143 is also used, providing write precompensation when in double-density, from tracks 44-77. The DDEN line can either be controlled by a toggle switch or a logic level from the host system.

The data separator must be adjusted with the RDD or VFOE/WF line at a Logic 1 Logic 1. Adjust the bias voltage potentiometer for 1.4V on pin.2 of the 74S124. Then adjust the range control to yield 4.0MHZ on pin 7 of the 74S124.

To adjust write precompensation, issue a command to the 179X so that write data pulses are present. This can be done with a 'WRITE TRACK' command and the IP line open, or a continuous 'WRITE SECTOR' operation. With a scope on pin 4 of the 1691, adjust the precomp pot for the desired value. This will range from 100 to 300 ns typically. The pulse width set on pin 4 (ØI) will be the desired precomp delay from nominal.



1691 to FD1771-01 Interface

	SYMBOL	NAME	FUNCTION
	WDIN	WRITE DATA INPUT	Ties directly to the 179X WD pin.
,4,19	$\overline{\phi 2}$,$\overline{\phi 3}$,$\overline{\phi 1}$,$\overline{\phi 4}$	PHASE 2,3,1,4	4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.
	STB	STROBE	Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of $\phi 4$.
	WDOUT	WRITE DATA OUTPUT	Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.
	WG	WRITE GATE	Ties directly to the 179X WG pin.
	$\overline{\text{VFOE/WF}}$	VFO ENABLE/ WRITE FAULT	Ties directly to the 179X $\overline{\text{VFOE/WF}}$ pin.
	TG43	TRACK 43	Ties directly to the 179X TG43 pin, If Write Precompensation is required on TRACKS 44-76.
	V_{ss}	V_{ss}	Ground
	$\overline{\text{RDD}}$	READ DATA	Composite clock and data stream input from the drive.
	RCLK	READ CLOCK	RCLK signal generated by the 1691, to be tied to the 179X RCLK pin.
	PU	PUMP UP	Tri-state output that will be forced high when the 1691 requires an increase in VCO frequency.
	$\overline{\text{PD}}$	PUMP DOWN	Tri-state output that will be forced low when the 1691 requires a decrease in VCO frequency.
5	$\overline{\text{DDEN}}$	Double Density Enable	Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two.
6	VCO	Voltage Controlled Oscillator	A nominal 4.0MHz (8" drive) or 2.0MHz (5.25" drive) master clock input.
7, 18	EARLY LATE	EARLY LATE	EARLY and LATE signals from the 179X, used to determine Write Precompensation.
0	V_{cc}	V_{cc}	+5V $\pm$ 10% power supply

Device Description

The WD1691 is divided into two sections:

1) Data Recovery Circuit
2) Write precompensation Circuit

The Data Separator or Recovery Circuit has four inputs: $\overline{DDEN}$, VCO, $\overline{RDD}$, and $\overline{VFOE/WF}$; and three outputs: PU, $\overline{PD}$ and RCLK. The $\overline{VFOE/WF}$ input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

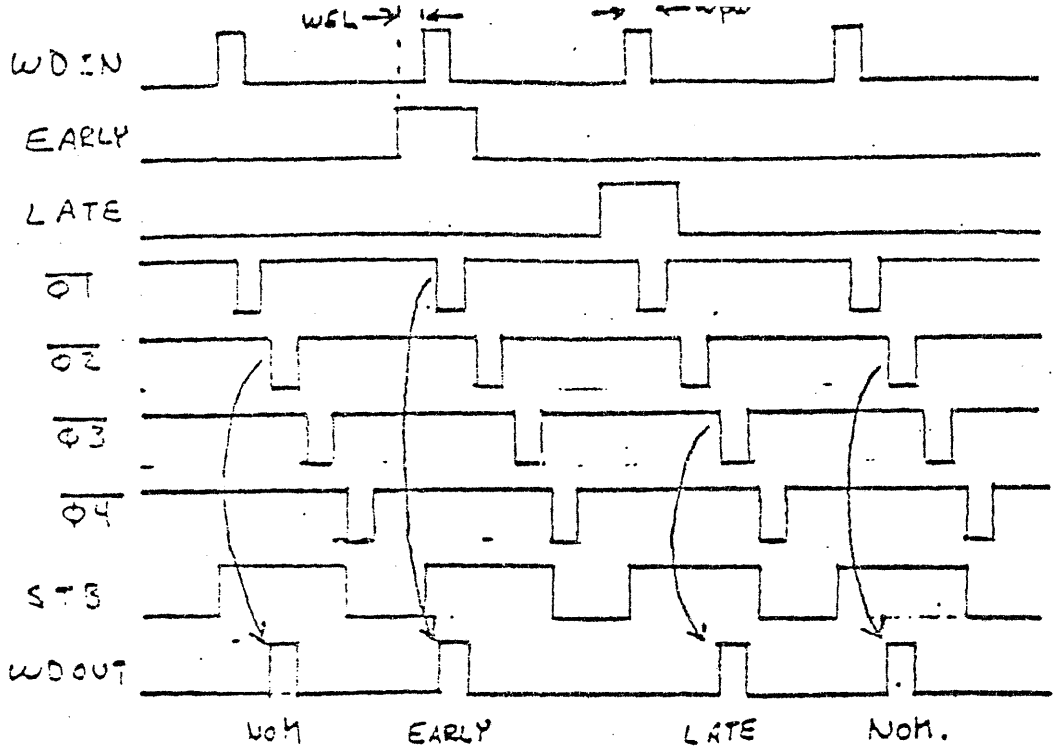
When VFOE/WF and WRITE GATE are low, the data recovery circuit is enabled. When the $\overline{RDD}$ line goes Active Low, the PU or $\overline{PD}$ signals will become active. If the $\overline{RDD}$ line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic 1, requesting an Increase in VCO frequency. If the $\overline{RDD}$ line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while $\overline{PD}$ will go to a logic zero, requesting a Decrease in VCO frequency. When the leading edge of $\overline{RDD}$ occurs in the center of the RCLK window, both PU and $\overline{PD}$ will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. The RCLK signal is a divide-by-16 ($\overline{DDEN}$=1) or a divide-by-8 ($\overline{DDEN}$=Ø) of the VCO frequency.

WG	$\overline{VFOE/WF}$	$\overline{RDD}$	PU+$\overline{PD}$
1	X	X	HI-Z
0	1	X	HI-Z
0	0	1	HI-Z
0	0	0	Enable

The Write Precompensation circuit has been designed to be used with the WD2143-01 clock generator. When the 1691 is operated in a "single density only" mode, write precompensation as well as the 2143-01 is not needed. In this case, $\overline{Ø1}$, $\overline{Ø2}$, $\overline{Ø3}$, $\overline{Ø4}$, and STB should be tied together, DDEN left open, and TG43 tied to gound.

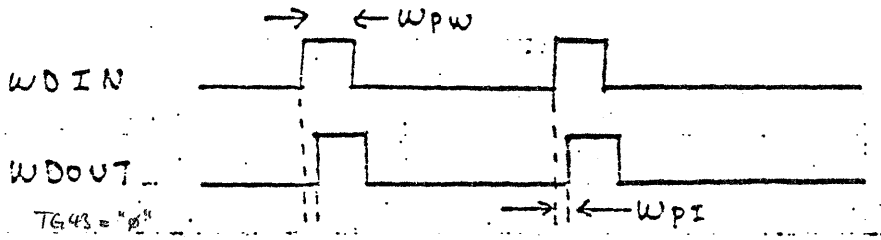
In the double-density mode($\overline{DDEN}$=Ø), the signals Early and Late are used to select a phase input ($\overline{Ø1}$ - $\overline{Ø4}$) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the 2143-01 to start its pulse generation. Ø2 is used as the write data pulse on nominal (Early=Late=Ø), $\overline{Ø2}$ is used for early, and $\overline{Ø3}$ is used for late. The leading edge of $\overline{Ø4}$ resets the STB line in anticipation of the next write data pulse. When TG43=Ø or $\overline{DDEN}$=1, Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic 1) while $\overline{DDEN}$=Ø.

The signals, $\overline{DDEN}$, TG43, and $\overline{RDD}$ have internal pull-up resistors and may be left open if a logic 1 is desired on any of these lines.



TG43 = "1"
DDEN = "0"

WRITE DATA TIMING (MFM)



TG43 = "0"
DDEN = "1"

WRITE DATA TIMING (FM