CHAPTER

2

THEORY

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LIST OF ILLUSTRATIONS

LIST OF TABLES

This chapter contains block level theory of operation discussions for the subassemblies of the 4230/05 Workstations. The equipment is covered in the subsections of this chapter as listed below.

Section 2.1 Monitor
Section 2.2 Keyboard
Section 2.3 Electronics Base
Section 2.4 4230 TC Option
Section 2.5 4230/05 Arabic WS

2.1 MONITOR

The Monitor unit (figure 2-1) contains a 12-inch green-on-black CRT with a Monitor PCA to process video and synchronization signals. The CRT screen has a capacity of 25 lines with 80 characters per line for a total of 2000 characters displayed.

The Monitor PCA receives +12 Vdc from the switching power supply in the Electronics Base via one lead of the Monitor power cable assembly. The +12 Vdc directly supplies the higher current horizontal deflection circuitry and the CRT filament. A series regulator is used to derive a +5 Vdc supply from the +12 Vdc input for the logic devices on the Monitor PCA.

Input signals to the Monitor PCA include VIDEO, HSYNC, VSYNC and INTEN which are generated in the Electronics Base of the particular model Workstation. These signals are applied to the Monitor PCA via the eight-pin monitor video cable, buffered and then presented to the appropriate circuits on the PCA.

2.1 MONITOR (Continued)

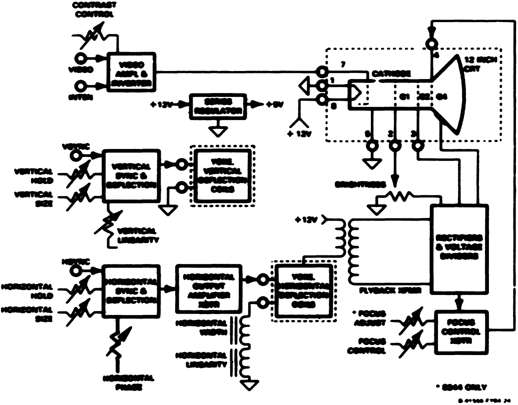


Figure 2-1. Monitor PCA Block Diagram

2.1 MONITOR (Continued)

The VIDEO input is applied to a common-emitter stage in the video amplifier and inverter which provides amplification and inversion of the incoming video signal. The amplified and inverted video drives the cathode of the 12-inch (diagonal) CRT. A special portion of the video amplifier and inverter receives the INTEN signal, which is used to intensify or highlight selected characters on the CRT screen. The INTEN signal causes the CRT cathode voltage to decrease, causing an increase in intensity for the instant that the INTEN sig- nal is present. The front-panel contrast control adjusts the extent to which the circuit reacts to the INTEN signal.

The horizontal sync (HSYNC) input is applied to the horizontal sync and deflection circuitry, comprising a horizontal processor device followed by a driver and, finally, the horizontal output amplifier. The horizontal phase and horizontal hold adjustments are inputs to the horizontal sync and deflection device and provide for a phase and frequency-stable horizontal deflection ramp to be fed to the output stage.

The horizontal output transistor feeds the horizontal deflection coils of the yoke with a sawtooth-type deflection waveform. The current in the yoke windings develops an electro-magnetic field for deflecting the CRT electron beam in the horizontal direction. Adjustments for horizontal width and horizontal linearity form part of the total horizontal deflection coil load.

2.1 MONITOR (Continued)

At horizontal retrace (flyback), the current field in the horizontal deflection coils of the yoke collapses and the resultant energy is stepped up by the flyback transformer. On the secondary side of the flyback transformer are separate windings which feed diode rectifiers and associated voltage divider circuits. Anode operating potential, focus (G4), G1 and G2 voltages are all derived from these rectifier and voltage divider circuits.

The vertical sync (VSYNC) input is applied to the vertical sync and deflection circuitry. Vertical processing is performed wholly by a vertical processor device which develops the final vertical sawtooth waveform that drives the vertical deflection coils of the yoke. Vertical hold, vertical size and vertical linearity adjustments are all inputs to the vertical sync and deflection device.

2.2 KEYBOARD

This section provides an overview of Keyboard operations as well as a functional block diagram level of theory discussion.

2.2.1 KEYBOARD OVERVIEW

The detached Keyboard contains a dedicated 8031 microprocessor that accepts commands from the Z-80 in the Electronics Base while sending both Keyboard status data and keystroke data back to the Z-80. This communication occurs between the serial I/O port of the 8031 in the Keyboard and another 8031 located in the Electronics Base. The Keyboard communicates in a full-duplex mode.

Pressing a key causes the Keyboard to send a 7-bit keystroke code to the Z-80 in the Electronics Base. Every key has its own unique keystroke code, which is arbitrary and bears no relationship to any of the various character codes. In addition to the keystroke codes produced when they are pressed, the left and right SHIFT keys also generate different codes, called release codes, when they are released.

The release code for any key is identical to its keystroke code, but with high-order bit 7 set (i.e., keystroke code plus '80'). Special Keyboard commands establish release codes for up to five other designated keys or, alternately, for all of the keys on the Keyboard.

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

The LOCK and SHIFT keys have transmittable codes that allow maximum flexibilty at the host system. The LOCK key has an LED (bit 0) for a visual indication that the key is engaged. The host system decodes the LOCK key transmittal code and returns a code back to the Keyboard through the 8031 to light the LOCK LED.

The left and right SHIFT keys have make and break codes in the Keyboard default scheme. When either SHIFT key is depressed, it will transmit its own X/Y code (make code). When the SHIFT key is released, a break code will be transmitted. When a shift condition is sensed, the host system will append an '80' bit to all keys until it sees the break code for the shift key.

Any key on the Keyboard is a potential repeat key. If the Keyboard is programmed to generate a release code for a particular key, the Z-80 in the Electronics Base can assume that the key remains down (or pressed) between the time it receives the keystroke code and the time it receives the corresponding release code. Therefore, when a program that is monitoring the Keyboard recognizes a pressed key in this way, it can decide whether the key will repeat, and at what rate.

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

Figure 2-2 shows keystroke code assignments for the standard Keyboard. There are some possible keystroke codes and their corresponding release codes that are not produced by any key.

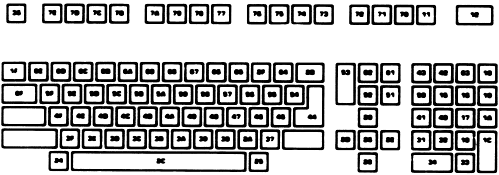


Figure 2-2. Keycode Assignments

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

One of these, code '01', is used as a query response byte, which is always followed by one or more status bytes. When the Z-80 makes an inquiry by sending one of the query control byte sequences, it continues accepting Keyboard input until it receives the '01' query response byte and then accepts the appropriate number of status bytes before resuming normal Keyboard input.

A 4-conductor cable fitted with a 4-pin DIN connector carries power and interface signals between the Keyboard interface and the detached Keyboard. The Keyboard connector and 4-pin DIN connector signals are shown below.

CONNECTOR PIN NO.	DIN PLUG PIN NO.	SIGNAL
1	N/C	Negative lead to speaker
2		Positive lead to speaker
3	1	Ground
4	2	Data output to Keyboard
5	4	5 Vdc power
6	3	Data input from Keyboard

LED control commands are used to turn on individual LEDs as well as turn on and turn off all LEDs. The Keyboard LEDs are used to indicate diagnostic errors. The LED status command allows the host system to read the LED status at any time. The Keyboard is initialized with all LEDs off.

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

N-key rollover exists between all encoded keys on the Keyboard. Therefore, when a key is depressed while other keys are held down, the Keyboard will be able to output the latest keycode. Two 8-bit switchbanks on the Keyboard identify the particular Keyboard configuration.

The Keyboard interface in the Electronics Base is designed around an 8031 microprocessor with a full duplex serial port UART operating at 62.5k baud. On power-up or system reset, hardware initializes the 8031 to transmit and receive serial protocol that consists of one start bit (cleared to zero), an 8-bit data word (least significant bit first), and two stop bits (set to one), without parity.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION

Refer to Figure 2-3 for the following discussion.

Figure 2-3. Low-Profile Serial Keyboard Block Diagram

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD THEORY OF OPERATION (Continued)

The 8031 device is a single-component 8-bit microprocessor that contains 128 x 8-bit internal RAM memory, an internal oscillator and timing circuit for data synchronization, and a full duplex serial port UART. The 8031 device requires one supply voltage (+5 volts) for operation. Keyboard data is either sent or received across the full-duplex Keyboard interface.

A 4 MHz crystal-generated clock is used for the synchronization of the 8031 to the various other components located on the board. This clock is necessary since only power and data are transmitted from the Electronics Base.

The 8031 uses its port zero lines as both the data and the address bus in a multiplexed bus scheme. Lines D0 - D7 identify the shared bus. Signal ALE (address latch enable) enables the address latch when the bus is in the address mode, thus storing an address in the latch. The address latch addresses the EPROM while signal PSEN (program store enable) enables the EPROM to read the instruction at that address onto the bus, which is now in the data mode. The EPROM stores the operational routines for the 8031.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

At power-up, the reset circuit sets the 8031 program counter to zero and the 8031 starts executing its initialization code from the EPROM. The initialization routine performs the following tasks:

1. Configure internal UART to 62.5k baud
2. Configure line protocol (1 start bit, 8 data bits, 2 stop bits)
3. Load zeros to sound generator
4. Clear LEDs
5. Set up two internal timers

After initialization, the 8031 starts its X axis scan routine, continuously polling port 1 for an input from the X/Y matrix. The Keyboard keys are laid out in a 16 x 8 X/Y matrix for a total of 128 possible configurations. Not all possible configurations are used. The 8031 supplies three scan lines (A8, A9, A10) to the two 3-to-8 decoders. The three scan lines count in binary from zero to 7 for each of the two decoders, thus causing a strobe to occur sequentially from X_0 to X_{15}.

The Y lines in the matrix are the return lines to the 908 device. When a key is pressed, the capacitive reactance is sensed by the 908 device and the device translates the sense to a TTL level for the 8031. Upon receipt of the input from the 908, the 8031 reads the 908 input again to confirm the original read.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

The 8031 now looks in an internal table for the keycode that matches the Y location from the 908 device and the X location from the 3-to-8 decoders.

The keycode is then sent to the 8031's internal UART where it is serialized. A start bit and two stop bits are added and the serial stream is transmitted to the Electronics Base. After transmission of the last bit in the stream, the 8031 UART generates an internal interrupt which causes the 8031 to resume its X axis scanning routine.

The X portion of the X/Y matrix also serves to read the settings of the two on-board switchbanks. One side of each switch is connected to one of the X lines. Each X line is normally pulled up to 5V. The other side of each switch is connected to one common transistor. When an X line is strobed (brought low) and its switch is closed, the strobe is coupled through the switch to the transistor and the transistor changes state.

This pulse is applied to the 8031 as an interrupt at P3.2, and the 8031 registers the switch closure in an internal register dedicated to holding the switch settings. When an X line is strobed (brought low) and its switch is open, the transistor is unaffected and no interrupt occurs.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

The switch setting scan routine occurs after each X/Y matrix read routine. The switch settings can be read from the 8031's internal register anytime the Z-80 in the Elec- tronics Base issues a query command.

Communication from the Z-80 in the Electronics Base to the 8031 in the Keyboard occurs as follows. The command to the Keyboard is received by the 8031's internal UART, the start and stop bits are stripped and the command is looked up in a table in the 8031. The starting address of the routine associated with that command is put on the address bus, and the 8031 executes code from the EPROM to satisfy the particular routine.

The six LEDs located on the Keyboard PCB are under the control of the Z-80 CPU in the Electronics Base. The Z-80 CPU sends LED data serially to the 8031 in the Keyboard. The 8031 strips the start and stop bits and converts the serial data to parallel data. The LED data is then placed on port zero lines P0.0 - P0.7 and latched in the tri-state LED latch. The 8031 enables the LED latch, thus driving the LEDs with the data from the Z 80 in the Electronics Base. Any low output from the LED latch will illuminate the associated LED.

A programmable sound generator device provides the Keyboard with its beep and click sounds.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

Upon receipt of a beep or click command from the Z-80 in the Electronics Base, the associated routine is called from the EPROM.

The 8031 receives the appropriate data for the sound generator from the EPROM. This includes the data required to load the sound generator's attenuation and frequency registers to produce the desired sound. The data is latched from the data bus and then applied to the sound generator. A common operational amplifier is used to drive the speaker.

2.3 4230/4205 ELECTRONICS BASE

The standard 4230/4205 Electronics Base with no options houses one PCA which carries out all logic functions of the workstation. This PCA is referred to as the 4230 Workstation Electronics PCA, part number 210-8287, or the 4205 Workstation Electronics PCA, part number 210-8287-1. These PCAs are referred to in this section simply as the 8287 PCA. The information contained in this section is applicable to both the 4230 and the 4205 workstation Electronics PCA except where specifically noted.

Figure 2-4 is a functional representation of the single PCA workstation.

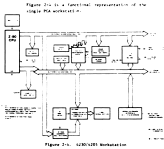


Figure 2-4. 4230/4205 Workstation Functional Block Diagram

2.3 4230/4205 ELECTRONICS BASE (Continued)

2.3.1 210-8287 CPU PCA

The 8287 CPU PCA contains three LSI (large scale integration) devices and their support logic, thus providing all logic required for workstation operation on a single board. The LSI devices are a Z-80 CPU, an 8031 microprocessor for the serial keyboard interface and a WL-2001 device which provides all the functions of a standard Wang 928 data link in a single LSI device.

Support logic for these main LSI devices includes 64k bytes of main memory with parity, a 4k PROM containing the Built-In Test (BIT) power-up diagnostic, and CRT RAM including 4k of character RAM, 4k of attribute RAM and 8k of font RAM. (The 4205 has only 4K of font RAM.) Another 4k PROM stores the operating program for the 8031 microprocessor.

The connector header mounted on the rear of the PCA contains the DATA LINK BNC/TNC connectors for cable connection to the host CPU as well as the connectors for the Monitor and Keyboard.

2.3.1.1 Z-80 Central Processor Unit (CPU)

Bus operations are controlled by the Z-80A CPU. The CPU receives sequential instructions from main memory over the data bus. It assigns device access and tasks based on these instructions and communicates with workstation logic through the data, address, and control buses.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.1 Z-80 Central Processor Unit (CPU) (Continued)

CPU signals are sequenced according to both its internal instruction set and instructions received from main memory over the data bus. The CPU requires a single, +5 Vdc supply and employs a 4 MHz clock as its time base.

Bidirectional data flow is accomplished by an 8-bit, tri-state data bus. The CPU transmits address information over a 16-bit, tri-state address bus. A reset line initializes the CPU and the six control-output lines. The six control-output lines are:

M1, CPU Fetch Cycle: This line is active during the first cycle (fetch cycle) of each instruction-request cycle, and during the special interrupt cycles.

MREQ, Memory Request: Active when the address bus holds a valid address for a memory read or write operation.

IORQ, Input/Output Request: Active when the lower half of the address bus holds a valid I/O address for an I/O read or write operation. Also becomes active for the interrupt acknowledge cycle.

RD, Read: When active, indicates that the CPU will input data while performing a memory-access or I/O instruction.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.1 Z-80 Central Processor Unit (CPU) (Continued)

WR, Write: When active, indicates that the CPU will output data while performing a memory-access or I/O instruction.

RFSH, Refresh: During an M1 (memory period 1) cycle, the CPU outputs an address for memory refresh. RFSH confirms the active presence of that address.

In addition to the control-output lines, there are three CPU input control lines. These lines are:

BUSRQ, Bus Request: An outside device can request bus access by asserting this signal. BUSRQ input causes the CPU to switch its address, data, and status lines into a high-impedance state to accommodate the outside device.

BUSAK, Bus Acknowledge: Becomes active to indicate that the CPU has complied with a BUSRQ.

WAIT: An outside device can request the CPU to extend the current memory access or I/O cycle by asserting this signal. The CPU waits as long as the signal remains asserted.

2.3.1.2 CPU Interrupts

The workstation employs Z-80 interrupt mode 0. In this mode, the CPU receives its next instruction from the interrupting device.

2.3.1.2 CPU Interrupts (Continued)

The workstation employs Z-80 interrupt mode 0. In this mode, the CPU receives its next instruction from the interrupting device. In the 4230/4205 Workstation, interrupts are received from the 8031 processor used for the Keyboard interface. The interrupt notifies the CPU that a keystroke has been received and is ready for processing.

Two interrupt inputs to the CPU are provided, maskable (INT) and nonmaskable (NMI). Keystroke interrupts are of the maskable type, while a non-maskable interrupt (unconditional entrance to the program) occurs only for a detected memory parity error.

2.3.1.3 Main Memory

Main memory consists of 64k bytes of dynamic RAM with one bit of parity for each byte of memory. Physically, memory is implemented with nine 64k x 1-bit devices. Main RAM can be accessed by both the CPU and the data link. (The data link is a DMA path.) The DRAM controller is responsible for generating row address strobe (RAS) and column address strobe (CAS) logic to address main memory. RAS and CAS lines enable 16-bit addresses to be processed in 8-bit, half-address form, permitting 16-bit main memory addresses to dynamic RAM devices with only eight address input pins.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.3 Main Memory (Continued)

RAS/CAS logic transfers high and low-order address bits through the same device pins at different times.

RAS/CAS cycles are required any time main memory is addressed. Main memory is addressed during these operations: CPU instruction fetch/refresh cycle, CPU data read, CPU data write and DMA transfer

2.3.1.4 Main Memory Parity Checking

Memory parity logic is one of two parity generation/detection circuits. The other circuit is part of the Data Link. Memory parity logic generates and then tests for even parity on all data transfers leaving or entering the CPU through the data bus. During a CPU write, each parity bit is calculated and stored in main memory.

The parity line is checked on each CPU read. If a memory parity error is detected, the diagnostic PROM is enabled and the CPU receives a non-maskable interrupt which causes it to jump to location '0066'. At that location in PROM is the main memory parity error routine which causes the contents of the CRT screen to be underlined, thus informing the operator of the error.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.4 Main Memory Parity Checking (Continued)

The underlining condition can be cleared only through a Z-80 RESET. In the 4230/4205, a RESET can be accomplished by cycling ac power to the workstation or, in some cases, by the host CPU.

Following workstation reset (restart), the diagnostic built-in test (BIT) runs and the usual power-up checks ensue. If the memory parity error was a soft error, the workstation will pass the BIT and be ready for operation again. During diagnostics, the parity detection circuitry itself is tested by forcing bad parity to be written and then reading back the same data location.

2.3.1.5 Address Assignments and Page Select Logic

The Z-80 CPU, with its 16 address lines, is capable of addressing up to 65,536 (64k) different memory locations. Many of the programs available on a host VS/OIS CPU require the full 64k of main memory within the 4230 workstation in order to run. Nevertheless, character, attribute and font memories comprise another large segment of memory that must be addressed as directed by CRT controlling routines within the workstation.
To overcome the limit placed upon the number of available addresses by the 16-bit address bus, a method of memory address assignments called page selection is used in the 4230/4205 Workstation.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.5 Address Assignments and Page Select Logic (Continued)

Page selection allows the same addresses to be assigned to more than one physical memory device. Thus, while both the main and CRT memories see the address lines from the CPU, only the memory that is enabled at the time responds to the current address on the bus.

Figure 2-5 is a simplified representation of the hardware used to implement the page select scheme. The central element in the page select hardware is the block memory decode PAL (programmable array of logic). The PAL is programmed to output the appropriate memory enables for the combination of inputs it receives. In the 4205, this PAL is programmed to inhibit main RAM addresses above 32k.

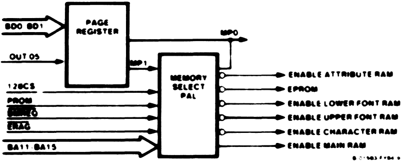


Figure 2-5. 4230/4205 Workstation Memory Page Select Logic

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.5 Address Assignments and Page Select Logic (Continued)

The available addresses are assigned differently for each of three pages available to the CPU for selection. The three pages and their ad- dress assignments are shown in Figure 2-6.

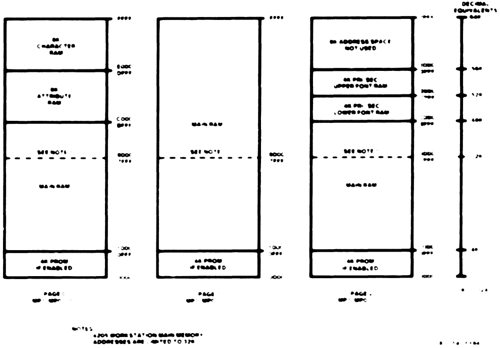


Figure 2-6. 4230/4205 Workstation Memory Addressing Assignments

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.5 Address Assignments and Page Select Logic (Continued)

The inputs to the PAL are listed below with a description of their function in the page selection scheme. Table 2-1 shows how the different inputs combine to decode blocks of memory addresses.

Table 2-1 Block Memory Decoding

CONDITIONS REQUIRED											
MEM. ADDRESSED	EPROM	MP1	MP0	128CS	ADDRESS	A15	A14	A13	A12	A11	A10-A0
EPROM	1	x	x	x	0K-4K	0	0	0	0	x	x
CHARACTER RAM	x	0	0	x	56K-64K	1	1	1	x	x	x
ATTRIBUTE RAM	x	0	0	x	48K-56K	1	1	0	x	x	x
LOWER FONT RAM	x	1	0	0	48K-52K	1	1	0	0	x	x
LOWER FONT RAM	x	1	0	1	48K-50K	1	1	0	0	0	x
UPPER FONT RAM	x	1	0	0	52K-56K	1	1	0	1	x	x
UPPER FONT RAM	x	1	0	1	52K-54K	1	1	0	1	0	x
MAIN RAM	0	x	x	x	0K-4K	0	0	0	0	x	x
MAIN RAM	x	x	x	x	4K-8K	0	0	0	1	x	x
MAIN RAM	x	x	x	x	8K-16K	0	0	1	x	x	x
MAIN RAM	x	x	x	x	16K-32K	0	1	x	x	x	x
MAIN RAM	x	x	x	x	32K-48K	1	0	x	x	x	x
MAIN RAM	x	x	1	x	48K-64K	1	1	x	x	x	x

Notes:

1. x = don't care
2. Main RAM addresses above 32k are inhibited in the 4205 Workstation.
3. The 4205 has only 4k of font memory versus 8k in the 4230.

2.3.1.5 Address Assignments and Page Select Logic (Continued)

MPO, MP1: The Z-80 CPU selects the appropriate page configuration (page 0, 1, 2) required for any operation by writing to the page register. Command OUT '05' clocks page select data off the data bus (BD0, BD1) and into the page register. The resultant lines MPO and MP1 (MP = memory page) are used as inputs to the memory select PAL.

PROM: An active PROM bit disables the lower 4k of workstation main memory and enables the 4k diagnostic PROM. All write cycles to the lower 4k of memory addresses are inhibited. All read cycles are called from the PROM regardless of what page is indicated by the page register.

128CS An active 128 character set bit inhibits all memory cycles to the upper 2k of the lower and the upper font memory. The font memory can contain two 256 character sets, requiring the total 4k lower font memory and 4k upper font memory. If a 128 character set is selected, however, this bit is used to prevent memory accesses outside of the selected character set.

BA11 - BA15: Address bits BA11 - BA15 determine which 4k block within the current page is to be accessed.

The memory request signal (BMREQ) and the eight-bit refresh generator signal (ERAG) from the Z-80 are also applied to the PAL for synchronizing its memory enable outputs.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.6 Programmable Read-Only Memory (PROM)

At power-up, the CPU executes code from the diagnostic PROM which is selected by the block memory decode logic. Sequential testing of different groups of logic is performed to verify the integrity of the workstation. During this phase, the data link is disabled. Upon successful completion of the tests, PROM is deselected and the data link is enabled. At this point, conventional data link downloading commences as though the workstation had just been powered-up.

2.3.1.7 I/O Decoders

The Z-80 uses IN and OUT instructions to transfer data to and from input/ output devices. The Z-80 design allows for 256 discrete I/O ports to be assigned using the eight least significant bits of the address bus (A0 - A7). An active IORQ from the CPU indicates that a valid I/O address is present on the lower half of the address bus. The I/O decoders decode these address lines to provide single chip enable lines for each I/O address.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.7 I/O Decoders (Continued)

The I/O port assignments for the 4230/4205 workstation are shown in Table 2-2.

Table 2-2 4230/4205 Workstation Input/Output Commands

COMMAND	DESCRIPTION
OUT00	Sounds Keyboard Clicker
OUT01	Sounds Keyboard Speaker
OUT02	Loads data into start column register
OUT05	Loads data into page register
OUT06	Selects primary character set
OUT07	Selects secondary character set
OUT09	Selects normal or reverse video
OUT0E	Diagnostic use
OUT10	TC Loopback Enable/Disable (4230 TC only)
OUT11	Sets TC baud rate (4230 TC only)
OUT12	Clears key pending interrupt (4230 TC only)
OUT13	Clears 10 msec interrupt (4230 TC only)
OUT14	Selects TC clock mode and sets/clears secondary RTS (4230 TC only)
OUT15	Writes data to USART (4230 TC only)
OUT16	Disables TC interrupts (4230 TC only)
OUT17	Enables TC interrupts (4230 TC only)
OUT20	Selects 256 or 128 character set
OUT21	Selects/deselects Arabic mode
OUT25	Writes commands to Keyboard
OUT35	Writes command or control information to USART (4230 TC only)
IN00	Reads serial Keyboard keystroke data
IN02	Reads TC status register (4230 TC only)
IN03	Reads interrupt status register (4230 TC only)
IN04	Reads installation status switches (4230 TC only)
IN07	Reads device type switch
IN08	Reads device type switch
IN15	Reads data from USART (4230 TC only)
IN35	Reads status from USART (4230 TC only)

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.8 Data Link

The 4230/4205 Workstation employs a recently introduced LSI device, the WL-2001, to carry out the standard Wang 928 data link functions.

The data link permits workstation memory to be loaded or read by the host CPU. The host CPU can write new memory instructions into workstation memory; it can also record (archive) information entered by the workstation onto a common disk. The workstation CPU is disabled when the host CPU uses the Data Link. During this time, the data link device provides bus synchronization and timing for direct memory access (DMA) read/write operations into and out of workstation main memory. DMA logic does not support CRT memory transfers.

The data link (Figure 2-7) permits the host CPU to transfer data at high speed between its main memory (or disk) and main memory in its peripheral subsystems.

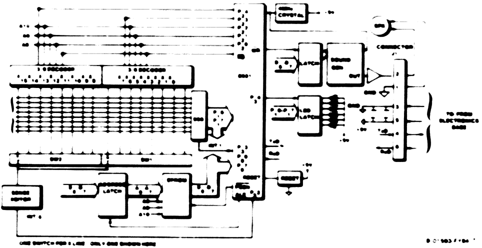


Figure 2-7. Data Link Device and Support Logic

2.3.1.8 Data Link (Continued)

In particular, the host CPU uses this link to load programs into workstations, store documents produced at workstations, and to feed high-speed printers. Each workstation is connected to the host CPU separately, through a radial bus structure. All transmissions are controlled by the host CPU.

Data is transferred directly between memories using a DMA path through the data link. Data transfer is carried out in a serial, asynchronous, byte-oriented format using a half-duplex line. The transmission line itself is a balanced pair of coaxial cables operating at 4M baud. The actual data transfer rate is approximately 260k bytes per second.

2.3.1.8.1 Data Link Commands

Data link commands are received over the serial data link and processed by the WL-2001 device, thus carrying out the functions commanded by the host CPU. Six Data Link commands permit the host CPU to:

- Check Slave STATUS and ID
- Initiate Slave Operation (RESTART)
- Load Slave Memory (WRITE - 2 commands)
- Store Slave Data (READ - 2 commands)

2.3.1.8.1 Data Link Commands (Continued)

STATUS and ID Commands

STATUS and ID commands send Slave status and ID to the host CPU on command. The STATUS read is the method a host CPU uses to interrogate a slave. Upon receipt of this command, the WL-2001 reads the external status register to obtain this information. Eight bits of information are transmitted from the slave as shown and described below:

```
                  MSB                             LSB
                  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                   |_______________| |_| |_| |_|
  Device Type___________|              |   |   |
     Memory PE_________________________|   |   |
Receive Error______________________________|   |
     Not Ready_________________________________|
```

Not Ready: A high level indicates to the host CPU that the slave is not running.

Receive Error: A high level indicates to the host CPU that the slave has detected either a line parity error or line framing error (non-contiguous bytes in a message stream) during a transmission from the host CPU to the slave.

2.3.1.8.1 Data Link Commands (Continued)

Main Parity Error: A high level indicates the slave has detected a parity error in its own memory. In on-line applications, this bit would not be seen because the data link would be disabled, an NMI would occur and the CPU would read its memory parity routine from the diagnostic PROM.

Device Type: defines the type of slave on the data link.

RESTART Command

The RESTART command causes the WL-2001 to activate a signal (DLCL, data link clear) which can be used to reset the slave CPU. While this signal is not used in the 4230/4205 Workstation, the RESTART command is used to generate a data link restart command via the data link function lines. These lines, in turn, are decoded and a RESTART signal is applied to the power-up reset logic, thus causing a power-up reset of the workstation.

WRITE and READ Commands

WRITE and READ commands may each transfer either 1 byte or 256 bytes. A one-byte command transfers a single DMA cycle. A 256-byte command transfers a single page of data (1 page = 256 bytes).

2.3.1.8.1 Data Link Commands (Continued)

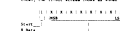
In response to any of the following commands, the WL-2001 device gains control of the Z-80 data, address and control lines via built-in DMA controls (see section 2.3.1.8.5).

1-Byte Read: This instruction is followed by two bytes indicating the address to be read from the slave's main memory. Address information is transferred to the slave (workstation) in half-address form, in order to accommodate 16-bit addresses on the 8-bit data link data bus. The WL-2001, upon latching the address, requests control of the Z-80 bus and then reads the appropriate memory location. This data is transmitted to the host CPU along the serial data link.

1-Byte Write: This instruction is similar to the 1-byte read (above), but the address is followed by a single byte of data. The data is stored in a WL-2001 internal register until memory access has been granted. The byte of data is then written into workstation main memory and the data link device returns to its receive state.

256-Byte Write: This instruction is followed by a starting address and then 256 bytes of data to be written sequentially into workstation main memory.

256-Byte Read: This instruction is followed by a starting address for a sequential memory transfer of 256 bytes of data from workstation main memory to the host CPU.



2.3.1.8.2 Data Link Receive Functions

The WL-2001 device receives commands and data via the balanced serial data link line from the host CPU. Data is first applied to a line receiver and then sent to the WL-2001 on the data link receive (DLR) line.

After power-up of the 4230/4205 Workstation, the WL-2001 idles in its receive mode, monitoring the data link receive input of the device. This means it is waiting for a command from the host CPU, which is indicated by the start bit of the 11-bit line protocol used in the data link. In total, the 11-bit stream looks as shown below.

```
       |1 | X | X | X | X | X | X | X | X | X | 0|
       |_| |MSB____________________________LSB| |_| |_|
Start___|                  |                      |   |
8 Data_____________________|                      |   |
Evev Parity_______________________________________|   |
Stop__________________________________________________|
```

The WL-2001 internal clock rate allows four clock cycles for each bit time. When it senses an active line (high) for two consecutive samples, a start bit is assumed to have been received and the device synchronizes itself internally so that the following data bits are sampled near their center. After the appropriate number of clock cycles have occurred for the 11-bit stream, the internal start bit detector is reset, thus allowing for variations in the transmission data rate on a byte-by-byte basis.

2.3.1.6.2 Data Link Receive Functions (Continued)

The sampled data bits are serially loaded into an 8-bit shift register inside the WL-2001. Together, the internal start bit detector and shift register function as an asynchronous receiver/transmitter to convert serial data to parallel data for use by the WL-2001 device. The received byte of data is either transferred to the internal instruction decoder or to an external register such as the low or high byte address register, or the data bus transceiver.

Internally, the WL-2001 checks received data for line parity and for framing errors. Parity is checked by calculating the parity bit for the data byte as it was received and comparing it to the parity bit sent with the data byte. If the two parity bits are not the same, the receive error (RE) line is activated.

Framing errors are gaps in the data stream. After a valid multiple byte instruction is received and the WL-2001 is expecting additional data bytes from the host CPU, a framing error will be indicated by the start bit detector being active for more than six clock samples, or 1.5 bit times. The receive error (RE) line is activated to indicate framing errors.

2.3.1.8.3 Data Link Transmit Functions

Data transmission from the WL-2001 to the host CPU is controlled by two lines, data link transmit enable (DLXEN) and data link transmit (DLT). When a transmission from the slave (workstation) to the host CPU is required, DLXEN is asserted while DLT is deactivated for a minimum of one byte time. During this one byte time, the appropriate external register is accessed (either status or data) and the data to be transmitted is loaded into the WL-2001.

The DLT line is then forced active for one bit time, thus forming the start bit of the line protocol for the host CPU. The WL-2001 internal shift register is loaded with the data to be transmitted and it is shifted serially to the DLT line, MSB first. After the 8-bit stream is shifted out, parity is appended and then a stop bit is sent. The parity bit sent to the host CPU is the main memory parity bit stored with that particular byte of data in the case of workstation main memory reads. Parity for all other data bytes is calculated within the WL-2001 and appended as the data is shifted out onto the line. If subsequent bytes of data are to be transmitted to the host CPU, they are loaded into the WL-2001 while the previous byte is being shifted out.

2.3.1.8.4 Line Turn-Around

Line turn-around control is also provided by the WL-2001 device, with two internal registers provided to set line turn-around delays. Line turn-around control ensures that the WL-2001 is ready to receive commands from the host CPU and also introduces a preset delay between transmit and receive operations on the half-duplex line. The delay allows the line to quiet between transmit and receive operations.

The interval from the reception of the last instruction or address byte from the host CPU to the beginning of a transmission to the host CPU is referred to as turn-around-time 1. Conversely, after the last byte has been transmitted to the host CPU, the interval until the start bit detector is reenabled is called turn-around-time 2. In the 4230/4205 Workstation, these turn-around times are preset to 8 and 7 microseconds respectively.

2.3.1.8.5 Direct Memory Access (DMA) and Z-80 Bus Arbitration

The WL-2001 provides a complete complement of control signals for direct memory accesses. All host CPU accesses to workstation main memory are DMA paths through the WL-2001 device. In addition, the device uses another set of control lines to allow any other devices to directly access workstation main memory. This additional DMA provision is referred to as a DMA2 operation.

2.3.1.8.5 Direct Memory Access (DMA) and Z-80 Bus Arbitration

In the 4230 Workstation, DMA2 accesses are used to support data transfers to and from the option PCA.

When either the host CPU or a DMA2 device requests a main memory access, the WL-2001 device generates a bus request signal which is forwarded to the Z-80 (slave) CPU. This signals the slave CPU that a DMA request is pending, and that it should give up control of its buses within 3.5 microseconds. The timing constraint ensures that the data and address buses will be free as soon as the incoming data byte arrives, since the WL-2001 provides no data buffering.

When the Z-80 CPU has placed its buses in the high impedance state, the WL-2001 is signaled with a bus acknowledge signal. When the WL-2001 senses bus acknowledge, and at the end of each DMA cycle, the device arbitrates between all bus requests to determine which request will be granted. The following priorities are observed:

1. Any memory operation in progress
2. Data link (host CPU) requests
3. DMA2 requests
4. Slave CPU operations

The WL-2001 provides the required memory interface signals during DMA operations including memory request and memory write (an inactive memory write indicates a read operation).

2.3.1.8.5 Direct Memory Access (DMA) and Z-80 Bus Arbitration

An additional signal, data valid, is used to signal the WL-2001 that valid data exists on the data bus or that write data has been latched. The data valid signal is generated in the DRAM control logic and applied to the WL-2001. Timing is such that, when the data valid line is active, the memory refresh function can be carried out (RAS-only memory cycle). Thus, in-between direct memory accesses, the DRAM is refreshed.

The DMA2 controls provide a means for devices other than the host or slave CPU to access workstation main memory. These controls are used in the 4230 Workstation to support data transfers to and from the option PCA. DMA2 accesses are single byte reads or writes only. The device requesting the DMA2 must provide a valid address (and data, in the case of a memory write) on the Z-80 (slave) data bus. DMA2 requests are granted only if no host CPU DMA requests are pending.

2.3.1.8.6 Data Link Functions and Function Decoding

A multiplexing scheme is used to transfer data in and out of the WL-2001 device. Data transfers occur over the 8-bit bidirectional data link data bus, DLD0 - DLD7. A ninth line is used to transfer the main memory parity bit when reading from workstation main memory.

2.3.1.8 Data Link (Continued)

2.3.1.8.6 Data Link Functions and Function Decoding (Continued)

The data link data bus is connected to four registers, each serving to latch data from or drive data onto the bus. These registers are the status register, the data bus bidirectional transceiver, the high-byte address register and the low-byte address register.

The function and direction of the data on the data link data bus is under control of the data link function decode lines, DLFA - DLFD, providing up to 16 possible decoded commands. In the 4230/4205, three of these lines are decoded to provide six different commands used to control the four registers connected to the data link data bus. These commands are shown below.

DLFD	DLFC	DLFB	DLFA	FUNCTION
0	0	1	0	Latch Address High
0	0	1	1	Latch Address Low
0	0	0	1	Enable Write
0	1	0	1	Enable Read
0	1	0	0	Status Read
0	1	1	1	Data Link Restart

The first five of these lines are represented on the diagram in Figure 2-7 as control lines, acting as enables for the associated registers. The data bus transceiver requires both an enable and a direction control line. The sixth command is data link restart which is sent to the power-up reset logic.

2.3.1.8 Data Link (Continued)

2.3.1.8.6 Data Link Functions and Function Decoding (Continued)

Upon decoding a data link restart, the 4230/4205 Workstation is forced into a power-up restart cycle, as if the unit had just been turned on.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.9 Serial Keyboard Interface

The serial keyboard interface to the Z-80 CPU uses an 8031 microprocessor, the same microprocessor used in the Keyboard itself. The 8031 device is a single-component, 8-bit microprocessor that contains 128 x 8-bit internal RAM, an internal oscillator and timing circuit for data synchronization, and a full duplex serial port UART. The 8031 device requires one supply voltage (+5 volts) for operation. A 4 MHz crystal-generated clock is used for synchronization. Keyboard data is either sent or received across the full-duplex Keyboard interface. (Refer to Figure 2-8.)

2.3.1.9.1 8031 Program Storage and Retrieval

The 8031 uses its port zero lines as both the data and the address bus in a multiplexed bus scheme. Lines P0.0 - P0.7 in Figure 2-8 identify the shared bus. Signal ALE (address latch enable) enables the address latch when the bus is in the address mode, thus storing an address in the latch.

2.3.1.9 Serial Keyboard Interface (Continued)

2.3.1.9.1 8031 Program Storage and Retrieval (Continued)

The address latch addresses the EPROM, along with additional address lines A8 - A11 from port 2 lines P2.0 - P2.3. Signal PSEN (program store enable) enables the EPROM to output the instruction at that address onto the bus, which is now in the data mode. The EPROM stores the operational routines for the 8031.

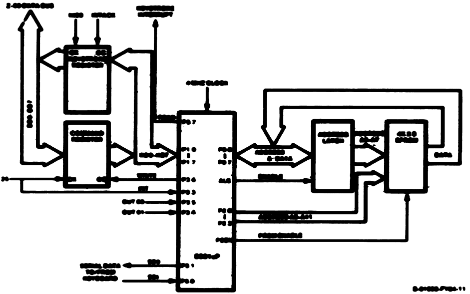


Figure 2-8. 4230/4205 WS Keyboard Interface

2.3.1.9 Serial Keyboard Interface (Continued)

2.3.1.9.2 Initialization (Continued)

At power-up, the 8031 is reset, thus setting the internal program counter to zero. The 8031 then starts executing its initialization code from the EPROM. The initialization routine configures the internal UART to 62.5k baud and sets line protocol to 1 start bit, 8 data bits and 2 stop bits. This matches the line protocol configured in the serial Keyboard.

2.3.1.9.3 Receiving Keystrokes

Upon receipt of a keystroke from the serial Keyboard (SDI, serial data in), the 8031 loads a restart instruction ('C7') into the keystroke register. Since the CPU is set for mode zero interrupts, the interrupting device must provide the CPU with the next instruction. This next instruction for the CPU is the restart instruction stored in the keystroke register.

After the restart instruction is loaded, a keystroke interrupt is issued by the 8031 to the Z-80 CPU. The CPU, in response to the keystroke interrupt, generates an interrupt acknowledge (INTACK) which reads the restart instruction from the keystroke register onto the data bus. The restart instruction loads the program counter in the CPU with the location of the keystroke servicing routine.

2.3.1.9 Serial Keyboard Interface (Continued)

2.3.1.9.3 Receiving Keystrokes (Continued)

During the time that the CPU is jumping to the keystroke routine, the 8031 loads the received keycode into the keystroke register. The CPU issues an IN '00' as part of the keystroke routine, which reads the keystroke onto the data bus for use by the CPU.

2.3.1.9.4 Transmitting Commands

The CPU can issue one-byte commands to the Keyboard via the 8031 interface, using the OUT '25' instruction. These commands are used for switching the Keyboard LEDs and a variety of other purposes detailed in the section on Keyboard theory of operation.

The one-byte command is loaded into the command register with the OUT '25' instruction. OUT '25' is also used as an interrupt for the 8031 to inform it of the pending command to be transmitted. The 8031 reads the command register onto its data bus using the write signal (P3.3), performs a parallel-to-serial conversion via its internal UART, appends the required start and stop bits and transmits the command to the Keyboard (SDO, serial data out).

2.3.1.9 Serial Keyboard Interface (Continued)

2.3.1.9.5 Beep and Click Functions

The Keyboard responds to every keystroke, legal or not in any particular software program, with either a beep or a click. Since these are high-usage, repetitive functions, the required routines to send beep and click commands to the Keyboard are stored in the 8031's EPROM. Instructions OUT '00' and OUT '01' call the click and beep routines (respectively) from the EPROM, causing the the associated keyboard commands to be transmitted to the Keyboard.

2.3.1.10 CRT RAM, Character Generation and CRT Display

A simplified representation of the CRT character generation and display circuits is shown in the block diagram of Figure 2-4 as four blocks, CRT timing control, CRT RAM address multiplexers, CRT RAM and video serialization. These blocks are expanded and shown in more detail in Figure 2-9, the CRT RAM addressing and character generation block diagram. Figure 2-9 is discussed in detail in the sections that follow.

2.3.1.10.1 Character RAM

The amount of RAM allocated for character storage is 4k bytes, or sufficient to store 25 rows of 160 characters or columns. (25 x 160 = 4000.) The CRT displays only 80 of these character columns at any time.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.1 Character RAM (Continued)

The remainder of the characters in memory can be displayed by exercising the horizontal scrolling capability of the workstation. The Z-80 CPU must enable page zero of its address assignments to access character RAM. Page zero allocates 8k of addresses for character memory, from 56 to 64k, though only 4k is used. In the 4205, character memory is limited to 96 characters per line.

The CPU addresses are multiplexed with the row and column addresses generated in the CRT timing control logic. The resulting address allows the CPU to select the three most significant bits of the address. When addressing character memory, it selects a starting address of 56k to coincide with the address assignments for character memory. The row and column addresses select which location in the next 4k of memory space will be used to store a particular character. The result of address multiplexing for the character RAM is shown below.

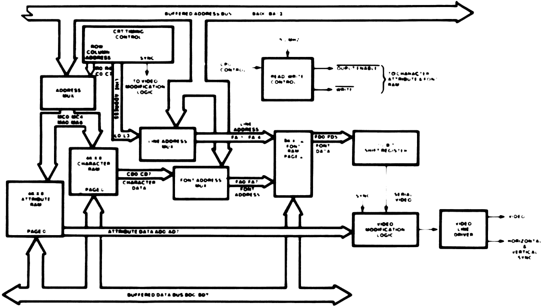
Z-80 Address	A15	A14	A13	A12	A11	A10	A09	A08
CRT Address	1	1	1	R04	R03	R02	R01	R00

Selects 56k address range

Addresses rows 0 - 24

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.1 Character RAM (Continued)



NOTES

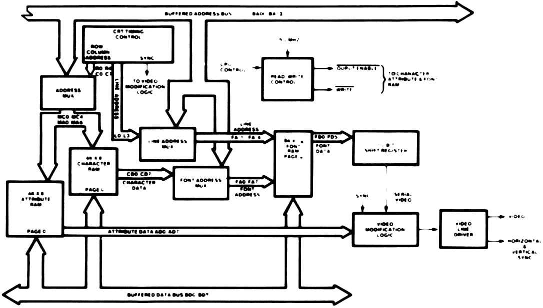
1. 4206 WORKSTATION USABLE CHARACTER AND ATTRIBUTE RAM IS LIMITED TO APPROXIMATELY HALF THAT SHOWN (80 CHARACTERS PER LINE ONLY)

2. 4206 WORKSTATION FONT RAM IS 4K X 12

Figure 2-9. CRT RAM Addressing and Character Generation

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.1 Character RAM (Continued)



NOTES

1 4206 WORKSTATION USABLE CHARACTER AND ATTRIBUTE RAM IS LIMITED TO APPROXIMATELY HALF THAT SHOWN (80 CHARACTERS PER LINE ONLY)

2 4206 WORKSTATION FONT RAM IS 4K X 12

Figure 2-9. CRT RAM Addressing and Character Generation

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.1 Character RAM (Continued)

Z-80 Address	**A07**	**A06**	**A05**	**A04**	**A03**	**A02**	**A01**	**A00**
CRT Address	**C07**	**C06**	**C05**	**C04**	**C03**	**C02**	**C01**	**C00**

Addresses columns 0 - 159

Character RAM is loaded by the CPU via the Z-80 bidirectional data bus, allowing the CPU to load an ASCII character code into each 8-bit location in character memory. These ASCII codes are used to generate font addresses in the font address multiplexer. The codes are transferred over lines CD0 - CD7. Read/write control for character RAM is generated in the read/write control logic.

2.3.1.10.2 Dot Matrix Display

Characters are formed on the CRT screen by a 16-line by 12-pixel matrix. ("Pixel" is short for "picture element" and is the smallest division of the CRT screen that can be displayed.)

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.2 Dot Matrix Display (Continued)

The CRT displays only 12 lines of 10 pixels per character as shown in Figure 2-10. Alphanumeric and special characters are created by illuminating a specific pattern of pixels within the matrix associated with each character position. A horizontal group of matrices form a character row. Twenty-five rows can be displayed on the CRT screen. Eighty character columns can be displayed in each character row.

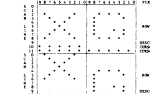


Figure 2-10. 4230/4205 WS Character Matrix

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.3 Font RAM

In order to display a character stored in character memory, a corresponding pixel pattern must be available for each character. This is the function of font memory. Within font RAM, a pixel pattern is stored for each character available in the workstation's character set.

The 4230 Workstation provides sufficient font RAM to store a 512 character set. Considering a total of 192 pixels per character (12 x 16 = 192), 512 characters would require 512 x 192 = 98,304 memory locations to store a character set of this size. Font RAM in the 4230 Workstation is 8k x 12, or 8192 x 12 = 98,304, and thus large enough to accommodate the 512 character set. The Z-80 CPU must enable page 2 of its address assignments to access font RAM. Page 2 allocates 8k of addresses for font memory. (The 4205 Workstation, with its 256 character set, uses a 4k x 12 font memory, one half the size of the 4230.)

The four lines of pixels within font memory that are not normally displayed (lines 12 to 15) are loaded with logic 0. These four blanked lines of pixels are used for superscript or subscript characters. When a superscript character is displayed, a value of two is added to the CRT line counter value. This causes the font data for scan line 2 to be presented to the CRT circuitry when scan line 0 is normally displayed, and so on for the entire character. The result is that font data for scan lines 2 through 13 are displayed for the current character.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.3 Font RAM(Continued)

A subscript character is displayed in a similar manner. A value of fourteen is added to the CRT line counter value. This causes font data for scan lines 14, 15 and 0 through 9 to be displayed for the current character. The vertical positions for the underline and cursor are fixed.

The pixel patterns stored in font RAM are loaded via the microcode sent to the workstation at its initial program load (IPL). This approach allows fonts to be changed for different applications.

Font data for each character is received over the 8-bit Z-80 data bus which allows only eight pixels to be loaded at a time. The remaining four pixels are loaded with another byte from the Z-80. For this reason, font memory is divided into lower and upper portions. Lower font memory stores pixels 0 through 7, while upper font memory stores pixels 8 through 11. In the 4230, lower font memory occupies address space 48k to 52k while upper font memory occupies address space 52k to 56k. In the 4205, only half of these addresses are used. Use of the Z-80 data bus for loading font RAM is illustrated in the next frame.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.3 Font RAM (Continued)

Z-80 Data	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
Pixel	7	6	5	4	3(11)	2(10)	1(9)	0(8)

Font RAM addresses are generated by multiplexing the character data from character RAM, line addresses from the line address multiplexer and CPU addresses from the Z-80 address bus. The Z-80 address controls the four most significant bits of the font address and uses these to select an address range starting at 48k or 52k for either lower or upper font RAM. Character data lines CD0 - CD7 select which pixel pattern is to read out of font RAM. Line addresses select which of the sixteen lines within the pixel pattern is to be read out of font RAM. The result of address multiplexing for font RAM is shown below. Read/write control for font RAM is generated in the read/write control logic.

```
                  Z-80 Address | A15 | A14 | A13 | A12 |
                  Font Address |  1  |  1  |  0  |  0  |
                               |_____________________|
Selects Lower Font RAM,                  |
48k Address Range________________________|
```

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.3 Font RAM (Continued)

```
        Z-80 Address | A15 | A14 | A13 | A12 |
        Font Address |  1  |  1  |  0  |  1  |
                     |_______________________|
Selects Upper Font RAM,          |
52k Address Range________________|
```

```
Z-80 Address |A11|A10|A09|A08|A07|A06|A05|A04|
Font Address |CD7|CD6|CD5|CD4|CD3|CD2|CD1|CD0|
             |_______________________________|
Selects Pixel Pattern______|
```

```
        Z-80 Address | A03 | A02 | A01 | A00 |
        Font Address | L03 | L02 | L01 | L00 |
                     |_______________________|
Selects 1 of 16 lines          |
in pixel pattern_______________|
```

2.3.1.10.4 Character Serialization

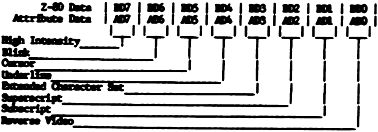
A 10-bit shift register is used to transform the parallel font data to a serial stream of data that can be used by the CRT. Font data is received from font RAM over lines FD0 - FD9, serialized and then sent to the video modification logic.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.5 Attribute RAM

Attribute memory stores information that controls how characters appear on the CRT, whether they are underlined, blinking, highlighted or in some other condition. Since these attributes can be different for each character, attribute RAM contains one byte of data for each byte of character RAM. The Z-80 CPU must enable page zero of its address assignments to access attribute RAM. Page zero allocates 8k of addresses for attribute memory, from 48 to 56k, though only 4k is used.

The description of character memory addressing in section 2.3.1.10.1 is the same for attribute RAM. Refer there for a complete description. Read/ write control for attribute RAM is generated in the read/write control logic. Data format for the attribute memory is shown below.



2.3.1.10.6 Video Modification Logic and Video Line Driver

All character-related data is finally merged in the video modification logic. This circuit receives serialized character data from the 10-bit shift register, synchronization signals from the CRT timing control logic and attribute data from attribute RAM. The incoming pixel stream is modified according to the attribute data for that character.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.6 Video Modification Logic and Video Line Driver (Continued)

These three conditions are black (off), normal intensity, or high intensity. These two bit-streams are joined by the horizontal and vertical synchronization signals and all four of the signals are then driven by a differential line driver to the CRT.

2.3.1.10.7 CRT Timing Control Logic

The CRT timing control logic controls the horizontal and vertical beam position for the CRT via its synchronization signal outputs. It also generates row/column addresses for character and attribute RAM and line addresses for font RAM. These addresses are generated in synchronism with the CRT horizontal and vertical sync signals, thereby causing the line of pixels corresponding to the current CRT beam position to be driven to the Monitor.

2.3.1.10.8 Read/Write Control for Character, Attribute and Font RAM

The character, attribute, and font RAMs are shared by the CPU and the CRT timing logic. The CPU generates the image in memory and the CRT timing logic displays the image on the CRT.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.8 Read/Write Control for Character, Attribute and Font RAM (Continued)

The read/write control timing originates from a 19.2 MHz crystal oscillator which provides the time base for the read/write logic.

The CRT logic has the highest priority when accessing character, attribute or font memory. If the CPU needs to access any of these memories, it must wait until the CRT logic operation is complete. The transfer to or from the CPU is then given 260ns to take place. A temporary storage register holds the data during a read operation since the CPU is too slow to read the memory without causing flicker in the display. This interleaving ensures that the CRT display will remain flicker-free by allowing the CRT logic to access the character, attribute, and font memories immediately when new data is required.

2.3.1.10.9 Character Set Control (4230 Only)

There are two 256 character sets which occupy the same address space (48k to 56k) in font memory. The selection of the primary or secondary character set is controlled by an OUT '06' or OUT '07' command.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.9 Character Set Control (4230 Only) (Continued)

The selection of a character set can also be controlled on a character by character basis. Attribute bit three selects the extended character set when it is active. When the primary character set is selected, the secondary character set becomes the extended character set. If the secondary character set is selected, the primary character set becomes the extended character set. By utilizing attribute bit three, both the primary and secondary character sets can be used as a single 512 character set.

The software may instruct the hardware to appear as though there are two 128 character sets by executing an OUT '20' command. The hardware will inhibit all font memory accesses outside of the two 128 character sets. In this mode a maximum of 256 characters may be accessed.

2.3.1.10.10 Horizontal and Vertical Scrolling

Vertical scrolling of information on the CRT is controlled by software. The character and attribute data is read one screen location at a time and rewritten to the screen location one row above its original position. This is repeated until the entire screen has been vertically scrolled upward by one row.

2.3.1.10 CRT RAM, Character Generation and CRT Display (Continued)

2.3.1.10.10 Horizontal and Vertical Scrolling (Continued)

Horizontal scrolling is controlled by hardware. A start column value is loaded into a start column register by an OUT '02' command. The start column value can range from 0 to 80 (decimal) inclusive. The CRT will display the first character corresponding to the start column value on the left edge. The next 79 characters will follow from left to right. For example, if the start column value is 29, the 29th to the 108th character will be displayed on each line. Rows 0, 23 and 24 will always display characters zero to 79, that is, they cannot be horizontally scrolled. In the 4205 Workstation, a maximum of 96 characters per line can be displayed and thus horizontal scrolling will only be effective to display the remaining 16 characters not already displayed on the 80 character screen.

2.4 4230 TELECOMMUNICATIONS (Optional)

Telecommunications is supported on the 4230 64K workstation by utilizing the Z80 microprocessor and TC functions on PCA 210-8298. This optional board is loaded above the 210-8287 in the 4230 Electronics Base. The workstation can support a variety of asynchronous and synchronous communication protocols when loaded with the appropriate microcode. A typical 4230 TC local configuration is shown in Figure 2-11.

4230 Workstation

Figure 2-11. 4230 TC Local Configuration

2.4 4230 TELECOMMUNICATIONS (Optional) (Continued)

The 64k 4230 workstation is connected to a modem by an RS-232-C cable running between the modem and the workstation modem connector. If the modem is supplied by the telephone company, they are responsible for the modem connection (figure 2-12).

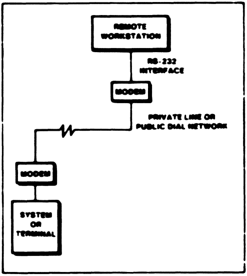


Figure 2-12. Remote TC Configuration

2.4 4230 TELECOMMUNICATIONS (Optional) (Continued)

2.4.1 FUNCTIONAL THEORY

Telecommunications logic resides on the 210-8298 PCA. The major logic functions are:

- o USART (Conversion)
- o Data Input/Output
- o Decoders
- o Modem Interface

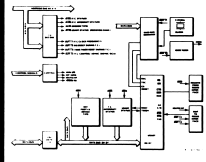


Figure 2-13. 210-8298 Telecommunication PCA Functional Block Diagram

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.1 8251A USART

THE 8251A USART (Universal Synchronous/Asynchronous Receiver/Transmitter) is programmed by the CPU to operate using 2780, 3780, WPS, TTY, or 2741 protocols. When the desired protocol has been selected, the CPU sends a set of control words to the USART that program Baud Rate, Character Length, Number of Stop Bits, Synchronous or Asynchronous Operation, and Even, Odd, Off, Mark, Space, and Parity. The USART then accepts data characters from the CPU in parallel format and converts them into a continuous serial data stream for transmission. It can simultaneously receive serial data streams via the modem and converts them into parallel data characters for the CPU.

Internal device timing for the USART is provided by a 2.45 MHz clock circuit. Transmit clock and receive clock are derived from this clock circuit.

2.4.1.2 Data Input/Output

During a transmit operation, data is received from the CPU in a parallel format via a bi-directional driver. The bi-directional driver is controlled by the Z80A CPU which enables/disables the driver as well as selects the direction of the data flow. The data (D7-D0) is gated into the USART where it is converted into serial stream format, gated to the transmit driver and sent to the 25-pin RS-232-C connector interface.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.2 Data Input/Output (Continued)

During a receive operation, data is received by the RS-232 receive circuitry in a serial stream format and gated into the USART where it is converted into a parallel format. The data is then sent through the bi-directional driver and presented to Z80A CPU via the data bus.

2.4.1.3 "In"/"Out" Decoding

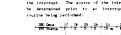
The Z80A CPU uses "IN" and "OUT" command instructions to send or receive control or status information to and from the TC PCA. These instructions are described individually in the following sections. When setting control bits and reading status bits, a logical ON condition is represented by a "1" bit, and a logical OFF condition is represented by a "0" bit.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

IN'02' Read Modem Status Signals

The IN'02' instruction interrogates the status of the various signal lines of the RS-232-C connector. This command returns the connector status in the following format:



IN'03' Read Interrupt Status

The IN'03' instruction interrogates the interrupt status register. The interrupt status register is read by the Z80A CPU to determine what caused the interrupt. The source of the interrupt must be determined prior to an interrupt service routine being performed.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

IN'04' Read Telecommunications Port ID Switch

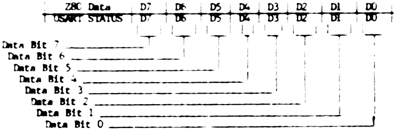
Located on the Telecommunication PCA is a 5-bank switch denoted SW1. When set, this switch indicates the Telecommunications address. The switch is read by the Master unit (via the Z80A) with an IN'04' instruction. The data pattern read is related to the switch positions of SW1. The switch positions read is in the following format:

Z80 Data	D7	D6	D5	D4	D3	D2	D1	D0
TC SWITCH	0	0	0	SW1	SW2	SW3	SW4	SW5

Always Set
Switch 1 Setting
Switch 2 Setting
Switch 3 Setting
Switch 4 Setting
Switch 5 Setting

IN'15' Input Received Character from USART

A received character is input from the USART by the Input Received Character instruction. This clears the receiver ready condition and the interrupt condition which it causes. If a transmission character of fewer than 8 bits is being used, the character to be transmitted is right adjusted in the byte input into the accumulator. This command returns the interrupt status in the following format:



2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

IN'35' Read USART Status

The IN'35' instruction is used to read the USART status register. This command returns the USART status in the following format:

Z80 Data	D7	D6	D5	D4	D3	D2	D1	D0
USART STATUS	DSR	SBD	FE	OE	PE	TXE	RXR	TXR

Data Set Ready
Sync/Break Detect
Framing Error
Overrun Error
Parity Error
Transmitter Empty
Receiver Empty
Transmitter Ready

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

OUT '10' Internal Loopback

The Internal Loopback instruction enables/disables the loopback function. This instruction is used by the Built-In-Test (B.I.T.) to verify correct operation of the TC Option board. An OUT '10' instruction with data of '01' (bit D0 set) enables the loopback test. An OUT'10' instruction with data of '00' disables loopback. This OUT instruction (when D0 is set to 1) requires a loopback connector be used on the RS-232-C Connector. Refer to paragraph 2.4.4 for loopback connector description. The command and data format is as follows:

OUT'12' Clear Keyboard Interrupt

The OUT'12' instruction clears the Key pending interrupt. The data byte supplied with the instruction is irrelevant.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

OUT'13' Clear 10 msecond Interrupt

The OUT'13' instruction clears the 10 msecond (millisecond) interrupt. The data byte supplied with the instruction is irrelevant.

OUT'11' Set Internal Clock Rate

The OUT'11' instruction is used to set the baud rate of the USART. For asynchronous communications, the USART Baud Rate Factor must also be set by a USART mode instruction. The table below list the possible baud rates and the associated data bit pattern.

Baud Rate	OUT '11' DATA Aysnc Mode	OUT '11' DATA Sync Mode	USART Baud Rate Factor
50	'40'		1
75	'80'		1
100	'A0'		1
110	'A9'		1
134.5	'B9'		1
150	'C0'		1
200	'D0'		1
300	'E0'		1
600	'F0'		1
1200	'F8'		1
2400	'F0'	'01'	0
4800	'F8'	'80'	0
9600	'FC'	'C0'	0

Note: When the on-board clock is used to provide a synchronous clock signal, the Baud Rate Select Code is different from that used for asynchronous clock signal.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

OUT'14' Set Secondary Request to Send and Clock Mode

The OUT'14' instruction is used to select BISYNC or ASYNC clock mode. This instruction is also used to set and clear the Secondary Request to Send signal. The modem control signal Secondary Request to Send (SRS, bit D4) and the Select Asynchronous Clock/Select Bisync Clock bit (bit D0) are set at power up. The command and data format is as follows:

OUT'16' Disable Telecommunications Interrupts

An OUT'16' instruction disables the 10 msecond, transmitter, receiver, and Key pending interrupts. All the telecommunications interrupts are disabled after power-on or a datalink restart. No data is required with this instruction.

OUT'17' Enable Telecommunications Interrupts

An OUT'17' enables the interrupts after the interrupts have been disabled and after a interrupt service routine has been successfully serviced. No data is required with this instruction.

OUT'15' Output Character to USART for Transmission

The OUT'15' instruction is used to write a character into the USART's transmit register. This clears the transmitter ready condition and the interrupt condition which it causes. If a transmission character of fewer than 8 bits is being used, the character to be transmitted is assumed to be right adjusted in the byte output from the accumulator.

OUT'35' Set USART Mode/Command Data

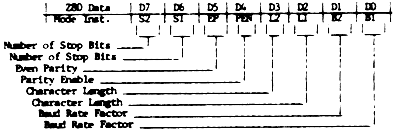
The OUT'35' instruction is used to send mode, command, and sync information to the USART. The interpretation of the byte of data output by the SET USART Mode/Command instruction is determined by the state of the USART. Following a reset of the USART, which can be caused by either a power-on condition or a bit in the Command Word, the first byte output by this instruction is interpreted as a Mode instruction.

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

If the Mode instruction selects asynchronous mode, all bytes subsequently output by the instruction (unless they specify an internal reset) are Command Words. If the Mode instruction selects synchronous mode, the next one or two bytes, as determined by the Mode instruction, output by the instruction define the synchronization pattern. All subsequently bytes output by the instruction are command words. The mode instructions for asynchronous and synchronous modes are as follows:

Asynchronous Mode



Number of Stop Bits (D7 and D6)

S2	S1	M
0	0	Invalid
0	1	1 Stop Bit
1	0	1.5 Stop Bits
1	1	2 Stop Bit

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

Even Parity Generation/Checker (D5)

D5 = 1 denotes Even Parity, D5 = 0 denotes Odd Parity

Parity Enable (D4)

D4 = 1 denotes parity enabled, D4 = 0 denotes parity disabled

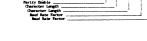
Character Length (D3 and D2)

D3	D2	Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Baud Rate Factor (D1 and D2)

D1	D0	Factor
0	0	Sync Mode
0	1	1 Time
1	0	16 Times
1	1	64 Times

Synchronous Mode



2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

Single Character Sync (D7)

D7 = 1 denotes single sync character,
D7 = 0 denotes double sync character

Even Parity Generation/Checker (D5)

D5 = 1 denotes Even Parity, D5 = 0 denotes

Odd Parity

PEN (D4) must be set

Parity Enable (D4)

D4 = 1 denotes parity enabled, D4 = 0 denotes parity disabled

Character Length (D3 and D2)

D3	D2	Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

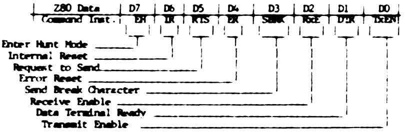
Baud Rate Factor (D1 and D2)

D1	D0	Factor
0	0	Sync Mode

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.3 "In"/"Out" Decoding (Continued)

Synchronous Command



Enter Hunt Mode (D7) when set (applicable to synchronous only)

Internal Reset USART (D6) when set

Request to Send Modem Signal (D5) when set (Note: forces RST pin low)

Error Reset (D4) when set, resets Framing, Overrun, and Parity Error Status

Send Break Character (D3) when set, Break character latched until cleared

Receive Enable (D2) when set, Receive disable' when D2 = 0

Data Terminal Ready (D1) when set (Note DTR pin is forced low)

Transmit Enable (D0) when set, Transmit disabled when D0 = 0

2.4.1 FUNCTIONAL THEORY (Continued)

2.4.1.4 USART Limitations

The USART chip has several limitations which must be observed. These are:

- The status of the USART will not be valid until 28 clock periods from an event affecting the status (11.4 microseconds).
- The TXRDY pin will not be valid for 8 clock cycles after last transmission (3.25 microseconds)
- The RXRDY pin will not be valid for up to 24 clocks after the last received character. (9.77 microseconds).

Note: The main USART clock is independent of the system clock and has a fixed frequency of 2.4576 MHz.

2.4 4230 TELECOMMUNICATIONS (Optional) (Continued)

2.4.2 MODEM INTERFACE

The workstation contains a 25-pin EIA RS-232-C connector located on the rear panel of the 4230 workstation. Pin designations are shown below.

Pin	EIA	Source	Signal Description
1 *	AA	---	Protective Ground
2 *	BA	TC PCA	Transmitted Data
3 *	BB	Modem	Received Data
4 *	CA	TC PCA	Request to Send
5 *	CB	Modem	Clear to Send
6 *	CC	modem	Data Set Ready
7 *	AB	---	Signal Ground
8 *	CF	Modem	Received Line Signal Detector
9	--	---	(Reserved for Data set Testing)
10	--	---	(Reserved for Data Set Testing)
11 *	SCA	TC PCA	Secondary Request to Send
12 *	SCF	Modem	Secondary Received Line Signal Detector
13	SCB	Modem	Secondary Clear to Send
14	SBA	---	Secondary Transmitted Data
15 *	DB	Modem	Transmit Signal Element Timing
16	SBB	Modem	Secondary Received Data
17 *	DD	Modem	Receiver Signal Element Timing
18	--	---	Unassigned
19 *	SCA	TC PCA	Secondary Request to Send
20 *	CD	TC PCA	Data Terminal Ready
21	CG	Modem	Signal Quality Detector
22	CE	Modem	Ring Indicator
23	CHCI	Modem	Data Signal Rate Selector
24	DI	---	Transmit Signal Element Timing
25	--	---	Unassigned

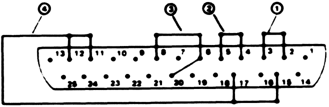
* Denotes signals used by the TC workstation

2.4 4230 TELECOMMUNICATIONS (Optional) (Continued)

2.4.3 RS-232-C LOOPBACK CONNECTOR

An RS-232-C Loopback connector (part number 420-1040) is required for loopback testing of the 4230 TC PCA. This connector should be installed on the RS232 port prior to running the loopback diagnostics.

If the loopback connector is not available, use a RS-232 blank connector (part number 350-1030) and jumper the pins as shown in figure 2-14.



(Note: loopback connector is viewed head on.)

Figure 2-14. Loopback Connector Jumper Diagram

2.5 ARABIC WORKSTATION

The theory of operation for the Arabic (Middle Eastern) Workstations is very similar to that of the 4230/4205 Workstations found in chapter 2 of this 4205/4230 Product Maintenance Manual, however, the Arabic mode will function only if a 210-8287-3 Workstation PCA has been installed in the workstation.

When software issues the proper command, circuitry on the 210-8287-3 PCA presents all characters to be displayed on the CRT in reverse order. The software instructs the workstation to go into an Arabic mode by issuing an OUT '21' command. If the command is issued with a HEX value of '01', the horizontal order of all characters on the CRT to be reversed (right-to-left). If the OUT21 command is issued with a HEX value of '00', the horizontal order of all characters on the CRT is normal (left-to-right).

The start column value functions in exactly the same way as in the non-Arabic mode. If a start column value of 29 is loaded into the start column register, the 108th to the 29th character will be displayed left to right on the CRT.