UNIVAC®

V77-600 SYSTEM
REFERENCE MANUAL

98A 9906 402

NOVEMBER 1977

Sperry Univac is a division of Sperry Rand Corporation

Printed in U.S.A.

CHANGE RECORD

Page Number	Issue Date	Change Description
All	10-76	Original issue.
5-7, 5-9	12-76	Corrected memory bank selection cabling.
8-1 thru 8-24	12-76	Added I/O system section.
v	5-77	Added section 2.7.
viii	5-77	Changed page numbers.
2-1	5-77	Changed name of BOOT switch to LOAD.
2-5	5-77	Added data-save information.
2-10 thru 2-24	5-77	Rearranged text and added section 2.7 and table 2-2.
3-2	5-77	Revised section 3.3.3.
3-3	5-77	Listed four additional options.
7-2	5-77	Changed name of BOOT switch to LOAD.
7-3	5-77	Revised section 7.1.4.
7-10 thru 7-13	5-77	Revised section 7.3.2 and deleted table 7-4.
Various		Deleted all references to Varian.

Change Procedure:

When changes occur to this manual, updated pages are issued to replace the obsolete pages. On each updated page, a vertical line is drawn in the margin to flag each change and a letter is added to the page number. When the manual is revised and completely reprinted, the vertical line and page-number letter are removed.

96A0730-000A

LIST OF EFFECTIVE PAGES

Page Number	Change in Effect
All	Original issue.
5-7	Memory bank selection cabling.
5-9	Memory bank selection cabling.
8-1 thru 8-24	Added I/O system section.
v, vii, 2-1, 2-10 thru 2-24, 3-3, 7-2	Corrected existing errors.
2-5, 7-3, 7-10 thru 7-13	Revisions for the register-selectable program loaders.
All	Complete revision.

9600731-0008

TABLE OF CONTENTS

SECTION 1
INTRODUCTION

SECTION 2
V77-600 SYSTEM COMPUTER

SECTION 3
PROCESSOR

CONTENTS

SECTION 4
MEMORY SYSTEM

SECTION 5
COMPUTER CONFIGURATIONS

SECTION 6
INSTALLATION

SECTION 7
OPERATION

SECTION 7
OPERATION *(continued)*

SECTION 8
INPUT/OUTPUT SYSTEM

CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS *(continued)*

LIST OF TABLES

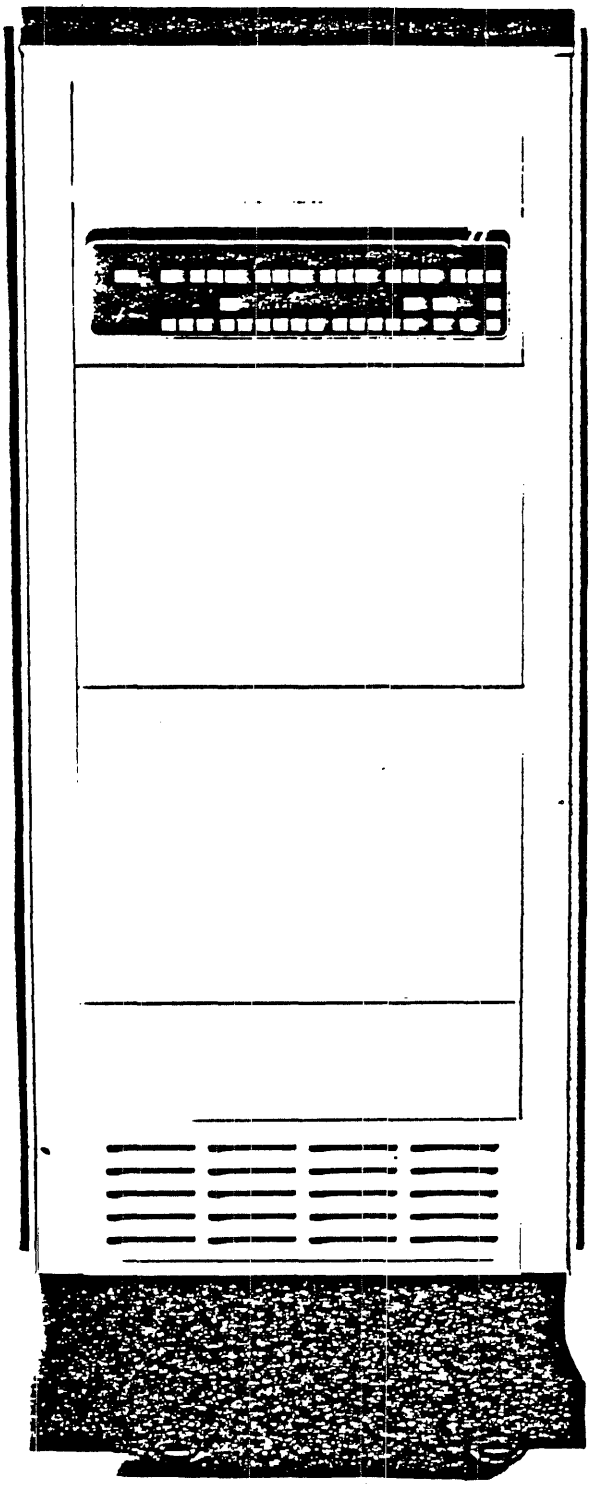


Figure 1-1. The V77-600 Computer System

SECTION 1
INTRODUCTION

This manual describes the V77-600 computer system (figure 1-1) and the operation and integration of product line components which configure this member of the V77 family of computers.

The manual is divided into eight sections:

- Introduction
- V77-600 Computer
- Processor
- Semiconductor Memory
- System Configurations
- Installation
- Operation
- Input/Output System

1.1 SYSTEM FEATURES

The primary features of the V77-600 computer system are listed below:

- Processor -- Operates on 16-bit words with a full-cycle execution time of 660 nanoseconds.
- Modular MOS Memory System -- Can be expanded from 16,384 (16K) words to 256K words within a 7-inch mainframe chassis equipped with the megamap option. Can be expanded to a maximum of 1,048,576 words in 64K increments with memory expansion chassis and a megamap option. This memory system features a low cost dual-port memory module with a full-cycle time of 660 nanoseconds.
- Memory Management System (Megamap Option) -- Permits expansion of MOS memory system to 1-million words in 64K-word increments.
- Cache Memory System (Option) -- Increases system throughput by holding frequently used instructions and data words in special high-speed memory thereby reducing the normal 660 nanosecond memory cycle time.
- Large Instruction Set -- Recognizes 201 arithmetic, decision, and control instructions, many of which can be microcoded to extend the effective instruction repetoire into the hundreds.
- Multiple Addressing Modes -- Including direct, multilevel indirect, immediate, indexed/indirect, relative, and extended with preindexing and postindexing.

- Effective Input/Output -- Includes a full complement of peripheral controllers and devices and three types of I/O operations: program-controlled, direct memory access, and priority memory access.

- Extensive Software — The available program package includes:
  a. VORTEX II (operating system)
  b. Macro Assembler
  c. MAINTAIN III (maintenance)
  d. COBOL
  e. FORTRAN IV
  f. BASIC
  g. RPG II
  h. PRONTO (transaction processing)
  i. TOTAL (data base management)
  j. TSS (time-shared BASIC)
  k. VTAM (data communications)
  l. VIDEO (data entry)
  m. HASP (remote job entry)
  n. UT200 (Control Data 200 emulator)
  o. TEN04 (Univac 1004 emulator)
  p. MIDAS (micro assembler)
  q. MICSIM (micro simulator)
  r. MIUTIL (micro utility)

1.2 SYSTEM APPLICATIONS

The V77-600 system consists of a general-purpose microprogrammable computer, various computer options, and several peripheral options designed for otimum performance and adaptability within a system oriented environment. When integrated with other systems, such as, instrumentation, data acquisition, and communications systems, the V77-600 is an ideal computer system for a variety of scientific, commercial, and industrial applications including business data processing, industrial control, data communications, scientific research, and education.

The most basic system contains the V77-600 computer, with 660 nanosecond semiconductor memory and option board, and a keyboard-printer (Teletype) for data entry and retrieval (input/output). This basis system is suitable as a research laboratory tool for simple scientific computations or as an educational tool for storing field study information and research data. By adding high-speed paper tape equipment (punch and reader) for increased input/output efficiency and digital plotters and oscilloscope display systems for graphic presentation of computed results and stored data, the basic system can be enhanced to perform high-speed calculations or data retrieval in a form suitable for later analysis or review.

Business and accounting applications require a large data base management system that can efficiently store, easily access, and promptly display or print out data. For a small business or simple accounting operation, an adequate large data base management system might contain the basic computer system with an expanded 660 nanosecond semiconductor memory of up to 1,048,576 words for main storage and an additional high-speed line printer for output. By adding disc memory and/or magnetic tape units for additional

bulk storage and punched-card and/or paper-tape equipment for increased input/output efficiency, this smaller data base system can be expanded to meet the requirements of almost any size business or accounting department.

Industrial process control applications require frequent sampling and interpretation of data as materials are being processed and as goods are being manufactured. Here again the basic computer system Teletype system comprises the heart of the system. Analog, digital, and relay I/O devices can be connected on the I/O bus for the input of signals from the processing/manufacturing area and for the output of signals to control devices or displays. Secondary data storage devices make it possible to record data for allied operations, i.e., accounting, production control, etc. If additional operator input is required, several Teletypes can be used at the same time.

The basic computer system and Teletype can also be used to integrate and unify a communications network by adding a Sperry Univac data communications multiplexor. Used as a data concentrator, this expanded system links and switches variable-speed modems and communications lines, thus, adapting them to a variety of communications devices and transfer rates. With a second addition of disc or magnetic tape units, the expanded system can be used as preprocessor that can organize data for efficient, time-shared processing in larger computer systems.

1.3 SUPPORT DOCUMENTATION

The basic architecture of the V77-600 computer system, as well as other V70 series computer systems, is described in the V70 series Architecture Manual. This manual contains data and instruction formats, addressing modes, and instruction set descriptions.

The architecture manual, along with other hardware manuals pertinent to the V77-600 computer system are listed according to document number as follows:

V70 Series Architecture	98A 9906 00x
V70 Series Processor	98A 9906 02x
V70 Series Option Board	98A 9906 05x
660 Nanosecond Semiconductor Memory	98A 9906 26x
V70 Series Megamap	98A 9906 27x
V70 Series Cache	98A 9906 28x
V70 Series Writable Control Store II	98A 9906 29x
V70 Series System Power Supply	98A 9906 46x

Note that the x that appears at the end of each document number is the revision number and can be any digit 0 through 9.

Software manuals are also available for the V77-600 computer system and are also listed according to document number as follows:

Microprogramming Guide	98A 9906 07x
MAINTAIN III	98A 9952 07x
VORTEX Reference	98A 9952 10x
VORTEX II Reference	98A 9952 24x

VORTEX/VORTEX II Installation	98A 9952 25x
TOTAL	98A 9952 41x
RPG II	98A 9952 42x
COBOL	98A 9952 43x
TSS (Time Sharing Subsystem)	98A 9952 44x
V70 Assembly Language	98A 9952 45x
VIDEO	98A 9952 46x
Utility Programs	98A 9952 47x

1.4 SYSTEM DOCUMENTATION

System documentation is assembled for each system prior to its shipment. The contents include:

System memoranda
System arrangement drawing
Hardware performance standards
Test Data
Logic diagrams and schematics
Option and controller documentation
All engineering notices affecting any supplied documentation

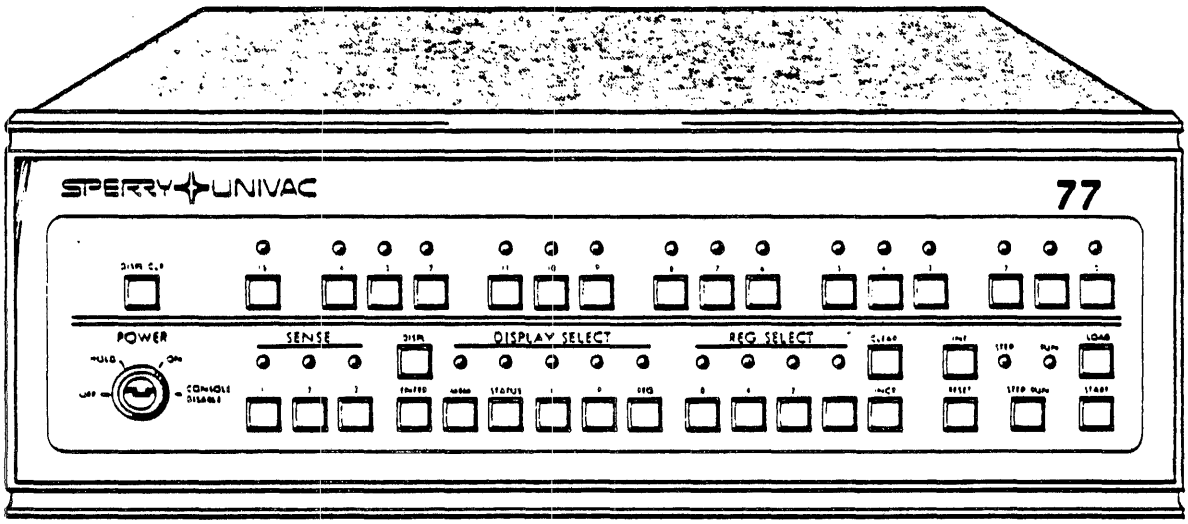
SECTION 2
V77-600 SYSTEM COMPUTER

2.1 GENERAL DESCRIPTION

The V77-600 computer, a general-purpose microprogrammed minicomputer (figure 2-1), is the key element of all V77-600 computer systems. Designed for maximum system flexibility, the V77-600 can be used to configure systems having a wide range of application requirements. To meet these requirements, the computer provides modular expansion for open-ended system growth, microprogramming for expanded system control, and reliability and easy maintenance for minimum system down time. Also designed to be compatible with existing V70 series software and peripheral hardware and with other V77 family components, the V77-600 is easily adapted to changing system technology.

2.2 STANDARD FEATURES

A mainframe chassis, control panel, instruction set, and V77-600 processor with hardware multiply/divide, memory parity logic, dual memory buses for dual port memory, I/O bus with direct memory access, and automatic bootstrap loader comprise the standard features of the computer.



VTII-3654

Figure 2-1. The V77-600 Mainframe (7-inch Chassis)

The standard 7-inch mainframe chassis (figure 2-2) or optional 14-inch mainframe chassis (not shown) accommodates the control panel, processor, semiconductor memory, option board, expansion hardware for I/O and memory expansion, and other hardware options, as required.

All of the controls and indicators necessary to operate the computer are located on the control panel which is used with both standard and optional mainframes (second 7).

The instruction set contains 201 single and multiple-register instructions. Many instructions can be microcoded to extend the effective repertoire to several hundred microinstructions. Refer to the V70 Series Architecture Manual for additional information on the instruction set and to the V70 Microprogramming Guide for microinstruction and microprogram information.

The high-performance processor has a microinstruction execution time of 165 nanoseconds and can operate independently from both memory and I/O devices. This processor features eight general-purpose programming registers, eight general-purpose microprogramming registers, 16-bit wide data paths, arithmetic and logical function generators, and data path selection logic which is controlled by microprogramming firmware stored in a programmable read only memory or a writable control store (WCS) option (section 2).

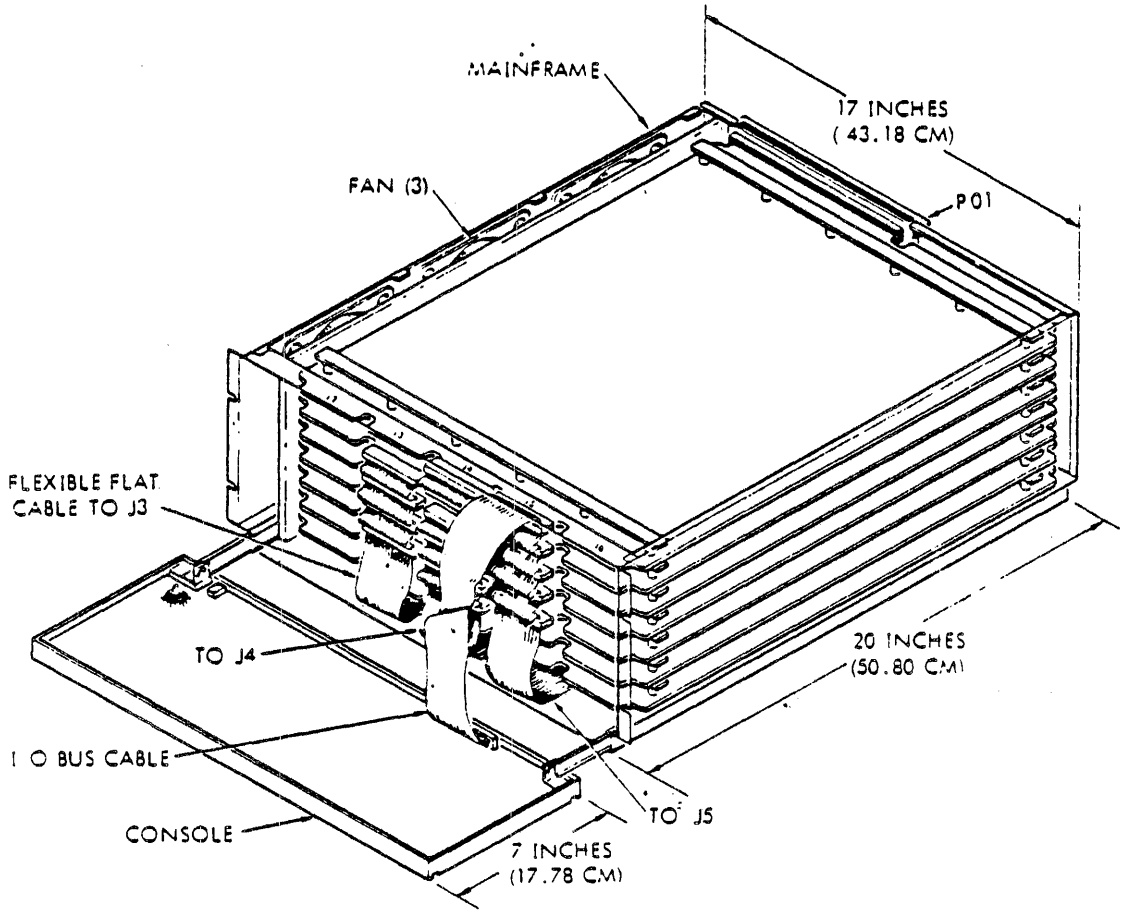
2.3 OPTIONAL FEATURES

A wide range of optional features are available to permit maximum system flexibility. These features are available for basic computer operation as well as for increased computer efficiency and throughput.

Options that are required for basic operation are the 660 nanosecond semiconductor memory, the V77-600 option board, and the V77 system power supply.

The 660 nanosecond semiconductor memory (section 4) is a dual-port, expandable, random-access, metal-oxide-semiconductor (MOS) memory available in 16,384 (16K), 32,768 (32K), or 65,536 (64K) by 16-bit word modules. An 18-bit version of each of these three modules is also available as an option and includes additional storage for two parity bits per word (one parity bit per 8-bit byte). When addressed with the megamap option (section 2.3.2), a V77-600 semiconductor memory system using 64K modules is expandable to 262,144 (256K) words of storage within a single 7-inch mainframe chassis or to 1,048,576 (1024K) words of storage within three additional memory expansion chassis. Full cycle time for this memory without megamap is 660 nanoseconds; access time is 560 nanoseconds.

The common configuration of the V77-600 option board includes I/O bus control logic (with DMA), Teletype (TTY) or CRT controller, power failure/restart (PF/R), and a standard real-time clock (RTC). Alternate configurations of the option board may include memory protection (MP) and/or priority memory access (PMA) and/or one of several special (nonstandard) RTC configurations. The option board is also contained in the mainframe chassis which provides connection to I/O expansion and memory expansion chassis.



VTI1-3547

Figure 2-2. 7-Inch Mainframe Chassis (Typical Layout)

The V77 system power supply delivers dc power to components located in the mainframe chassis of the computer and peripheral controller boards located in the optional I/O cardframe expansion chassis. Although housed in a separate chassis, the V77 system power supply is turned on or off by the power switch located on the control panel. When the system power supply is turned on, it provides all dc power required by the mainframe processor, option board, megamap option, writable control store option, cache memory option, floating-point processor option, and up to 256K words of 660 nanosecond semiconductor memory. It will also provide sufficient dc power for several peripheral controller boards at the same time. With ac line voltage applied to the input, the V77 system power supply delivers each of the following dc output voltages under the maximum load current specified:

+5V at 100 amperes (logic power)

+5.2V at 6.0 amperes (memory power)

+12V at 4.0 amperes (memory power)

+12V at 1.2 amperes (data communications)

-12V at 1.4 amperes (data communications)

In addition to the remote on/off control, the V77 system power supply provides overcurrent protection, overvoltage protection, and low noise operation.

Several important options that contribute to the efficiency and throughput of the V77-600 computer but are not required for basic computer operations are described in subsequent paragraphs of this section.

The V77-600 megamap mainframe option contained on a single board allows the main memory to be expanded to over a million words (two million bytes). In combination with VORTEX II software, the megamap option divides the memory into 512-word pages and assigns these to individual application programs on either a contiguous or non-contiguous basis — depending on the most efficient use of the memory available. Memory protection is also provided on a page-by-page basis.

The floating-point processor (FPP) option, another high-performance mainframe option, performs high-speed floating point arithmetic on single and double precision numbers associated with FORTRAN programs.

The cache memory mainframe option increases throughput by separately storing the most frequently used instructions and data processed by an application program. The cache is a high-speed memory with a capacity for storing 1,024 of the most recently used words that have been transferred to or from memory. The cycle time for a word stored in cache is only 371 nanoseconds, compared to the 660 nanoseconds cycle time for main memory. In the execution of a typical application program, over 90 percent of the transfers will be with cache rather than main storage.

Throughput efficiency can be enhanced by writable control store (WCS) options which add 512, 1,024, or 2,048 additional storage locations for 64-bit microinstructions (up to 4,096 WCS locations can be included with each computer system). Users can write their own microinstructions to perform frequently used subroutines or special functions unique to their application. As an alternative, Sperry Univac also provides standard firmware packages which increase the speed of scientific programs written in FORTRAN or commercial programs written in COBOL or RPG II. Further efficiencies, in the case of FORTRAN programs, can be achieved by the addition of an optional floating point processor.

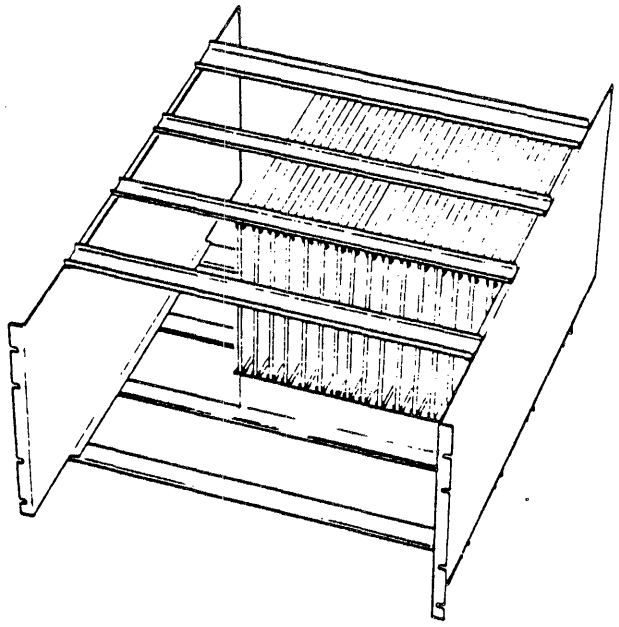
Other computer mainframe options include: priority interrupt module (PIM), buffer interface controller (BIC), and block transfer controller (BTC). The PIM establishes eight levels of interrupt request on the I/O bus in order of priority. The BIC implements the direct memory access (DMA) capabilities of the basic computer, permitting cycle-stealing I/O data transfers between memory and peripheral controllers at rates of up to 361,800 words per second. The BTC implements automatic data transfers between peripheral controllers and memory via the priority memory access (PMA).

The data-save option is a power-supply option that provides battery power to maintain data in the semiconductor memory during a loss of ac line voltage. A memory of 64K by 16-bit words can be sustained for up to four hours; a larger memory of 256K words for up to two hours. The data-save battery box requires no vertical rack space in the equipment cabinet since it mounts on the rear panel of the power supply. To ensure reliable performance, the three 6-volt series-connected batteries located in the battery box are kept fully charged by circuits in the power supply.

For systems requiring further data-save protection, additional data-save battery packs are available. These battery packs can be used to protect memory above 256K words or can be used in parallel with existing data-save batteries to extend memory protection. Each additional battery pack sustains 256K words of memory for up to 1.5 hours or 64K words for up to 8 hours.

To permit the user to install his own battery pack, a connector at the rear of the system power supply is provided.

The I/O expansion cardframe chassis (figure 2-3) accomodates connector-planes with a total combined capacity of 24 card slots, cardguide adaptor brackets, and cardguides for up to 23 peripheral controller boards and one I/O connector paddelboard. Connector-planes (figure 2-4) which are mounted on the rear of a cardframe chassis provide power and I/O bus connections to associated controller boards. Power connections are made directly from the system power supply (section 2.3.1) to one connector-plane via associated power cables. Power to the other connector-planes are provided through jumper power cables.



VTII-3623

Figure 2-3. I/O Chassis Cardframe

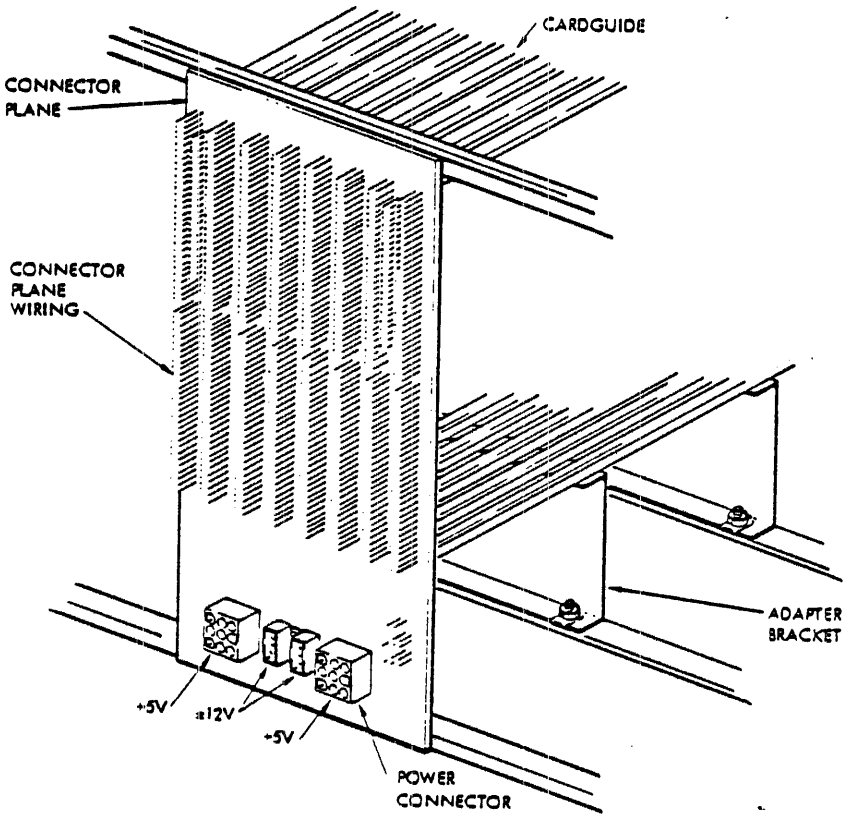


Figure 2-4. Typical Connector-Plane

Two electrical equipment cabinets are available which provide useable rack space of 45.5 to 56.0 inches, respectively, for housing system components. Each has an internal blower on the bottom and an exhaust fan at the top to provide cooling for chassis mounted inside. The tan tray option provides vertical air flow cooling for three cardframe chassis units. It is mounted in an electrical equipment cabinet so that it can pull cooling air up through two chassis and blow cooling air up through the bottom of the other two chassis.

Throughput efficiency is increased through the use of a wide range of optional software developed by Sperry Univac. For example, VORTEX II is Sperry Univac's multi-programming operating system that permits concurrent execution of a variety of real-time and background tasks. VORTEX II can be used with a variety of subsystems such as TOTAL for data base management, VTAM for data communications, PRONTO for transaction processing and network control, TSS for multi-user editing and time-shared BASIC, and HASP for remote job entry of IBM 360/370 workstation tasks. HASP functionally emulates an IBM 360/25 HASP workstation. In addition to HASP, Sperry Univac has developed two other programs for remote job entry. The UT200 emulates functions of a Control Data 200 User Terminal and the TEN04 functionally emulates a Univac 1004 performing remote job entry to a Univac 1100 series CPU operating under an EXEC 8 program. Sperry Univac has also developed test programs for testing the computer hardware and utility programs for program editing and debugging, as well as many programming languages for added efficiency such as, a macro assembler, FORTRAN, COBOL, RPG II, and BASIC. With a writable control store option, three micro program languages are available. The MIDAS is a micro assembler; the MICSIM is a micro simulator; and the MIUTIL is a micro utility language.

2.4 PHYSICAL CHARACTERISTICS

This secion explains and illustrates the optional 7-inch (17.78 cm) or 14-inch (35.56 cm) mainframe chassis, I/O expansion cardframe chassis and memory expansion chassis, along with power distribution and control. All chassis fit into a RETMA standard 19-inch (48.26 cm) wide by 24-inch (60.96 cm) deep cabinet. Detailed explanations of physical dimensions, circuit locations, bus structures, connections, and general assembly information is covered in the following subsections.

2.4.1 Control Panels

The 7- by 19-inch (17.78 by 48.26 cm) molded-plastic control panel contains all of the controls and indicators necessary to operate the computer (section 7) and has a printed circuit (PC) card mounted to the back side which holds light emitting diodes and switches. The control panel, hinged at the bottom to the 7-inch mainframe chassis, folds down for easy access to the circuit boards.

The 14- by 19-inch (35.56 by 48.26 cm) front panel contains a control panel in the bottom half and a blank panel in the top half. The front panel is molded plastic which is hinged at the bottom of the control panel to the 14-inch mainframe chassis, and folds down, parallel to the floor, for easy access to the circuit boards.

The control panel makes connection to the various circuit boards in the mainframe via a 50-wire flat I/O cable, from a 50-pin connector on the rear of the control panel. A power cable also connects to the rear of the control panel to activate indicators and switches.

2.4.2 Mainframe Chassis

The 7-inch mainframe chassis (figure 2-2) with 7 slots accommodates the control panel, processor, semiconductor memory, option board, fans, and the capability for I/O and memory expansion.

The 14-inch chassis has the same physical configuration as the 7-inch chassis except that it is designed to contain 16 universal slots. The control panel mounts on the bottom front half with a blank panel covering the top half.

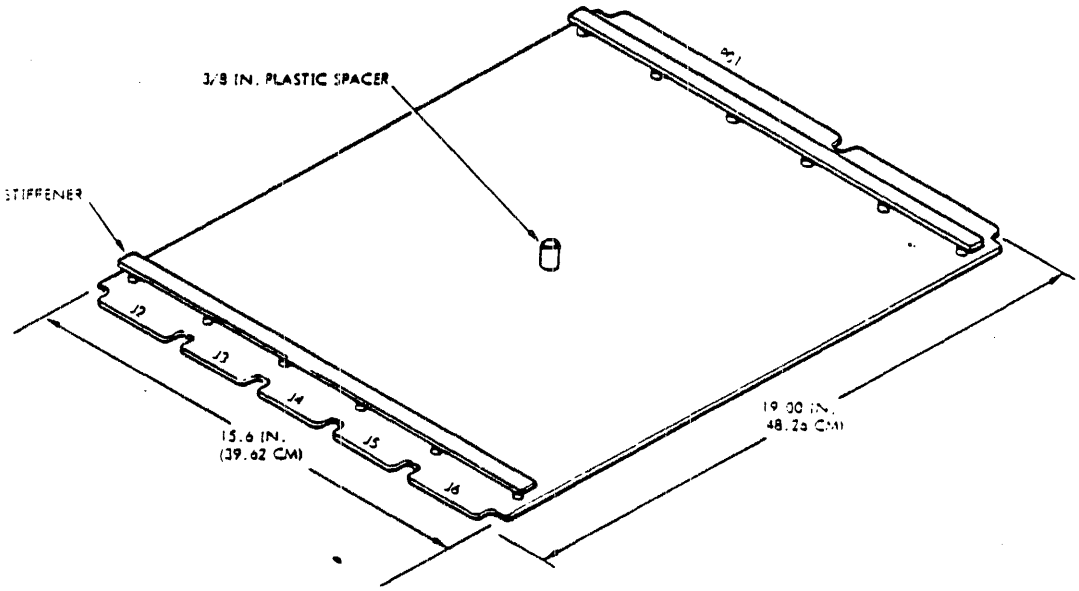
The 14-inch mainframe chassis with a processor and option board can contain any size semiconductor memory (in 16K, 32K or 64K increments) up to 256K. Fourteen remaining slots may be used for memory, writable control store, megamap, etc.

Because of the flexible design of the mainframe, any multilayer circuit board (processor/option are four layers; semiconductor memories are two layers) can be mounted in any of the seven universal slots (16 slots in the 14-inch mainframe) numbered from bottom to top. Any combination of circuit boards are tied together via a 50-wire flat cable at the front. The front of each circuit board has up to five 50-pin board edge connectors and are numbered from left to right (facing front) from J2 through J6 in vertical rows. The I/O flat cable buses connect the appropriate circuit boards and can then loop in along the bottom several inches

to connect with the I/O port. Dimensions of width and depth for the mainframe chassis are also shown in figure 2-2.

The I/O port consists of a subassembly of card guides, connectors, and PC board interconnections. If an I/O expansion cardframe chassis is used, an I/O extender board plugs into the I/O port. Otherwise an I/O bus termination shoe is plugged into the I/O port.

The 15.6- by 19-inch (39.62 by 48.26 cm) circuit boards (figure 2-5) slide into the mainframe from the front and plug into the power and memory buses in the rear. The PC boards are spaced on 0.6-inch (1.524 cm) centers. Also, there are device connectors for the I/O controllers, PMA (J7A, J7B), TTY (J8), and RTC (J9) mounted at the rear of the option board.



VTI1-3548

Figure 2-5. Typical Mainframe Circuit Board

The power supply control and dc power signals connect to the rear, right side of either the 7-inch or 14-inch chassis (facing from the rear). The ac power for the fans enters at the lower right rear with the three, 4.5-inch square, muffin fans (six in the 14-inch chassis) mounted vertically on the right side of the mainframe (facing rear). Memory and dc voltage distribution is via a three-layer PC bus connector board that provides access to all boards in either the 7- or 14-inch mainframes.

2.4.3 I/O Expansion Cardframe

The I/O expansion cardframe is 12.25-inches high by 19-inches wide by 24-inches deep (31.12 cm by 48.3 cm by 60.96 cm). The cardframe can accommodate connector-planes which provide up to 24 connector slots for printed circuit boards. The first slot contains an I/O cable connector PC board and the remaining slots (up to 23) contain the controller boards as required. A termination shoe (board) is plugged into the last slot position of the I/O bus and provides a load to I/O signals (figure 2-6).

The connector-plane, located at the rear of the cardframe, contains power connectors for *+5V and* +12V dc. Connector-planes are available in 4, 8, 12, or 16 slot capacities for connection to peripheral controller boards.

Each peripheral controller board is 7.75-by-12-inches (19.7 by 30.3 cm) and contains a 122-pin connector for mating with an s-slot or sw-slot connector-plane in the I/O cardframe. The other end of controller board has two 44-pin connectors that mate with peripheral device cables.

The mainframe connects to the I/O expansion cardframe with a flat cable from a paddleboard connection at the I/O port. The flat I/O cable extends between the I/O port at the rear of the mainframe chassis and the I/O paddleboard located in the righthand slot at the font of the I/O cardframe.

2.4.4 Memory Expansion Chassis

The memory expansion chassis is a 7-inch (17.78 cm) high chassis that can hold four PC boards and is designed similar to the mainframe chassis.

The rear of the memory expansion chassis connects with the rear of the mainframe chassis via the flat cable from the bottom of the memory bus in the memory chassis to the top of the memory bus in the mainframe (figure 2-7). When memory expansion chassis are used in a shared memory system, connections are made as shown in figure 2-8.

Power enters at a 16-pin connector on the right rear (facing rear) with power control beneath it on an 8-pin connector. Ac fan power is brought in on a small connector at the bottom rear corner.

2.4.5 System Power Supply

The system power supply is a modular supply that is self-contained in a 5.25- by 19- by 19.5-inch chassis that is mounted in the top of a standard-size electrical equipment cabinet (figure 2-9). It mounts in a vertical rack space 5.25-inches high and a horizontal rack space 19-inches wide. The system power supply contains either full-size or half-size dc output power modules or a combination of both. Full size modules are 5- by 8- by 12-inches in outside maximum demensions; half-size modules are 5- by 8- by 5.25-inches. Full size modules have self-contained forced-air cooling. Half-size modules are cooled by chassis mounted fans (one fan per two half-size modules). AC input power distribution is provided by seven connectors mounted to a power supply board located inside the front

panel of the chassis. DC output power distribution is provided by output connectors mounted to the rear side of the power supply chassis. The AC input power cable, all DC voltage adjustment controls and AC fan power connectors are also mounted to the rear panel. A single power switch is mounted to the front panel.

When a data-save option is installed on the rear panel of the system power supply the overall depth dimension of the power supply chassis is increased by 6.62-inches (figure 2-9).

2.4.6 Equipment Cabinets

One of two electrical equipment cabinets with an installed equipment rack is 77-inches high by 24-inches wide by 30-inches deep and provides 56-inches of vertical rack space for mounting components of the Varian 77-600 computer system. The other cabinet is 64.1-inches high by 25.4-inches wide, by 36-inches deep and provides 45.5-inches of vertical rack space. Excluding peripherals, each equipment cabinet can house all of the computer equipment required for an expanded system with a 1024K memory system and a full compliment of high-performance options. Each cabinet has a rear panel mounted at the bottom of the rack that mounts an AC input power connector. Normal AC input power to the connector is 115V AC at 30 amperes maximum current. However, for input power voltages other than 115V AC an optional step-down transformer which mounts to the floor of a cabinet is available for converting to 115V AC. An AC outlet strip mounted on the inside of each cabinet at the rear provides 115V AC power for connection to V77-600 system components. If more than one cardframe chassis is used to house PC boards of an expanded system, an optional fan tray (figure 2-10) must be used. This fan tray measures 1.69-inches high, 17.50-inches wide, 24-inches deep and installed between cardframe chassis. It contains six fans.

2.5 POWER DISTRIBUTION AND CONTROL

Figure 2-11 shows power distribution for a system with an installed system power supply.

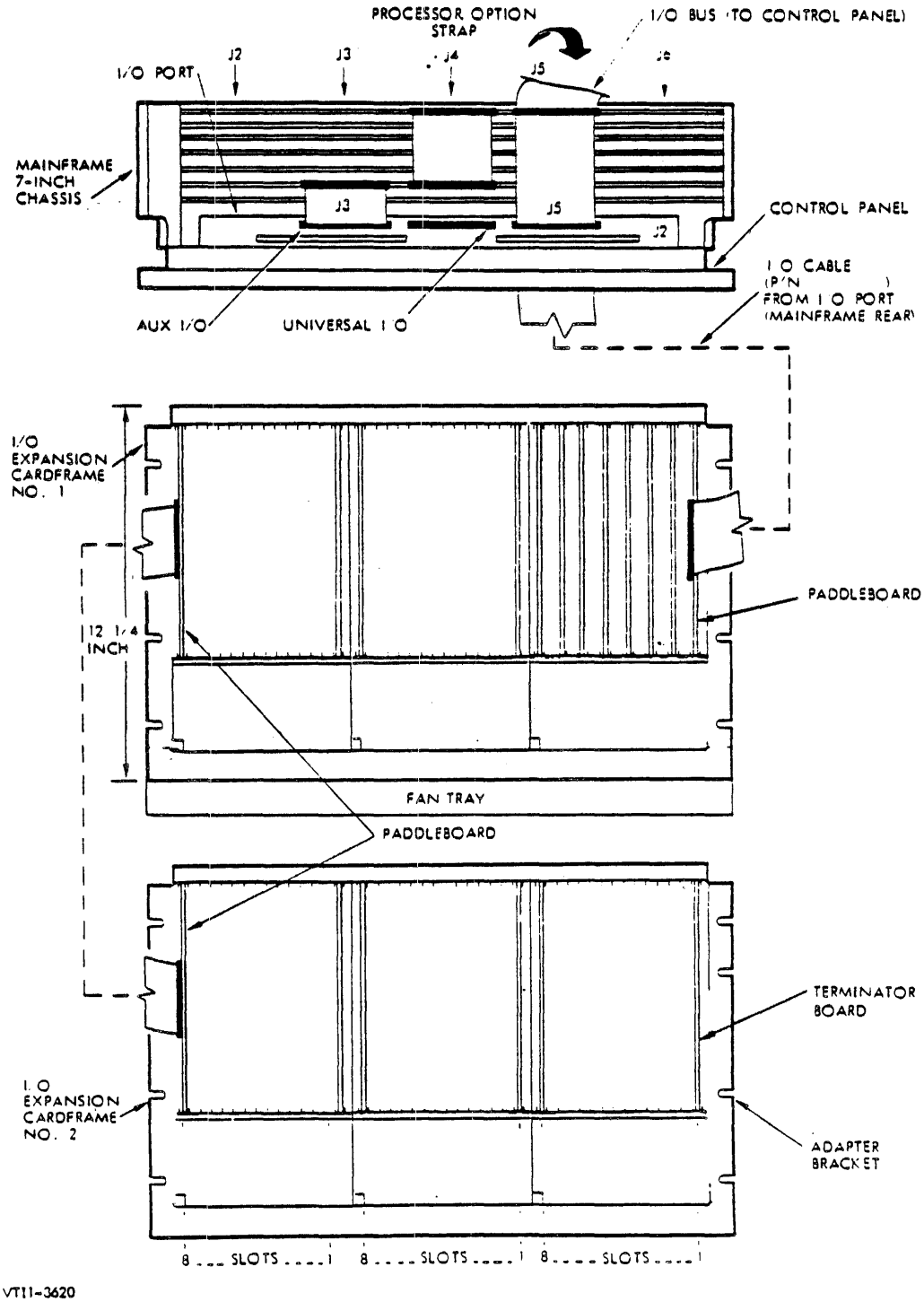
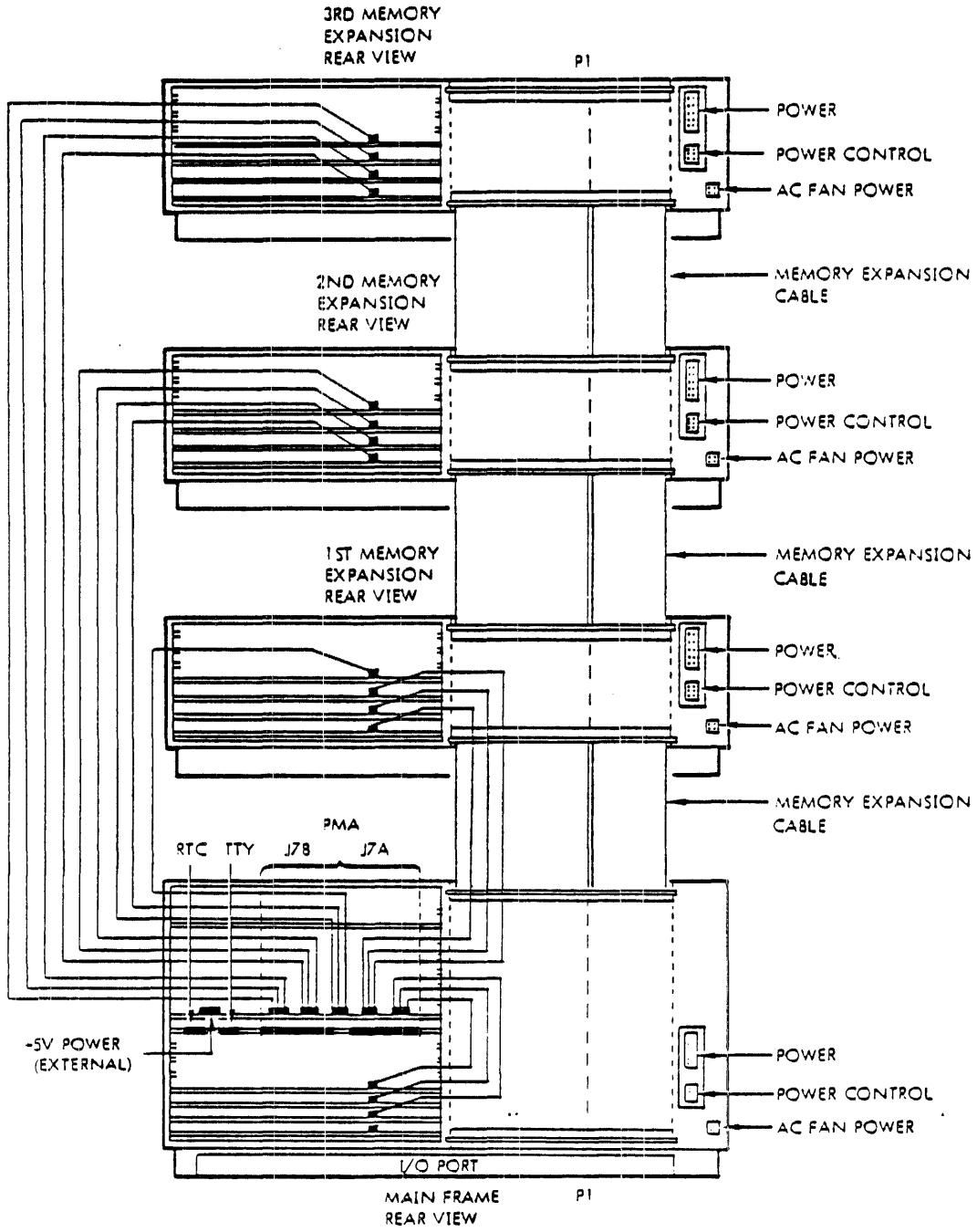
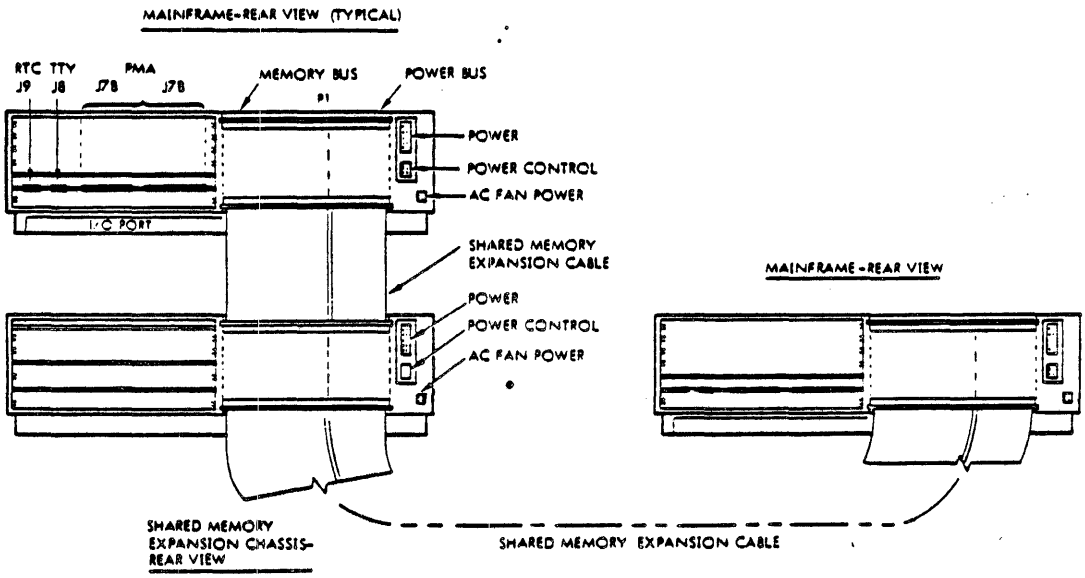


Figure 2-6. I/O Expansion—Front View



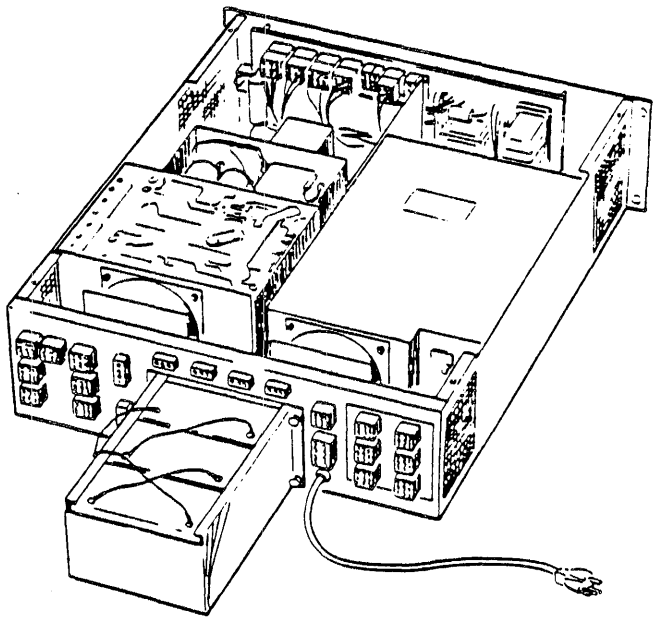
VTII-3550 A

Figure 2-7. Typical Expanded Memory System Configuration



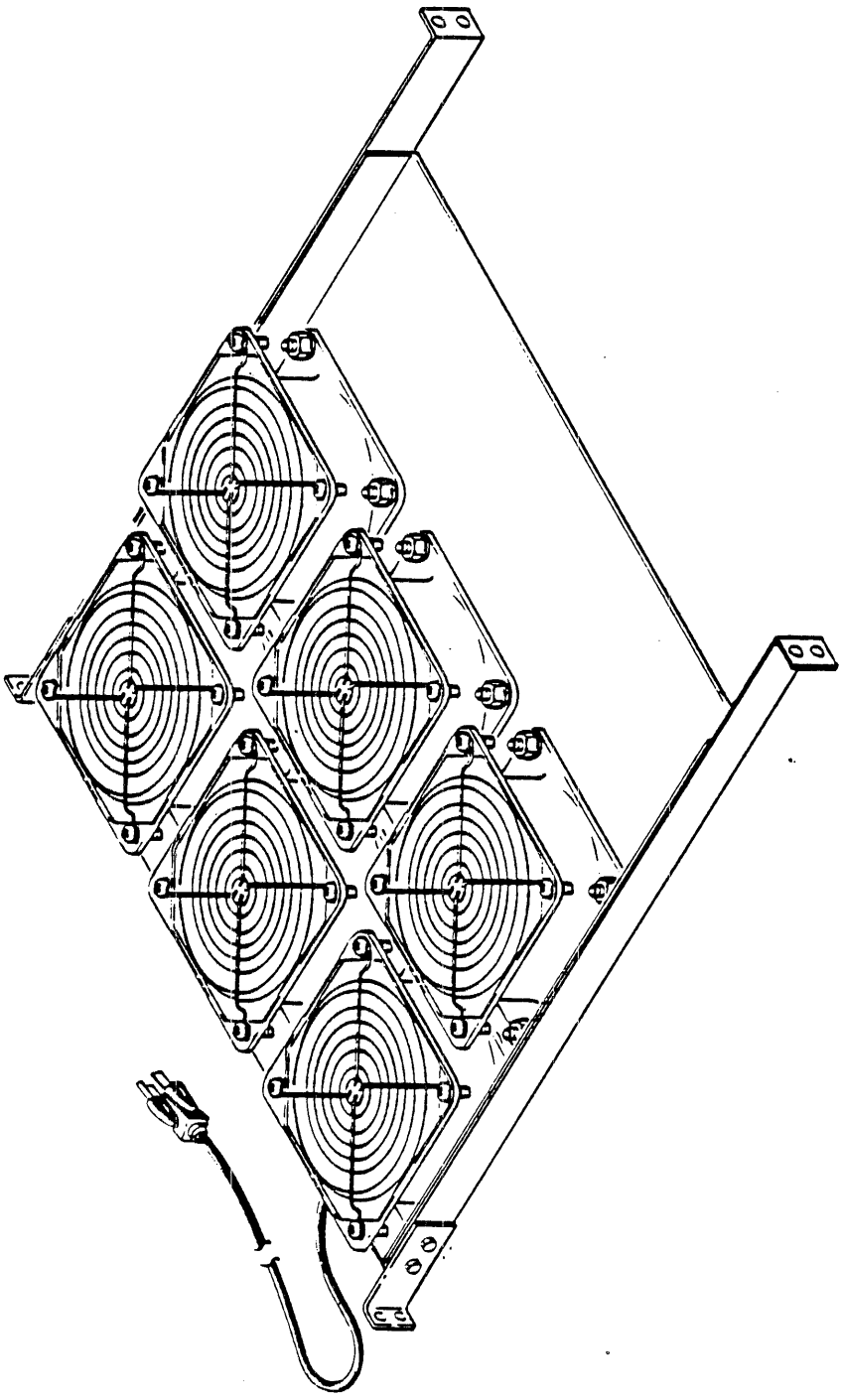
VTI1-3551

Figure 2-8. Shared Memory System Configuration (No Mainframe Options Shown)



VTI1-3618

Figure 2-9. System Power Supply



VTII-3630

Figure 2-10. Fan Tray

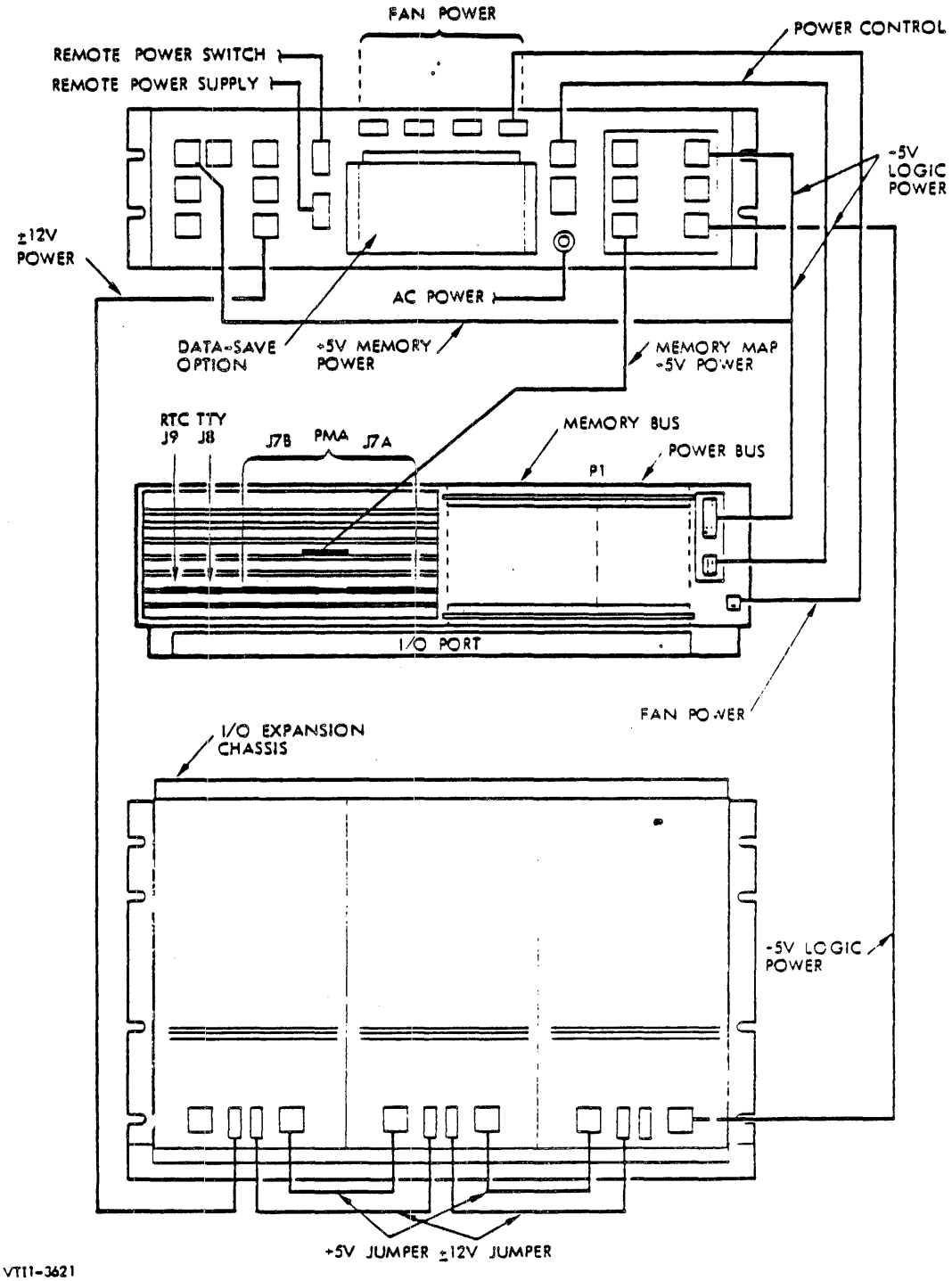


Figure 2-11. Typical Power Distribution Control (Rear View)

2.6 V77-600 SPECIFICATIONS

Specifications for the V77-600 computer are listed in table 2-1.

Table 2-1. V77-600 Specifications

Type	General-purpose microprogrammed digital computer.
Memory	Dual-port 660 nanosecond semiconductor memory with 16-bit word length. Available in 16K, 32K, or 64K modules, with optional byte parity.
Word length	8, 16, or 32 bits.
Register	24 registers: 8 16-bit registers for assembly programming, 8 16-bit general-purpose registers for microprogramming, and 8 special-purpose registers for microprogramming. Seven of the assembly programming registers can be used as index registers (byte, word, or double-word addressing). Four of these same registers can be used as two double-word registers.
Arithmetic	Binary twos complement.
I/O Transfer Rates	DMA (620 compatible): 250,000 words per second. PMA: 1,010,000 words per second (writing). 932,000 words per second (reading).
Instructions	187 standard, can be extended with writable control store. Floating point processor option provides an additional 14 instructions.
Addressing Modes	Byte addressing, word addressing, and double-word addressing, preindexed direct or indirect the 32,768 words using any of the 7 index registers.

(continued)

Table 2-1. V77-600 Specifications (continued)

	Direct to 2,048 words. Relative to P, X or B register to 512 words. Preindexing with X or B register. Multilevel indirect to 32,768 words. Indirect indexed. Immediate. Post indexing with X or B register. Extended mode to 32,768 words. Megamap addressing to 1,048,576 words.
Standard features	Multiply/Divide. Automatic program loader. Memory parity logic. Memory parity logic. I/O bus with direct memory access. Programmer control panel.
Options	Power failure/restart. Real time clock. Memory protection. Priority memory access. Block transfer controller. Priority interrupt module. Megamap. Cache. Floating point processor. Writable control store. Data-save power supply.
Software	Language processors Macro assembler (DAS) FORTRAN IV RPG II BASIC COBOL Operating systems VORTEX and VORTEX II multitasking systems Data base management TOTAL Interactive time-sharing subsystem (TSS) Transaction Processing PRONTO

(continued)

Table 2-1. V77-600 Specifications (continued)

	File Access Methods Indexed sequential Sequential Direct Microprogramming support Assembler Simulator Utility for loading and debugging Data communications VTAM Application software HASP/RJE UT200 TEN04 VIDEO data-entry system All of the above software operate with VORTEX II (except MOS).
Logic levels	Internal (positive logic): High = +2.4 to 5.0V dc Low = 0 to +0.5V dc I/O bus (negative logic): High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Dimensions	Mainframe chassis is either 14 or 7 inches high, 19 inches wide, and 20.5 inches deep (35.6 and 17.8 by 48.3 by 52.1 cm). I/O expansion chassis is 12.25 inches high, 19 inches wide, and 19 inches deep (31.1 by 48.3 by 48.3 cm). System power supply is 5.25 inches high, 19 inches wide and 19.5 inches deep (13.3 by 48.3 by 49.5 cm).
Input voltage	105 to 125V ac or 210 to 250V ac, at 50 or 60 Hz.
Input current	With 115V ac, the maximum ac current requirements for the system power supply is 15 amperes.
Operational environment	0 to 50 degrees C (32 to 122 degrees F), 0 to 90 percent relative humidity without condensation.

2.7 V77-600 INSTRUCTIONS

Instructions available with the V77-600 computer are listed in table 2-2.

Table 2-2. V77-600 Instructions

Register-to-Memory Instructions	
LD	Load
ST	Store
AD	Add
SB	Subtract
Byte Instructions	
LBT	Load Byte
SBT	Store Byte
Jump-If Instructions	
JZ	Jump if Register Zero
JNZ	Jump if Register Not Zero
JN	Jump if Register Negative
JP	Jump if Register Positive
JDZ	Jump if Double-Precision Register Zero
JDNZ	Jump if Double-Precision Register Not Zero
Double-Precision Instructions	
DLD	Double Load
DST	Double Store
DADD	Double Add
DSUB	Double Subtract
DAN	Double AND
DOR	Double OR
DER	Double Exclusive OR
Register-to-Register Instructions	
T	Transfer
ADR	Add Register
SBR	Subtract Register

(continued)

Table 2-2. V77-600 Instructions *(continued)*

Single Register Instructions	
INC	Increment Register
DEC	Decrement Register
COM	Complement Register
Immediate Instructions	
LDI	Load Immediate
ADI	Add Immediate
Load and Store Instructions	
LDA	Load A Register
LDAI	Load A Register Immediate
LDAE	Load A Register Extended
LDB	Load B Register
LDBI	Load B Register Immediate
LDBE	Load B Register Extended
LDX	Load X Register
LDXI	Load X Register Immediate
LDXE	Load X Register Extended
STA	Store A Register
STAI	Store A Register Immediate
STAE	Store A Register Extended
STB	Store B Register
STBI	Store B Register Immediate
STBE	Store B Register Extended
STX	Store X Register
STXI	Store X Register Immediate
STXE	Store X Register Extended
TSA	Transfer Switches to A Register
Arithmetic Instructions	
INR	Increment Memory and Replace
INRI	Increment and Replace Immediate
INRE	Increment Memory and Replace Extended
ADD	Add Memory to A Register
ADDI	Add Memory to A Register Immediate
ADDE	Add Memory to A Register Extended
SUB	Subtract Memory from A Register
SUBI	Subtract Memory from A Register Immediate
SUBE	Subtract Memory from A Register Extended
MUL	Multiply
MULE	Multiply Extended
MULI	Multiply Immediate
DIV	Divide
DIVI	Divide Immediate
DIVE	Divide Extended

(continued)

Table 2-2. V77-600 Instructions *(continued)*

Logic Instructions	
ORA	Inclusive-OR Memory and A Register
ORAI	Inclusive-OR to A Register Immediate
ORAE	Inclusive-OR Memory and A Register Extended
ERA	Exclusive-OR Memory and A Register
ERAI	Exclusive-OR to A Register Immediate
ERAE	Exclusive-OR Memory and A Register Extended
ANA	AND Memory and A Register
ANAI	AND to Register Immediate
ANAE	AND Memory and A Register Extended
Jump Instructions	
JMP	Jump Unconditionally
JOF	Jump if Overflow Indicator Set
JAP	Jump if A Register Positive
JAN	Jump if A Register Negative
JAZ	Jump if A Register Zero
JBZ	Jump if B Register Zero
JXZ	Jump if X Register Zero
JSS1	Jump if Sense Switch 1 Set
JSS2	Jump if Sense Switch 2 Set
JSS3	Jump if Sense Switch 3 Set
JIF	Jump if Combined Conditions Are Met
JANZ	Jump if A Register Not Zero
JBNZ	Jump if B Register Not Zero
JXNZ	Jump if X Register Not Zero
JS1N	Jump if Sense Switch 1 Not Set
JS2N	Jump if Sense Switch 2 Not Set
JS3N	Jump if Sense Switch 3 Not Set
JOFN	Jump if Overflow Indicator Not Set
IJMP	Indexed Jump
JSR	Jump Unconditionally and Set Return in Index Register
BT	Bit Test
SRE	Skip if Register Equal to Memory
Jump-And-Mark Instructions	
JMPM	Jump and Mark Unconditionally
JOFM	Jump and Mark if Overflow Set
JANM	Jump and Mark if A Register Negative
JAPM	Jump and Mark if A Register Positive
JAZM	Jump and Mark if A Register Zero
JBZM	Jump and Mark if B Register Zero
JXZM	Jump and Mark if X Register Zero
JS1M	Jump and Mark if Sense Switch 1 Set

(continued)

Table 2-2. V77-600 Instructions *(continued)*

JS2M	Jump and Mark if Sense Switch 2 Set
JS3M	Jump and Mark if Sense Switch 3 Set
JIFM	Jump and Mark if Combined Conditions Are Met
JOFNM	Jump and Mark if Overflow Not Set
JANZM	Jump and Mark if A Register Not Zero
JBNZM	Jump and Mark if B Register Not Zero
JXNZM	Jump and Mark if X Register Not Zero
JS1NM	Jump and Mark if Sense Switch 1 Not Set
JS2NM	Jump and Mark if Sense Switch 2 Not Set
JS3NM	Jump and Mark if Sense Switch 3 Not Set

Execution Instructions

XEC	Execute Unconditionally
XOF	Execute if Overflow Set
XAP	Execute if A Register Positive
XAN	Execute if A Register Negative
XAZ	Execute if A Register Zero
XBZ	Execute if B Register Zero
XXZ	Execute if X Register Zero
XS1	Execute if Sense Switch 1 Set
XS2	Execute if Sense Switch 2 Set
XS3	Execute if Sense Switch 3 Set
XIF	Execute if Combined Conditions Are Met
XOFN	Execute if Overflow Not Set
XANZ	Execute if A Register Not Zero
XBNZ	Execute if B Register Not Zero
XXNZ	Execute if X Register Not Zero
XS1N	Execute if Sense Switch 1 Not Set
SX2N	Execute if Sense Switch 2 Not Set
XS3N	Execute if Sense Switch 3 Not Set

Control Instructions

HLT	Halt
NOP	No Operation
SOF	Set Overflow Indicator
ROF	Reset Overflow Indicator

Shift Instructions

LSRA	Logical Shift Right A Register
LSRB	Logical Shift Right B Register
LRLA	Logical Rotate Left A Register
LRLB	Logical Rotate Left B Register

(continued)

Table 2-2. V77-600 Instructions *(continued)*

LASR	Long Arithmetic Shift Right
LASL	Long Arithmetic Shift Left
LLSR	Long Logical Shift Right
LLRL	Long Logical Shift Left
ASRA	Arithmetic Shift Right A Register
ASLA	Arithmetic Shift Left A Register
ASRB	Arithmetic Shift Right B Register
ASLB	Arithmetic Shift Left B Register

Register-Change Instructions

IAR	Increment A Register
IBR	Increment B Register
IXR	Increment X Register
DAR	Decrement A Register
DBR	Decrement B Register
DXR	Decrement X Register
CPA	Complement A Register
CPB	Complement B Register
CPX	Complement X Register
TAB	Transfer A Register to B Register
TAX	Transfer A Register to X Register
TBA	Transfer B Register to A Register
TBX	Transfer B Register to X Register
TXA	Transfer X Register to A Register
TXB	Transfer X Register to B Register
TZA	Transfer Zero to A Register
TZB	Transfer Zero to B Register
TZX	Transfer Zero to X Register
AOFA	Add Overflow to A Register
AOFB	Add Overflow to B Register
AOFX	Add Overflow to X Register
SOFA	Subtract Overflow from A Register
SOFB	Subtract Overflow from B Register
SOFX	Subtract Overflow from X Register
MERGE	Merge Source to Destination
INCR	Increment Source to Destination
DECR	Decrement Source to Destination
COMPL	Complement Source to Destination
ZERO	Zero Register

(continued)

Table 2-2. V76 Instructions *(continued)*

I/O Instructions	
SEN	Program Sense
EXC	External Control
EXC2	Auxiliary External Control
CIA	Clear and Input to A Register
CIB	Clear and Input to B Register
CIAB	Clear and Input to A and B Registers
INA	Input to A Register
INB	Input to B Register
INAB	Input to A and B Register
OAR	Output from A Register
OBR	Output from B Register
OAB	Output from A and B Registers
IME	Input to Memory
OME	Output from Memory
Floating Point Instructions	
FLD	Single Precision Load
FLDD	Double Precision Load
FST	Single Precision Store
FSTD	Double Precision Store
FLT	Reformat to Floating Point
FIX	Reformat to Fixed Point
FAD	Floating Add Single Precision
FADD	Floating Add Double Precision
FSB	Floating Subtract Single Precision
FSBD	Floating Subtract Double Precision
FMU	Floating Multiply Single Precision
FMUD	Floating Multiply Double Precision
FDV	Floating Divide Single Precision
FDVD	Floating Divide Double Precision

SECTION 3
PROCESSOR

3.1 GENERAL DESCRIPTION

The V77-600 processor, the central processing unit for the V77-600 computer, performs arithmetical and logical operations on 16-bit instruction and data words using standard V70 software. Unlike a conventional processor with a typical program control interface, the processor contains an internal control store with microprogrammed elements for faster and more efficient processor operations. Refer to the V70 Series Architecture Manual for the functional description of the processor and illustrated functional differences between a conventional and a microprogrammed processor.

Functional sections of the processor are contained on two boards, the processor and option boards, which are tied to the computer control panel board via the I/O bus. The I/O bus is part of a multiple bus structure which ties the internal sections together and to other components of the computer. Processor circuits are on the 15.6 by 19 inch processor board and the I/O control circuits are on a portion of the 15.6 by 19 inch option board. Refer to section 5 for the location of each of these boards in each type of mainframe chassis for each different V77-600 computer configuration. The control panel board is located on the back side of the control panel. Interconnection information for these three boards can be found in the V77-600 Processor Manual.

3.2 ELEMENTS OF MICROPROGRAMMING

In the processor, the control section controls some of the frequently performed operations of the other processor sections without instructions from a software program stored in the main memory (section 4). These controls are accomplished instead by altering the physical configuration of a high-speed programmable read-only-memory (ROM) integrated circuit (IC) device (firmware) located in the processor's internal control store. The physical array of the ROM IC is electrically altered (programmed) one time to provide up to 512 64-bit fixed control words written in simple machine language (binary code). Each of these 64-bit control words causes various elementary level tasks to be performed by other processor devices. Because they manipulate and control functional operations at the most elementary level, the control words are called microinstructions and the set of microinstructions is called a microprogram. Although they are both hardware related and perform similar tasks, the set of microinstructions should not be confused with the standard macro instruction set. The V70 series instructions are used to develop software programs that deal with complex operations of the entire computer system; whereas, the set of microinstructions are used to develop a microprogram that deals only with simple processor operations. Nevertheless, microprogramming is an important feature of the processor because it permits more compact program representation and reduces the number of main memory address locations required for system operation. In addition, the processor, with high-speed logic and programmable ROM, has a microinstruction execution time of only 165 nanoseconds as compared with a full-cycle time of 660 nanoseconds for standinstructions. A more detailed explanation of microprogramming is given in the V70 Microprogramming Guide.

3.3 STANDARD FEATURES

The following standard features are included with the processor:

- Automatic program loader
- Memory parity
- Hardware priority interrupt
- Direct memory access (DMA)

3.3.1 Instruction Set

The processor provides an instruction set with 201 standard instructions. This standard instruction set includes 27 instructions that permit programmer access to 8 general-purpose registers and operates on 8, 16, and 32-bit operands. The 27 instructions utilize registers R0 through R7; whereas, the remaining 174 instructions utilize registers R0, R1, and R2 only. The instruction format for each of these instructions is described in the V70 Series Architecture Manual.

3.3.2 Hardware Multiply/Divide

The hardware multiply/divide feature enhances the computational capabilities of the processor by reducing the number of steps required for multiplication and division operations.

During multiplication, the contents of the effective memory address are multiplied by the contents of the R1 register, then the R0 register contents are added to the product. The result is placed in the R0 and R1 registers, with the most significant half in the R0 register and the least significant half in the R1 register. The sign of the result is in bit 15 (sign bit) of the R0 register. The R1 register sign bit is always set to zero. The largest positive multiplier or multiplicand in an operation register of the processor is thus 15 binary bits.

During division, the dividend is contained in the combined R0 and R1 registers with the sign in bit 15 of the R0 register. The R1 register sign bit is not used. The divisor is in the effective memory address. The quotient and its sign are placed in the R1 register and the remainder (with the sign of the dividend), in the R0 register.

3.3.3 Automatic Program Loader

The automatic program loader is stored in a programmable read only memory in the processor. When a load command is received from the control panel, the loader is transferred to main memory. The loader is executed and reads the loading program into main memory from the peripheral device (Teletype, paper tape, or disc). Further information on the program loader is provided in section 7.

3.3.4 Memory Parity

The memory parity generates and checks parity for left and right bytes when accessing memory. Parity bits are generated during the memory writing sequence and are checked during the reading sequence. This circuit contains its own control and interrupt logic.

There are two external control instructions that enable (0445) and disable (0545) parity. Parity is generated and checked, but an interrupt is not generated if parity is disabled.

3.3.5 Hardware Priority Interrupt

The hardware priority interrupt feature establishes priorities for initiating a memory operation. Priority logic within the memory control section receives requests for memory operations from the priority memory access (option board), the I/O control section (option board), and the central control section (processor board) and determines the priorities for associated hardware.

3.3.6 Direct Memory Access (DMA)

The DMA feature permits I/O hardware to access the memory directly without requesting access through the central control section. This is known as cycle stealing I/O or trapping. This mode of operation allows peripheral signals on the I/O bus to transfer data to or from memory while temporarily halting the processing of the stored program.

3.4 OPTIONAL FEATURES

The optional features listed below are available with the V77-600 computer. The first five are described in this section, and the last four are described in section 5 along with configuration information.

- Power failure/restart (PF/R)
- Teletype controller (TC)
- Real-time clock (RTC)
- Memory protection (MP)
- Priority memory access (PMA)
- Megamap
- *Cache*
- *Writable control store (WCS)*
- Floating point processor (FPP)

3.4.1 Power Failure/Restart

The power failure/restart (PF/F) protects, during loss or reduction of ac line voltage, the program in progress and the contents of computer memory and registers. Upon restoration of

power, the PF/R automatically restarts the computer and causes it to reenter the interrupted program at the point of interruption.

Power reduction, failure, or turn-off initiates a power-down cycle during which the PF/R sustains execution of the current instruction and then interrupts the processor, directing it to the address of the user prepared SAVE subroutine. This SAVE subroutine loads the contents of the volatile registers (R0, R1, R2, program counter and overflow) into preselected addresses in memory. After the execution of SAVE, the PF/R disables the processor and memory until power is restored.

When power is restored so that all power-up conditions are satisfied, the PF/R enables the processor and memory, initiates the system-start signal, and directs the processor to the address of the RESTORE subroutine. This service subroutine reloads the registers with the saved data, and contains a jump instruction that directs the processor to reenter the program at the point of interruption and continue execution.

3.4.2 Teletype Controller

The Teletype controller (TC) is a serial, asynchronous, full-duplex, data-transfer interface between the processor and a Model 33 or 35 Teletype, using the I/O bus. The TC also provides for the buffering of data, the sensing of status by the processor, an interrupt capability for priority interrupt module (PIM) control, and the initialization of the system through program control or by use of the RESET switch on the control panel.

3.4.3 Real-Time Clock

The real-time clock (RTC) provides the following real-time functions:

- Variable-interval interrupt
- Memory-overflow interrupt
- Readable free-running counter

The variable-interval interrupt has three preselectable hardware timing sources: (1) a 10KHz signal (standard unless otherwise specified), (2) line frequency from the power supply, or (3) a user-supplied external source. The rate of the variable-interval interrupt is selectable under program control as follows. The program loads a number n between 1 and 4095 into the variable-interval logic. The logic repeatedly counts down from n to 0, issuing an interrupt each time 0 is reached. The variable-interval interrupt rate is thus 1/nth of the timing source rate.

The memory-overflow interrupt, which operates in conjunction with the variable-interval interrupt, is implemented by loading an increment-memory-and-replace instruction into the address of the variable-interval interrupt. This is monitored by the overflow-detection logic, which triggers the memory-overflow interrupt when the contents of the variable-interval interrupt are incremented to 040001.

The 16-bit readable free-running counter is continually updated and may be read under program control. Counter timing is based on the 10KHz clock, the variable-interval interrupt rate, the line frequency, or a user-supplied external source.

3.4.4 Memory Protection

Memory protection (MP) is contained on the V77 option board. MP prevents unauthorized or unintentional program access to, or modification of, protected areas of memory.

Memory is divided into 512-word segments, each of which can be either protected or unprotected. Segments not designated as protected are, by definition, unprotected. The protected/unprotected status of each segment is stored in the MP in eight 16-bit mask registers that are loaded by I/O instructions from the processor. These mask registers can store the status of up to 128 memory segments (65K).

MP monitors the address of the instruction being processed, the address specified by the next instruction in sequence, and the address specified by the effective address. Using this information and the status of the stored segment, the MP detects and operates on errors.

When a program is executed in unprotected memory, any of the following operations constitutes an error:

- Overflowing into a protected segment
- Writing into a protected segment
- Jumping into a protected segment
- Executing an I/O instruction in an unprotected segment
- Executing a halt instruction in an unprotected segment

When MP detects an error, execution of the current instruction is allowed to complete. However, if the instruction specifies writing or I/O operations, the contents of the R0, R1, and R2 registers, and memory are not modified and the I/O command is not issued to the I/O bus. The program is then interrupted and directed to one of five preassigned memory addresses. From this address, the program is directed to a user-written service subroutine for error analysis and correction.

3.4.5 Priority Memory Access (PMA)

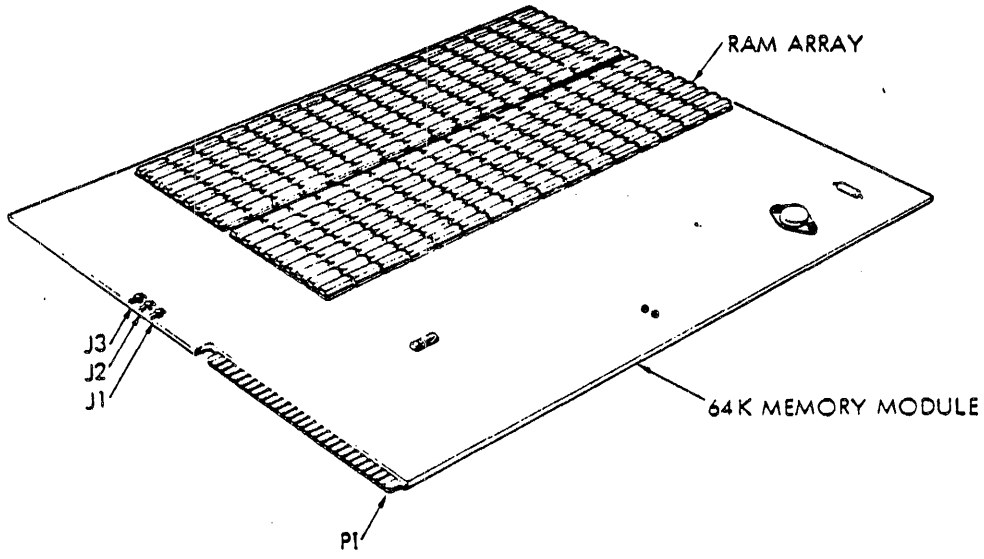
The priority memory access (PMA) is a mainframe option for the computer. The PMA option interfaces with PMA controllers to provide logic functions to interface four data transfer channels with the memory in a hardware-fixed priority. All signals can be asynchronous to free the PMA option/PMA controller interface from circuit and cable speed dependence. Also there is the capability to handle a variety of circuits and data rates, or synchronous operation for maximum rate of data transfer.

The PMA option can interface with up to eight PMA controllers distributed in any manner among the four priority levels although only one PMA controller per level can be active at a time. Each PMA controller interfaces with the PMA logic circuits on the option board in the mainframe and with the I/O bus for program control.

SECTION 4
MEMORY SYSTEM

4.1 GENERAL DESCRIPTION

The V77-600 computer utilizes a dual-port, random-access, semiconductor memory with an internal cycle time of 660 nanoseconds. This memory system can contain one or more of the 660 nanosecond semiconductor memory modules for storing instructions and data supplied by the computer or a peripheral device. Available in six different models (three with and three without parity), a memory module is contained on a single printed circuit (PC) board. Each memory module has a memory array for storing data and other logic for interfacing with computer or peripheral processors. The memory array for each of the six different models has a different number of dynamic storage elements placed in rows on the associated PC board (figure 4-1).



VTI1-3576

Figure 4-1. 660 Nanosecond Semiconductor Memory

4.2 MEMORY DESIGN

The basic memory array storage element is a dynamic 4,096-word (4K) by 1-bit random-access-memory (RAM) integrated circuit (IC) device with an N-channel, high-density, metal-oxide-semiconductor (MOS) substrate. Each 4K MOS RAM device is packaged in a 16-pin dual-in-line ceramic or plastic case that plugs into an IC socket on the memory module PC board. A single row of sixteen of these elements provides the 16-bit format for 4,096 computer words without parity.

Although the 4K MOS RAM elements are dynamic in operation, they are also volatile with respect to power which is characteristic of semiconductors. For this reason, each semiconductor memory module has internal refresh circuitry to periodically refresh (recharge) data already stored in the 4K MOS RAM elements. This feature prevents stored data from being lost during a read or write memory cycle. To prevent stored data from being lost during a computer power failure, a battery powered data-save option (Power Supply Manual, 98 A 9906 13x), installed on the power supply chassis, must be used to provide appropriate voltages to the refresh circuitry of each memory module.

The respective array for each of the three models of memory mdoules without parity contains 64, 128, and 256 elements for storing 16,384 (16K), 32,768 (32K), or 65,536 (64K) by 16-bit words. The PC board array for each of the three models of memory modules with parity contains 72, 144, or 288 elements, respectively, and is arranged with two additional elements per 4K row. These two additional elements per row provide 2 parity bits for each 16-bit word or one parity bit per 8-bit byte.

Each memory module PC board is also designed with an edge connector having two independent sets of memory bus terminals (port A and port B) for data entry and retrieval (write and read) from two different sources, e.g.; main and peripheral processors. A memory bus (ribbon cable) interconnects all of the memory modules at the rear of the mainframe or memory expansion chassis. In addition to the P1 edge connector, each 64K memory module PC board has two port-request connectors, J1 and J3, that connect to the megamap for management of a dual-port expanded memory system. Another connector, J3, is a refresh request connector that is provided for connection to an error correction circuit.

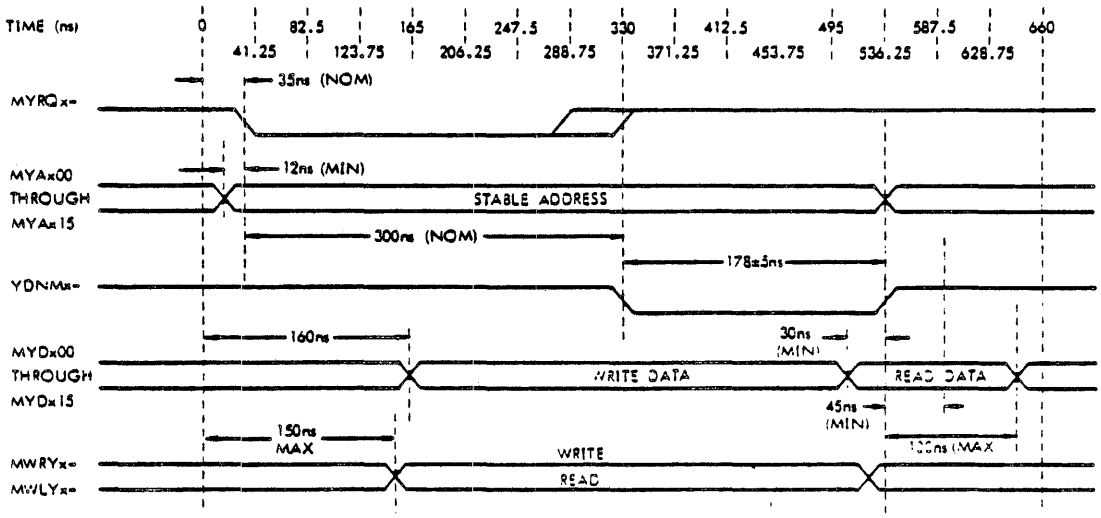
4.3 MEMORY INTERFACE

When installed in a mainframe chassis, the 660 nanosecond semiconductor memory option may interface via the memory bus, with the processor, option board, another memory bus (dual port), the writable control store option, megamap option, cache memory option, and floating-point processor option. All signals on the memory bus are buffered throgh the interfacing TTL logic to help eliminate noise problems and cross-talk. Typical interface signal waveforms are shown in figure 4-2. The address and control lines are unidirectional and the data lines are bidirectional. Interconnection of boards in the mainframe or memory expansion chassis is made with ribbon cables that connect at the rear of each chassis, thereby keeping the length of input/output lines to a minimum.

4.4 MEMORY TRANSFERS

Instruction and data transfers between processors and memory take place under the control of the source program. Initially, the input section of the main processor or peripheral processor receives binary-coded program instructions and data, in serial form, from input peripheral devices, e.g.; card readers, keyboard terminals, magnetic tape units, etc. and translates this information into a parallel binary format that can be accepted and stored by the 660 nanosecond semiconductor memory. The instruction and data words inherent to the controlling program are then executed by the control section of the main processor or transferred through the I/O bus connected to a peripheral controller and subsequently written into the elements of the memory array.

Instructions and data words, in parallel form, are read from the elements of the 660 nanosecond memory array and transferred to the control section of the main processor for execution. Under the control of the source program, these instructions and data words are then manipulated by the arithmetic section or routed directly to the output section of the main processor. The output section translates the processed instructions and data to a serial format that can be accepted by output peripheral devices, e.g., card punches, line printers, magnetic tape units, etc. and transmits this translated information to peripheral controllers through the I/O bus.



VTI1-3578A

Figure 4-2. Typical Interface Waveforms

4.5 WRAP-AROUND ADDRESSING

Since a processor is the address source, a memory address can specify a nonexistent memory location above the physical capacity of the memory. However, wrap-around addressing, available (upon request) as a feature of the 660 nanosecond semiconductor memory, automatically prevents the processor from accessing such a nonexistent memory location. If a memory has this wrap-around feature, the nonexistent address is directed to a corresponding physical address location where the processed data can be stored. Thereafter, when that nonexistent address occurs, the same corresponding physical address will be accessed. Without this capability, nonexistent addresses will result in an erroneous zero data readout and a loss of written data.

4.6 SPECIFICATIONS

Performance specifications for the 660 nanosecond semiconductor memory system are listed in table 4-1.

MEMORY SYSTEM

Table 4-1. Memory Specifications

Parameter	Description
Design	Dual-port and expandable utilizing dynamic 4K metal oxide semiconductor (MOS) random access memory (RAM) integrated circuit elements in a single board array
Cycle time	660 nanoseconds
Access time	560 nanoseconds
Capacity	16K, 32K, or 64K words per module
Operating modes	Memory address and internal refresh
Operating environment	0 to 50 degrees C; 0 to 90 percent relative humidity without condensation

SECTION 5
COMPUTER CONFIGURATIONS

5.1 CONFIGURATION CATEGORIES

Each single V77-600 computer configuration in this section is categorized according to the performance options included with standard computer components. If the configuration includes only those mainframe options required for basic computer operation, it is described under the basic configuration section. On the other hand, if the included mainframe options enhance basic V77-600 operation, the configuration is described under the high-performance configuration section.

A multiple computer configuration is described under the multiple computer/shared memory section. Like the basic V77-600 configurations, the multiple configuration is not shown with high-performance mainframe options.

All configurations described in subsequent paragraphs under each of these three categories have been selected to illustrate the flexibility built-in to V77-600 packaging, chassis and cabling layout, and expansion.

5.2 BASIC CONFIGURATIONS

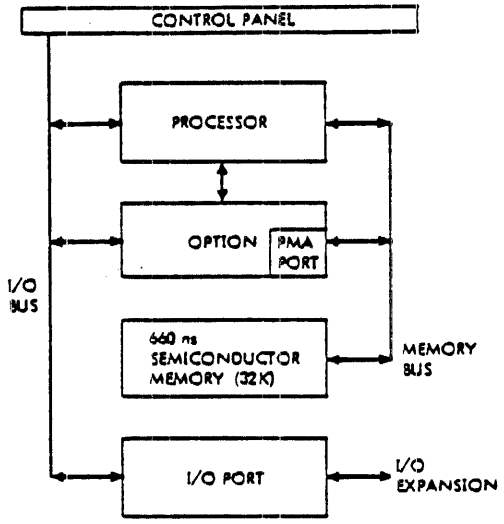
The basic configurations of the computer are either single or dual port configurations with minimum and maximum memory systems. These are typical configurations without high-performance mainframe options.

5.2.1 Single Port

The basic single port configurations utilize a standard processor, one or more optional 660 nanosecond semiconductor memory modules, an optional option board, and an I/O port (connector) for external connection to the I/O expansion chassis. Block diagram, figure 5-1, illustrates the basic single port functional units. Typical board installation and interconnection for single port configurations are shown in figure 5-2.

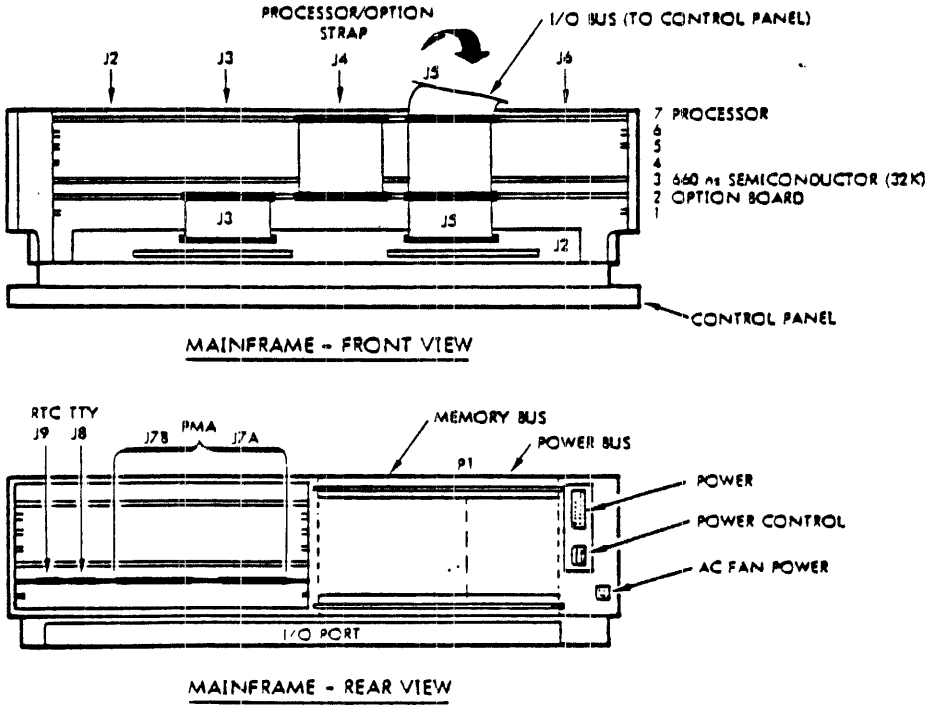
5.2.2 Dual Port

The basic dual port configurations not only utilize the same functional units as the single port configurations but also utilize a second memory bus. As a result, configurations with dual ports A and B can perform simultaneous I/O transfers and processor to memory reference operations without interference when common memory modules are not simultaneously accessed on both memory busses. Block diagram, figure 5-3, illustrates the basic dual port functional units. Note that the priority memory access (PMA) port shown in the block diagram is always on the port B memory bus. Typical board installation and interconnections for these configurations are shown in figure 5-4.



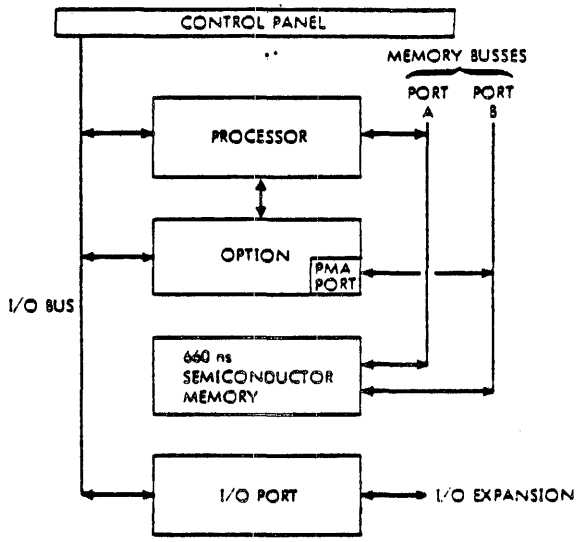
VTII-3554A

Figure 5-1. Basic Single Port Configuration



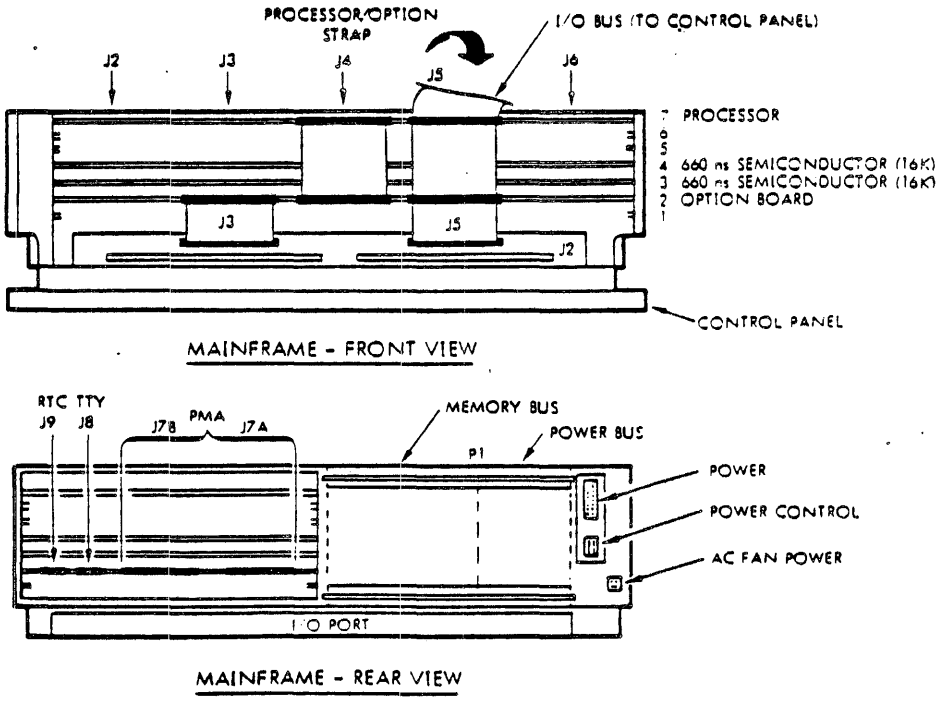
VTII-3555A

Figure 5-2. Typical Basic Single Port Installation



VTI1-3556 A

Figure 5-3. Basic Dual Port Configuration

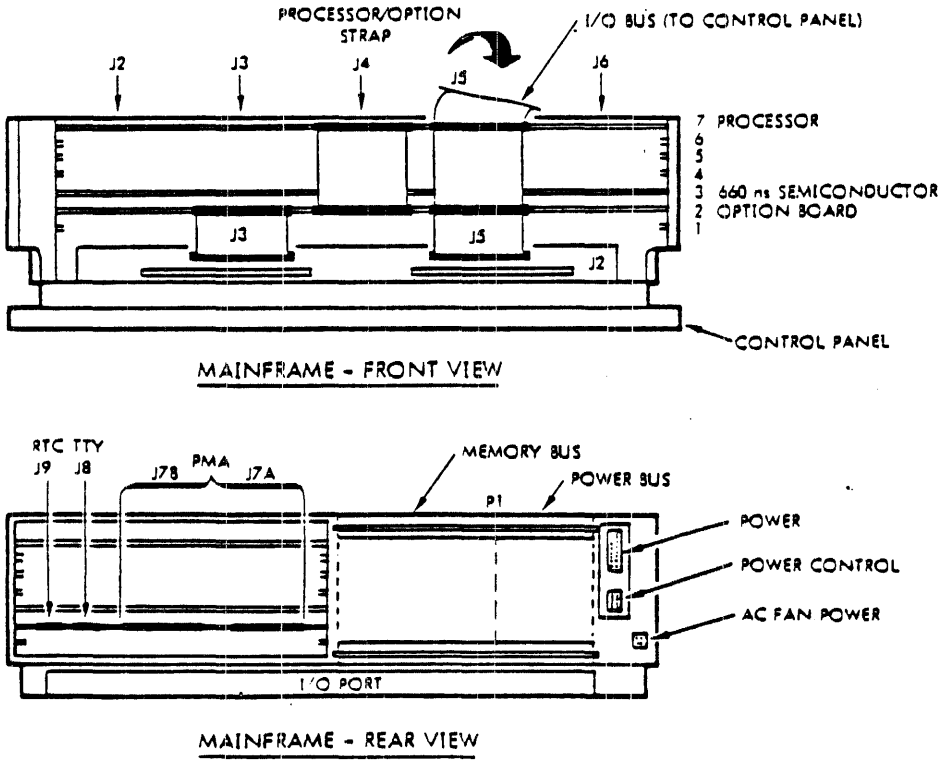


VTI1-3557 A

Figure 5-4. Typical Basic Dual Port Installation

5.2.3 Minimum Memory

A minimum memory system is an optional 660 nanosecond semiconductor memory module with a storage capacity of 16,384 (16K) words. This minimum memory system can be utilized in either a basic single or dual port configuration as described in sections 5.2.1 and 5.2.2. The typical board installation and interconnections for the minimum memory system are shown in figure 5-5.



VTII-3558A

Figure 5-5. Typical Minimum and Maximum Memory for Basic Configurations

5.2.4 Maximum Memory

The maximum memory system for a basic single or dual port configuration has a storage capacity of 32,768 (32K) words which is contained on a single 660 nanosecond semiconductor memory module. The typical board installation and interconnections for the maximum memory system in the basic configuration are shown in figure 5-5.

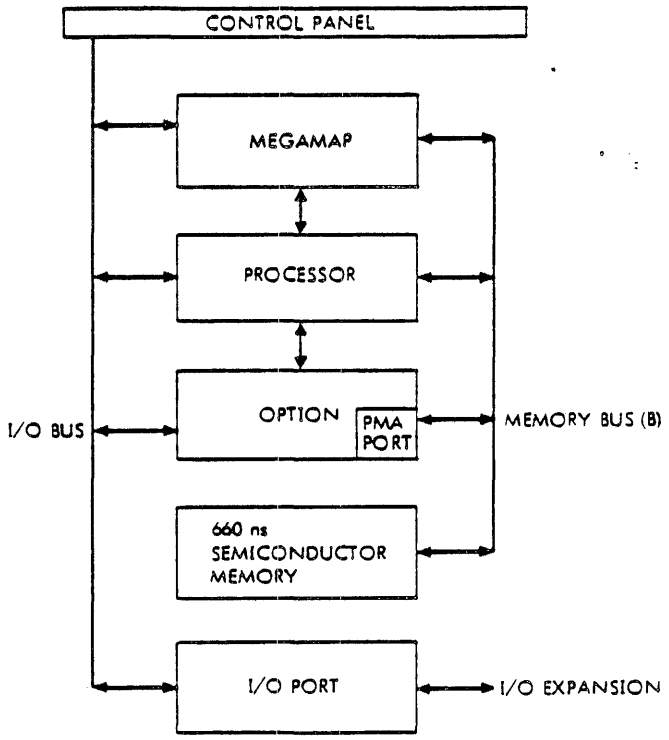
5.3 High-Performance Configurations

The high-performance configurations of the computer contain one or more of the following mainframe options:

- Megamap (Memory Management)
- Writable Control Store (WCS)
- Cache Memory
- Floating Point Processor

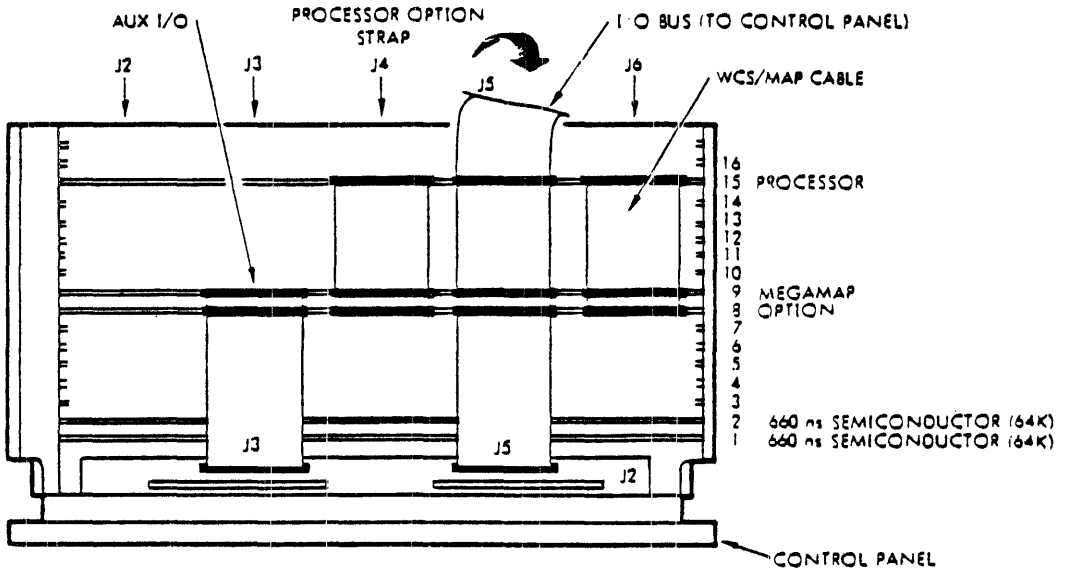
5.3.1 Megamap Option

The megamap option permits the processor to access a 660 nanosecond memory system with a storage capacity above 32K. Block diagram, figure 5-6, shows a typical computer configuration with megamap. Figure 5-7 shows the board installation and interconnections of a typical computer configuration with megamap.

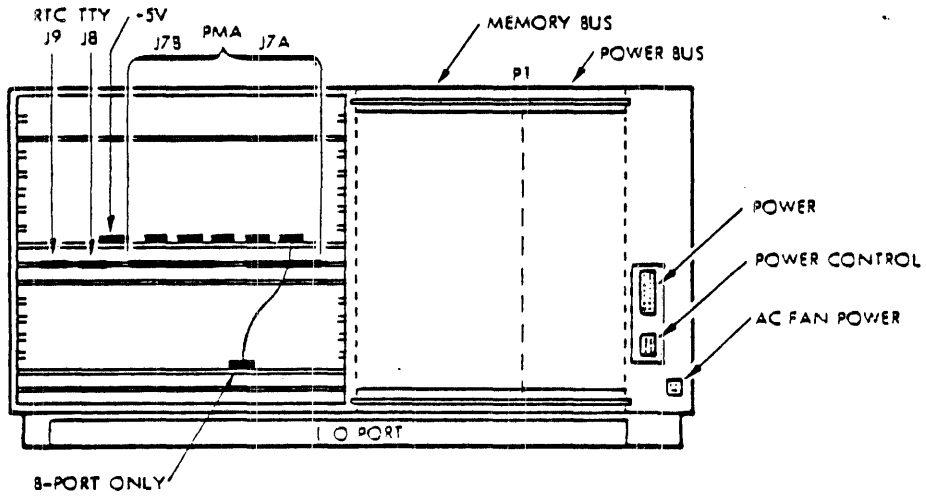


VTI1-3559A

Figure 5-6. Typical Computer Configuration with Megamap Option



MAINFRAME - FRONT VIEW

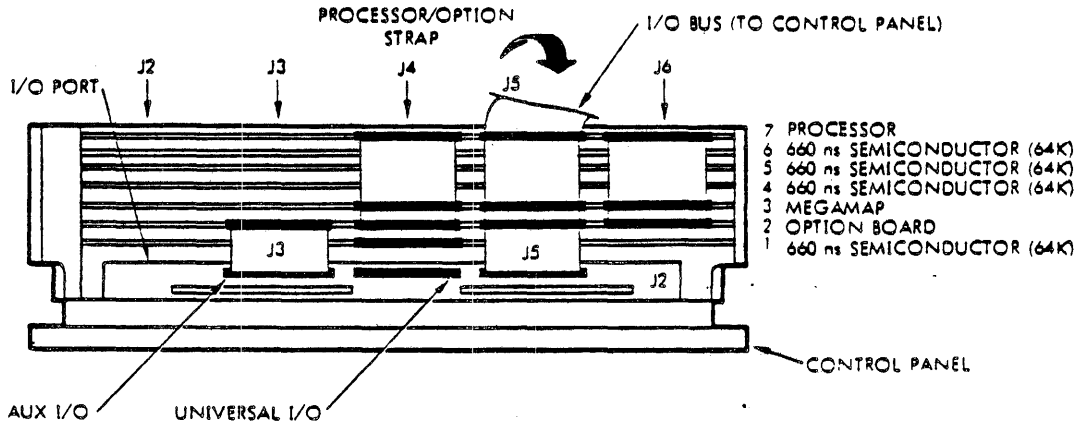


MAINFRAME - REAR VIEW

VTI1-3560 A

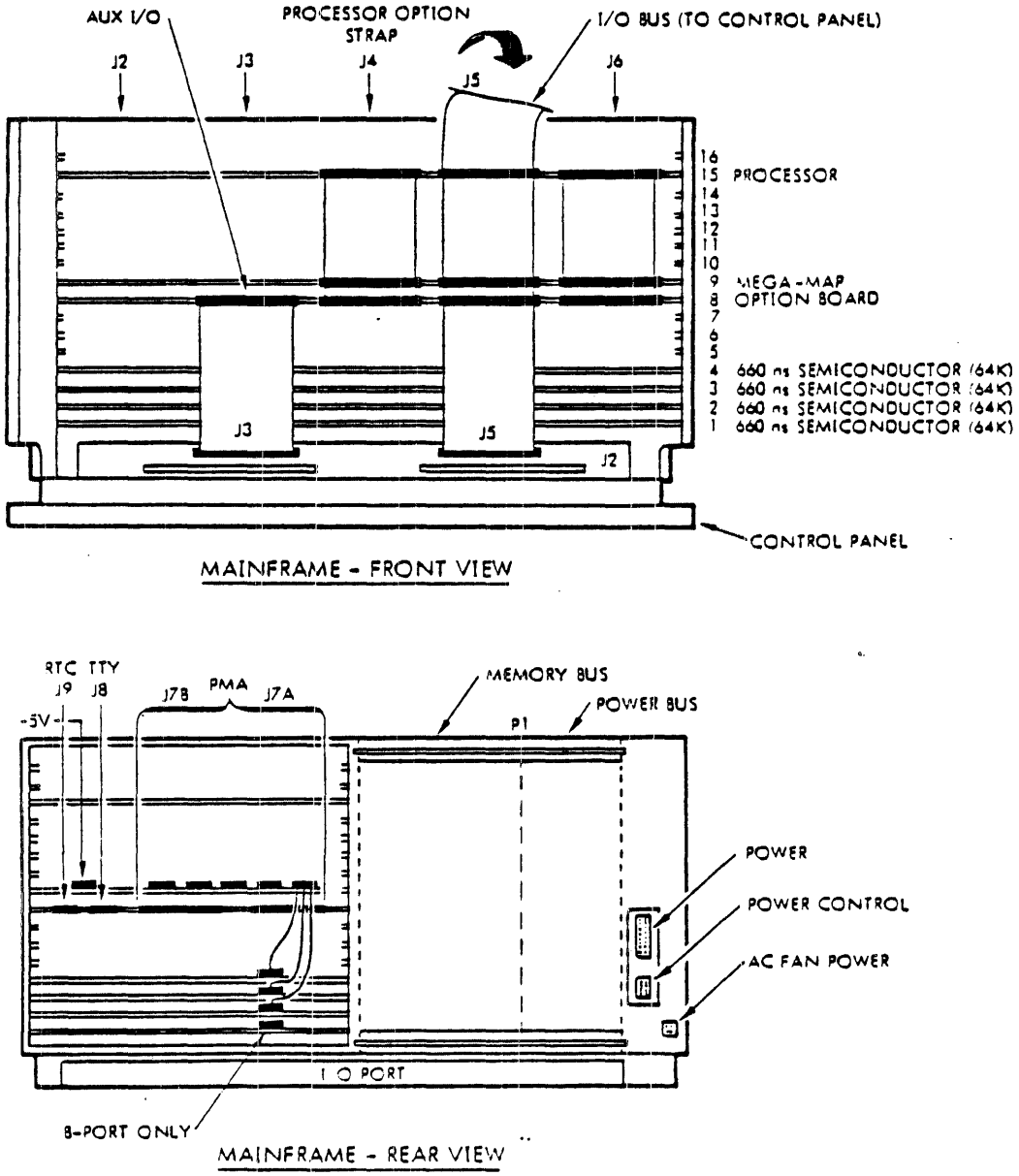
Figure 5-7. Typical Computer Installation with Megamap Option

The maximum memory installation with megamap in a 7-inch mainframe chassis is shown in figure 5-8; the maximum memory installation with megamap in a 14-inch chassis is shown in figure 5-9; and the maximum expanded memory system installation with megamap is shown in figure 5-10. Figure 5-11 shows the cable connections for the expanded system.



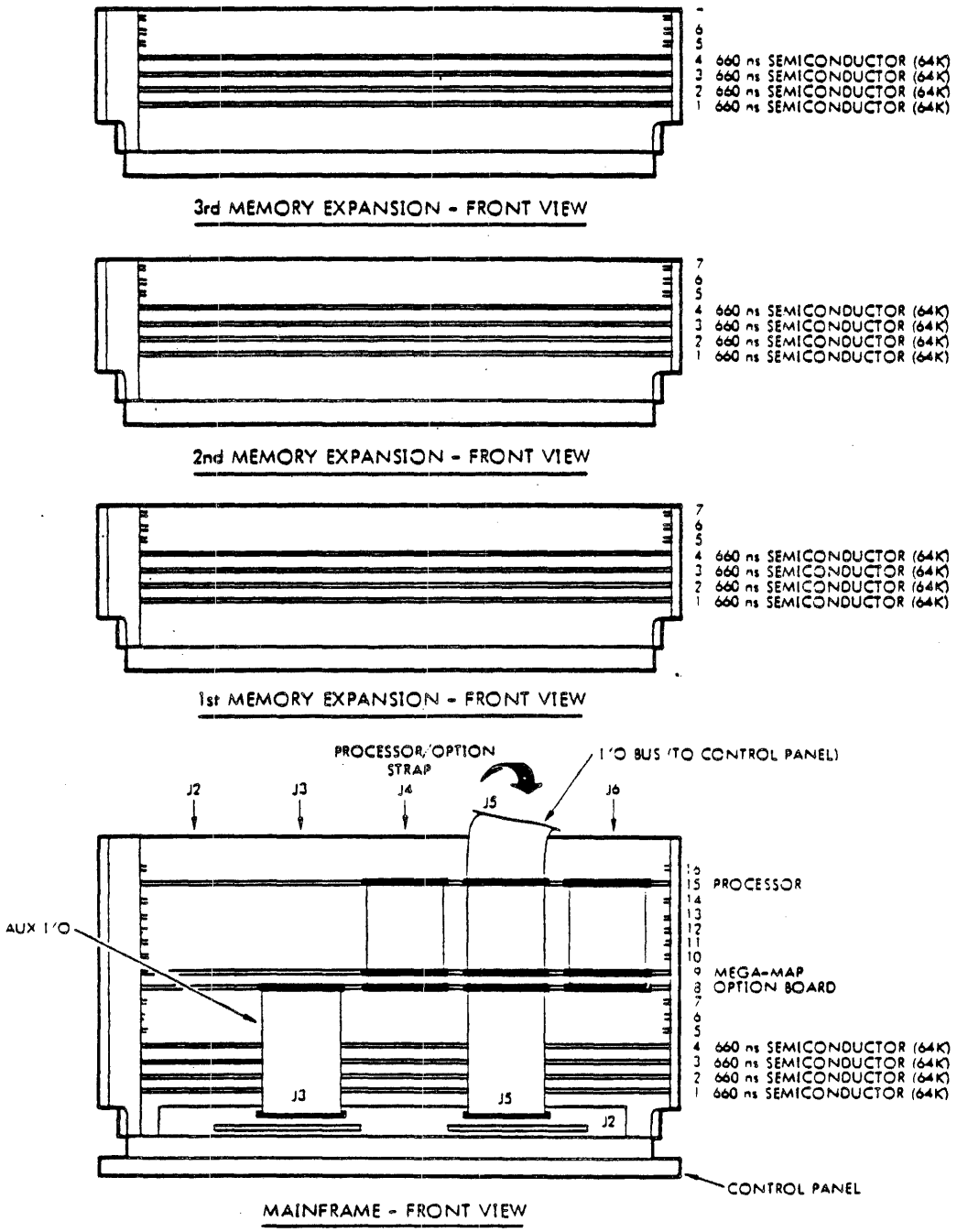
VTI1-3561A

Figure 5-8. Maximum Memory 7-Inch Mainframe Installation with Megamap



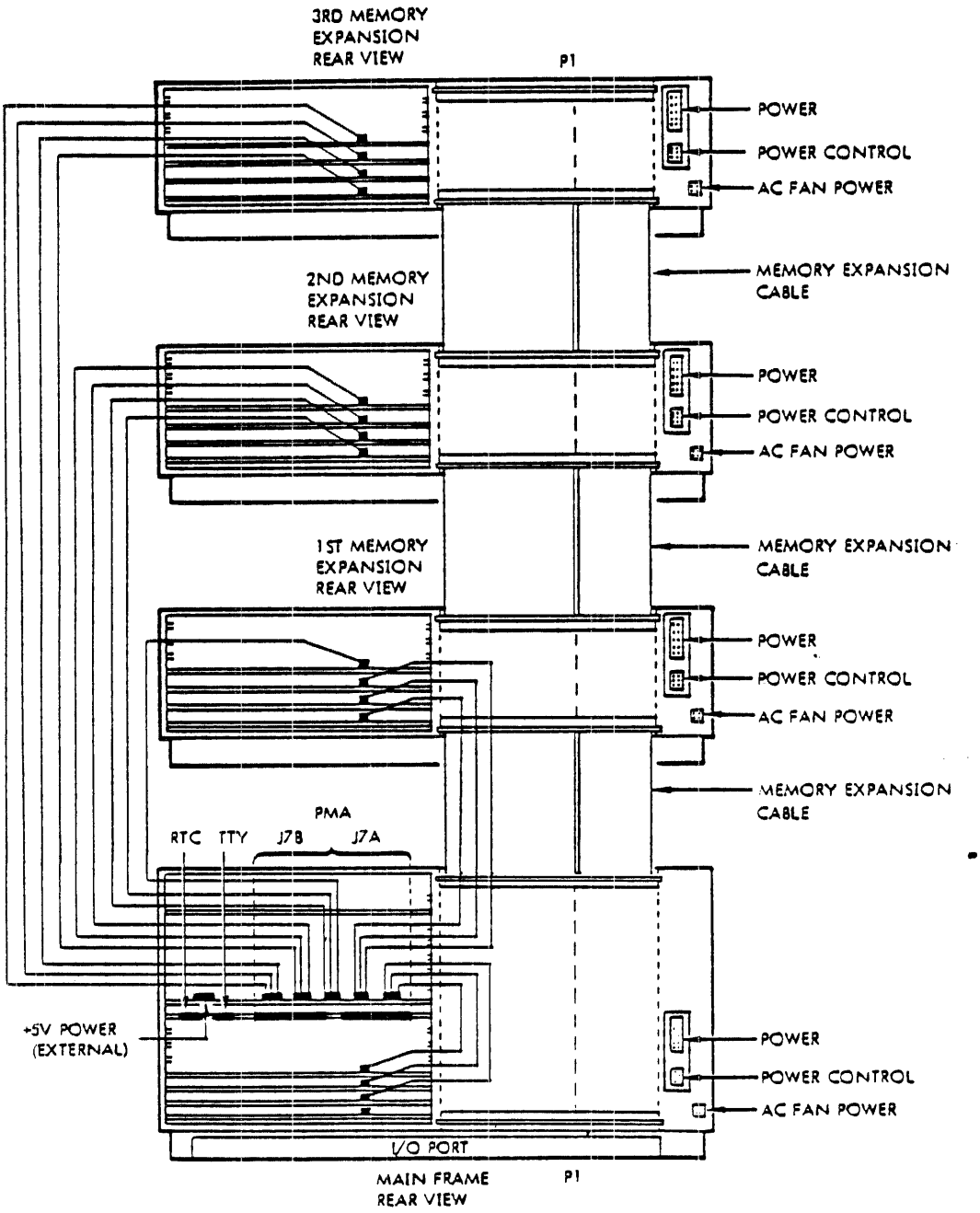
VTI1-3562A

Figure 5-9. Maximum Memory 14-Inch Mainframe Installation with Megamap



VTI1-3563A

Figure 5-10. Maximum Expanded Memory System Installation (1 Mega-word) with Megamap



VT11-3550A

Figure 5-11. Expanded Memory System Cable Connections

5.3.2 Writable Control Store Option

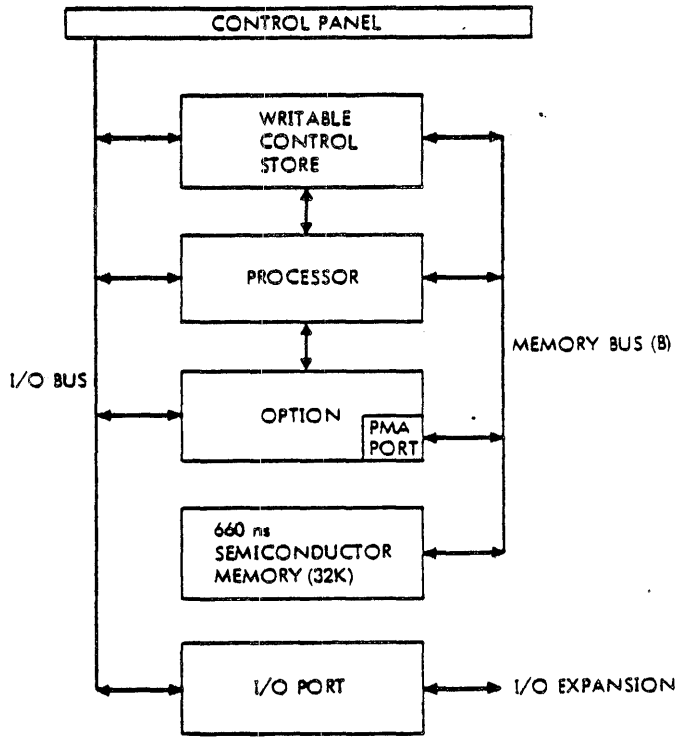
The functional configuration for writable control store (WCS) option is shown by block diagram (figure 5-12); and installation and interconnection (figure 5-13). The WCS inhibits the processor's internal control store and permits application of externally generated test stimuli during troubleshooting procedures. This enables high resolution static or dynamic fault isolation. The WCS is capable of dynamically changing the emulated instruction set and improving performance for specialized functions. Other advantages are:

a. Dynamic alteration of control store contents.

b. Systems can be reconfigured through replacement of faulty hardware functions by firmware routines.

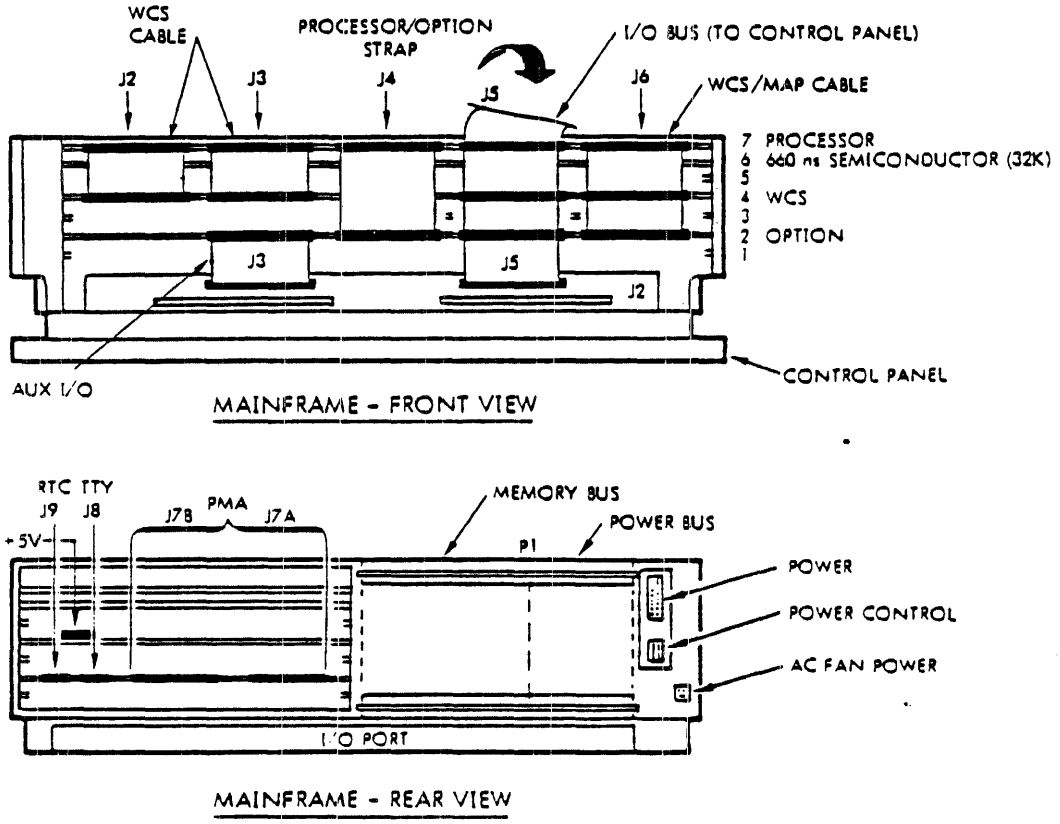
c. Easy incorporation of extensions to existing instruction sets.

The WCS is capable of loading from the memory bus to permit dynamic swapping of control store contents. Control can be by means of privileged I/O instructions.



VTI1-3565 A

Figure 5-12. Block Diagram of Typical Computer System with WCS

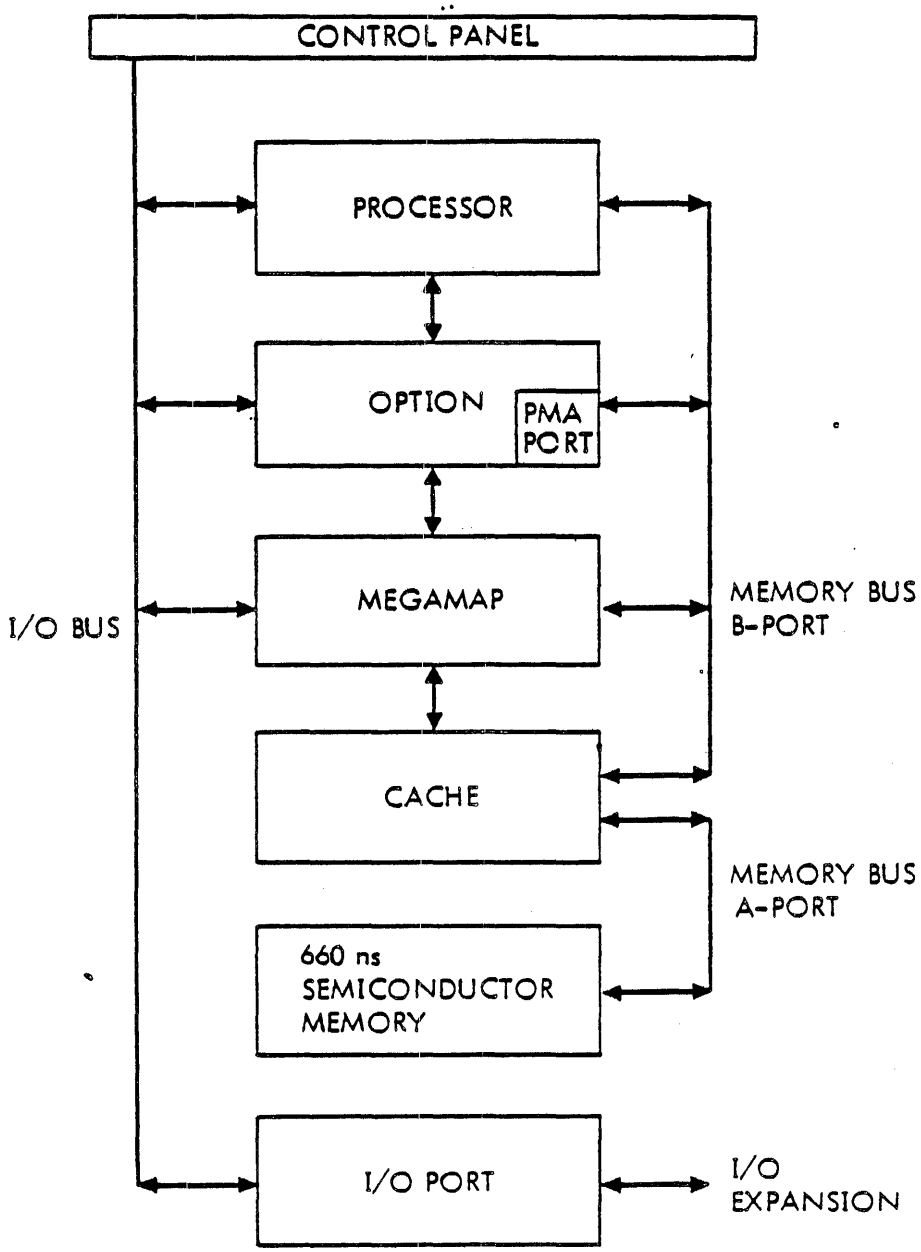


VTI1-3566A

Figure 5-13. Typical Computer Installation with WCS

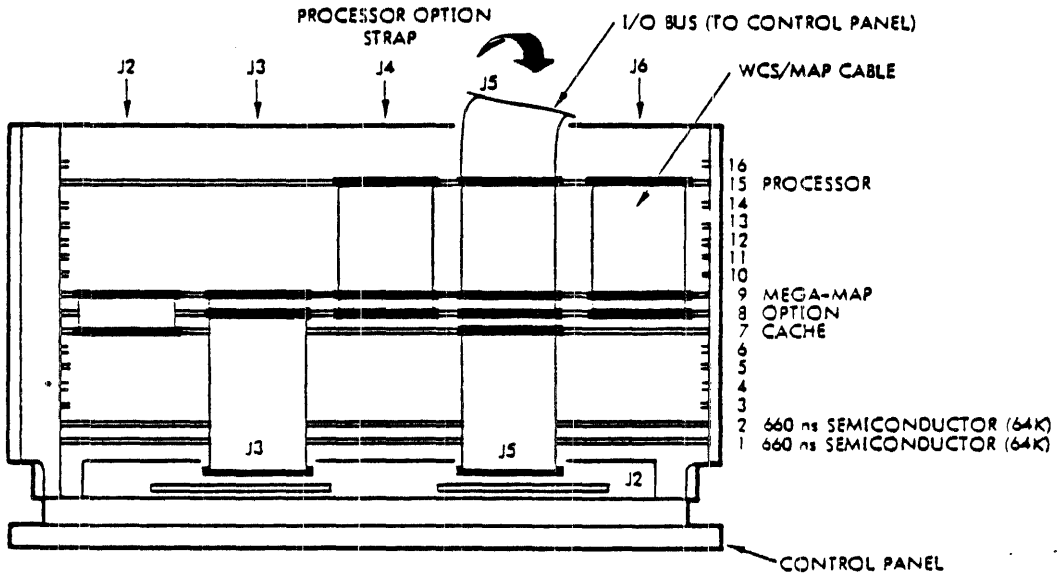
5.3.3 Cache Memory Option

Instructions and data sequentially referenced can account for well over 90 percent of the memory transfers in the execution of a typical application program. System throughput is increased by holding these frequently used words in a special high-speed cache memory which duplicates and stores up to 1,024 words. The system cycle time for the cache memory is only 371 nanoseconds, as compared with 660 nanoseconds for a semiconductor memory module. Block diagram, figure 5-14, shows a typical computer configuration with the cache memory option. Figure 5-15 shows the typical computer installation with the cache memory option.

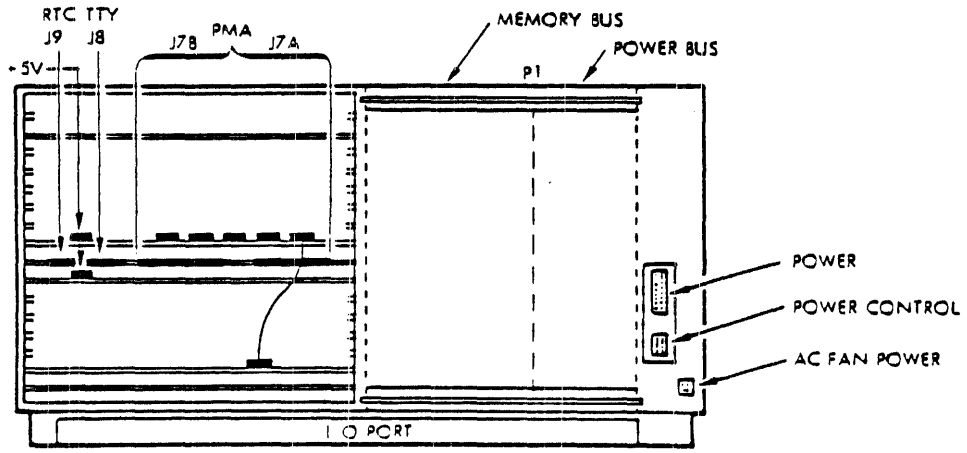


VTI1-3567A

Figure 5-14. Block Diagram of Computer Configuration with Cache Memory Option



MAINFRAME - FRONT VIEW



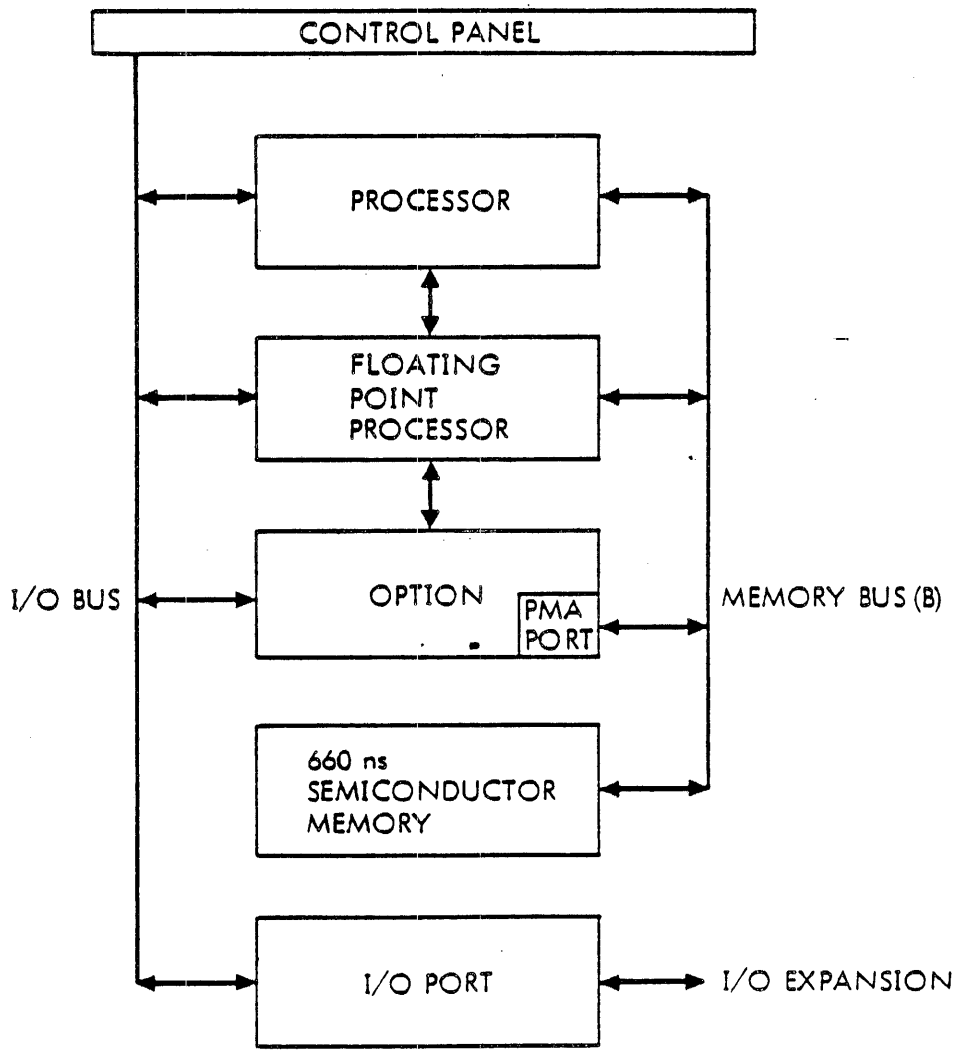
MAINFRAME - REAR VIEW

VTI1-3568A

Figure 5-15. Typical Computer Installation with Cache Memory Option

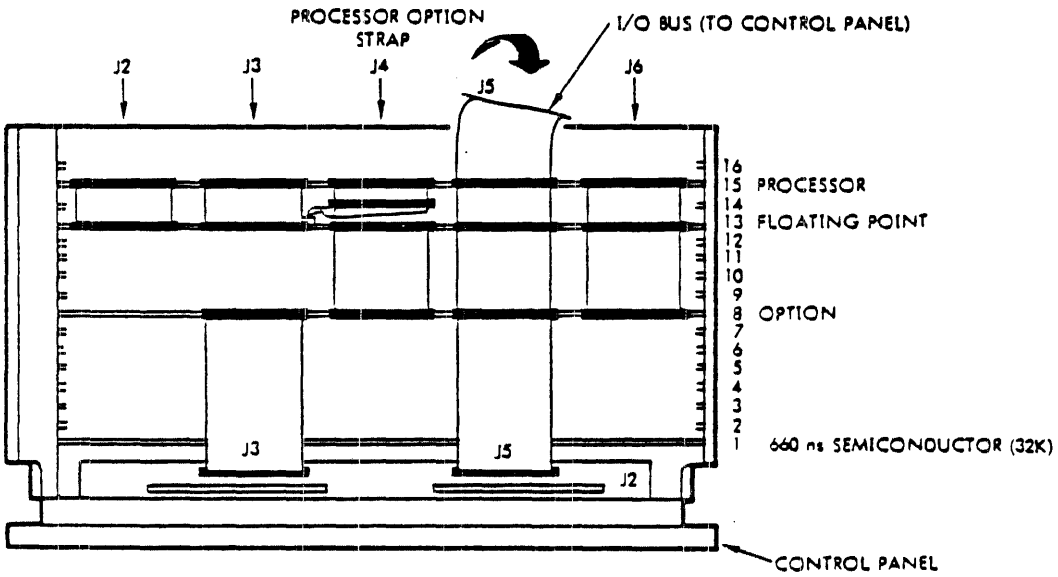
5.3.4 Floating Point Processor Option

The floating point processor option performs high-speed floating point arithmetic on single and double precision numbers. Block diagram, figure 5-16, shows a typical computer configuration with the floating point processor option. Figure 5-17 shows the typical computer installation with the floating point processor option.

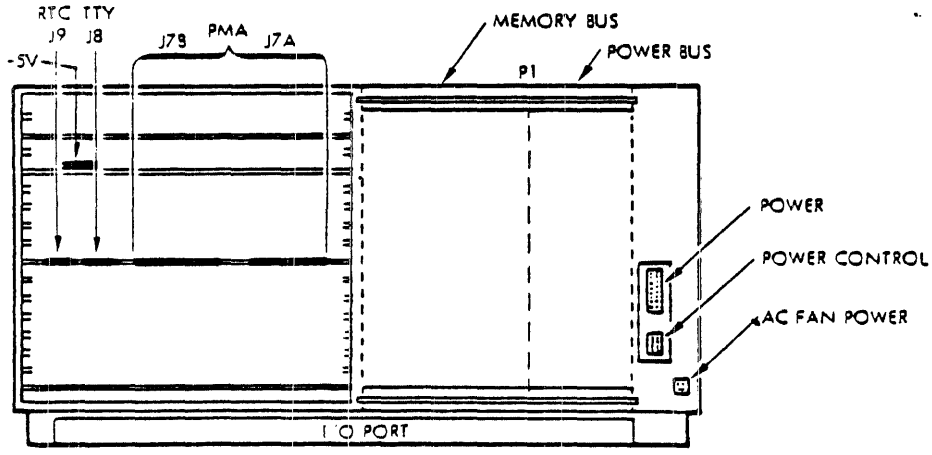


VTI1-3569A

Figure 5-16. Block Diagram of Computer Configuration with Floating Point Processor



MAINFRAME - FRONT VIEW



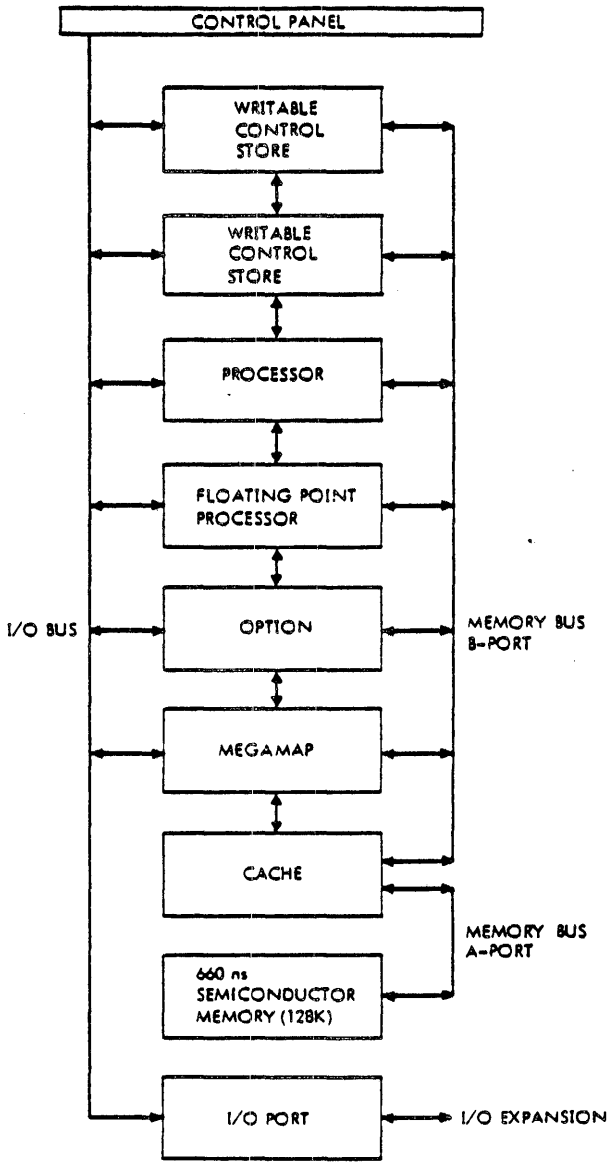
MAINFRAME - REAR VIEW

VTI1-3570A

Figure 5-17. Typical Computer Installation with Floating Point Processor

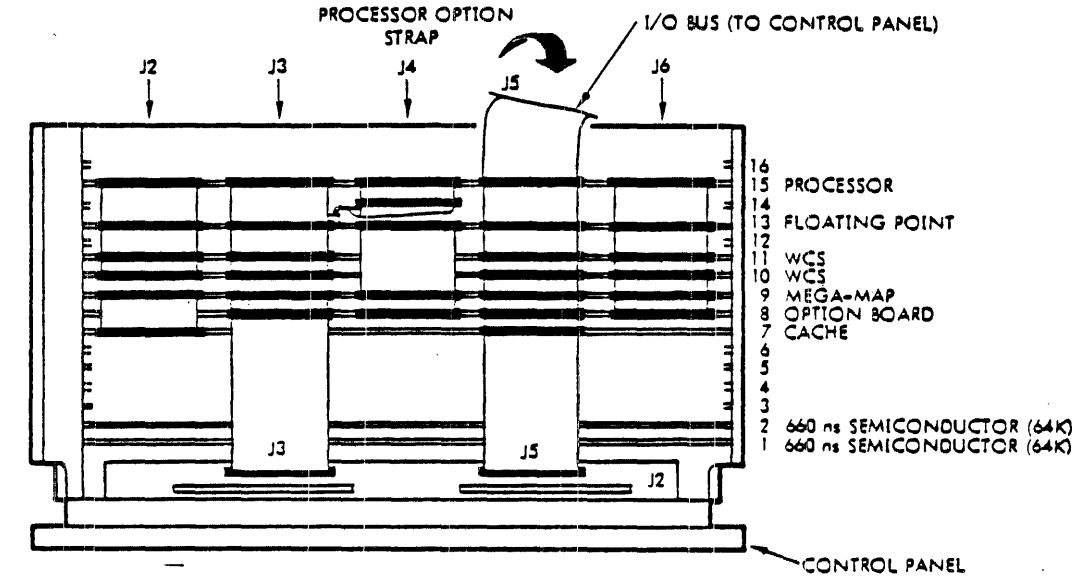
5.3.5 Complete Mainframe Option Package

Block diagram, figure 5-18, shows a typical computer configuration with all of the high-performance mainframe options including two WCS. Figure 5-19 shows the corresponding installation.

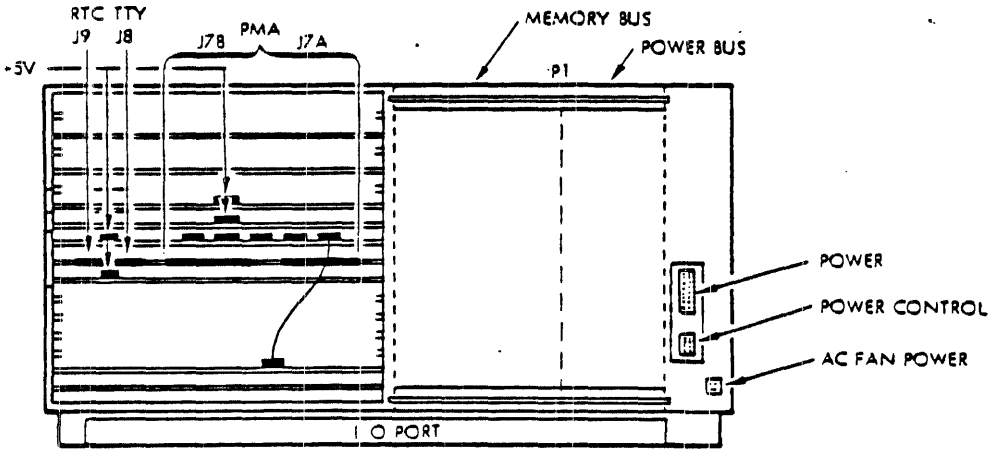


VTII-3571A

Figure 5-18. Block Diagram of Computer Configuration with All Mainframe Options



MAINFRAME - FRONT VIEW



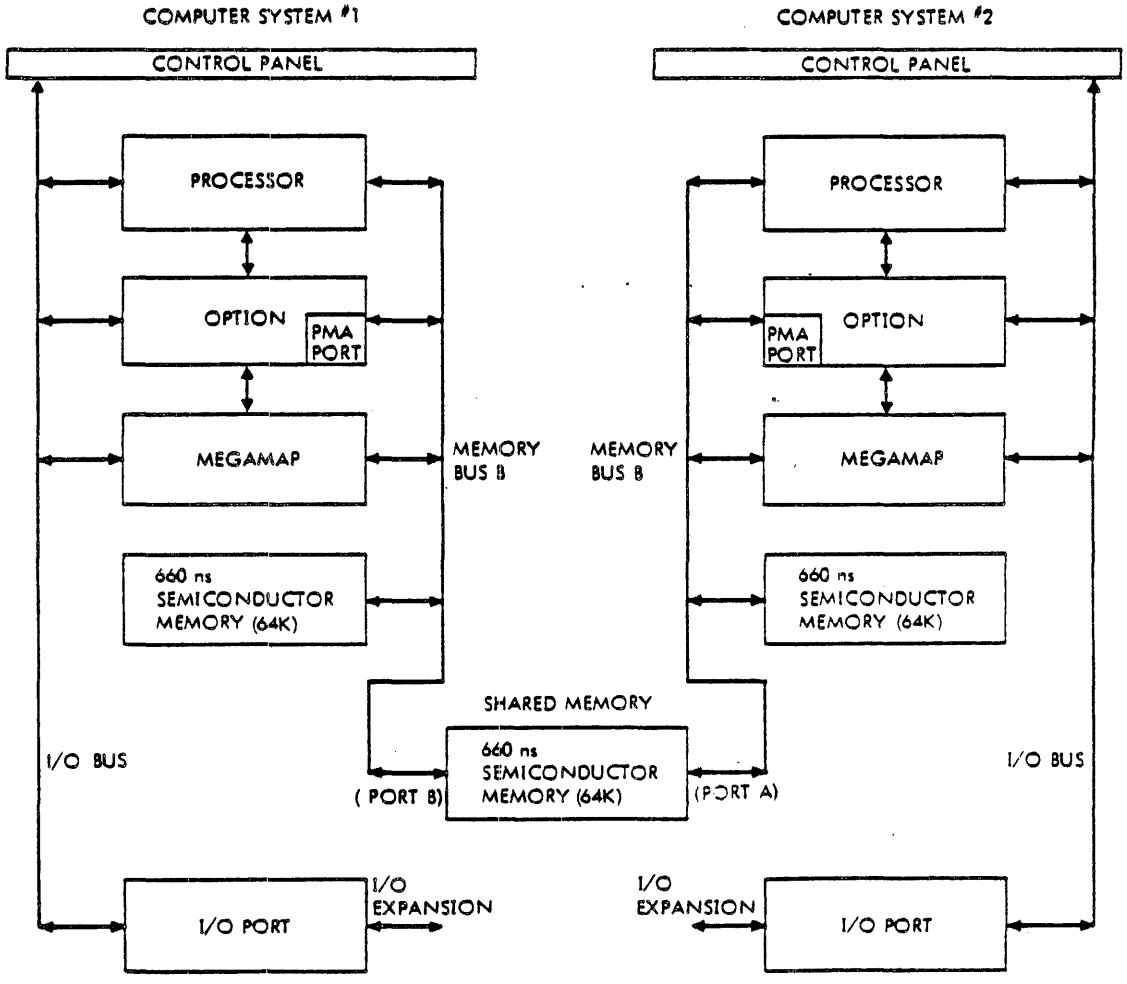
MAINFRAME - REAR VIEW

VTII-3572A

Figure 5-19. Typical Computer Installation with All Mainframe Options

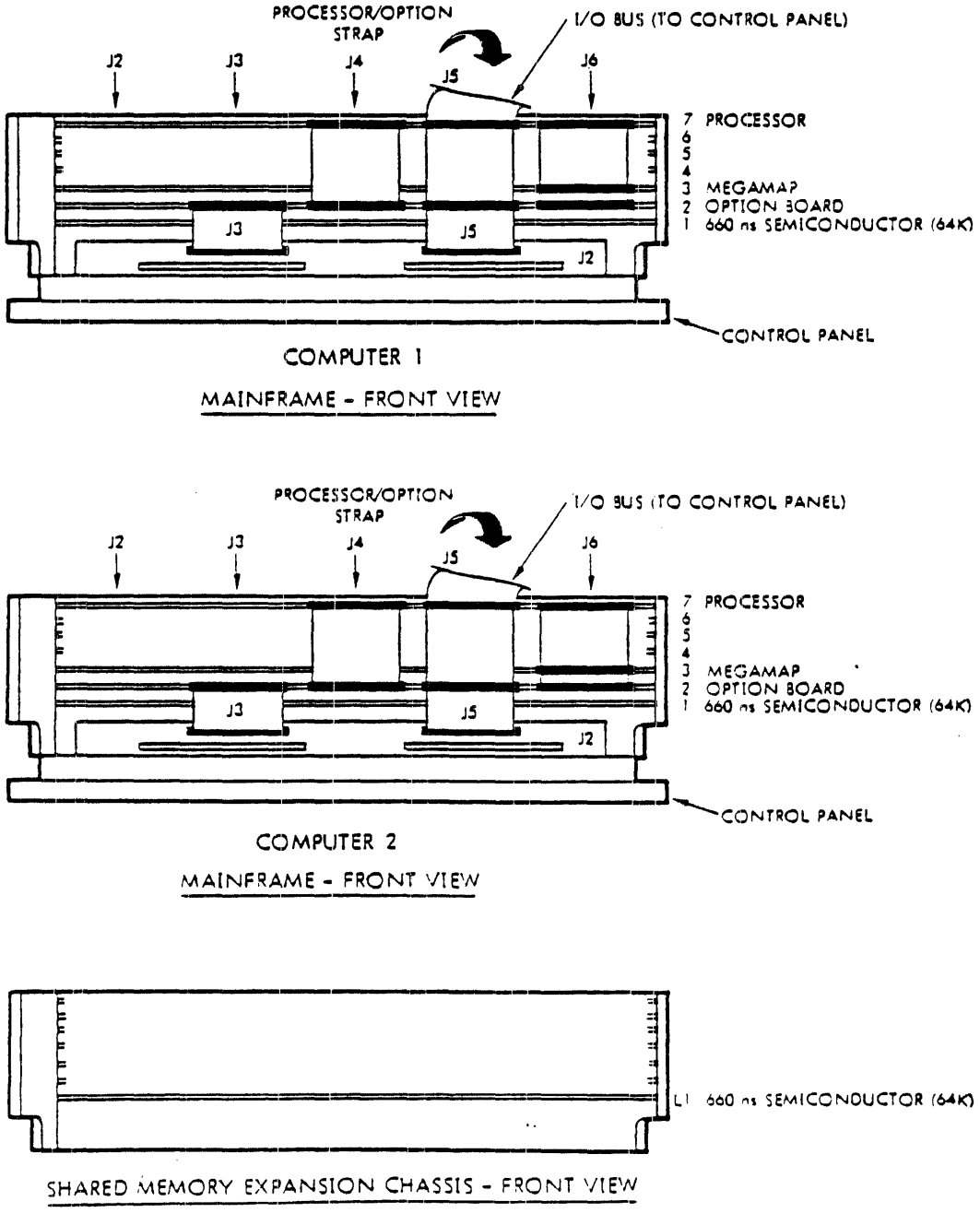
5.4 MULTIPLE COMPUTER/SHARED MEMORY CONFIGURATION

The multiple computer/shared memory configuration utilizes two or more basic or high performance computers and a shared memory system. Block diagram, figure 5-20, shows a typical configuration of the multiple computer/shared memory system; figure 5-21 shows the corresponding installation; and figure 5-22 illustrates corresponding cable connections.



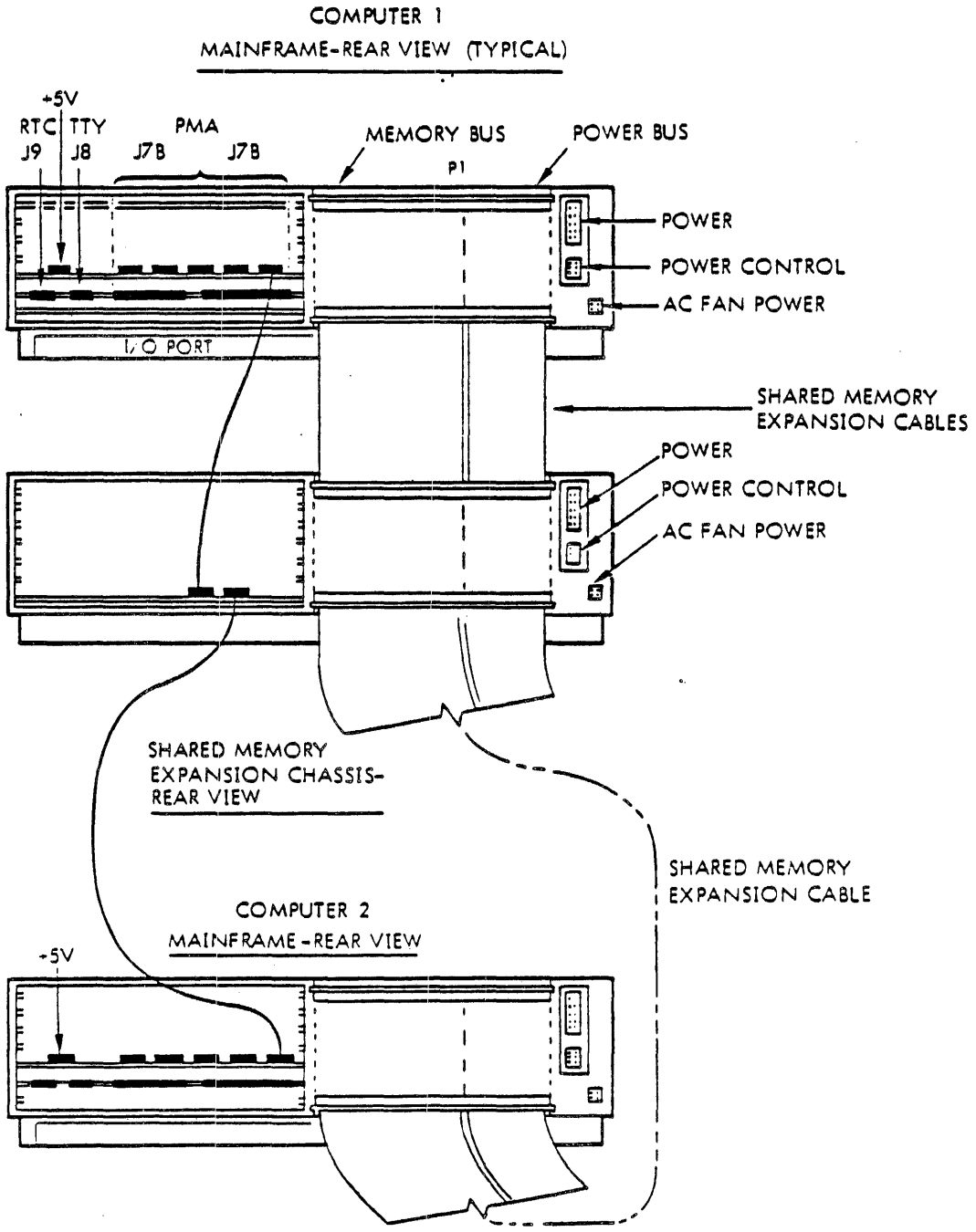
VTI1-3573A

Figure 5-20. Block Diagram of Typical Multiple Computer/Shared Memory Configuration



VTII-3574A

Figure 5-21. Typical Multiple Computer/Shared Memory Installation



VTI1-3575

Figure 5-22. Typical Multiple Computer/Shared Memory Cable Connections

SECTION 6
INSTALLATION

This section explains and illustrates the installation and interconnection of a V77-600 computer system.

6.1 UNPACKING

The computer system is packaged and shipped in several different containers. The computer mainframe is shipped in a single container with component boards mounted in respective slots of the mainframe chassis and held in place with a foam pad. The interconnecting cables are packaged separately for protection. When the I/O expansion cardframe chassis is packaged for shipment, it includes all connector-planes, connector terminators, cardguides, adaptor brackets, controller boards, and mounting hardware. In either case, the equipment is protected by resilient packing material and placed in a single container for shipment as a unit. This is also true for the system power supply, fan tray, and the electrical equipment cabinet. Peripherals including interconnecting cables are shipped as a complete package.

6.2 INSPECTION

After unpacking, inspect each system component for physical damage which may have been incurred during shipment. To ensure that component boards and other equipment installed in the mainframe or cardframe chassis have not been damaged, remove each board from the respective and check the following:

a. Component boards slide freely in and out of cardguides without jamming or binding

b. Connectors and plugs mate easily without binding

c. Connector terminals are clean and straight

d. Components on each board are in place and secure

e. Mounting hardware is in place and secure

f. All other equipment is in place and secure.

If damage exists or if equipment is missing:

a. Notify the transportation company

b. Notify Sperry Univac.

c. Save all packing material and shipping lists.

6.3 EXPANDED SYSTEM

The expanded V77-600 computer system can be installed in any type of stationary or mobile enclosure having adequate facilities for locating, operating, and maintaining system equipment. Cabinet installation of a typical expanded system is shown in figure 6-1. In this illustration, the control panel is folded down to show the computer interior. Refer to section 2 for environmental standards and power requirements.

6.4 BASIC SYSTEM

The basic V77-600 computer system can be installed in a single mainframe chassis. Figure 6-2 shows a typical mainframe chassis installation with the computer control panel folded down. Cables that attach to the optional boards are supplied only if the option is ordered. Refer to section 2 for power distribution.

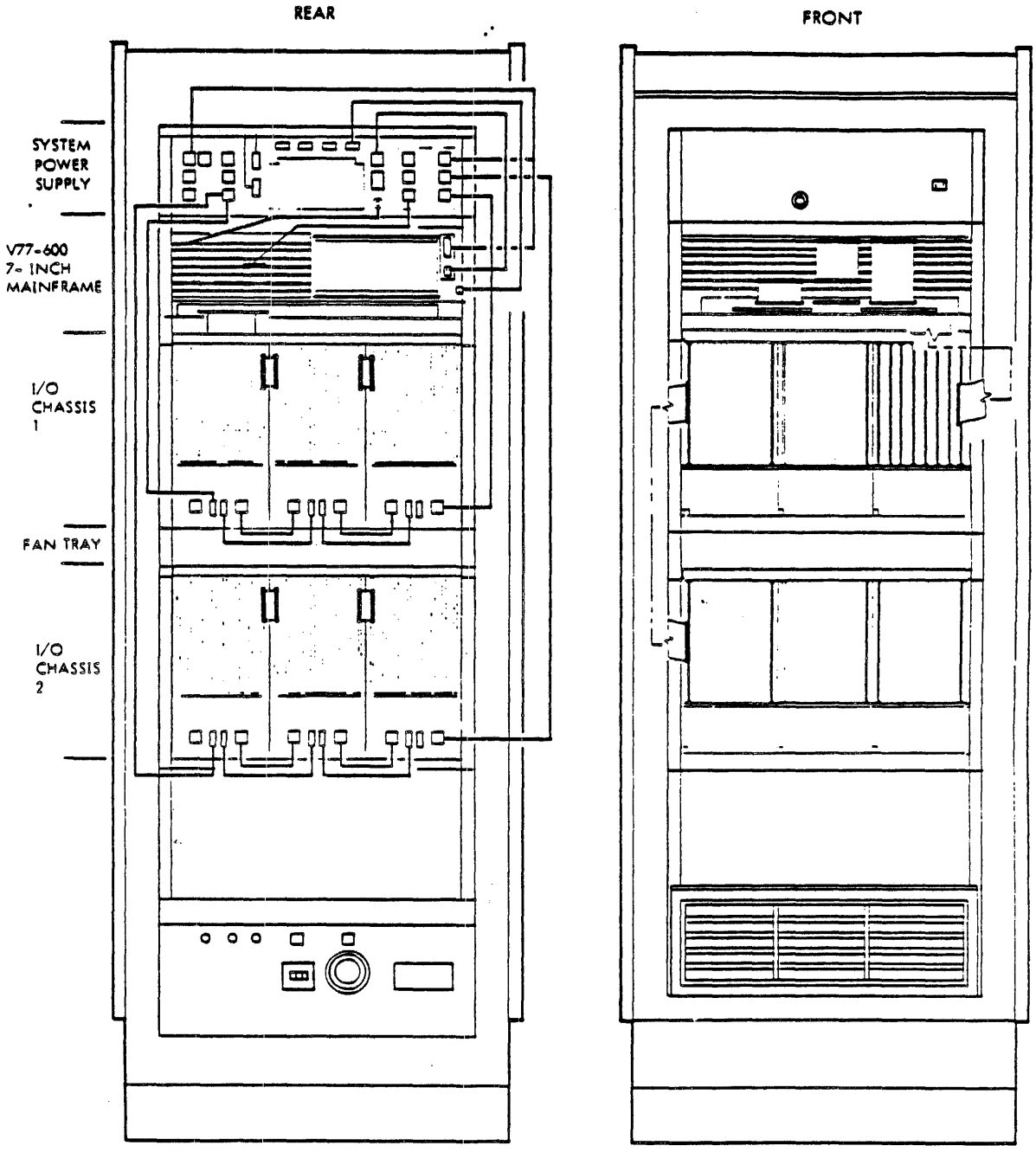
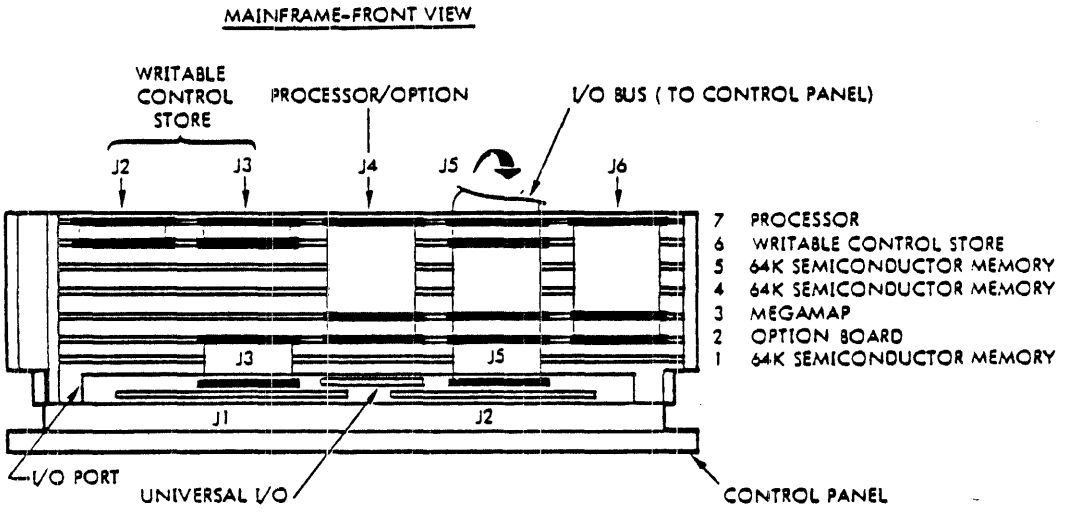
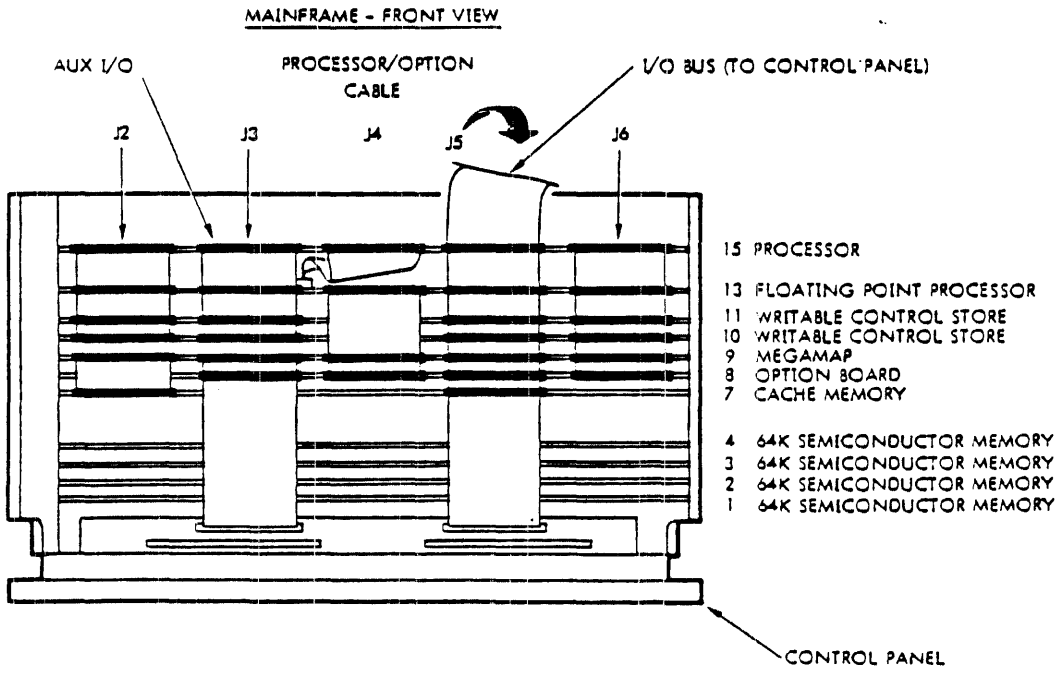


Figure 6-1. Typical Cabinet Installation



VTI1-3545A

Figure 6-2. Typical 7-Inch Mainframe Board Locations and Interconnections



VTI1-3543A

Figure 6-3. Typical 14-Inch Mainframe Interconnections

The next step is to mount the interconnecting cables as described in the following section.

6.5 INTERCONNECTION

Table 6-1 lists the interconnecting cable description, connector number, and number of pins in each connector.

6.6 POWER UP

After making sure all mainframe and peripheral device cables, connectors, system and power supply circuit breakers etc., are correctly mounted, plugged in and turned on (including peripheral devices powered on), turn power key on the control panel to the on position (reference section 2 for power distribution explanations and illustrations). In the on position, there is ac power to the power supply and both the system and console are fully operational with the STEP indicator illuminated, sense switches off, data display register cleared, display select on REG., and register select cleared.

If manually loading the bootstrap program, the console is ready as it is already in the STEP mode. For an automatic bootstrap load, press the STEP/RUN button to illuminate RUN indicator (blinks on-off). For the bootstrap program loading sequence, reference the step-by-step procedures in section 7.

Table 6-1. Typical System Cables and Connectors

Description	Connector	Pins
I/O bus connections: I/O Data Standard I/O control	J5	50
Expanded control store	J2, J3	50 each
Auxiliary I/O connector: Priority lines High Speed DMA Control	J3	50
Universal I/O connector: Additional priority lines BIC control signals I/O controller board interconnection (M.T., P.T., Disc, Drum, C.R., etc.)	J4	50
I/O Port:		
Printed-circuit mating connector	J2	122
Printed-circuit edge connector	J3, J4, J5	50 each
Power and memory bus etched card connects all seven slots (17 for 14 inch chassis)	P1	132
Device connectors to I/O controllers	J2	44
Priority Memory Access	J7A, J7B	40 each
Teletype controller	J8	
Real-Time Clock	J9	
Power supply control	J2	8
Power supply	J3	16
Ac fans in	J1	3
Memory (64K only):		
Printed-circuit edge connector	P1	132

(continued)

Table 6-1. Typical System Cables and Connectors *(continued)*

Megamap request port A connector	J1	4
Megamap request port B connector	J3	4
Error correction refresh request	J2	4
Megamap:		
Memory bank connectors	J8	12
	J9	12
	J10	12
	J11	12
	J12	12

SECTION 7
OPERATION

7.1 CONTROL PANEL

The V77-600 control panel (figure 7-1) contains all the switches and indicators needed for computer operation. Except for the POWER switch, which is key operated, all control panel switches are pushbutton type. The functions of the switches and indicators are described in the following paragraphs.

7.1.1 POWER Switch

The POWER switch is a key-operated, four-position switch that controls the ac line voltage to the computer power supply.

In the OFF position, ac line voltage is removed from the power supply.

In the ON position, the ac line voltage is applied to circuits of the power supply and dc voltages are generated for on-line operation.

In the HOLD position, the ac line voltage is applied to the power supply and all dc voltages are disabled except those required to maintain data in the semiconductor memory. In the HOLD condition, neither the computer nor the control panel are operational.

The CONSOLE DISABLE position is jumper selectable to operate in two modes:

a. All control-panel pushbutton switches are disabled.

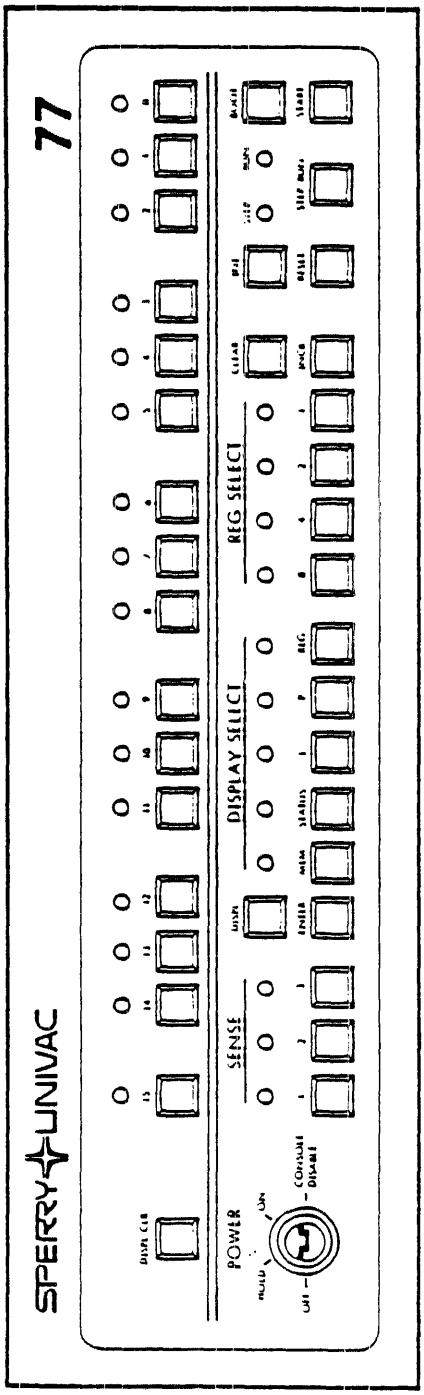
b. Only the STEP/RUN and RESET switches are disabled.

The jumper is factory installed on the control-panel circuit board. With the POWER switch in the CONSOLE DISABLE position, the ac line voltage is applied to the power supply, the computer is operational, and the control-panel indicator lights are functional. The key can be removed from the POWER switch in any of the four positions.

To turn off the computer from the CONSOLE DISABLE condition, turn the POWER switch ON, place the computer in the step mode (using STEP/RUN switch), and then turn the POWER switch to either the HOLD position (to maintain data in semiconductor memory) or the OFF position.

Note:

If a power-fail option is installed in the system, it is not necessary to place the STEP/RUN switch in the STEP position before turning the POWER switch to HOLD or OFF.



VT11-3619

Figure 7-1. V77-600 Control Panel

7.1.2 STEP/RUN Switch and STEP-RUN Indicators

The STEP/RUN switch is an alternate-action switch that switches the computer alternately to the step and run modes. In the step mode, the STEP indicator lights; in the run mode, the RUN indicator blinks on and off until the START switch is pressed at which time the RUN indicator is on continuously.

When the computer is in the step mode, pressing the STEP/RUN switch places the computer in the run mode. The STEP indicator goes out and the RUN indicator blinks on and off. When in the run mode, the computer is ready to be started (by pressing the START switch).

When the computer is in the run mode and has been started, pressing the STEP/RUN switch halts the computer after the current instruction has been executed and the next sequential instruction fetched and loaded into the I register; the RUN indicator goes out and the STEP indicator lights. In addition, a halt instruction (after the computer has been started) halts the computer and causes the RUN indicator to blink.

7.1.3 START Switch

When the computer is in the run mode but has not been started, pressing the START switch starts the program at the location specified by the contents of the program counter. The RUN indicator stops blinking and comes on continuously.

When the computer is in the step mode, pressing the START switch executes the instruction in the instruction register. Then it fetches the next instruction from the memory address specified by the contents of the program counter and loads it in the instruction register. The STEP indicator remains on.

7.1.4 LOAD Switch

The LOAD switch allows the program loader program to be loaded into the computer memory automatically. The loader program permits loadable programs to be loaded into main memory from a peripheral device. When the LOAD switch is pressed, the RUN indicator lights. Refer to the program execution portion of this section for loader program loading procedures.

7.1.5 Register-Entry Switches and Register-Display Indicators

The top row of control-panel lights comprise the 16 register-display indicators. They display the contents of the display register. This register, located on the control panel circuit board, can be loaded from the register-entry switches, located on the control panel just below the 16 indicators. In addition, 16-bit data words can be displayed by the register-display indicators under control of the DISPLAY SELECT and REG SELECT switches allowing the contents of the various register and memory locations to be visually examined.

The contents of the display register can be cleared (set to zero) by pressing the DISPL CLR switch. This turns off all sixteen display indicators. Any of the sixteen bits can be set by

pressing the corresponding register-entry switch. With a bit set, the corresponding display indicator lights. Pressing a register entry switch for a bit already set, has no effect. Bits can only be reset to zero by pressing the DISPL CLR switch. For negative data, the sign bit (bit 15) is set (one).

7.1.6 DISPL and ENTER Switches

The DISPL switch is used with the MEM switch for displaying memory data on the register-display indicators.

The ENTER switch is used with the MEM switch to load data into memory from the register-entry switches.

The procedures for displaying memory data and entering data into memory are described under manual operations (section 7.2).

7.1.7 DISPLAY SELECT Switches and Indicators

The five DISPLAY SELECT switches are used to select one of several registers for displaying its contents on the register display indicators and altering them from the register-entry switches. Pressing any DISPLAY SELECT switch cancels any previous selection, turns off the indicator for the previous selections, and lights the indicator for the new selection. The functions for each selector switch are described in the following paragraphs.

MEM switch: selects the memory for data entry or display. For entering data into memory and displaying the contents of memory refer to the manual operations portion of this section.

STATUS switch: selects the status of various signals from the processor. To display the status of these processor signals, perform the following:

a. Turn the POWER switch ON.

b. Place the computer in the step mode.

c. Press STATUS.

The register display indicators will then display the following:

Bit 15, Key register bit 15 (DCK15 +)
Bit 14, Key register bit 14 (DCK14 +)
Bit 13, Key register bit 13 (DCK13 +)
Bit 12, Key register bit 12 (DCK12 +)
Bit 11, Arithmetic and logic unit carry (DCNDC +)
Bit 10, Arithmetic and logic unit sign (DSGN +)
Bit 9, Arithmetic and logic unit output equals all ones (DEQ +)

Bit 8, Arithmetic and logic unit overflow (DOVF +)
Bit 7, Shift counter output bit 4 (DSC04 +)
Bit 6, Shift counter output bit 3 (DSC03 +)
Bit 5, Shift counter output bit 2 (DSC02 +)
Bit 4, Shift counter output bit 1 (DSC01 +)
Bit 3, Shift counter output bit 0 (DSC00 +)
Bit 2, Arithmetic and logic unit output zero (DCNOZ +)
Bit 1, Supervisor mode (CESK +)
Bit 0, Not used

I switch: selects the instruction (I) register for data display or entry. Pressing the I switch with the RUN indicator off or blinking (step mode or halted) displays the contents of the instruction register on the register display indicators. Changing the contents of the display register, by pressing the DISPLAY CLR switch and the register entry switches, automatically changes the contents of the instruction register. Except for a halt instruction, the instruction entered into the instruction register will be the next executed instruction. However, if the entered instruction is a halt instruction, the next executed instruction will be at a new address represented by the contents of the program counter.

P switch: selects the program (P) counter for data display or entry. Pressing the P switch with the RUN indicator off or blinking (step mode or halted) displays the contents of the program counter on the register display indicators. Changing the contents of the display register, by pressing the DISPLAY CLR and register entry switches, automatically changes the contents of the program counter. It should be noted that the contents of the I register determine the functional use of the contents of the program counter when the START switch is actuated. If the I register contains a halt instruction, the contents of the program counter at that address will be the new address of the first executed instruction. If the I register contains an instruction that is not a halt instructions, the contents of the program counter will be the address of the first executed instruction plus one address bit (address of next instruction).

REG switch: enables one of the registers designated by the REG SELECT switches to be selected for data display or entry.

7.1.8 REG SELECT Switches and Indicators

When the REG switch is pressed, any one of eight programming registers (R0 through R7) or any one of six registers used for WCS microprogramming can be selected for displaying its contents on the register display indciators or altering its contents from the register entry switches, as specified in table 7-1. The register selection is accomplished by entering a binary code using the four REG SELECT switches designated 8, 4, 2, 1. A one bit is produced by pressing the appropriate REG SELECT switch; a zero bit is produced by not pressing the switch. A one bit causes the corresponding indicator to light. The binary codes for specific

registers are listed in table 7-1. When the binary code has been entered, the register display indicators automatically display the contents of the selected register. Changing the contents of the display register, using the DISPLAY CLR and register entry switches, automatically changes the contents of the selected register.

The binary code for a selected register can be cleared (set to zero) by pressing the CLEAR switch. Each time the INCR switch is pressed, the binary code for a selected register is incremented by one allowing the subsequent register to be selected.

7.1.9 INT Switch

The INT switch is used to interrupt the computer and is functional only in the run mode (RUN indicator on). Pressing the INT switch, interrupts to memory address zero.

Table 7-1. Binary Codes for Register Selection

REG SELECT Switches				Selected Register
8	4	2	1	
0	0	0	0	R0 (A)
0	0	0	1	R1 (B)
0	0	1	0	R2 (X)
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0*	
1	0	0	1*	
1	0	1	0*	
1	0	1	1*	
1	1	0	0*	
1	1	0	1*	
1	1	1	0*	
1	1	1	1*	

* These codes select registers that are used for WCS microprogramming. With two exceptions the contents of these registers can be displayed and altered using the control panel; however, alteration from the control panel should be done only for maintenance purposes or special applications. The register selected with the binary code of 1000 always contains the contents of the instruction register. The registers selected with binary codes of 1011 and 1100 always contain all zeros and all ones, respectively; the contents of these two registers can not be altered from the control panel.

7.1.10 RESET Switch

Pressing the RESET switch:

a. Halts the computer

b. Stops I/O operation

c. Initializes both the computer and its peripheral devices

d. Leaves the computer in the step mode

e. Turns the RUN indicator off and the STEP indicator on, if the preceeding computer mode was the run mode

f. Resets the overflow indicator (bit-8 register display indicator, with STATUS switch pressed)

7.1.11 SENSE Switches and Indicators

The three SENSE switches permit the execution of predetermined program branching by the operator. When the program contains jump, jump-and-mark, or execution instructions that depend upon the setting of the SENSE switches, the jumps and executions occur only if the switch conditions are met.

Pressing a SENSE switch sets it and causes its associated indicator to light. Pressing the same switch again resets it, causing its indicator to go out.

EXAMPLE

A program can be written so that the operator can obtain a partial total of a column of figures being added by use of the JSS1 (jump if SENSE switch 1 is set) instruction. The program writes individual entries as long as SENSE switch 1 is not set. When the operator wants a partial total, he sets the switch. The program then jumps to an instruction sequence that prints the desired information.

7.2 MANUAL OPERATIONS

Using the control panel switches, data or instructions can be manually transferred to or from memory or a selected register, and stored programs can be manually executed.

Manual execution of a stored program is discussed in section 7.3.

7.2.1 Displaying Register Contents

To display the contents of the instruction register:

a. Place the computer in step mode.

b. Press I.

To display the contents of the program counter:

a. Place the computer in step mode.

b. Press P.

To display the contents of the remaining registers shown in table 7-1:

a. Place the computer in step mode.

b. Press REG G.

c. Using the four REG SELECT switches, enter the appropriate binary code as shown in table 7-1.

7.2.2 Entering Data Into a Register

To enter data or instructions into a register:

a. Display the contents of the selected register as described in the preceding paragraphs.

b. Using the DISPLAY CLR and register-entry switches, enter the desired data or instruction into the selected register.

7.2.3 Displaying Memory Contents

To display the contents of a memory address:

a. Place the computer in step mode.

b. Press P.

c. Using the DISPL CLR and register-entry switches, enter the desired memory address into the program counter.

d. Press MEM.

e. Press DISPL. The contents of the selected memory address are now displayed on the register-display indicators. The program counter is automatically incremented.

f. Repeated actuation of the DISPL switch displays the contents of consecutive memory addresses.

7.2.4 Entering Data Into Memory

To enter data into memory:

a. Place the computer in the step mode.

b. Press P.

c. Using the DISPL CLR and register-entry switches, enter the desired memory address into the program counter.

d. Press MEM.

e. Using the DISPL CLR and register-entry switches, enter the desired data into the register.

f. Press ENTER to load the desired data into the previously addressed memory location. The program counter is automatically incremented.

g. Repeat steps e and f to enter data into consecutive memory addresses.

7.2.5 Executing a Stored Program

To execute a stored program manually:

a. Place the computer in step mode.

b. Press P.

c. Using the DISPL CLR and register-entry switches, enter the address of the first program instruction into the program counter.

d. Press I.

e. Press DISPL CLR to clear the instruction register.

f. Press START. This loads the instruction specified by the program counter into the instruction register.

g. Press START again. This executes the instruction and loads the next program instruction into the instruction register.

h. Repeat step g once for each instruction in the program.

7.2.6 Overflow Indication

To observe the overflow indication:

a. Place the computer in step mode.

b. Press STATUS.

c. Observe the bit-8 register display indicator. If the indicator is on, an overflow condition exists; if it is off, overflow does not exist.

7.3 PROGRAM EXECUTION

To make a cold start (i.e., when a new system is being initialized or the contents of memory are unknown), the following operations are required:

a. Turn power on.

b. Load the program loader

c. Load the binary load/dump program.

d. Load the object program.

Descriptions of power turn on and program loader loading (automatic and manual) are provided in this section. The Utility Programs Manual provides descriptions for loading the binary load/dump and object programs.

7.3.1 Power On

Turn on computer power by placing the POWER switch to ON. When power is initially applied the following conditions will occur:

a. Step mode (STEP indicator on).

b. Sense switches not set (SENSE indicators off).

c. Register cleared (register display indicators off).

d. P switch on (P indicator on).

e. REG SELECT switches off (REG SELECT indicators off).

When power is removed and reapplied without actuation of the POWER switch (by loss and recovery of the ac line voltage), the same conditions apply, except the computer will be in the run mode (RUN indicator on) instead of the step mode.

7.3.2 Loading the Program Loader

The program loader permits loadable programs to be loaded into main memory from a peripheral device. It is a program contained in programmable read only memory (PROM) located in the processor. By using the computer control panel, the operator can automatically load the program loader into main memory which in turn transfers the object program from the peripheral device to main memory. Standard program loader routines are included for four devices: Teletype paper tape reader, high-speed reader, high-speed paper tape reader, model 70-755X disc memory, and model 70-760X/70-761X disc memory. The disc versions of the program loader are primarily used for the automatic program loading in a VORTEX operating system. The paper tape versions of the program loader are primarily used for the automatic loading of the binary load/dump program which is required for certain stand-alone programs contained on paper tape. Refer to the V70 Utility Programs

Manual for manual loading procedures and a description of the binary load/dump program. Loading procedures for specific software (VORTEX, FORTRAN IV, V70 Assembler, etc.), are described in corresponding V70 software manuals.

For reference purposes, the addresses and instruction codes for the automatic program loaders are listed in table 7-2 and 7-3.

The desired program loader routine is selected by loading the appropriate program loader code into register R0. The selection codes (in octal) are:

a. Teletype paper tape reader 000000

b. High-speed paper tape reader 000001

c. 70-760X/70-761X disc memory 000002

d. 70-755X disc memory 000003

If the binary load/dump program is to be used, insert the binary load/dump tape into the paper tape reader with the first binary frame at the reading station.

To load the program loader, perform the following steps:

a. With the POWER switch in the ON position, place the computer in the step mode (STEP indicator on).

b. Press REG.

c. Using the four REG SELECT switches, enter the binary code for register R0 (0000).

d. Using the DISPL CLR and register-entry switches, enter the desired bootstrap selection code into register R0.

e. Place the computer in the run mode by pressing the STEP/RUN switch (RUN indicator blinking).

f. Press LOAD (RUN indicator is now on). This loads the bootstrap program and object program into main memory.

Table 7-2. Automatic Program Loaders for High-Speed and Teletype Readers

Address	Instruction Code	Symbolic Coding		
000200	102637* (102601)	READ	CIB	RDR
000201	004011		ASLB	NBIT
000202	004041		LRLB	1
000203	004446		LLRL	6
000204	001020		JBZ	SEL

(continued)

Table 7-2. Automatic Program Loaders for High-Speed and Teletype Readers *(continued)*

Address	Instruction Code	Symbolic Coding		
000205	000214	(Memory address)		
000206	055000		STA	0,1
000207	001010		JAZ	LHLT + 1
000200	007000	(Memory address)		
000211	0005144		IXR	
000212	0005101	ENTR	INCR	1
000213	100537* (102601)		SEL	RDON
000214	101537* (101201)	SEL	EXC	IBFR,READ
000215	000200	(Memory address)		
000216	001000		JMP	*2
000217	000214	(Memory address)		

* When using the Teletype reader, replace this code with the one in parentheses.

Table 7-3. Automatic Program Loader for Disc Memory (Model 70-760X/70-761X)

Address	Instruction Code	Symbolic Coding			
001130	100416	A	EXC	0416	Initialize disc controller
001131	104016		EXC	016	Select disc drive 0
001132	100216		EXC	216	Set disc controller to seek mode
001133	005001		TZA		Clears A register
001134	103116		OAR	016	Seek track 0
001135	101016	B	SEN	016, C	Sense completion of seek
001136	001141				Address
001137	001000		JMP	B	Wait until ready
001140	001135				Address
001141	102516	C	CIA	016	Input status
001142	151167		ANA	01167	Mask out status
001143	001016		JANZ	A	Start over if error exists
001144	001130				Address
001145	100021		EXC	021	Initialize BIC
001146	100316		EXC	0316	Set disc controller to sector selector mode
001147	005102		INCR	02	Add 1 to B register
001150	103216		OBR	016	Select sector 1
001151	103120		OAR	020	Load initial BIC address
001152	006010		LDAI	01130	Load A register immediate
001153	001130				Operand
001154	103121		OAR	021	Load final BIC address
001155	100020		EXC	020	Activate BIC
001156	100016		EXC	016	Select read mode and select BIC
001157	101416	D	SEN	0416, D	Sense disc controller busy

(continued)

Table 7-3. Automatic Program Loader for Disc Memory (Model 70-760X/70-761X) *(continued)*

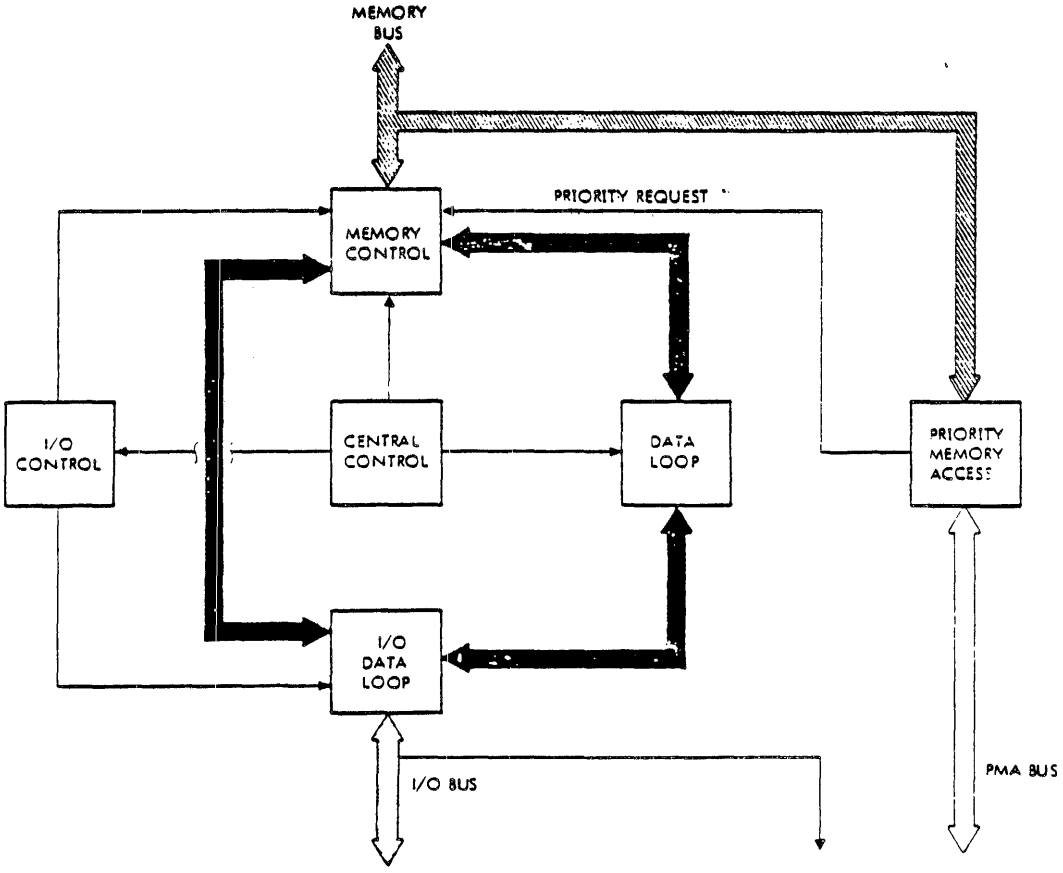
Address	Instruction Code	Symbolic Coding		
001160	001157			Address
001161	102516	CIA	0516	Input status
001162	151167	ANA	01167	Mask out status
001163	001016	JANZ	A	Start over if an error exists
001164	001130			Address
001165	010000	JMP	0600	Execute at initial VORTEX address
001166	000600			Address
001167	007760	Data	07760	Status mask

SECTION 8
INPUT/OUTPUT SYSTEM

8.1 GENERAL DESCRIPTION

The V77-600 input/output (I/O) system allows the computer to communicate with a variety of peripheral devices. The system is composed of computer I/O circuits, peripheral interface (controllers), and peripheral devices. Computer I/O circuits are on the processor and option boards in the mainframe. Each controller is contained on one or more controllers boards which plug into slots in the I/O expansion chassis. One controller can control one or more similar peripheral devices.

The I/O system provides data transfer paths between the computer and peripheral equipment. There are two major sections in the system: the I/O bus and the priority memory access. Figure 8-1 illustrates the general system organization and shows the various paths over which data is transferred.



VTI1-3228A

Figure 8-1. I/O System Organization

8.1.1 I/O Bus System

The I/O bus system contains the following principal elements:

- Timing, control, and internal bus interface in the processor.
- Various peripheral controllers.
- A party-line, time-shared I/O bus connecting the processor and controllers.

The I/O bus has two data paths, both through the memory control in the processor. Data can be transferred between memory and controllers through the registers in the data loop by program controlled I/O or interrupt initiated I/O. The direct memory access (DMA), utilizing trap-initiated I/O, bypasses the processor data loop and transfers data through the I/O data loop and memory control.

8.1.2 Priority Memory Access

The priority memory access (PMA) option provides I/O control and memory control functions to interface four data transfer channels with memory in a hardware-fixed priority scheme. The PMA can interface with up to eight PMA controllers distributed in any manner among the four channels; however, only one controller per channel can be active at a time. Data is transferred between memory and the controllers through the PMA option.

8.2 SYSTEM PRIORITY

A typical system priority structure is shown in figure 8-2 and includes both memory access priority and I/O control priority. Three priority levels are established for access to main memory:

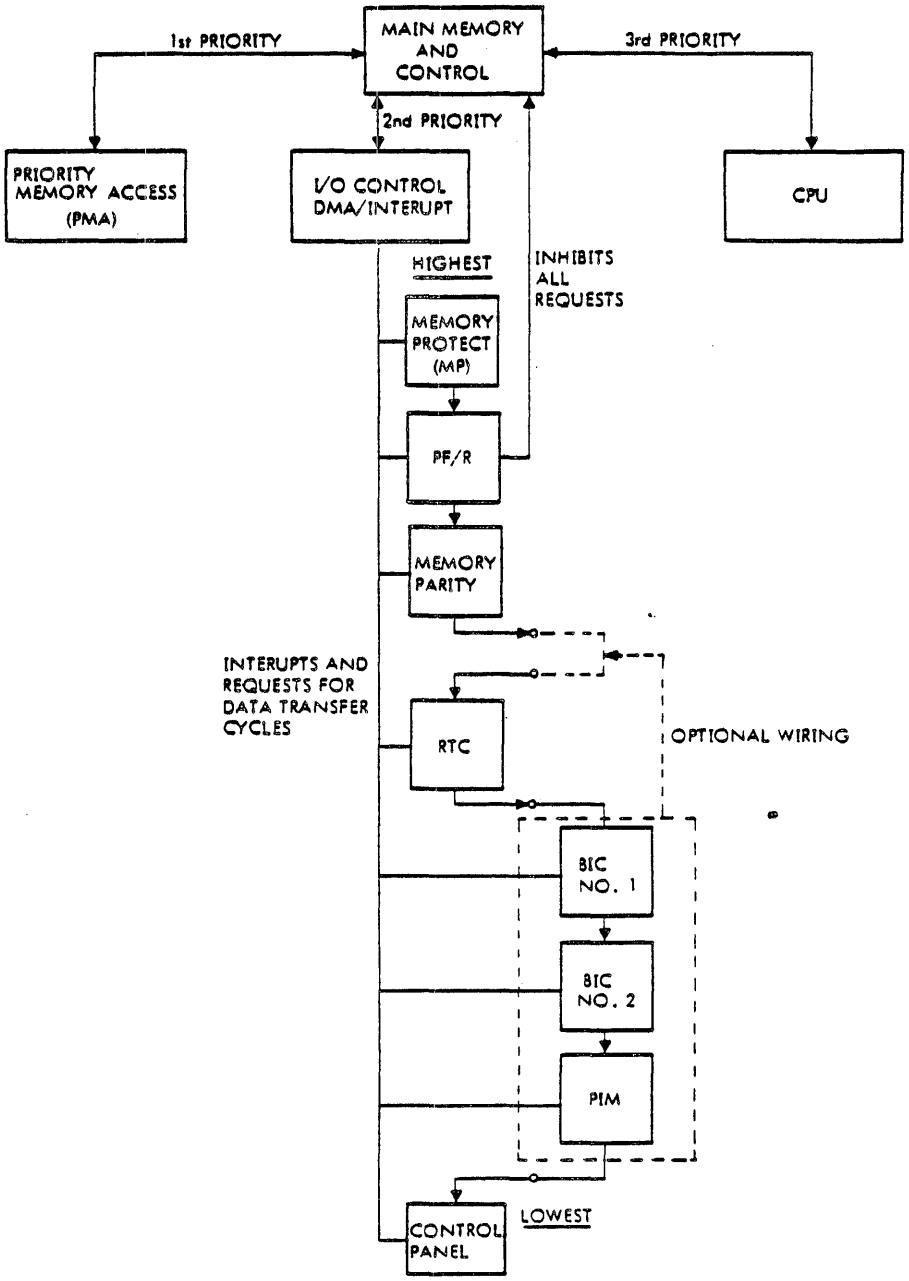
- Priority memory access has the first priority, except for power fail/restarts (PFR).
- I/O control has the second priority.
- Processor has the third and lowest priority.

Within the I/O control priority chain, the highest DMA/interrupt priority is given to memory protect (MP), followed by power fail/restart (PFR), memory parity, and the real-time clock (RTC). These option board features are followed by buffer interface controllers (BICs), priority interrupt modules (PIMs), and the control panel. As shown by the dotted lines in figure 8-2, the RTC, BICs, and PIMs may be placed in alternate priority order.

8.3 I/O BUS STRUCTURE

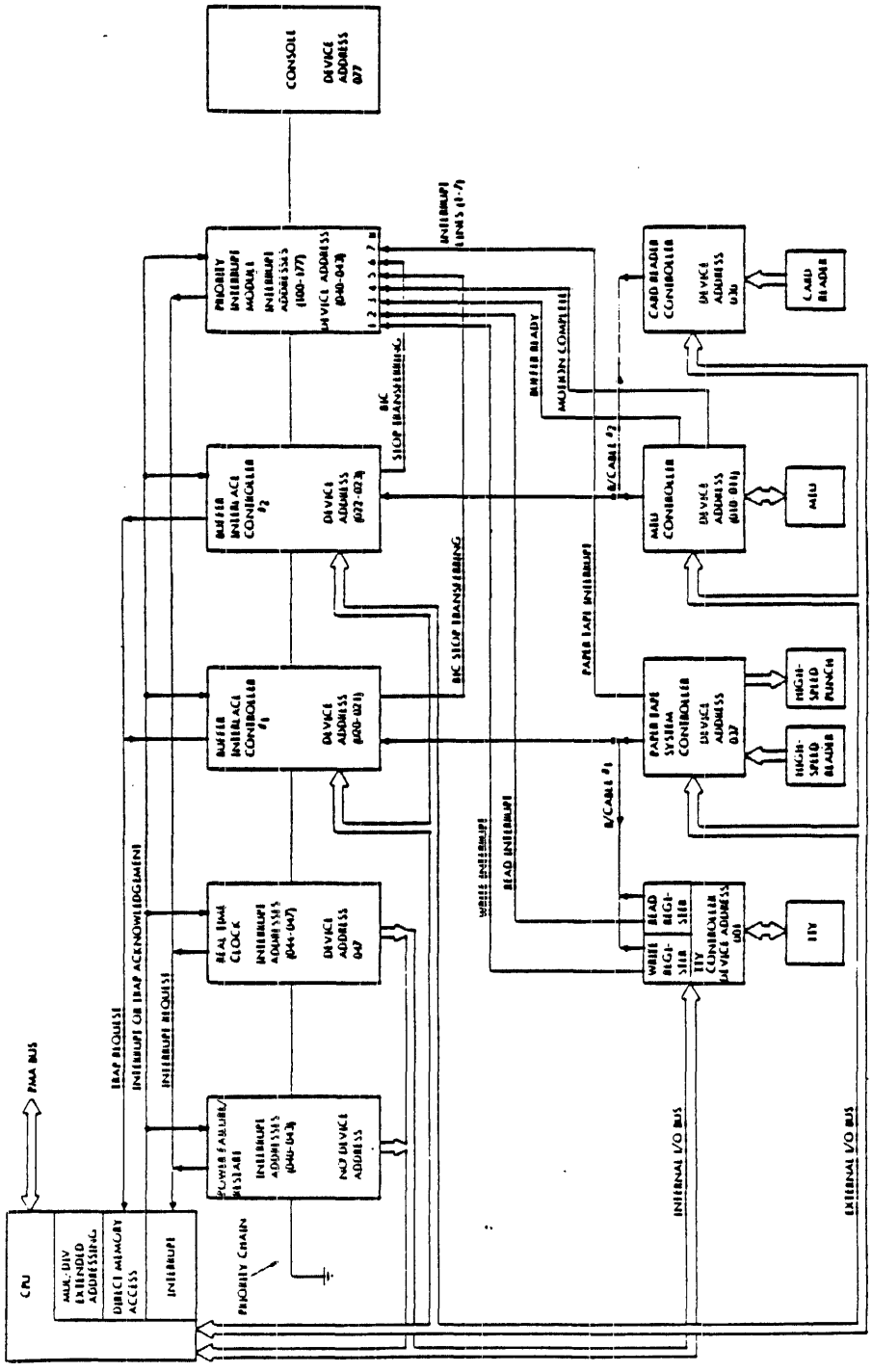
The I/O control system utilizes a bidirectional I/O bus which allows one set of data and control lines to communicate with all system peripherals. The organization of a typical I/O

system is illustrated in figure 8-3. All peripheral controllers and I/O options connect to the I/O bus.



VTI1-1480A

Figure 8-2. Typical System Priority



VTI3-0279A

Figure 8-3. Typical I/O System Block Diagram

NOTE: The I/O bus has two connections, one internal and one external. The option board, containing the first Teletype controller and various I/O options, is connected to the internal I/O bus. All other controllers are connected to the external I/O bus.

The data bus, priority chain, BIC control, interrupt request, trap request, and acknowledgement lines (shown in figure 8-3) are contained in the I/O bus cable. They are separated in the illustration for clarity. The interrupt lines to the PIM are separate entities, installed as needed during system installation or expansion.

8.3.1 Data Bus

A bidirectional 16-bit I/O data bus (EB00-I through EB15-I) is used to transmit I/O instructions, device addresses, and data from the computer to the peripheral devides. In turn, the data bus is used by the peripheral devices to transmit interrupt/trap addresses and data back to the computer.

A data bus signal is true when it is at 0 volts dc, and it is false when it is at +3 volts dc.

8.3.2 Control Lines

Individual lines carry control signals used during I/O instructions, interrupts, and DMA operations. The following signals are true at 0 volts dc and false at +3 volts dc:

FRYX-I: Function ready - This signal is generated by the computer to indicate that an I/O instruction and device address have been placed on the data bus. Each peripheral controller examines the device address and, upon a true-to-false transition of FRYX-I, the addressed peripheral responds to the I/O instruction.

DRYX-I: Data ready - This signal is generated by the computer to indicate that it has placed data on the data bus, or that is has accepted data placed on the data bus by the peripheral. The transfer of data occurs on the true-to-false transition of the signal.

IUAX-I: Interrupt acknowledge - This signal is generated by the computer to acknowledge the receipt of an interrupt, trap-in, or trap-out request. The interrupting or trapping peripheral controller can send an address to the computer and can transfer data to or from the computer when this signal is true. IUAX-I also inhibits device address decoding in all controllers during the address phase of an interrupt or trap operation to prevent the controllers from interpreting any part of the memory address as a device address.

SYRT-I: System reset - This signal is used to initialize all peripheral controllers connected to the I/O bus. It is true when the RESET switch on the control panel is pressed or when the power supply reset function is active.

SERX-I: Sense response - This signal is a controller response to a program sense instruction. During the execution of the instruction, the computer places a function code and a device address on the data bus. The addressed controller is instructed to indicate the status of a peripheral device action. If the status (sensed condition) is true, the controller responds by driving SERX-I true.

IUCX-I: Interrupt clock - This signal is an interrupt and trap synchronization clock from the comptuer. It is disabled when IUAX-I is true. The true-to-false transition of IUCX-I sets the interrupt or trap request flip-flop in the appropriate peripheral controller. IUCX-I is jumper selectable for one of two clock rates: 660 or 990 nanoseconds. The 990 nanosecond rate is standard.

IURX-I: Interrupt request - An interrupting peripheral controller (e.g., PIM) requests the computer to execute an instruction by driving this signal true. The address of the instruction is placed on the data bus when the computer acknowledges the interrupt request (IUAX-I).

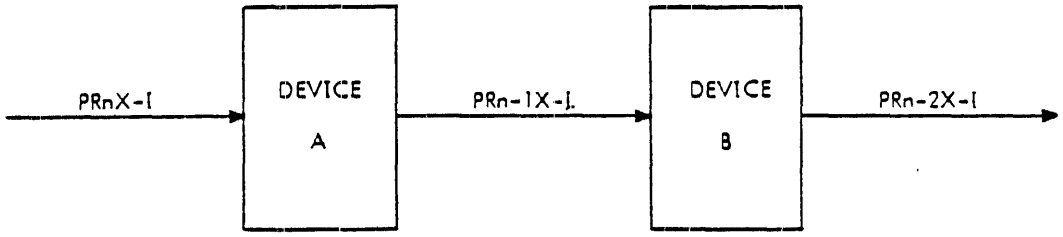
IUJX-I: Interrupt jump - This signal is generated by the computer to inhibit all interrupts following a jump-and-mark instruction when that instruction is executed at the interrupt memory location as the result of an interrupt request.

TPIX-I: Trap in - A trapping peripheral controller (e.g., BIC) drives TPIX-I true to request the computer to input one word of data to memory. The address is placed on the data bus by the controller when the computer acknowledges the request (IUAX-I).

TPOX-I: Trap out - A trapping peripheral controller (e.g., BIC) drives TPOX-I true to request the computer to output one word of data from memory. The address is placed on the data bus by the controller when the computer acknowledges the request (IUAX-I).

8.3.3 Priority Lines

Ten priority lines, PR1X-I through PR10X-I are located in the I/O bus cable. They are used to establish the priority of system interrupts and traps by connecting devices in a priority chain. Figure 8-4 shows two devices in the priority chain with device A having the higher priority. Before a device can generate an interrupt or trap request, the incoming priority signal must be true, indicating that any higher priority device is not generating an interrupt or trap request.



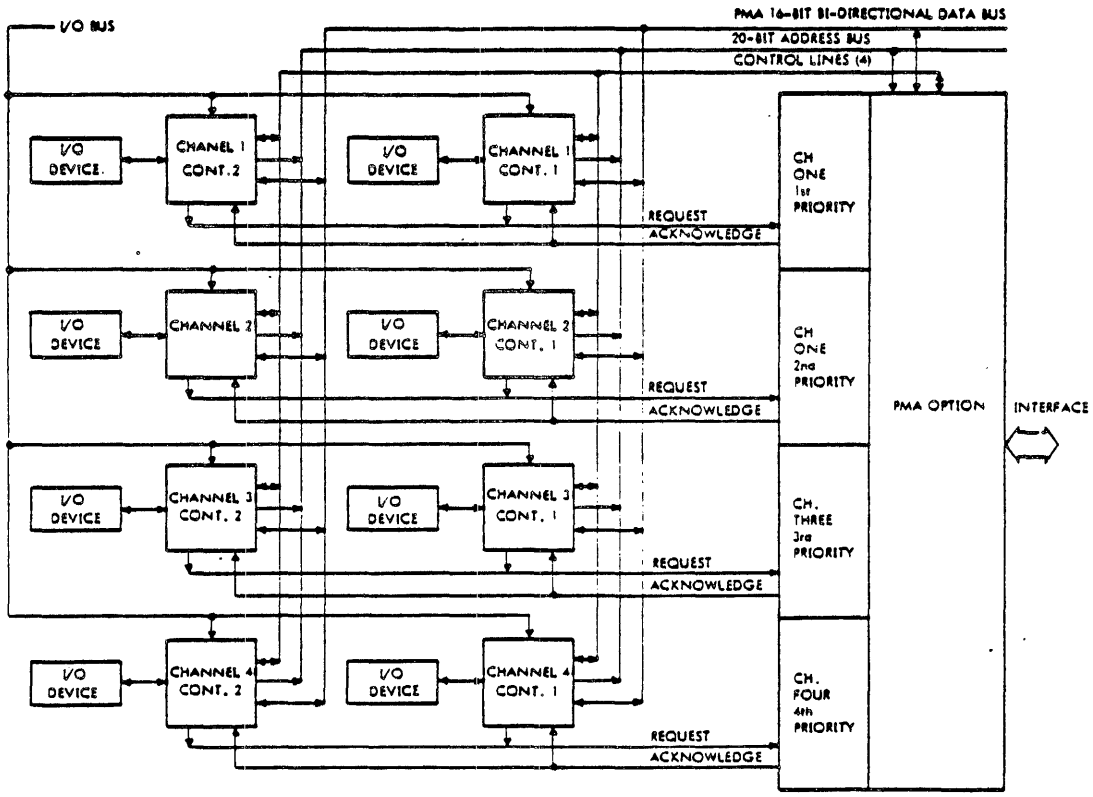
VTII-3682

Figure 8-4. I/O Priority Line Scheme

The devices that can be included in this chain are described in the system priority paragraph and shown in figure 8-2. The priority wiring is established when the system is installed; however, it may be modified as system requirements change.

8.4 PMA BUS STRUCTURE

The PMA option utilizes a bidirectional PMA bus which allows one set of data lines, one set of address lines, and control lines to communicate with all PMA controllers. The organization of a typical PMA bus system is shown in figure 8-5. All PMA controllers connect to this bus for data transfers. They also connect to the I/O bus for operation initiation.



VTI2-0378A

Figure 8-5. Typical PMA System

8.4.1 Data Bus

A bidirection 18-bit PMA data bus (PD00+ through PD17+) is used to transfer data between the PMA option on the option board and the PMA controllers. A data bus signal is true when it is at +3 volts dc, and it is false when it is at 0 volts dc.

8.4.2 Address Bus

A 20-bit address bus (PA00+ through PA19+) is used to transfer memory addresses from the PMA controllers to the PMA option. An address bus signal is true when it is a +3 volts dc, and it is false when it is at 0 volts dc.

8.4.3 Control Lines

Individual lines carry control signals used during PMA operations. The following signals are true at 0 volts dc and false at +3 volts dc:

REQn-: Request - This signal is generated by the PMA controller when it is ready to receive or transmit data. There are four request lines, one associated with each of the four data channels. Priority among the four requests is determined by the PMA option; REQ1- has the highest priority and REQ4- the lowest.

ACKn-: Acknowledge - This signal is generated by the PMA to acknowledge the request from the controller. It is driven true when the PMA has reserved the next memory cycle and received the acknowledge from the processor. There are four acknowledge lines; one associated with each of the four data channels. The trailing edge of this signal is also used to signal the end of a data transfer.

READ-: This signal is generated by the controller to indicate that the data transfer will be a PMA output transfer. When this signal is false, a PMA input transfer follows.

GO-: This signal is generated by the controller in response to the acknowledge signal and indicates that the memory address is on the bus and the controller is ready for the data transfer.

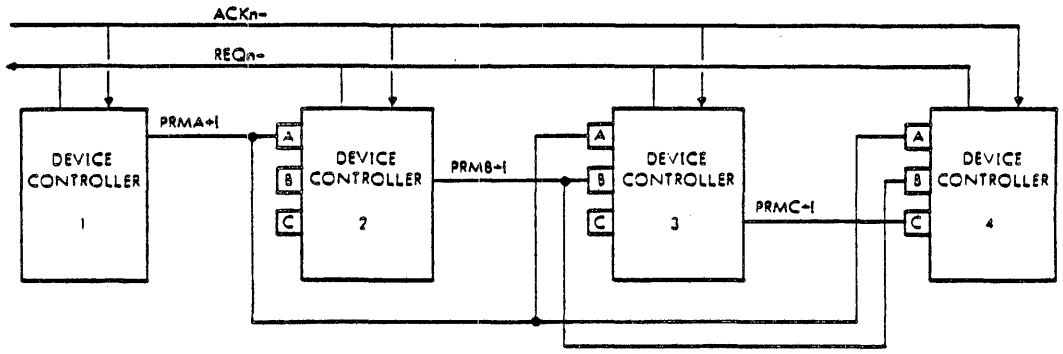
HOG-: This signal is generated by the controller to indicate that the controller is requesting successive memory access cycles.

PMRS-: PMA reset - This signal is generated by the controller to reset the PMA. The signal resets the request, memory, and data sequencer flip-flops of the PMA.

8.4.4 PMA Priority

Priority among the four PMA channels is determined by the PMA option. Channel 1 has the highest priority and channel 4 has the lowest. Requests are stored in the PMA and as each higher priority request is serviced lower priority device requests are honored.

Among PMA controllers attached to one PMA channel, priority is determined by controller interconnections, as shown in figure 8-6. The PMA priority lines PRMA + I through PRMC + I connect the controllers in a parallel priority chain. The output of each higher priority device is connected directly to the input of each lower priority device.



VTI1-3229A

Figure 8-6. PMA Priority Chain

8.5 INPUT/OUTPUT OPERATIONS

All input/output operations originate under the control of the stored program. Instructions containing function codes and addresses are transmitted to the appropriate devices. Subsequent data transfers can occur by program controlled I/O, interrupt-initiated I/O, direct memory access, or priority memory access.

8.5.1 Program Controlled I/O

There are four types of input/output instructions used for program controlled I/O:

- External Control: An external control code, specifying a peripheral function and device address, is transmitted from the computer to a peripheral controller.
- Program Sense: The status of a selected peripheral controller sense line is interrogated by the computer.
- Input Data Transfer: One word of data is transferred from a peripheral controller to the A register, B register, or a location in memory.
- Output Data Transfer: One word of data is transferred to a peripheral controller from the A register, B register, or a location in memory.

Under program control, the I/O system communicates directly with the peripherals. The computer can initiate peripheral operations by transmitting an external control function code and device address to the selected controller via the I/O bus. The computer can determine when a peripheral is ready for a data transfer by interrogating the associated sense line. A peripheral can be requested to place a word of data on the I/O bus during a computer input data transfer, or to accept a word of data placed on the bus by the computer during an output data transfer.

Only part of an I/O instruction is transmitted intact over the data bus. The device address (bits 0 through 5) are transmitted unchanged in all four instruction types. The function code (bits 6 through 8) is transmitted unchanged with external control and sense instructions. Bits 9 through 15 are decoded in the processor so that one of the lines EB11-I through EB15-I is true to identify the specific operation. These lines indicate:

EB11-I:	External control command
EB12-I:	Sense command
EB13-I:	Data input
EB14-I:	Data output
EB15-I:	Extended external control command

Table 8-1 summaries the signals transmitted over the data bus and control lines. Figures 8-7 through 8-10 show the timing for the program controlled operations.

8.5.2 Interrupt Initiated I/O

The computer I/O system includes an interrupt capability by which certain devices and options, on a priority basis, can request the computer to execute an instruction or series of instructions independently of the program in progress. The external interrupt system is implemented by the use of the priority interrupt module (PIM).

The PIM provides for the orderly servicing of peripheral-initiated interrupts. It does so by:

- Establishing up to eight levels of interrupt priority for selected peripheral controllers.
- Storing interrupt requests originated by associated peripheral controllers and placing the requests in the order of the established priority.

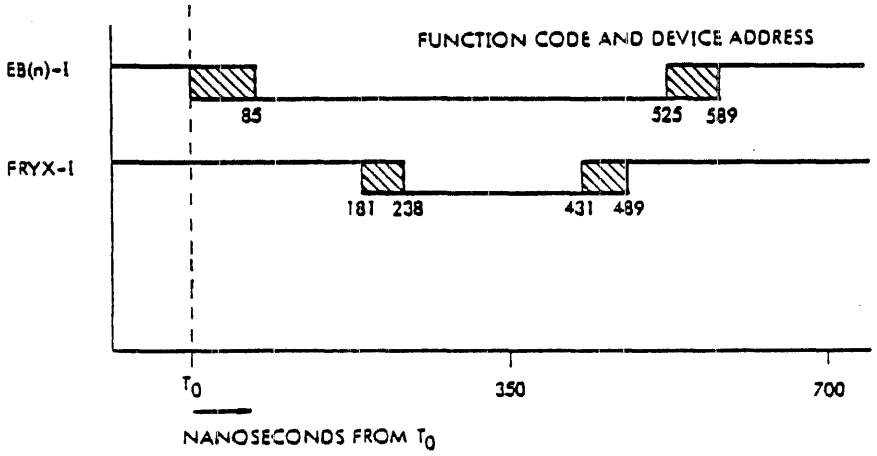
A peripheral controller connected to a PIM directs an interrupt request to the PIM which determines priority and sets IURX-I true. The PIM waits for the computer to acknowledge the request (IUAX-I true) and then places the appropriate interrupt address on the I/O bus.

Table 8-1. Data Bus and I/O Control Signals

OPERATION	External Control	Sense	Data Transfer		Trapping Sequence		Interrupt Sequence
CONTROL LINE	FRYX-I* (Phase 1)	FRYX-I* SERX-I* (Phase 1)	FRYX-I* (Phase 1)	DRYX-I (Phase 2)	TPOF-I, TPOX-I or TPIX-I IUAF-I, IUAX-I, FRYF-I, FRYX-I, (Phase 1)	TPIF-I, IUAF-I, IUAX-I, DRYF-I, DRYX-I (Phase 2)	IURX-I IUAX-I (Phase 1)
DATA LINE EB00-I	Device address	Device address	Device address	Data	Address	Data	Pairs of signals used for specific interrupts
EB01-I							
EB02-I							
EB03-I							
EB04-I							
EB05-I							
EB06-I	Function code	Function code	Not used				
EB07-I							
EB08-I							
EB09-I	Not used	Not used					
EB10-I							
EB11-I	External control command	Zero	Zeros				
EB12-I	Zeros	Sense command					
EB13-I		Zeros	Data in				
EB14-I			Data out				
EB15-I	See note 3		Zero				

NOTES:
1. Phase 1 is device or memory selection.
2. Phase 2 is the data transmission.
3. For extended external control, and data lines are the same as external control except EB11-I is zero and EB15-I is one.

* IUAX interlock; used in address decoding.



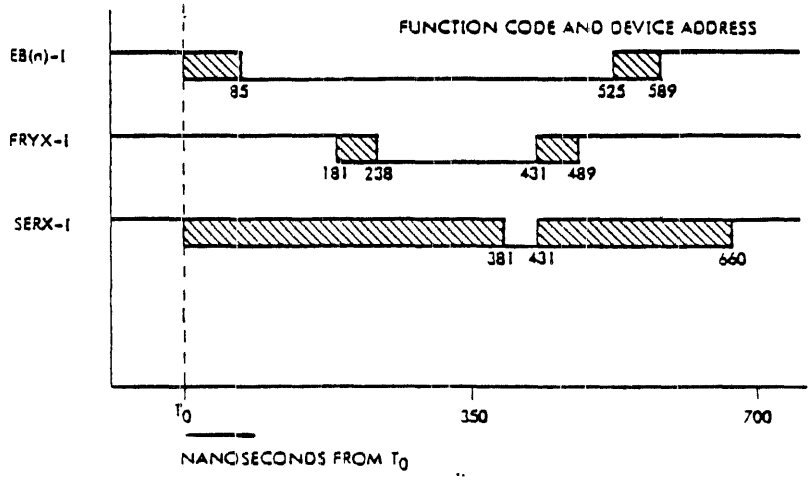
T_0 is the start of the execute phase of the external control instruction.

Logic levels: true = 0V dc,
false = +3V dc.

▨ = time when signal is settling.

VTI1-1506

Figure 8-7. External Control Timing



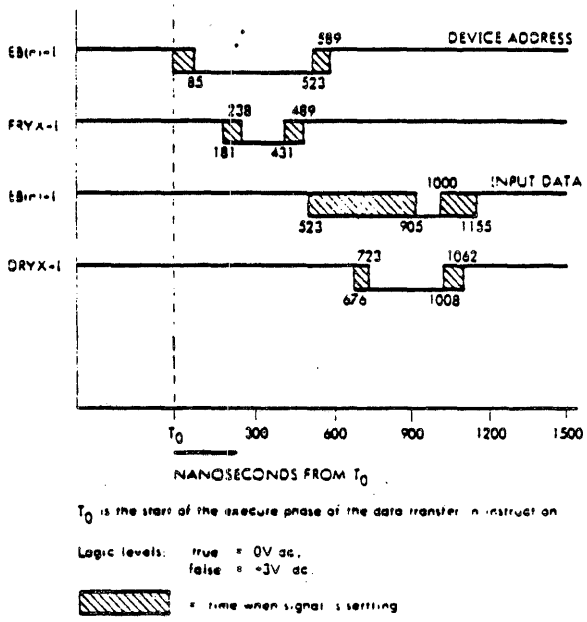
T_0 is the start of the execute phase of the sense instruction.

Logic levels: true = 0V dc,
false = +3V dc.

▨ = time when signal is settling.

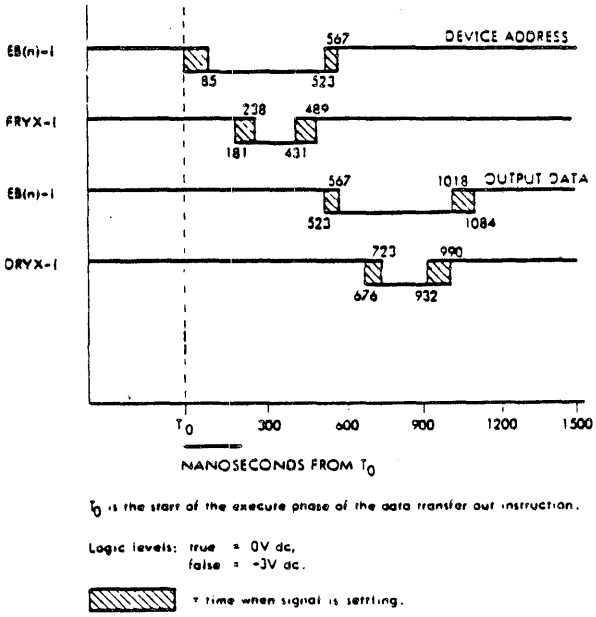
VTI1-1507

Figure 8-8. Sense Response Timing



VTI1-1508A

Figure 8-9. Data Transfer-In Timing

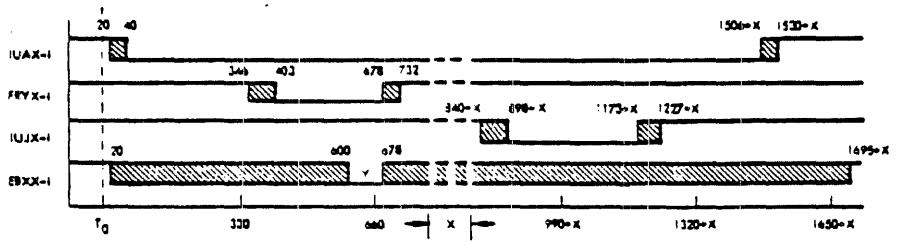


VTI1-1509

Figure 8-10. Data Transfer-Out Timing

The computer is directed to a memory location by the interrupt and executes the instruction at that address. The instruction at that address is normally a jump-and-mark instruction that results in the processing of an I/O service subroutine. At the conclusion of the interrupt subroutine, the computer returns to the original program through an appropriate jump instruction.

Figure 8-11 shows a typical timing sequence for an interrupt. Table 8-2 lists the standard interrupt addresses. Table 8-3 lists the instructions used with the PIM.



X = THE PROCESSOR TIME REQUIRED TO FETCH AND DECODE THE INSTRUCTION AT THE INTERRUPT LOCATION.

Y = INTERRUPT ADDRESS

VTII-2197A

Figure 8-11. Interrupt Timing

Table 8-2. Standard Interrupt Addresses

Address	Interrupt
020,021	memory protect halt error
022, 023	memory protect I/O error
024, 025	memory protect write error
026, 027	memory protect jump error
030, 031	memory protect overflow error
040, 041	power failure
042, 043	power restart
044, 045	real-time clock interval
046, 047	real-time clock overflow
100 · 117	PIM, first module
120 · 177	PIM, remaining modules

The parity interrupt address is configured by jumpers.

Table 8-3. PIM Instructions

Mnemonic	Octal Code	Description
	External Control	
EXC 014*	10014*	Clear interrupt registers
EXC 024*	10024*	Enable PIM
EXC 0244	100244	Enable all PIMs in system
EXC 034*	10034*	Clear interrupt registers and enable PIM
EXC 044*	10044*	Disable PIM
EXC 0444	100444	Disable all PIMs in system
EXC 054*	10054*	Clear interrupt registers and disable PIM
	Data Transfers	
OME 04*	10304*	Transfer contents of memory to mask register
OAR 04*	10314*	Transfer contents of A register to mask register
OBR 04*	10324*	Transfer contents of B register to mask register

* Represents the last octal digit of the device address

8.5.3 Direct Memory Access

The direct memory access (DMA) permits the transfer of blocks of data directly between the memory and peripheral controllers. Each data word transfer stops the processing of the stored program for one memory cycle to permit the DMA to access memory. In effect, the DMA "steals" one cycle from the processor. This mode of operation is also referred to as "trapping".

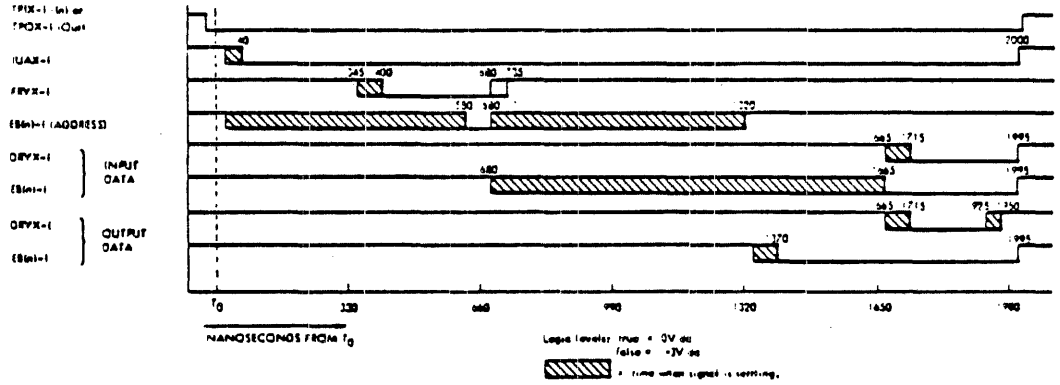
Operation of the DMA is implemented by the use of one or more (up to four) buffer interface controlers (BICs). Each BIC supports up to ten peripheral devices and provides the memory addresses necessary to access memory. Contained within the BIC are an initial address register, a final address register, a sequence controller, and drivers and receivers. When the Megamap option is used in conjunction with the BIC, an additional register is used in the BIC to store the key bits.

The DMA trapping operations are initiated by the stored program. The BIC service subroutine establishes the initial and final addresses for the transfer, identifies the peripheral controller, and initializes both the selected controller and the BIC.

When data is to be transferred, the peripheral controller requests the BIC to issue a trap request (TPIX-I or TPOX-I) to the processor. When the processor acknowledges the request (IUAX-I), the BIC places the initial memory address on the data bus and increments the initial address register by one. The DMA stops the processor, uses the memory address to access

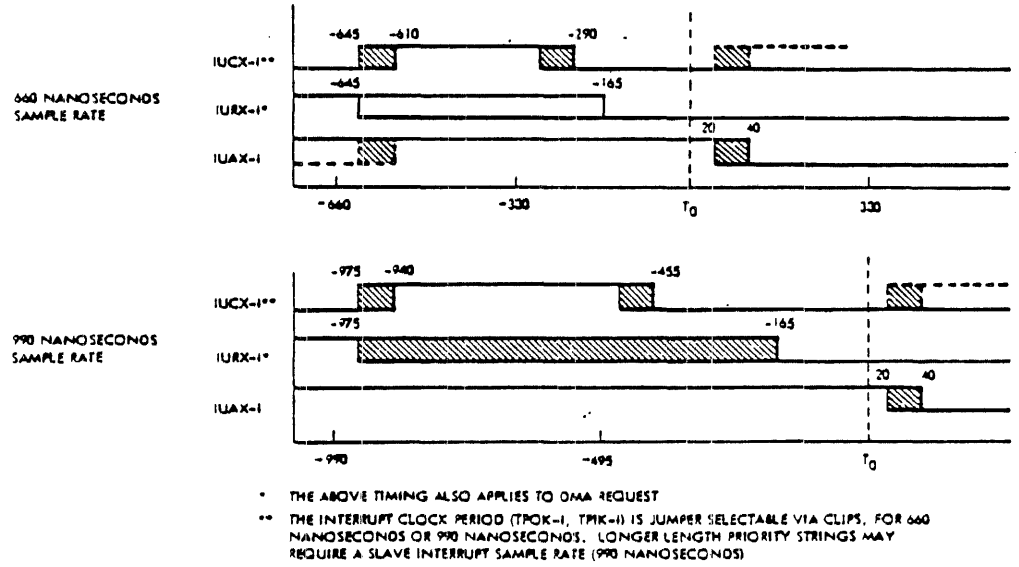
memory, and transfers data in or out. When the data word has been transferred, the processor is free to continue the stored program and the peripheral controller is free to generate a new trap request. This sequence is continued until the initial buffer contents equal the final buffer contents.

The BIC will perform DMA transfers at the peripheral device rate up to the maximum rate dependent on the memory access time, interrupt clock interval, and I/O control rate. Figure 8-12 shows the 620 compatible input and output timing. Figure 8-13 shows the DMA and interrupt timing.



VTII-2192

Figure 8-12. DMA Input and Output Timing



* THE ABOVE TIMING ALSO APPLIES TO DMA REQUEST

** THE INTERRUPT CLOCK PERIOD (TPOK-I, TPIK-I) IS JUMPER SELECTABLE VIA CLIPS. FOR 660 NANOSECONDS OR 990 NANOSECONDS. LONGER LENGTH PRIORITY STRINGS MAY REQUIRE A SLAVE INTERRUPT SAMPLE RATE (990 NANOSECONDS)

VTII-3162

Figure 8-13. DMA and Interrupt Request Timing

Table 8-4 lists the instructions used with the BTC.

Table 8-4. BIC Instructions

Mnemonic	Octal Code	Description
	External Control	
EXC 020	100020	Activate BIC
EXC 021	100021	Initialize
EXC 0321	100321	Enable loading of key bits
	Data Transfer	
OAR 020	103120	Load initial register from A
OBR 020	103220	Load initial register from B
OME 020	103020	Load initial register from memory
OAR 021	103121	Load final register from A
OBR 021	103221	Load final register from B
OME 021	103021	Load final register from memory
INA 020	102120	Read initial register into A
INB 020	102220	Read initial register into B
IME 020	102020	Read initial register into memory
CIA 020	102520	Read initial register into cleared A
CIB 020	102620	Read initial register into cleared B
	Program Sense	
SEN 020	101020	Sense BIC not busy
SEN 021	101021	Sense abnormal device stop
SEN 0121	101121	Senses if BIC has been stopped due to a memory map error

8.5.4 Priority Memory Access

The priority memory access (PMA) provides a direct data path between memory and high speed peripherals. Each data word transfer inhibits access to memory by the I/O control and the processor.

Operation of the PMA is implemented by the use of one or more block transfer controllers (BTCs). The BTC provides memory address control when data is organized into "blocks" of words. The BTC contains an initial address register, a final address register, a sequence controller, and drivers and receivers. It also has a key-bit register for use with the Megamap, and an odd-parity generator for use in systems with parity.

PMA operations are originated by program control. The BTC service subroutine establishes the initial and final addresses for the transfer, identifies the peripheral controller, and initializes both the selected peripheral and the BTC.

When data is to be transferred, the BTC issues a request to the PMA. The PMA determines priority and reserves the next memory cycle. When the PMA acknowledges the request, the BTC places the initial address on the PMA bus. The PMA gates the address through to the memory bus and the data transfer to or from memory is made.

The BTC increments the initial address register and data transfers continue until the initial address equals the final address.

Table 8-5 lists the instructions used with the BTC.

Table 8-5. BTC Instructions

Mnemonic	Octal Code	Description
	External Control	
EXC 002x	10002x	Activate BTC
EXC 002y	10002y	Initialize BTC
EXC 012x	10012x	Reset BTC
EXC 012y	10012y	Test data transfer
EXC 022x	10022x	Test input (writing) cycle
EXC 022y	10022y	Test output (reading) cycle
	Data Transfer	
OAR 02x	10312x	Load BTC initial-address register
OBR 02x	15322x	Load BTC initial-address register
OME 02x	10302x	Load BTC initial-address register
OAR 02y	10312y	Load BTC final-address register
OBR 02y	10322y	Load BTC final-address register
OME 02y	10302y	Load BTC final-address register
INA 02x	10212x	Read initial-address register
INB 02x	10222x	Read initial-address register
IME 02x	10202x	Read initial-address register
CIA 02x	10252x	Read initial-address register
CIB 02x	10262x	Read initial-address register
INA 02y	10212y	Read final-address register
INB 02y	10222y	Read final-address register
CIA 02y	10252y	Read final-address register
CIB 02y	10262y	Read final-address register
	Program Sense	
SEN 002x	10102x	Sense BTC not busy
SEN 002y	10102y	Sense abnormal device-stop
SEN 012x	10112x	Test sense-end-of-block

x is the last digit of the even address
y is the last digit of the odd device address (y = x + 1)

8.6 DEVICE ADDRESSES

Standard device addresses assigned to options and peripherals are listed in table 8-6 grouped according to their function (i.e., class).

Table 8-6. Standard Device Addresses

Class Code	Addresses	Option or Peripheral
00-07	01-07	Teletype or CRT device
010-017	010-013	Magnetic tape unit
	014	Fixed-head rotating memory
	015	Movable-head rotating memory
	016,017	Movable-head rotating memory
020-027	020,021	First BIC
	022,023	Second BIC
	024,025	Third BIC
	026,027	Fourth BIC
030-037	030	Card reader
	031	Card punch
	032	Digital plotter
	033	Electrostatic plotter
	034	Second paper tape system
	035,036	Line printer
	037	First paper tape system
040-047	040-043	PIM
	044	All PIM enable/disable
	045	MP
	046	Megamap
	047	RTC
050-047	050-053	Special applications, and Digital-to-analog converter
	056	Megamap alternate
	054-057	Analog system
060-067	060-067	Digital I/O controller Buffered I/O controller
070-077	070-073	Data communications system
	070-075	Writable control store
	074-076	Relay I/O controller Special applications
	077	Control panel

8.7 INTERFACE CONNECTIONS

The I/O system has two main interface cables over which data and control signals are transmitted. These cables are the I/O cable and the PMA cable. The I/O cable connects through the I/O port in the mainframe to the auxiliary I/O bus (J03) and the I/O bus (J05) documented in the configuration section of the manual. The PMA cable connects to J07A and J07B on the option board.

Tables 8-7 and 8-8 list the pin connections for the I/O cable at J03 and J05. Tables 8-9 and 8-10 list the pin connections for the PMA cable at J07A and J07B.

Table 8-7. Auxiliary I/O Bus Cable Connections - J03

J03 Pin	Mnemonic	J03 Pin	Mnemonic
1	Ground	2	Ground
3	IUB8-I	4	Ground
5	IUAA-I	6	Ground
7	SPFA-	8	Ground
9	PRIX-I	10	Ground
11	PR2X-I	12	Ground
13	PR3X-I	14	Ground
15	PR4X-I	16	Ground
17	PR5X-I	18	Ground
19	PR6X-I	20	Ground
21	PR7X-I	22	Ground
23	PR8X-I	24	Ground
25	PR9X-I	26	Ground
27	BTMES-I	28	Ground
29	IOK1-I	30	IOK2-I
31	IOK3-I	32	IOK4-I
33	Ground	34	BIMES-I

(continued)

Table 8-7. Auxiliary I/O Bus Cable Connections - J03 *(continued)*

J03 Pin	Mnemonic	J03 Pin	Mnemonic
35	Ground	36	Spare
37	Spare	38	Ground
39	TPOF-I	40	Ground
41	TPIF-I	42	Ground
43	IUCF-I	44	Ground
45	FRYF-I	46	Ground
47	IUAF-I	48	Ground
49	DRYF-I	50	Ground

Table 8-8. I/O Cable Pin Connections - J05

J05 Pin	Mnemonic	J05 Pin	Mnemonic
1	Ground	2	EB00-I
3	EB01-I	4	EB02-I
5	EB03-I	6	EB04-I
7	EB05-I	8	EB06-I
9	EB07-I	10	EB08-I
11	EB09-I	12	EB10-I
13	EB11-I	14	EB12-I
15	EB13-I	16	EB14-I
17	EB15-I	18	Ground
19	NSS2-	20	NSS1-
21	NSS3-	22	Ground

(continued)

Table 8-8. I/O Cable Pin Connections - J05 *(continued)*

J05 Pin	Mnemonic	J05 Pin	Mnemonic
23	IEIDLA +	24	Ground
25	NSTR-	26	Ground
27	OPSTRT-	28	Ground
29	PR10X-I	30	Ground
31	SERX-I	32	Ground
33	IURX-I	34	Ground
35	TPOX-I	36	Ground
37	TPIX-I	38	Ground
39	IUAX-I	40	Ground
41	FRYX-I	42	Ground
43	IUCX-I	44	Ground
45	SYRT-I	46	Ground
47	DRYX-I	48	Ground
49	IUJX-I	50	Ground

Table 8-9. PMA Cable Pin Connections - J07A

J07A Pin	Mnemonic	J07A Pin	Mnemonic
1	Ground	2	Ground
3	Ground	4	Ground
5	Spare	6	Ground
7	START-	8	Ground
9	GO-	10	Ground

(continued)

Table 8-9. PMA Cable Pin Connections - J07A *(continued)*

J07A Pin	Mnemonic	J07A Pin	Mnemonic
11	HOG-	12	Ground
13	PMRS-	14	Ground
15	ACK4-	16	Ground
17	ACK3-	18	Ground
19	ACK1-	20	Ground
21	ACK2-	22	Ground
23	REQ3-	24	Ground
25	READ-	26	Ground
27	Spare	28	Ground
29	REQ4-	30	Ground
31	Spare	32	Ground
33	SYRT-P	34	Ground
35	REQ1-	36	Ground
37	REQ2-	38	Ground
39	Spare	40	Ground

Table 8-10. PMA Pin Connections - J07B

J07B Pin	Mnemonic	J07B Pin	Mnemonic
1	Ground	2	PA00 +
3	PA01 +	4	PA02 +
5	PA03 +	6	PA04 +
7	PA05 +	8	PA06 +
9	PA07 +	10	PA08 +

(continued)

Table 8-10. PMA Pin Connections - J07B *(continued)*

J07B Pin	Mnemonic	J07B Pin	Mnemonic
11	PA09 +	12	PA10 +
13	PA11 +	14	PA12 +
15	PA13 +	16	PA14 +
17	PA15 +	18	PA16 +
19	PA17 +	20	PA18 +
21	PA19 +	22	PD00 +
23	PD01 +	24	PD02 +
25	PD04 +	26	PD04 +
27	PD05 +	28	PD06 +
29	PD07 +	30	PD08 +
31	PD09 +	32	PD10 +
33	PD11 +	34	PD12 +
35	PD13 +	36	PD14 +
37	PD15 +	38	PD16 +
39	PD17 +	40	Ground

8.8 I/O SYSTEM REFERENCES

Documentation supporting the I/O system is as follows:

- V70 Series Processor Manual, 98 A 9906 02x, describes the I/O control circuits, interrupt processing, and the DMA.
- V70 Series Option Board Manual, 98 A 9906 05x, describes the PMA.
- Priority Interrupt Module Manual, 98 A 9902 42x.
- Buffer Interface Controller Manual, 98 A 9902 01x.
- System Documentation (described in section 1.4) provides detailed information on a specific system.