


	C	B	A	
1	LOCAL CONTROL L01009	CONTROL #1 J0 L00014	JK CORE DATA 0-8 L01000	1
2		CONTROL #2 J0 L00013	J DATA REG 0-7 L00006	2
3	L01018.1 PARITY, MUATO, CORE SEL.	CONTROL #3 J L01005	K DATA REG 0-7 L00006	3
4		CONTROL #1 J1 L00014	INPUT SWITCH 0-7 L00002	4
5		CONTROL #2 J1 L00013	PORT DATA 0-8 L01003	5
6	CORE CONTROL JK L01002	CONTROL #1 K0 L00014	OUTPUT SWITCH 0-7 L00002	6
7		CONTROL #2 K0 L00013	L DATA REG 0-7 L00006	7
8		CONTROL #3 K L01005	M DATA REG 0-7 L00006	8
9		CONTROL #1 K1 L00014	LM CORE DATA 0-8 L01000	9
10		CONTROL #2 K1 L00013	BITS 8, 17 JK L01040	10
11		ADDRESS REG J0 L00010	BITS 8, 17 LML01040	11
12		ADDRESS REG J1 L00010	JK CORE DATA 9-17 L01000	12
13		CORE ADDRESS JK L01001	J DATA REG 9-16 L00006	13
14		ADDRESS REG K0 L00010	K DATA REG 9-16 L00006	14
15		ADDRESS REG K1 L00010	INPUT SWITCH 9-16 L00002	15
16	PORT ADDRESS CC L01004	REG LATCHES (EVEN) L00003	PORT DATA 9-17 L01003	16
17	CLOCK CARD #1 L01000	REG LATCHES (ODD) L00003	OUTPUT SWITCH 9-16 L00002	17
18	CLOCK CARD #2 L01001	REG LATCHES (NATURE) L00003	L DATA REG 9-16 L00006	18
19	CLOCK CARD #3 L01002	ADDRESS REG L0 L00010	M DATA REG 9-16 L00006	19
20		ADDRESS REG L1 L00010	LM CORE DATA 9-17 L01000	20
21		CORE ADDRESS LM L01001	GO CARD L01003	21
22		ADDRESS REG M0 L00010	REG RESPONSE L01004	22
23		ADDRESS REG M1 L00010	ACC RESPONSE L00473	23
24		CONTROL #1 L0 L00014	SAT RESPONSE L00473	24
25		CONTROL #2 L0 L00013	JK CORE DATA 18-25 L01000	25
26		CONTROL #3 L L01005	J DATA REG 18-25 L00006	26
27		CONTROL #1 L1 L00014	K DATA REG 18-25 L00006	27
28	CORE CONTROL LM L01002	CONTROL #2 L1 L00013	INPUT SWITCH 18-25 L00002	28
29		CONTROL #1 M0 L00014	PORT DATA 18-25 L01003	29
30		CONTROL #2 M0 L00013	OUTPUT SWITCH 18-25 L00002	30
31		CONTROL #3 M L01005	L DATA REG 18-25 L00006	31
32		CONTROL #1 M1 L00014	M DATA REG 18-25 L00006	32
33		CONTROL #2 M1 L00013	LM CORE DATA 18-25 L01000	33

	
P. CAHOESIAN H. MATSUYAMA	NEW FM BACKPANEL NEW FM L01039.1
DATE: _____ TIME: _____	APPROVED: _____ REVISION: _____