COURSE OUTLINE

INTRODUCTION TO CONTROL COMPUTERS

FIRST WEEK: GENERAL DISCUSSION OF COMPUTERS, COMPUTER-
CONTROL SYSTEMS, PROGRAMMING CONSIDERATIONS,
and COMPUTER INPUT-OUTPUT CHARACTERISTICS

MONDAY

Orientation

Introduction to TRW

Introduction to TRWC

Project Organizational Responsibility

"Closing the Loop" (movie)

General Discussion of Computers

Analog

Digital

Typical Applications

General Discussion of Digital Computers

Digital Computer Classifications

Organization of Digital Computers

How Digital Computers Work

Details of Digital Computer Sub-systems

General Discussion of a TRW Control Computer

Number Systems

Typical Instructions

Discussion of Simple Program

Introduction to Control Computers

TUESDAY

The Digital Control Computer

Objectives of Automatic Process Control

Mathematical Model of the Process

Objective Equation

Optimizing Function

Logging Function

Alarm Function

Demonstration of Fractionating, Mix, and Thermocouple Display

A TRW Computer Control System

Computer inputs from process instrumentation (analog inputs)

Ability to Enter Additional Information (digital inputs)

Executive Routine

Limit Checking

Alarm Function

Control Calculations

Logging Function

Ability to Request Information

Self-checking

Computer Outputs to the Process

Fail-Safe System

WEDNESDAY

Methods of Programming

Flow Diagrams

Types of Words

Instruction Format

Program Listing

Introduction to Control Computers

Methods of Programming (continued)

Indicators

Memory

Track, Sector, Bit

Track Assignments

Expanded Memory

Extra Writable Tracks

Registers (A, B, C, N, Y, and P)

Simple Programming Problem

Use of Flexowriter

THURSDAY

Analog Input/Output System

Minimum and Maximum System

Input Storage Locations

Method of Conversion

High-level and Low-level Inputs

Noise Rejection

Output Storage Locations

Power Gate Characteristics

Analog Rack

Analog System Options: Automatic Scanning, High-Speed Scanning, Unique Systems, Bi-Polar System, Programmed Inputs

Programming Practice

Basic Arithmetic Commands

Decision Commands

Flow Charting, Listing, Housekeeping

Introduction to Control Computers

Programming Practice (continued)

Loading Program

Running Program

Programming Analog Inputs and Outputs

FRIDAY

Digital Input/Output System

Digital Inputs

Digital Outputs

One-bit Outputs

Multi-bit Outputs

Types of Digital Input/Output Equipment: Digital Clock,
Digitran Switches, Matrix Switch, Push-button Switches

Programming Practice

Programming Digital Inputs and Outputs

Logic Commands

General Discussion of the Load Program

Introduction to Control Computers

SECOND WEEK: DETAILED PROGRAMMING, PROGRAMMING PRACTICE, and REVIEW

MONDAY

Computer Controls

Operation

Demonstration of Test and Maintenance Panel

Summary of the Command Repertoire

Introduction to the Program Library

Utility Package

Utility Package Demonstration

Trace Routine

Trace Routine Demonstration

OPUS

Programming Practice

TUESDAY

Programming Using Loops

Programming With Address Modification

Methods of Printing Out

Programming Practice

WEDNESDAY

Review of RW-300 Command Structure

Programming Practice

THURSDAY

Review of Analog and Digital Input/Output System

Programming Practice

FRIDAY

Programming Practice

COURSE OUTLINE

THEORY OF OPERATION AND MAINTENANCE

I. INTRODUCTION

A. PURPOSE AND GENERAL APPROACH

B. BASIC COMPUTER COMPOSED OF FOUR SECTIONS

1. Input/output

2. Arithmetic

3. Control

4. Memory

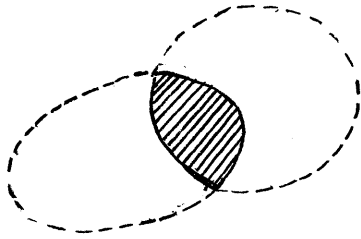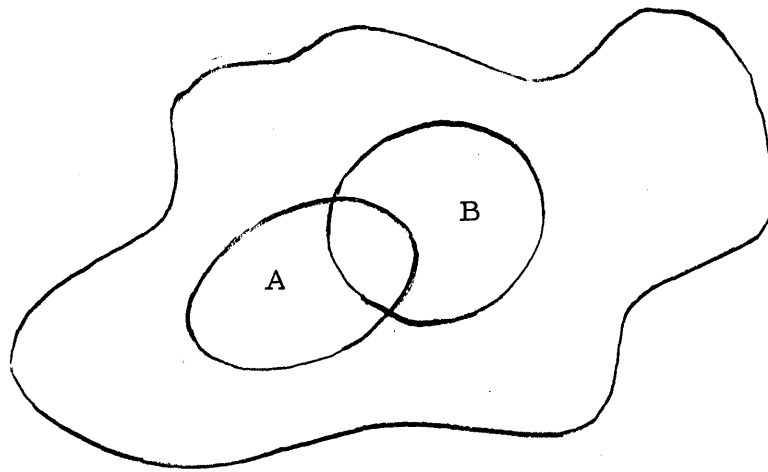C. INDEPENDENT ANALOG INPUT/OUTPUT SYSTEM

1. In addition, the RW-300 has an independent analog input/output system. This course starts with the analog system because it is easier to work with from a maintenance standpoint.

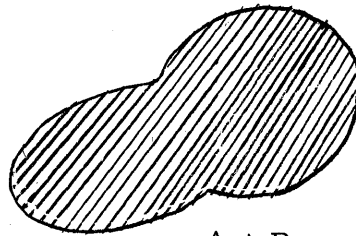II. INTRODUCTION TO SYMBOLIC LOGIC

A. BOOLEAN ALGEBRA

1. Two connectives (operations)

a. And (X) a.b, a x b, ab, a∧b

b. Or (+) a + b, a∨b

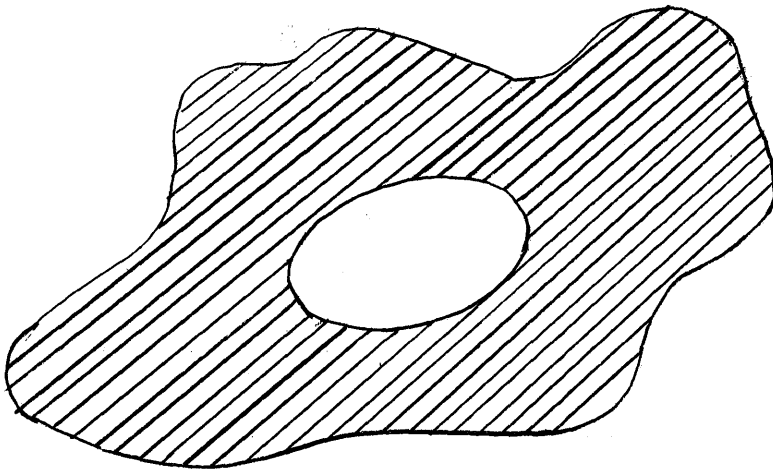c. (Diagram -- See Page 2)

(II. A. 1. c.)

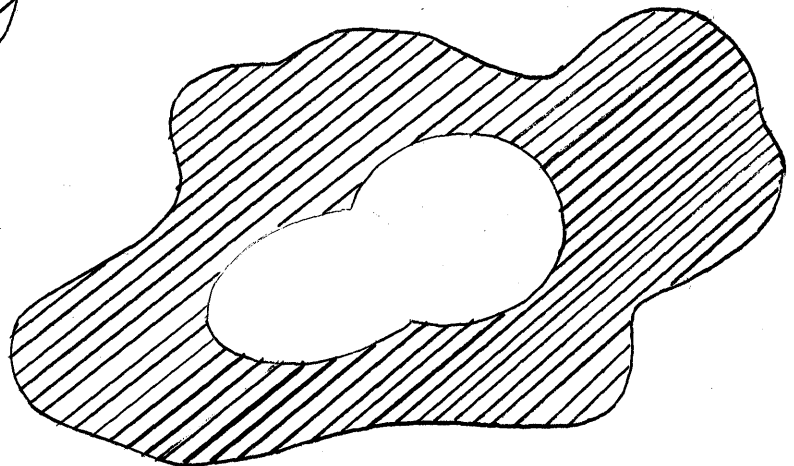A x B

A + B

A'

(A+B)' = A' x B'

2. Important Relationships

    a.   Two Values

        1)   True = (1)

        2)   False = (0)

    b.   Statement   Written

Statement	Written
0 AND 0 = 0	00 = 0
0 AND 1 = 0	01 = 0
1 AND 0 = 0	10 = 0
1 AND 1 = 1	11 = 1
0 OR 0 = 0	0 + 0 = 0
0 OR 1 = 1	0 + 1 = 1
1 OR 0 = 1	1 + 0 = 1
1 OR 1 = 1	1 + 1 = 1

    c.   Variables of Y

$$0Y = 0$$
$$1Y = Y$$
$$0 + Y = Y$$
$$1 + Y = 1$$
$$YY = Y$$
$$Y + Y = Y$$

    d.   Associative

        1) $(XY)Z = X(YZ)$

        2) $(X+Y) + Z = X+(Y+Z)$

    e.   Commutative

        1) $XY = YX$

        2) $X + Y = Y + X$

f. Distributive

    1) $X(Y + Z) = XY + XZ$

    2) $X + XY = X(1 + Y)$

           $X + XY = X(1)$

           $X + XY = X$

g. Negation (opposite)

    1) $0' = \overline{0} = 1$

    2) $1' = 0$

    3) $X + X' = 1$

    4) $XX' = 0$

    5) $X + X'Y = X + Y$

    6) $(X + Y)' = X'Y'$

    7) $(XY)' = X' + Y'$

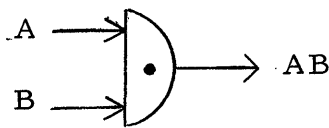h. Four useful identities

    1) $X + YZ = (X + Y)(X + Z)$
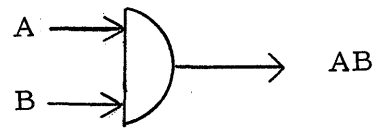
    2) $XY' + XY = X$

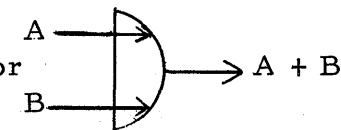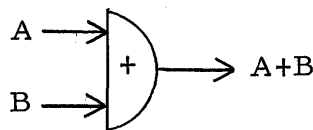   3) $X + XY = X$

    4) $X + X'Y = X + Y$

B. SYMBOLS FOR DECISION ELEMENTS
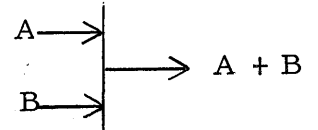
1. AND gate

2. OR gate

3.   Inverter (Negation)

   a.
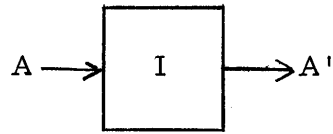
   b.   Outputs of inverters are sometimes underlined to indicate
         that they are derived by inversion (<u>D</u>2)

4.   Matrix Amplifier

   a.
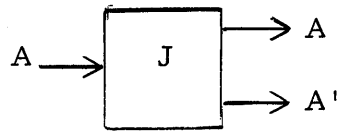
   b.   Amplifies power only

   c.   Two complementary outputs (A and A')

C.   CIRCUITS FOR DECISION ELEMENTS

   1.   Relay Circuits

      a.   AND Gates

b.   OR Gates
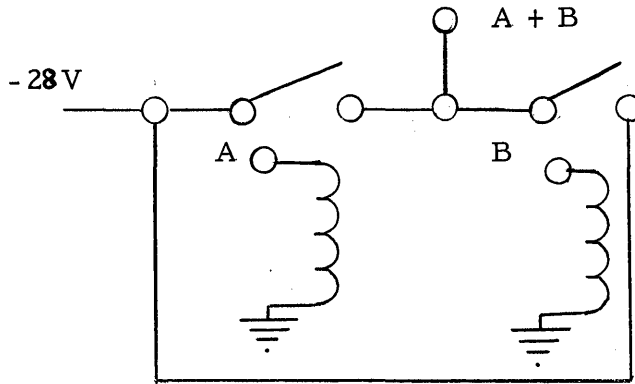
c.   Inverter
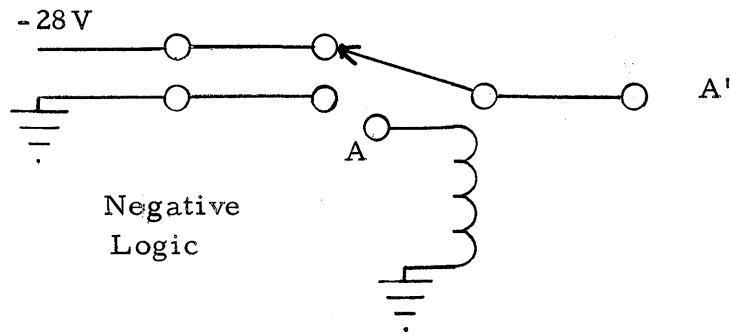
Negative
Logic

2.   Diode Circuits

a.   AND Gates
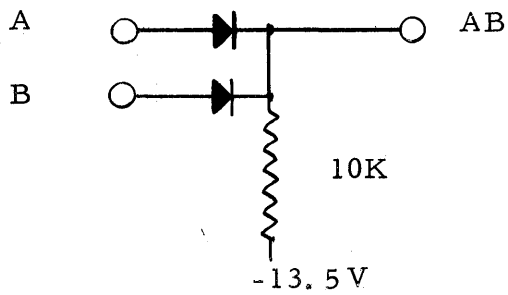
Negative AND   Positive AND
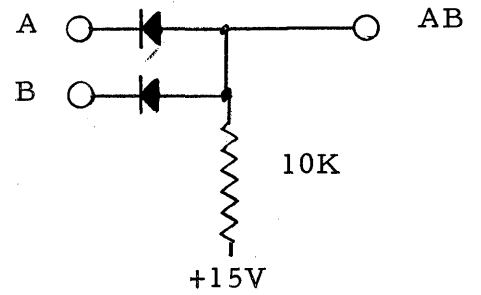
b.   OR Gates

Negative OR   Positive OR

A $\bigcirc$ ──▶│── ┬── $\bigcirc$ A + B   A $\bigcirc$ ──│◀── ┬── $\bigcirc$ A + B
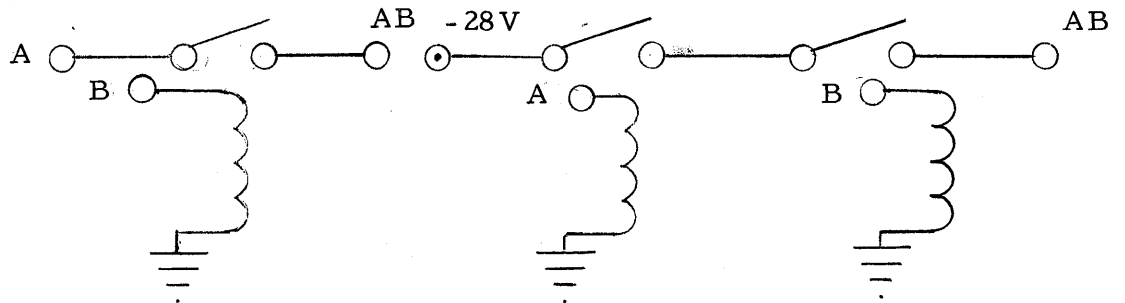
B $\bigcirc$ ──▶│── │   B $\bigcirc$ ──│◀── │

10K   10 K

+15 V   -13. 5 V
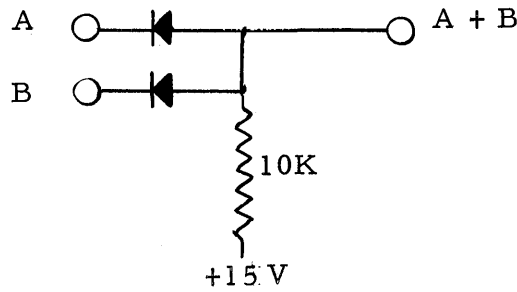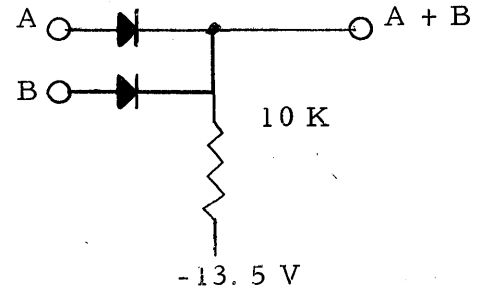
c.   Voltage drop across different types of diodes

1)   Germanium   . 2V average

2)   Silicon   . 7V average

3.   Transistor Circuits

a.   AND Gate

- 15V

A ──WWW──┐
                    ╲
B ──WWW──┘   ──▶ AB

PNP

b.   OR Gate

−15V   −15V

A ──   ── B

NPN chgd to PNP

A + B

c.   Inverter

15V

1.5K

A'

A

-5V
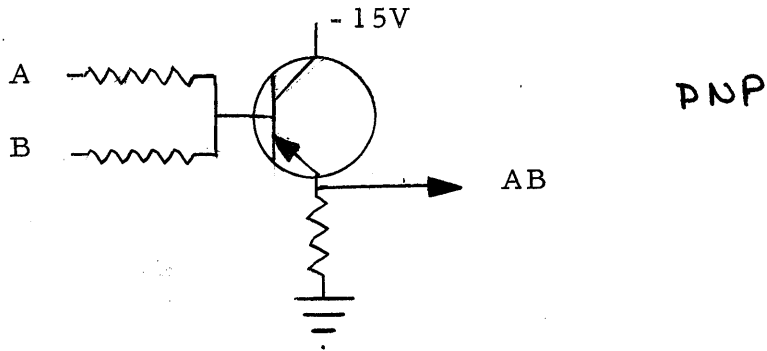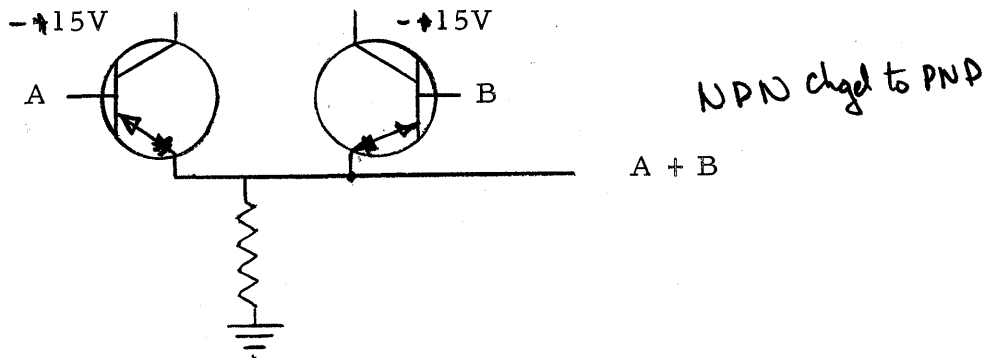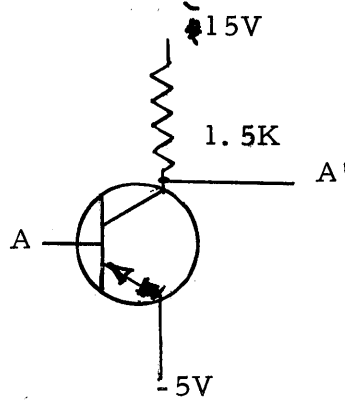
PNP
~~NPN~~

4.   References for those who wish to go further into implementation

a.   General Electric

b.   Richards

c.   Phister

d.   Grabbe, Ramo, Wooldridge

D.   DEVELOPMENT OF FUNCTIONS

1.   Example: $p = q$ ($f = 1$ when $p = q$)

a.   Truth Table

p	q	f
0	0	1
0	1	0
1	0	0
1	1	1

$f = p'q' + pq = (p' + q)(p + q')$ (Equality)

$f = pq + p'q'$
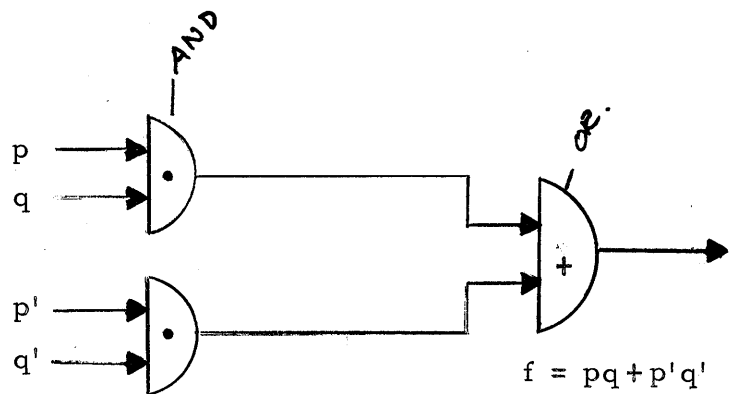
2. Example: Half Adder
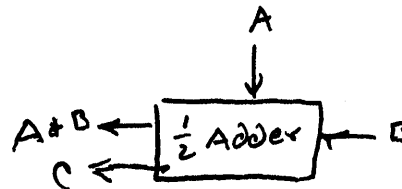
a. Truth table

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = A'B + AB'$

$C = AB$

3. Example: Full Adder
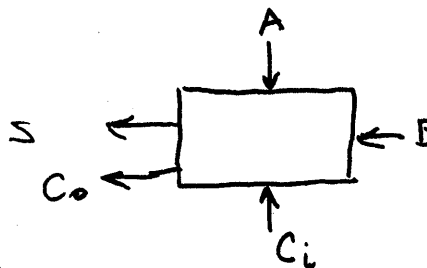
a. Truth table

A	B	C_i (CIN)	S	C_o (Cout)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(1)
$S = A'B'C_i + A'BC'_i + AB'C'_i + ABC_i$

or

� S = $C_i(AB + A'B') + C'_i(A'B + AB')$

$C_o = A'BC_i + AB'C_i + ABC'_i + ABC_i$

or

✶ $C_o = \underset{\text{NOT NEED SINCE Carry stays ON}}{C_i(A + B)} + AB(\underset{\text{always 1}}{C'_i + C_i})$

E. RW-300 Logic Structure

1. Typical Structure

✶ $C_o = A'B'$ turns carry to false

✶ STD ADDER EQUATIONS

(1) USED BY RW300

-9-

2. Logic Levels

    a.   A & C   *Logical voltage levels only*   *AC logic*

    FALSE $\pm$ 2.5

    b.   DG in-out   + 0   ← *FALSE*   *DC Logic*

                        -13.5

    c.   Analog   + 0   - *FALSE*

                        -13.5

F.   VARIATIONS OF AND & OR GATES

1.   Null -- $AB + AB' + A'B + A'B' = 0$ (Never True)

2.   Pierce Arrow -- $A'B' = 1$, $A \downarrow B$ (Also called NOR)

3.   Disjunction -- $AB + AB' + A'B = 1 = A + B$

4.   Sheffer Stroke -- $A'B + AB' + A'B = 1 = A \mid B$ (Also called NAND)

5.   Implication -- $A'B' + A'B + AB = 1$ (A implies B: If A is false,

                    equation is always satisfied; if A is true, B must

                    also be true to satisfy equation)

6.   Equivalence -- $A'B' + AB = 1$, $A \equiv B$

7.   Inequivalence -- $AB' + A'B = 1$, $A \neq B$, $A \oplus B$ (Also called

                        EXCLUSIVE OR) (E1)

8.   Identity -- $AB + AB' + A'B + A'B' = 1$ (Always TRUE)

G.   REFERENCES TO BOOKS AND CHAPTERS FOR THOSE WHO ARE INTERESTED IN SIMPLIFICATION TECHNIQUES

1.   Richards

2.   Ramo-Wooldridge

3.   Phister

H.   REVIEW AND ORAL QUIZ

III.   HAND OUT AND DISCUSS MAINTENANCE MANUALS

IV.   BASIC BUILDING BLOCKS (Three Types)

    A.   DECISION ELEMENTS

        1.   AND Gate

        2.   OR Gate

        3.   Inverter (not an independent decision element, but is used
              in decision logic)

    B.   MEMORY ELEMENTS

        1.   Flip-Flops
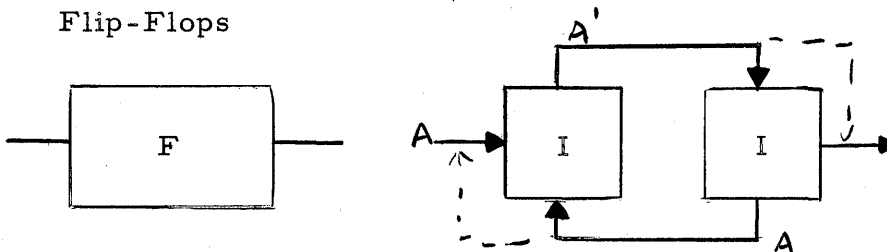
        a.   How to make a set-reset flip-flop using inverters
              (S R)

S = Set pulse

F ALSE

F & T chgs with
S & R T & F state

T
True

R   reset
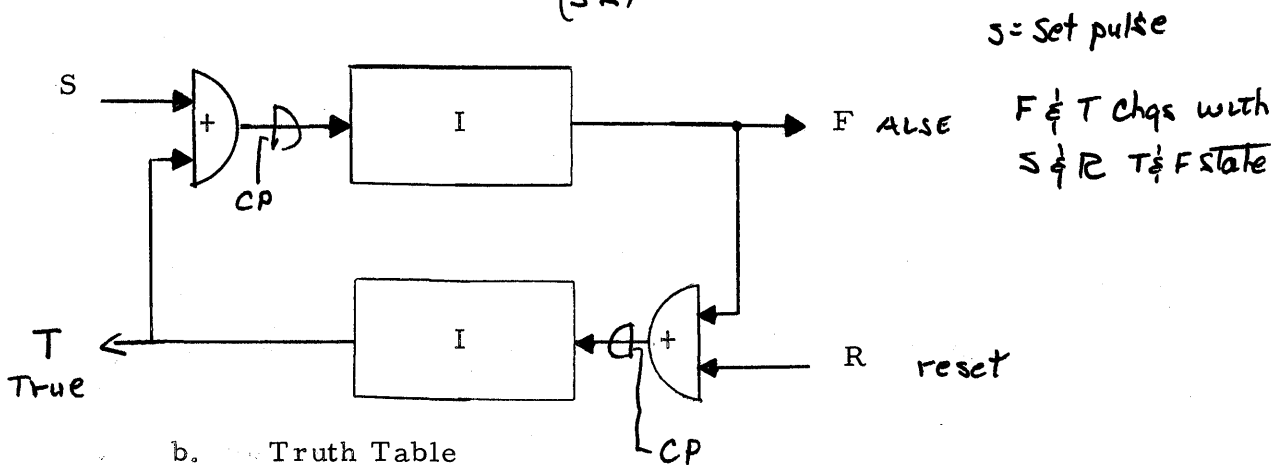
        b.   Truth Table

n is time interval

S_n	R_n	$T_n + 1$
0	0	T_n
1	0	1
0	1	0
1	1	?

1-bit delay

$$T_n + 1 = S + \overline{R}\ T_n$$

-11-

2. Synchronous S/R flip-flop (also called trigger f-f) FF #2, dcFF
(Hand out circuit description of FF #2)
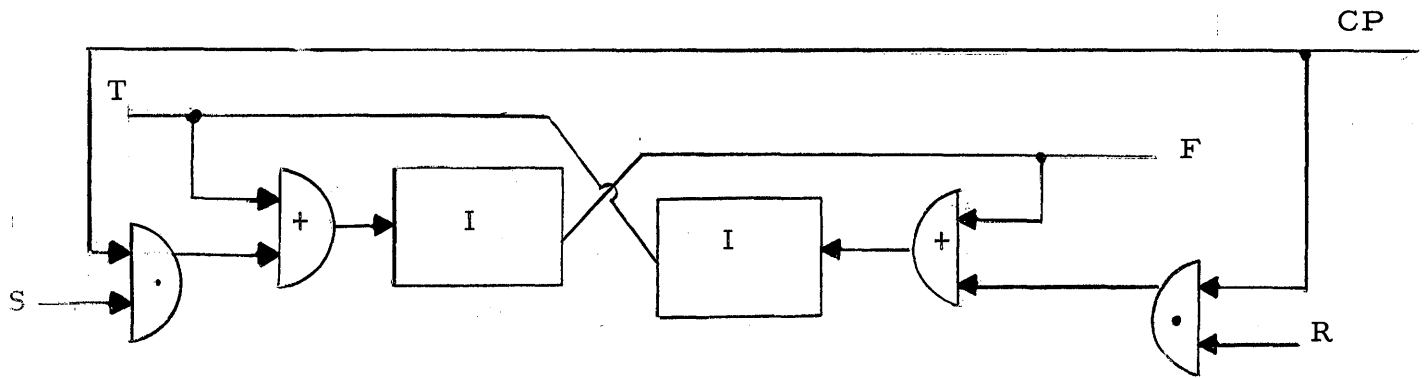
a. Clock pulses
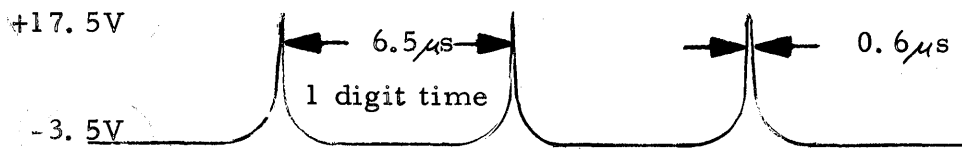
3. J-K Flip-flop
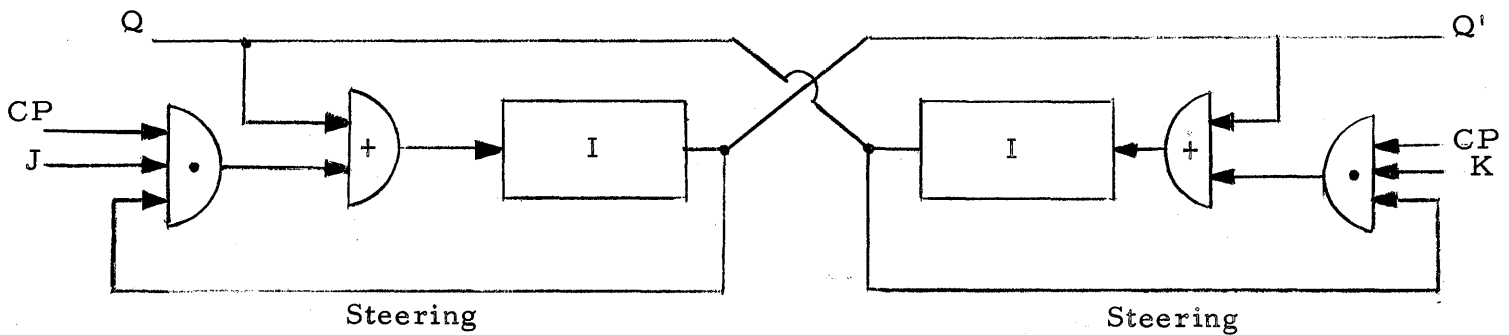
a. Truth Table

J_n	K_n	$Q_n + 1$
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n'

$$Q_n + 1 = J_n Q_n' + k'_n Q_n$$

b.   Logic Block Diagram
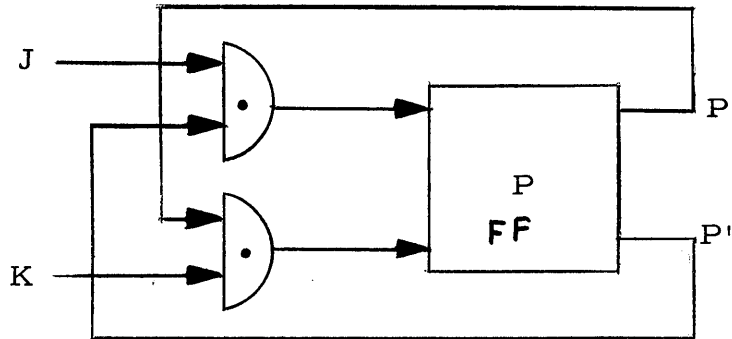
c.   Steering - Usually external -- Example Fl, F2 (Sector
       Counter)

4.   Delay Flip-flop

CLOCK
PULSE
IS INCLD.
IN CIRCUIT
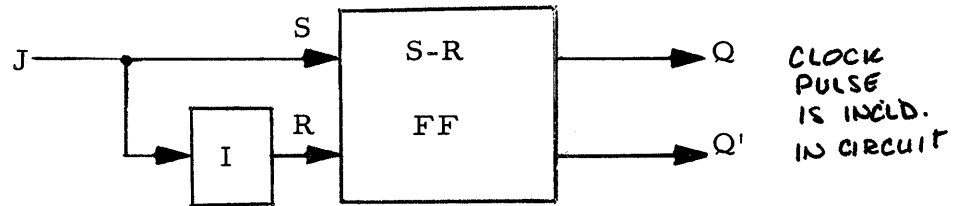
a.   Truth Table

J_n	$Q_n + 1$
0	0
1	1

$$n \quad\quad n+1$$
$$J = 1 \quad Q = 1$$
$$J = 0 \quad Q = 0$$

b.   Inverter may or may not be external

       1.   Delay FF (Internal Inverter)

       2.   Logic 11-1 & AL (External Inverter)

5.   Drum

       a.   Physical Characteristics

              1)   Diameter - 9"

              2)   Length - 9"

              3)   Circumference - 28.3"

-13-

4) Aluminum drum spray-coated with magnetic oxide

5) See Theory of Operation, Section 3-1 -- 3-3

b. Speed - 3600 RPM

1) 2 minutes to reach operating speed

2) 16 minutes to stop

c. Tracks

0-7	63	
7	64-CP	70-N
8-15		71-C
8-61	66-ST	72-A
8		73-B
62	69-Y	

Greater than 200 tracks can be used in quadruple memory system.

See Theory of Operation, Section 3-6 -- 3-11

d. Recording Method (Manchester)

WRITE VOLTAGE

10 V

0

-10 V

t ⟶

WRITE CURRENT

2^{00}ma

1^{00}ma

0

-1^{00}ma
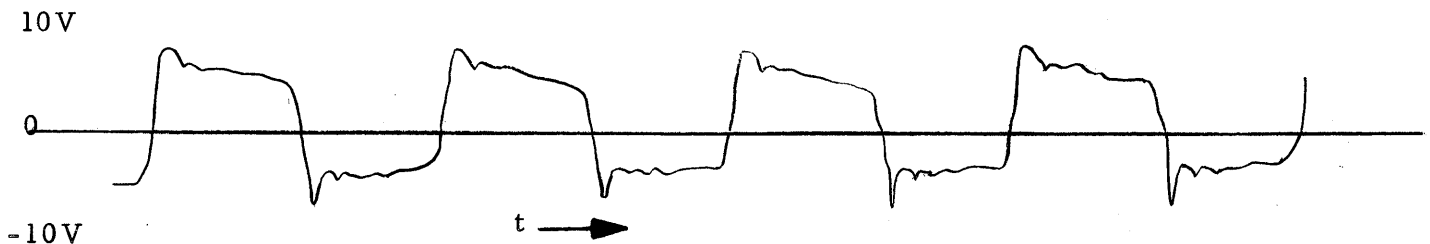
t ⟶
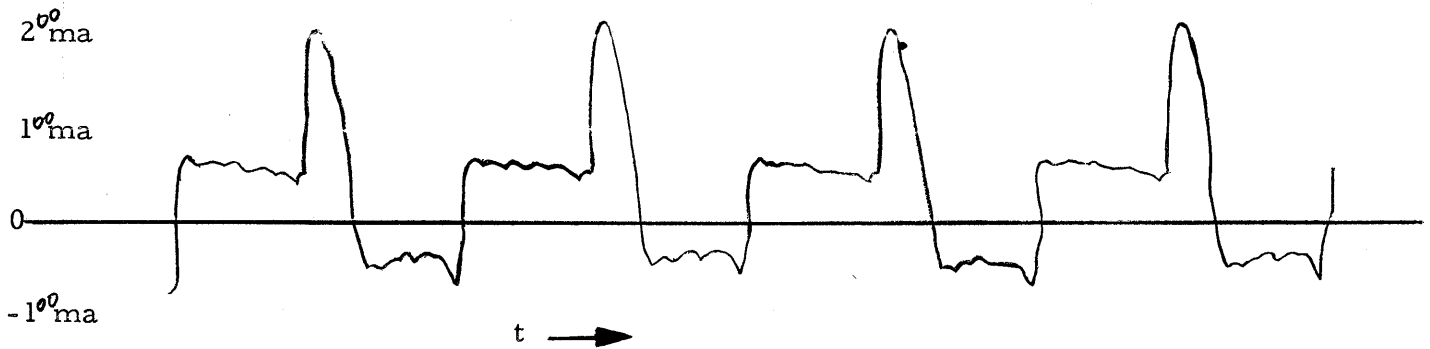
e.   Heads - (See CHK. & M. Pro. Page 4)

See Theory of Operation, Section 3-3 -- 3-6

6.   Review and Quiz

7.   A-C flip-flops (H 11, for example)   *H II IS AN AC FF IN ANALOG PORTION*

a.   Simplifies write problem

b.   Reduces power requirements of transistors, transformers, etc.

c.   Clock A and Clock B (What happens to FF?)

d.   How to detect the state of an a-c J-K flip-flop

e.   Gates controlling a-c flip-flops

C.   AMPLIFIERS

1.   Inverter

(See Schematic 4-2362, 4-1269)

2.   Clock Amplifier

(See Clock Read Circuit Description)

Hand out Circuit Description

3. Read Amplifier

(See Read Circuit Description)

Hand out Circuit Description

4. Matrix Amplifier

(See Matrix Amplifier Circuit Description)

Hand out Circuit Description

5. Write Circuit (also used as Power Amplifier)

(See Write Circuit Description)

Hand out Circuit Description

V. HOW BASIC BUILDING BLOCKS ARE USED IN THE ANALOG SYSTEM

A. COUNTERS (STATIC OR NON-RECIRCULATING REGISTERS)

1. Sector track (R66) as an example of a stored counter

a. Track Makeup

	1 2 3 4 5 6 7 8	9	10	11	12	13	14	15	16	17	18	19	20	1 2 3 4 5
SECTOR TRACK	Binary Coded Sector Number 0	0	0	0	0	1	0	0	1	0 or 1	0	0	1 or 0	Binary Coded Sector Number

Bit 17 is 0 in all sectors except Sector Track Sector 00.

Bit 20 is 1 in all sectors except Sector Track Sector 00.

b. Read Amplifier Converter

(See Read Amplifier Converter Circuit Description)

Hand out Converter Circuit Description

2. Revolution Counter as an example of straight binary counter
(See Analog Notes, page 5)

SHIFT OR RECIRCULATING REGISTER

(Can be simplified for true J-K FF operation, for use without shift pulse, for use as shift register only, and for use without clear)
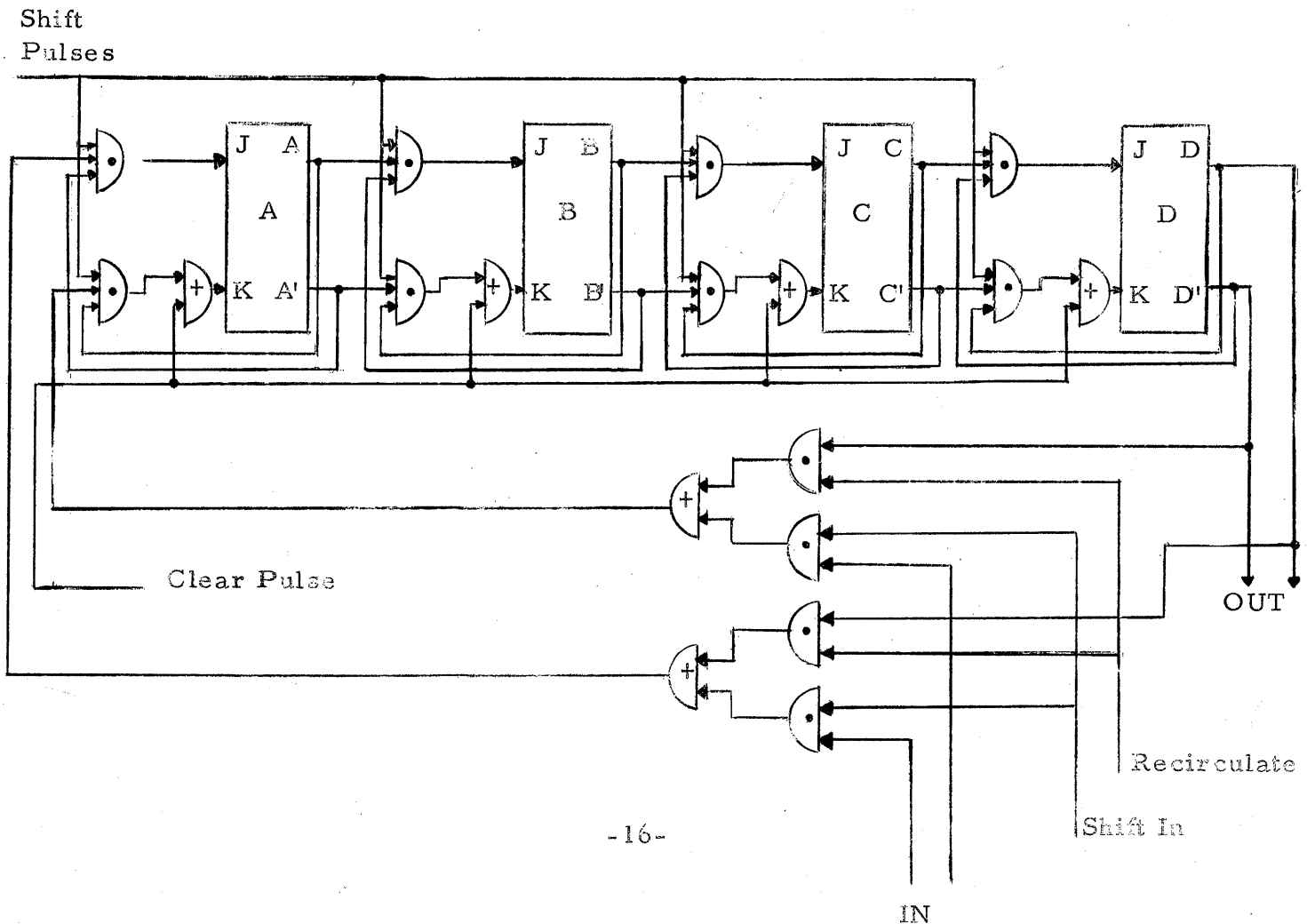
2. Circulating Registers:

Circulating registers will be discussed in Section VII.

VI. OPERATION OF THE ANALOG INPUT/OUTPUT SYSTEM

A. GENERAL FUNCTIONAL BLOCK DIAGRAM

(See Overall Function Block Diagram)

1. What analog system accomplishes

2. Maximum and minimum system limitations

B. DETAILED FUNCTION BLOCK DIAGRAM

(See Detailed Block Diagram)

1. Discussion of detailed block diagram

C. COUNTER-CONTROL FUNCTION

1. Digit Counter T10-T14

a. Function

b. Logical Block Diagram

(See Analog Notes, pages 1 and 2)

2. Sector Counter F1 - F7

a. Function

b. Logical Block Diagram

(See Analog Notes, pages 3 and 4)

c. Identify specific sectors of sector track (R66) using

F7 and delayed sweep

3. Revolution Counter X10-X13

a. Function

b. Logical Block Diagram

(See Analog Notes, page 5)

c. Note: LR is formed on back side of TB8. TB8 is

located behind Module 422.

c. Detailed description of Voltage Gate

(See Voltage Gate Circuit Description)

Hand out Circuit Description

5. Kin-tel Amplifier

a. Function

b. Logical Block Diagram

(See Block Diagram of Kin-tel Amplifier, Analog section of this notebook)

c. Detailed description of Kin-tel amplifier

(See Detailed Description of Kin-tel amplifier, Analog section of this notebook)

E. OUTPUT CONTROL FUNCTION

1. Analog Output Voltage Gates

a. Function

b. Logical Block Diagram

(See Analog Notes, page 17)

2. Analog Output Power Gates

a. Function

b. Logical Block Diagram

(See Analog Notes, page 17)

c. Detailed description of Output Power Gate

(See Power Gate Circuit Description)

Hand out Circuit Description

d. Note: Current feedback resistors are located on TB8.

F. CONVERTER FUNCTION

1. Input Detectors

a. Function of Input Amplifier, DA 1 & 2, and DA 3 as a group.

(See Circuit Descriptions of these)

Hand out Circuit Descriptions

b. Logical Block Diagram

(See Analog Notes, pages 16 and 17)

c. Detailed description of the Input Amplifier

d. Detailed description of Detector Amplifier 1 & 2

e. Detailed description of Detector Amplifier 3

2. Converter Register

a. Function

b. Logical Block Diagram

(See Analog Notes, pages 12-14)

3. Current Generator

a. Function of Current Gates and Current Weighter Resistors as a group

(See Circuit Descriptions of these)

b. Logical Block Diagram

(See Analog Notes, page 15)

4. AC FF H11

a. Function

b. Logical Block Diagram

(See Analog Notes, page 12 and Low-Level AC FF Circuit Description)

Hand out Circuit Description

5. Detector Amplifier 4

(See Circuit Description)

Hand out Circuit Description

a. Function

b. Logical Block Diagram

(See Analog Notes, pages 16 and 17)

c. Detailed Description of Detector Amplifier 4

6. Zero-Stabilization

    a. Function or VG 301 and PG 301 as a group

    b. Logical Block Diagram

       (See Analog Notes, page 16, Voltage Gate Circuit Description, and Power Gate Circuit Description)

7. Write FF X8

    a. Function

    b. Logical Block Diagram

       (See Analog Notes, page 11)

G. MEMORY FUNCTION

1. Power Inverter 08-15

   (See Schematic 4-1269)

    a. Function

    b. Logical Block Diagram

       (See Analog Notes, page 20 and 21)

    c. Detailed description of a Power Inverter

2. Write Amplifiers 08-15

    a. Function

    b. Logical Block Diagram

       (See Analog Notes, pages 20 and 21)

    c. Detailed Description of a Write Amplifier

       (See Write Circuit Description)

3. Drum

    a. Function in analog system

    b. Methods for determining where analog inputs will be placed on the drum

    c. Optimization

       1) Methods for using minimum number of analog tracks

       2) Methods for using minimum number of voltage gates

       3) Methods for using minimum number of Kin-tel Amps.

H.   FLOW DIAGRAM OF WIRED ANALOG SYSTEM PROGRAM

(See Flow Diagram of Analog Input/Output System, Analog Section
of this notebook)

I.   ADJUSTMENT PROCEDURE FOR ANALOG INPUT/OUTPUT SYSTEM

(See Adjustment Procedure for Analog Input/Output System, Analog
section of this notebook)

J.   ANALOG INPUT CABINET

(See Analog Input Cabinet notes, Analog Section of this notebook)

1.   Analog J-Box

2.   Dual input relay assembly

3.   Relay gate assembly

4.   Indicator assembly

5.   +18V and -24V power supplies are located here but will be
       discussed later

6.   Thermocouple reference junction oven.

K.   REVIEW AND TEST

VII.   HOW BASIC BUILDING BLOCKS ARE USED IN THE A & C SYSTEM

A.   RECIRCULATING REGISTERS (ONE-WORD REVOLVERS)

1.   A Register

a.   Logical Block Diagram

(Hand out blank register layouts)
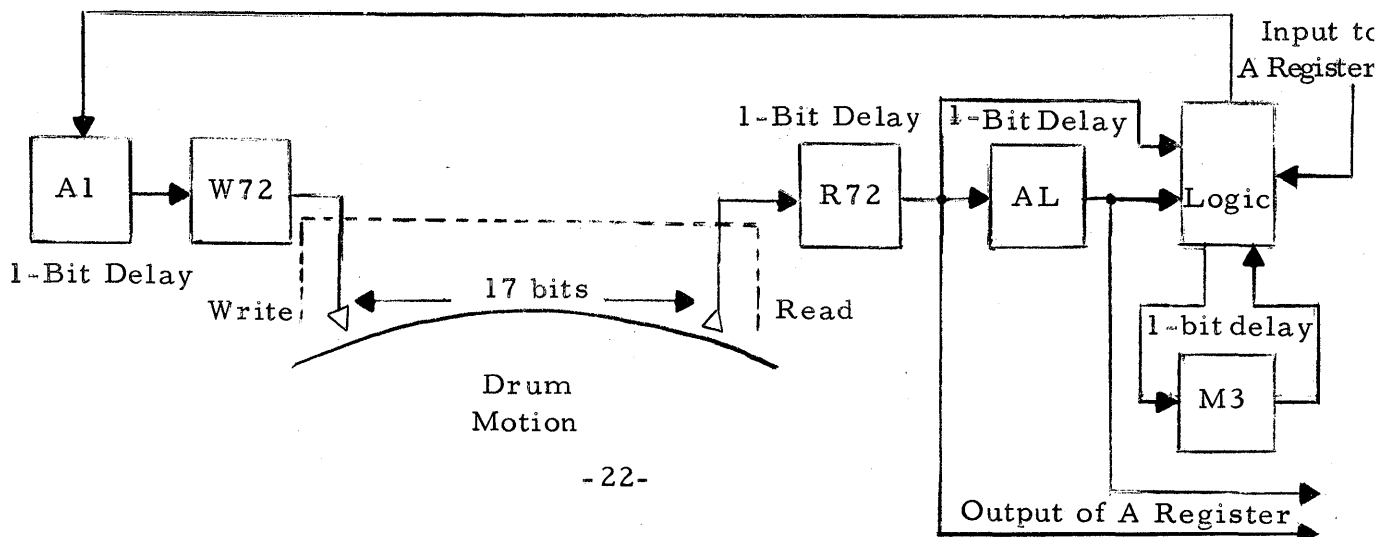
b.   Functions

   1)   Contains augend and then sum in add

   2)   Contains subtrahend and then difference in subtract

   3)   Contains multiplicand, partial product, and then bits of
         product in multiply.

   4)   Contains dividend, partial quotient, and quotient in
         divide.

2.   B Register

   a.   Logical Block Diagram
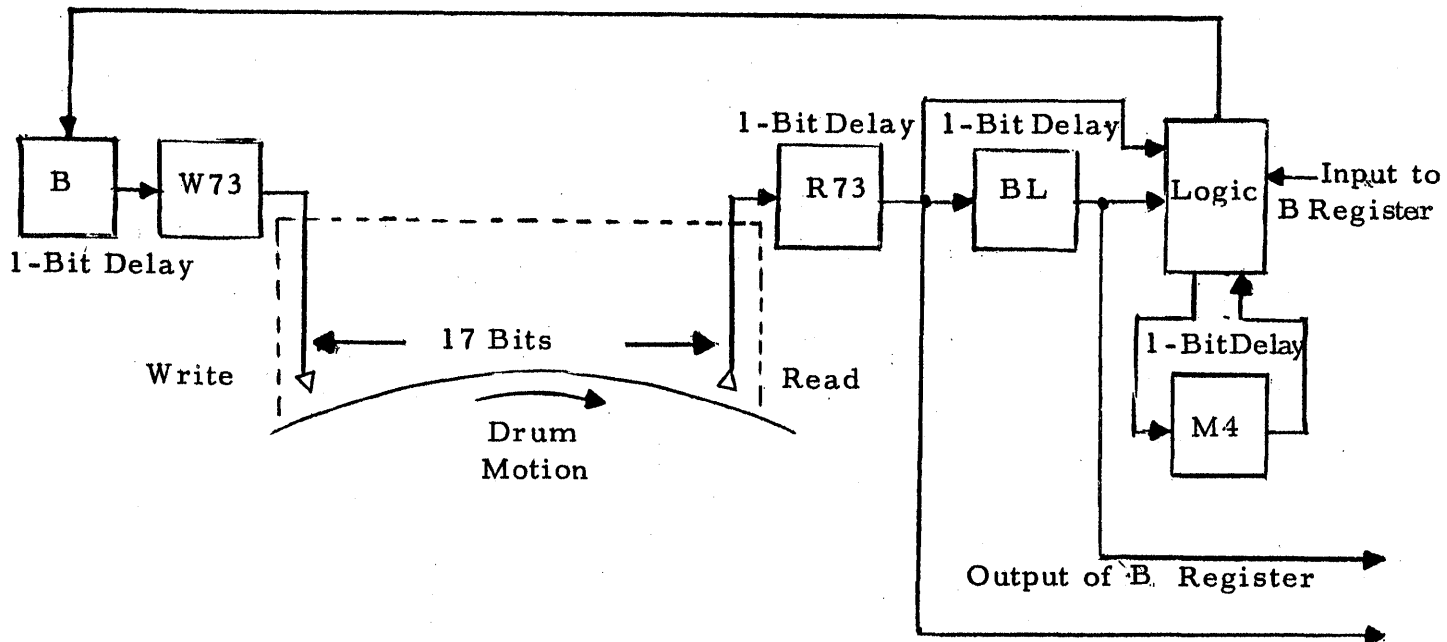
b.   Functions

   1)   Contains multiplier and then LS bits of product
         in multiply

   2)   Contains dividend and then remainder in divide

3.   C Register

   a.   Logical Block Diagram
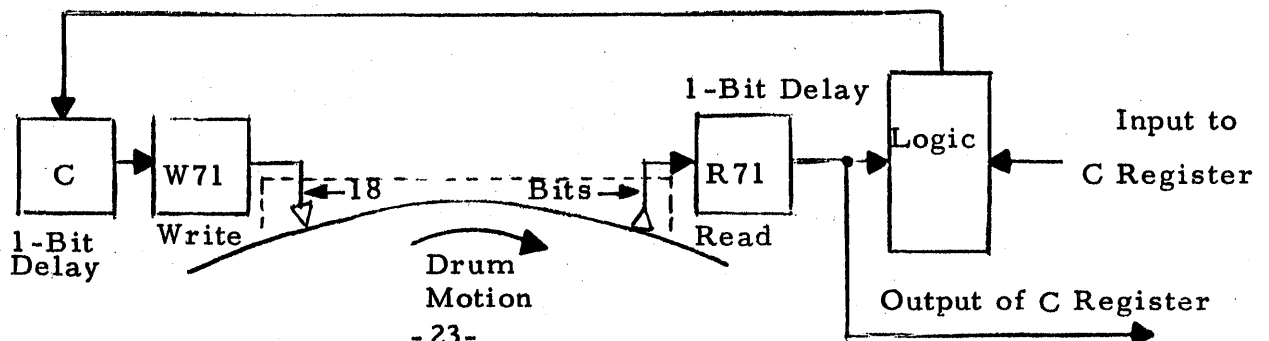
b.   Functions

     1)   Contains EX Code

     2)   Contains multiplicand in multiply

     3)   Contains divisor in divide

4.   N Register

    a.   Logical Block Diagram
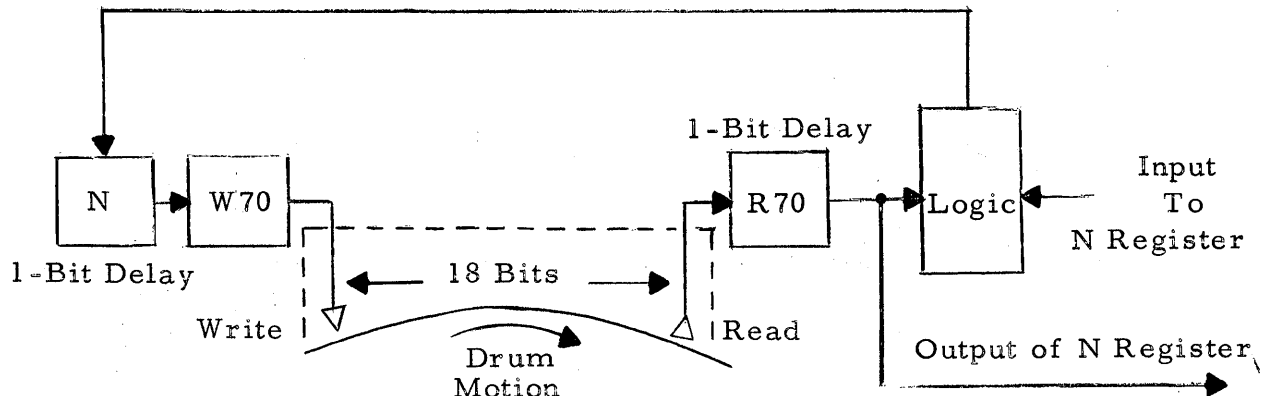
b.   Functions

     1)   Contains next instruction address

     2)   May contain operand address in transfer command

5.   Y Register

    a.   Logical Block Diagram
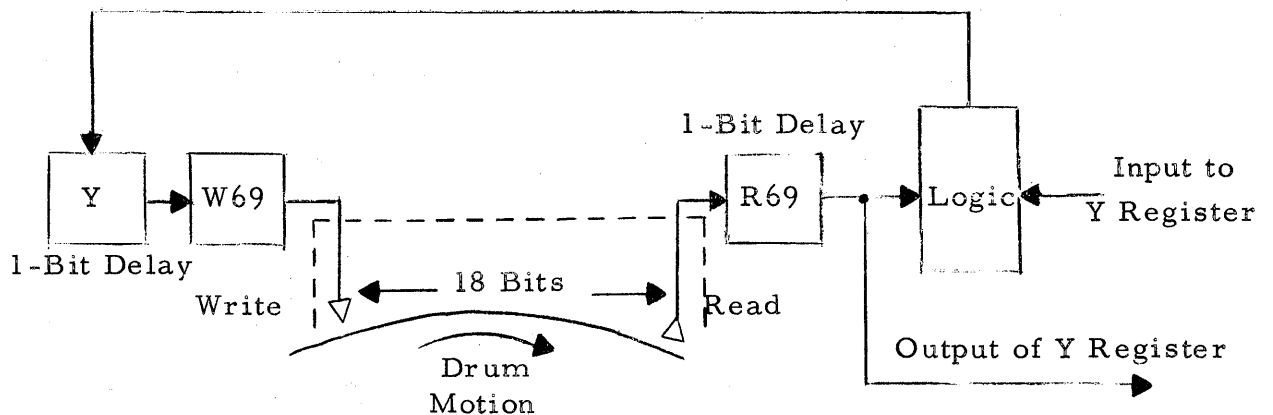
b.   Functions

     1)   Contains operand address

     2)   Contains operand address plus EX code in SH, M, D

B.   SPECIAL INDICATORS

    1.   Equality: E1 LLFF

        a.   Logical Block Diagram

    2.   Overflow: Z2 LLFF
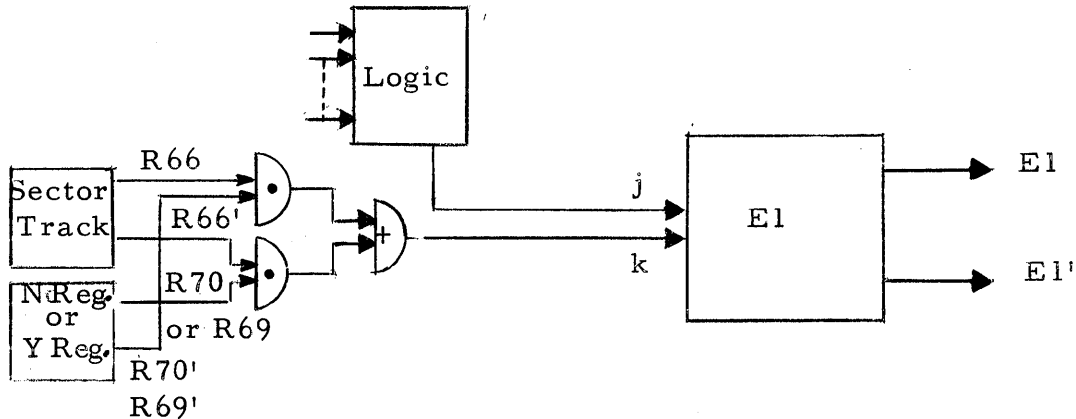
        a.   Logical Block Diagram
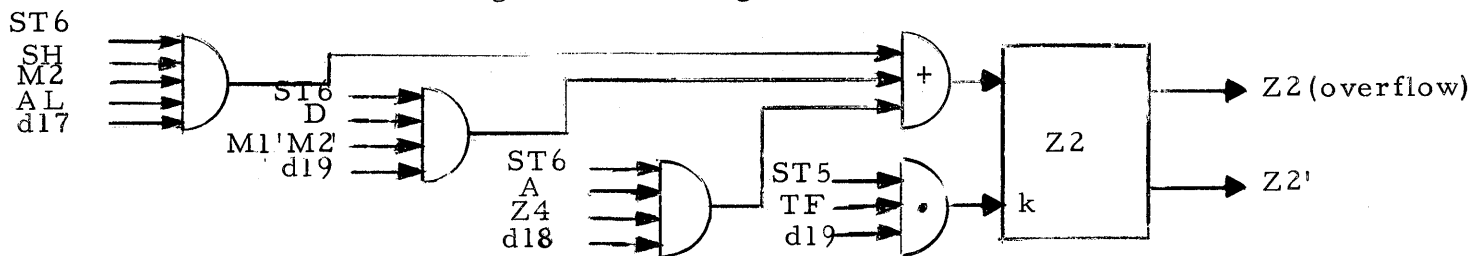
    3.   The description of the T & M panel

        a.   Scope

            1)   (V19, V20, V21, Z12, L31)

        b.   Track guard relay and switch

        c.   Selector switch

            1)   Neon indicators

            2)   Neon drivers

C.   ADDER: J6   J7   J8 MATRIX AMPLIFIERS   Z4 LLFF

    1.   Does all arithmetic operations

2.   Logical Block Diagram
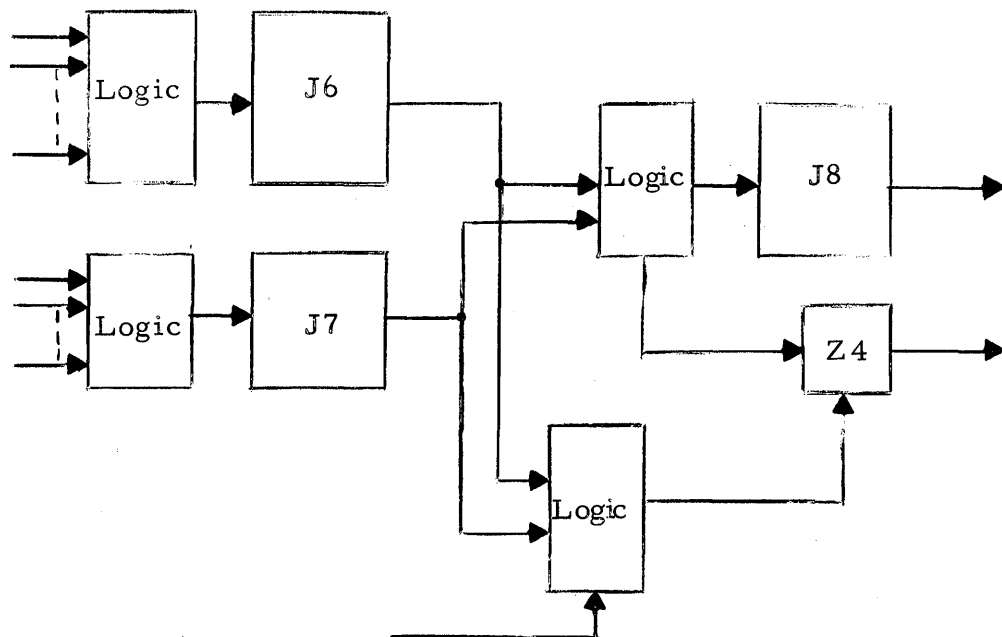
3.   Review development of adder logical equations

VIII. FUNCTION, LOGICAL BLOCK DIAGRAM, AND PARTICULARS OF EACH COUNTER AND REGISTER IN THE A & C UNIT

A.   SECTOR COUNTER (R66)

    1.   Description of Sector Track

    (See Section V. A. 1)

B.   DIGIT COUNTER (T) (T1-T9)

    1.   6 LLFF   2 WA-T8, T9   3 HL FF-T2, T5, T7

    2.   Uses more FF's and therefore fewer diodes, resulting in reduced cost

    3.   Logical Block Diagram

(SEE NEXT PAGE)

T2 — j T1
T2'T3 — k LLFF

T8' — j T2
T3T8 — k HLFF

T2T4T5 +T1'T5 — j T3
T1T2'T3 +T5' — k LLFF

T4' — j T4
T2T8' — k LLFF

T2T3' — j T5
T1'T3 — k HLFF

T2 (T2T7') (R66) — j T6
k LLFF

T2 (T2'T3'T5') (R66) — j T7
k HLFF

T2 — j T8
T2'T9' — k LLFF WA

T2 — j T9
T2'T6' — k LLFF WA
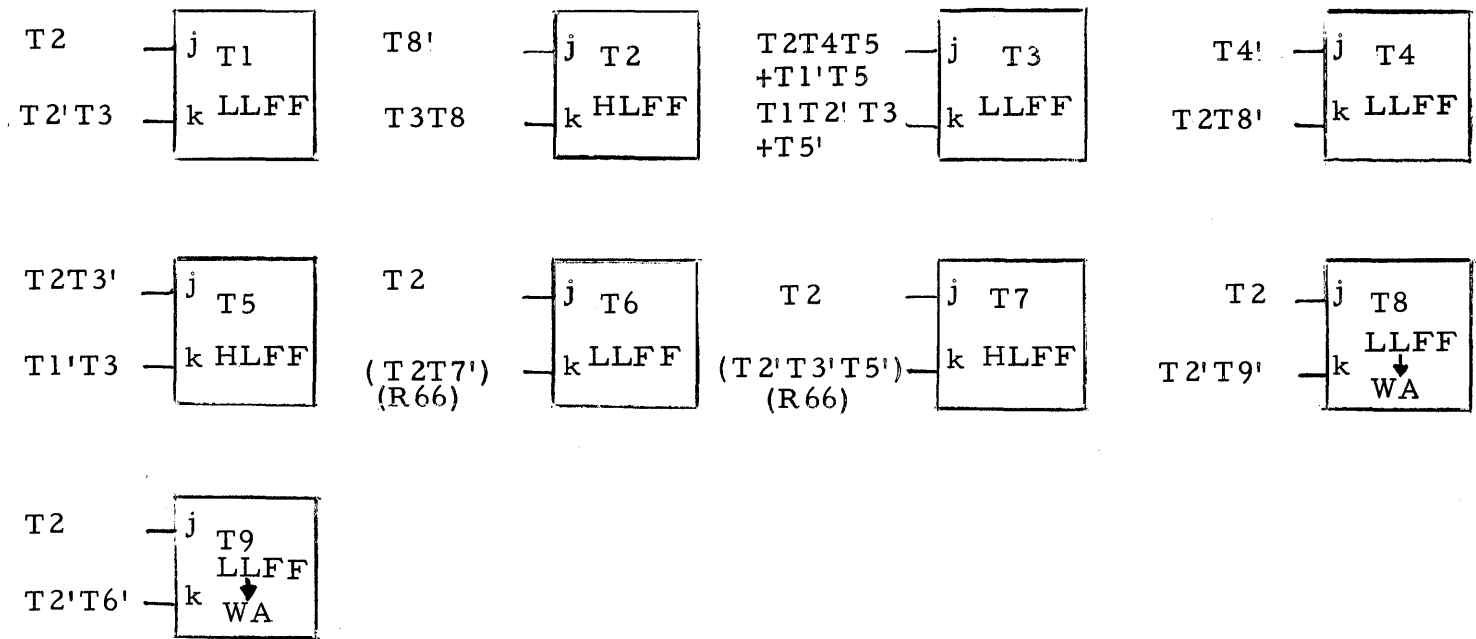
C.   STATE COUNTER (S) (DOESN'T COUNT IN SEQUENCE)

1.   Introduction of the state concept

(See Theory of Operation Manual, page 3-26 for state counter sequence)

2.   Logical Block Diagram
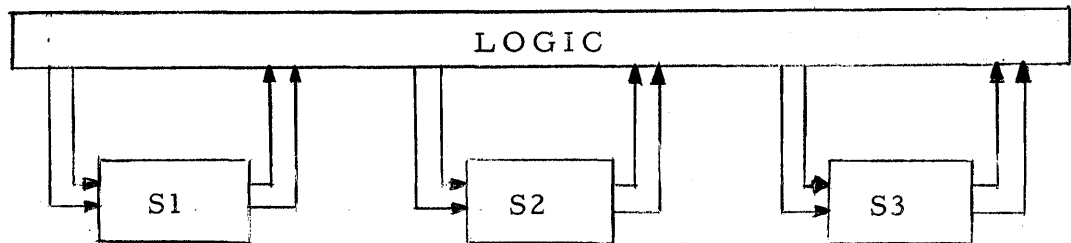
D.   INSTRUCTION REGISTER (P)

1.   Uses

a.   Extracts EX code from first instruction word

b.   Transfers EX code to C Register

c.   Extracts instruction code from second instruction word

2. Logical Block Diagram
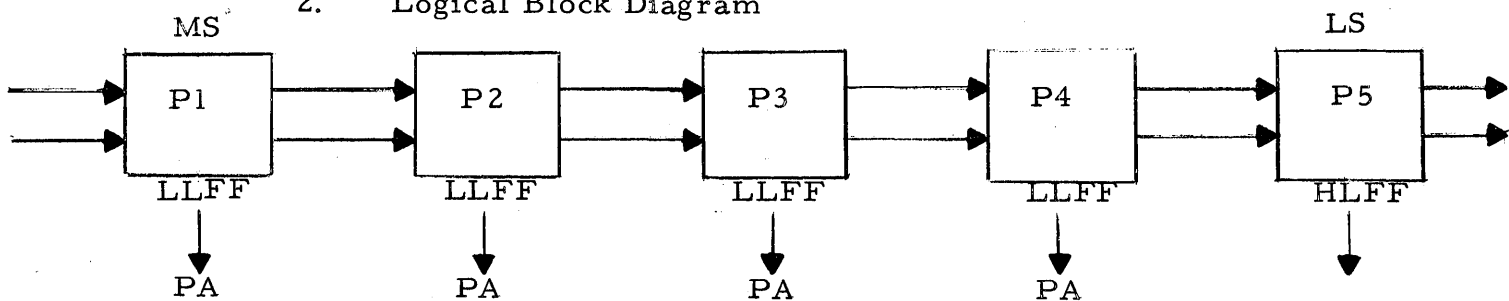
E. TRACK REGISTER (M)

1. Uses

    a. Contains track address of operand

    b. Contains track address of next instruction

    c. Contains type of switch or type of shift

    d. Contains digital input or output address

    e. FF M1 is used in connection with A and B registers in multiply or divide

    f. FF M3 lengthens A register

    g. FF M4 lengthens B register

    h. FF M5 holds sign of remainder in divide (same sign as dividend)

2. Logical Block Diagram
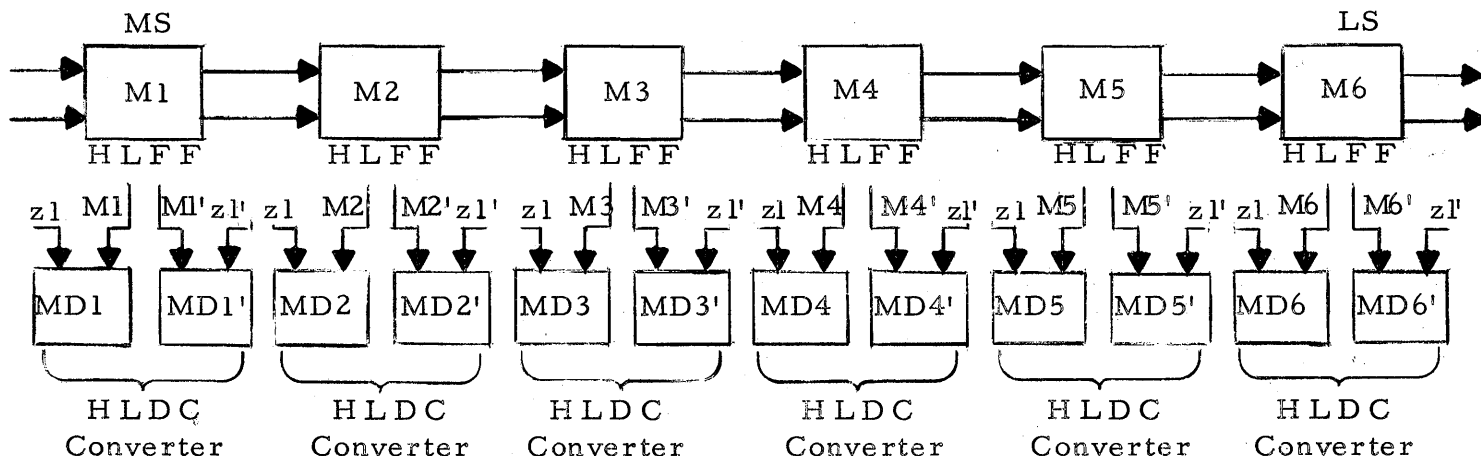
F.   REVOLVER

1.   Logical Diagram

IN   OUT

From A Reg.   To A Reg.
or B Reg.   or B Reg.

| W63 | Logic | R63 |

31 sectors + 19 bits
or 16 sectors + 19 bits

Write   Read
Q263   Q63

Drum
Motion
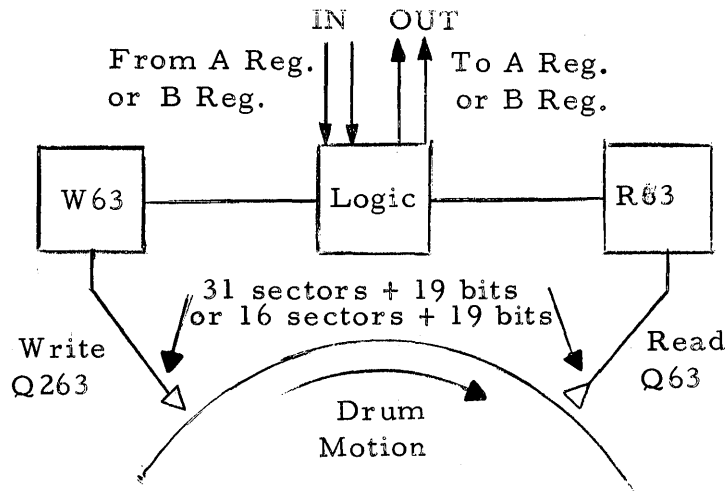
IX.   READ/WRITE CIRCUITS

A.   READ CIRCUITS

1.   Location of read heads

(See Theory of Operation, Figures 3-3, 3-4)

2.   Preamplifiers

(See Schematic 4-13800)

3.   Read selection matrix   MD1 - MD6

(See Theory of Operation, Figures 3-7, 3-8)

4.   Isolation circuits

(See A & C notes)

a.   Isolation Circuit No. 1

      (See Schematic 4-4251)

b.   Isolation Circuit No. 2

      (See Schematic 4-4251)

5.   Read amplifiers

a.   Clock read

Note: To prevent destroying clock track and sector track,
always stop machine and allow drum to stop before removing
or inserting clock read circuit.

(See Circuit Description, Read Circuit Schematic 3-767)

b.   General storage read (GSR)   (R1)

      (See Circuit Description, Read Circuit Schematic 4-4110)

c.   Various Read Circuits

      1)   R63 - Revolver

      2)   R66 - Sector Read

      3)   R69 - Y Register

      4)   R70 - N Register

      5)   R71 - C Register

      6)   R72 - A Register

      7)   R73 - B Register

      8)   R88 - Analog Read

      9)   R89 - Analog Read

B.   WRITE CIRCUITS

(See Circuit Descriptions: Memory Control, Write Control, and Write Circuit)

1.   Location of write heads and use of read heads for writing

(See Theory of Operation, Figures 3-3, 3-4)

(See Programming Manual, Figure 4-1)

2.   MD terms

a.   Why MD terms are used

b.   Selection of specific track

(See Write Head selection portion of Write Control vellum and quadrile)

c.   Selection of write module (113 or 422)

(See Instructions by States, SA and SB)

1)   Explain MD3'SW

3.   Logical Block Diagram

(See Write Control vellum and quadrile)

4.   Record error (J1, J2)

(See Relay Driver Card Block Diagram, A & C section of this notebook).

C.   EXPANDED MEMORY

    1.   Read switching

       (See notes on Expanded Memory)

    2.   Write switching

       (See notes on Expanded Memory)

X.   <u>HOW BASIC BUILDING BLOCKS ARE USED IN THE DIGITAL</u>
<u>INPUT/OUTPUT SYSTEM</u>

A.   REGISTERS

    1. $V_1 -- V_{18}$

       a.   Serial in -- Parallel out

       b.   Holds contents of A register

    2. $V_{26} -- V_{30}$

       a.   Parallel in-out

       b.   Holds track address so that M register can be
         used for other things

B.   SPECIAL FLIP-FLOPS AND THEIR ASSOCIATED CIRCUITRY

    1.   VXX (22, 23, etc) (also A2, A3)

       a.   Function of flip-flop and associated relays

       b.   Circuit Description

C.   DIGITAL INPUT/OUTPUT SYSTEM

(For detail on the following, see the Digital section of this notebook)

    1.   Parallel to serial input conversion

    2.   Serial to parallel output conversion

    3.   Magnetic latching relays

    4.   Multi-bit outputs

5. One-bit outputs

6. One-bit outputs with override

7. Flexowriter

    (See Flexowriter Schematic 4-3480 -- also Theory of
    Operation Manual, Figure 3-24)

8. Logging Typewriter

9. High-speed punch

10. Ferranti tape reader

11. Block diagram of Digital Input/Output system

    (See Theory of Operation manual, Figure 3-25)

12. Delay Generator

    Hand out delay generator Circuit Description

D. OPERATOR'S CONSOLE

    (For detail on the following, see the Operator's Console section
    of this notebook)

    1. Function

    2. Breakdown

        a. Matrix and Digitran Switches

        b. Other Switches

        c. Digital Clock

        d. Watchdog Timer

        e. Digital Drawer

            1) Input power amps

            2) Logic C Cord

            3) Input level changing emitter follower

            4) Relay control amplifiers

            5) Relay chassis

        f. Logging decoder

        g. Fail-safe chassis

XI. INSTRUCTIONS BY STATES

(See Instructions by States section of this notebook)

A.   STATES 1, 2, 3, and 8

   1.   State 1

      a.   Operation: Search for next instruction

      b.   Detailed explanation

      c.   Logic equations for State 1

   2.   State 2

      a.   Purpose: Read first word

      b.   Detailed explanation (class participation)

      c.   Relating description to logic equations (class participation)

   3.   State 3

      a.   Purpose: Read second word

      b.   Quiz class to lead to explanation

   4.   State 8

      a.   Purpose:

      b.   Detailed explanation

         1)   Manual controls

            a)   Fetch

            b)   Execute

            c)   Stop

2)   Stop command

3)   Record error

4)   Use of M1, M2

B.   INSTRUCTIONS REQUIRING OPERAND

1.   Load A

2.   Load B

3.   Load A negative

4.   Add

$$
\begin{array}{llll}
+5 & +5 & +(-5) & +(-5) \\
\underline{+9} & \underline{+(-9)} & \underline{+9} & \underline{+(-9)} \\
+14 & -4 & +4 & -14
\end{array}
$$

(See Add/Subtract flow chart in A & C Section of this notebook)

5.   Subtract

6.   Compare magnitude

7.   Extract

8.   Merge

9.   Multiply

(See multiply flow chart, A & C section of this notebook)

10. Divide

    a.   Corrective   (See Division by Corrective and Non-corrective Add, A & C Section of this notebook)

    b.   Non-corrective

    (See divide flow chart, A & C Section of this notebook)

C.   INSTRUCTIONS NOT REQUIRING OPERAND

1. Real address as operand address

    a.   Use

    b.   Instructions

        1)   Store A

        2)   Store B

        3)   TN

        4)   TF

        5)   TZ

2. Psuedo address as operand address

    a.   Use

    b.   Instructions

        1)   Shift

        (See shift flow chart, A & C section of this notebook)

            a)   Use

                1))   00-15 A right nn places

                2))   16-31 A left nn places

                3))   48-63 A, B left nn places

        2)   Switch

            a)   Use

                1))   00-15 A $\rightarrow$ B

                2))   16-31   B $\rightarrow$ A

                3))   32-47   A $\leftrightarrow$ B

                4))   48-63   0 $\rightarrow$ A, B

3) Digital

    a)   Use:

        1))   00-31 Output

            a))   00 Output to Flex

            b))   01 Logging Typewriter

            c))   02 High Speed Punch

            d))   03 Pre-empted if High Speed
                         Punch is used

            e))   04-31 Watchdog Timer, Logging
                         Decoder, Indicators,
                         Alarms, etc.

        2))   32-63 Input

            a))   32 Flex

            b))   33 Ferranti

            c))   34 Pre-empted if High Speed
                         Punch is used

            d))   35 Pre-empted if High Speed
                         Punch is used

            e))   36-63 Clock, Watchdog Timer,
                         Switches, Matrix Switches,
                         etc.

    4)   Tape

D.   INSTRUCTIONS NOT REQUIRING AN OPERAND ADDRESS

    1.   Stop

    2.   No op

XII.   <u>LOCATION OF PARTS</u>

Point out the location of all modules, chassis, and terminal boards.

XIII. CLOCK PULSE GENERATION, POWER SUPPLY, AND POWER CONTROL

A. CLOCK GENERATOR CIRCUITS

1. General function description of Clock Circuitry

   (See Clock Circuitry Circuit Description)

2. Clock Generator Circuitry

   (See Clock Generator Circuit Description)

B. PRIMARY POWER CONTROL CIRCUITS

(See Power On, Power Off relay sequencing Circuit Description and power control schematic in Schematics section of this notebook)

C. POWER SUPPLY CIRCUITS

1. Voltage Distribution

   (See Voltage Distribution Diagram RW-300 in Schematics section of this notebook)

2. -27 volt supply

   (See Voltage Distribution Diagram in Schematic section of this notebook)

   a. Function
   b. Schematic (4-2677)

3. -5 volt supply

   (See Voltage Distribution Diagram in Schematic section of this notebook)

   a. Function
   b. Schematic (4-2677)

4. +15 volt supply

   (See Voltage Distribution Diagram in Schematic section of this notebook)

a. +15 volt supply

    1) Function

    2) Schematic (4-2677)

b. +13 volt supply

    1) Function

    2) Schematic (4-2677)

5. +325 volt supply

(See Voltage Distribution Diagram in Schematic section of this notebook)

a. Function

b. Schematic (4-2677)

6. -13.5 volt supply

(See Voltage Distribution Diagram in Schematic section of this notebook)

a. Function

b. Schematic (4-4319)

7. -13.5 (R) volt supply

(See Voltage Distribution Diagram in Schematic section of this notebook)

a. Function

b. Schematic (4-4319)

8. +18 volt supply

(See Voltage Distribution Diagram in Schematic section of this notebook)

a. Function

b. Schematic (4-2669)

9. -24 volt supply

(See Voltage Distribution Diagram in Schematic section of this notebook)

   a.   Function

   b.   Schematic (4-2668)

10. Reference (+256 volt) supply

(See Voltage Distribution Diagram in Schematic section of this notebook)

   a.   Function

   b.   Schematic (4-525)

11. -45 volt supply

(See Voltage Distribution Diagram in Schematic section of this notebook)

   a.   Function

   b.   Schematic (4-2677)

12. +35 volt supply

(See Voltage Distribution Diagram in Schematic section of this notebook)

   a.   +35 volt supply

        1.   Function

        2.   Schematic (4-2319)

   b.   +27 volt supply

        1.   Function

        2.   Schematic (4-2319)

XIV.   TROUBLESHOOTING PROBLEMS

For a list of troubleshooting problems, see Troubleshooting Problems section of this notebook.