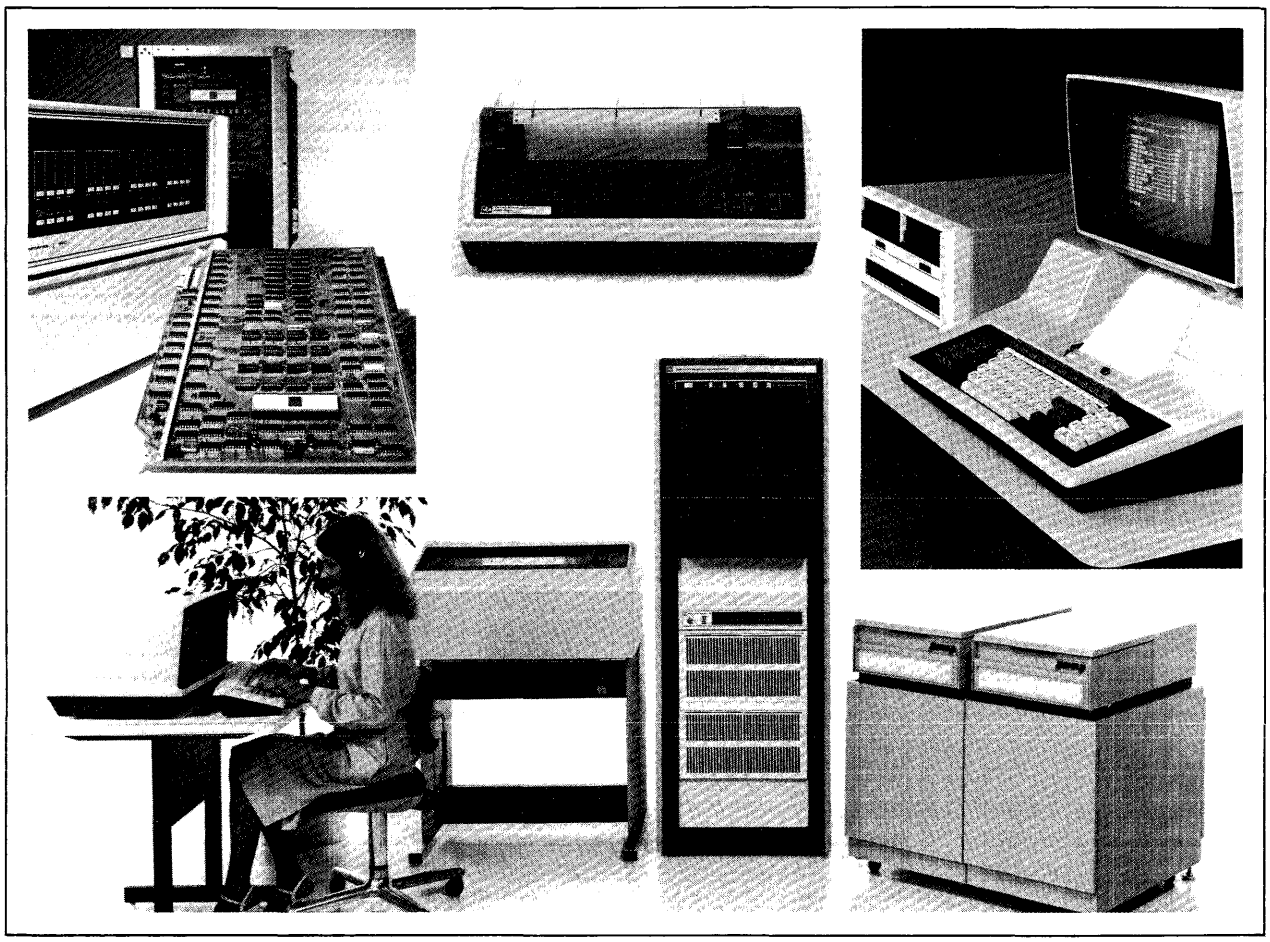
Model 990 Computer
Model 911 Video Display Terminal
Depot Maintenance Manual



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TEXAS INSTRUMENTS

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PREFACE

This manual provides maintenance instructions for the United States, European, and Japanese versions of the Texas Instruments Model 911 Video Display Terminal. It also provides theory of operation for the terminal. The manual consists of two sections and six appendixes:

I Theory of Operation – This section contains a detailed block diagram description of the Model 911 Video Display Terminal, describes the terminal's interfaces with the Model 990 Computer, and provides a discussion of the terminal's operation.

II Maintenance – This section provides troubleshooting and fault isolation procedures for the terminal.

A. United Kingdom Model – This appendix describes the United Kingdom version of the 911 Video Display Terminal (VDT) keyboard, including codes, modes, matrix, and special character set produced by it.

B. French Model – This appendix illustrates the French version of the 911 VDT keyboard, including codes, modes, matrix, and special character set produced by it.

C. German Model – This appendix illustrates the German version of the 911 VDT keyboard, including codes, modes, matrix, and special character set produced by it.

D. Swedish/Finnish Model – This appendix illustrates the Swedish/Finnish version of the 911 VDT keyboard, including codes, modes, matrix, and special character set produced by it.

E. Norwegian/Danish Model – This appendix illustrates the Norwegian/Danish version of the 911 VDT keyboard, including codes, modes, matrix, and special character set produced by it.

F. Japanese Katakana Model – This appendix illustrates the Japanese Katakana keyboard, including codes, modes, matrix, special character set, keyboard logic, and additional 128 eight-bit displayed character set produced by it.

Additional information related to the Model 911 Video Display Terminal may be found in the following documents:

Title	Part Number
990 Computer Family Systems Handbook	945250-9701
Model 990/4 Computer System Depot Maintenance Manual	945403-9701
Model 990/10 Computer System Depot Maintenance Manual	945404-9701

Title	Part Number
Model 990 Computer Family Maintenance Drawings	945421-9701
Model 990 Computer Programming Card	943440-9701
Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide	943441-9701
Model 990 Computer Model 911 Video Display Terminal Installation and Operation	945423-9701
Model 990 Computer Diagnostics Handbook	945400-9701

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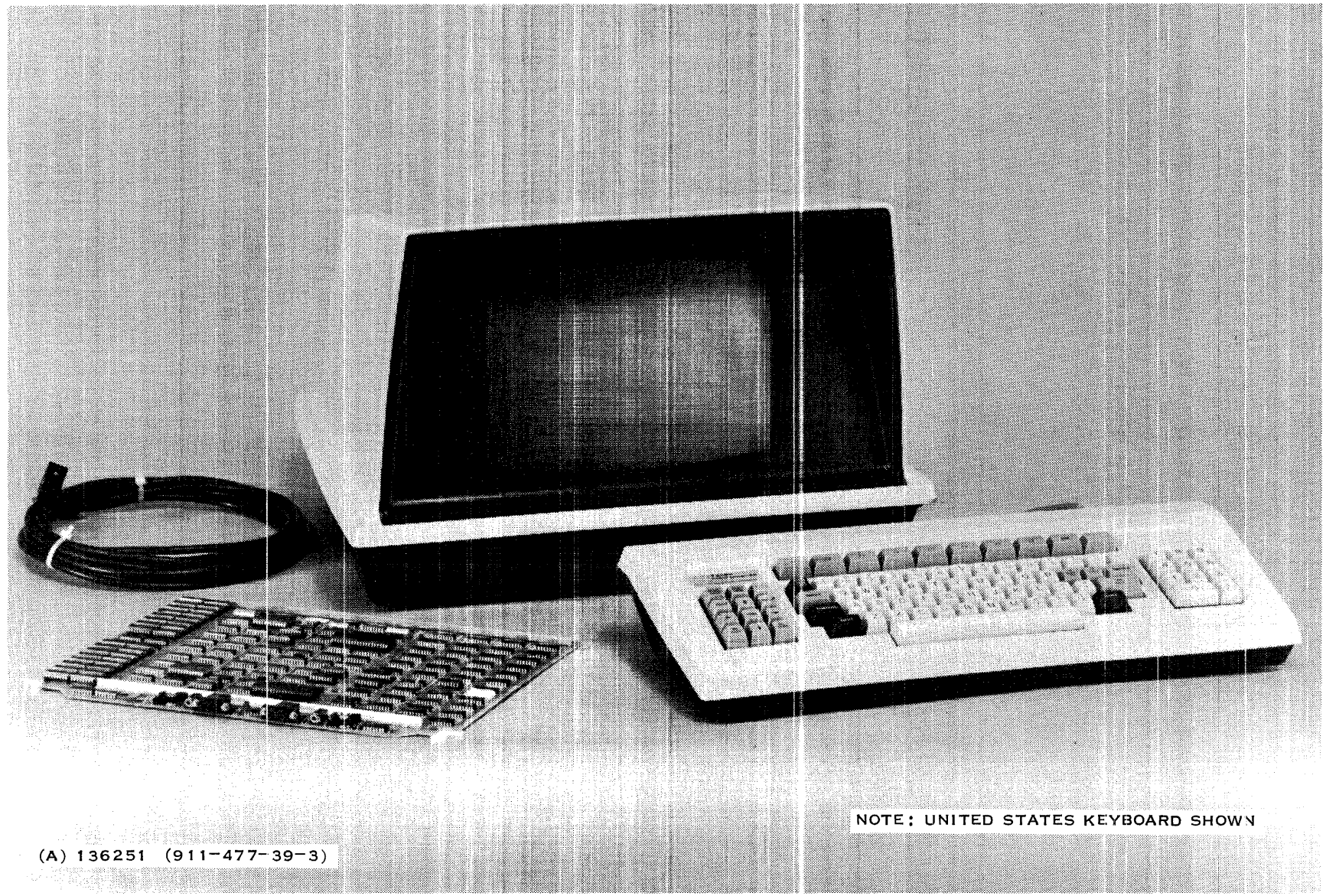

Figure 1-1. Basic Model 911 VDT Kit

SECTION I

THEORY OF OPERATION

1.1 GENERAL

This manual provides depot-level operation and maintenance information for the United States, European, and Japanese versions of the Texas Instruments Model 911 Video Display Terminal used with the Model 990 family of computers.

This section provides a discussion of the operation of the Model 911 Video Display Terminal. Functional theory is described, supported by block diagrams, circuit diagrams, flowcharts and timing diagrams. Detailed discussions of the terminal's circuitry and descriptions of the interfaces within the terminal and between the terminal and its host computer are also provided.

1.2 SYSTEM DESCRIPTION

The Model 911 Video Display Terminal consists of the following functional entities:

- Keyboard with associated electronics
- Keyboard and video data paths in display unit assembly
- Power supply
- CRT monitor
- Video display terminal (VDT) controller

The keyboard and keyboard electronics are contained in the keyboard assembly housing. The keyboard and video data paths in the display unit assembly, power supply, and CRT monitor are contained in the display unit cabinet. The VDT controller is in the main computer chassis or an expansion chassis and interfaces with the computer's Communications Register Unit (CRU). The display unit and the VDT controller are interconnected by an interface cable.

Figure 1-1 shows the components of a basic Model 911 VDT kit, and figure 1-2 is a block diagram of the terminal. Figure 1-3 shows the locations of the components located in the display unit cabinet. The following paragraphs describe each component of the terminal and function(s) of each component within the terminal subsystem.

1.2.1 KEYBOARD. The keyboard consists of keyswitch arrays on a printed wiring board (pwb) in the keyboard's own housing. The etched circuitry on the pwb forms an electrical contact matrix for the keyswitches. The keyboard also contains logic that performs the following functions:

- Detects key depression (switch closure).
- Allows multilevel encoding of data keys using the following mode keys: SHIFT, CONTROL, and UPPER CASE LOCK. The Japanese keyboard has two additional keys for alphanumeric or Katakana mode select.
- Produces an eight-bit code for each data key actuation.

- Produces new code for each data key actuation regardless of any keys already being held down.

- Makes the REPEAT key condition available at the interface.

The keyboard has a typewriter key cluster, a numeric pad, a cursor pad, and a function key array. Figure 1-4 illustrates the United States keyboard arrangement. All keys, except the REPEAT key, are designated as either mode or data keys. The mode keys determine which eight-bit code will be produced by each data key. The United States and European versions have three mode keys (SHIFT, CONTROL, and UPPER CASE LOCK) to select one of four codes for each data key. The Japanese Katakana keyboard has five mode keys to select one of six codes for various data keys. The mode keys alone do not cause an eight-bit code to be produced by the keyboard.

1.2.2 **VIDEO DISPLAY UNIT.** The video display unit consists of a CRT monitor and a power/logic pwb. The CRT monitor displays characters and symbols designated by software in the computer and produced by the VDT controller. The power/logic pwb provides the interface between the keyboard and the VDT controller; and all dc power required by the keyboard, CRT monitor, and the power/logic pwb. The following paragraphs describe the CRT monitor and the power/logic pwb.

1.2.2.1 **CRT Monitor.** The CRT monitor is a high-resolution monitor consisting of a CRT and a pwb. The pwb contains a video amplifier, a horizontal deflection amplifier, and a vertical deflection amplifier. The video pwb accepts the video signal, the horizontal drive signal, and the vertical sync signal from the power/logic pwb; and provides the signal shaping necessary to display the character designated by the data portion of the video signal on the CRT screen.

Video data, horizontal drive, and vertical sync are separated out of the composite video signal by the circuitry on the power/logic pwb and amplified separately. The horizontal drive component is provided to the logic in the keyboard data path to provide timing for data transfers.

The CRT monitor is capable of displaying 12 or 24 rows (as directed by the VDT controller) of 80 characters each. Characters are normally displayed on a dark background except at the cursor position. The cursor is displayed in reverse video format. (Reverse video format implies displaying a lighted background surrounding a dark character.)

The cursor appears on the CRT screen as a steady or blinking (software selected) high-intensity character block where the next character or symbol is to be entered. If the cursor is positioned over a displayed character, the character is displayed in reverse video format. If software directs cursor blinking, the cursor and character at that position blink in complementary video formats.

All information displayed on the CRT screen is originated by software executing in the computer. The actual video signals for displaying information on the screen are generated by character generation read-only memories (ROMs) on the VDT controller.

1.2.2.2 **Power/Logic PWB.** The power/logic pwb contains logic that provides the interfaces between the keyboard and the VDT controller and between the VDT controller and the CRT monitor. The power/logic pwb also contains three power supply circuits that provide +5 Vdc to the keyboard, and -12 Vdc and +15 Vdc to the keyboard and video data path logic on the pwb and the CRT monitor.

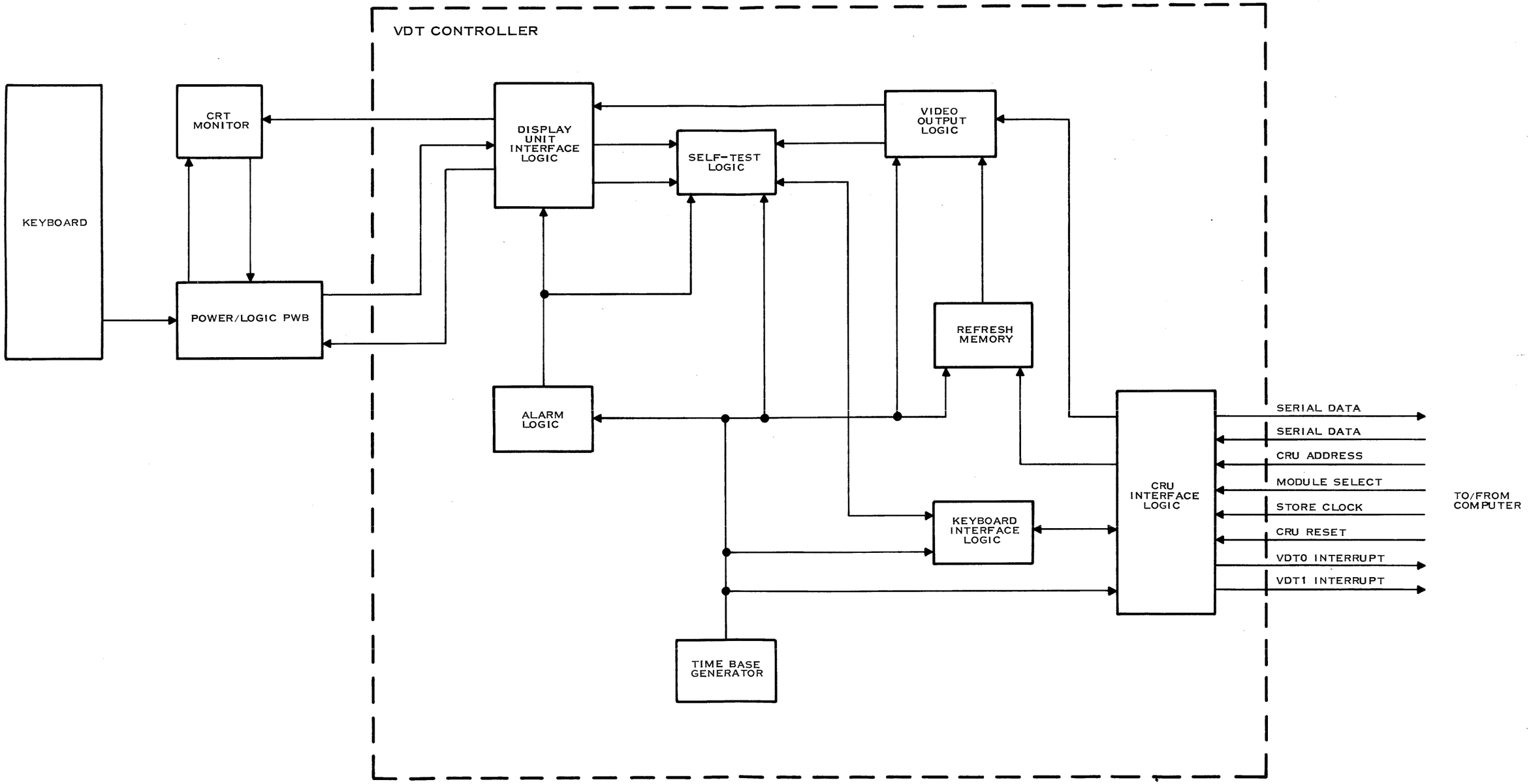

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Figure 1-2. Model 911 VDT Block Diagram

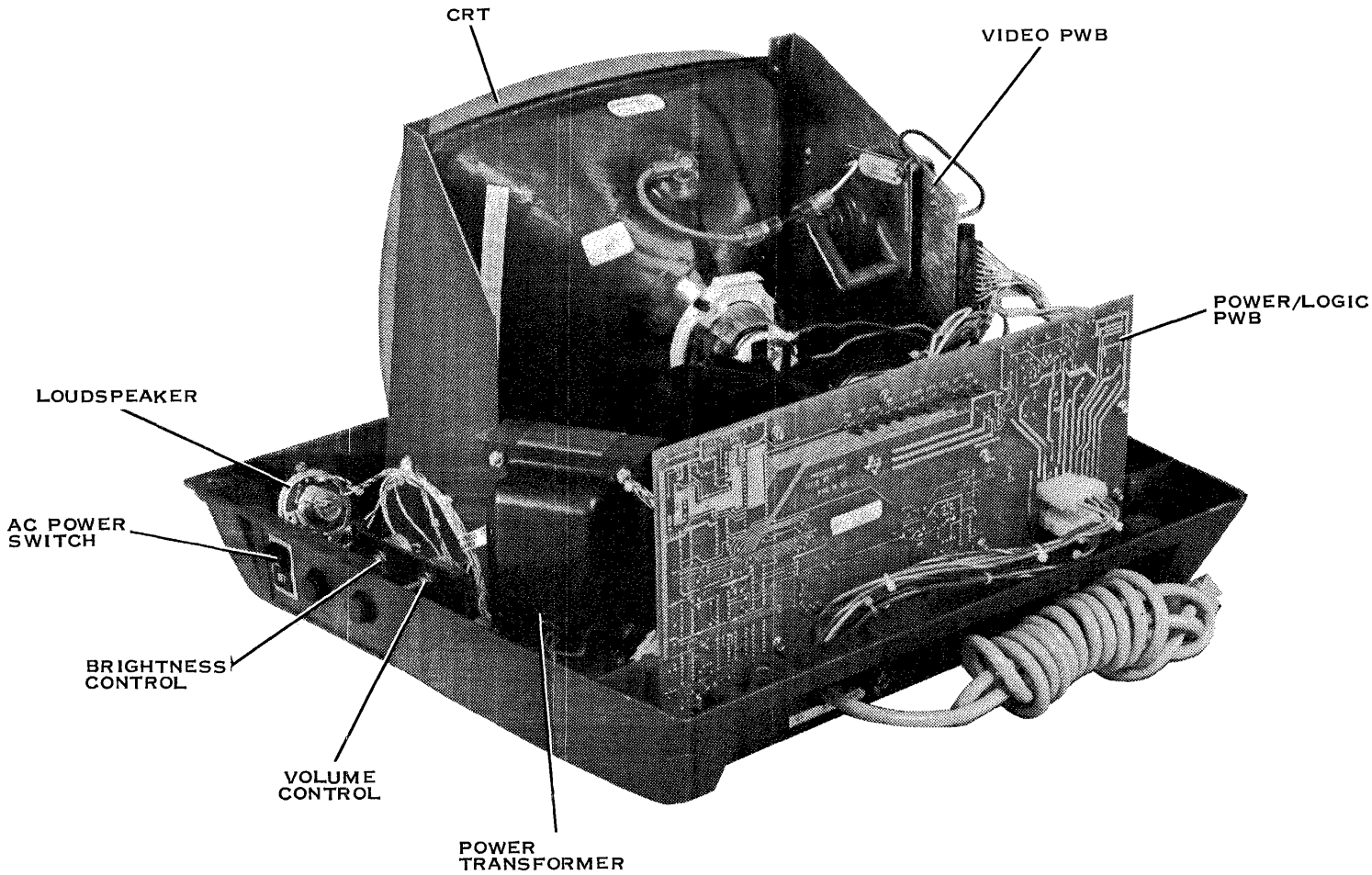

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Figure 1-3. Model 911 VDT Component Locations

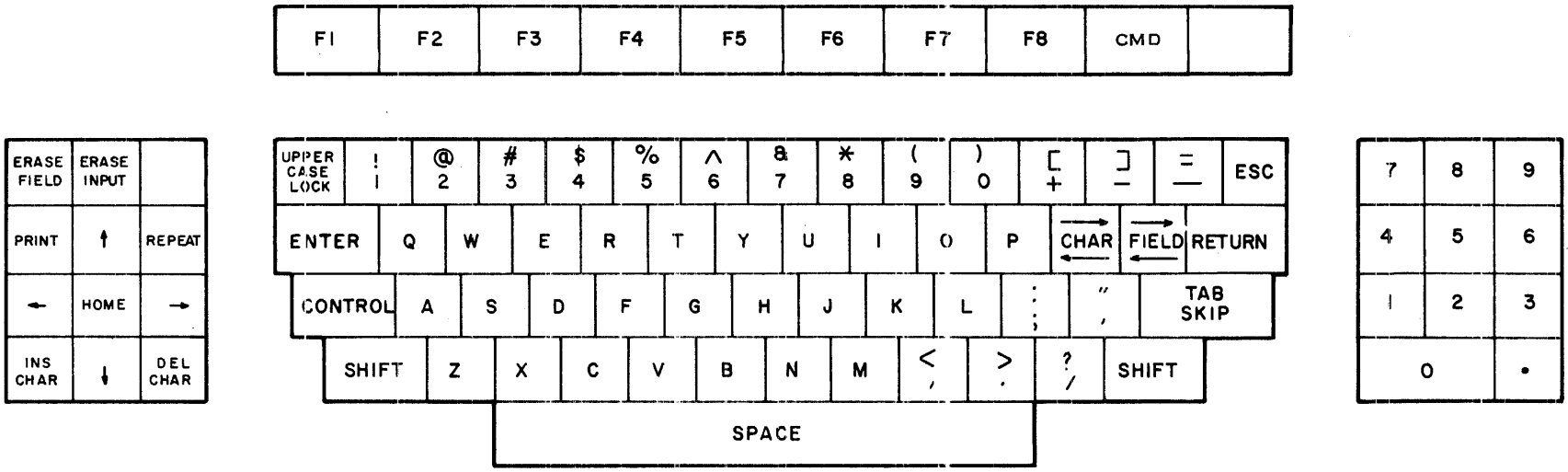


Figure 1-4. United States Model 911 VDT Standard Keyboard

Keyboard and Video Data Path Logic. The keyboard and video data path logic on the power/logic pwb performs the following functions:

- Latches keyboard data from the keyboard and holds the last code entered from the keyboard until a new code is entered
- Adds one start bit, one stop bit, and one parity bit to the keyboard data code
- Serializes the keyboard data code and transmits the serial code to the VDT controller
- Converts the serial keyboard data into an eight-bit parallel code and a parity error indicator bit and displays the bits with nine light-emitting diodes (LEDs) on the rear of the display unit housing
- Repeatedly produces the 11-bit serial code for any data key actuated with the REPEAT key held
- Produces an audio signal to drive a loudspeaker in the display unit cabinet in response to a software-produced alarm condition
- Provides amplifier for monitoring audio signals from a modem.
- Buffers composite video signal from VDT controller before providing the signal to other circuitry
- Separates video, horizontal drive, and vertical synchronization components from the composite video signal from VDT controller
- Provides video data, horizontal drive, and vertical synchronization signals to drive CRT monitor circuitry
- Compensates for cable lengths shorter or longer than approximately 1000 feet (304.8 metres) with a switch-selectable-gain video amplifier that provides its low gain for short cables and its high gain for long cables.

Power Supplies. There are three series-regulated dc power supply circuits on the power/logic pwb. These supplies are provided with alternating current (ac) by a multiple-secondary power transformer mounted in the base of the display unit cabinet. The power supplies provide +5 Vdc to the keyboard, and -12 Vdc and +15 Vdc to the CRT monitor's video pwb, keyboard, and video data path logic on the power/logic pwb.

1.2.3 VDT CONTROLLER. The VDT controller is implemented on a pwb that occupies a full slot in either a main or expansion computer chassis. The pwb contains the logic for one (always) or two (optionally) autonomous controllers, and supports as many keyboard/display unit combinations as there are controllers on the pwb. When two controllers reside on a single pwb, the controllers share the same CRU interface and time-base generator.

In this manual, the discussion concerns itself with the primary controller that is always present. The discussion is valid for the second controller, if present. On the logic diagrams for the VDT controller, logic for two controllers is included with signatures for the second controller denoted by an asterisk (*) as the last character of each signature.

There are two VDT controllers available with the Model 911 VDT. The United States and European controller is part number 946076; the Japanese Katakana controller is part number 2263490.

The VDT controller performs the following functions:

- Provides interfaces between keyboard and computer, and between computer and CRT monitor.
- Generates (via ROMs) character codes for 96 standard display symbols, including uppercase and lowercase Gothic alphabet characters, numeric characters, and special symbols (+, -, ;, etc.). An additional 64 Katakana characters are produced by the Japanese version.
- Provides storage for as many as 2048 (2K) eight-bit character codes originated by the computer for display on the CRT screen (1024 for 960-character version).
- Transmits contents of refresh memory to CRT screen to refresh display 50 or 60 times per second, depending upon ac input.
- Loops back computer-supplied character code and cursor address, video data, horizontal sync, vertical sync, and software alarm enable (audio enable) to output multiplexers for examination by diagnostic software.

The interface between the computer and the VDT controller is a standard 990 CRU interface consisting of a serial output data line and associated output data strobe (STORECLOCK–), four CRU address lines that specify to the VDT controller which of its 32 internal latches and/or registers should accept the serial data or control bit, a module select signal that indicates that the VDT controller has been selected by the computer as the destination device for the CRU transfer, a serial input data line, and a device interrupt line.

The computer provides the module select signal, four-bit CRU address, and strobe signal for each bit of information on the data line (CRUBITOUT) to the VDT controller. The controller responds to the module select signal by decoding each four-bit CRU address and either latching the accompanying bit of information in the appropriate latch or register, or responding to strobe commands (Increment Cursor, Reset Keyboard Interrupt, etc.).

During entry of data from the keyboard into the computer, the VDT controller accepts the 11-bit serial keyboard code from the power/logic pwb. The VDT controller removes the start, parity and stop bits from the data code and gates the resulting eight-bit data-only code to an output multiplexer. The controller then issues an interrupt to notify the computer that keyboard data is ready to be transferred to the computer. When the computer has accepted the data from the keyboard, it issues Keyboard Acknowledge to reset keyboard data ready.

During a data retrieval operation (initiated by the keyboard), the computer provides the VDT controller with eight bits of character data (generated in computer memory) over the serial data line (CRUBITOUT). This information determines what is to be displayed on the CRT screen, and whether the displayed information is to be displayed normally or at high intensity (low-intensity symbols are displayed with circular dots, and high-intensity symbols with elongated dots). The computer also provides display and cursor enable signals, and an 11-bit cursor address, all over the same serial output data line. The cursor address specifies the position on the screen where the information is to be displayed and the location in the VDT controller's refresh memory where the information is to be stored. The VDT controller continually routes the contents of refresh memory to the CRT screen to maintain the screen images.

After the computer has transmitted all of the data and address information to the VDT controller, the computer issues a Write Data Strobe on the data line (with module select, four-bit CRU address, and clock). The VDT controller responds by storing the screen data code into its refresh memory at the cursor address provided by the computer. The VDT controller also encodes the computer-provided data into dot patterns to be transmitted to the CRT monitor for display. For each character to be displayed on the CRT screen, the VDT controller produces 10 (16 for 960-character display) seven-dot codes (one for each of the 10 scan lines required for each character block on the screen). The controller generates timing signals to provide horizontal and vertical synchronization signals for the CRT monitor and superimposes them on the video data signal to produce a composite video signal for the CRT monitor.

During normal typing operations where screen data is repeatedly transferred from the keyboard to the computer and back to the CRT monitor, the computer provides the VDT controller with the initial cursor address and a control bit that causes the VDT controller to increment the cursor address for each succeeding transfer. A cursor address counter in the VDT controller performs the incrementing so that all characters are transmitted in the proper order and stored in refresh memory in consecutive locations. For operations other than transmission of information for display in consecutive locations, the computer provides an 11-bit cursor address for each character to be displayed.

The VDT controller provides a software alarm function for the computer. The controller produces a signal that enables an oscillator in the display unit cabinet in response to CRU output bit E_{16} (bit F_{16} = 1) from the computer (transferred over the serial output data line as previously described). The signal can be used to indicate the entry of illegal codes and other software violations.

The computer can direct the VDT controller to enter the self-test mode. In the self-test mode, the computer monitors the root signals of outputs to the VDT and simulates keyboard input from the VDT. Diagnostic software examines these signals to verify timing and for fault isolation. The computer accomplishes this operation by setting five control bits on the controller interface to direct the VDT controller to return simulated keyboard data, video, horizontal sync, vertical sync, and audio signals. Simulated keyboard data is one of four patterns as determined by two control bits. Only one of the four inputs (video, horizontal sync, vertical sync or audio) is available during self-test and is selected by two control bits.

1.3 INTERFACE DESCRIPTIONS

The following paragraphs describe the interfaces between the VDT controller and the computer, the keyboard and the power/logic pwb, the power/logic pwb and the VDT controller, and the power/logic pwb and the CRT monitor.

1.3.1 VDT CONTROLLER/COMPUTER INTERFACE. The interface between the VDT controller and the computer is illustrated in figure 1-5. The interface is the serial CRU interface of the Model 990 family of computers. The CRU interface provides for up to 4096 directly addressable input bits and up to 4096 directly addressable output bits. The VDT controller/computer interface utilizes 16 directly addressable bits each for input and output operations for each controller resident on the VDT controller pwb. Computer operations can address the bits individually or in fields of from one to 16 bits. The computer instructions that drive the CRU interface can set, reset, or test any bit on the interface or move data between computer memory and the CRU data fields. These 16 directly addressable bits are multiplexed to effectively provide 32 input and 32 output signals.

CRU operations can be divided into two broad categories: those involving a single control bit transfer and those requiring input or output of multiple data or status bits.

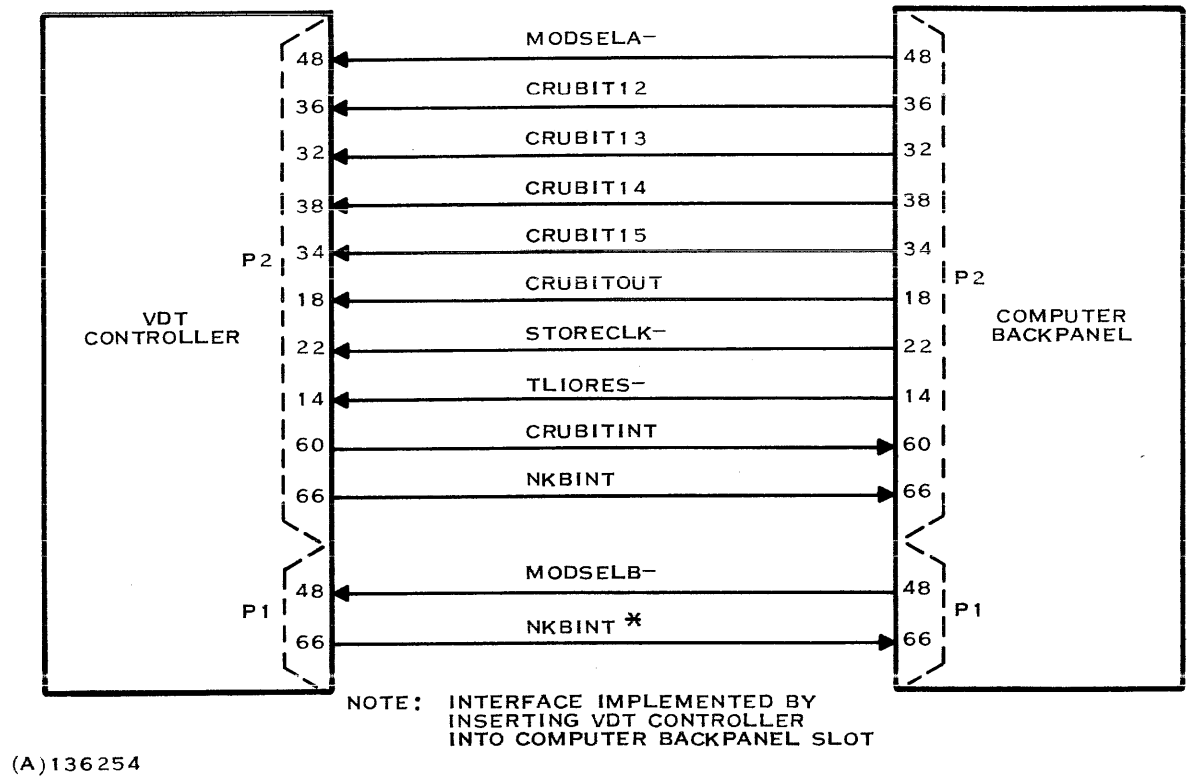


Figure 1-5. Model 911 VDT Controller/Computer Interface Signals

1.3.1.1 **Single-Bit Operations.** Single-bit operations typically involve the computer's setting a control bit or sampling a status bit. When a status bit is set, the computer responds by setting a control bit or by transferring to another set of instructions.

1.3.1.2 **Multiple-Bit Operations.** Multiple-bit operations typically involve a data input device such as the display keyboard, or an output device such as the terminal's CRT monitor. An interrupt from the terminal causes the computer to perform a store communications register (STCR) instruction to read keyboard data from the terminal and store it into memory. Similarly, to output data to the display, the computer executes a load communications register (LDCR) instruction to fetch data from memory and transfer the data to the VDT controller.

1.3.1.3 **Addressing.** The computer produces a 12-bit address as shown in figure 1-6 to address up to 4096 individual bits. The 12-bit address is used for both input and output operations. Bits 4 through 6 address a particular chassis in the system, and bits 7 through 11 are encoded to produce the module select signals that address a particular half slot within the chassis. Bits 12 through 15 select one of 16 possible bits from the selected module. The module select signals (one for each half slot in the chassis) and bits 12 through 15 of the address are provided to each CRU interface (half slot) implemented in the chassis. The functions of the module select signal and bits 12 through 15 of the address are explained in more detail in the discussion of the software interface between the VDT controller and the computer.

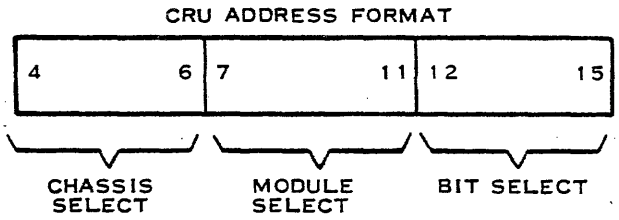


Figure 1-6. CRU 12-Bit Addressing Scheme

1.3.1.4 **Interface Timing.** The computer conforms to minimum CRU input and output timing restrictions as defined by figures 1-7 and 1-8. Figure 1-7 illustrates the timing sequence for an LDCR R1,2 instruction followed by an SBZ 15 instruction. Figure 1-8 illustrates the timing sequence for an STCR R1,2 instruction followed by TB 15. Minimum timing restrictions are the same for both instructions.

Timing restrictions shown in figure 1-7 are based on a clock period (STORECLOCK–) of 250 nanoseconds.

CRU addresses and module selects are defined only during the execution of CRU input or CRU output instructions. CRUBITOUT and STORECLOCK– are held high when the processor is not executing a CRU output instruction. The CRU device (VDT controller) clocks the CRUBITOUT line using the positive edge of the STORECLOCK– pulse.

CRUBITINT is defined only during the execution of a CRU input instruction. The VDT controller decodes the CRU address and places the appropriate data on the CRUBITINT line. The VDT controller drives the CRUBITINT line with a three-state gate that is enabled only when the VDT controller is selected by the module select signal.

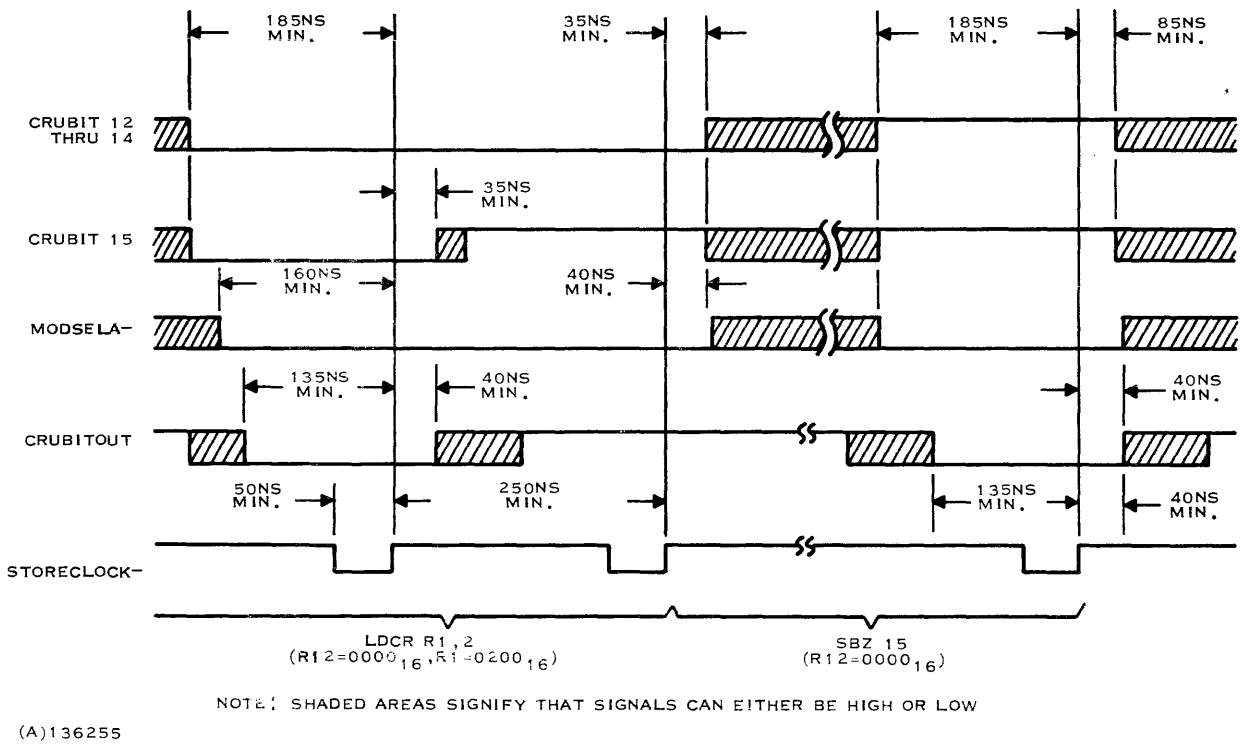


Figure 1-7. CRU Minimum Output Timing Restrictions

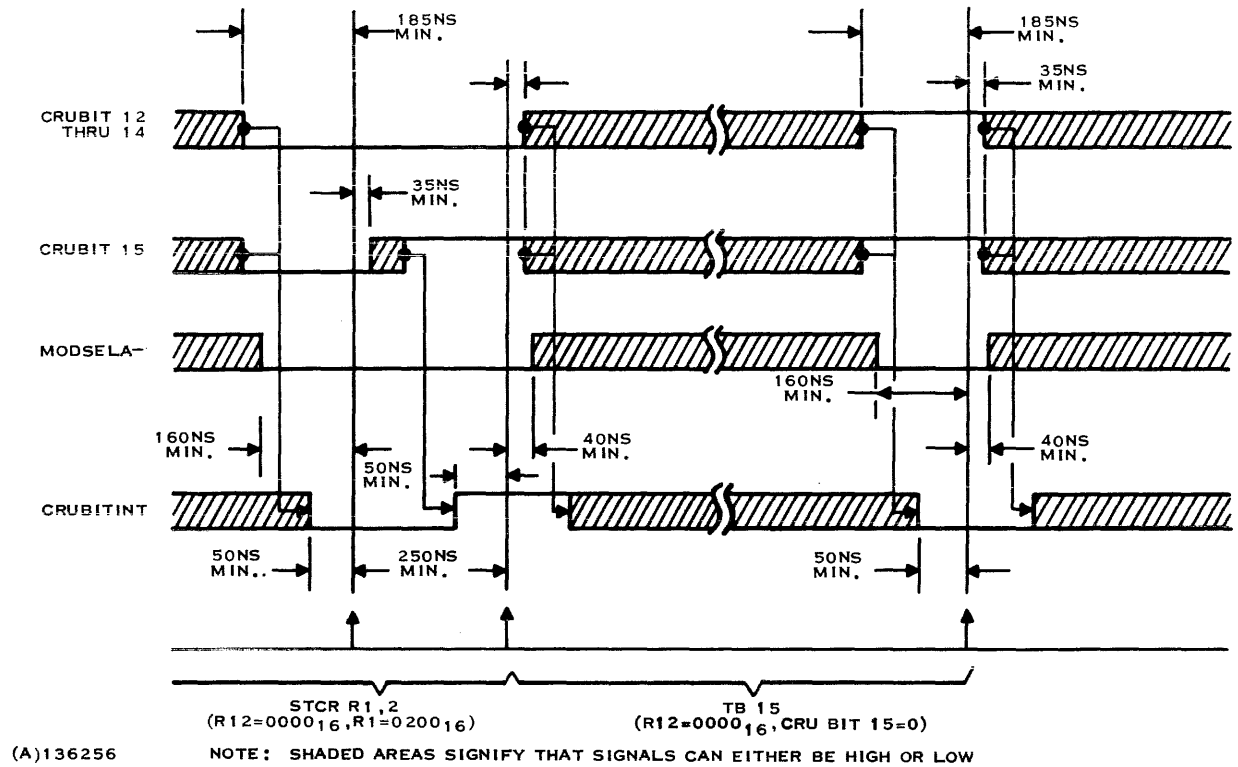


Figure 1-8. CRU Minimum Input Timing Restrictions

1.3.1.5 Hardware Interface Signals. Figure 1-5 depicts the 12 signal lines that convey all the information exchanged by the VDT controller and the computer. Following are descriptions of the signal functions:

- Module Select (MODSELA– and MODSELB–) – The module select signals are low-active signals decoded from the CRU address by the CPU in a main chassis or a CRU buffer board in an expansion chassis. Each half-slot connector in the chassis contains one unique module select line that determines which pwb in the chassis has been selected for a CRU input or output data transfer. Since the VDT controller occupies two half slots, two module select lines are available. These two module select signals are used to implement the dual-terminal VDT controller option (two autonomous controllers on one pwb). MODSELA– enables the logic for a single-terminal VDT controller, or for VDT 0 of a dual-terminal VDT controller. MODSELB– enables the logic for the second controller (VDT 1) of a dual-terminal controller.

- CRU Address Bits (CRUBIT,12-15) – The CRU address bits are the four high-active bit select signals shown in figure 1-6. CRUBIT,12-15 provide 16 encoded hexadecimal bit addresses (0 through F_{16}) to the VDT controller. The value of CRUBITOUT when CRUBIT,12-15 = F_{16} is used by the computer to effect a 32-bit interface with the VDT controller using only 16 addresses. If CRUBITOUT = 0 when CRUBIT,12-15 = F_{16}, the remaining 15 bits addressed by CRUBIT,12-15 have different meanings than if CRUBITOUT = 1 when CRUBIT,12-15 = F_{16}.

- CRU Output Data (CRUBITOUT) – CRUBITOUT is the high-active serial output of the computer. CRUBITOUT provides the 32 bits of information shown in figure 1-9 as the bits addressed by CRUBIT,12-15. Descriptions of the 32 bits shown in figure 1-9 are found in paragraph 1.3.1.6.

- Store Clock (STORECLOCK–) – STORECLOCK– is the low-active clock produced by the computer that strobes each bit contained by CRUBITOUT to the address specified by CRUBIT,12-15 at the positive-going edge of STORECLK–. STORECLOCK– has a pulse width of 50 nanoseconds (nominal) and a period of 250 nanoseconds (nominal).

- CRU Input Data (CRUBITINT) – CRUBITINT is the high-active serial output from the VDT controller to the computer. CRUBITINT provides the 32 bits of information shown in figure 1-10 as the bits addressed by CRUBIT,12-15.

- TILINE I/O Reset (TLIORES–) – TLIORES– is the low-active system reset signal that resets all VDT controller devices in response to an RSET instruction or during application of power to the system. TLIORES– keeps all connected devices reset until dc power to the system is up and stable.

- Terminal Interrupts (NKBINT and NKBINT*) – NKBINT and NKBINT* are the low-active device interrupt signals for the primary (VDT 0) and optional (VDT 1) controllers, respectively. Each controller produces its interrupt each time a character code is received from the keyboard, then awaits the computer's reply, Keyboard Acknowledge.

1.3.1.6 Software Interface. Figures 1-9 and 1-10 illustrate the 32 output and 32 input bits, respectively, designated by the system processor with CRUBIT,12-15. The descriptions of the bit assignments follow.

NOTE

For the following discussions, it is assumed that CRUBITOUT and CRUBIT,12-15 have set CRU output bit F_{16} to 0 prior to addressing the bit under discussion.

Display Memory Write Data (CRU Output Bits 0-7_{16} With Output Bit 9_{16} = 0). These eight bits represent a character code to be displayed on the CRT screen when Write Data Strobe (CRU output bit 8_{16} with output bit F_{16} = 0) is issued. The VDT controller latches Display Memory Write Data and uses it to load refresh memory. Characters read from the displayable portion of refresh memory produce the video dot codes that cause the symbols to be displayed on the CRT screen. On the United States and European controller versions, bits 0-6_{16} represent a seven-bit character, and bit 7 (most significant bit) is used to select character intensity. The Japanese controller has 256 characters (Katakana and alphanumeric), and the dual intensity feature is not active, since bits 0 through 7 are required to describe each character.

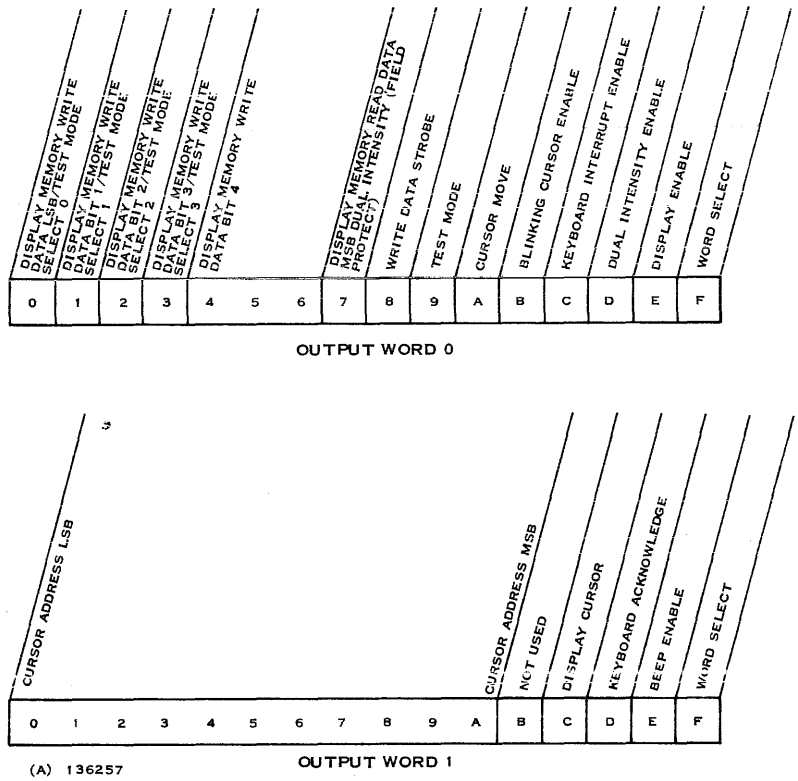


Figure 1-9. CRU Output Bit Assignments for Model 911 Video Display Terminal

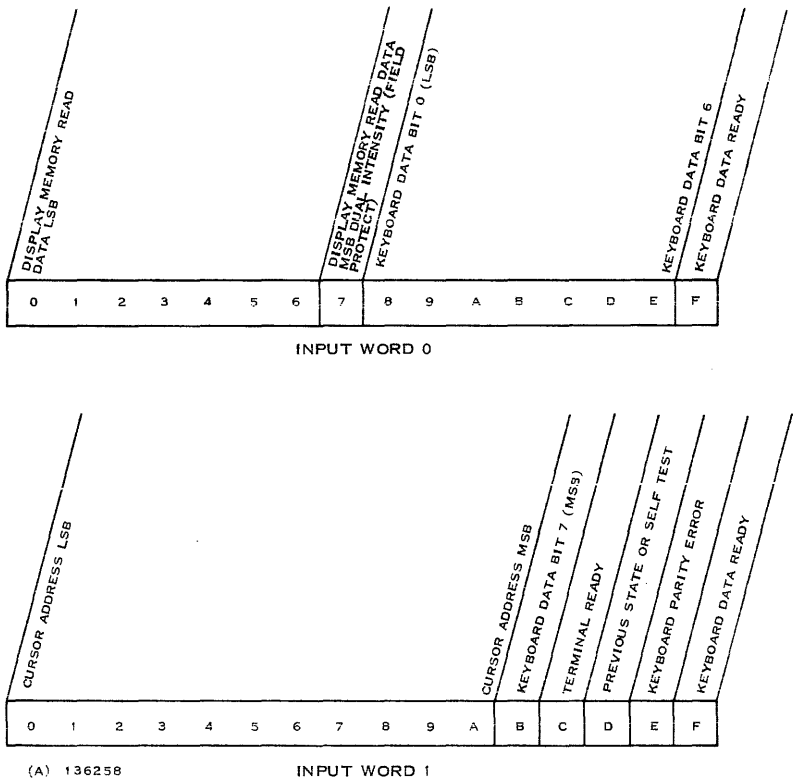


Figure 1-10. CRU Input Assignments for Model 911 Video Display Terminal

Test Mode Select (CRU Output Bits 0-3_{16} With Output Bit 9_{16} = 1). When Test Mode (CRU output bit 9_{16} with output bit F_{16} = 0) is logic 1, CRU output bits 0 and 1 select one of four test inputs for the VDT controller's built-in test logic. The selected input is read as the CRU input signal Previous State or Self Test (CRU output bit D_{16} with output bit F_{16} = 1). Table 1-1 shows the characteristics of the test inputs. Bits 2 and 3 program the parallel input to the Universal Asynchronous Receiver/Transmitter (UART) transmitter section. Transmitter serial data is routed, during self-test, through the built-in test logic multiplexer to the UART to simulate keyboard data. The UART converts the serial code into parallel data for the input multiplexer that provides serial data to the computer. Table 1-2 relates the state of the control bits to the character generated by the UART.

Dual Intensity (CRU Output Bit 7_{16}). This bit is used by the VDT controller as the eighth bit of data loaded into refresh memory and provided to the character generator ROMs to produce the dot code for the character to be displayed on the screen. On United States and European versions, when set to 0, or if Dual Intensity is not enabled (CRU output bit D_{16} = 1 with output F_{16} = 0), Dual Intensity directs that the character with which it is loaded be displayed at high intensity. Graphics characters are always displayed at low intensity. When Dual Intensity is enabled, the character dual intensity attribute determines the intensity of each alphanumeric character. Dual Intensity may be used as a software flag or to permit use of nondisplayed memory for storage of byte-oriented data. Protected fields are typically displayed at low intensity. On the Japanese version this bit is data, and software must not activate the dual intensity feature.

Table 1-1. Model 911 VDT Built-In Test Signals With CRU Output Bit 9 = 1 and CRU Output Bit F_{16} = 0

Input Signal	CRU Bit 0	CRU Bit 1	Signal Characteristics
Video	0	0	Depends upon data previously stored in memory. Video is 0 if all refresh memory locations are set to 20_{16} (space, or blank, character). Video is logic 1 if all refresh memory locations are set to 19_{16} (intensified character space).
Horizontal Sync	1	0	Frequency = 15.720 KHz, period = 63.5 μsec. Signal is high for 12 μsec.
Vertical Sync	0	1	Frequency determined by control ROM. Frequency is 50 Hz or 60 Hz to match ac power input to computer and terminal. Period @ 50 Hz = 20 msec Period @ 60 Hz = 16.6 msec Signal = 1 for 192 μsec.
Audio	1	1	Normally low. High when audio alarm is enabled by Beep Enable (CRU output bit E_{16} with CRU output bit F_{16} = 1). Duration @ 50 Hz = 280-320 msec Duration @ 60 Hz = 230-270 msec

Table 1-2. Model 911 VDT Built-In Test Keyboard Simulation Data

Test Input Select		Keyboard Data	CRU Data Bits		Memory Image	
CRU Bits		KBDQ or KBDQ*	Word 0	Word 1	MSB	LSB
2	3	01234567	89ABCDE	B		
0	0	00000000	0000 000	0	00000000	
0	1	11001100	1100 110	0	00110011	
1	0	00110011	0011 001	1	11001100	
1	1	11111111	1111 111	1	11111111	

Write Data Strobe (CRU Output Bit 8_{16}). Address Bit 8_{16} (its value makes no difference) directs memory control logic on the VDT controller to load Display Memory Write Data and Dual Intensity into refresh memory at the present cursor address.

Test Mode (CRU Output Bit 9_{16}). When Test Mode is set to 1, the VDT controller is placed in the self-test mode. In the self-test mode, the computer can examine the simulated keyboard data code from the built-in test UART (transmitter), and the selected test parameter (Video, Horizontal Sync, Vertical Sync, or Audio) input on the Previous State or Self–Test bit as described under Test Mode Select.

Cursor Move (CRU Output Bit A_{16}). When Cursor Move is set to 0, the cursor address is the cursor address register is incremented. When set to 1, Cursor Move decrements the cursor address in the cursor address register. During the transfer of character data to be displayed in consecutive locations on the CRT screen, the system processor supplies the initial cursor address and increments that address for each successive transfer. Cursor Move thus allows computer software to move the cursor on the screen by a single-bit transfer.

Blinking Cursor Enable (CRU Output Bit B_{16}). When set to 1 and enabled by Display Cursor (CRU output bit C_{16} with output bit F_{16} = 0), Blinking Cursor Enable causes the cursor to blink on and off at two hertz. If Blinking Cursor Enable is set to 0, the blinking function is disabled, and the cursor is displayed (if enabled) continuously. Power-up reset disables cursor blinking.

Keyboard Interrupt Enable (CRU Output Bit C_{16}). When set to 1, the VDT controller keyboard data path logic is permitted to send the Terminal Interrupt (NKBINT or NKBINT*) as an indication that keyboard data has been latched by the VDT controller (Keyboard Data Ready). When set to 0, Keyboard Interrupt Enable masks the interrupt. Keyboard Interrupt Enable is set to 0 during application of power to the system.

Dual Intensity Enable (CRU Output Bit D_{16}). Dual Intensity Enable, when set to 1, enables the VDT controller to interpret Dual Intensity as previously indicated. This bit should not be enabled on the Japanese controller.

Display Enable (CRU Output Bit E_{16}). This bit, when set to 1, enables video output logic on the VDT controller to drive out the character video to the CRT monitor. When Display Enable is 0, as it is after power application to the computer, video output logic is disabled, and the CRT screen is blanked. Synchronization signals to the CRT monitor are not blanked, so a stable raster should always be present.

Word Select (CRU Output Bit F_{16}). Word select determines the interpretation attached to the computer's output, CRUBITOUT, and input, CRUBITINT, by the VDT controller. When Word Select = 0, the VDT controller's CRU interface logic enables a different set of latches and registers to accept or output data for the other 15 bits addressed by CRUBIT,12-15 than are enabled when Word Select = 1.

NOTE

For the following discussions, it is assumed that CRUBITOUT and CRUBIT,12-15 have set CRU output bit F_{16} to 1 prior to addressing the bit under discussion.

Cursor Address (CRU Output Bits 0-A_{16}). These 11 bits define a cursor address for loading refresh memory and determining the location on the CRT screen where a character is to be displayed. Cursor Address defines hexadecimal addresses from 0 through $7FF_{16}$. The memory on a "960-character" controller has 1024 locations (0-$3FF_{16}$). Only addresses from 0 through $3BF_{16}$ are displayable on a "960-character screen", and addresses from 0 through $77F_{16}$ on a "1920-character screen". The addresses for which no data is displayed can be used by software. If the cursor address specifies a nondisplayable location, the cursor is not visible.

Addressing bit A_{16} of the cursor address is the VDT controller's indication that a new cursor address is to be loaded; therefore, this bit must always be output during alteration of the cursor address.

Bit 9_{16} is the most significant bit of the cursor address for a "960-character" display, but as mentioned previously, bit A_{16} must also be output. CRU output bit B is not used.

Display Cursor (CRU Output Bit C_{16}). When set to 1, Display Cursor enables the cursor to be displayed on the CRT screen as described under Blinking Cursor Enable. Display Cursor is set to 0 during application of power to the system.

Keyboard Acknowledge (CRU Output Bit D_{16}). Keyboard Acknowledge is the computer's response to the VDT controller's Keyboard Interrupt signal. When addressed (its value makes no difference), Keyboard Acknowledge resets Keyboard Data Ready (CRU input bit F_{16}), Keyboard Parity Error (CRU input bit E_{16} with output bit F_{16} = 1), and the controller's device interrupt, NKBINT.

Beep Enable (CRU Output Bit E_{16}). This bit, when addressed by the computer (its value makes no difference), causes the VDT controller's audio alarm logic to produce a 0.3-second (nominal) oscillator enable signal. This enable turns on the 2-kilohertz tone oscillator driving the loudspeaker in the display unit housing.

Word Select (CRU Output Bit F_{16}). Word Select determines the interpretation attached to the computer's output, CRUBITOUT, and input, CRUBITINT, by the VDT controller. When Word Select = 0, the VDT controller's CRU interface logic enables a different set of latches and registers to accept or output data for the other 15 bits addressed by CRUBIT,12-15 than are enabled when Word Select = 1.

NOTE

For the following discussions, it is assumed that CRUBITOUT and CRUBIT 12-15 have set CRU output bit F_{16} to 0 prior to addressing the bit under discussion.

Display Memory Read Data (CRU Input Bits 0-7_{16}). These eight bits are the data stored in refresh memory at the current cursor address. These bits represent an eight-bit character or a seven-bit character with an intensity attribute.

Display Memory Read Data (CRU Input Bit 7_{16}). This bit may indicate whether the character or symbol represented by Display Memory Read Data (bits 0 through 6) is displayed at high or low intensity. High intensity is indicated by the bits being equal to zero, and normally represents unprotected data. On the Japanese controller, this bit represents data; dual intensity is not allowed.

Keyboard Data (CRU Input Bits 8-E_{16}). In the normal mode, Keyboard Data are the first seven bits (lsb through 6) of the eight-bit data code from the keyboard. In the self-test mode, Keyboard Data are the first seven bits of the simulated keyboard code selected by the computer for diagnostic purposes. Keyboard Data are valid only when Keyboard Data Ready (CRU input bit F_{16}) is high.

Keyboard Data Ready (CRU Input Bit F_{16}). Keyboard Data Ready is set to 1 by the VDT controller when Keyboard Data is ready to be addressed and read by the computer. Keyboard Data Ready is reset by Keyboard Acknowledge.

NOTE

For the following discussions, it is assumed that CRUBITOUT and CRUBIT,12-15 have set CRU output bit F_{16} to 1 prior to addressing the bit under discussion.

Cursor Address (CRU Input Bits 0-A_{16}). These 11 bits are the current cursor address. This is the refresh memory address that is altered if a Write Data Strobe is issued. The address also defines the screen position where the cursor is displayed, when enabled. Bit A_{16} is always 0 for the 960-character display.

Keyboard Data MSB (CRU Input Bit B_{16}). This bit is the most significant bit of either the keyboard code from the keyboard or the simulated keyboard code during the self-test mode.

Terminal Ready (CRU Input Bit C_{16}). Terminal Ready, in the normal mode, indicates the status of the terminal subsystem. Terminal Ready = 0 indicates that the terminal is operational. Terminal Ready = 1 indicates one of the following conditions:

- No power to display assembly
- Interconnection cable disconnected or broken
- Self-test mode.

Previous State or Self-Test (CRU Input Bit D_{16}). In normal mode, this bit indicates the state of the Word Select logic prior to the last transfer to word 1 (selected by CRU output bit F_{16} = 1). Logic 0 indicates that word 0 was last selected; logic 1 indicates that word 1 was last selected. In the self-test mode, Previous State or Self-Test carries the information listed in table 1-1.

The previous state interpretation permits interrupt-driven software to determine the controller state prior to a keyboard interrupt. This permits the controller to process the interrupt and restore previous conditions.

Keyboard Parity Error (CRU Input Bit E_{16}). When Keyboard Parity Error = 1, it indicates that a parity error existed during the last keyboard data transmission. Keyboard Parity Error is valid only if Keyboard Data Ready (CRU Input Bit F_{16}) = 1. Keyboard Acknowledge (CRU output bit D_{16} with CRU output bit F_{16} = 1) resets Keyboard Parity Error.

Keyboard Data Ready (CRU Input Bit F_{16}). Keyboard Data Ready is set to 1 by the VDT controller when Keyboard Data is ready to be addressed and read by the computer. Keyboard Data Ready is reset by Keyboard Acknowledge.

1.3.2 **KEYBOARD-TO-POWER/LOGIC PWB INTERFACE.** The interface between the keyboard and the power/logic pwb in the display unit cabinet is implemented by an interconnection cable that connects directly to the power/logic pwb inside the display unit cabinet. Figure 1-11 illustrates the interface, and the following paragraphs describe the signals on the interface.

1.3.2.1 **Keyboard Data (KBDT,1-8).** Keyboard Data are the high-active eight-bit codes produced by the keyboard encoder for each data key on the keyboard.

1.3.2.2 **Keyboard Data Strobe (KBSIN–).** Keyboard Data Strobe is the low-active 20-microsecond (nominal) strobe signal produced by the keyboard encoder each time new data is stable on the Keyboard Data lines.

1.3.2.3 **Repeat (REPEAT–).** Repeat is the low-active output of the REPEAT key, and is used to drive the repeat logic on the power/logic pwb to cause repetition of the code carried by Keyboard Data at 10 ±2 hertz whenever Repeat is active prior to Keyboard Data Strobe.

1.3.3 **POWER/LOGIC PWB-TO-VDT CONTROLLER INTERFACE.** The interface between the power/logic pwb and the VDT controller is implemented by an interconnection cable. Figure 1-12 illustrates the interface signals originated by the power/logic pwb for the VDT controller. The signals produced by the VDT controller for the power/logic pwb also travel on the same interconnection cable, and are discussed in a later paragraph. The following paragraphs describe the signals from the power/logic pwb to the VDT controller.

1.3.3.1 **Keyboard Data (TET,1,2,T).** Keyboard Data are complementary outputs of a differential line driver on the power/logic pwb. These signals travel on a pair of lines that carry the serial 11-bit keyboard code with start, stop and parity bits to the VDT controller. The format for the 11-bit code is shown in figure 1-13.

1.3.3.2 **Terminal Ready (TRD,1,2,T).** The Terminal Ready signals are complementary outputs of a differential line driver on the power/logic pwb. These two signals provide the indication of whether the terminal is operational to the computer via the VDT controller. If TRD1T = 0 and TRD2T = 1, the condition is an indication of loss of horizontal synchronization signals from the VDT controller or loss of power from the power supply.

1.3.4 **VDT CONTROLLER-TO-POWER/LOGIC PWB INTERFACE.** The interface between the VDT controller and the power/logic pwb in the display unit cabinet is implemented by the same interconnection cable and wiring harness described in paragraph 1.3.3. Figure 1-14 illustrates the interface signals produced by the VDT controller for the power/logic pwb.

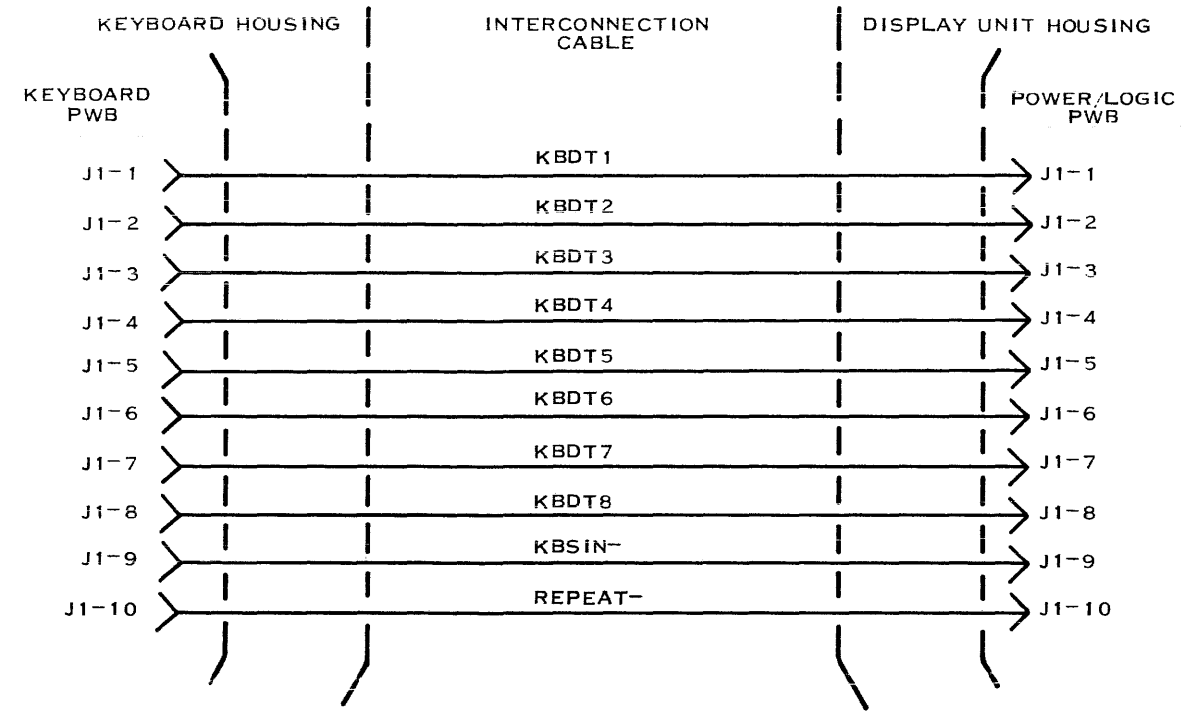


Figure 1-11. Model 911 VDT Keyboard-to-Power/Logic PWB Signal Interface

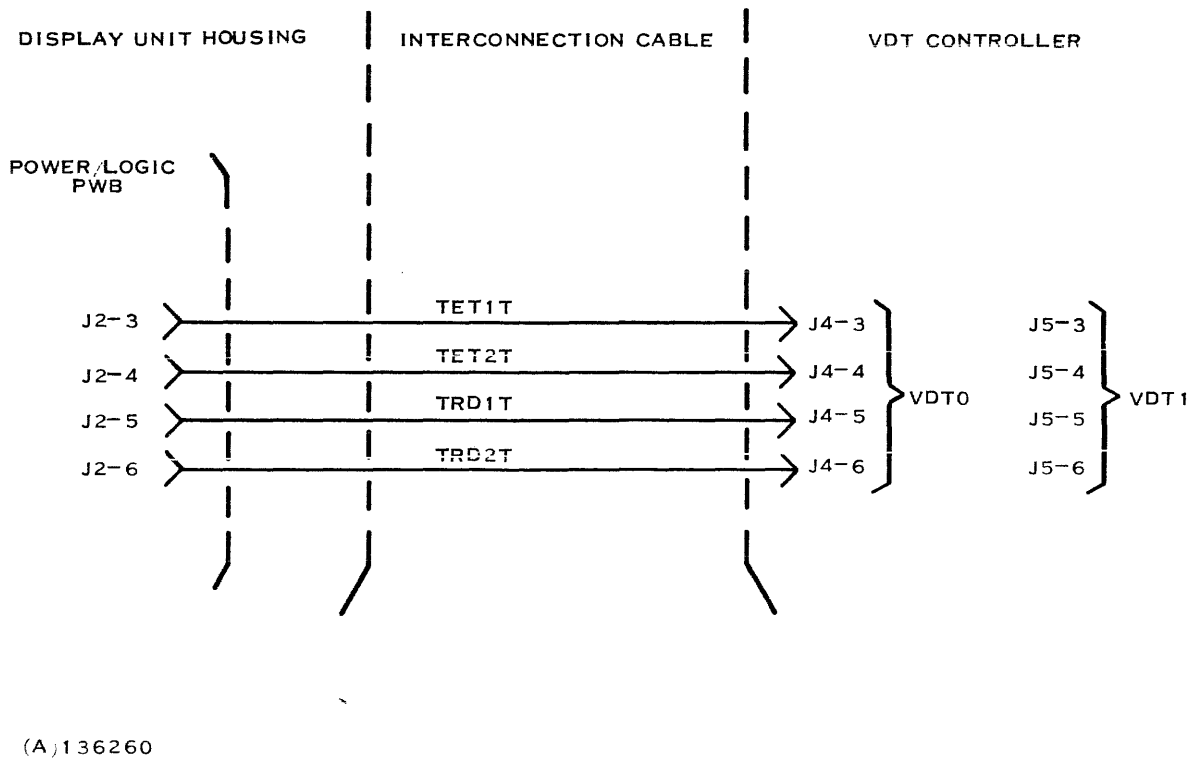


Figure 1-12. Model 911 VDT Power/Logic PWB-to-VDT Controller Interface

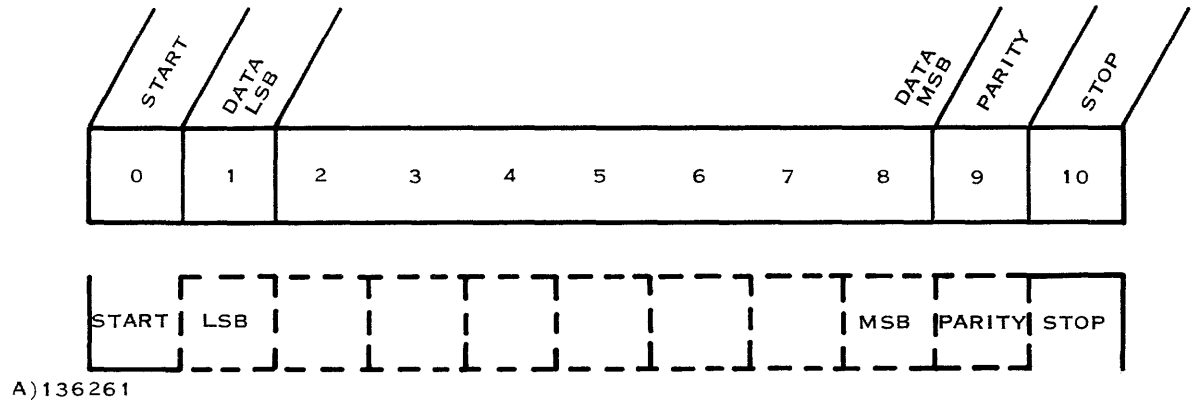


Figure 1-13. Model 911 VDT Power/Logic PWB-to-VDT Controller Data Format

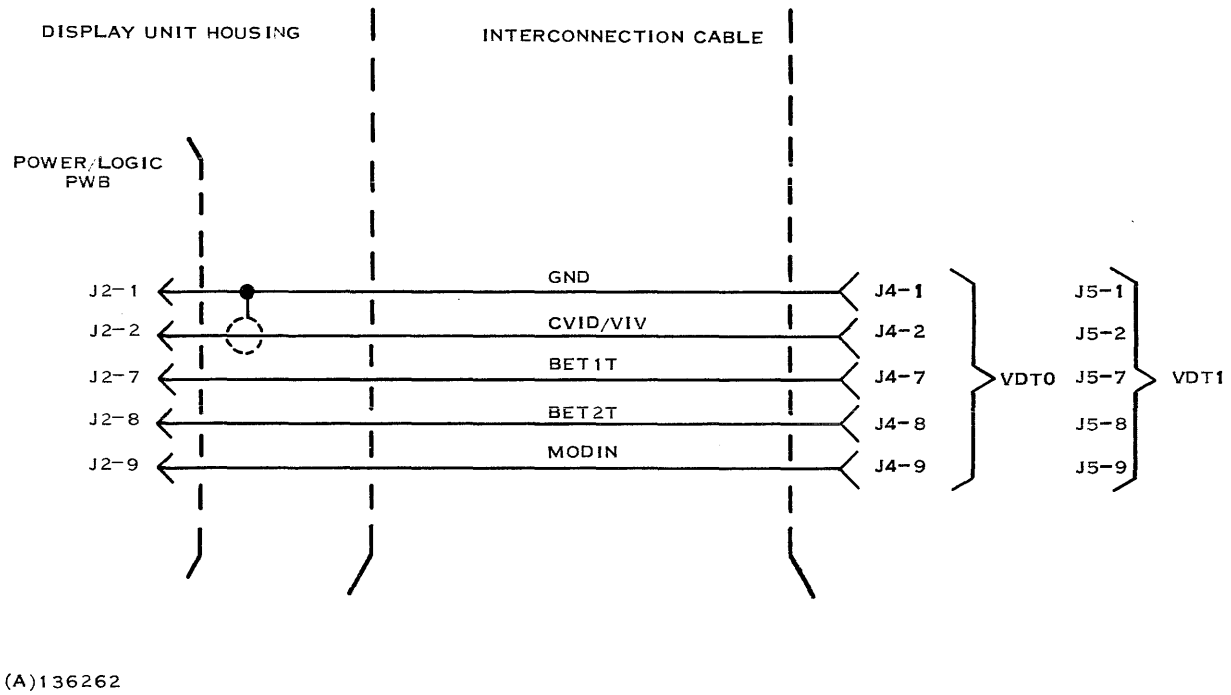


Figure 1-14. Model 911 VDT Controller-to-Power/Logic PWB Interface

1.3.4.1 **Video (CVID/V1V and GND).** Video (V1V) carries the composite video signal from the VDT controller to the power/logic pwb for separation into its components (video data, horizontal sync, and vertical sync) for the CRT monitor. CVID is the power/logic pwb mnemonic for the composite video signal. CVID travels on the center conductor of a coaxial cable, and GND is the grounded shield.

1.3.4.2 **Beep Enable (BET,1,2,T).** Beep Enable are complementary outputs of a differential line driver on the VDT controller that are active for 0.3 seconds (nominal) in response to Beep Enable (CRU output bit E_{16} with output bit F_{16} = 1). The Beep Enable pair enable an oscillator on the power/logic pwb for their duration to produce an audible tone via a loudspeaker in the base of the display unit housing.

1.3.4.3 **Modem Audio (MODIN).** Modem Audio carries low-level audio signals from the modem connected to the modem audio jack on the VDT controller. Modem Audio allows audio signals from a modem to be amplified and sent to the loudspeaker in the display unit housing. A patch cord (part number 0996373-1) is needed to connect the modem to the controller. A discrete jumper must also be made on the power supply/logic pwb between connector J2 pin 9 and resistor R34. If the modem audio is enabled, this signal line in the interconnection cable must be kept short to prevent noise pickup in the alarm circuits. The modem signal line should be less than 15.24 metres (50 feet).

1.3.5 **POWER/LOGIC PWB-TO-CRT MONITOR INTERFACE.** The interface between the power/logic pwb and the CRT monitor is implemented by a wiring harness inside the display unit housing that interconnects the power/logic pwb and the video pwb of the CRT monitor. Figure 1-15 illustrates the interface signals produced by the power/logic pwb for the CRT monitor. VERT, SYNC, VID OUT, and HOR. SYNC provide driving signals for the video pwb's vertical deflection amplifier, video amplifier, and horizontal deflection amplifier, respectively. Table 1-3 provides descriptions of the signals.

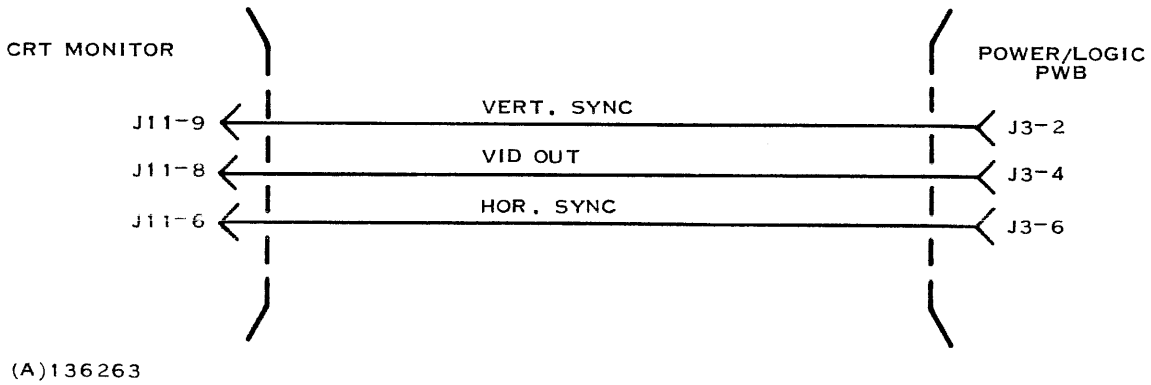


Figure 1-15. Model 911 VDT Power/Logic PWB-to-CRT Monitor Signal Interface

Table 1-3. Model 911 VDT Power/Logic PWB-to-CRT Monitor Interface Signal Characteristics

Signal	Pulse Rate or Width	Amplitude
VID OUT	Width = 20 nsec or greater	Low = 0.0 to +0.4V High = 4 ± 1.5V
VERT. SYNC	Rate = 47 to 63 per second	Same as for VID OUT
HOR. SYNC	Rate = 15K to 15.720K per second	Same as for VID OUT

1.4 PRINCIPLES OF OPERATION

The following paragraphs provide detailed descriptions of the operation of the various circuitry of the Model 911 VDT subsystem. Figure 1-16 is the detailed block diagram that provides the basis for the remainder of this section's discussion. Discussions of specific circuitry are augmented with more detailed circuit diagrams, flowcharts, and timing diagrams as needed for the discussion.

1.4.1 KEYBOARD. United States, European, and Japanese keyboard operation is discussed. Keyboard encoding is accomplished by one of two methods:

- Diode-isolated mechanical keyswitches with L52 encoder and scanner
- Solid-state keyswitches with microprocessor scanner and encoder.

Japanese Katakana keyboards will be vendor-supplied with solid-state keyswitches. The keyboard assembly logic diagram and contact matrix description are provided in Appendix F. Figure 1-17 is a block diagram of the diode-isolated mechanical keyboard used in United States and European keyboard versions; paragraphs 1.4.1.1, 1.4.1.2, and 1.4.1.3 provide detailed discussions of the keyboard's circuitry. United States keyboards will be supplied with both encoding techniques.

1.4.1.1 Contact Matrix. The contact matrix for the keyswitches consists of two sets of scan lines, each in a different plane, that run behind the keyswitches in such a manner that each time a keyswitch is actuated, the switch closes a circuit between an X and a Y scan line with the keyswitch and a diode, forming a series circuit between the scan lines. Figure 1-18 illustrates the United States and European contact matrix and a typical keyswitch circuit. Figure 1-19 shows the United States keyboard with each key numbered, and table 1-4 identifies the matrix connections and diodes involved in each keyswitch closure. Japanese Katakana contact matrix information is illustrated in Appendix F.

1.4.1.2 Encoder. The encoder is a four-mode programmable encoder that performs the following functions:

- Produces a unique eight-bit parallel data code for each combination of signals input to its X, Y, Shift, and Control inputs
- Produces a 20-microsecond (nominal) strobe pulse for each new eight-bit parallel code
- Produces a new eight-bit code and strobe pulse for each key struck regardless of any keys being held down.

Table 1-5 lists the codes produced by the encoder for each key in each mode and relates the information to figure 1-19. Appendixes A through F contain the codes produced by the national keyboards available with the Model 911 VDT. The key legends and codes are those not shown in table 1-5, and the information is related to numbered keyboard illustrations similar to figure 1-19.

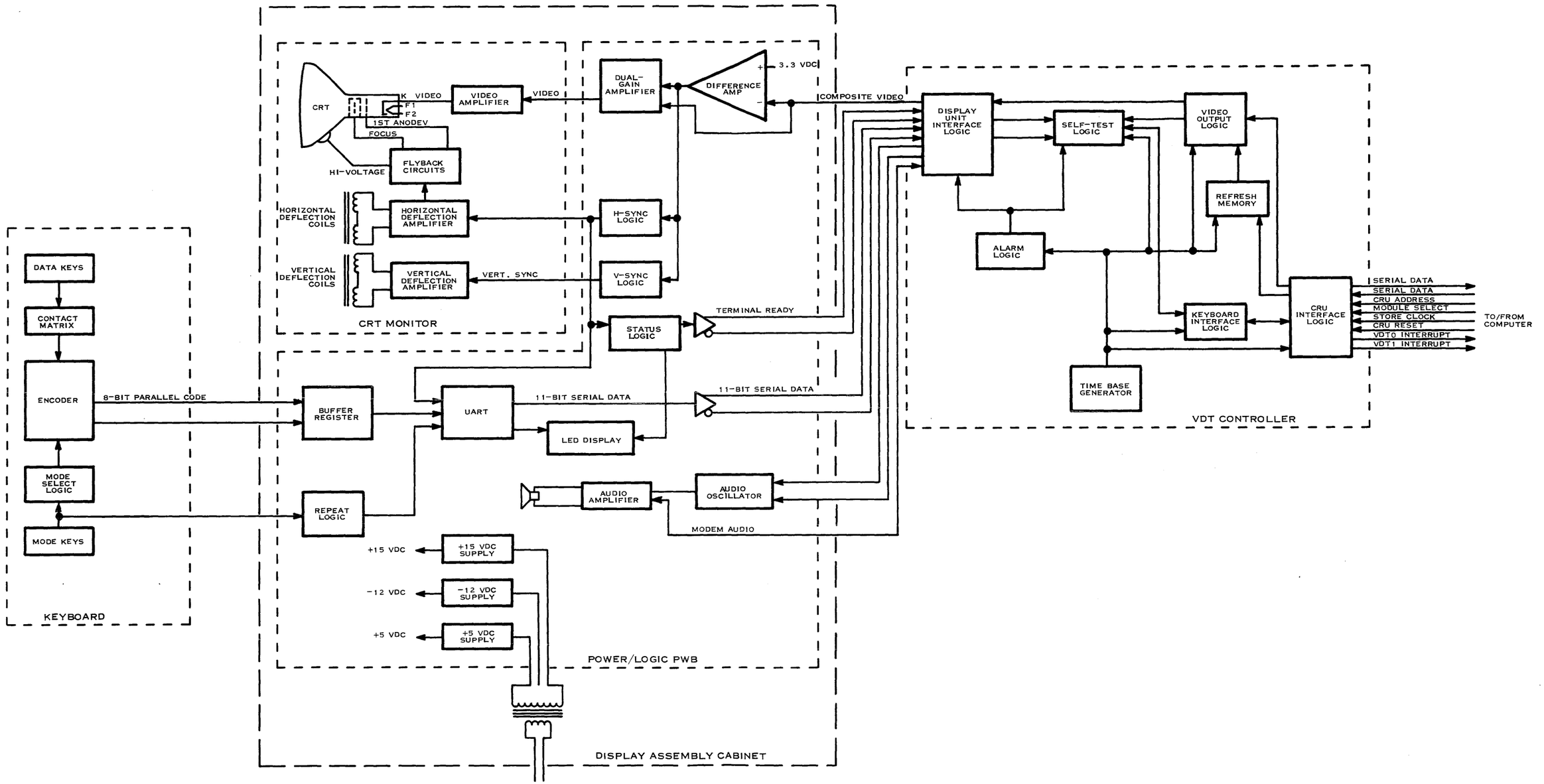
1.4.1.3 Mode Keys and Mode Select Logic. The SHIFT, CONTROL, UPPER CASE LOCK, and REPEAT keys with the mode select logic shown in figure 1-20 determine the code produced by the keyboard encoder and whether or not that code is repeatedly transmitted to the computer. There are two SHIFT keys. They are wired in parallel and perform the same function.

Each of the five mode keys closes a single set of contacts when actuated. These contacts, except for the REPEAT key, are decoded to select the keyboard encoder mode, and are not connected to the contact matrix. One side of each mode keyswitch is grounded, and the other side (used to provide an input to mode select logic) is connected to +5 Vdc via a pullup resistor. The pullup resistor guarantees that the keyswitch's output to mode select logic is held high until the keyswitch is closed, at which time the line is grounded.

The SHIFT, CONTROL, and UPPER CASE LOCK keys provide the inputs to mode select logic, as shown in figure 1-20, and the REPEAT key provides its signal directly to logic on the power/logic pwb that repeats the code from the encoder 10 times per second as long as the REPEAT key is held down. The repeated code is the code for the next data key struck following the actuation (holding down) of the REPEAT key.

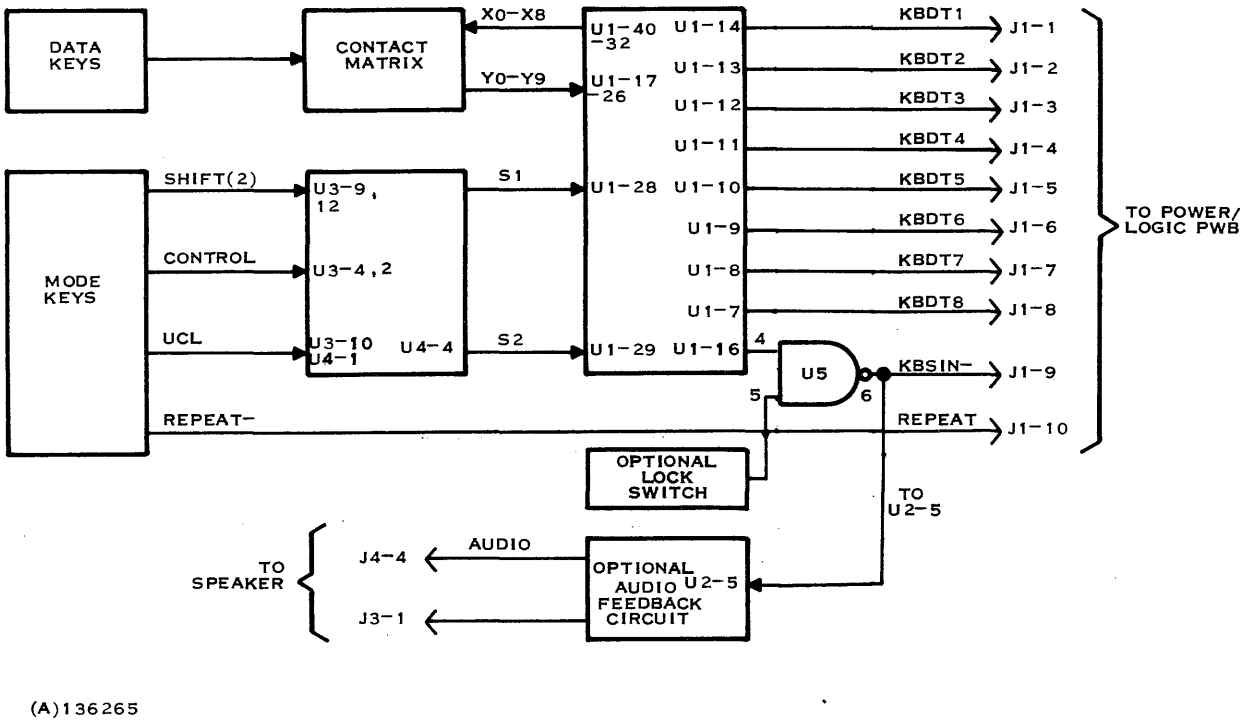
Mode select logic decodes the signals from the SHIFT, CONTROL, and UPPER CASE LOCK keyswitches to provide the signals labeled S1 and S2 in figure 1-20 to provide the Control and Shift inputs, respectively, to the encoder. These inputs are used by the encoder to provide the codes listed in table 1-5.

1.4.2 POWER/LOGIC PWB. Figure 1-21 is a detailed block diagram of the video, audio, and keyboard data path logic on the power/logic pwb. Figure 1-22 is a detailed block diagram of the power supply circuitry on the power/logic pwb and includes the power transformer and capacitors mounted off the power/logic pwb. The following paragraphs describe the operation of the circuits on the power/logic pwb.



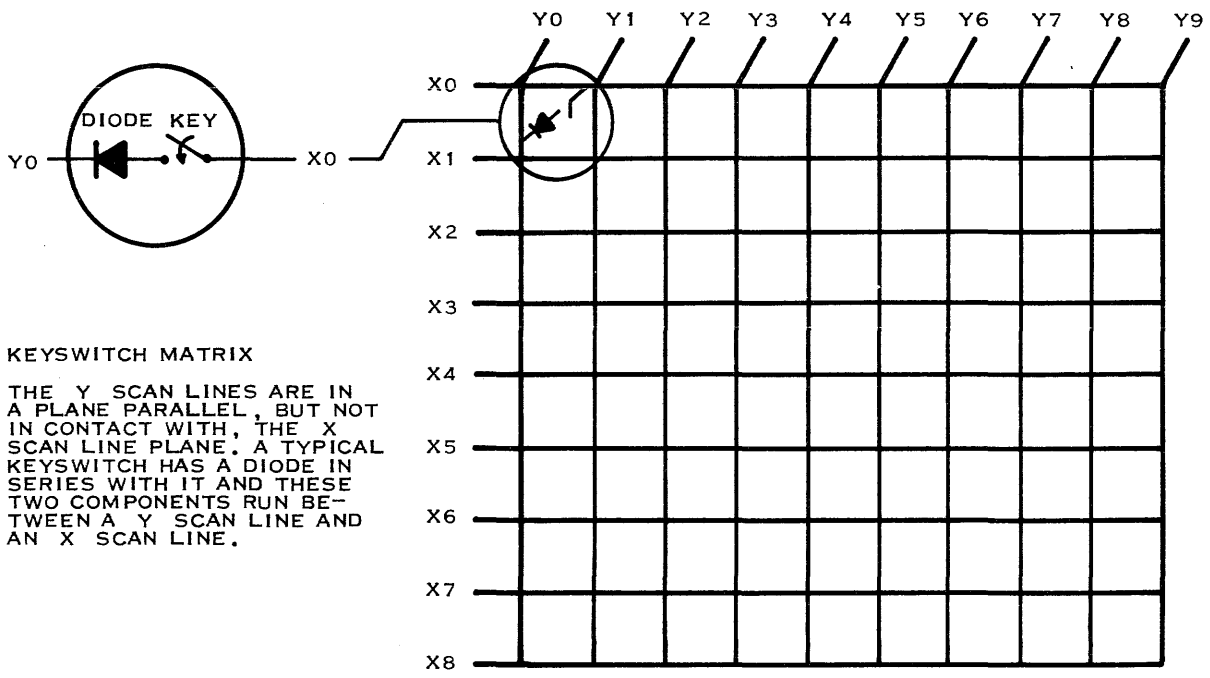
(D)136250

Figure 1-16. Model 911 VDT Detailed Block Diagram



(A)136265

Figure 1-17. Model 911 VDT Keyboard Block Diagram



(A)136266

Figure 1-18. Model 911 VDT Keyboard Contact Matrix

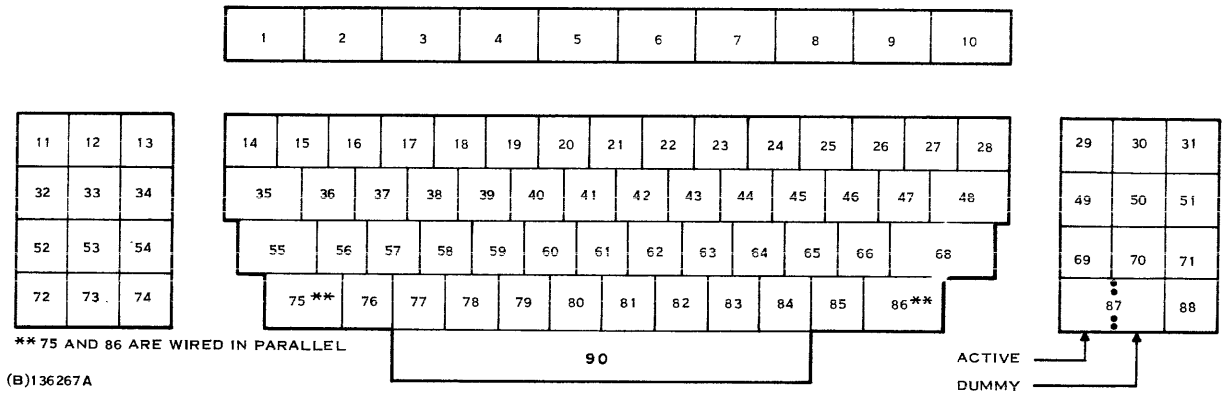


Figure 1-19. United States Model 911 VDT Keyboard with Keys Numbered

Table 1-4. Contact Matrix Connections and Associated Diodes for United States and European Model 911 VDT Keyboards

	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	
X0	11 CR12	32 CR13	52 CR14	72 CR15	12 CR16	33 CR17	53 CR18	73 CR19	54 CR20	74 CR21	KEY DIODE
X1	1 CR8	2 CR7	3 CR9	4 CR10	5 CR11	6 CR6	7 CR5	8 CR4	9 CR3	10 CR2	KEY DIODE
X2	87 CR78	69 CR79	70 CR80	71 CR81	49 CR82	50 CR83	51 CR84	29 CR85	30 CR86	31 CR87	KEY DIODE
X3	88 CR68	28 CR69	48 CR70	68 CR71	67* CR72	27 CR73	47 CR74	66 CR75	85 CR76	91* CR77	KEY DIODE
X4	26 CR58	46 CR59	65 CR60	84 CR61	25 CR62	45 CR63	64 CR64	83 CR65	24 CR66	44 CR67	KEY DIODE
X5	63 CR48	82 CR49	81 CR50	62 CR51	43 CR52	23 CR53	80 CR54	61 CR55	42 CR56	22 CR57	KEY DIODE
X6	21 CR38	41 CR39	60 CR40	79 CR41	78 CR42	59 CR43	40 CR44	20 CR45	90 CR46	77 CR47	KEY DIODE
X7	58 CR28	39 CR29	19 CR30	76 CR31	57 CR32	38 CR33	18 CR34	17 CR35	37 CR36	13 CR37	KEY DIODE
X8	16 CR22	15 CR23	36 CR24	35 CR25	56 CR26	89* CR27					KEY DIODE

* NOT INSTALLED IN EVERY CONFIGURATION

(A)136268A

Table 1-5. Universal Keyboard Outputs in Hexadecimal

KEY NUMBER	KEY LEGEND	MODE *			
		LC	UC	S	C
1	F1	92	92	92	92
2	F2	93	93	93	93
3	F3	94	94	94	94
4	F4	95	95	95	95
5	F5	96	96	96	96
6	F6	97	97	97	97
7	F7	98	98	98	98
8	F8	99	99	99	99
9	CMD	9B	9B	9B	9B
10		9C	9C	9C	9C
11	ERASE FIELD	80	80	80	80
12	ERASE INPUT	81	81	81	81
13		9F	9F	9F	9F
14	UPPER CASE LOCK				
15	! 1	90	90	90	90
16	@ 2	32	32	40	91
17	# 3	33	33	23	00
18	$ 4	34	34	24	A1
19	% 5	35	35	25	8D
20	^ 6	36	36	5E	8E

* LC = LOWER CASE
UC = UPPER CASE
S = SHIFT
C = CONTROL

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Table 1-5. Universal Keyboard Outputs in Hexadecimal (Continued)

KEY NUMBER	KEY LEGEND	MODE *			
		LC	UC	S	C
21	& 7	37	37	20	8F
22	SEE NATIONAL TABLES **				
23	(9	39	39	28	60
24	SEE NATIONAL TABLES **				
25	SEE NATIONAL TABLES **				
26	SEE NATIONAL TABLES **				
27	SEE NATIONAL TABLES **				
28	ESC	1B	1B	1B	1B
29	7	37	37	37	37
30	8	38	38	38	38
31	9	39	39	39	39
32	PRINT	9A	9A	9A	9A
33	↑	89	89	89	89
34	REPEAT				
35	ENTER	A0	A0	A0	A0
36	SEE NATIONAL TABLES **				
37	SEE NATIONAL TABLES **				
38	E	65	45	45	05
39	R	72	52	52	12
40	T	74	54	54	14

** REFER TO APPENDIX FOR KEY LEGEND AND CODES OF VARIOUS NATIONAL KEYBOARDS.

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Table 1-5. Universal Keyboard Outputs in Hexadecimal (Continued)

KEY NUMBER	KEY LEGEND	MODE *			
		LC	UC	S	C
41	SEE NATIONAL TABLES **				
42	U	75	55	55	15
43	I	69	49	49	09
44	O	6F	4F	4F	0F
45	P	70	50	50	10
46	SEE NATIONAL TABLES **				
47	SEE NATIONAL TABLES **				
48	SEE NATIONAL TABLES **				
49	4	34	34	34	34
50	5	35	35	35	35
51	6	36	36	36	36
52	←	88	88	88	88
53	HOME	82	82	82	82
54	→	8A	8A	8A	8A
55	CONTROL				
56	SEE NATIONAL TABLES **				
57	S	73	53	53	13
58	D	64	44	44	04
59	F	66	46	46	06
60	G	67	47	47	07

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Table 1-5. Universal Keyboard Outputs in Hexadecimal (Continued)

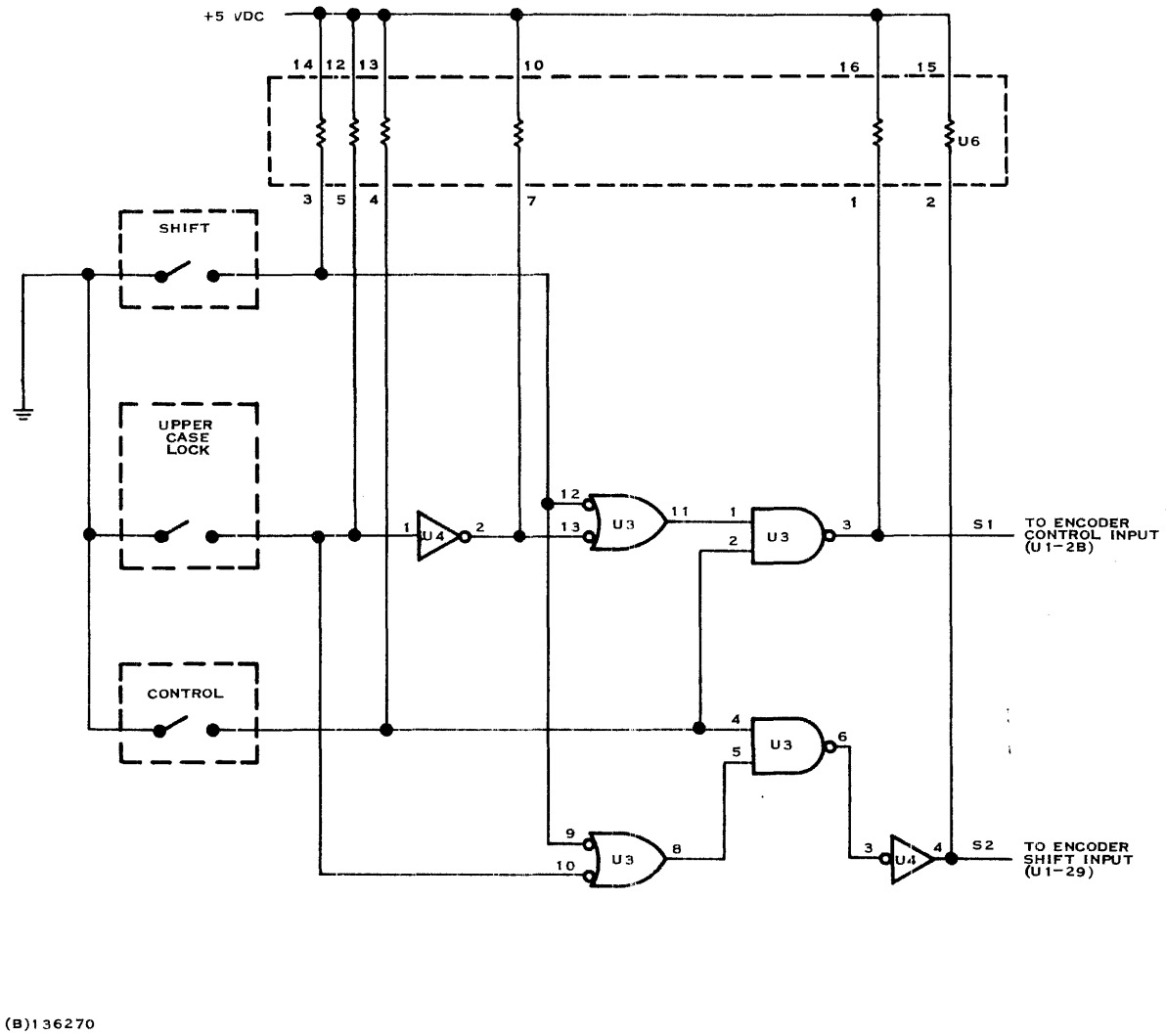
KEY NUMBER	KEY LEGEND	MODE *			
		LC	UC	S	C
61	H	68	48	48	08
62	J	6A	4A	4A	0A
63	K	6B	4B	4B	1B
64	L	6C	4C	4C	0C
65	SEE NATIONAL TABLES **				
66	SEE NATIONAL TABLES **				
67	SEE NATIONAL TABLES **				
68	TAB SKIP	85	85	83	85
69	1	31	31	31	31
70	2	32	32	32	32
71	3	33	33	33	33
72	INS CHAR	86	86	86	86
73	↓	8B	8B	8B	8B
74	DEL CHAR	84	84	84	84
75	SHIFT				
76	SEE NATIONAL TABLES **				
77	X	78	58	58	18
78	C	63	43	43	03
79	V	76	56	56	16
80	B	62	42	42	02

(A) 140151 (4/5)

Table 1-5. Universal Keyboard Outputs in Hexadecimal (Continued)

KEY NUMBER	KEY LEGEND	MODE *			
		LC	UC	S	C
81	N	6E	4E	4E	0E
82	SEE NATIONAL TABLES **				
83	< ,	2C	2C	3C	1C
84	> .	2E	2E	3E	1E
85	? /	2F	2F	3F	1F
75 86	SHIFT				
87	0	30	30	30	30
88	SEE NATIONAL TABLES **				
89	JAPAN KEYBOARD ONLY				
90	SPACE BAR	20	20	20	20
91	SEE NATIONAL TABLES**				

(A) 140151 (5/5)



TRUTH TABLE				
CONTROL	SHIFT	UCL	S1	S2
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	1	1
1	1	1	0	0

Figure 1-20. Model 911 VDT Mode Select Logic and Truth Table

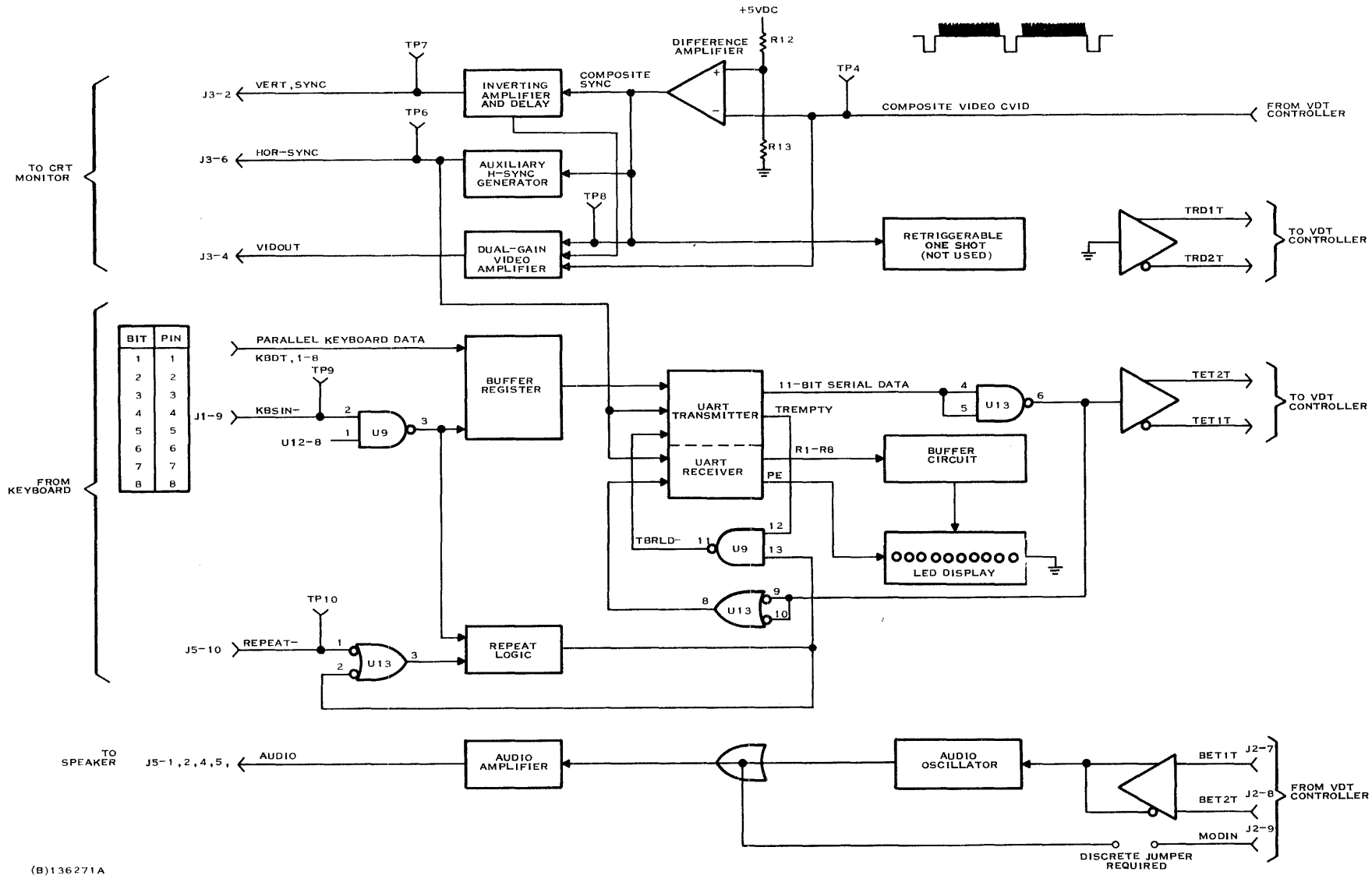


Figure 1-21. Model 911 VDT Power/Logic PWB Detailed Block Diagram of Keyboard Data Path, Video, and Audio Logic

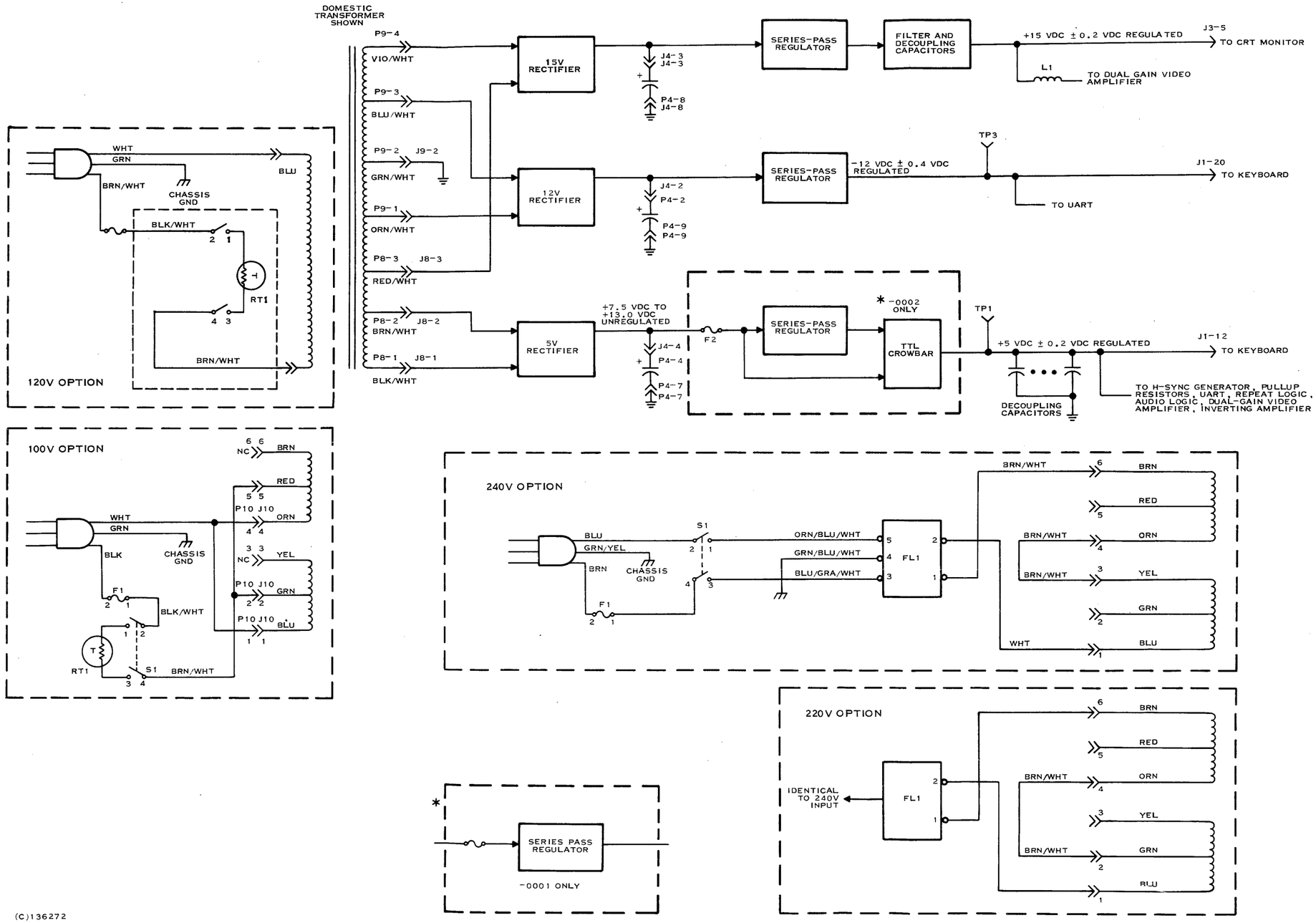


Figure 1-22. Model 911 VDT Power/Logic PWB Power Supply Block Diagram

1.4.2.1 **Buffer Register.** The buffer register is an eight-bit flip-flop register that latches the eight-bit keyboard data code, KBDT,1-8, when strobed by Keyboard Data Strobe (KBSIN–) and holds the latched keyboard code for the UART transmitter until a new data code is transmitted by the keyboard. The buffer register always contains the last character code transmitted by the keyboard.

1.4.2.2 **UART Transmitter.** The UART transmitter is the transmitter portion of a universal asynchronous receiver/transmitter. The transmitter accepts the parallel eight-bit output of the buffer register when loaded by TBRLD–. The transmitter latches the eight-bit code, adds one start bit, one parity bit, and one stop bit, and serializes the "assembled" 11-bit code, clocking the data out at the rate of one bit for each 16 clocks. The serial 11-bit code is driven out to the VDT controller on a pair of lines and provided to the serial input of the UART receiver. The UART receiver output drives a LED display for operator monitoring of keyboard operation.

The frequency of the output of the H-Sync generator is 15.72 kilohertz, so the character output rate of the UART transmitter is 89.3 characters per second (16 clocking pulses are required for each bit converted from parallel to serial format by the UART transmitter). Figure 1-23 illustrates the timing relationships for the UART transmitter.

Each time the UART transmitter transmits a character, the transmitter produces a signal, TREMPTY, that enables the transmitter to accept a new data code from the buffer register. During character transmission, TREMPTY is held low to disable the acceptance of a new code from the buffer register.

1.4.2.3 **UART Receiver.** The receiver portion of the UART monitors the 11-bit serial output of the UART transmitter, removes the start and stop bits, converts the remaining nine bits into a parallel code identical to the eight-bit code received from the keyboard, and provides a parity test flag bit. These nine outputs of the UART receiver are used to drive the LED display to allow visual monitoring of the last code received from the keyboard and a parity indication.

1.4.2.4 **LED Display.** The LED display consists of 10 LEDs that indicate the status of each of the eight keyboard data bits, the parity bit, and the presence or absence of horizontal sync pulses. Figure 1-24 illustrates the LED display which is located on the rear of the display unit cabinet.

For the keyboard data bits, a lighted LED indicates a logic 1. The parity (P) LED is normally lighted and indicates that the parity of the last character transmitted by the UART was correct. The Sync (S) LED should always be lighted during normal operation of the terminal to indicate the presence of horizontal synchronization pulses from the VDT controller.

1.4.2.5 **Repeat Logic.** The repeat logic on the power/logic pwb produces the pulses that load the outputs of the buffer register into the UART transmitter. The repeat logic produces one pulse (TBRLD–) to load the transmitter each time a data key is struck without the REPEAT key actuated, or produces 10 ± 2 pulses (TBRLD–) per second whenever a data key is struck while the REPEAT key is being held down. The repeat circuit is illustrated in figure 1-25.

The primary component of the repeat circuit is a timer biased for astable oscillation at 10 ± 2 hertz. The remainder of the circuit enables the timer whenever a data key is struck, either alone or with the REPEAT key, and disables the timer all the rest of the time.

Whenever a data key is struck, KBSIN– sets the strobe flip-flop and enables the timer. The timer produces a high-active output that loads the UART transmitter (drives TBRLD– low) if the transmitter is empty (TREMPTY = 1).

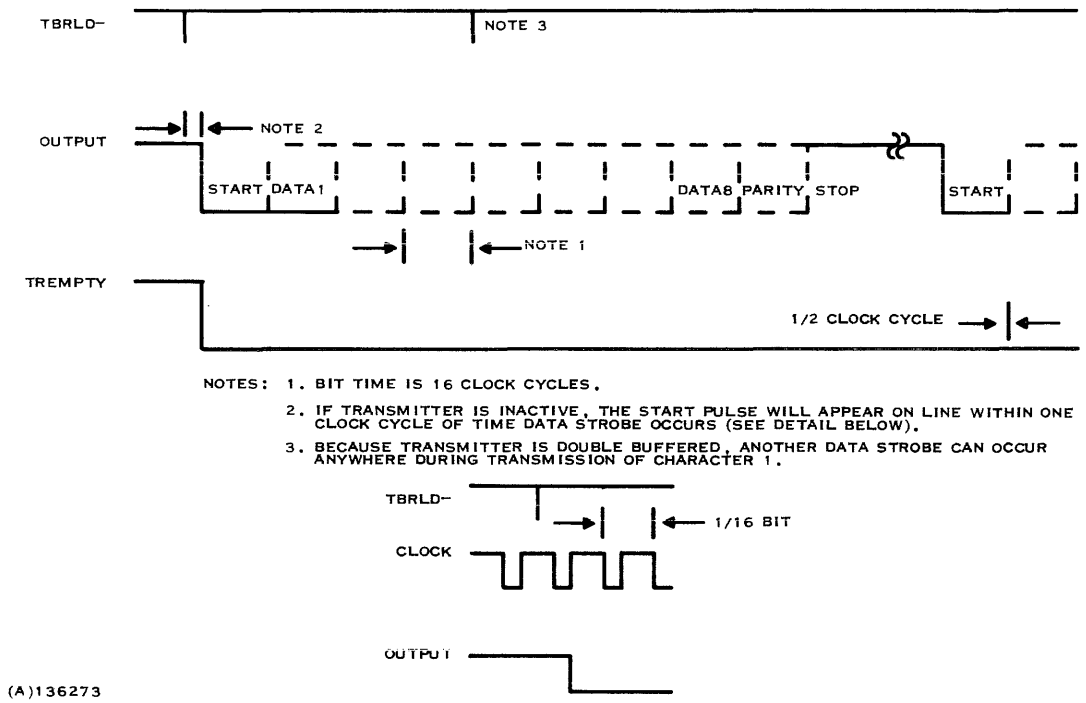


Figure 1-23. Model 911 VDT Power/Logic PWB UART Transmitter Timing Diagram

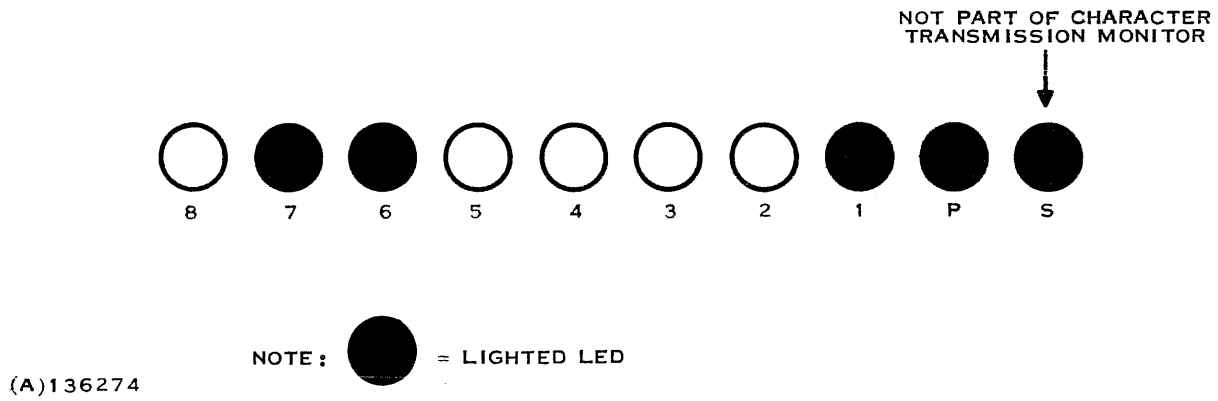


Figure 1-24. Model 911 VDT LED Display

If the REPEAT key is not held down (REPEAT– = 1), the trailing edge of the timer's high-active output resets the repeat flip-flop and, in turn, resets the strobe flip-flop and disables the timer before a second output pulse can be produced.

If the data key is struck while the REPEAT key is held down, KBSIN– sets the strobe flip-flop and enables the timer. Since REPEAT– is held low, the timer's output does not reset the repeat flip-flop, and the timer produces outputs at 10 ± 2 hertz as long as the REPEAT key is held down. Since the UART transmitter empties itself at a faster rate than the repeat circuit produces loading pulses, TREMPTY is always logic 1 prior to each timer output pulse during the repeat operation. Therefore, TBRLD– oscillates at 10 ± 2 hertz (the timer circuit rate) and causes the character code being held by the buffer register to be repeated.

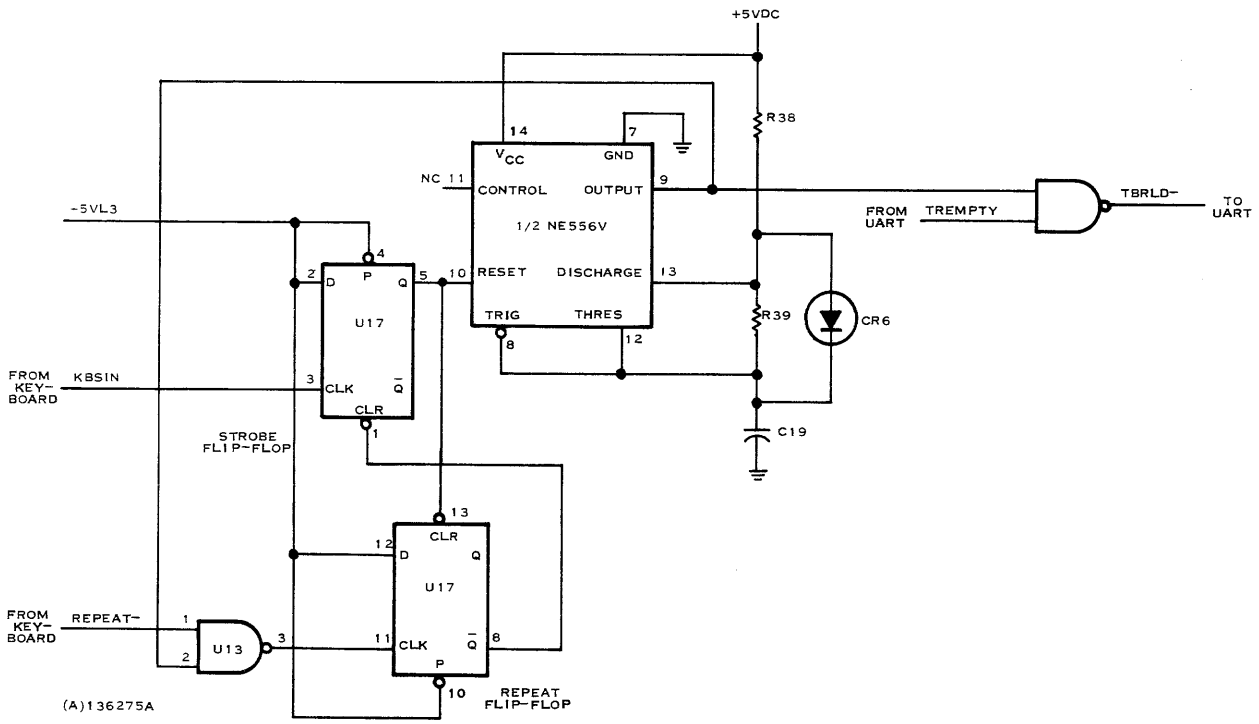


Figure 1-25. Model 911 VDT Repeat Logic

1.4.2.6 **Difference Amplifier.** The difference amplifier removes the video from the composite video waveform. The difference amplifier is biased to respond only to signals that have voltage levels lower than approximately 0.3 Vdc. Since the video data (see figure 1-21) lies above the 0.3 Vdc reference, only the horizontal and vertical synchronization components of the incoming composite video signal from the VDT controller are amplified by the difference amplifier.

1.4.2.7 **Dual-Gain Video Amplifier.** The dual-gain video amplifier provides one of two gain paths for the composite video from the VDT controller. One gain path provides gain for short interconnection cables, and the other gain path provides a higher gain to compensate for cable lengths greater than approximately 304.8 metres (1000 feet). Figure 1-26 shows the dual-gain video amplifier schematic diagram.

Transistor Q2 buffers the composite video signal from the VDT controller. Switch S1 in the output circuitry of Q2 is the line compensation switch. For cable lengths less than 304.8 metres (1000 feet), S1 should be open to provide a divider network for the output of Q2. For cables longer than 304.8 metres, S1 should be closed to bypass R15, allowing less attenuation of the output of Q2.

Transistor Q6 is biased near turnon to eliminate the horizontal sync component of the video signal. The video component of Q6's input turns Q6 on, and Q6 amplifies that component. The horizontal sync component is attenuated and drives Q6 toward cutoff.

Q3 provides further amplification of the video, and the signal at its output is clamped to TTL-compatible levels by the diode network.

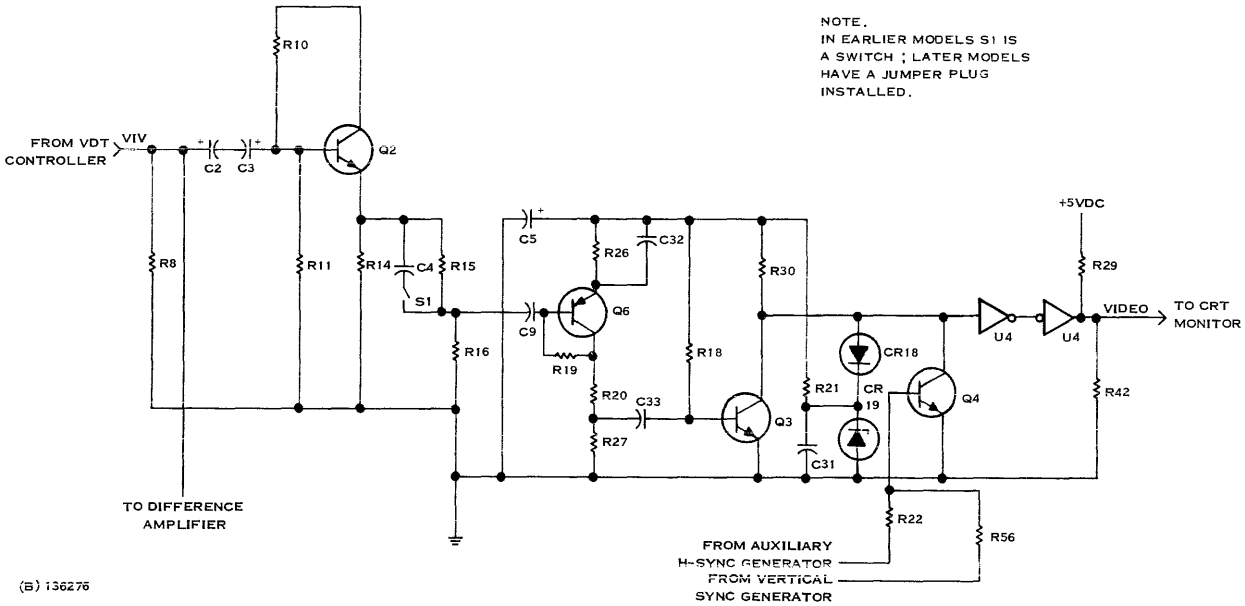


Figure 1-26. Model 911 VDT Power/Logic PWB Dual-Gain Video Amplifier

Transistor Q4 (clamping circuit) conducts during horizontal or vertical sync to pull the level of the video signal to ground. This prevents display of extraneous video components during retrace, and the passing of horizontal and vertical synchronization pulses by the dual-gain video amplifier.

1.4.2.8 **Vertical Sync Generator.** The vertical sync generator amplifies and passes only the vertical component of the composite sync signal from the difference amplifier. Figure 1-27 is a schematic diagram of the vertical sync generator. The circuitry at the base of Q5 acts as a low-pass filter to pass only the 60-hertz (or 50-hertz) vertical synchronization component of the composite sync signal. Transistor Q5 then amplifies and inverts the vertical synchronization component of the composite sync signal. The output of transistor Q5 drives two cascaded Schmitt-Trigger inverters which form a pulse shaping and delay circuit. The low-active output of this circuit is nominally low for 220 microseconds.

1.4.2.9 **H-Drive Generator.** Figure 1-28 is a schematic diagram for the H-drive generator that passes the horizontal synchronization component of the composite sync signal during normal operation, and produces an "artificial" horizontal synchronization when the terminal is not connected to an operating controller. Horizontal synchronization signal (CRTCLK) is also used to clock the keyboard UART.

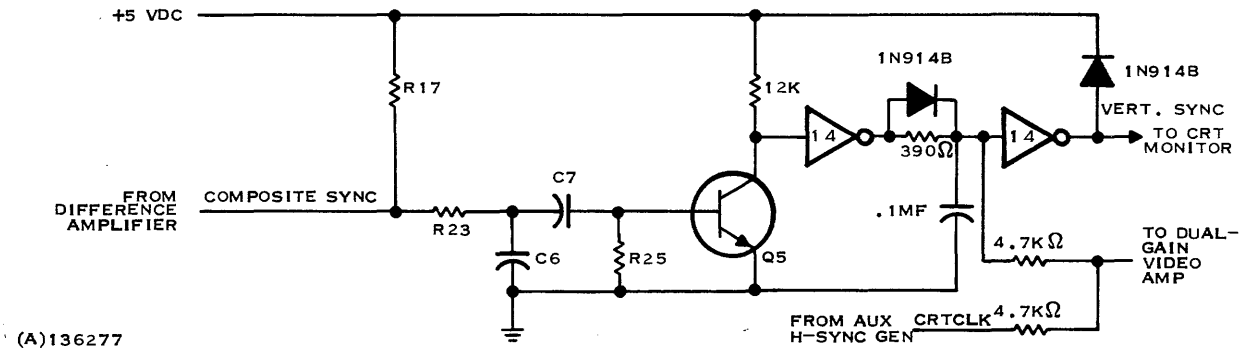


Figure 1-27. Model 911 VDT Power/Logic PWB Vertical Sync Generator Schematic Diagram

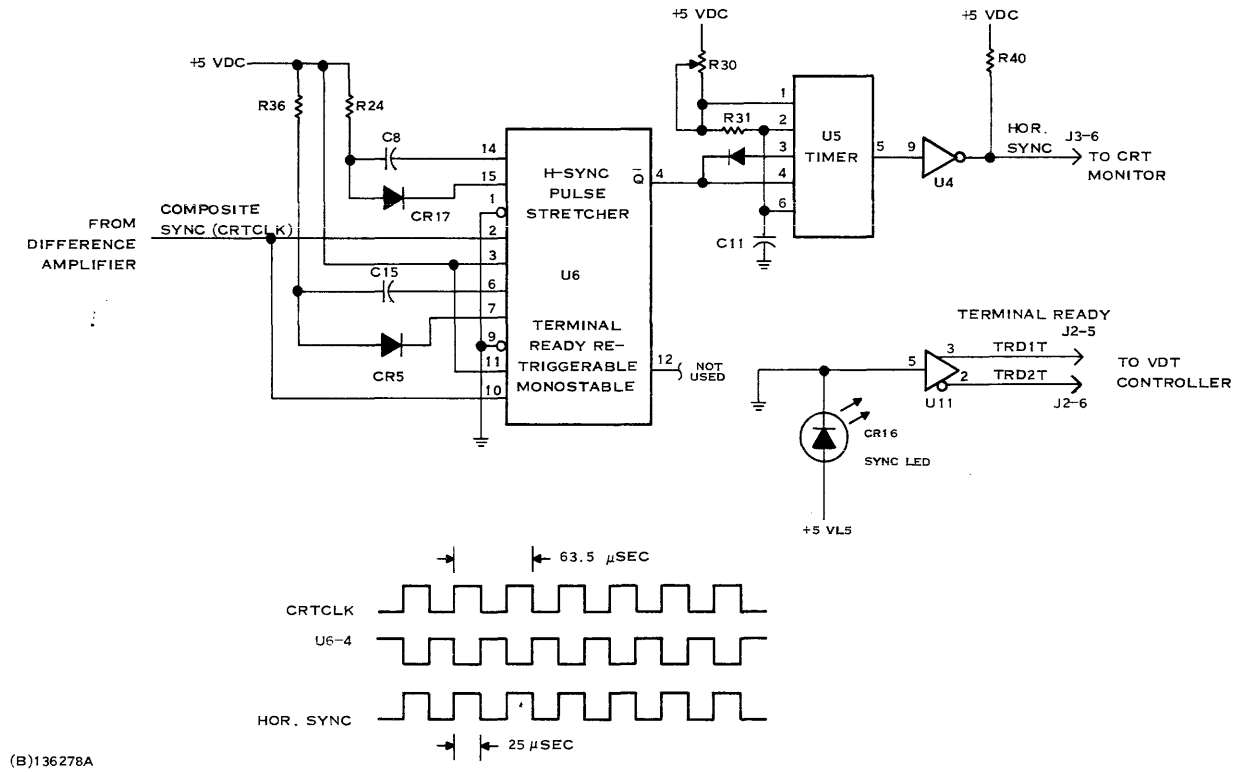


Figure 1-28. Model 911 VDT Power/Logic PWB Auxiliary H-Sync Generator Schematic Diagram

The H-SYNC pulse stretcher monostable multivibrator (U2) in the H-drive generator changes the duty cycle of the composite sync pulse to approximately 39% (25 microseconds low; 40 microseconds high). The stretched composite sync signal resets the timer and keeps the timer reset for the duration of the low-level (25 microseconds) pulse. Since the frequency of the composite sync signal (15.720 KHz) is greater than the "natural" frequency of the astable multivibrator (approximately 15 KHz), the timer "locks in" on the horizontal component of the composite sync signal. The "natural" frequency of the horizontal timer circuit is set by R30.

With no composite sync signal present, as would be the case if the video display unit were not connected to a VDT controller, the timer provides an artificial horizontal sync signal to be used for self-test. The horizontal synchronization signal, whether provided by the VDT controller or generated at the "natural" frequency of the timer network, clocks all operations of the UART.

The Sync (S) LED continually lights when power is applied to the terminal. The LED is the S LED shown in figure 1-24. Terminal Ready (signals TRD1T = logic 0 and TRD2T = logic 1) indicates the terminal is powered on and does not depend upon any controller input.

1.4.2.10 Audio Circuitry. Figure 1-29 illustrates the circuitry that monitors Beep Enable from the VDT controller and audio from an external modem (relayed by the VDT controller). The differential (two-wire) line receiver for Beep Enable provides noise immunity. The software alarm condition (Beep Enable) enables the SN74LS132 to oscillate at a frequency determined by the time constant of the RC biasing network. The SN74LS00 isolates the Beep Enable input circuitry from the modem audio input. The LM386N amplifies whatever input it is provided (Beep Enable-produced oscillator output or modem audio) and provides the amplified audio signal to a loudspeaker and volume control mounted in the front portion of the display unit's base.

1.4.3 CRT MONITOR. Figure 1-30 is a block diagram of the CRT monitor located in the display unit cabinet. The monitor consists of a pwb and a CRT assembly.

The video amplifier amplifies the video data received from the power/logic pwb and modulates the cathode of the CRT. A BRIGHTNESS control adjusts the brightness of the display by varying the relative dc potential between the CRT cathode and the control grid.

The horizontal amplifier, triggered by horizontal drive pulses, develops a sawtooth current to drive the horizontal deflection coils of the CRT yoke. The horizontal deflection circuit drives the horizontal coils and the flyback circuits to develop high voltage for the second anode, dc voltages for CRT bias (first anode), focus and accelerating grids and a dc voltage for the video output stage.

The vertical amplifier is triggered by the vertical synchronization pulses from the power/logic pwb and develops the 50-hertz or 60-hertz sawtooth currents used to drive the vertical deflection coils of the CRT yoke.

1.4.4 VDT CONTROLLER. A block diagram of the VDT controller is shown in figure 1-31. The controller is implemented on a full-size CRU pwb that is installed into a designated backpanel slot in either the main computer chassis or an expansion chassis. The VDT controller performs the following functions:

- Provides data paths between keyboard and computer and between computer and CRT monitor
- Generates video format character codes for 96 standard display symbols including uppercase and lowercase alphabet characters, numeric characters, and special symbols (+, -, ;, etc.)

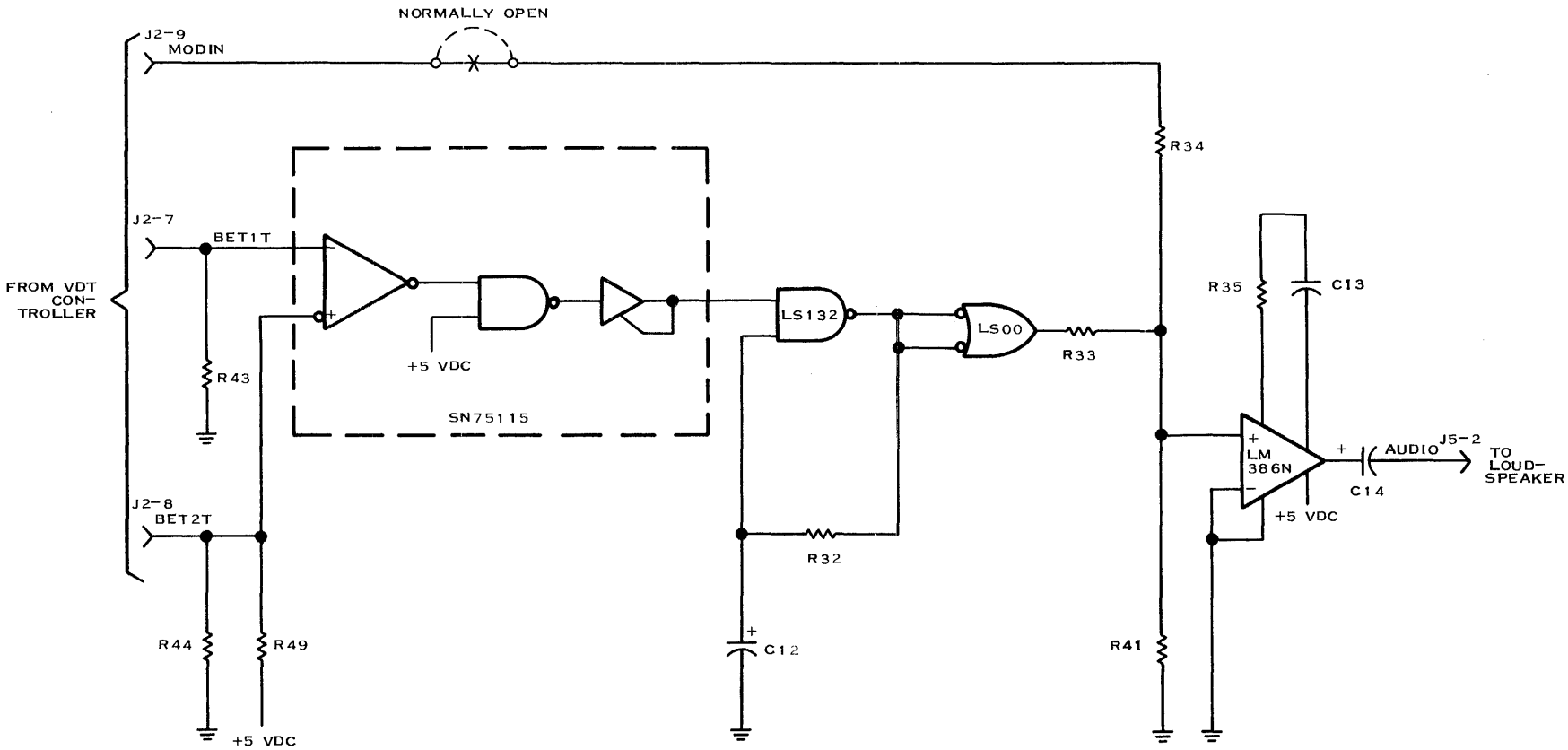


Figure 1-29. Model 911 VDT Power/Logic PWB Audio Circuitry

- Generates all video data, horizontal synchronization, and vertical synchronization signals for CRT monitor
- Provides storage (refresh memory) for characters to be displayed by CRT monitors
- Provides self-test logic to aid in fault isolation.

1.4.4.1 CRT Interface Logic. CRT interface logic consists of two differential line receivers for the serial keyboard data and Terminal Ready from the power/logic pwb, a differential line driver for the Beep Enable signal to the power/logic pwb, and a video line driver (shown in figure 1-32) to drive out the composite video signal to the power/logic pwb.

The differential line receivers and driver provide noise immunity for the transmission lines between the VDT controller and the power/logic pwb.

The video line driver buffers the character-containing video signal NVIDL, and the composite sync signal, CSQ, combines them into one composite video signal, then amplifies the signal for transmission over coaxial cable to the power/logic pwb.

1.4.4.2 Built-In Test Logic. Figure 1-33 shows built-in test logic. During normal operation, the A inputs of the four 2-to-1 selectors are selected for routing to other logic. The built-in test logic outputs are as follows:

- BTL = NTRL – Terminal Ready from the keyboard. Passed to CRU interface as received.
- BKBINL = TKBL – Serial Keyboard Data from keyboard.
- BBTSL = PREVW1Q – State of VDT controller prior to last Word Select (CRU output bit F_{16})
- NLEDL = NLEDL* – Enable for Self Test LED (shared by both controllers on a 2-controller VDT controller pwb). If second controller is in self-test mode, NLEDL* = 0 to light LED.

When the computer selects the self-test mode by setting Test Mode to 1, CRA9Q is 1 and causes the 2-to-1 selectors to pass the data at their B inputs according to table 1-6 and as follows:

- BTL = 1 (Terminal Not Ready)
- BKBINL = KBTL – Serial test output of VDT controller UART.
- BBTSL = BTSL – See table 1-7.
- NLEDL = 0 – lights self-test LED.

CRA0Q and CRA1Q select one of the four inputs to the test input multiplexer according to table 1-7.

The test mode indicator (located on the VDT controller pwb) is lighted whenever CRA9Q is high to select the self-test mode.

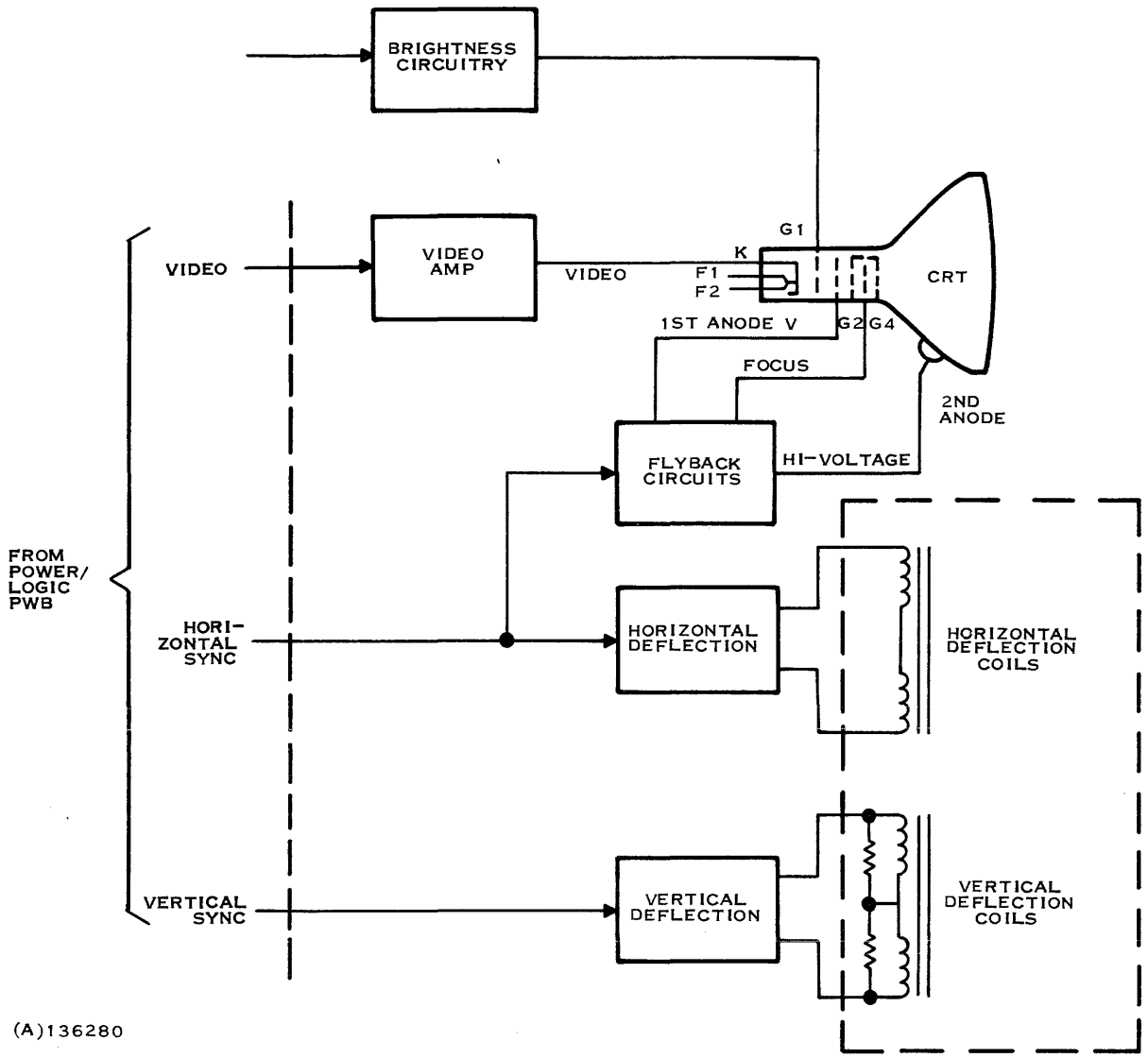


Figure 1-30. Model 911 VDT CRT Monitor Block Diagram

1.4.4.3 **Keyboard Logic.** Keyboard logic provides functions for the data entry and self-test modes of operation. Figure 1-34 shows keyboard logic.

In the data entry mode, the keyboard UART (TMS6011 or equivalent) removes the start, stop, and parity bits from the serial data, BKBINL, from built-in test logic and converts the data to eight-bit parallel format. The UART produces a high-active signal, KBRDYL, when the parallel data outputs, KBD,0-7,Q, are stable. KBRDYL sets the keyboard data ready latch, KBDRQ, to enable Keyboard Data Ready (CRU input bit F_{16}) at the CRU interface. When KBDRQ is active, it drives the device interrupt, NKBINT, low to notify the computer of the impending data transfer when interrupt-enabled CRACQ = 1 (CRU output bit C_{16} with CRU output bit F_{16} = 0). Figures 1-9 and 1-10 illustrate the CRU input and output bit assignments for the Model 911 Video Display Terminal.) The UART also produces a parity error signal, KBPEL, which indicates, when active, that the data on the keyboard data lines was transferred with incorrect parity.

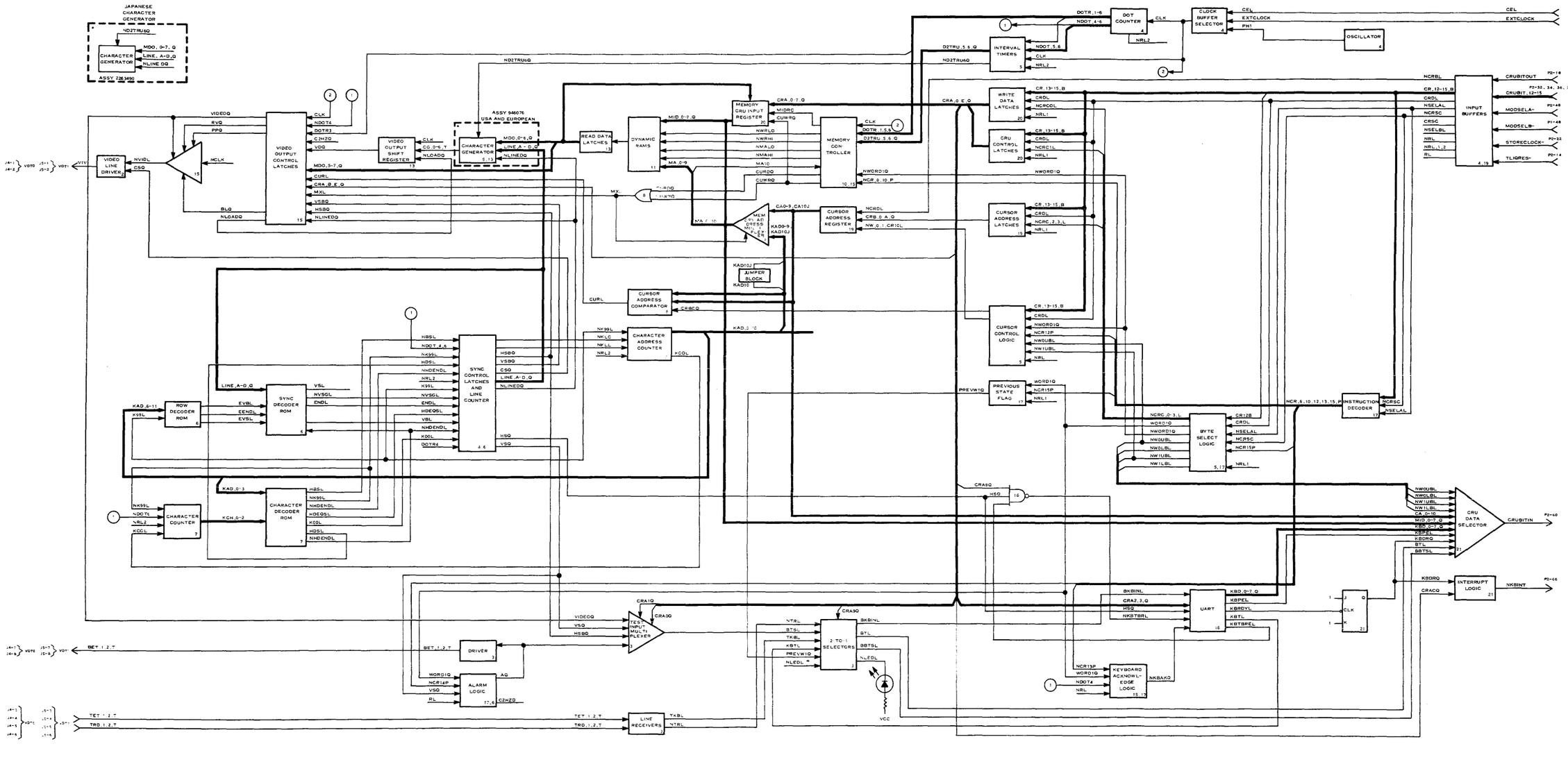


Figure 1-31. Model 911 VDT Controller Block Diagram

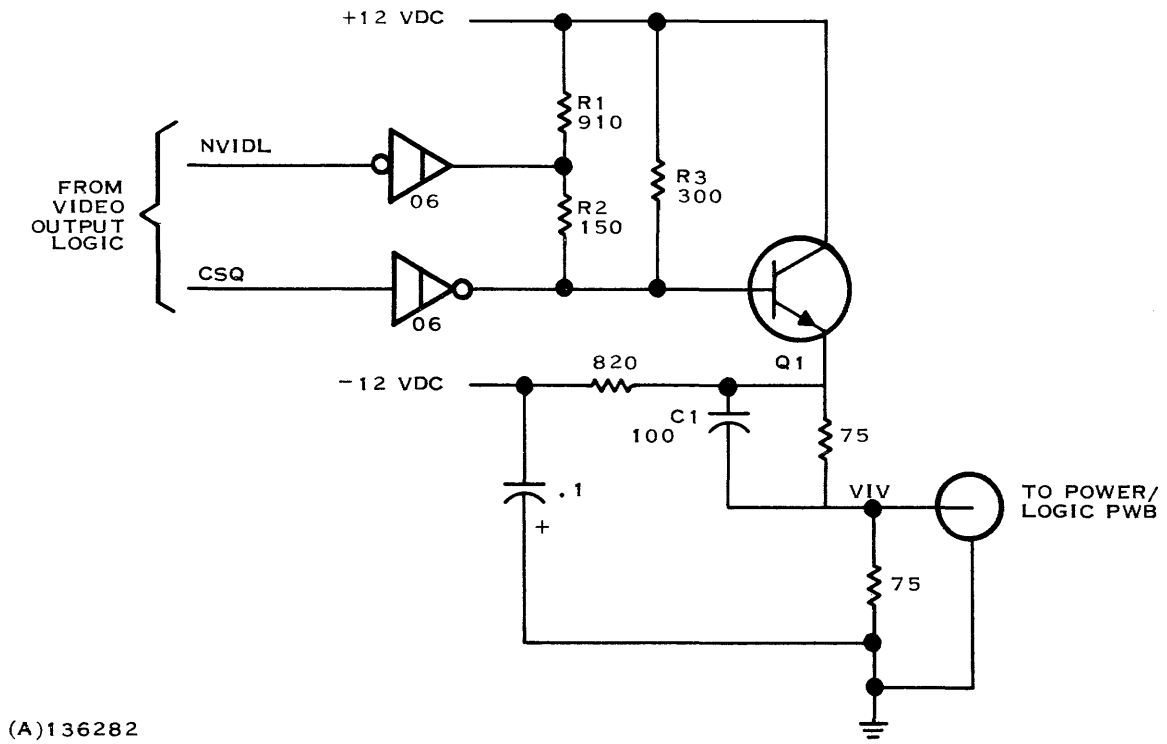


Figure 1-32. Video Line Driver

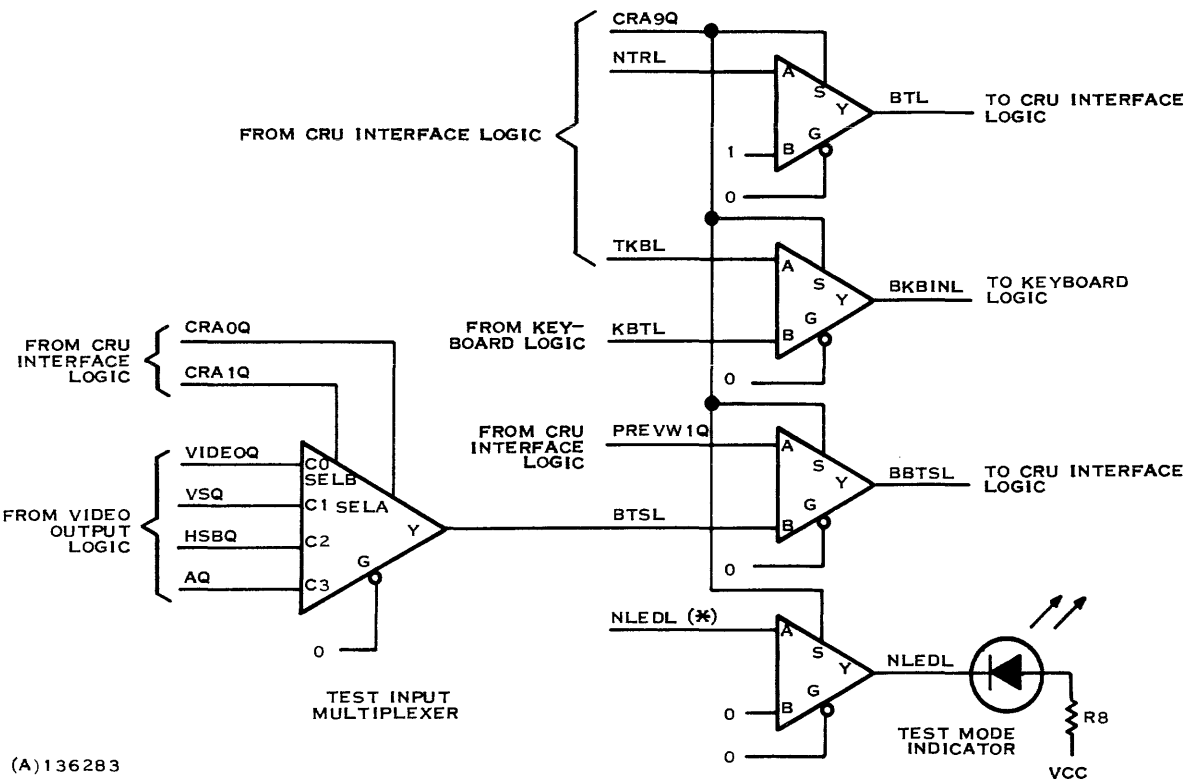


Figure 1-33. Model 911 VDT Built-In Test Logic

Table 1-6. Test Data Selection

CRA9Q	BTL	BKBINL	BBTSL	NLEDL
0	NTRL	TKBL	PREVW1Q	NLEDL*
1	1	KBTL	BTSL	0

Table 1-7. Selected Test Inputs

CRA0Q	CRA1Q	BBTSL
0	0	VIDE0Q
0	1	VSQ
1	0	HSBQ
1	1	AQ

The computer acknowledges Keyboard Data Ready by setting Keyboard Acknowledge which sets the keyboard acknowledge latch (KBACKQ). The keyboard acknowledge latch holds KBACKQ high until the keyboard interrupt reset latch is set to ensure proper input conditions are provided to the keyboard acknowledge synchronizer latch (KBASQ). The keyboard acknowledge synchronizer latch and the keyboard interrupt reset latch provide double-buffered synchronization to ensure recognition of Keyboard Acknowledge by the UART. KBAKQ, the double-buffered synchronized version of Keyboard Acknowledge, clears the keyboard acknowledge latch and the keyboard data ready latch (Keyboard Data Ready) KBRDYL, and the parity error signal from the UART, and removes the device interrupt, KNBINT, from the interface.

Figure 1-35 shows flowcharts for the transmitter and receiver portions of keyboard logic.

1.4.4.4 CRU Interface Logic. CRU interface logic provides the circuitry to input and output data, control, and status signals to and from the computer. Figure 1-36 shows CRU interface logic, and the following discussions describe the circuits in that diagram.

Input Buffers. The input buffers provide buffering for all the CRU interface signals from the computer.

Instruction Decoder. The instruction decoder monitors CRUBIT,12-15 and decodes those signals to provide the instructions contained by bits 8_{16} through F_{16} of each CRU output word. Table 1-8 lists the instructions provided by the instruction decoder.

Word Select Latch. The word select latch is a flip-flop that latches the Word Select signal from the CRU interface. When NCR15P from the instruction decoder makes a high-to-low-to-high transition, the word select latch's Q output goes to the value of CRDL, the buffered CRUBITOUT from the computer. The word select latch maintains its last state until cleared by the computer (NRL1).

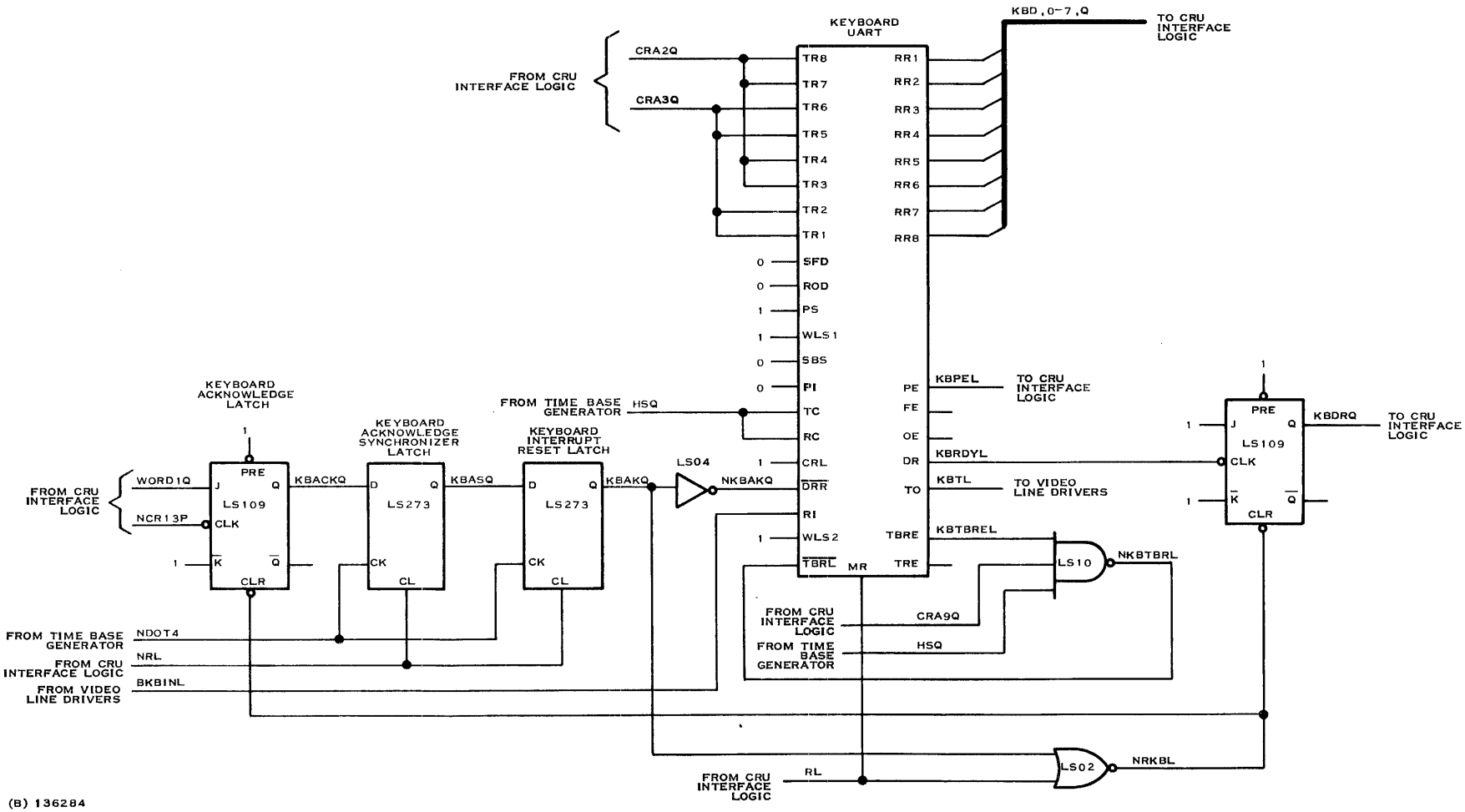


Figure 1-34. Model 911 VDT Keyboard Logic

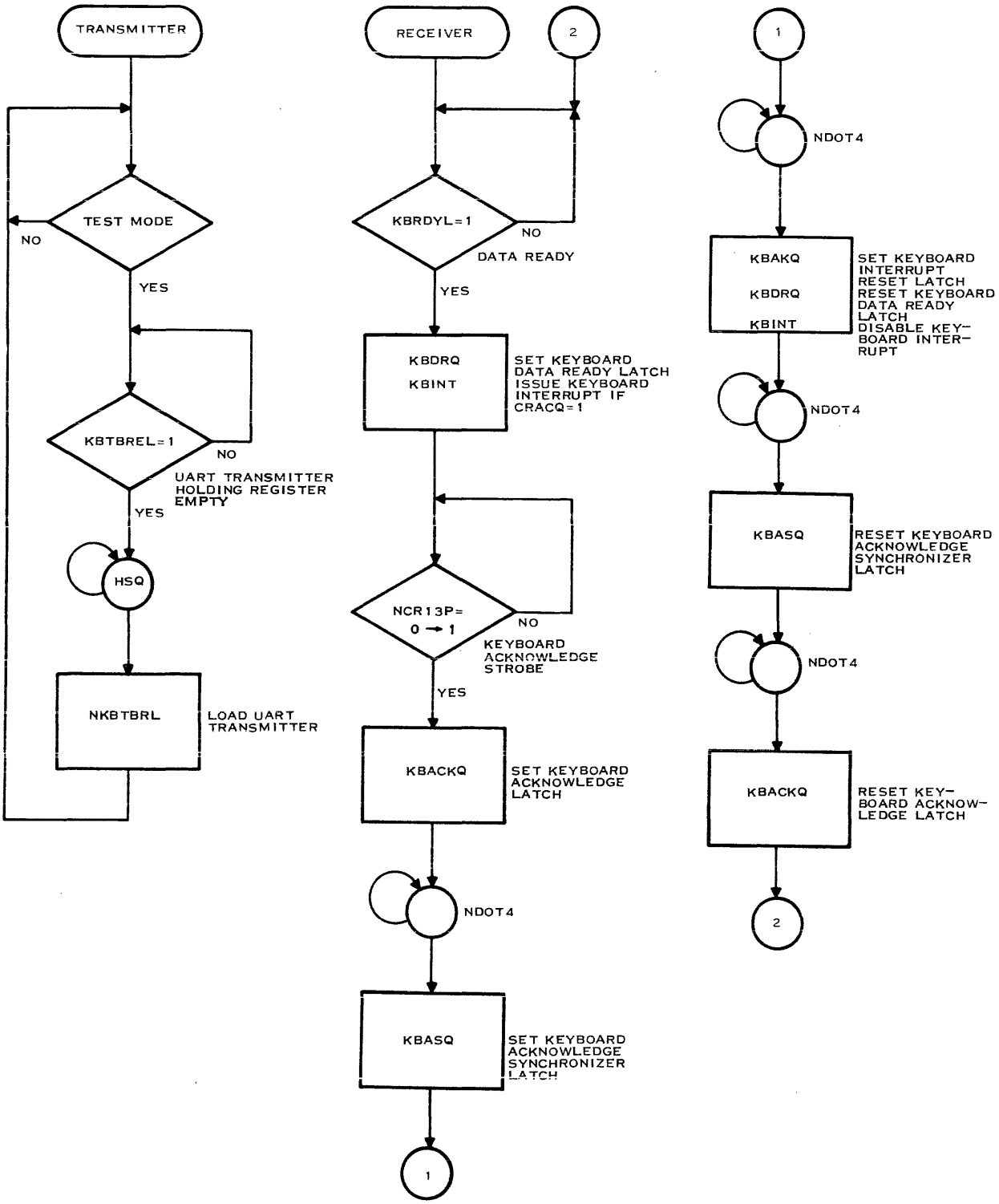


Figure 1-35. Keyboard Logic Flowcharts

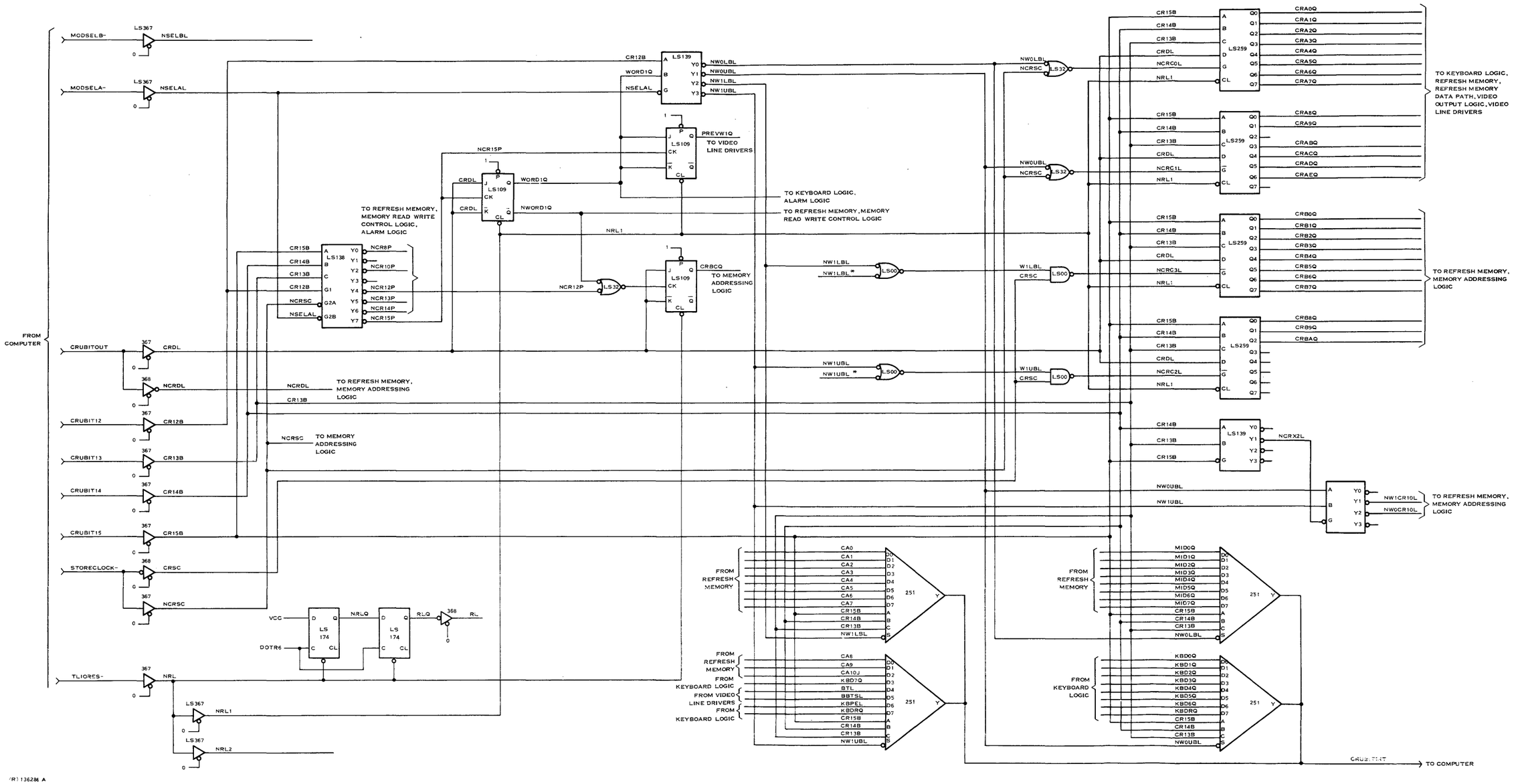


Figure 1-36. CRU Interface Logic

Table 1-8. Instruction Decoder Instructions

CRUBIT, 12-15	CRU Word	Active Output	Instruction
1000	0	NCR8P	Write Data Strobe
1000	1	NCR8P	– – – –
1001	0	No Output	
	1	No Output	
1010	0	NCR10P	Cursor Move } Forces refresh
1010	1	NCR10P	Cursor Move } memory read cycle
1011	0	No Output	
1011	1	No Output	
1100	0	NCR12P	Keyboard Interrupt Enable
1100	1	NCR12P	Display Cursor
1101	0	NCR13P	Dual Intensity Enable
1101	1	NCR13P	Keyboard Acknowledge
1110	0	NCR14P	Display Enable
1110	1	NCR14P	Beep Enable
1111	0	NCR15P	Word Select
1111	1	NCR15P	Word Select

Previous State Flag. The previous state flag latches the output of the word select latch and holds it until reset by the computer (NRL1). The previous state flag is used during the normal mode to indicate the state of CRU output bit F_{16} just prior to the setting of CRU output bit F_{16} to 1 to read the previous state flag.

Cursor Enable Latch. When CRU output bit C_{16} (with output F_{16} = 1) is set, the cursor enable latch (CRBCQ) is set to enable the displaying of the cursor on the CRT screen.

Byte Selector. The byte selector produces signals to gate the write data latches, the CRU control latches, the cursor address latches, and the CRU input bit selectors. Table 1-9 is a truth table for the byte selector that shows which output is active (logic 0) for the possible input combinations of CR12B and WORD1Q. NSELAL (or NSELBL for VDT 1) must be low to enable the byte selector. If NSELAL (or NSELBL) is high, all byte selector outputs are high.

Write Data Latches. The write data latches comprise an eight-bit addressable latch register that always contains the last character written to refresh memory by the CRU. When NW0LBL from the byte selector is low, the write data latches convert the serial data from the computer, CRDL,

Table 1-9. Byte Selector Truth Table

Inputs		
CR12B	WORD1Q	Active Output (Low)
0	0	NW0LBL (Select word 0, bits 0-7)
1	0	NW0UBL (Select word 0, bits 8-15)
0	1	NW1LBL (Select word 1, bits 0-7)
1	1	NW1UBL (Select word 1, bits 8-15)

into eight bits of parallel data, CRA,0-7,Q. Each output is addressable by CR,13-15,B. The CRU data is strobed to the addressed output by NCRSC according to the following scheme:

CR,13-15,B	Selected Output
000	CRA0Q
001	CRA1Q
010	CRA2Q
011	CRA3Q
100	CRA4Q
101	CRA5Q
110	CRA6Q
111	CRA7Q

CRU Control Latches. The CRU control latches are another set of addressable latches with an addressing scheme like that for the write data latches. They are enabled by NW0UBL. The outputs of the CRU control latches provide the following control signals for VDT controller logic:

- CRA9Q – Logic 1 selects test mode.
- CRABQ – Logic 1 enables blinking cursor; logic 0 disables blinking cursor.
- CRACQ – Logic 1 enables Keyboard Interrupt.
- CRADQ – Logic 1 enables Dual Intensity.
- CRAEQ – Logic 1 enables CRT display.

Cursor Address Latches. The cursor address latches provide the inputs to the cursor address register in the refresh memory when addressed according to the same scheme as for the write data latches.

CRU Address Command Decode. The CRU address command decode logic decodes CRU bit A_{16} to provide signals to enable loading, incrementing, or decrementing the cursor address register.

CRU Bit Selectors. The CRU bit selectors decode addresses CR,13-15,B and if enabled by one of the byte select signals at the S input, pass data (D0 through D7) at the selected input to the computer as CRUBITINT.

1.4.4.5 Refresh Memory and Control Logic. Figure 1-37 is a block diagram of the VDT controller's refresh memory and associated control and addressing logic.

During a data retrieval (computer writing to CRT) operation, the computer provides the VDT controller with eight bits of character data over the serial output line (CRUBITOUT). This information determines what is to be displayed on the CRT screen at the current cursor location and whether the displayed information is to be displayed normally or at low intensity. The computer also provides control bits to enable the display and the cursor, and an 11-bit cursor address over the same serial output data line. The cursor address specifies the position on the screen where a symbol is to be altered or displayed and the location in the refresh memory where the information is to be stored. The VDT controller continually reads the contents of refresh memory and converts the ASCII codes to dot patterns that are sent to the CRT.

After the computer has transmitted the write data and address information to the VDT controller, the computer issues a Write Data Strobe on the data line (with module select, four-bit CRU address, and clock). The VDT controller responds by storing the screen data code into its refresh memory at the cursor address provided by the computer.

During typing operations, when data for display on the screen is repeatedly transferred from the keyboard to the computer, and then from the computer to the CRT monitor, the computer may provide the VDT controller with only the initial cursor address. Then, after each character is stored in refresh memory, an increment command is sent by the computer to update the cursor address. A counter in the memory control logic performs the incrementing so that all characters are transmitted in the proper order and stored in refresh memory in consecutive locations. For operations other than transmission of information for display in consecutive locations, the computer provides an 11-bit cursor address for each character to be displayed.

The following discussions describe the operation of the circuitry depicted in figure 1-37.

Memory/CRU Input Data Register. The memory/CRU input data register consists of two quadruple two-input multiplexer latch networks that contain the character at the current cursor location for input to the CRU. Inputs to this register are provided by the computer (CRA,B-7,Q) or the read data latches (MDO,0-7,Q).

When a write data strobe occurs, a memory write cycle is initiated. The write data character (CRA,0-7,Q) is selected by the memory/CRU input data register and latched. This data is then written into memory and is immediately available for input to the computer via the CRU interface.

When the cursor moves (increment, decrement or load new address), a memory read cycle is initiated. Memory output data is selected by the memory/CRU input data register and latched. In this way the register always contains the character stored at the present cursor address.

MIDRC is the clock which controls the memory/CRU input data register. When the clock is high, the register output tracks the selected input, and the output is latched when the high-to-low transition occurs.

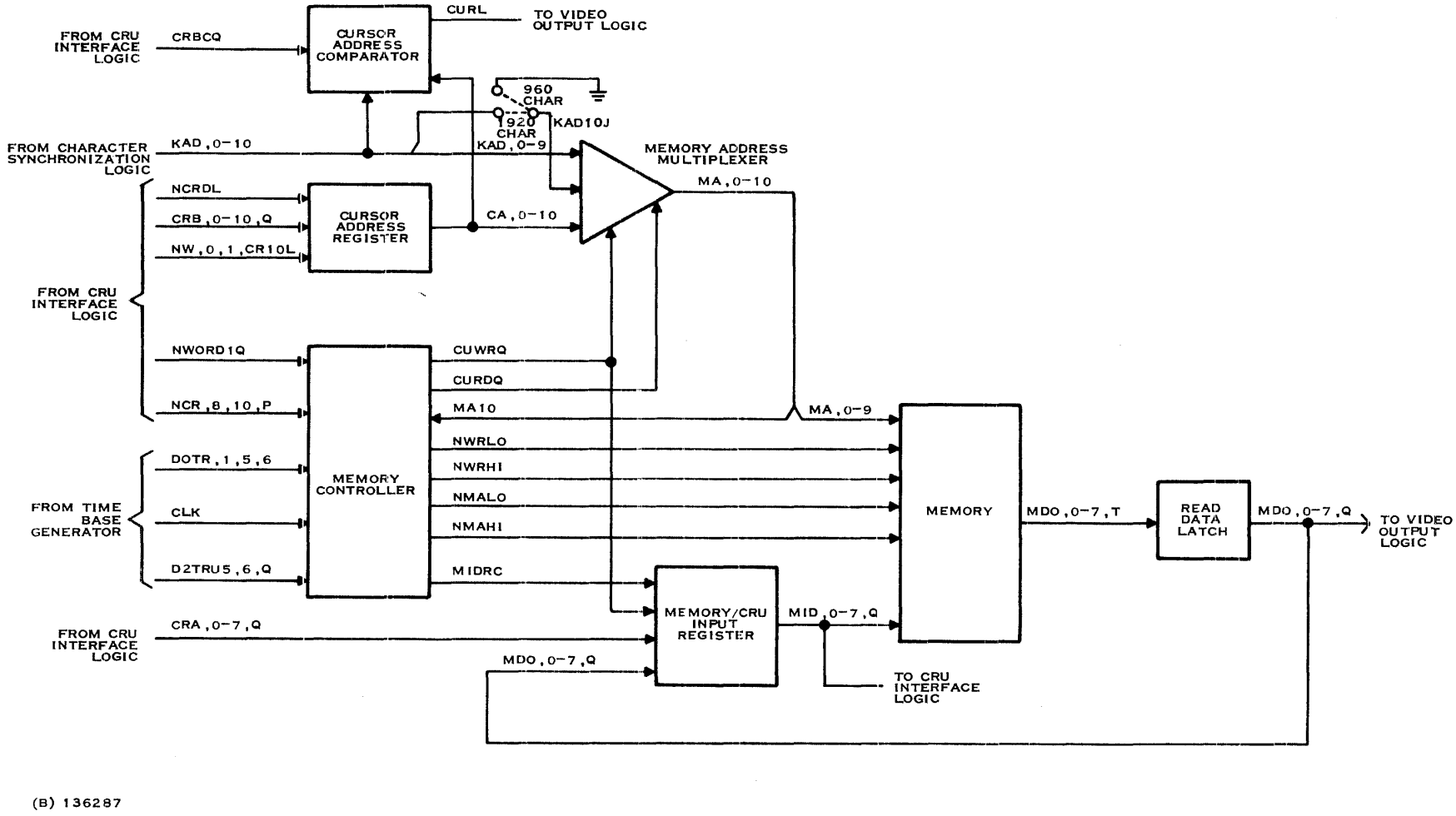


Figure 1-37. Refresh Memory Block Diagram

Memory Array. The memory array consists of 16 TMS4033 1024-word-by-1-bit static RAM chips arranged to provide 2048 (2K) eight-bit words of storage. Data inputs for the memory array are produced by the memory/CRU input data register. Characters are addressed (MA,0-A) by the memory address multiplexer, which provides the address of the present cursor location or the next character required for screen refresh. Only 1024 (1K) eight-bit words of storage are available for the 960-character controller, while the full 2K words are available for the 1920-character controller.

Read Data Latches. The read data latches (see figure 1-38) latch the character data output by the memory array and provide the data to the character generator for producing dot patterns for display on the CRT screen, and to the memory/CRU input data register as the character read at the cursor address when the cursor is moved to a new location.

Memory Control Logic. Figures 1-39 and 1-40 show the control logic associated with the refresh memory, and figures 1-41 through 1-43 are flowcharts for memory control logic.

The circuitry shown in figure 1-39 latches and synchronizes read and write commands from CRU interface logic to control the writing of a character into memory for display by the CRT monitor, and the reading of a character from memory to update the memory/CRU input data register. Synchronization of the read and write commands from CRU interface logic is required because the commands from the computer are asynchronous to the controller.

The circuitry shown in figure 1-40 selects the memory address. The address provided to the memory (MA,0-10) is selected from the character address provided by the time base generator for refresh purposes (KAD,0-10) or the current cursor address provided by the cursor address register (CAD,0-10). The cursor address register output is selected to write a new character at the cursor location or to read the character at the cursor location when the address changes.

1.4.4.6 Video Output Logic. The video output logic shown in figure 1-44 produces (from the outputs of refresh memory and the time base generator's line counter) the video signal for amplification and transmission to the video display unit. The primary character generator produces seven-bit dot codes for each of the eight scan lines addressed by LINE,A-C,Q. If the graphics jumper, P9, is not installed, the video output logic suppresses display of the graphics symbols during scan lines 0 through 7. When a graphic character is presented for display without the graphics option installed and enabled, the entire character space is intensified (low intensity).

The generators for lines 8 and 9 are installed only for implementing graphics on the 1920-character displays and produce seven-bit dot codes for scan lines 8 and 9, respectively, of the 7- X 10-dot character matrix. The latched output of the video output shift register and the outputs of the video output control latches address the selector to provide the composite video signal to be driven out to the power/logic pwb. The composite video signal contains a seven-bit dot pattern for each character of each row of characters to be displayed. Ten scan lines of composite video are produced and transmitted for each row of characters on the CRT monitor screen (two lines are blanked when graphics not installed or eight lines are blanked for 960-character displays). Figure 1-45 illustrates the character space and how it is filled by the three possible matrixes. Figure 1-46 shows the characters produced within the character space on the CRT screen, including the graphics characters. Note that other character generators are substituted to produce the unique symbols for European countries and the Japanese Katakana characters (figure 1-47).

1.4.4.7 Alarm Logic. Figure 1-48 shows the alarm logic on the VDT controller. Whenever Beep Enable is active, AQ goes high to enable the audio logic on the power/logic pwb. NAQ goes low to enable the timer, then allows the timer to run for approximately 0.25 seconds before clearing the alarm flip-flop and disabling the audio logic.

1.4.4.8 **Time Base Generator.** The time base generator produces all the signals necessary for timing and synchronizing VDT controller operations. Figures 1-49 and 1-50 illustrate the logic that makes up the time base generator.

NOTE

A dual-controller VDT controller contains only one time base generator that provides identical functions for both controllers on the pwb.

Oscillator. The oscillator is a monolithic crystal oscillator circuit with crystal, oscillator circuit, and TTL output buffer in a single 14-pin package. The crystal is cut for 11.004 megahertz.

Clock Buffer/Selector. The clock buffer/selector selects the output of the crystal oscillator (PH1) or an externally-produced clock (EXTCLOCK) for use by VDT controller logic. Grounding CEL disables the crystal oscillator so that an external clock may be used. Leaving CEL ungrounded enables the oscillator and disables the external clock (EXTCLK).

The basic clock period of 90 nanoseconds determines the size of elements within a displayed character matrix. For example, alphanumeric characters are five dots across and seven dots high. High-intensity character dots are a full 90-nanosecond dot period, and low-intensity characters are 45-nanosecond half-dot period.

Dot Counter. The dot counter divides the 11.004-megahertz clock (CLK) into seven 1.57-megahertz clocks used to synchronize events throughout the controller. Figure 1-51 illustrates the relationship between CLK and the seven 1.57-megahertz dot clocks. The counter forces zeros into the serial input of a shift register until the first six outputs (DOTR0 through DOTR5) are zero. Then the counter enables a 1 to the shift register input (DOTR6=1) and the next CLK drives DOTR0 to 1.

Interval Timers. The interval timer flip-flops produce two 1.57-megahertz outputs (D2TRU5Q and D2TRU6Q). D2TRU5Q controls memory write enable. D2TRU6Q gates memory addresses and enables the output of the graphic character generator during lines 8 and 9, and the standard character generator during lines 0 through 7.

Character Counter and Character Address Counter. The character counter and character address counter count the number of character positions (0-99) for each scan line and count the character positions as the CRT screen is scanned. Following are specific character address counts for the character address counter:

Character	Count
First displayed character	0
960th character or 960-character screen	$3BF_{16}$
1920th character on 1920-character screen	$77F_{16}$

The maximum allowable count of FFF_{16} is never reached because the counter is reset to 0 at the end of a frame. Figures 1-52 and 1-53 illustrate the counting scheme for 960- and 1920-character displays, respectively.

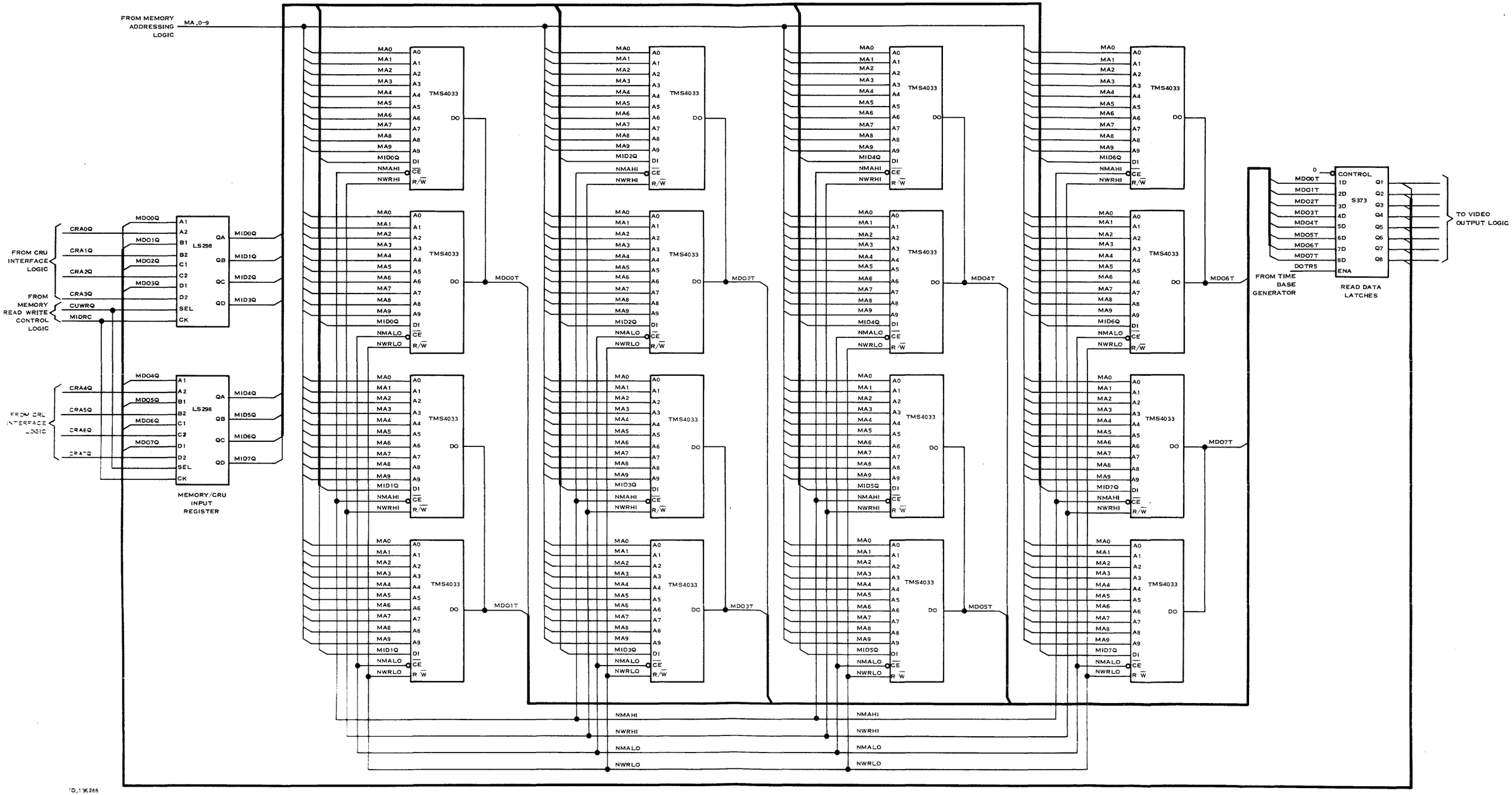


Figure 1-38. Refresh Memory Data Path

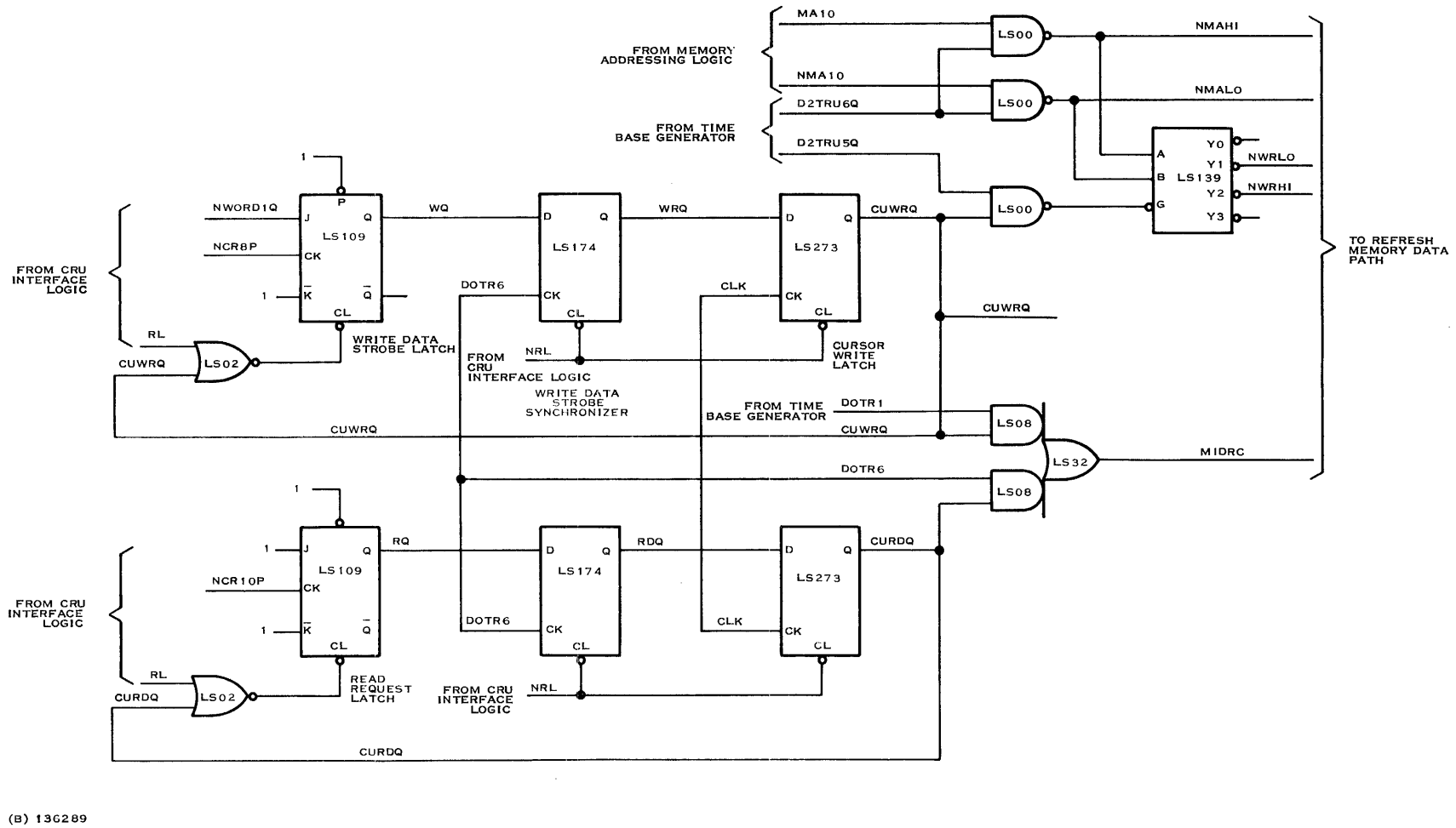


Figure 1-39. Memory Read and Write Control Logic

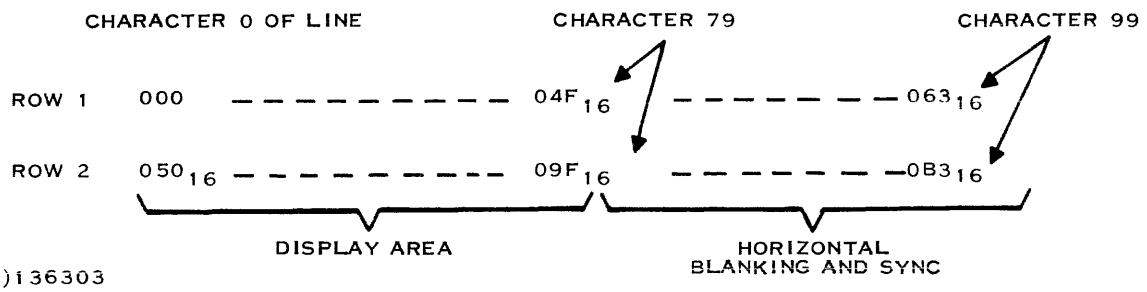
The character counter and character address counter share hardware circuitry. The 12-bit character address counter (KAD,11-0) consists of three hexadecimal counter stages. The carry from the first stage, KCOL, feeds the second stage and the single-stage character counter.

The character address counter is a 12-bit counter that contains the character address that is presented to the cursor address comparator, refresh memory, the character decoder ROM, and the row decoder ROM. The address in the counter is compared to the cursor address. When the two addresses are identical, the next character is fetched from memory for screen refresh at the current cursor location and displayed in reverse video (inside the cursor).

The timer control ROMs (character decoder ROM, row decoder ROM, and sync decoder ROM) decode the output of the character address counter to determine the instantaneous position along a TV scan line (from character time 0 through 99) and the position of the scan line in the raster. The row decode of the most significant bits determines whether the row is in the display region or whether it occurs during vertical retrace (blanking and sync). The row decoder information, along with line decode and character position along a scan line, determines the instant at which events such as horizontal sync, horizontal blanking, vertical sync, and vertical blanking occur.

The character address counter starts counting at 000_{16}. The counter is initialized to 000_{16} after completing a scan of a frame (one noninterlaced sweep of the display screen). A frame is repeated 50 or 60 times per second and the same frequency as the input ac power. A 50-hertz rate requires that 314 lines are scanned, while 262 lines are scanned for a 60-hertz rate. The horizontal scan frequency is 15.720 kilohertz for both 50-hertz and 60-hertz frame rates.

The character address counter divides a scan line into 100 equal segments (character times) – 80 character times for display of 80 characters and 20 character times for horizontal blanking and synchronization. The counter must also have incremented *only* 80 character times at the beginning of the next row of characters. As an example, consider the following illustration of the character address counts for the first and second display rows:



During the scan of the first row, the count progresses from 000_{16} (0_{10}) to 063_{16} (99_{10}). But, since only 80 characters are displayed, the first character of the second row must be read from memory location 050_{16} (not 064_{16}).

The value stored in the character address counter is copied into the character address latch at character time 0 (enabled by K00L) of each scan line (only the most significant eight bits are latched). Figures 1-52 and 1-53 show that the values are 00, 05, 0A, etc. The value in the character address latch is written back into the character address counter at character time 99 (enabled by K99L) (the least significant four bits are cleared). This operation permits the character address counter to continuously count from an initial value, i, to i + 63_{16} (000-063_{16}, 0A0-103_{16}, etc.) for each scan line of a particular row. For the 960-character display, there are

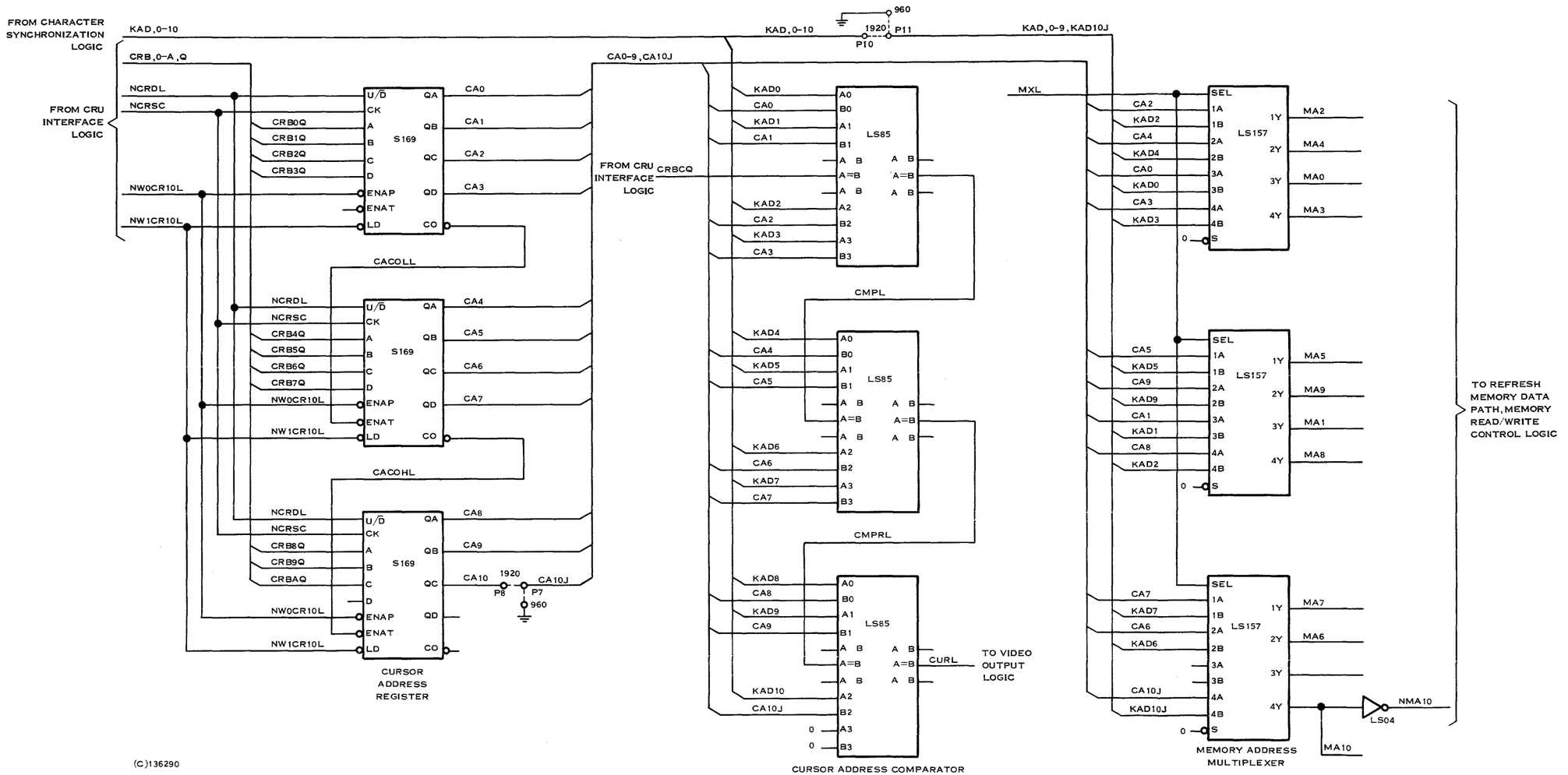


Figure 1-40. Memory Addressing Logic

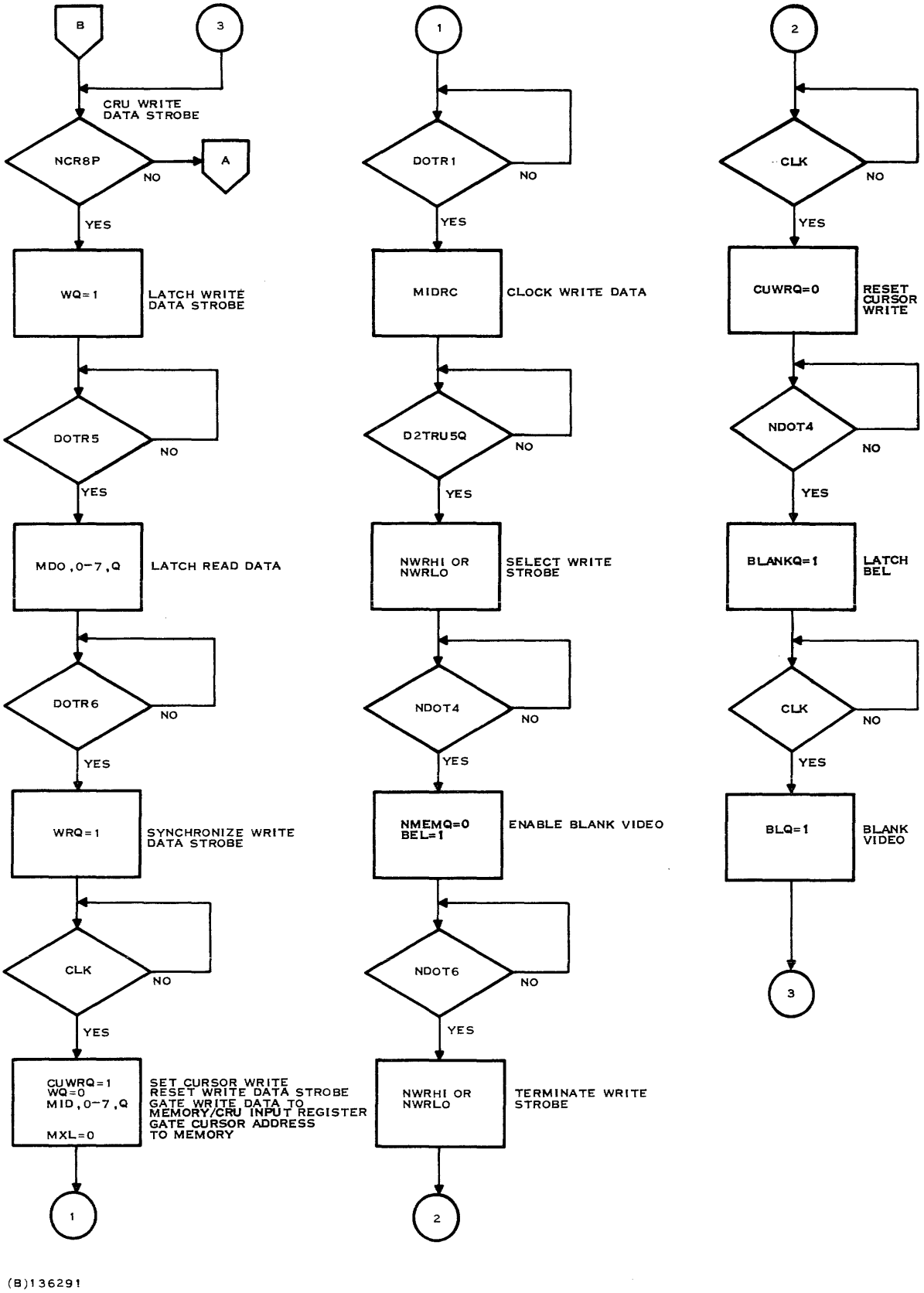


Figure 1-41. Flowchart for Memory Write Operation

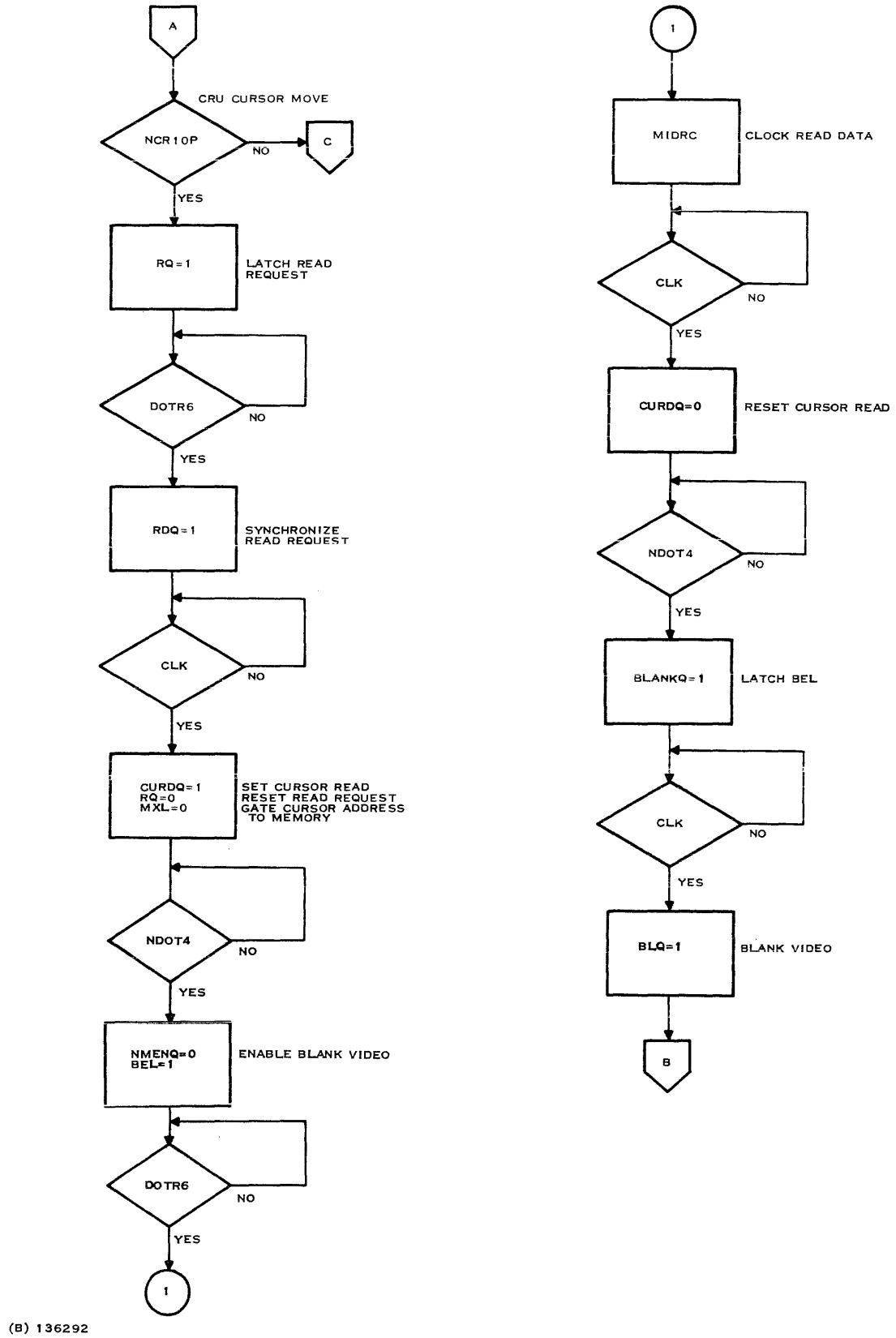


Figure 1-42. Flowchart for Memory Read Operation

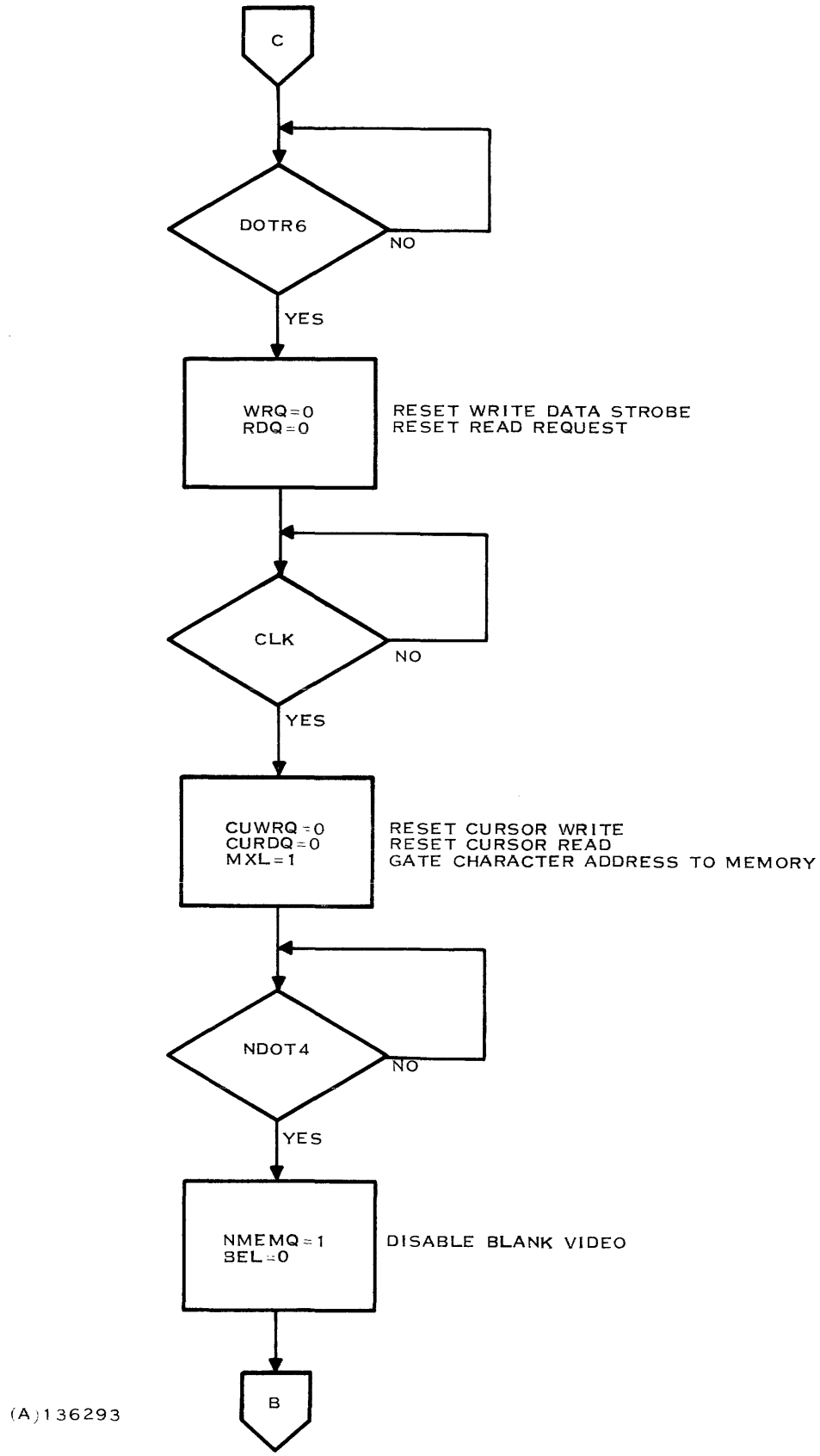


Figure 1-43. Display Screen Refresh Cycle Flowchart

16 scan lines per row; for the 1920-character display, there are 10 scan lines per row. Therefore, each character is read 16 or 10 times (once each scan line) for display on the screen. The ASCII character from each location (even those not displayed during retrace) is presented to the character generator each character time. Then, depending on the line being scanned, a pattern is produced to develop the video for that particular character.

The first character of the row following the current row is *not* the next character in sequence in the character address counter. The contents of the character address counter are copied into the character address latch during character 0 (for the row, not the scan line). The value in the character address latch is modified during the scan of the last line of every row at character time 90 (trailing edge of HSQ – horizontal sync). This places the value in the latch (05_{16} in the case of the first row) required to initialize the character counter at the end of the scan line. The latch contents are then written into the counter as 050_{16} as the first character (character 0) of the second row.

Notice that during the scan of the first row, characters 000 through $04F_{16}$ are displayed, and characters 050_{16} through 063_{16} (normally displayed in second row) are accessed during horizontal retrace. Characters 050_{16} through 063_{16} are not displayed (at this time) even though their addresses are presented to memory, a character is read from memory, and an output (VDQ) is produced by the video output shift register. The video output shift register's output is blanked by the video output amplifier. (If the VDT controller were in the self-test mode, VDQ would still be returned to the computer.) Likewise, if the cursor is at some location (052_{16}, for example) the comparator logic indicates a cursor compare operation while scanning row 0, but the compare does not affect the blanked screen.

NOTE

The character address counter values change in such a way that unique character values *cannot* be decoded along a scan line (e.g., the last (99th) character of row 0 is 063_{16}; of row 1 is $0B3_{16}$; of row 2 is 103_{16}, etc.).

The least significant four bits (KAD,3-0) are valid since they are set to 0 at the beginning of each scan line. The carry (KCOL) from this stage of the character address counter is used to enable the character counter to develop KCH,0-2. The character counter is set to 0 at the end of every scan line (K99L).

Character Decoder ROM. KAD(3-0) and KCH(2-0) are decoded by the character decoder ROM as shown in table 1-10 to produce the following signals:

Standard (Row) Character	Signature	Description
0	KOOL	Character time 0
74	HDEQSL	End sync during vertical sync
79	HBSL	Start horizontal blanking
82	HDSL	Start horizontal drive
90	HDENDL	End horizontal drive
90	NHDENDL	Inverted end horizontal drive
99	K99L	Character time 99
99	NK99L	Inverted character time 99

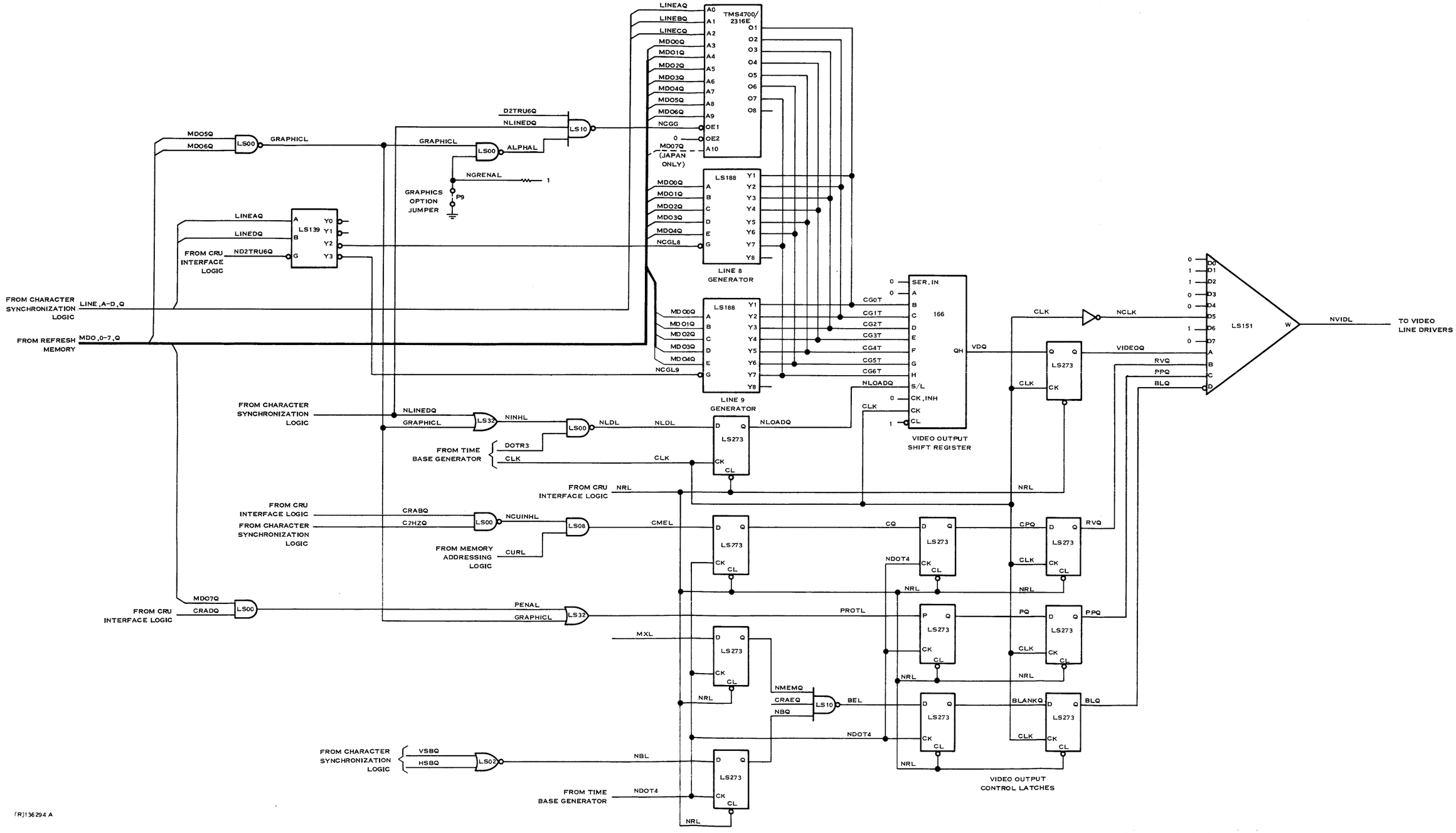


Figure 1-44. Video Output Logic

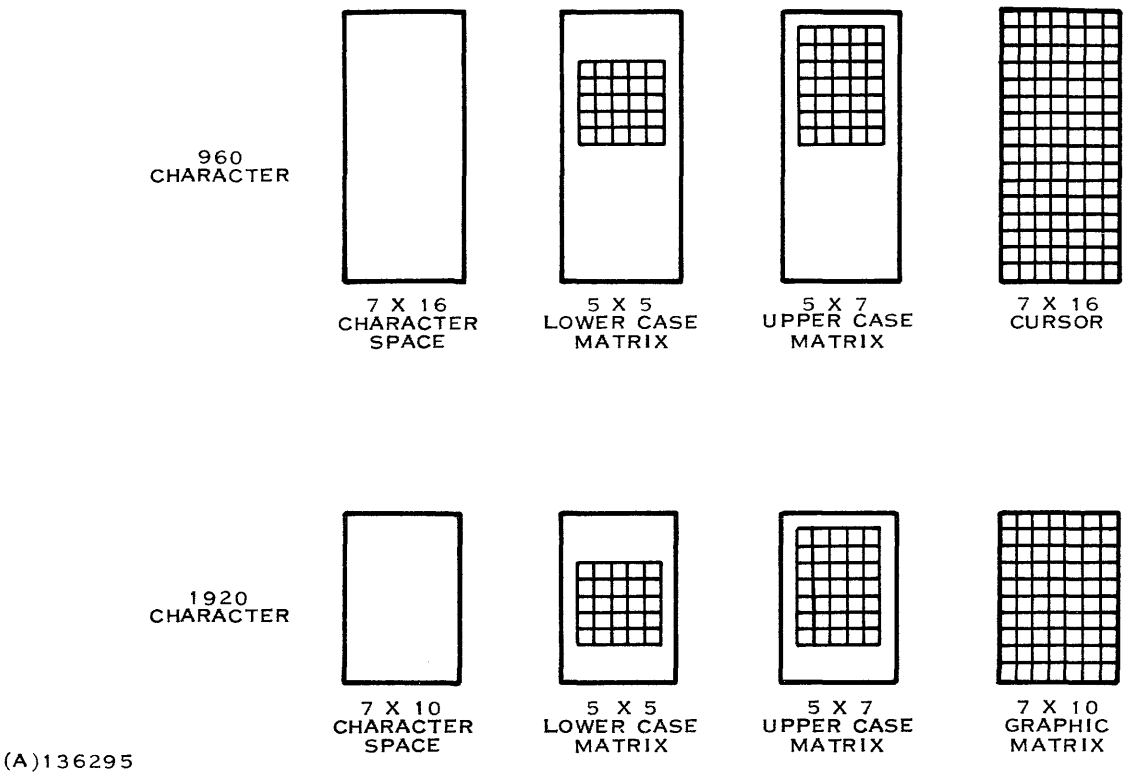
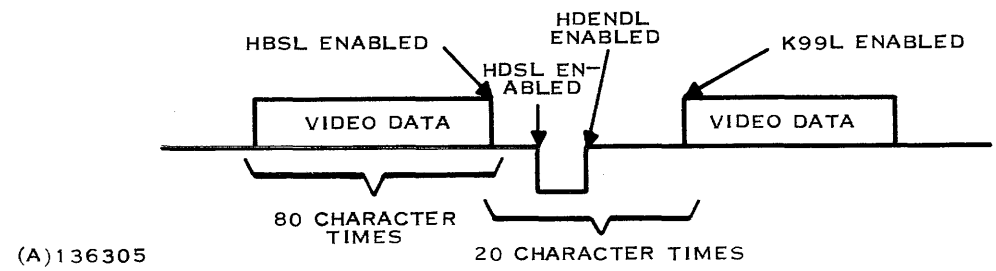
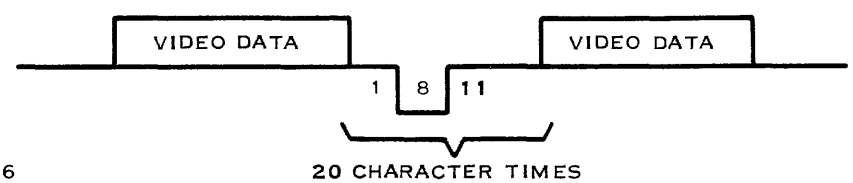


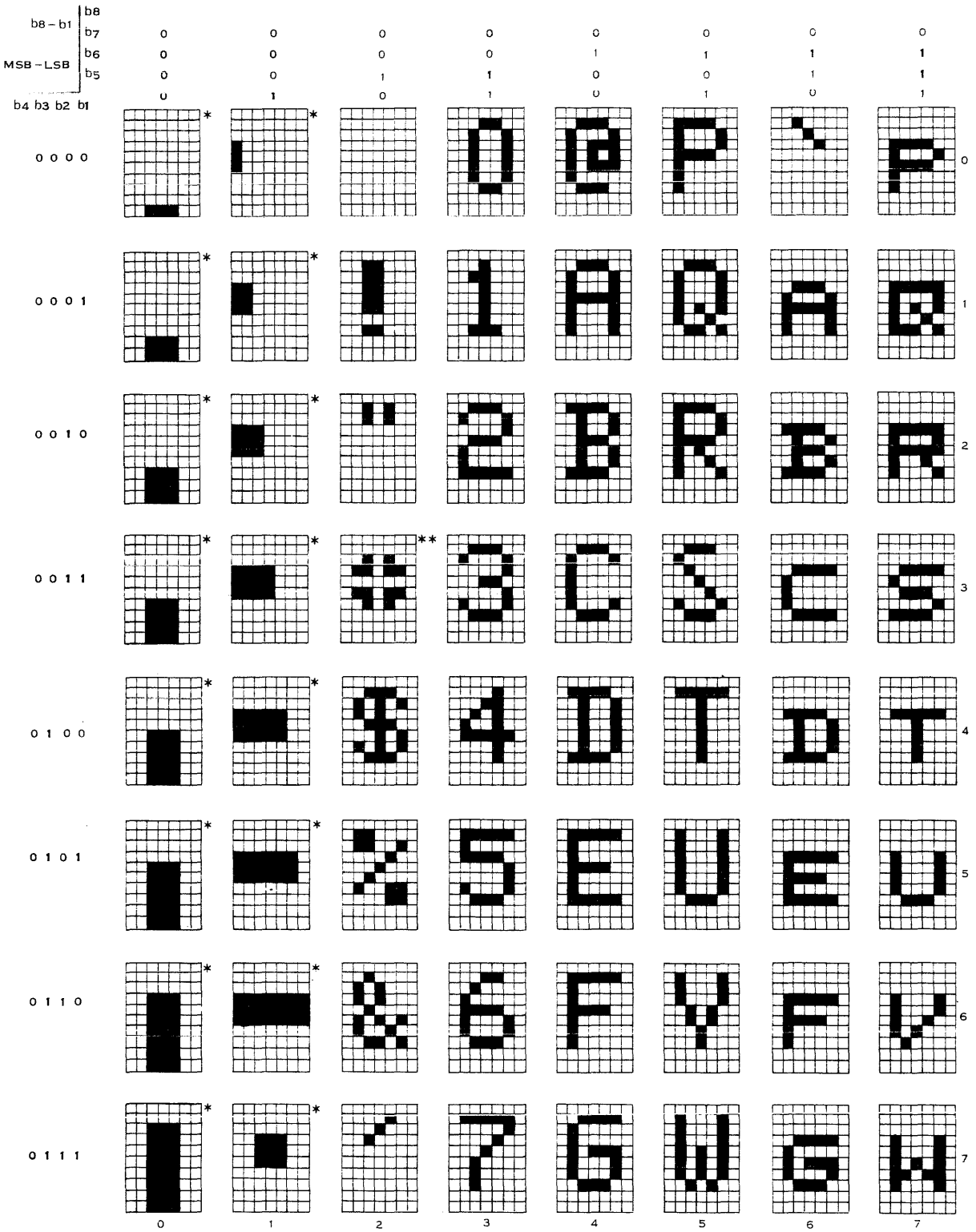
Figure 1-45. Model 911 VDT Character Matrix Formats

The standard character times decoded to begin and end events do not depend on ac input frequency (50 or 60 hertz) or display size (960 or 1920 characters). They can change with a new control ROM to permit different synchronization. The standard Model 911 VDT format requires the following relationship between video data and synchronization signals.



By changing the character times decoded, the standard RS170 format can be generated as follows:



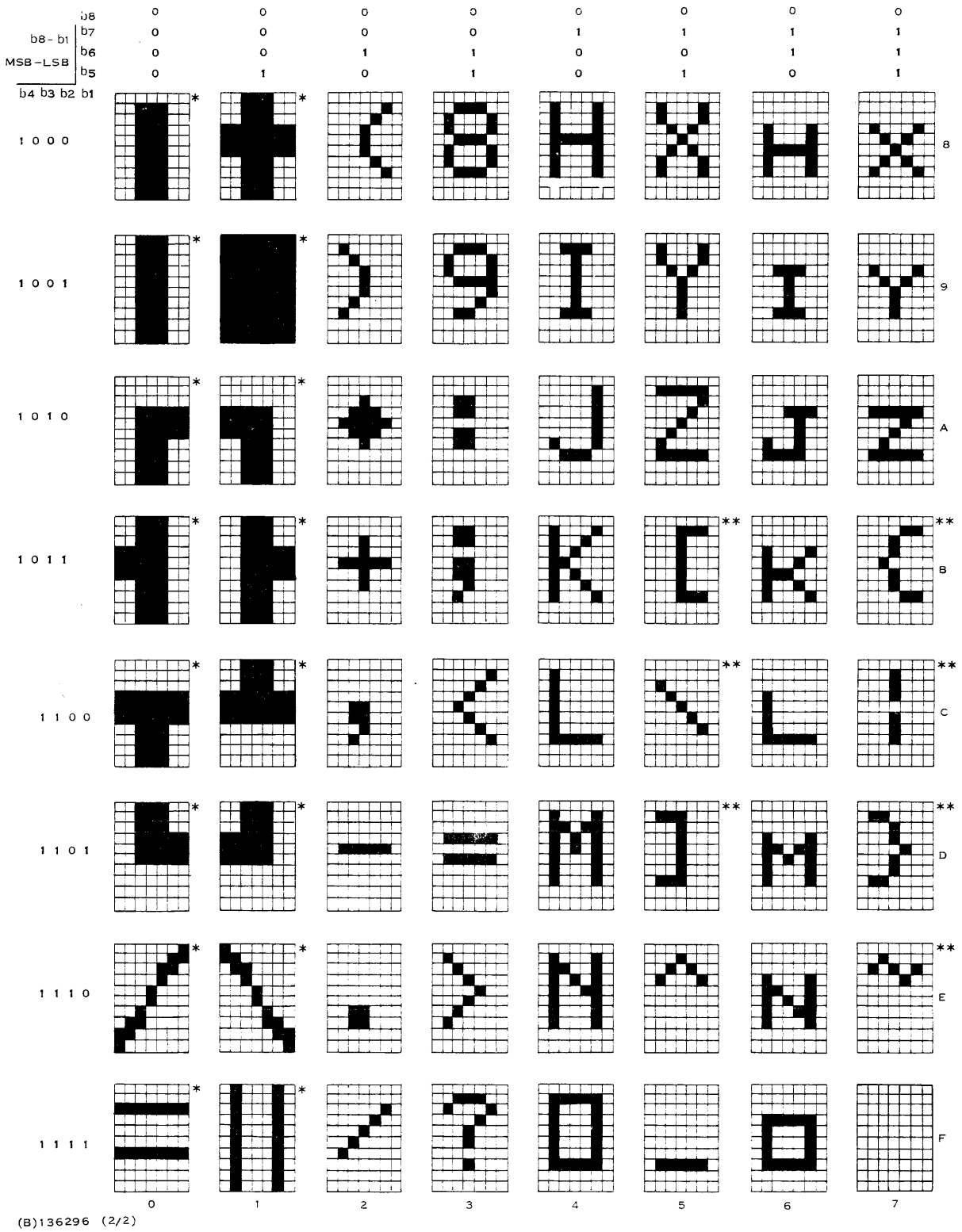


* GRAPHICS (1920-CHARACTER DISPLAY ONLY)

** REFER TO FIGURE 1-47 FOR EUROPEAN AND JAPANESE CHARACTER SETS THAT VARY FROM THOSE SHOWN.

B) 136296A (1/2)

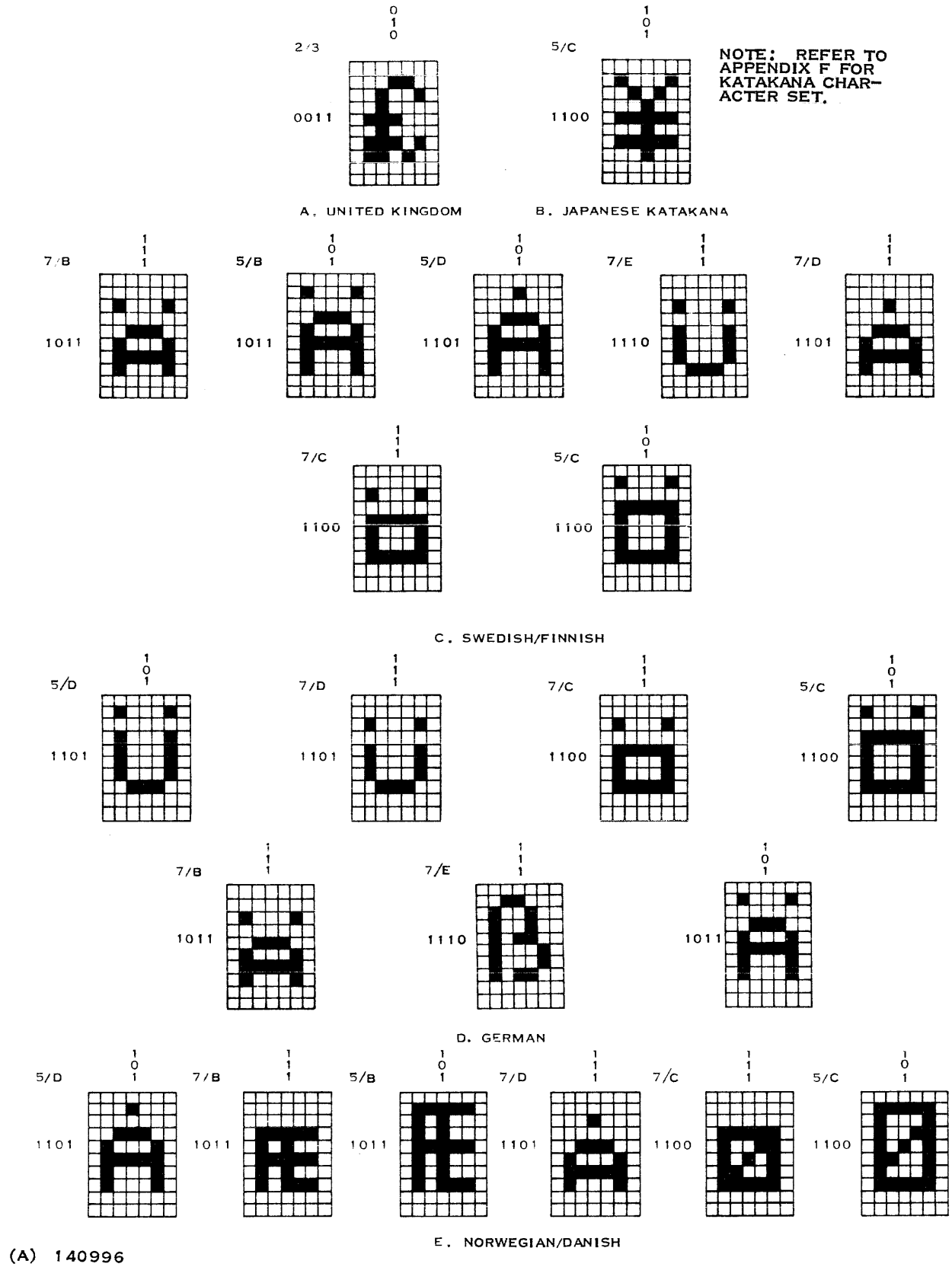
Figure 1-46. Model 911 VDT Displayed United States Character Set, Including Graphics Symbols (Sheet 1 of 2)



* GRAPHICS (1920-CHARACTER DISPLAY ONLY)

** REFER TO FIGURE 1-47 FOR EUROPEAN AND JAPANESE CHARACTER SETS THAT VARY FROM THOSE SHOWN.

Figure 1-46. Model 911 VDT Displayed United States Character Set, Including Graphics Symbols (Sheet 2 of 2)



(A) 140996

Figure 1-47. Model 911 VDT International Displayed Characters

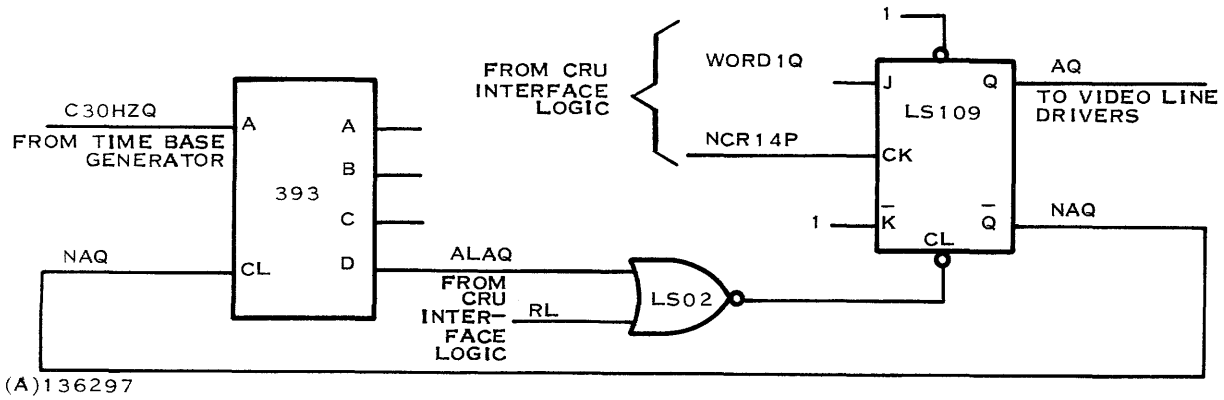


Figure 1-48. Model 911 VDT Alarm Logic

The RS170 ROM can be used to drive an industry standard monitor, but not a Model 911 Video Display Terminal.

Row Decoder ROM. Table 1-11 shows the input-output relationships for the row decoder ROM. The ROM's inputs are from the character counter (KAD,11-6) and the character decoder ROM. The outputs are as follows:

Output	Description
EVSL	Enable vertical sync for this row
EENDL	Enable end of frame for this row
EVBL	Enable vertical blanking for this row

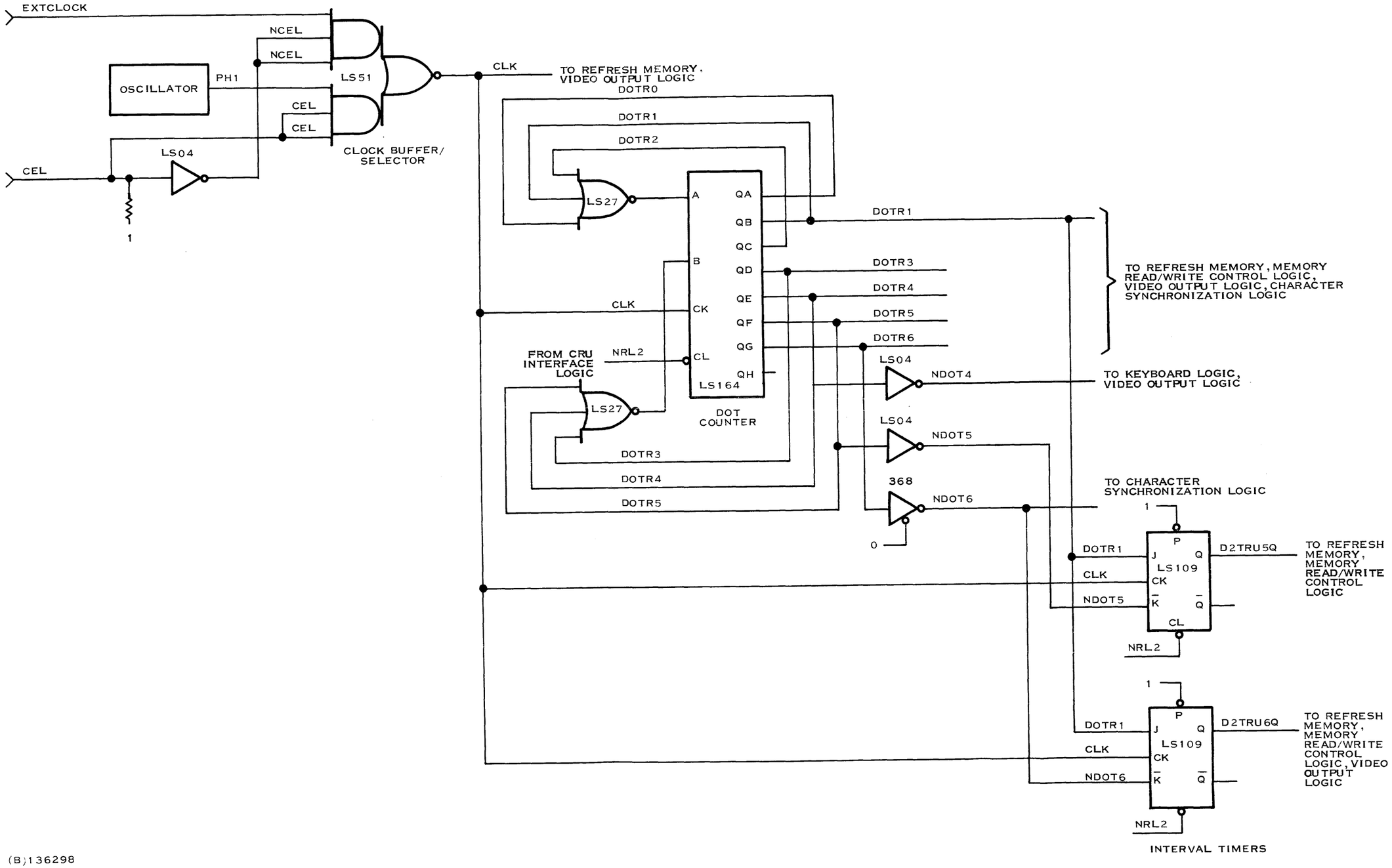
As shown in table 1-11, there are four configurations for the row decoder ROM, dependent upon input ac power frequency and display character capacity.

The row decoder ROM's outputs are provided to the sync decoder ROM where they are used with line and character information to determine the positions on the screen at which events occur.

Sync Decoder ROM. Table 1-12 shows the input-output relationships for the sync decoder ROM. The ROM's inputs are row enables (EENDL, EVSL, and EVBL) from the row decoder ROM, the outputs of the line counter (LINE,D-A,Q), and Character 79 (HDSL) from the character decoder ROM. These inputs provide character, line, and row information that permits specification of times at which events must occur, such as end frame, start vertical sync, etc..

The sync decoder ROM outputs are:

Output	Description
NVGSL	Enable end vertical sync
VSL	Enable vertical sync
ENDL	Enable end frame
VBL	Enable vertical blanking



(B)136298

Figure 1-49. Model 911 Video Display Controller Time Base Generator Oscillator and Dot Clock

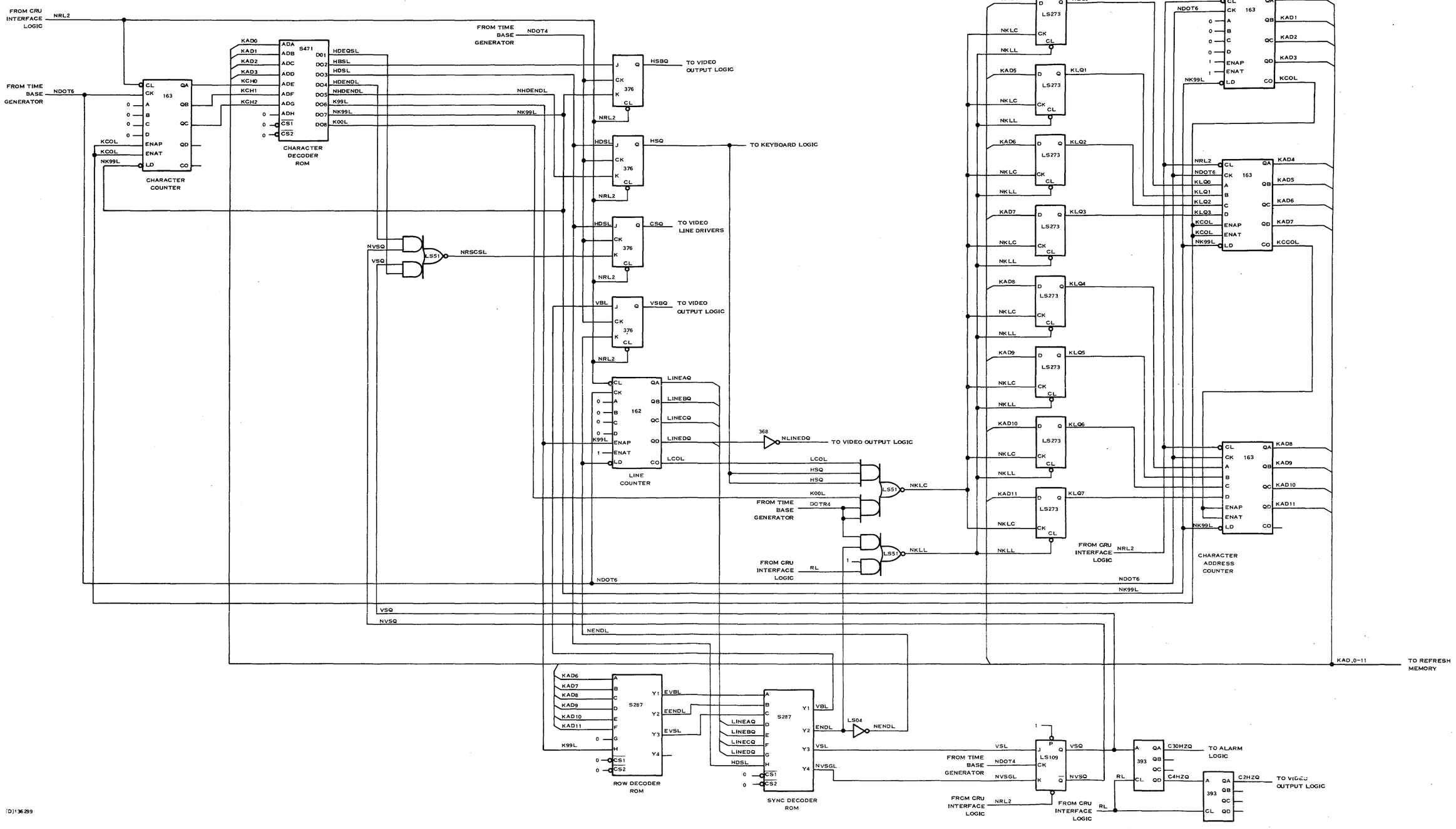


Figure 1-50. Model 911 VDT Time Base Generator Character Synchronization Logic

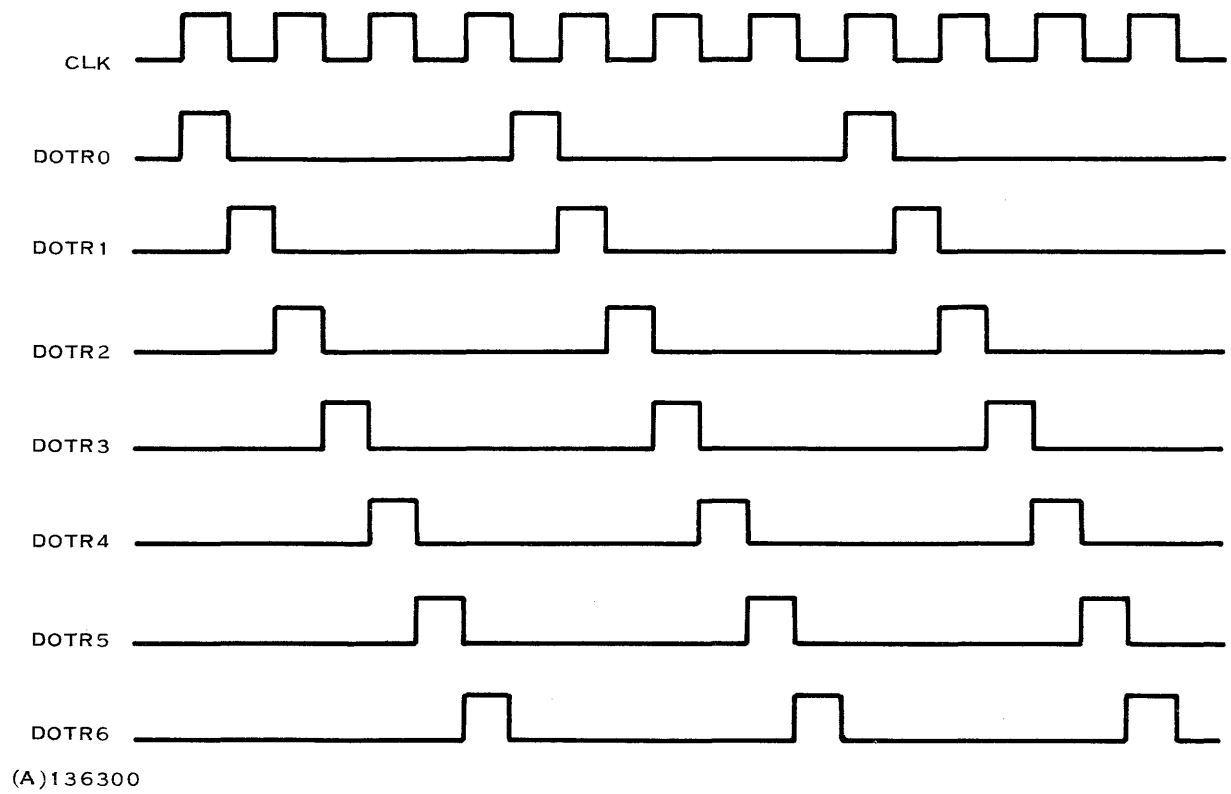


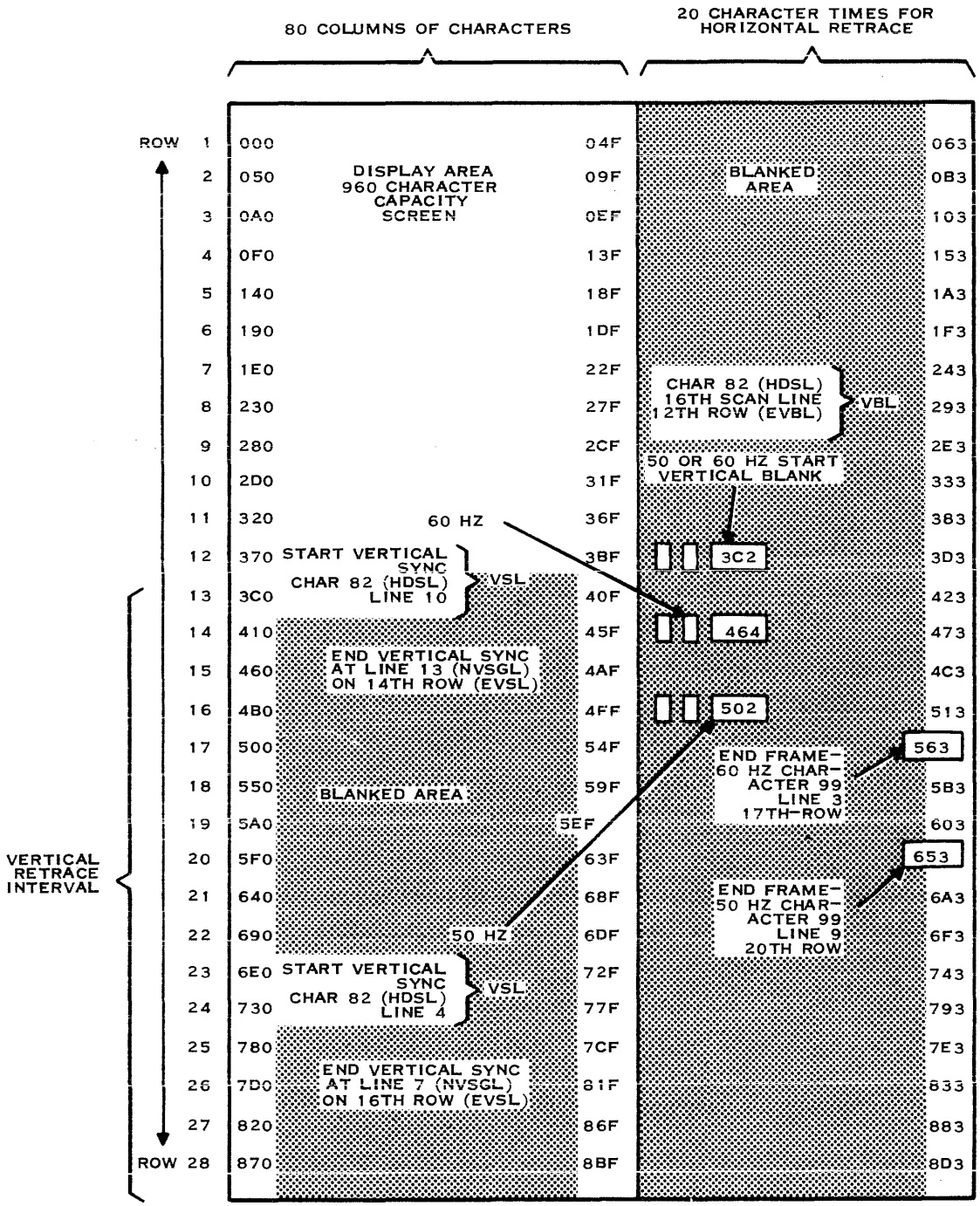
Figure 1-51. Model 911 VDT Dot Counter Outputs

Sync Generator. Outputs from the control ROMs (see tables 1-10 through 1-12) control the flip-flops that comprise the sync generator to produce the following sync timing control signals.

- HSQ – Horizontal Sync
- HSBQ – Horizontal Blanking
- VSQ, NVSQ – Vertical Sync
- VSBQ – Vertical Blanking
- CSQ – Composite Sync
- NBQ – Composite Blanking

Figure 1-54 illustrates the timing relationships for the sync generator.

Composite Blanking (NBQ) indicates that either HSBQ or VSBQ is high (logic 1), and blanks output video.



(A)136301

Figure 1-52. Model 911 VDT 960-Character Display Character Address Counting Scheme

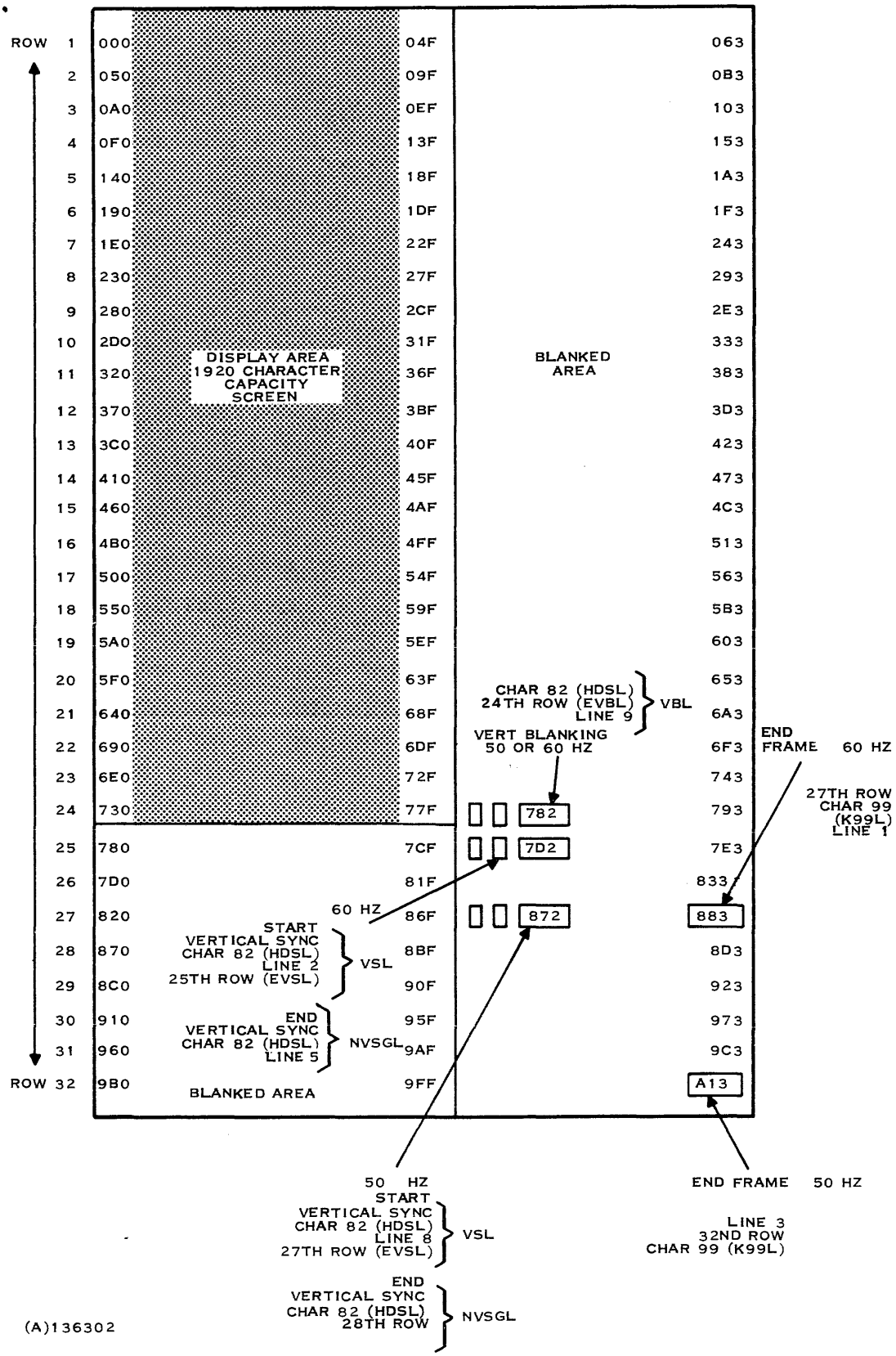


Figure 1-53. Model 911 VDT 1920-Character Display Character Address Counting Scheme

Table 1-10. Model 911 VDT Character Decoder ROM Table

ROM INPUTS									ROM OUTPUTS								
H	G	F	E	D	C	B	A		D8	D7	D6	D5	D4	D3	D2	D1	
GROUND *	KCH2	KCH1	KCH0	KAD3	KAD2	KAD1	KAD0	CONFIG-URATION	K00L	NK99L	K99L	NHDENDL	HDENDL	HDSL	HBSL	HDEQSL	
X	0	0	0	0	0	0	0		1	1	0	1	0	0	0	0	0 + 128
X	1	1	0	0	0	1	1		0	0	1	1	0	0	0	0	63 + 227
X	1	0	1	1	0	1	0		0	1	0	0	1	0	0	0	90 + 218
X	1	0	1	0	0	1	0	BALL DRIVE	0	1	0	1	0	1	0	0	82 + 210
X	1	0	0	1	1	1	1		0	1	0	1	0	0	1	0	79 + 207
X	1	0	0	1	0	1	0		0	1	0	1	0	0	0	1	74 + 202

* ROM IS PROGRAMMED TO BE INDEPENDENT OF UNUSED H INPUT.

(A)136304

Composite Sync (CSQ) indicates that either HSQ or VSQ is high. Composite Sync is *not*, however, the logical OR of HSQ and VSQ. During vertical sync, Vertical Sync is serrated with pulses similar to Horizontal Sync to maintain horizontal synchronization during vertical synchronization. The positive transition of Composite Sync is always enabled at character time 82. During vertical sync the negative transition occurs at the next character 74 time. Normally (not during vertical sync), the negative transition occurs at character time 90.

Table 1-11. Model 911 VDT Row Decoder ROM Table

ROM INPUTS									ROM OUTPUTS				
H	G	F	E	D	C	B	A		D4	D3	D2	D1	
K99L	GROUND	KAD11	KAD10	KAD9	KAD8	KAD7	KAD6	CONFIG-URATION	NOT USED	EVSL	EENDL	EVBL	REMARKS
X	X	X	X	1	1	1	1	50 HZ 960 CHAR PN 948554-8	0	0	0	1	ROW12,3C0-3FF
1	X	0	1	1	0	0	1		0	0	1	0	ROW20,640-67F,CHAR 99
X	X	0	1	0	1	0	0		0	1	0	0	ROW16,500-53F
X	X	0	1	1	1	1	0	50 HZ 1920 CHAR PN 948554-6	0	0	0	1	ROW24,780-7BF
1	0	1	0	1	0	0	0		0	0	1	0	ROW32,A00-A3F,CHAR 99
X	X	1	0	0	0	0	1		0	1	0	1	ROW27,840-87F
X	X	X	X	1	1	1	1	60 HZ 960 CHAR PN 948554-4	0	0	0	1	ROW12,3C0-3FF
1	X	X	1	0	1	0	1		0	0	1	0	ROW17,540-57F, CHAR 99
X	X	X	1	0	0	0	1		0	1	0	0	ROW14,440-47F
X	X	X	1	1	1	1	0	60 HZ 1920 CHAR PN 948554-2	0	0	0	1	ROW24,780-7BF
1	0	1	0	0	0	1	0		0	0	1	0	ROW27,880-8BF, CHAR 99
X	X	X	1	1	1	1	1		0	1	0	0	ROW25,7C0-7FF

NOTE: ROW DECODES ARE FOR THE CHARACTER COUNT AT TIME HDSL WHICH IS NORMALLY CHARACTER TIME 82 SINCE END IS AN EVENT THAT OCCURS AT THE END OF A LINE (CHARACTER TIME 99), THE DECODE ADDRESS IS THE ONE WHICH WILL BE VALID AT K99L TIME.

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Table 1-12. Model 911 VDT Sync Decoder ROM Table

ROM INPUTS									ROM OUTPUTS				
H	G	F	E	D	C	B	A		D4	D3	D2	D1	
HDSL	LINEDQ	LINECQ	LINEBQ	LINEAQ	EVSL	EENDL	EVBL	CONFIG-URATION	NVSGL	VSL	ENDL	VBL	REMARKS
1	1	1	1	1	0	0	1	50 HZ 960 CHAR PN 948554-9	1	0	0	1	HDSL · LINE15
X	1	0	0	1	0	1	0		1	0	1	0	LINE9
1	0	1	0	0	1	0	0		1	1	0	0	HDSL · LINE4
1	0	1	1	1	X	X	X		0	0	0	0	HDSL · LINE7
1	1	0	0	1	0	0	1	50 HZ 1920 CHAR PN 948554-7	1	0	0	1	HDSL · LINE9
0	0	0	1	1	0	1	0		1	0	1	0	LINE3
1	1	0	0	0	1	0	0		1	1	0	0	HDSL · LINE8
1	0	0	0	1	X	X	X		0	0	0	0	HDSL · LINE1
1	1	1	1	1	0	0	1	60 HZ 960 CHAR PN 948554-5	1	0	0	1	HDSL · LINE15
0	0	1	0	1	0	1	0		1	0	1	0	LINE5
1	1	0	1	0	1	0	0		1	1	0	0	HDSL · LINE10
1	1	1	0	1	X	X	X		0	0	0	0	HDSL · LINE13
1	1	0	0	1	0	0	1	60 HZ 1920 CHAR PN 948554-3	1	0	0	1	HDSL · LINE9
X	0	0	0	1	0	1	0		1	0	1	0	LINE1
1	0	0	1	0	1	0	0		1	1	0	0	HDSL · LINE2
1	0	1	0	1	X	X	X		0	0	0	0	HDSL · LINE5

NOTE: STANDARD TIME FOR HDSL IS CHARACTER TIME 82.

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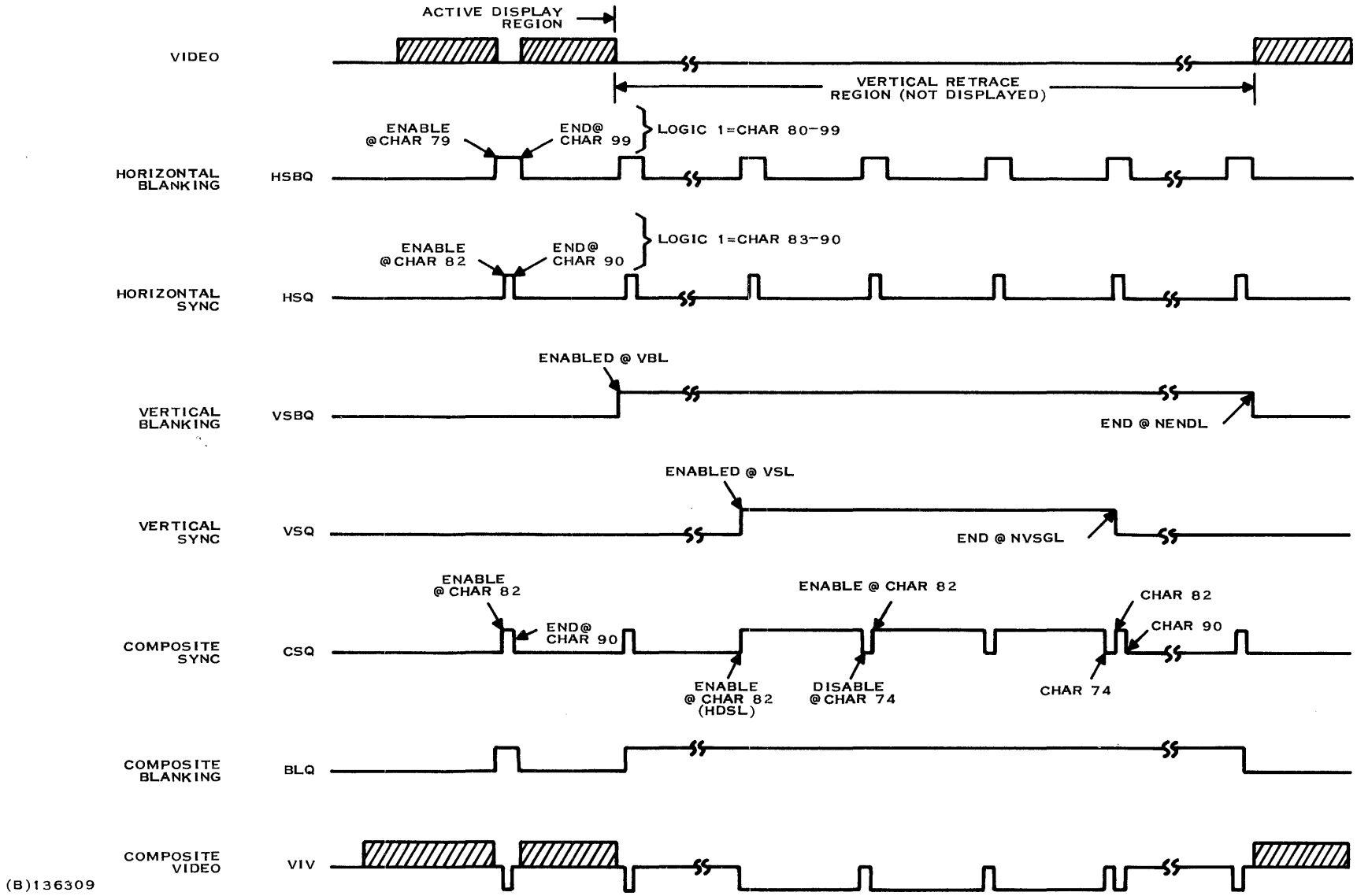

Figure 1-54. Model 911 VDT Sync Timing Diagram

SECTION II

MAINTENANCE

2.1 GENERAL

This section describes the maintenance philosophy for the Model 911 Video Display Terminal and provides troubleshooting procedures to assist in fault isolation to the component level. Component replacement procedures are given in the system depot maintenance manual for the appropriate Model 990 series computer.

2.2 MAINTENANCE PHILOSOPHY

Depot maintenance for the Model 911 Video Display Terminal is based upon the use of a diagnostic test executing in a hot mock-up system incorporating a Model 990 series computer, a Model 990 Maintenance Unit, and a combination dual-trace oscilloscope/digital multimeter as shown in figures 2-1 and 2-2.

The Model 911 Video Display Terminal is tested using the 911 VDT diagnostic and its error messages to troubleshoot the terminal. Component-level fault isolation is accomplished by using the diagnostic to establish scoping loops through the portion of the terminal under test and checking the logic with the aid of the logic diagrams in *Model 990 Computer Family Maintenance Drawings*.

The keyboard subassembly is tested by connecting the keyboard to an operable video display unit and observing the code displayed by the row of LEDs on the rear of the video display unit as each keyboard key is struck. Faults are recorded and thus isolated to the replaceable component by checking the faulty circuit from the cable connector at the video display unit back through the cable and through as much of the keyboard assembly's circuitry as is necessary to locate the fault.

The VDT controller and the power/logic board in the video display unit are tested by running the diagnostic with the controller or video display unit installed in a hot mock-up system, observing the error messages, and acting upon the indications given by the error messages. Scoping loops are established by continuously repeating (looping) performance tests that give error indications. The circuitry being exercised is then probed around the loop to isolate faulty components or by executing diagnostic utility routines which exercise specific logic areas (e.g., CRU interface, cursor address register, memory read/write, etc.).

2.3 SPECIAL TEST EQUIPMENT

The special test equipment required to perform depot maintenance on the Model 911 Video Display Terminal includes:

- Model 990 Computer hot mock-up system
- 911 VDT diagnostic, part number 2250101-1006 – Fully linked object for 990/10 – Fully linked object for front panel.

Diagnostic medium (card, diskette, cassette) must be specified. Part number does not reflect medium.

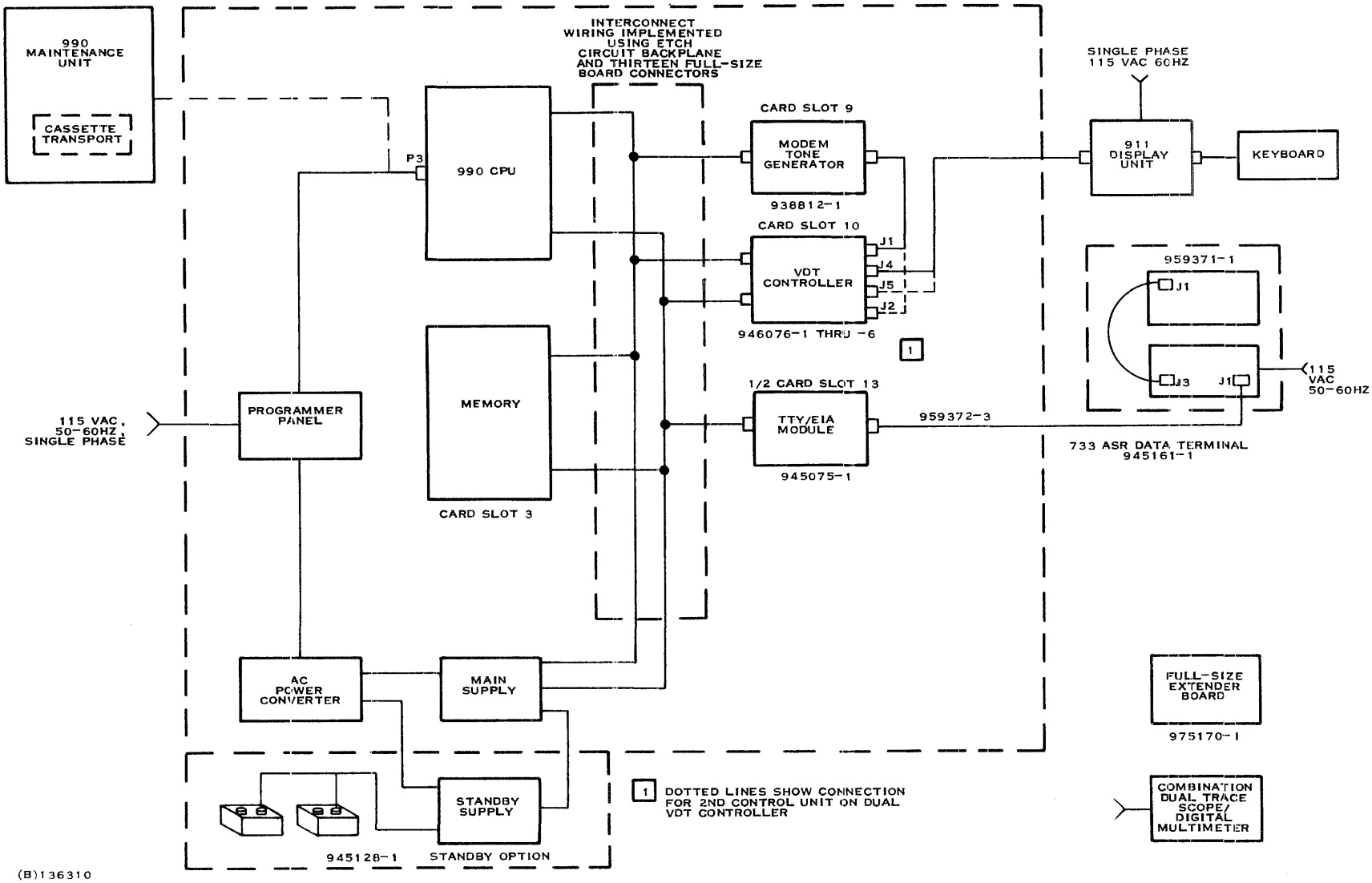

Figure 2-1. Model 990 Computer Hot Mock-Up System for 60-Hertz Model 911 VDT Testing

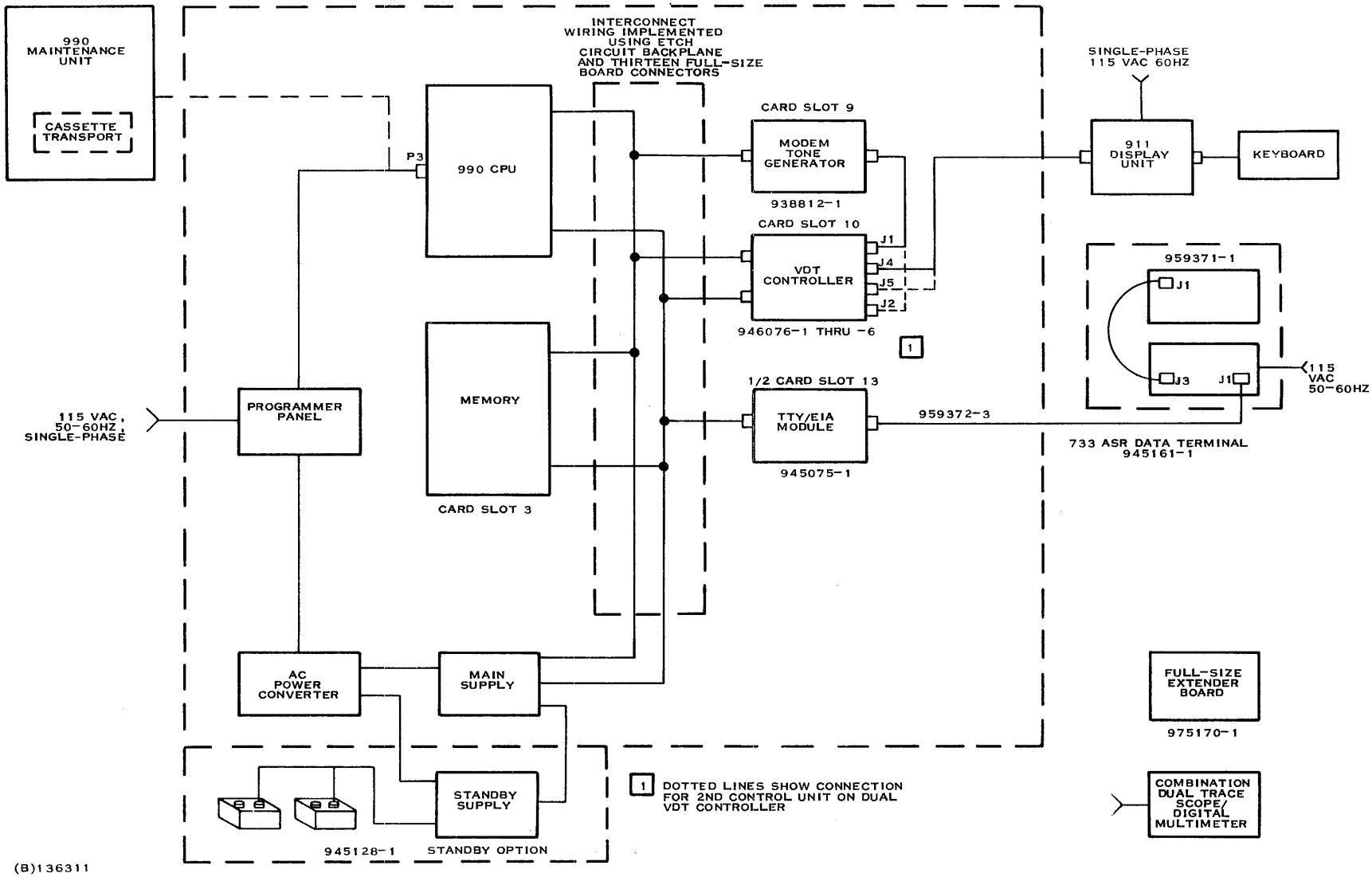

Figure 2-2. Model 990 Computer Hot Mock-Up System for 50-Hertz Model 911 VDT Testing

2.3.1 **HOT MOCK-UP SYSTEM.** Operating instructions for the hot mock-up system are provided in the system depot maintenance manual for the appropriate Model 990 series computer.

NOTE

Refer the the manufacturer-supplied user manuals for oscilloscope/ digital multimeter operating procedures.

2.3.2 **DIAGNOSTIC.** The 911 VDT diagnostic executes under control of the VERBPAC to test and facilitate fault diagnosis within a Model 911 Video Display Terminal consisting of a keyboard, a VDT controller, a video display unit and interconnecting cables. If a VDT controller pwb contains logic for two controllers, the board responds to two CRU base addresses. The diagnostic must be executed for each controller using the appropriate CRU base address for each execution.

An error counter records detected failures. Accumulated errors are printed upon conclusion of each routine. When loop routines (L1, L2, L3, etc.) are executed, the accumulated count is printed after each pass through a test part. If error messages are suppressed, error counts may be observed by aborting the current test (depress "@" on the keyboard of the interactive device) and using the Print Error Count (PE) verb.

2.3.2.1 **Loading the Diagnostic.** Following are procedures for loading the 911 VDT diagnostic into a hot mock-up system from a Model 733 ASR Data Terminal.

1. Apply power to hot mock-up system.
2. Insert cassette containing 911 VDT diagnostic (part number 2250101-1006) into Model 733 ASR Data Terminal cassette transport. Set 733 POWER switch to ON.
3. Set 733 CONT START/STOP switch to STOP.
4. Press 733 REWIND switch for appropriate cassette transport.
5. Set 733 KEYBOARD, PLAYBACK and PRINTER switches to LINE.
6. Set 733 OFF LINE/ON LINE switch to ON LINE.
7. Press 733 LOAD/FF and wait for READY indicator.
8. Set programmer panel key switch to UNLOCK.
9. Press programmer panel LOAD switch.

2.3.2.2 **Using the Diagnostic.** There are two versions of the performance demonstration test: one is for the Japanese model; the other is for the United States and European models. Consult the operating instructions for procedures involving operator interaction during diagnostic testing. Detailed information about the scope of each test is provided in the program description.

United States and European
- Program description – 911 VDT diagnostic part number 2250101-9901
- Operating instructions – 911 VDT diagnostic part number 2250101-9920

Japanese Katakana
- Program description – 911 VDT diagnostic part number 2250253-9901
- Operating instructions – 911 VDT diagnostic part number 2250253-9920

2.3.2.3 **Special Verbs.** Two special verbs can be used with the 911 VDT diagnostic to make the diagnostic more versatile and to allow more specific fault isolation. Those verbs are CU (Cursor Move) and CD (Modify VDT Memory/Scope Loop Verb).

Cursor Move Verb. The Cursor Move verb permits the operator to move the cursor from any memory location to any other memory location (displayed or not displayed). Initially, the verb performs the following:

1. Resets Self-Test and clears Keyboard Interrupt Enable
2. Enables video and nonblinking cursor.

Cursor commands are used with the Cursor Move verb to specify the function. The cursor commands are as follows:

- U – Up one position
- D – Down one position
- L – Left one position
- R – Right one position
- C – To column zero
- Z – To row zero
- A – Direct cursor address
- I – Iterate direct cursor address

The Cursor Move verb is entered from the keyboard of the hot mock-up system's Model 733 ASR Data Terminal by typing –CU–x, where x is any of the cursor commands except A and I, in response to the diagnostic message, VERB?. The cursor commands, A and I, are entered as follows:

1. Wait for message, VERB?.
2. Enter –A or –I.
3. Wait for message –nnnn (hexadecimal value of current cursor location).
4. Enter –mmmm (hexadecimal value of desired cursor location).

Following are examples of printed lines following entry of the Cursor Move verb:

- VERB? –CU –U
- VERB? –CU –A –0377 –0000

Entering @ terminates the Cursor Move verb.

All cursor commands except A and I affect only the cursor position and provide no additional information. Cursor commands, A and I, cause the current cursor address to be read and displayed and allow the operator to specify any memory location (displayed or not displayed) as the new cursor location. Cursor command, A, permits a new entry after each cursor move operation. The cursor command, I, continuously writes the operator-selected cursor address into the controller register.

Modify VDT Memory/Scope Loop Verb (CD). The Modify VDT Memory/Scope Loop Verb (CD verb) assists the operator in the isolation of a system or unit fault. The CD verb allows the operator to modify the data at the current cursor address which may point to any address (displayed or not displayed) in VDT memory. The CD verb can also activate useful routines for scoping. The CD verb has five commands, as follows:

- S – Read or read and modify memory character at current cursor address.
- R – Read or read and modify memory character at current cursor address and move cursor right one position.
- F – Free form input mode.
- SL – Modify and read data at cursor address.
- C – Exercise CRU interface.
- D – Write pattern to screen (Japanese Katakana model only).

The command S allows the operator to read memory data at the current cursor address and to write new data at that location without changing the cursor address. The data in the read data register following this operation is the result of a CRU data transfer, not an actual memory read operation. Figure 2-3 illustrates the entry of the five CD verb commands.

The command R. reads the memory contents at the current cursor address and allows the operator to modify the memory contents at that location. The command then increments the cursor address and reads again.

The command F permits free-form input to the screen from the terminal's keyboard. The command is initiated from the hot mock-up system's 733.

The command SL reads refresh memory at the current cursor address and allows the operator to modify memory at that location (memory write). Following acceptance or modification of the data byte, the program continuously cycles performing a write followed by an increment and decrement of the cursor address to cause memory read operations. This loop permits scoping of a memory write operation followed by two memory reads using an operator-selected data pattern.

The command C exercises the CRU address bits (and word select circuitry) in a tight loop for scoping.

The command D, available only on the Japanese Katakana model, allows the operator to specify a two-character sequence that is written to the entire screen. This pattern could then be used to check display parameters such as geometry, size, and forms.

The CD verb is terminated by entry of @.

When using the CD verb, the display screen initially contains the data written by the most recently completed test. If a particular pattern is desired, it can be quickly initialized using the CD–F command or by executing test E4 of the diagnostic (character test).

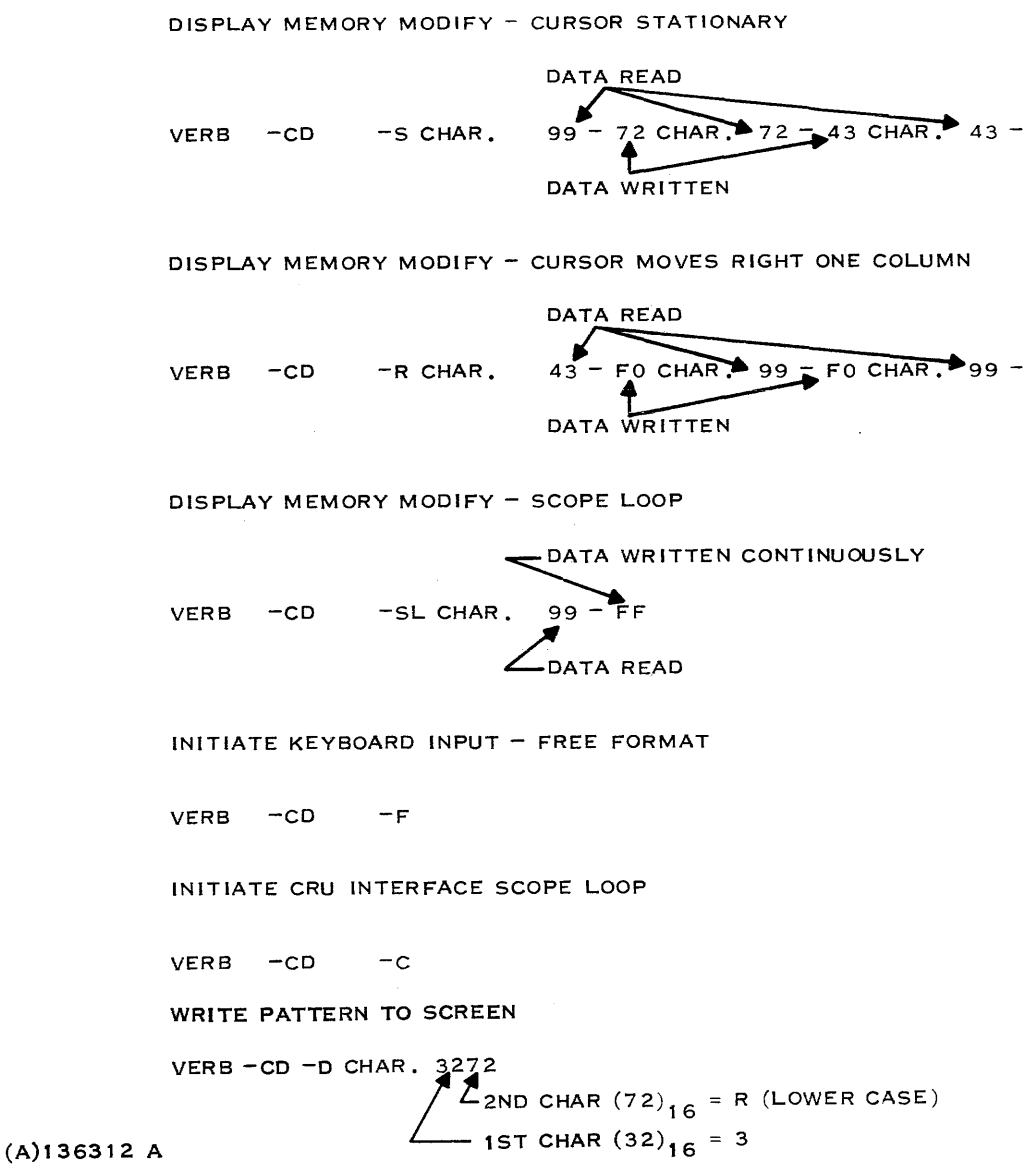

Figure 2-3. CD Verb Entry

2.4 GENERAL MAINTENANCE PROCEDURES

Maintenance procedures consist of a preliminary checkout of the suspect unit to determine if any problems exist which might be visually detected and fault isolation procedures to locate faulty circuit components. The following paragraphs describe those procedures as they apply generally to the components of the Model 911 Video Display Terminal. More detailed procedures for specific components are included with the discussions of maintenance procedures for the components.

2.4.1 PWB PRELIMINARY CHECKOUT. Upon receipt of a suspect pwb from the field maintenance facility, visually inspect the board for the following:

- Broken board
- Loose or missing components
- Damaged (broken) components, wires, etc.
- Broken or missing heat sinks
- Broken, missing, or disconnected jumper wires
- Breaks in etched circuitry
- Foreign materials lodged between package pins that may be causing short circuits.

If a thorough visual inspection indicates no problems, proceed with the fault isolation procedures for the pwb.

2.4.2 GENERAL FAULT ISOLATION PROCEDURES. Each component of the Model 911 Video Display Terminal is tested individually by incorporating the suspect component into the hot mock-up system shown in figure 2-1 or 2-2. All components of the system, except the unit to be tested, should be verified to be operable. The 911 VDT diagnostic is loaded and executed in accordance with the instructions in the *Model 990 Computer Diagnostics Handbook,* part number 945400-9701. The diagnostic is used, with the special verbs available, to establish scoping loops for the unit under test.

2.4.2.1 Scoping Loops. A scoping loop is a short repetitive software program which establishes and maintains a set of conditions in the circuitry under observation so that an error of normally brief duration can be observed and isolated. Once an error message has been printed, determine which test was being performed from the printout of the 733 or the CRT screen. Failure of diagnostic test part E1, E2, or E3 may be looped by activating the L1, L2, or L3 verb, respectively.

2.5 KEYBOARD MAINTENANCE PROCEDURES

Keyboard maintenance procedures consist of a preliminary checkout to determine if any problems exist which might be visually detected, and fault isolation procedures to locate faulty circuit components. The following paragraphs describe those procedures.

2.5.1 KEYBOARD PRELIMINARY CHECKOUT. Upon receipt of a suspect keyboard from the field maintenance facility, visually inspect the assembly for any indications of damage from dropping or mishandling. Note any indications for future reference. Perform the following procedure to check out the keyboard prior to troubleshooting.

1. Turn keyboard assembly upside down and remove four screws.
2. Grasp keyboard assembly at both ends to keep cover top and bottom from separating and turn assembly upright.

3. Lift off top half of case to expose keyboard logic.

NOTE

With the top of the keyboard housing removed, the front of the pwb can be raised and rotated back over the cable entry point for access to the bottom side of the pwb.

4. Visually inspect the pwb for the following:

- Broken board
- Loose edge connector
- Loose or missing components
- Damaged (broken) components, wires, etc.
- Breaks in etched circuitry
- Foreign materials lodged between component pins that may cause short circuits.

2.5.2 KEYBOARD FAULT ISOLATION PROCEDURES. With the keyboard assembly opened, connect the keyboard into the hot mock-up system (see figure 2-1) as the only component in the system whose operation is doubtful. Load the 911 VDT diagnostic as directed in paragraph 2.3.1.1 and initiate the keyboard portion of part E4 of the diagnostic.

The following discussion applies to the United States keyboard. European keyboards differ only in character assignments within the matrix chart, (figure 2-4). Japanese Katakana and European matrix charts are shown in the appendixes.

One distinctive keyboard failure is the generation of two different characters with one depression of a data key. When this situation exists, there are usually nine keys that may exhibit this behavior. The cause for this is usually a solder bridge, usually at one of the scanned matrix diodes. Tracing a solder bridge requires a chart of the scanned matrix and the 911 keyboard logic diagram.

Depress one of the affected keys and note the character(s) generated. These two characters should point to two distinct columns of the matrix chart. Depressing another affected key should give two more characters appearing in the same two columns; one character in each. The key depressed each time is one of the characters, and *one* column in the matrix will contain all the same characters that the depressed key represents. An example of this: depressing the 'N' key produces the characters 'N' and 'J'. Then the column that the legend 'N' appears in (see figure 2-4) represents all the affected keys. On the chart, the legend 'G' is in the same column with 'N', so depressing it gives 'G' and 'V'. Depress those keys that produce the characters appearing in the *other* column. One key should provide a double character and the rest single, correct characters. This key should be noted and, using sheet 2 of the logic diagram, locate the diode's associated number. Go to this diode on pwb and look carefully for solder bridge. If, after eliminating a solder bridge, the problem still exists, then there might have been two diodes, each bridged, affecting the same keys. If there are more than nine keys generating double characters, multiples of nine keys will be affected, meaning at least two bridges, functioning independently. Track down columns affected and treat each set independently. If the diodes are clean, and problem still exists, check etch patterns for bridges. (The bridge does not necessarily occur at a diode.)

Table 2-1 lists fault isolation procedures for the keyboard.

X \ Y	0	1	2	3	4	5	6	7	8	9
0	ERASE FIELD	PRINT	←	INSERT CHAR.	ERASE INPUT	↑	HOME	↓	→	DELETE CHAR
1	F1	F2	F3	F4	F5	F6	F7	F8	CMD	NOT USED
2	0	1	2	3	4	5	6	7	8	KEY 91 NOT USED
3	•	ESC	RETURN	TAB SKIP	KEY 67 NOT USED	= / —	→ FIELD ←	| / I	? /	FOR KEY 3
4	] / –	→ CHAR ←	: / ;	> / .	[/ +	P	L	< / ,	) / 0	0
5	K	M	N	J	I	(/ 9	B	H	U	* / 8
6	& / 7	Y	G	V	C	F	T	^ / 6	SPACE	X
7	D	R	% / 5	Z	S	E	$ / 4	# / 3	W	NOT USED
8	@ / 2	! / 1	Q	ENTER	A	KEY 89 NOT USED	NOT USED			NOT USED

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Figure 2-4. United States Model 911 VDT Keyboard Matrix Chart

Table 2-1. Model 911 VDT Fault Isolation Procedures Keyboard

Symptom	Probable Cause	Possible Solution
One keystroke, two or more identical characters generated, one specific key	Debounce capacitor of encoder either missing or wrong value	Check C2 for presence, value, tolerance, or solder bridge.
	Excessive keyswitch bounce greater than 5 msec	Replace contacts of keyswitch.
One keystroke, two different characters generated, occurs with nine keys or multiples of nine keys	Solder bridge on scan lines or multiple solder bridges on scan lines, of pwb	Strike keys with those legends which correspond to the second characters generated and see which key(s) also generate dual characters. Solder bridge(s) along scan lines, usually on diodes associated with these keys.
On power-up, keyboard in repeat mode with some random character	Main 26-pin connector not fully seated on mating connector	Disassemble keyboard, check mating of 26-pin connector.
	Solder bridge across repeat key contacts	Check for solder bridge.
	Repeat key contacts damaged when keycap installed, and they are shorting	Remove keycap, check contact functionality.
Dead data key, exclusive of shift, control, UCL, and repeat keys	Diode assigned to this key either in pwb backwards, missing or bad	Check diode for presence, check forward/backward resistance with VTVM.
	Contacts may be spread too far, contacts may be missing, contacts damaged when keycap installed	Remove keycap, inspect and check for functionality.
	Solder bridge across key terminal	Inspect pwb for solder bridge.
	Flow solder missed contacts	Inspect pwb for missing solder.
Tab/skip key generates two different characters with one keystroke	Dummy key under double wide keycap has contacts installed	Desolder contacts, pull out with needle-nose pliers.
	Solder bridge on scan lines or multiple solder bridges on scan lines, of pwb	Strike keys with those legends which correspond to the second characters generated and see which key(s) also generate dual characters. Solder bridge(s) along scan lines, usually on diodes associated with these keys.

Table 2-1. Model 911 VDT Fault Isolation Procedures Keyboard (Continued)

Symptoms	Probable Cause	Possible Solution
Codes out of keyboard mostly wrong, seems like one bit of 8-bit data locked to one polarity	Main 26-pin connector not fully seated on mating connector	Disassemble keyboard, check mating of 26-pin connector.
	Bad encoder bit driver	Replace encoder.
No key response on all data keys	Keyboard power interrupted	Disassemble keyboard, check mating of 26-pin connector.
	Keyboard strobe bad, KBSIN–	Check KBSIN– for functionality.
	Encoder scanning oscillator malfunctioning	Check R1 and C1 for presence, values, or solder bridges.
	Bad encoder	Replace encoder.

2.5.3 **KEYBOARD OPERATIONAL CHECKOUT.** After troubleshooting the keyboard and repairing all detected faults, initiate part E4 of the diagnostic and ensure that the keyboard works properly in the hot mock-up system. If the keyboard malfunctions, repeat the procedure in paragraph 2.5.2. If the keyboard performs satisfactorily, reassemble the keyboard assembly as follows:

1. Lay the cover upside down on the work surface.
2. Align the two holes on the keyboard pwb over the mounting studs on the inside of the cover.
3. Ensure that the cable is tightly connected.
4. Place assembly base over keyboard and cover and replace the four screws that hold the case halves together.

With the keyboard assembly reassembled, initiate part E4 of the diagnostic and ensure that the keyboard works properly in the hot mock-up system. If the keyboard malfunctions, repeat the procedures in paragraph 2.5.2 and the first part of this paragraph.

2.6 POWER/LOGIC PWB MAINTENANCE PROCEDURES

Maintenance procedures for the power/logic board consist of a preliminary checkout to determine if any problems exist which might be visually detected, and fault isolation procedures to locate faulty circuit components.

2.6.1 POWER/LOGIC PWB PRELIMINARY CHECKOUT. Upon receipt of a suspect power/logic pwb from the field maintenance facility, visually inspect the board for the problems listed in paragraph 2.4.1. If a thorough visual inspection indicates no problems, proceed with the fault isolation procedure for the pwb.

2.6.2 POWER/LOGIC PWB FAULT ISOLATION PROCEDURES. Table 2-2 lists procedures for troubleshooting the power/logic pwb with a hot mock-up system. Table 2-3 lists procedures to isolate faults indicated by abnormal conditions detected by table 2-2 procedures.

2.7 VDT CONTROLLER MAINTENANCE PROCEDURES

Maintenance procedures for the VDT controller consist of a preliminary checkout to determine if any problems exist which might be visually detected, and fault isolation procedures to locate faulty circuit components.

Table 2-2. Power/Logic PWB Troubleshooting Procedure

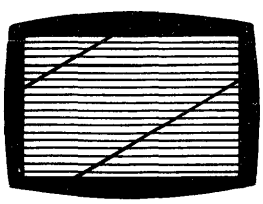
Step	Procedure	Normal Indication	If Abnormal
1	Install power/logic pwb into hot mock-up system.		
2	Apply power to hot mock-up system.	Blank CRT screen.	Perform step 1, table 2-3.
		Sync(s) LED on rear of display unit lighted.	Perform step 2, table 2-3.
3	Turn brightness control clockwise to display raster.	Dark margin surrounding raster (may not be visible on all sides of raster) of horizontal lines which appear fixed in position. Bright, angular vertical retrace. 	Perform step 3, table 2-3.
4	Load and execute diagnostic.	Diagnostic runs with no error indications.	Perform steps 4 through 9, table 2-3.

Table 2-3. Power/Logic PWB Fault Isolation Procedures

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	CRT screen not blank when power first applied	Spurious oscillations in video circuitry (figure 1-22)	Check circuitry from J3-4 back to source of signal.	No video detected	Replace component producing output.
2	Sync LED not lighted with power applied	Horizontal sync generator (figure 1-22)	Check circuit back from high side of CR16.	Logic 0 @ U6-12	Trace circuit back until horizontal sync pulse is found. Remove and replace faulty component(s).
2a		Interface cable connector P2 disconnected	Ensure that cable is properly connected.	Cable properly connected	Secure cable.
3	Unstable or no raster	Horizontal or vertical sync circuits (figure 1-22)	Check circuit back from J3-2 and J3-6.		Trace circuit back from J3-2 and J3-6 to U7-7.
4	No beep during part 1 of diagnostic	Audio logic (figure 1-22)	Loop on part 1 (L1) and scope circuit.	0.25-second tone	Trace back from speaker until audio signal is found. Remove and replace faulty component(s).
5	Failure of any portion of parts 1 through 3 of diagnostic	Video circuitry (figure 1-22)	Execute part 4 and scope circuit.	Proper video and audio responses to diagnostic	Trace circuit and replace faulty component(s).
6	Terminal Ready failure	Driver U11	Execute part 4 and scope circuit.	Proper response to diagnostic	Trace circuit back from J2-6. Remove and replace faulty component(s)

Table 2-3. Power/Logic PWB Fault Isolation Procedures (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
7	Improper picture displayed	Video circuitry (figure 1-22)	Execute part 4 and scope circuit.	Proper display of symbols	Trace circuit back from J3-4 to J2-2. Remove and replace faulty component(s).
8	Keyboard failure	UART failure (figure 1-22)	Exercise and trace circuit for lowercase g and for F7.	Proper codes displayed on LEDs $g = 67_{16}$ $F7 = 98_{16}$	Strike key giving incorrect response. Trace forward from U14 inputs.
9	Repeat test failure	Repeat circuit (figure 1-22)	Exercise and trace circuit.	Characters repeated at 10 ± 2 hertz	Trace circuit forward from J1-10 until repeat indication is lost. Remove and replace faulty component(s).

2.7.1 **VDT CONTROLLER PRELIMINARY CHECKOUT.** Upon receipt of a suspect VDT controller from the field maintenance facility, visually inspect the controller for the problems listed in paragraph 2.4.1. Figure 2-5 shows the maximum configuration for a VDT controller with two controllers. Table 2-4 lists additional items that should also be checked. If a thorough visual inspection indicates no problems, proceed with fault isolation procedures.

2.7.2 **VDT CONTROLLER FAULT ISOLATION PROCEDURES.** Table 2-5 lists procedures for troubleshooting the VDT controller with a hot mock-up system. Tables 2-6 through 2-14 list fault isolation procedures for various types of problems.

2.8 CRT MONITOR MAINTENANCE PROCEDURES

Maintenance procedures for the CRT monitor consist of a preliminary checkout to determine if any problems exist that might be visually detected, and fault isolation procedures to locate faulty circuit components.

2.8.1 **CRT MONITOR PRELIMINARY CHECKOUT.** Upon receipt of a suspect CRT monitor from the field maintenance facility, visually inspect the CRT for signs of damage, and for flaws caused by deterioration. Visually inspect the PWB for problems listed in paragraph 2.4.1. If a thorough visual inspection indicates no problems exist, proceed with the fault isolation procedure for the monitor.

2.8.2 **CRT MONITOR FAULT ISOLATION PROCEDURES.** Table 2-15 lists fault isolation procedures for the CRT monitor in a hot mock-up system. Figures 2-10 through 2-12 are CRT monitor schematic diagrams.

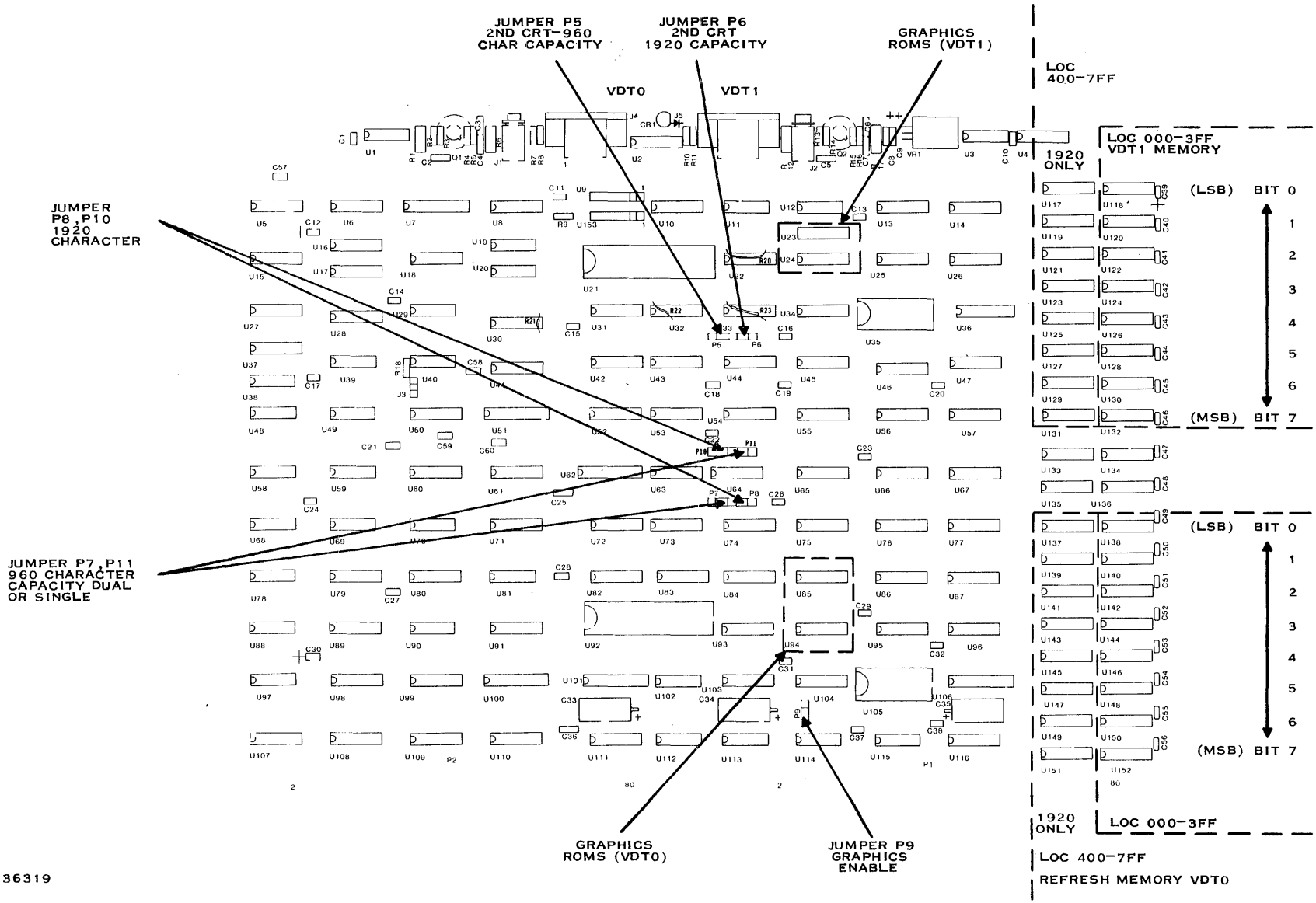


Figure 2-5. VDT Controller Assembly Configuration

Table 2-4. VDT Controller Standard Configurations

CONTROLLER ASSEMBLY A=USA AND EUROPEAN PN 946076 B=JAPAN PN 2263400 DASH NO (S)	TIMER ROMS PN948554			LINE COUNTER DEVICE TYPE @U41	GRAPHIC ROM NETWORK LOCATIONS		GRAPHICS OPTION JUMPER PLUG P9	CURSOR ADDRESS JUMPER PLUGS	REQUIREMENT FOR SINGLE CONTROLLER HARDWARE JUMPERS U22 PIN 10 TO 16 U33 PIN 7 TO 16 U32 PIN 4 TO 16 U30 PIN 9 TO 8	REQUIRED MEMORY NETWORKS	DESCRIPTION D/S DUAL/ SNG F/H 1920/ 960 50/60 HZ G GRAPHICS
	CHARACTER DECODER ROM DASH NO. @U51	ROW DECODER ROM DASH NO. @U52	SYNC DECODER ROM DASH NO. @U42		LINE 8 PN972923-1	LINE 9 PN972923-2					
A-1	-1	-2	-3	SN74162N			NONE	P6,P8,P10	NONE	U117 THRU U132 U137 THRU U152	D,F,60
A-2	-1	-2	-3	SN74162N			NONE	P8,P10	YES	U137 THRU U152	S,F,60
A-3, B-1	-1	-4	-5	SN94163N			NONE	P5,P7,P11	NONE	EVEN NUMBERED NETWORKS U118 THRU U132;U138 THRU U152	D,H,60
A-4, B-2	-1	-4	-5	SN74163N			NONE	P7,P11	YES	EVEN NUMBERED NETWORKS U138 THRU 152	S,H,60
A-5, B-3	-1	-2	-3	SN74162N	U94,U24	U85,U23	YES	P6,P8,P10	NONE	U117 THRU U132 U137 THRU U152	D,F,60,G
A-6, B-4	-1	-2	-3	SN74162N	U94	U85	YES	P8,P10	YES	U137 THRU U152	S,F,60,G
A-7	-1	-6	-7	SN74162N			NONE	P6,P8,P10	NONE	U117 THRU U132 U137 THRU U152	D,F,50
A-8	-1	-6	-7	SN74162N			NONE	P8,P10	YES	U137 THRU U152	S,F,50
A-X09* B-5	-1	-8	-9	SN74163N			NONE	P5,P7,P11	NONE	EVEN NUMBERED NETWORKS U118 THRU U132,U138 THRU U152	D,H,50
A-X10* B-6	-1	-8	-9	SN74163N			NONE	P7,P11	YES	EVEN NUMBERED NETWORKS U138 THRU U152	S,H,50
A-X11* B-7	-1	-6	-7	SN74162N	U94,U24	U85,U23	YES	P6,P8,P10	NONE	U117 THRU U132 U138 THRU U152	D,F,50,G
A-X12* B-8	-1	-6	-7	SN74162N	U94	U85	YES	P8,P10	YES	U137 THRU U152	S,F,50,G

*IN PART NUMBER A-X09, -X10, -X11 AND -X12, THE X INDICATES THE EUROPEAN COUNTRY AND SPECIFIES THE CHARACTER SET.

X	COUNTRY
00	FRANCE
01	GREAT BRITAIN
02	GERMANY
03	NORWAY/DENMARK
04	SWEDEN/FINLAND

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Table 2-5. VDT Controller Troubleshooting Procedure

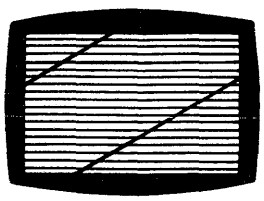
Step	Procedure	Normal Indication	If Abnormal
1	Install VDT controller into hot mock-up system.		
2	Apply power to hot mock-up system.	Blank CRT screen	Perform step 1, table 2-6.
		Test LED off	Perform step 2, table 2-6.
		Sync(s) LED on rear of display unit lighted.	Perform step 3, table 2-6.
		Dark margin around raster of horizontal lines which appear fixed in position. Bright, angular retrace. Dark margin may not appear surround raster.	Perform step 4, table 2-6.
			
		Clock oscillator frequency = 11.004 MHz.	Perform step 5, table 2-6.
3	Load and execute diagnostic.	No error messages	Proceed to tables 2-7 through 2-14.

Table 2-6. VDT Controller Preliminary Fault Isolation Procedures

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	CRT screen not blank	Video output logic (figure 1-44)	Scope circuit.		Trace back from J4-2 (J5-2 for 2nd controller) until fault is found. Replace faulty component(s).
2	Test LED on	Built-in test and master clear logic (figure 1-35)	Scope circuit.	Logic 1 at U83-12	Trace back from U83-12 until fault located. Replace faulty component(s).
3	Sync LED not lighted	Video output logic (figure 1-44)	Scope circuit.		Trace back from J4-2 (J5-2 for 2nd controller) until fault is found. Replace faulty component(s).
4	Unstable or missing raster	Timing logic (figure 1-49, 1-50)	Scope circuit.		Trace back from J4-2 (J5-2 for 2nd controller) until fault is found. Replace faulty component(s).
5	Basic clock signal (CLK) faulty	Oscillator	Scope circuit.	CLK = 90.9 nsec	Trace back from U40-8. Replace faulty component(s).

Table 2-7. Fault Isolation Procedures When Unable to Load Diagnostic

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Diagnostic does not execute	Constant keyboard interrupt	Scope circuit.	Logic 1 at P2-66 (P1-66 for 2nd controller).	Trace back until fault is located. Replace faulty component(s).
2	Diagnostic does not load, test LED lighted	Master clear not functioning or always active	Scope circuit.	Logic 1 at P2-66 (P1-66 for 2nd controller).	Trace back until fault is located. Replace faulty component(s).
3	Diagnostic does not load	CRU interface signal shorted to another signal or to ground	Master clear system (cycle chassis power off and back on)	CRUBIT12 = 0 CRUBIT13 = 0 CRUBIT14 = 0 CRUBIT 15 = 0 CRUBITOUT = 0 STORECLOCK- = 1 MODSELA– = 1 MODSELB– = 1 CRUBITINT = 1 NKBINT = 1	Remove CPU or CPU buffer. Ground each input. Check effect of grounded input on other input. Check continuity to locate short circuit path. Repair.
4	Diagnostic does not load, CRU lines not shorted to each other	CRU interface signal(s) shorted to ground	Same as for step 3	Same as for step 3.	Remove VDT controller. Check CRUBIT, 12-15, and CRUBITOUT for ground.

Table 2-8. Fault Isolation Procedures for Apparent CRU Interface Problems

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Raster stable, screen blank, timing errors, previous word select error, keyboard self-test failure, test LED not lighted	CRU base for diagnostic not properly initialized, CRU bit decoder, multiplexer	Reinitialize.	CRU base correct	Execute IT verb, enter correct CRU base and interrupt level.
		Input buffers or byte selector (figure 1-36)	Exercise interface with CD-C verb.	See figure 2-6.	See figure 2-6.

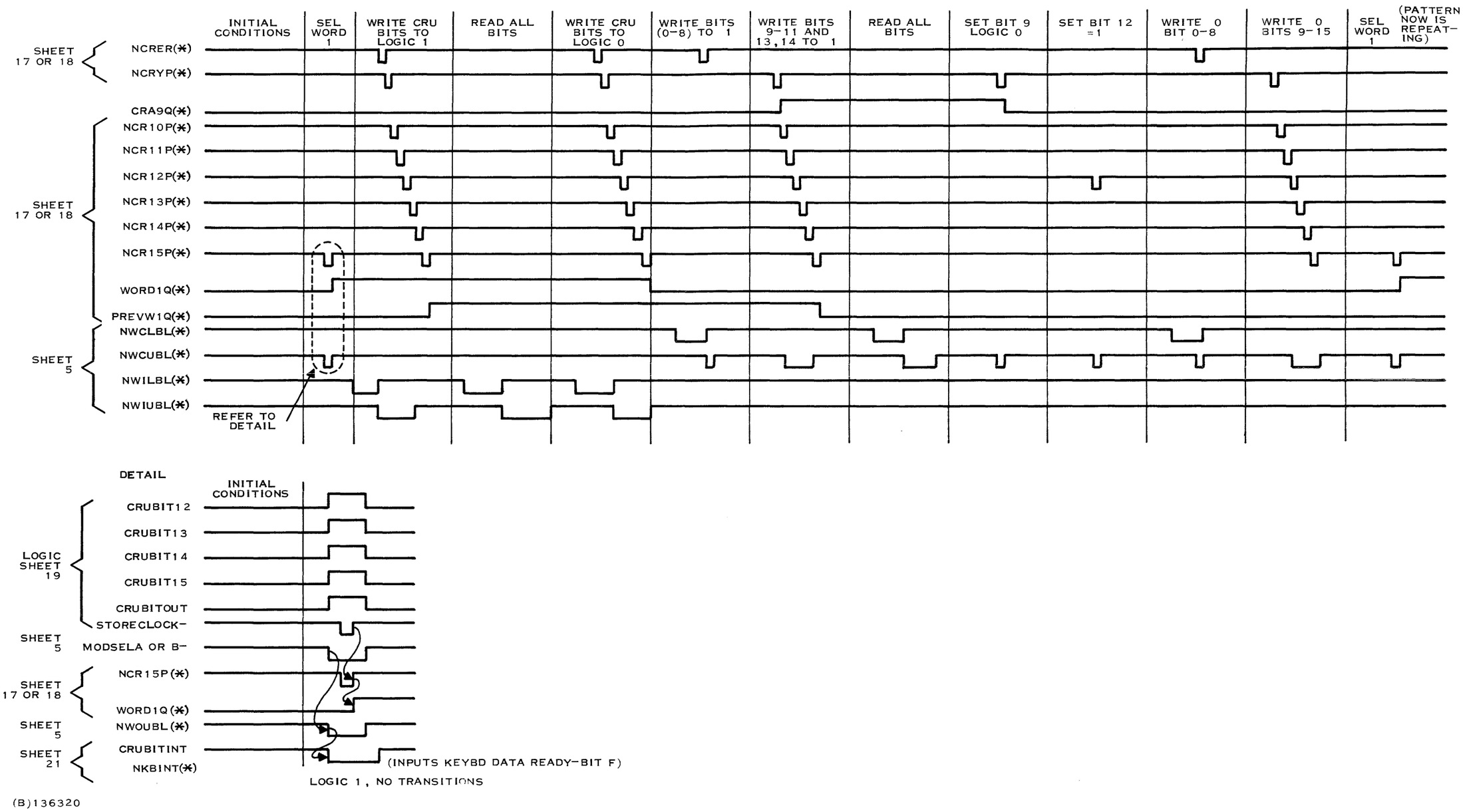
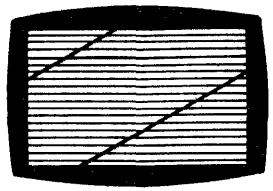
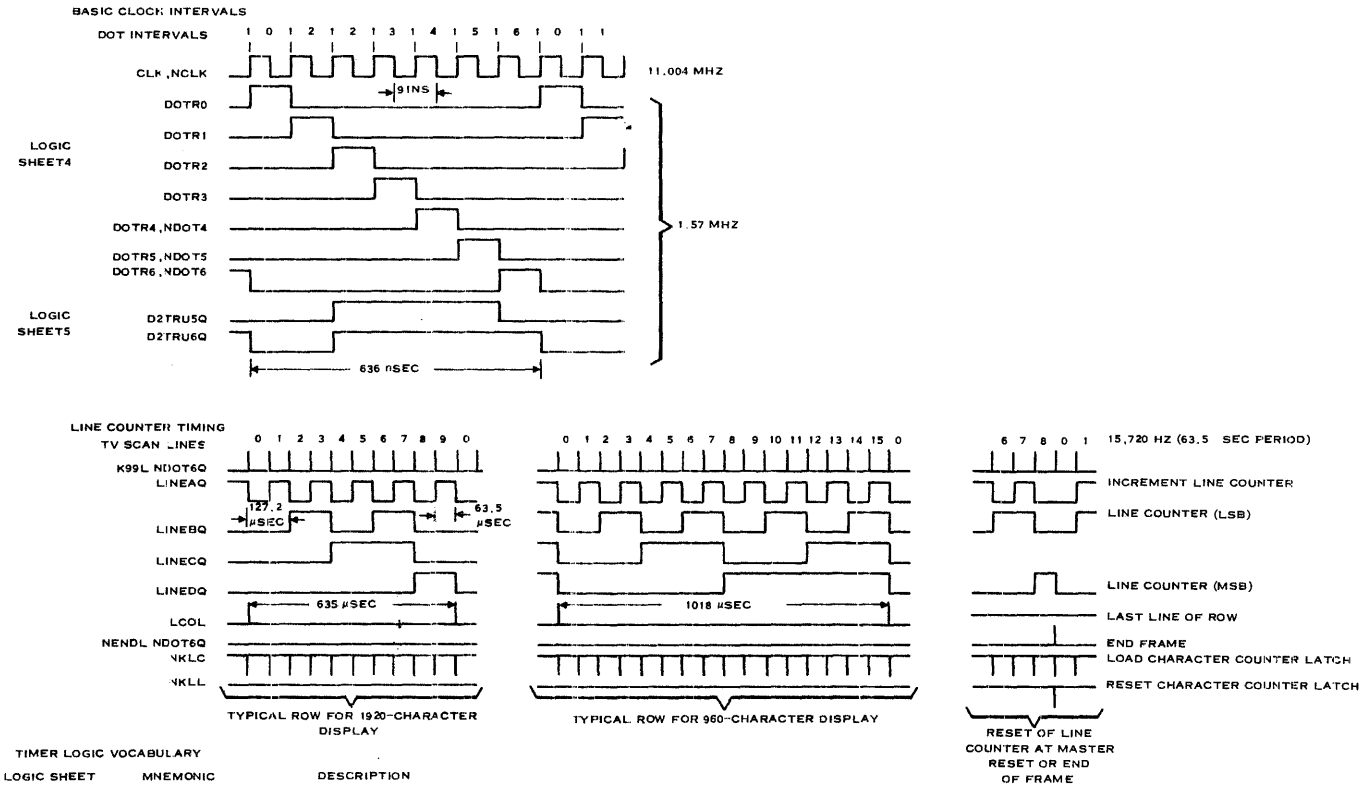


Figure 2-6. CRU Interface Waveforms During Exercise by the CD-C Verb

Table 2-9. Fault Isolation Procedures for Apparent Timer Problems

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Screen blank, raster unstable, previous word select error, keyboard self-test failure, sync(s) LED not lighted	Defective clock	Scope circuit.	Clock period = 90.2 nanoseconds at U40-8.	Trace circuit back from U40-8. Replace faulty component(s).
		Constant system reset	Scope circuit.	NRL2=1 at U98-13	Trace circuit back from U98-13 until source of error is found. Replace faulty component(s).
2	Sync (S) LED not lighted	Additional symptoms needed	Execute part 1 (E1).		
3	H-Sync error only for part 1. Video bar on screen, but raster unstable	Horizontal blanking flip-flop or steering circuit	Scope circuit.	HSBQ = 63.5 μ sec period.	Trace circuit back from U50-4 until fault is found. Replace faulty component(s).
		Horizontal sync flip-flop or steering logic	Scope circuit.	HSQ = 63.5 μ sec period	Trace circuit back from U50-5 until fault is found Replace faulty component(s).
4	Sync error may cause keyboard self-test to fail; will probably cause manual keyboard to input to fail	Composite sync flip-flop or steering logic	Scope circuit.	See figure 2-7.	Sync on VSBQ at U50-13. Trace circuit back from U50-12. Replace faulty component(s).



TIMER LOGIC VOCABULARY

LOGIC SHEET	MNEMONIC	DESCRIPTION
7	CSQ	COMPOSITE SYNC FF
5	C2HZQ	TWO HERTZ CLOCK
5,4	ENDL,NENDL	ENABLE RESET OF CHARACTER COUNTER AND LINE COUNTER TO ZERO (ROM DECODES A SPECIFIC ROW, LINE AND CHARACTER 99 TO DETERMINE END OF FRAME)
7	HBSL	ENABLE HORIZONTAL BLANKING (OCCURS EVERY LINE)
7	HDENDL,NHDENDL	ENABLE RESET OF COMPOSITE SYNC FF (EACH LINE) EXCEPT DURING VERTICAL SYNC
7	HDEQSL	ENABLE RESET OF COMPOSITE SYNC FF (EACH FRAME) DURING VERTICAL SYNC
7	HDSL	ENABLE HORIZONTAL DRIVE/SYNC
7	HSBQ	HORIZONTAL BLANKING INTERVAL (EVERY LINE)
7	HSQ	HORIZONTAL SYNC INTERVAL (EVERY LINE)
6	KAD0-11	CHARACTER ADDRESS COUNTER (DETERMINES A CHARACTER ADDRESS FOR EVERY INTERVAL WITHIN A FRAME) BIT 11 IS MOST SIGNIFICANT BIT.
6	KCH0-2	CHARACTER COUNTER (THESE BITS AND KAD0-3 ARE USED TO COUNT THE CHARACTER TIMES FROM 0 TO 99 ON ANY LINE)
7	K99L,NK99L	DECODE OF CHARACTER TIME 99 (THE END OF A SCAN LINE). END BLANKING, ENABLE LOAD OF CHARACTER ADDRESS LATCH, RESETS
4	LCOL	LAST LINE OF A TYPICAL ROW. OCCURS DURING LINE 9 ON 1920 CHARACTER DISPLAY AND LINE 15 ON 960 CHARACTER DISPLAY. (CHARACTER 99 TIMES)
4	LINE (A,B,C,D)Q	LINE COUNTER OUTPUTS - RESET TO ZERO AT END OF LINE (LCOL) OR AT END OF FRAME (ENDL).
8	NKLC	LOADS CHARACTER ADDRESS LATCH (KLQ0-KLQ7)
7	NKLL	CLEARS CHARACTER ADDRESS LATCH (KLQ0-KLQ7)
6	NRSCSL	RESETS THE COMPOSITE SYNC FF UNDER THE CONTROL OF HDENDL OR HDEQSL
5	VBL	ENABLE VERTICAL BLANKING
7	VSBQ	VERTICAL BLANKING INTERVAL (EVERY FRAME)
5	VSQ	VERTICAL SYNC INTERVAL (EVERY FRAME)
7	KLQ(0-7)	CHARACTER ADDRESS LATCH - CONTAINS THE ADDRESS OF THE FIRST CHARACTER OF THE NEXT SCAN LINE. THE ADDRESS CHANGES DURING THE LAST LINE OF EVERY ROW (AT HSQ TIME).

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Figure 2-7. Timer Signal Relationships

Table 2-10. Fault Isolation Procedures for Apparent Memory Failure

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Fails part 1 measurement of video Full, Blank, or H-Sync pattern		Perform parts 2 and 3 to obtain more information.		
2	Fails part 2; passes part 3. Program unable to write a particular pattern at location(s) within a bank of networks	Defective memory network(s). Read data multiplexer. Read data latches memory control logic	Use CU verb to move cursor to failing location(s). Use CD-S to verify failure mode. Use CD-SL to establish scoping loop.	See example.	Proceed as in example.

Example:

1. Part 1 (E1) failed. Video values not 0 (suggests memory picking up bits).

2. Part 2 (E2) failed.

EXPECTED DATA	ACTUAL DATA	ACTUAL ADDRESS	EXPECTED ADDRESS
30	32	17F	17F
75	77	27F	27F

   (suggests picking up bit at lower memory addresses)

3. Part 3 (E3) passed. Memory errors probably not caused by cursor address malfunctions.

4. Select verb CU-A. Set address to $17F_{16}$.

5. Select verb CD-S. Set data to 30_{16} (ASCII 0).

6. Use CD-SL verb to establish scoping loop as symptoms indicate and data set to 30_{16} (ASCII 0).

7. If data read (30_{16}) and display is character 0 at cursor location, memory/CPU input register (figure 1-24) is probable cause. Sync on CURDQ (U100-19) (U6-15 for 2nd controller). Check M1D1Q at U87-14 (U14-14 for 2nd controller).

8. If data read (30_{16}) and display is 2 at cursor location, check memory output MDO1Q at U106-5 (U36-5 for 2nd controller). Data read by program is data written to memory. Data on screen at current cursor location is data read from suspect location. MID, 0-7, Q contains write data until cursor is moved, at which time it contains read data.

Table 2-11. Fault Isolation Procedure for Apparent Alarm Problems

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Alarm duration out of tolerance	Defective alarm logic (figure 1-48)	Execute part 4 (E-4) alarm test.	See figure 2-8. .28 - .32 sec at 50 Hz .23 - .27 sec at 60 Hz.	Trace circuit back from U79-6 (U37-6 for 2nd controller). Replace faulty component(s).
		Built-in test logic (figure 1-33)	Loop on part 1 (L1).	BBTSL follows AQ.	Sync on AQ at U79-6 (U37-6 for 2nd controller). Trace forward from U80-9 (U18-9 for 2nd controller). Replace faulty component(s).

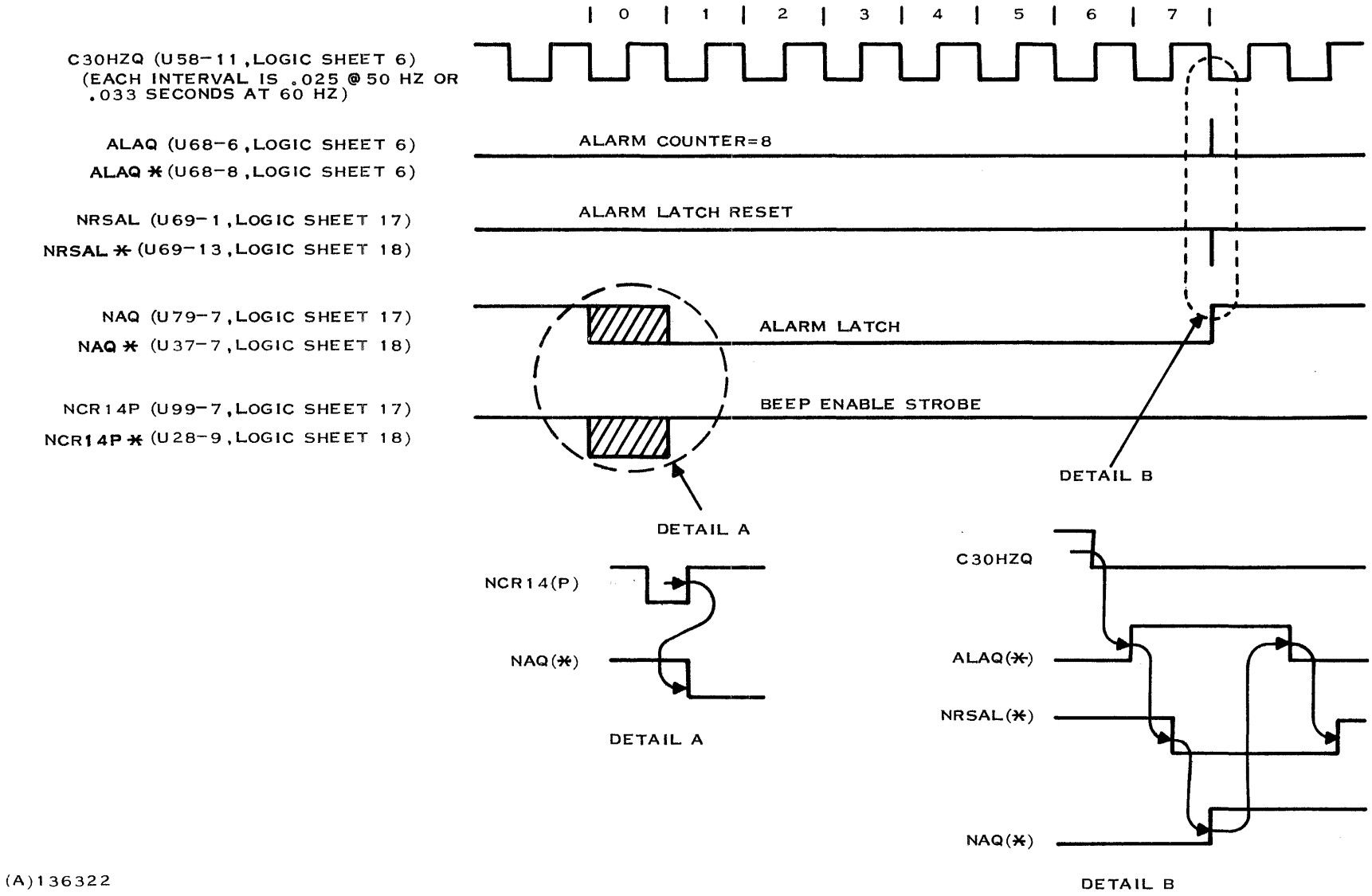


Figure 2-8. Alarm Signal Timing Diagram

Table 2-12. Fault Isolation Procedures for Apparent Keyboard-Related Problems

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Keyboard self-test failure of part 1 (E1)	H-Sync error	See step 3, table 2-9.		
2	Correct H-Sync keyboard or parity error	UART, keyboard logic (figure 1-35), Built-in test logic (figure 1-34)	Loop on part 1 (L1).	See figure 2-9.	Sync on negative edge of NKBTBRL at U102-8 (U19-8 for 2nd controller). Check KBTL at U92-25 (U21-25 for 2nd controller). Check forward.
3	Part 1 (E1) passes; keyboard test in part 4 (E4) does not detect keyboard code	Keyboard data receiver, or built-in test logic (figure 1-34)	Scope circuit while reportedly striking a keyboard data key.	See figure 2-9.	Check initial receiver conditions against figure 2-10. Sync on TET1T (U8-11 (U10-11 for 2nd controller)). Trace forward to UART. Replace faulty component(s).
4	Part 1 (E1) passes. Part 4 (E4) fails interrupt test. Data entered correctly	CRU interface logic	Halt CPU at interrupt test of Part 4 (E4) after printout but before timeout. Strike a data key to cause interrupt.	NKBINT = 0	Trace back from P2-66 (P1-66 for 2nd controller) until fault is located. Replace faulty component(s).
5	Constant keyboard interrupt	Interrupt enable latch (CRACQ)	Used CD-C verb to exercise latch.	See figure 2-6.	Trace back from P2-66 (P1-66 for 2nd controller) until fault is found. Replace faulty component(s). Removal of 990 slot interrupt jumper may be helpful.

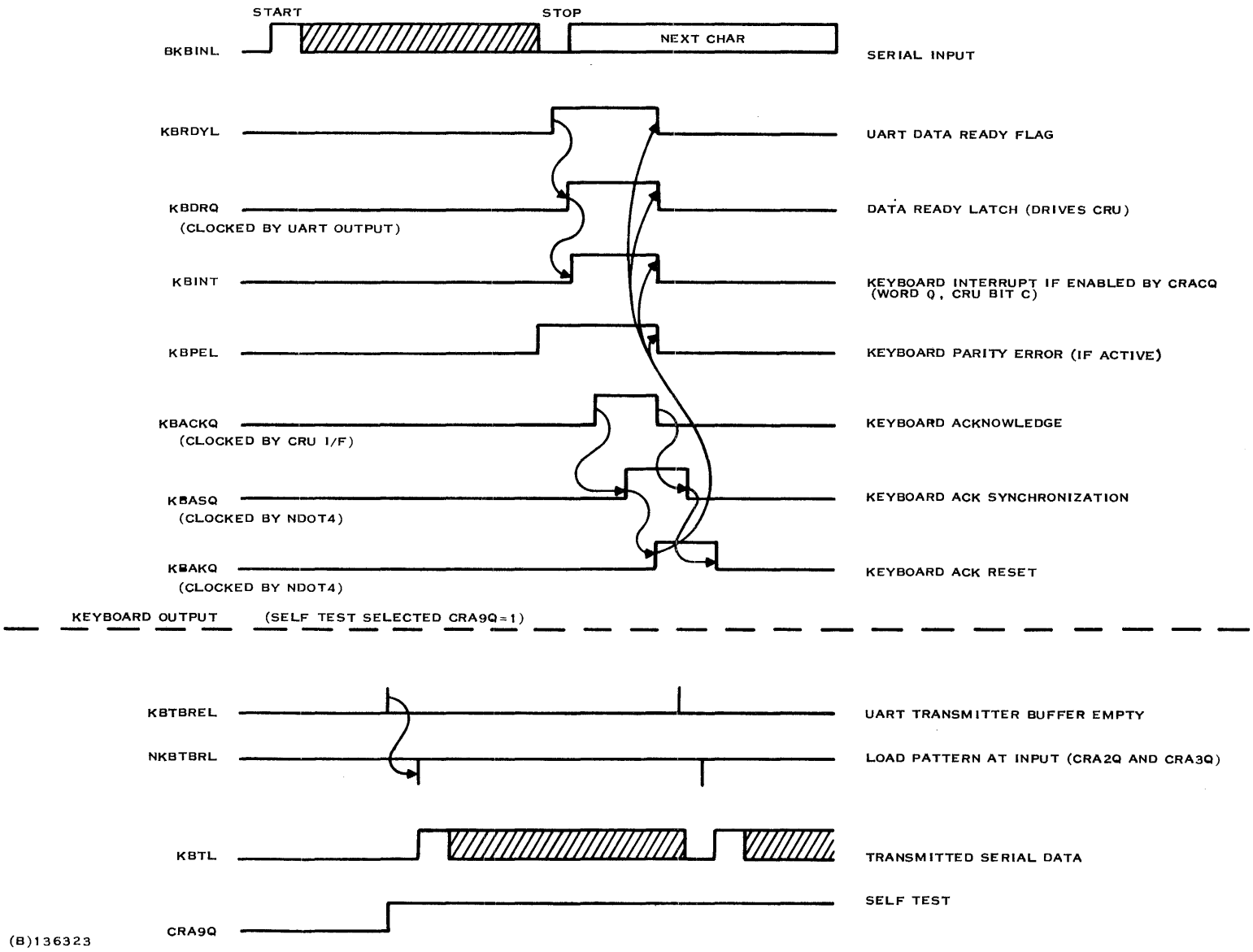


Figure 2-9. Model 911 VDT Controller Keyboard Logic Timing Diagram

Table 2-13. Fault Isolation of Apparent Cursor Address Problems

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Cursor Error 1	CRU interface logic, cursor address buffer, cursor address register	Use CU-SL verb to continuously increment and decrement.		Sync on NW0CR10L (U93-10 (U22-6 for 2nd controller)). Examine CA, 0-10.
2	Cursor Error 2	Cursor command decode logic	Use CU-I verb to position cursor and continuously load selected address.		Sync or NW1CR10L (U93-11 (U22-5 for 2nd controller)). Examine CRB, 0-A,Q.
3	Cursor Error 3	CRU interface logic, cursor address buffer, cursor address register, cursor command decode logic	Use CU-A verb to position cursor and CD-SL verb to continuously increment and decrement cursor address.		Sync on NW0CR10L (U93-10 (U22-6 for 2nd controller)). Examine CA, 0-10.

Table 2-14. Fault Isolation of Problems Indicated by Self-Test LED

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Self-test LED does not light.	Lamp or driver	Loop on part 1 (E1).	LED blinks.	Trace back from U83-12 until signal is found. Replace faulty component(s).
		Self-test mode not selected	See table 2-8.	See table 2-8.	See table 2-8.
2	Self-test LED always lighted	Self-test mode selected by other controller	Scope circuit.		If either controller is in self-test mode, LED will be lighted.

Table 2-15. Fault Isolation Procedures for CRT Monitor

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Any fault with symbol form	CRT, sweepboard, yoke, or flyback			
	• Video dim	Sweepboard	Check socket at base of tube for tightness and intermittent connection. Isolate fault to sweepboard by replacement.	Normal bright video in contrast to raster	Replace defective element (socket assembly or sweep-board component).
		CRT (tube)	Check for internal arcing, or broken or missing pins on base.		Replace defective tube.
	• Poor geometry (raster shape)	Linearity sleeve placement	Adjust horizontal linearity sleeve for optimum hori-zontal character linearity (if applicable).	No distortion	Check yoke or sweep-board.
		Linearity sleeve ground strap placement	Move ground (copper foil) to another area on Aquadag.	No distortion	Readjust linearity sleeve.
		Yoke	Look for missing pincushion magnets and attempt to correct with additional magnets.	No distortion	Replace yoke or glue in appropriate magnet(s).
		Flyback	Isolate to flyback by replacement.	No distortion	Replace flyback.
		CRT	Isolate to CRT tube.	No distortion	Replace tube.
	• Symbols not same size across screen	Yoke assembly	Adjust linearity sleeve under yoke (if applicable).	Symbol size - 66 dots per inch, ± 7 dots	Replace yoke or CRT tube.

Table 2-15. Fault Isolation Procedures for CRT Monitor (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
		Sweepboard	Adjust horizontal linearity control (if applicable).	Symbol size - 66 dots per inch, ± 7 dots	Check horizontal circuit.
	• Symbols not same size at top and bottom	Sweepboard	Adjust vertical linearity control.	Same number of dots per inch at top and bottom, ± 4 dots	Check vertical circuit.
	• Focus unsatisfactory	Sweepboard or CRT	Adjust focus control.	All dots resolved with low intensity character at 3 foot-lamberts (full screen)	Replace defective element.
2	Unstable raster	Bad mechanical connection at sweepboard, yoke, flyback, or vertical choke	Visual check of connectors: Ten pin I/F Flyback Press fit (yoke and ground wires)	Stable scan lines on screen with dark border on all sides	Repair, clean, or replace termination.
		Sweepboard	Use scope to check vertical and horizontal waveforms.	Same as above	Isolate and repair defective circuit.
3	Tilted display and raster	Yoke	Check position and tightness of yoke.	Level raster	Rotate yoke and tighten as required.
4	Display not centered	Sweepboard	Use horizontal centering control to center data horizontally (if applicable).	Display is centered horizontally and vertically ± 6 mm (0.25 in.).	Check horizontal circuit.
		Yoke	Use centering rings to position display vertically and horizontally.	Same as above	Replace yoke if display cannot be centered without distortion.

Table 2-15. Fault Isolation Procedures for CRT Monitor (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
5	Display compressed to strip about 0.38 mm (0.5 in.) in height	Sweepboard/ vertical choke	Check continuity through vertical choke circuit.	Normal display height	Replace vertical choke or check vertical circuit.
6	Display is horizontal or vertical line	Yoke, sweepboard, or flyback inter-connection	Visually inspect, then check waveforms per schematic.	Raster is visible.	Repair open circuit.
7	No raster (blank screen)		Listen for flyback output.	Barely audible hum	Check horizontal and vertical transistor.
		Sweepboard	Check horizontal output transistor.	15 V ± 0.3 V horizontal transistor collector	If approximately 0.5 V, disconnect flyback connector and measure vertical output transistor collector. If the vertical collector measures approximately 13.5 V, replace horizontal output transistor.
		Sweepboard	Check horizontal output transistor.	15 V ± 0.3 V	If zero, check flyback resistance and 15 V Picofuse (if applicable).
		Flyback transformer	Check flyback resistance.	Resistance from any low voltage winding to another is approximately 0.5 ohm. From the high voltage winding to any low voltage winding, the resistance is approximately 6 ohm.	Replace defective flyback.

Table 2-15. Fault Isolation Procedures for CRT Monitor (Continued)

Step	Symptom	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
		Sweepboard	Check vertical output transistor.	13.5 V vertical transistor collector	If zero with flyback disconnected, check for 15 V Picofuse blown or short on sweepboard.
		Sweepboard	Rotate master brightness control.	Control should allow the raster brightness to be varied.	Replace defective circuit element.

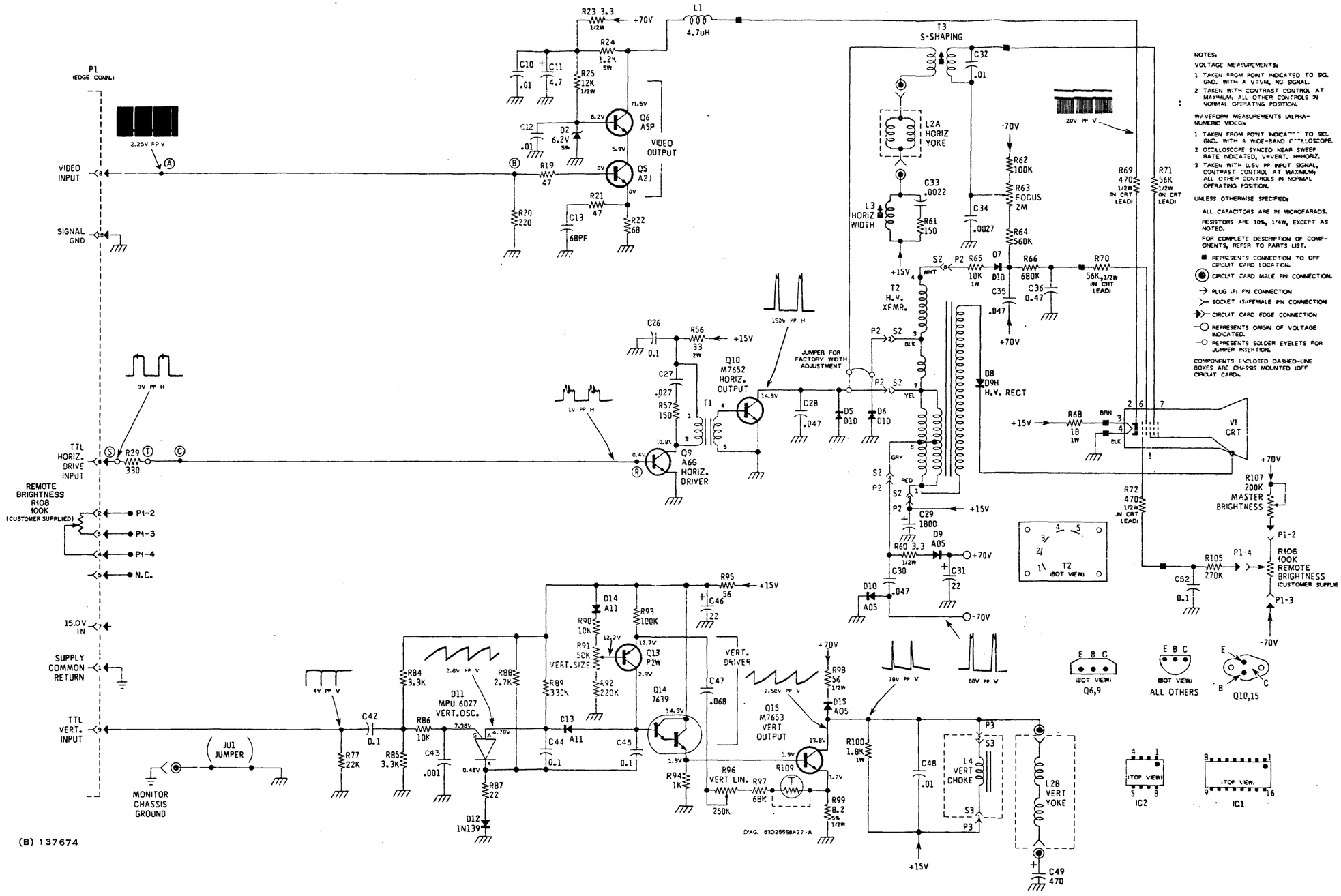
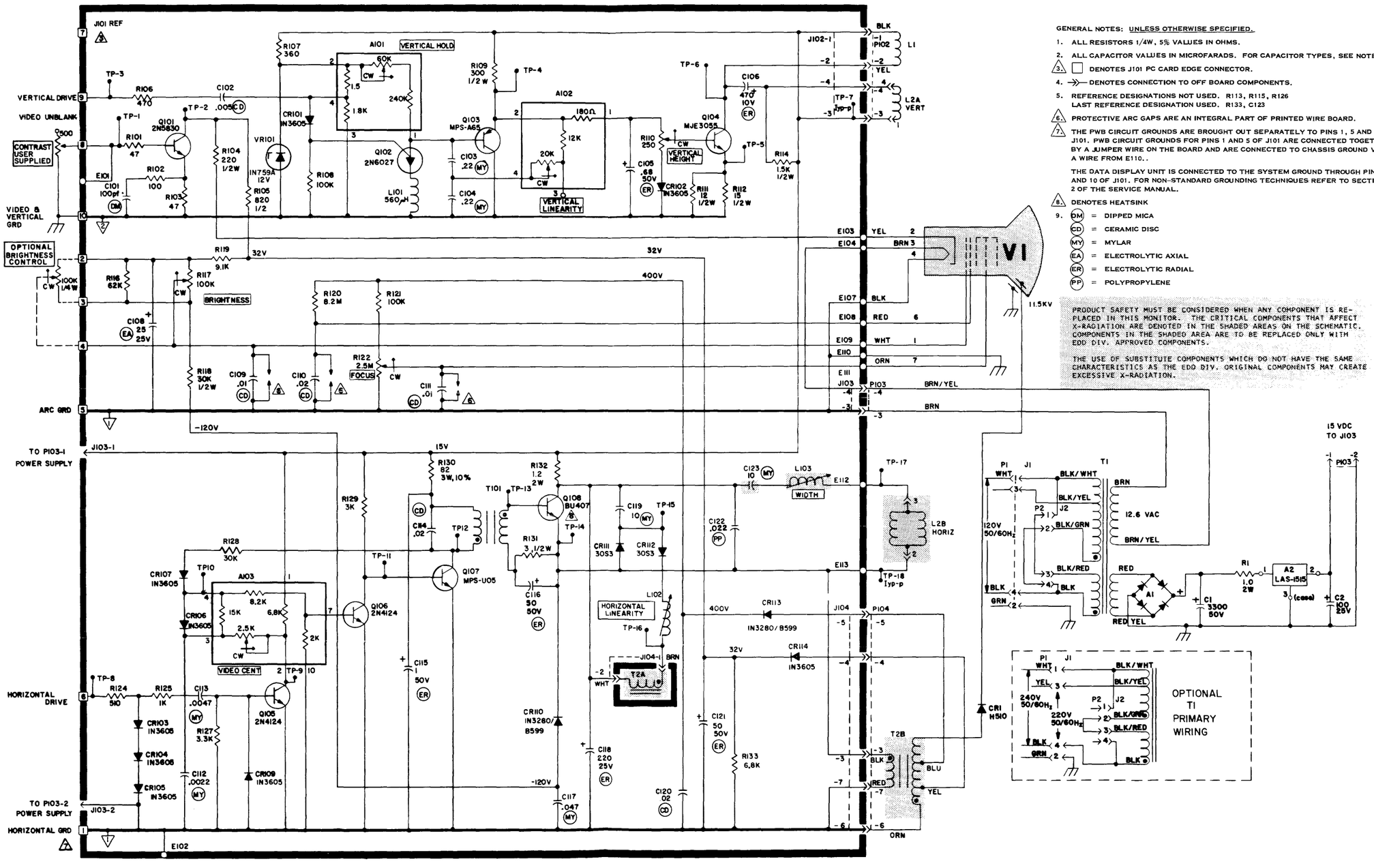


Figure 2-10. CRT Monitor Schematic Diagram, Source 1 (M3960-392/-393)



GENERAL NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS 1/4W, 5% VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS. FOR CAPACITOR TYPES, SEE NOTE #9.
3. □ DENOTES J101 PC CARD EDGE CONNECTOR.
4. →⊢ DENOTES CONNECTION TO OFF BOARD COMPONENTS.
5. REFERENCE DESIGNATIONS NOT USED. R113, R115, R126 LAST REFERENCE DESIGNATION USED. R133, C123
6. PROTECTIVE ARC GAPS ARE AN INTEGRAL PART OF PRINTED WIRE BOARD.
7. THE PWB CIRCUIT GROUNDS ARE BROUGHT OUT SEPARATELY TO PINS 1, 5 AND 10 OF J101. PWB CIRCUIT GROUNDS FOR PINS 1 AND 5 OF J101 ARE CONNECTED TOGETHER BY A JUMPER WIRE ON THE BOARD AND ARE CONNECTED TO CHASSIS GROUND VIA A WIRE FROM E110..

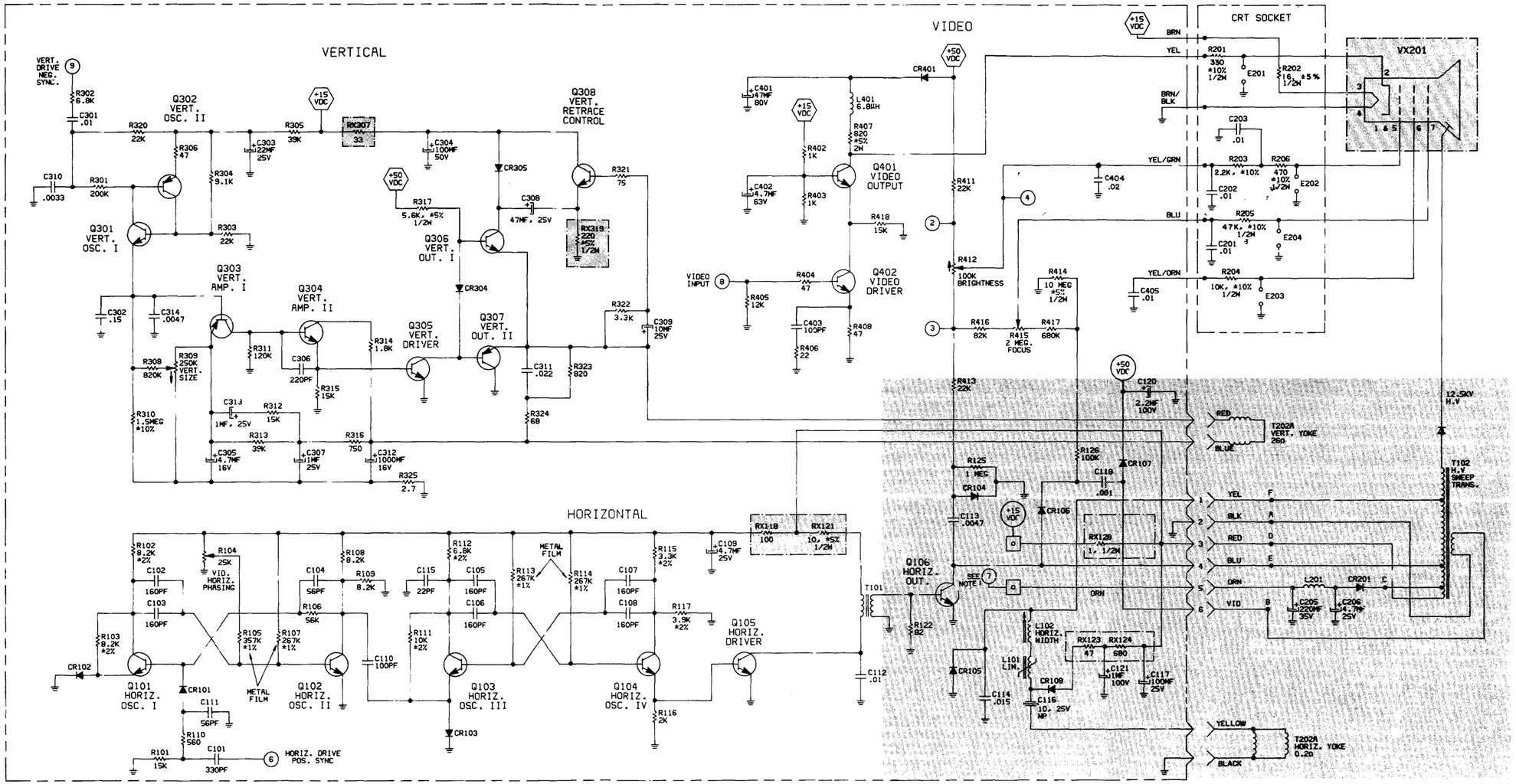
   THE DATA DISPLAY UNIT IS CONNECTED TO THE SYSTEM GROUND THROUGH PINS 1 AND 10 OF J101. FOR NON-STANDARD GROUNDING TECHNIQUES REFER TO SECTION 2 OF THE SERVICE MANUAL.
8. DENOTES HEATSINK
9. (DM) = DIPPED MICA
   (CD) = CERAMIC DISC
   (MY) = MYLAR
   (EA) = ELECTROLYTIC AXIAL
   (ER) = ELECTROLYTIC RADIAL
   (PP) = POLYPROPYLENE

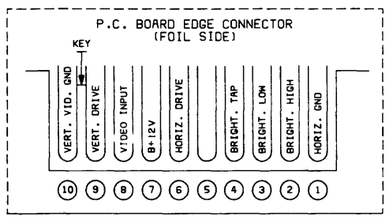
PRODUCT SAFETY MUST BE CONSIDERED WHEN ANY COMPONENT IS REPLACED IN THIS MONITOR. THE CRITICAL COMPONENTS THAT AFFECT X-RADIATION ARE DENOTED IN THE SHADED AREAS ON THE SCHEMATIC. COMPONENTS IN THE SHADED AREA ARE TO BE REPLACED ONLY WITH EDD DIV. APPROVED COMPONENTS.

THE USE OF SUBSTITUTE COMPONENTS WHICH DO NOT HAVE THE SAME CHARACTERISTICS AS THE EDD DIV. ORIGINAL COMPONENTS MAY CREATE EXCESSIVE X-RADIATION.

Figure 2-11. CRT Monitor Schematic Diagram, Source 2 (TV120/-0200133)

D12 VIDEO DISPLAY 15.7KHz





= DC VOLTAGE SOURCE

= DC VOLTAGE APPLIED

NOTE: 1. CUSTOMER SUPPLIED EXTERNAL DC SOURCE ON PIN 7 EDGE CONNECTOR

IMPORTANT SAFETY NOTICE

When servicing this chassis, under no circumstances should the original design be modified or altered without permission from the Zenith Radio Corporation. All components should be replaced only with types identical to those in the original circuit. Special components are used to prevent shock and fire hazard. These critical components are shaded on the schematic and parts list for easy identification.

This circuit diagram may occasionally differ from the actual circuit used. This way, implementation of the latest safety and performance improvement changes into the set is not delayed until the new service literature is printed.

IMPORTANT SAFETY NOTICE

FOR X-RADIATION, FIRE OR SHOCK HAZARD PREVENTION, CERTAIN SPECIAL OR REDUNDANT PARTS ARE USED. USE ONLY EXACT REPLACEMENTS. DO NOT ALTER THE CIRCUIT OR DEFEAT THE FUSES. FAILURE TO COMPLY MAY BE UNLAWFUL.

Figure 2-12. CRT Monitor Schematic Diagram, Source 3 (D12 Series)

APPENDIX A

UNITED KINGDOM MODEL 911 VDT KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, ASCII, SPECIAL CHARACTER SET, AND MATRIX CHART

APPENDIX A

UNITED KINGDOM MODEL 911 VDT KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, ASCII, SPECIAL CHARACTER SET, AND MATRIX CHART

The standard limited-ASCII United Kingdom Model 911 VDT keyboard layout and symbolization are shown in figure A-1. Figure A-2 shows the same keyboard layout with the keys numbered. Table A-1 lists the special character set hexadecimal code outputs by key number, key legend, and mode of the United Kingdom Model 911 VDT keyboard. Figures A-3 through A-6 show keyboard mode character positions. Table A-2 lists the United Kingdom ASCII and special character set. The keyboard matrix chart is shown in figure A-7.

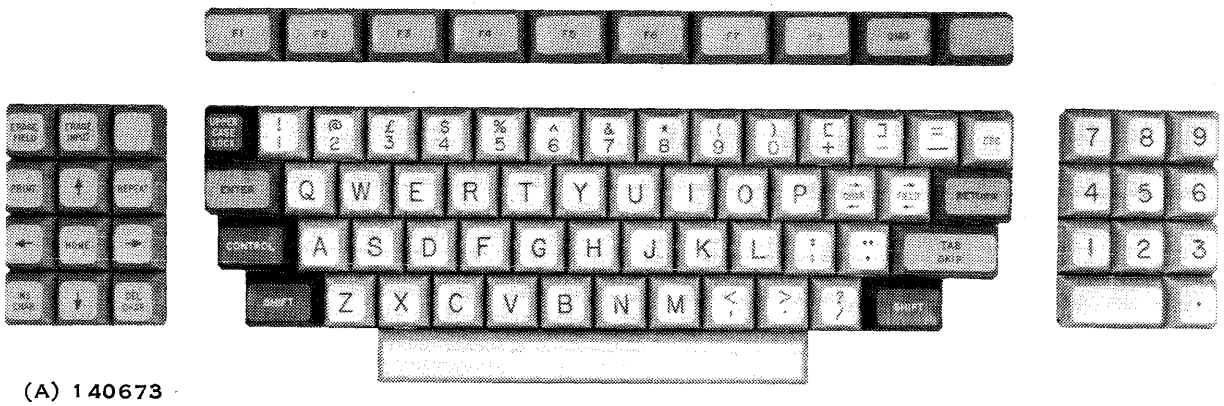


Figure A-1. United Kingdom Model 911 VDT Keyboard Arrangement

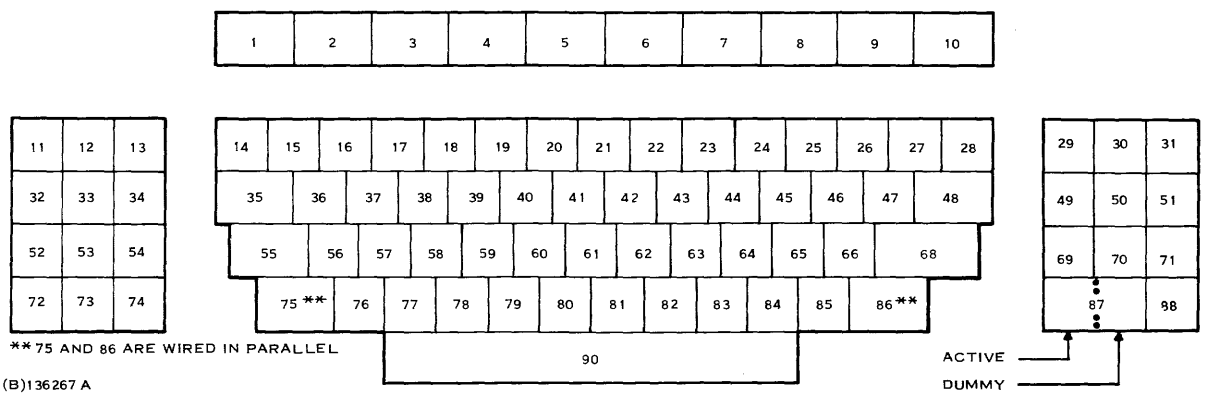


Figure A-2. United Kingdom Model 911 VDT Keyboard with Keys Numbered

Table A-1. United Kingdom Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs

KEY NUMBER	KEY LEGEND	MODE *			
		LC	UC	S	C
17	£ 3	33	33	23	00
22	* 8	38	38	2A	7C
24	) 0	30	30	29	7E
25	[+	2B	2B	5B	1D
26	] –	2D	2D	5D	7F
27	= ___	5F	5F	3D	5C
36	Q	71	51	51	11
37	W	77	57	57	17
41	Y	79	59	59	19
46	→ CHAR ←	88	88	8A	88
47	→ FIELD ←	87	87	8C	87
48	RETURN	0D	0D	0D	0D
56	A	61	41	41	01
65	: ;	3B	3B	3A	7B
66	| \	27	27	22	7D
67	COVERED BY TAB/SKIP KEY				
76	Z	7A	5A	5A	1A
82	M	6D	4D	4D	0D
88	.	2E	2E	2E	2E

* LC = LOWER CASE
UC = UPPER CASE
S = SHIFT
C = CONTROL

(A) 140674

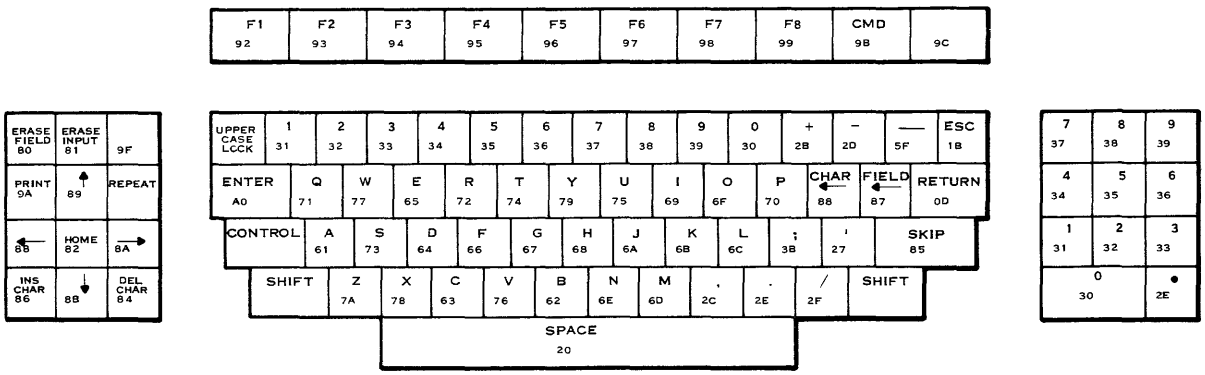


Figure A-3. United Kingdom Keyboard Showing Lowercase Mode Character Positions and Hexadecimal Codes

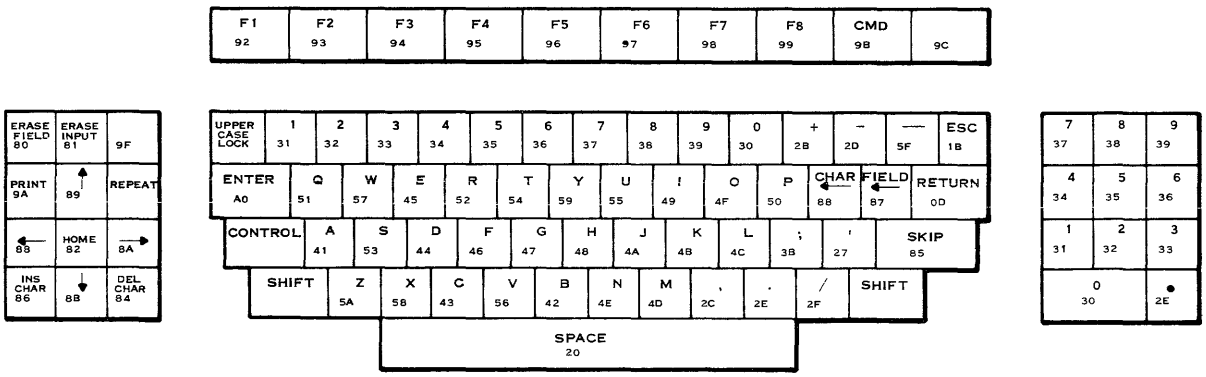


Figure A-4. United Kingdom Keyboard Showing Uppercase Mode Character Positions and Hexadecimal Codes

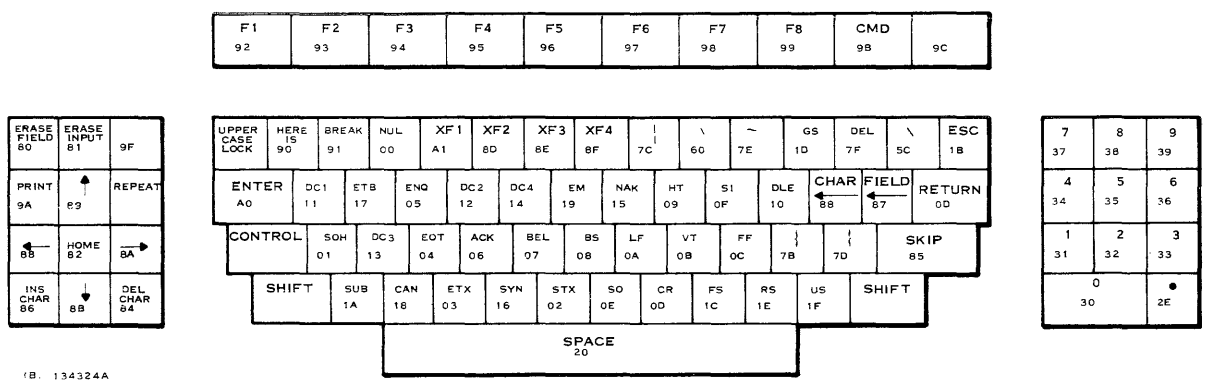


Figure A-5. United Kingdom Keyboard Showing Control Character Positions and Hexadecimal Codes

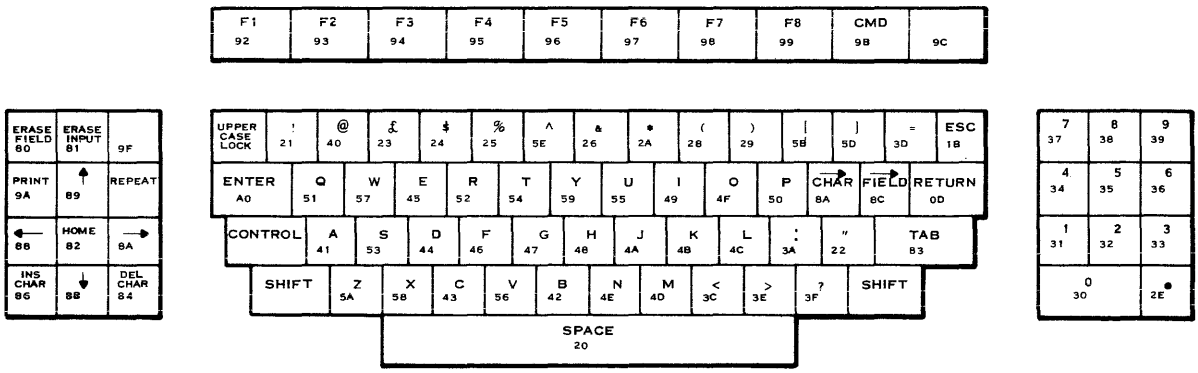


Figure A-6. United Kingdom Keyboard Showing Shift Mode Character Positions and Hexadecimal Codes

Table A-2. United Kingdom Model 911 VDT ASCII and Special Character Set

b8 b7 b6 b5 / b4 b3 b2 b1	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0
0 0 0 0	NUL	DLC	SP	0	@	P	\	p	ERASE FIELD	HERE IS	ENTER
0 0 0 1	SOH	DC1	!	1	A	Q	a	q	ERASE INPUT		XF1
0 0 1 0	STX	DC2	"	2	B	R	b	r	HOME	F1	
0 0 1 1	ETX	DC3	£	3	C	S	c	s	TAB	F2	
0 1 0 0	EOT	DC4	$	4	D	T	d	t	DELETE CHAR	F3	
0 1 0 1	ENQ	NAK	%	5	E	U	e	u	SKIP	F4	
0 1 1 0	ACK	SYN	&	6	F	V	f	v	INSERT CHAR	F5	
0 1 1 1	BEL	ETB	'	7	G	W	g	w	FIELD ←	F6	
1 0 0 0	BS	CAN	(	8	H	X	h	x	←	F7	
1 0 0 1	HT	EM	)	9	I	Y	i	y	↑	F8	
1 0 1 0	LF	SUB	*	:	J	Z	j	z	→	PRINT	
1 0 1 1	VT	ESC	+	;	K	[	k	{	↓	CMD	
1 1 0 0	FF	FS	,	<	L	\	l	|	→ FIELD		
1 1 0 1	CR	GS	-	=	M	]	m	}	XF2		
1 1 1 0	SO	RS	.	>	N	^	n	~	XF3		
1 1 1 1	SI	US	/	?	O	_	o	DEL	XF4		

(A)140675A

X \ Y	0	1	2	3	4	5	6	7	8	9
0	ERASE FIELD	PRINT	←	INSERT CHAR.	ERASE INPUT	↑	HOME	↓	→	DELETE CHAR
1	F1	F2	F3	F4	F5	F6	F7	F8	CMD	NOT USED
2	0	1	2	3	4	5	6	7	8	9
3	•	ESC	RETURN	TAB SKIP	KEY 67 NOT USED	= —	→ FIELD ←	// /	? /	KEY 91 NOT USED
4	] –	→ CHAR ←	: ;	> •	[+	P	L	< ,	) 0	0
5	K	M	N	J	I	(9	B	H	U	* 8
6	& 7	Y	G	V	C	F	T	^ 6	SPACE	X
7	D	R	% 5	Z	S	E	$ 4	£ 3	W	NOT USED
8	@ 2	! 1	Q	ENTER	A	KEY 89 NOT USED	NOT USED	←	→	NOT USED-

(A)136314

Figure A-7. United Kingdom Model 911 VDT Keyboard Matrix Chart

APPENDIX B

FRENCH MODEL 911 VDT KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, ASCII, SPECIAL CHARACTER SET, AND MATRIX CHART

APPENDIX B

FRENCH MODEL 911 VDT KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, ASCII, SPECIAL CHARACTER SET, AND MATRIX CHART

The standard limited -ASCII French Model 911 VDT keyboard layout and symbolization are shown in figure B-1. Figure B-2 shows the same keyboard with the keys numbered. Table B-1 lists the special character set hexadecimal code outputs by key number, key legend, and mode of the French Model 911 VDT keyboard. Figures B-3 through B-6 show keyboard mode character positions. Table B-2 lists the French ASCII and special character set. The keyboard matrix chart is shown in figure B-7.

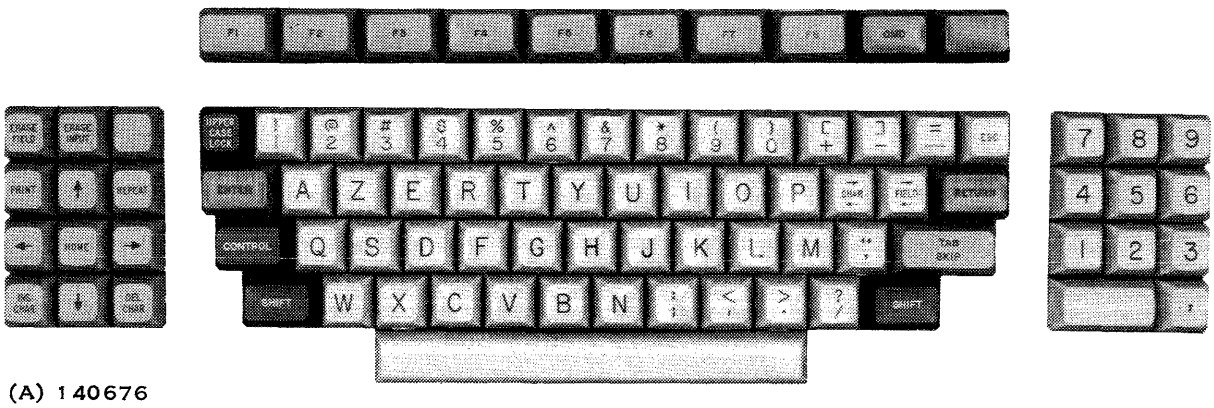


Figure B-1. French Model 911 VDT Keyboard Arrangement

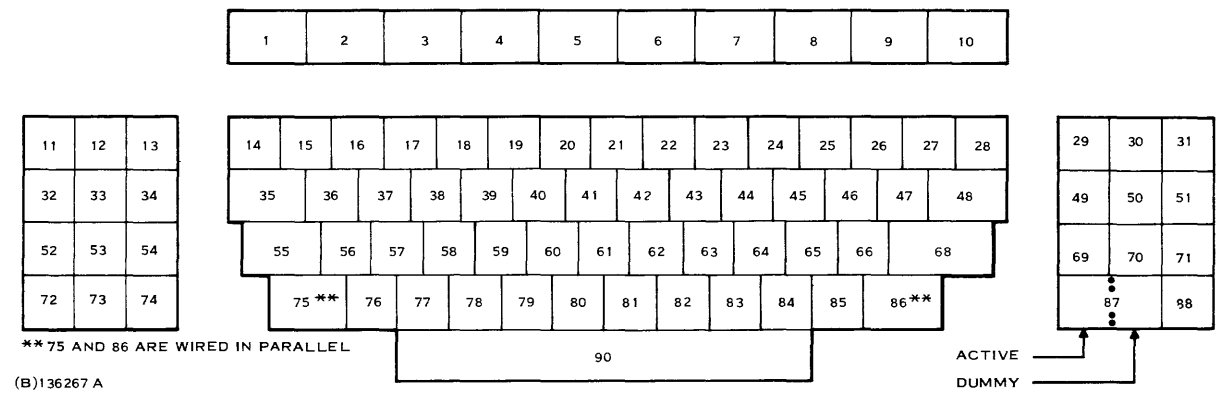


Figure B-2. French Model 911 VDT Keyboard with Keys Numbered

Table B-1. French Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs

KEY NUMBER	KEY LEGEND	MODE *			
		LC	UC	S	C
17	# 3	33	33	23	00
22	* 8	38	38	2A	7C
24	) 0	30	30	29	7E
25	[+	2B	2B	5B	1D
26	] –	2D	2D	5D	7F
27	= —	5F	5F	3D	5C
36	A	61	41	41	01
37	Z	7A	5A	5A	1A
41	Y	79	59	59	19
46	→ CHAR ←	88	88	8A	88
47	→ FIELD ←	87	87	8C	87
48	RETURN	0D	0D	0D	0D
56	Q	71	51	51	11
65	M	6D	4D	4D	0D
66	' ,	27	27	22	7D
76	W	77	57	57	17
82	: ;	3B	3B	3A	7B
88	,	2C	2C	2C	2C

* LC = LOWER CASE
UC = UPPER CASE
S = SHIFT
C = CONTROL

(A) 140677

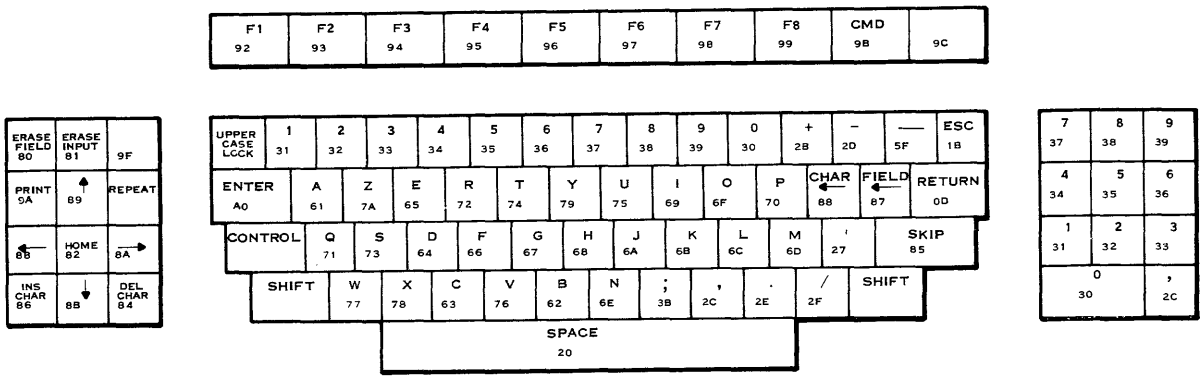


Figure B-3. French Keyboard Showing Lowercase Mode Character Positions and Hexadecimal Codes

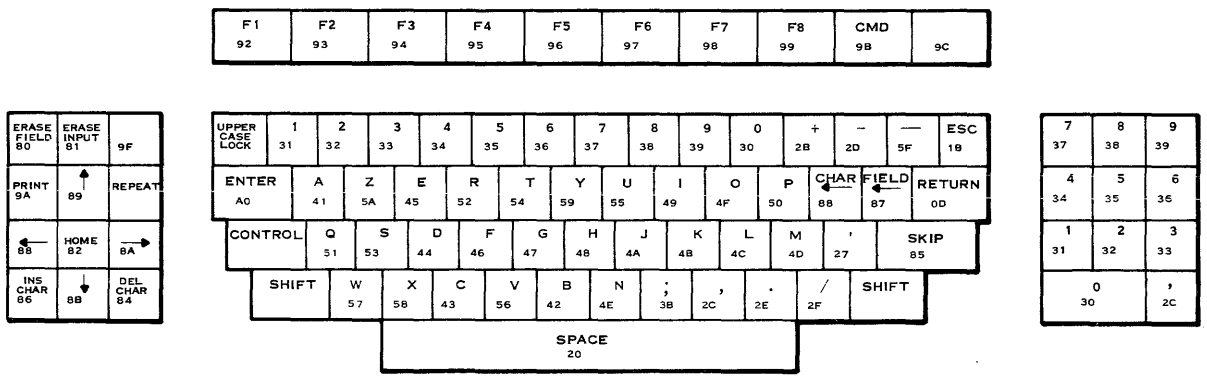


Figure B-4. French Keyboard Showing Uppercase Mode Character Positions and Hexadecimal Codes

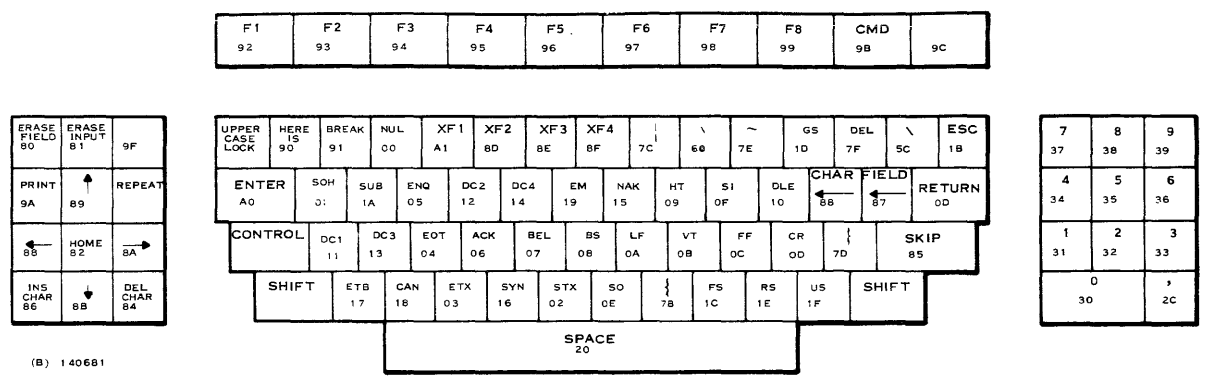


Figure B-5. French Keyboard Showing Control Character Positions and Hexadecimal Codes

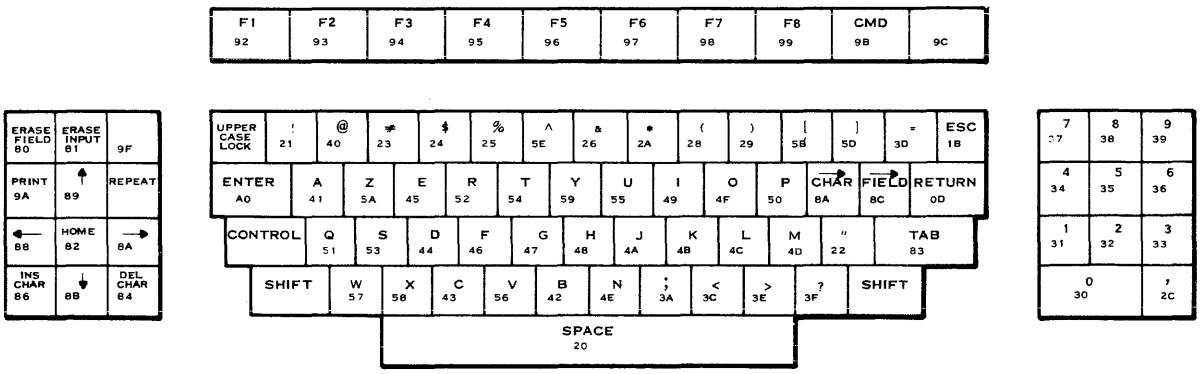


Figure B-6. French Keyboard Showing Shift Mode Character Positions and Hexadecimal Codes

Table B-2. French Model 911 VDT ASCII and Special Character Set

b8 b7 b6 b5 / b4 b3 b2 b1	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0
0 0 0 0	NUL	DLC	SP	0	@	P	`	p	ERASE FIELD	HERE IS	ENTER
0 0 0 1	SOH	DC1	!	1	A	Q	a	q	ERASE INPUT		XF1
0 0 1 0	STX	DC2	"	2	B	R	b	r	HOME	F1	
0 0 1 1	ETX	DC3	#	3	C	S	c	s	TAB	F2	
0 1 0 0	EOT	DC4	$	4	D	T	d	t	DELETE CHAR	F3	
0 1 0 1	ENQ	NAK	%	5	E	U	e	u	SKIP	F4	
0 1 1 0	ACK	SYN	&	6	F	V	f	v	INSERT CHAR	F5	
0 1 1 1	BEL	ETB	'	7	G	W	g	w	FIELD ←	F6	
1 0 0 0	BS	CAN	(	8	H	X	h	x	←	F7	
1 0 0 1	HT	EM	)	9	I	Y	i	y	↑	F8	
1 0 1 0	LF	SUB	*	:	J	Z	j	z	→	PRINT	
1 0 1 1	VT	ESC	+	;	K	[	k	{	↓	CMD	
1 1 0 0	FF	FS	,	<	L	\	l	|	→ FIELD		
1 1 0 1	CR	GS	-	=	M	]	m	}	XF2		
1 1 1 0	SO	RS	.	>	N	^	n	~	XF3		
1 1 1 1	SI	US	/	?	O	_	o	DEL	XF4		

(A)140678

X \ Y	0	1	2	3	4	5	6	7	8	9
0	ERASE FIELD	PRINT	←	INSERT CHAR.	ERASE INPUT	↑	HOME	↓	→	DELETE CHAR
1	F1	F2	F3	F4	F5	F6	F7	F8	CMD	NOT USED
2	0	1	2	3	4	5	6	7	8	9
3	'	ESC	RETURN	TAB SKIP	KEY 67 NOT USED	= _	→ FIELD ←	" |	? /	KEY 91 NOT USED
4	] _	→ CHAR ←	M	> .	[+	P	L	< ,	) 0	0
5	K	: . ;	N	J	I	(9	B	H	U	* 8
6	& 7	Y	G	V	C	F	T	^ 6	SPACE	X
7	D	R	% 5	W	S	E	$ 4	# 3	Z	NOT USED
8	@ 2	! : 1	A	ENTER	Q	FOR KEY 2	NOT USED	←	→	NOT USED

(A) 140683

Figure B-7. French Model 911 VDT Keyboard Matrix Chart

APPENDIX C

GERMAN MODEL 911 VDT KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, ASCII, SPECIAL CHARACTER SET, AND MATRIX CHART

APPENDIX C

GERMAN MODEL 911 VDT KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, ASCII, SPECIAL CHARACTER SET, AND MATRIX CHART

The standard limited-ASCII German Model 911 VDT keyboard layout and symbolization are shown in figure C-1. Figure C-2 shows the same keyboard with the keys numbered. Table C-1 lists the special character set hexadecimal code outputs by key number, key legend, and mode of the German Model 911 VDT keyboard. Figures C-3 through C-6 show keyboard mode character positions. Table C-2 lists the German ASCII and special character set. The keyboard matrix chart is shown in figure C-7.

Figure C-1. German Model 911 VDT Keyboard Arrangement

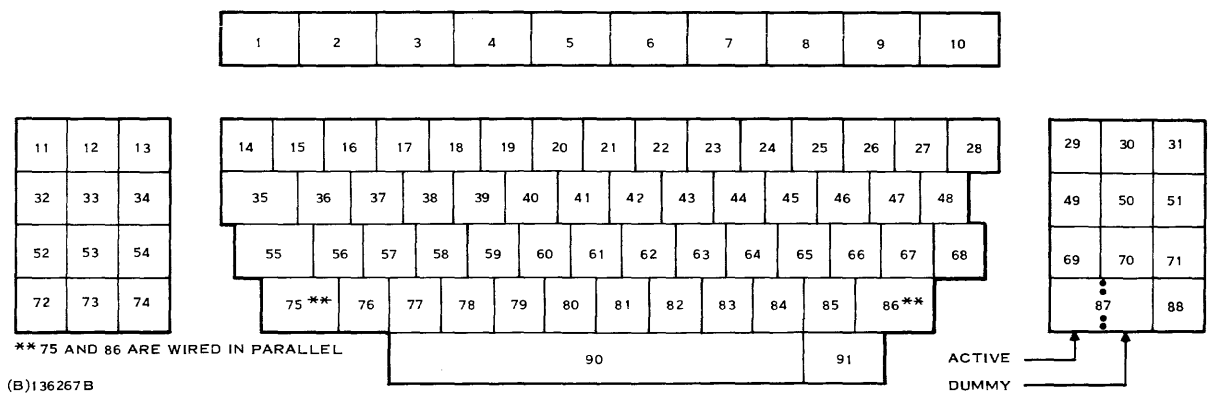


Figure C-2. German Model 911 VDT Keyboard with Keys Numbered

Table C-1. German Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs

KEY NUMBER	KEY LEGEND	MODE *			
		LC	UC	S	C
17	# 3	33	33	23	00
22	* 8	38	38	2A	7C
24	) 0	30	30	29	00
25	— +	2B	2B	5F	1D
26	= –	2D	2D	3D	7F
27	ß	7E	27	22	00
36	Q	71	51	51	11
37	W	77	57	57	17
41	Z	7A	5A	5A	1A
46	ü	7D	5D	5D	00
47	→ CHAR ←	88	88	8A	88
48	→ FIELD ←	87	87	8C	87
56	A	61	41	41	01
65	ö	7C	5C	5C	00
66	ä	7B	5B	5B	00
67	: ;	3B	3B	3A	00
76	Y	79	59	59	19
82	M	6D	4D	4D	0D
88	,	2C	2C	2C	2C
91	RETURN	0D	0D	0D	0D

* LC = LOWER CASE
UC = UPPER CASE
S = SHIFT
C = CONTROL

(A) 140685

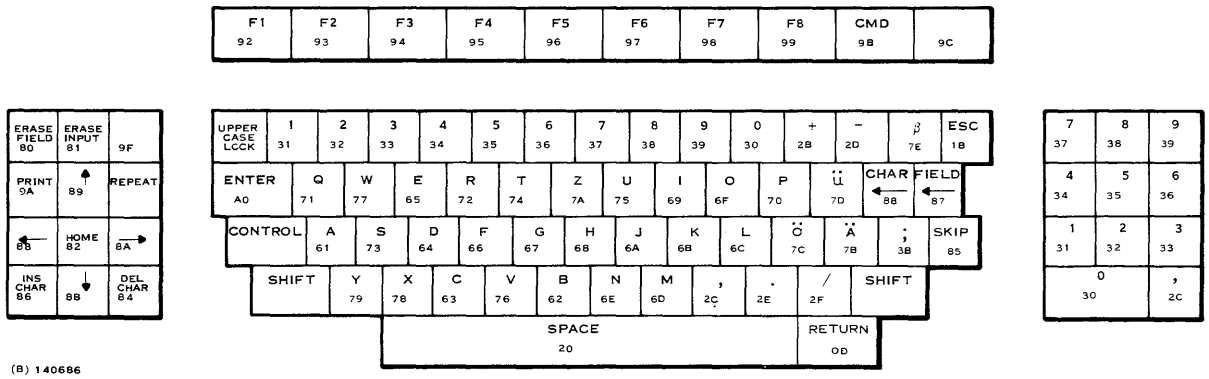


Figure C-3. German Keyboard Showing Lowercase Mode Character Positions and Hexadecimal Codes

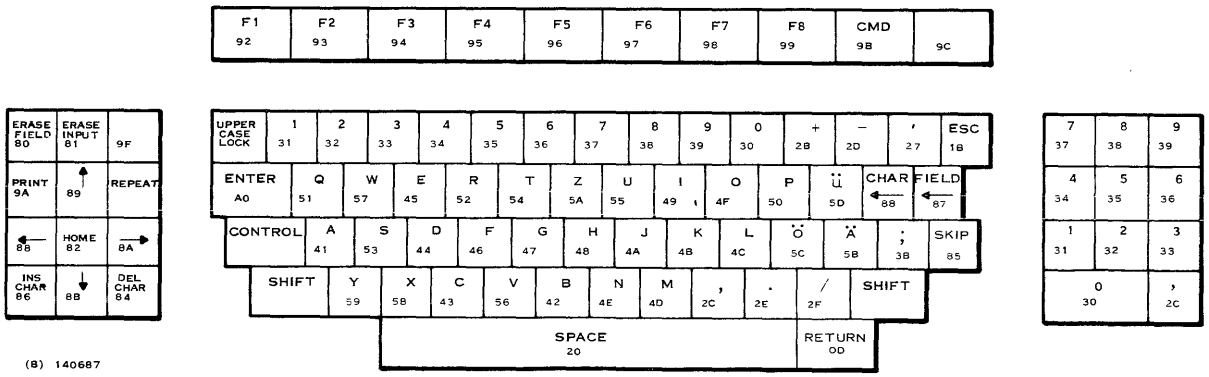


Figure C-4. German Keyboard Showing Uppercase Mode Character Positions and Hexadecimal Codes

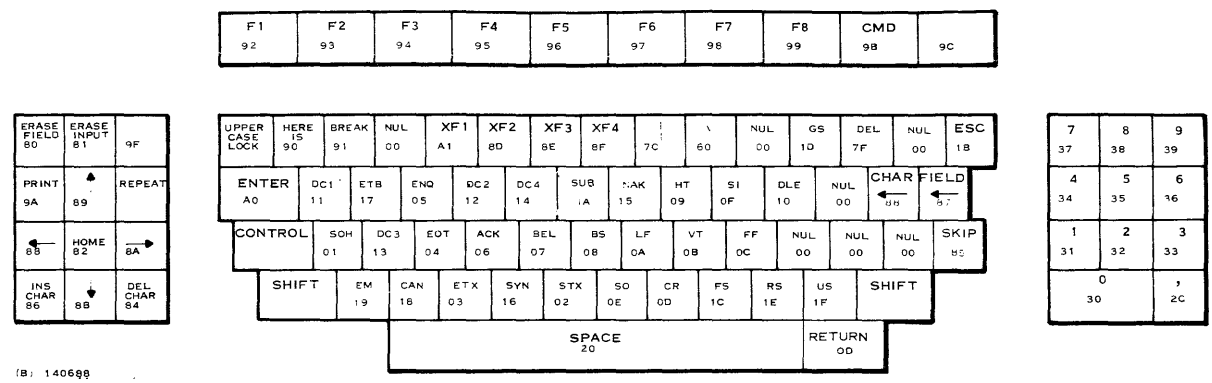


Figure C-5. German Keyboard Showing Control Character Positions and Hexadecimal Codes

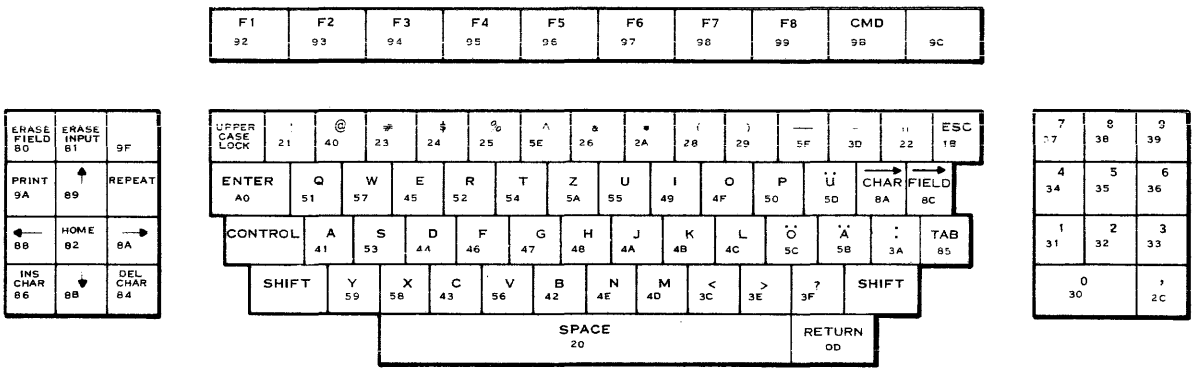
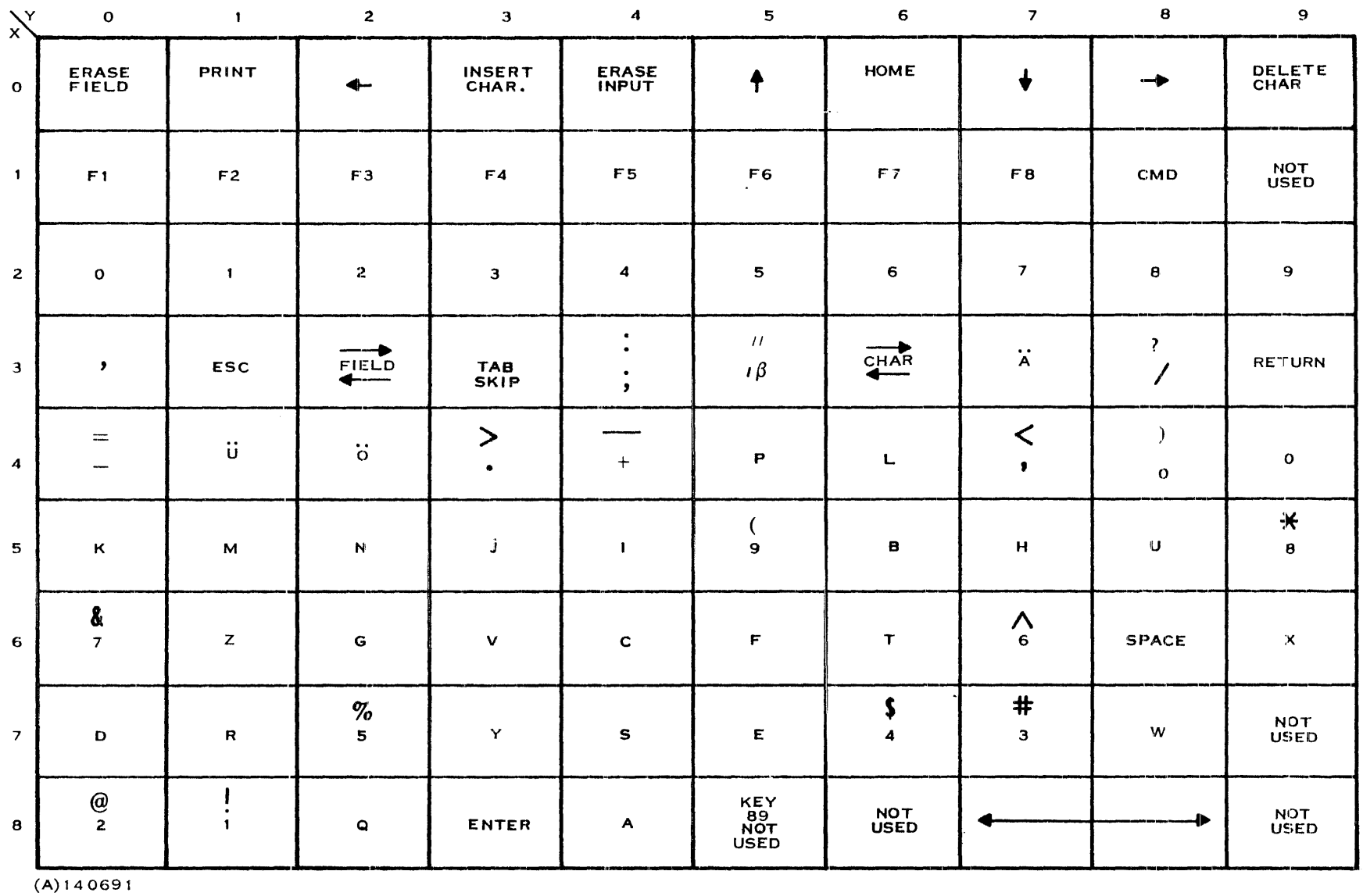


Figure C-6. German Keyboard Showing Shift Mode Character Positions and Hexadecimal Codes

Table C-2. German Model 911 VDT ASCII and Special Character Set

b8 b7 b6 b5 / b4 b3 b2 b1	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0
0 0 0 0	NUL	DLC	SP	0	@	P	`	p	ERASE FIELD	HERE IS	ENTER
0 0 0 1	SOH	DC1	!	1	A	Q	a	q	ERASE INPUT		XF1
0 0 1 0	STX	DC2	"	2	B	R	b	r	HOME	F1	
0 0 1 1	ETX	DC3	#	3	C	S	c	s	TAB	F2	
0 1 0 0	EOT	DC4	$	4	D	T	d	t	DELETE CHAR	F3	
0 1 0 1	ENQ	NAK	%	5	E	U	e	u	SKIP	F4	
0 1 1 0	ACK	SYN	&	6	F	V	f	v	INSERT CHAR	F5	
0 1 1 1	BEL	ETB	'	7	G	W	g	w	FIELD ←	F6	
1 0 0 0	BS	CAN	(	8	H	X	h	x	←	F7	
1 0 0 1	HT	EM	)	9	I	Y	i	y	↑	F8	
1 0 1 0	LF	SUB	*	:	J	Z	j	z	→	PRINT	
1 0 1 1	VT	ESC	+	;	K	Ä	k	ä	↓	CMD	
1 1 0 0	FF	FS	,	<	L	Ö	l	ö	FIELD →		
1 1 0 1	CR	GS	-	=	M	Ü	m	ü	XF2		
1 1 1 0	SO	RS	.	>	N	^	n	ß	XF3		
1 1 1 1	SI	US	/	?	O	_	o	DEL	XF4		

(A)140690



Y / X	0	1	2	3	4	5	6	7	8	9
0	ERASE FIELD	PRINT	←	INSERT CHAR.	ERASE INPUT	↑	HOME	↓	→	DELETE CHAR
1	F1	F2	F3	F4	F5	F6	F7	F8	CMD	NOT USED
2	0	1	2	3	4	5	6	7	8	9
3	,	ESC	FIELD → / ←	TAB SKIP	: / ;	// / ß	CHAR → / ←	Ä	? / /	RETURN
4	= / –	Ü	Ö	> / .	— / +	P	L	< / ,	) / 0	0
5	K	M	N	J	I	(/ 9	B	H	U	* / 8
6	& / 7	Z	G	V	C	F	T	^ / 6	SPACE	X
7	D	R	% / 5	Y	S	E	$ / 4	# / 3	W	NOT USED
8	@ / 2	! / 1	Q	ENTER	A	KEY 89 NOT USED	NOT USED	←	→	NOT USED

(A)140691

Figure C-7. German Model 911 VDT Keyboard Matrix Chart

APPENDIX D

SWEDISH/FINNISH MODEL 911 VDT KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, ASCII, SPECIAL CHARACTER SET, AND MATRIX CHART

APPENDIX D

SWEDISH/FINNISH MODEL 911 VDT KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, ASCII, SPECIAL CHARACTER SET, AND MATRIX CHART

The standard limited-ASCII Swedish/Finnish Model 911 VDT keyboard layout and symbolization are shown in figure D-1. Figure D-2 shows the same keyboard with keys numbered. Table D-1 lists the special character set hexadecimal code outputs by key number, key legend, and mode of the Swedish/Finnish Model 911 VDT keyboard. Figures D-3 through D-6 show keyboard mode character positions. Table D-2 lists the Swedish/Finnish ASCII and special character set. The keyboard matrix chart is shown in figure D-7.

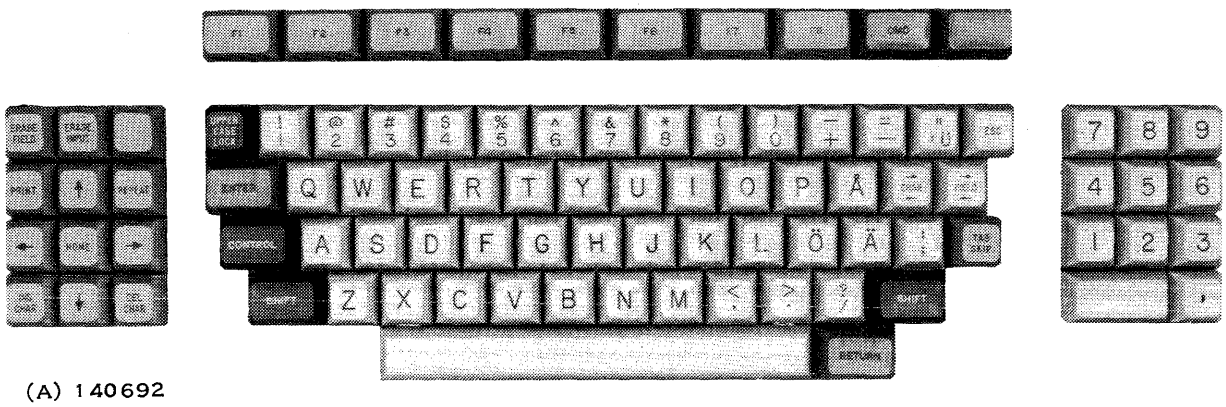


Figure D-1. Swedish/Finnish Model 911 VDT Keyboard Arrangement

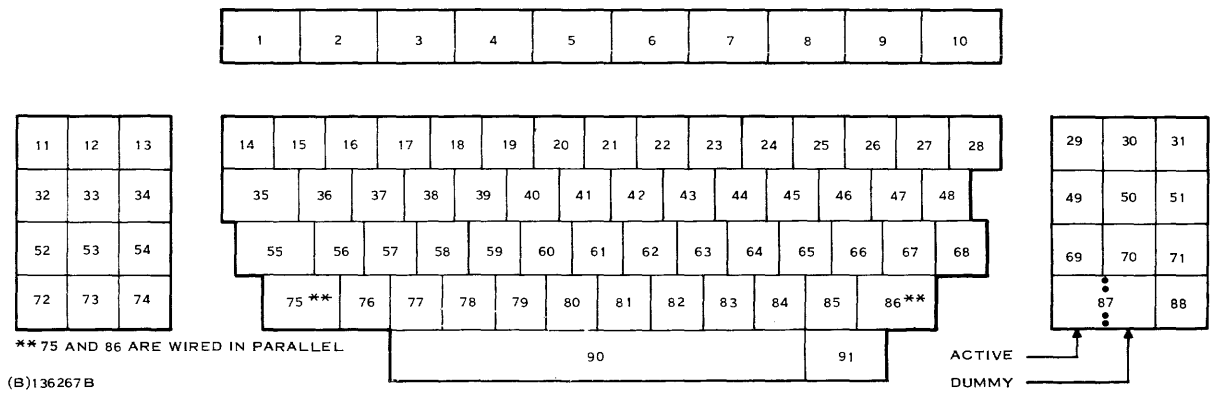


Figure D-2. Swedish/Finnish Model 911 VDT Keyboard with Keys Numbered

Table D-1. Swedish/Finnish Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs

KEY NUMBER	KEY LEGEND	MODE *			
		LC	UC	S	C
17	# 3	33	33	23	00
22	* 8	38	38	2A	00
24	) 0	30	30	29	00
25	— +	2B	2B	5F	1D
26	= --	2D	2D	3D	7F
27	¨ Ü	7E	27	22	00
36	Q	71	51	51	11
37	W	77	57	57	17
41	Y	79	59	59	19
46	˚ Å	7D	5D	5D	00
47	→ CHAR ←	88	88	8A	88
48	→ FIELD ←	87	87	8C	87
56	A	61	41	41	01
65	¨ Ö	7C	5C	5C	00
66	¨ Ä	7B	5B	5B	00
67	: ;	3B	3B	3A	00
76	Z	7A	5A	5A	1A
82	M	6D	4D	4D	0D
88	,	2C	2C	2C	2C
91	RETURN	0D	0D	0D	0D

* LC = LOWER CASE
UC = UPPER CASE
S = SHIFT
C = CONTROL

(A) 140693

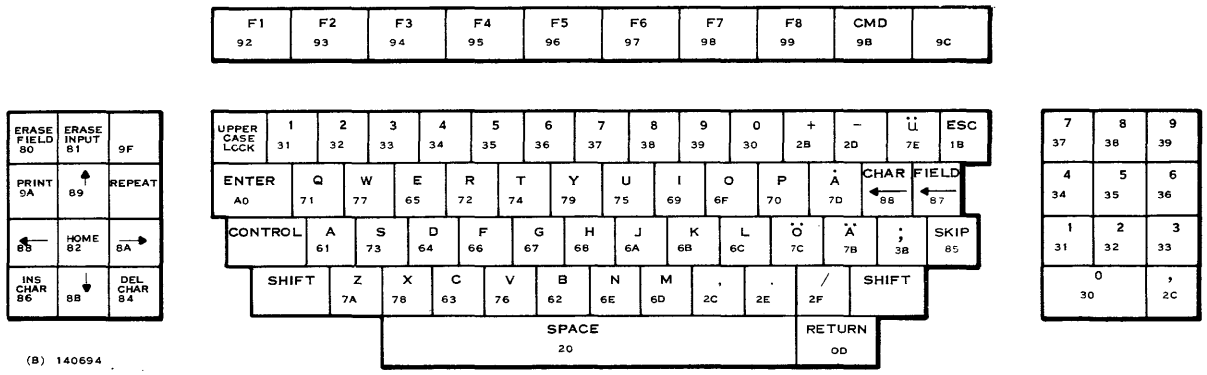


Figure D-3. Swedish/Finnish Keyboard Showing Lowercase Mode Character Positions and Hexadecimal Codes

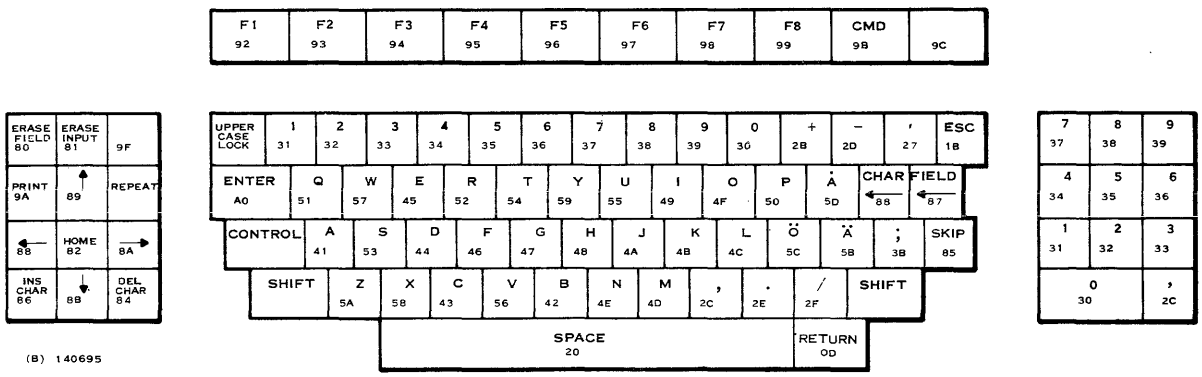


Figure D-4. Swedish/Finnish Keyboard Showing Uppercase Mode Character Positions and Hexadecimal Codes

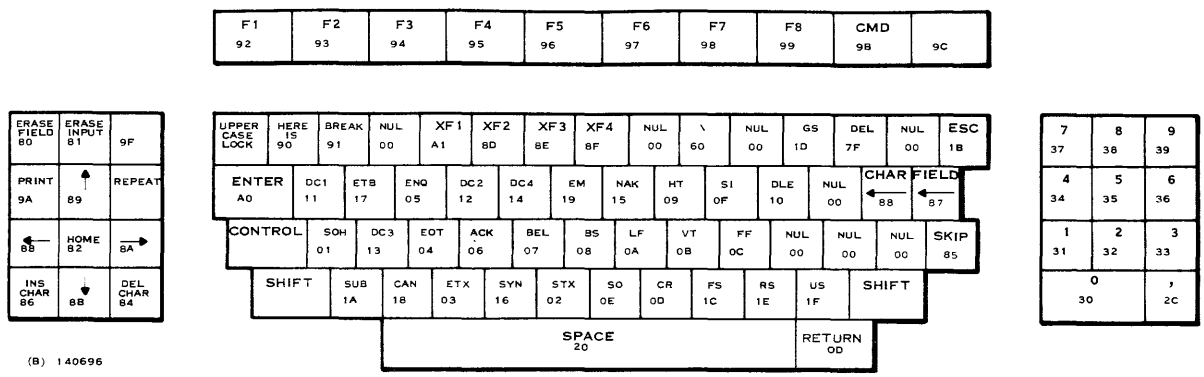


Figure D-5. Swedish/Finnish Keyboard Showing Control Character Positions and Hexadecimal Codes

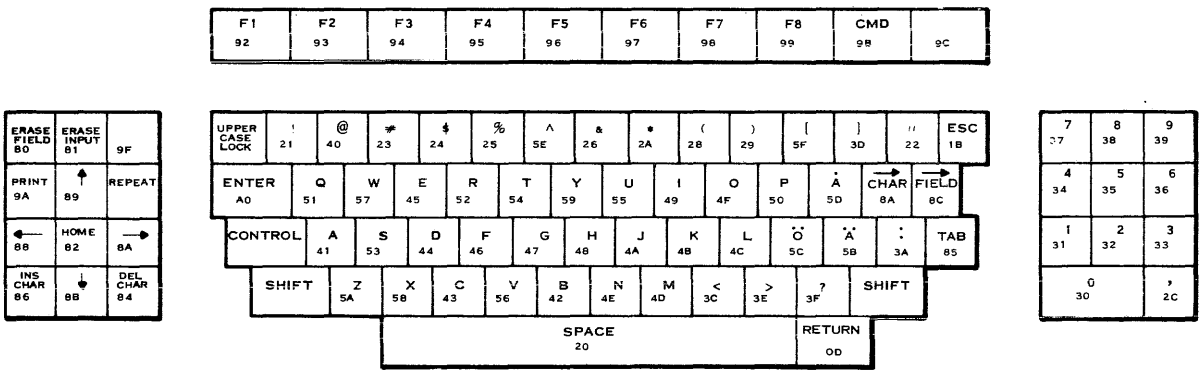


Figure D-6. Swedish/Finnish Keyboard Showing Shift Mode Character Positions and Hexadecimal Codes

Table D-2. Swedish/Finnish Model 911 VDT ASCII and Special Character Set

b8 b7 b6 b5 / b4 b3 b2 b1	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0
0 0 0 0	NUL	DLC	SP	0	@	P	\	p	ERASE FIELD	HERE IS	ENTER
0 0 0 1	SOH	DC1	!	1	A	Q	a	q	ERASE INPUT		XF1
0 0 1 0	STX	DC2	"	2	B	R	b	r	HOME	F1	
0 0 1 1	ETX	DC3	#	3	C	S	c	s	TAB	F2	
0 1 0 0	EOT	DC4	$	4	D	T	d	t	DELETE CHAR	F3	
0 1 0 1	ENQ	NAK	%	5	E	U	e	u	SKIP	F4	
0 1 1 0	ACK	SYN	&	6	F	V	f	v	INSERT CHAR	F5	
0 1 1 1	BEL	ETB	'	7	G	W	g	w	FIELD ←	F6	
1 0 0 0	BS	CAN	(	8	H	X	h	x	←	F7	
1 0 0 1	HT	EM	)	9	I	Y	i	y	↑	F8	
1 0 1 0	LF	SUB	*	:	J	Z	j	z	→	PRINT	
1 0 1 1	VT	ESC	+	;	K	Ä	k	ä	↓	CMD	
1 1 0 0	FF	FS	,	<	L	Ö	l	ö	FIELD →		
1 1 0 1	CR	GS	-	=	M	Å	m	å	XF2		
1 1 1 0	SO	RS	.	>	N	^	n	ü	XF3		
1 1 1 1	SI	US	/	?	O	_	o	DEL	XF4		

(A)140698

X \ Y	0	1	2	3	4	5	6	7	8	9
0	ERASE FIELD	PRINT	←	INSERT CHAR.	ERASE INPUT	↑	HOME	↓	→	DELETE CHAR
1	F1	F2	F3	F4	F5	F6	F7	F8	CMD	NOT USED
2	0	1	2	3	4	5	6	7	8	9
3	'	ESC	→ FIELD ←	TAB SKIP	: ;	// / Ü	→ CHAR ←	Ä	? /	RETURN
4	= –	Å	Ö	> .	— +	P	L	< ,	) 0	0
5	K	M	N	J	I	(9	B	H	U	* 8
6	& 7	Y	G	V	C	F	T	^ 6	SPACE	X
7	D	R	% 5	Z	S	E	$ 4	# 3	W	NOT USED
8	@ 2	! 1	Q	ENTER	A	KEY 89 NOT USED	NOT USED	←	→	NOT USED

(A)140699

Figure D-7. Swedish/Finnish Model 911 VDT Keyboard Matrix Chart

APPENDIX E

NORWEGIAN/DANISH KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, ASCII, SPECIAL CHARACTER SET, AND MATRIX CHART

APPENDIX E

NORWEGIAN/DANISH KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, ASCII, SPECIAL CHARACTER SET, AND MATRIX CHART

The standard limited-ASCII Norwegian/Danish Model 911 VDT keyboard layout and symbolization are shown in figure E-1. Figure E-2 shows the same keyboard with keys numbered. Table E-1 lists the special character set hexadecimal code output by key number, key legend, and mode of the Norwegian/Danish Model 911 VDT keyboard. Figures E-3 through E-6 show keyboard mode character positions. Table E-2 lists the Norwegian/Danish ASCII and special character set. The keyboard matrix chart is shown in figure E-7.

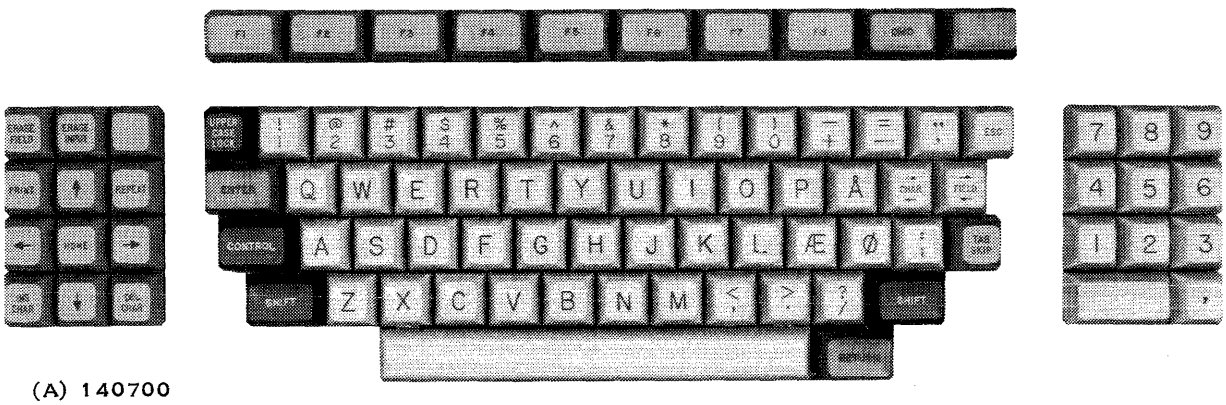


Figure E-1. Norwegian/Danish Model 911 VDT Keyboard Arrangement

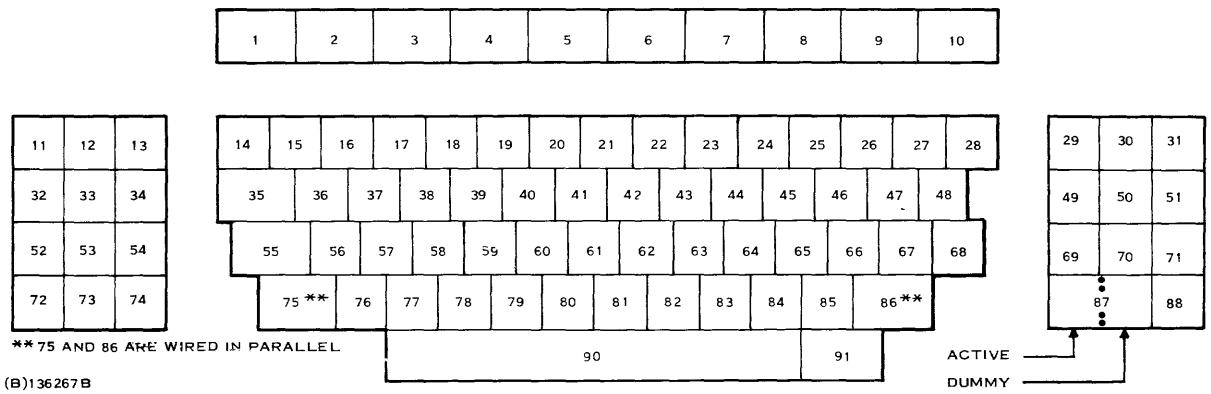


Figure E-2. Norwegian/Danish Model 911 VDT Keyboard with Keys Numbered

Table E-1. Norwegian/Danish Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs

KEY NUMBER	KEY LEGEND	MODE *			
		LC	UC	S	C
17	# 3	33	33	23	00
22	* 8	38	38	2A	00
24	) 0	30	30	29	00
25	— +	2B	2B	5F	1D
26	= –	2D	2D	3D	7F
27	| |	27	27	22	00
36	Q	71	51	51	11
37	W	77	57	57	17
41	Y	79	59	59	19
46	˙ Å	7D	5D	5D	00

KEY NUMBER	KEY LEGEND	MODE *			
		LC	US	S	C
47	→ CHAR ←	88	88	8A	88
48	→ FIELD ←	87	87	8C	87
56	A	61	41	41	01
65	Æ	7B	5B	5B	00
66	Ø	7C	5C	5C	00
67	: · ;	3B	3B	3A	00
76	Z	7A	5A	5A	1A
82	M	6D	4D	4D	0D
88	,	2C	2C	2C	2C
91	RETURN	0D	0D	0D	0D

* LC = LOWER CASE
UC = UPPER CASE
S = SHIFT
C = CONTROL

(A) 140701

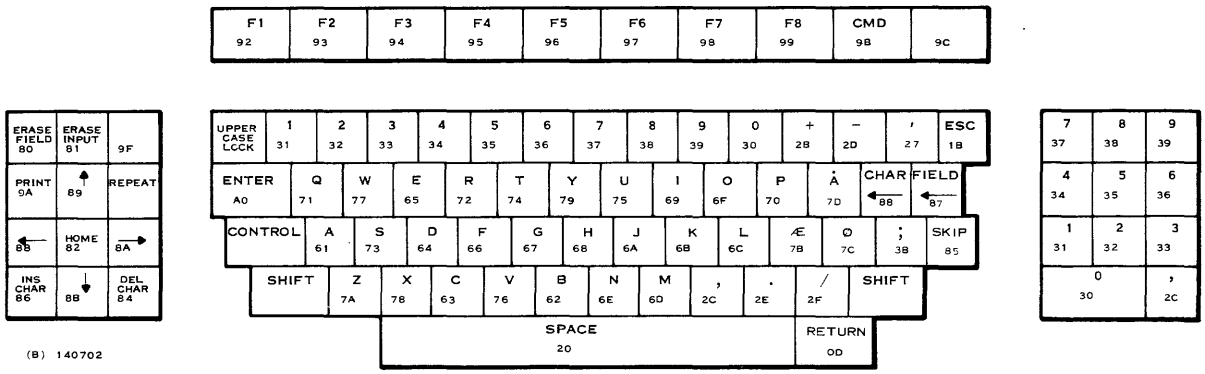


Figure E-3. Norwegian/Danish Keyboard Showing Lowercase Mode Character Positions and Hexadecimal Codes

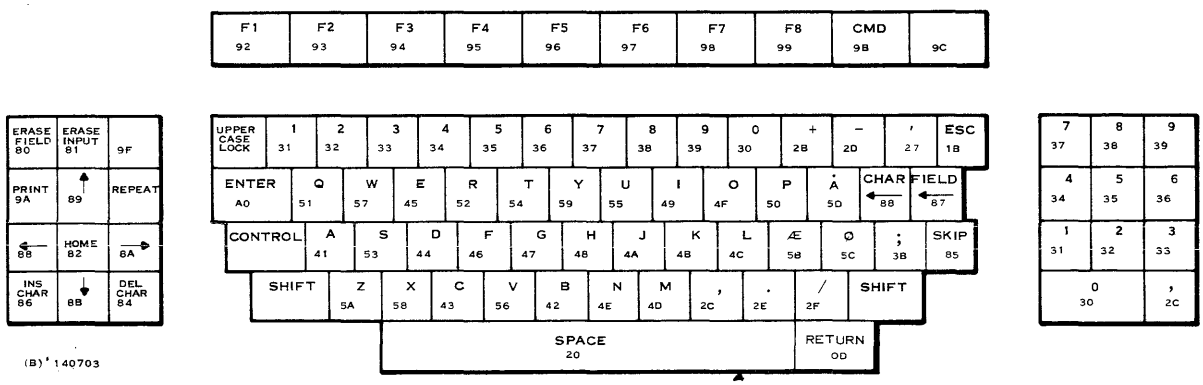


Figure E-4. Norwegian/Danish Keyboard Showing Uppercase Mode Character Positions and Hexadecimal Codes

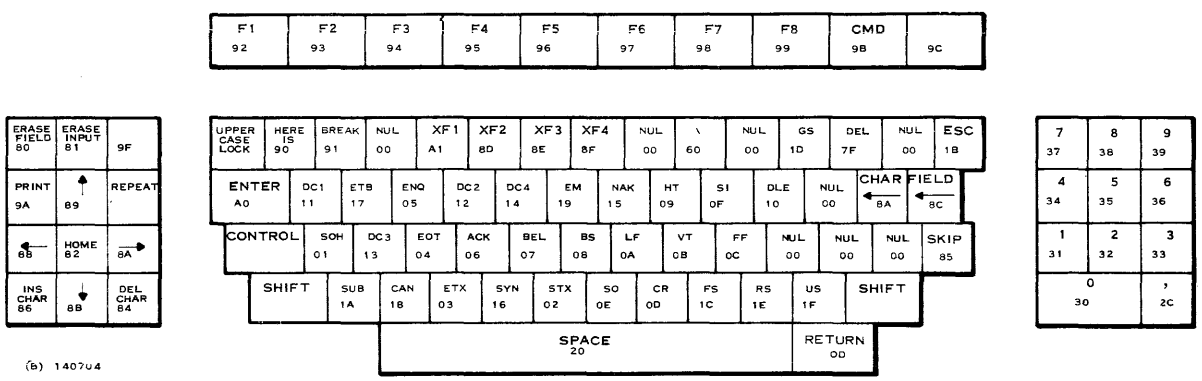
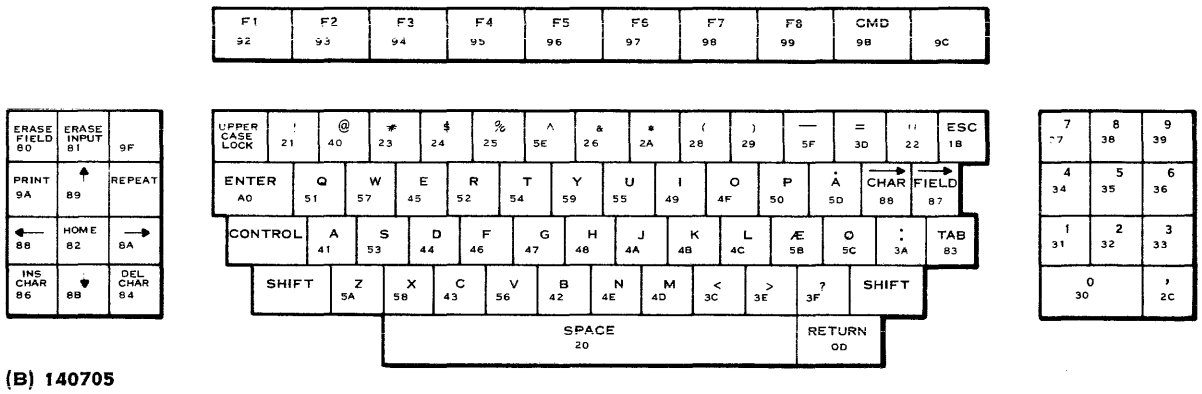


Figure E-5. Norwegian/Danish Keyboard Showing Control Character Positions and Hexadecimal Codes



(B) 140705

Figure E-6. Norwegian/Danish Keyboard Showing Shift Mode Character Positions and Hexadecimal Codes

Table E-2. Norwegian/Danish Model 911 VDT ASCII and Special Character Set

b8 b7 b6 b5 / b4 b3 b2 b1	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0
0 0 0 0	NUL	DLC	SP	0	@	P	\	p	ERASE FIELD	HERE IS	ENTER
0 0 0 1	SOH	DC1	!	1	A	Q	a	q	ERASE INPUT		XF1
0 0 1 0	STX	DC2	"	2	B	R	b	r	HOME	F1	
0 0 1 1	ETX	DC3	#	3	C	S	c	s	TAB	F2	
0 1 0 0	EOT	DC4	$	4	D	T	d	t	DELETE CHAR	F3	
0 1 0 1	ENQ	NAK	%	5	E	U	e	u	SKIP	F4	
0 1 1 0	ACK	SYN	&	6	F	V	f	v	INSERT CHAR	F5	
0 1 1 1	BEL	ETB	'	7	G	W	g	w	FIELD ←	F6	
1 0 0 0	BS	CAN	(	8	H	X	h	x	←	F7	
1 0 0 1	HT	EM	)	9	I	Y	i	y	↑	F8	
1 0 1 0	LF	SUB	*	:	J	Z	j	z	→	PRINT	
1 0 1 1	VT	ESC	+	;	K	Æ	k	æ	↓	CMD	
1 1 0 0	FF	FS	,	<	L	ø	l	ø	→ FIELD		
1 1 0 1	CR	GS	-	=	M	Å	m	å	XF2		
1 1 1 0	SO	RS	.	>	N	^	n	~	XF3		
1 1 1 1	SI	US	/	?	O	_	o	DEL	XF4		

(A)140706

X \ Y	0	1	2	3	4	5	6	7	8	9
0	ERASE FIELD	PRINT	←	INSERT CHAR.	ERASE INPUT	↑	HOME	↓	→	DELETE CHAR
1	F1	F2	F3	F4	F5	F6	F7	F8	CMD	NOT USED
2	0	1	2	3	4	5	6	7	8	9
3	,	ESC	→ FIELD ←	TAB SKIP	: ;	// /	→ CHAR ←	ø	? /	RETURN
4	= –	Å	Æ	> .	— +	P	L	< ,	) 0	0
5	K	M	N	J	I	(9	B	H	U	* 8
6	& 7	Y	G	V	C	F	T	^ 6	SPACE	X
7	D	R	% 5	Z	S	E	$ 4	# 3	W	NOT USED
8	@ 2	! 1	Q	ENTER	A	KEY 89 NOT USED	NOT USED	←	→	NOT USED

(A)140707

Figure E-7. Norwegian/Danish Model 911 VDT Keyboard Matrix Chart

APPENDIX F

JAPANESE KATAKANA KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, MODIFIED ASCII (JIS-8), SPECIAL CHARACTER SET, ADDITIONAL EIGHT-BIT DISPLAYED CHARACTER SET, KEYBOARD LOGIC DIAGRAM, AND CONTACT MATRIX INFORMATION

APPENDIX F

JAPANESE KATAKANA KEYBOARD ARRANGEMENT, HEXADECIMAL CODES, MODE CHARACTER POSITIONS, MODIFIED ASCII (JIS-8), SPECIAL CHARACTER SET, ADDITIONAL EIGHT-BIT DISPLAYED CHARACTER SET, KEYBOARD LOGIC DIAGRAM, AND CONTACT MATRIX INFORMATION

The standard limited-ASCII Japanese Katakana Model 911 VDT keyboard layout and symbolization are shown in figure F-1. Figure F-2 shows the same keyboard with keys numbered. Table F-1 lists the special character set hexadecimal code output by key number, key legend, and mode of the Japanese Katakana Model 911 VDT keyboard. Figures F-3 through F-8 show keyboard mode character positions. Table F-2 lists the Japanese Katakana modified ASCII (JIS-8) and special character set. The additional 128 eight-bit characters included in the displayed character set are illustrated in figure F-9. The keyboard logic diagram and contact matrix information are illustrated in figure F-10.

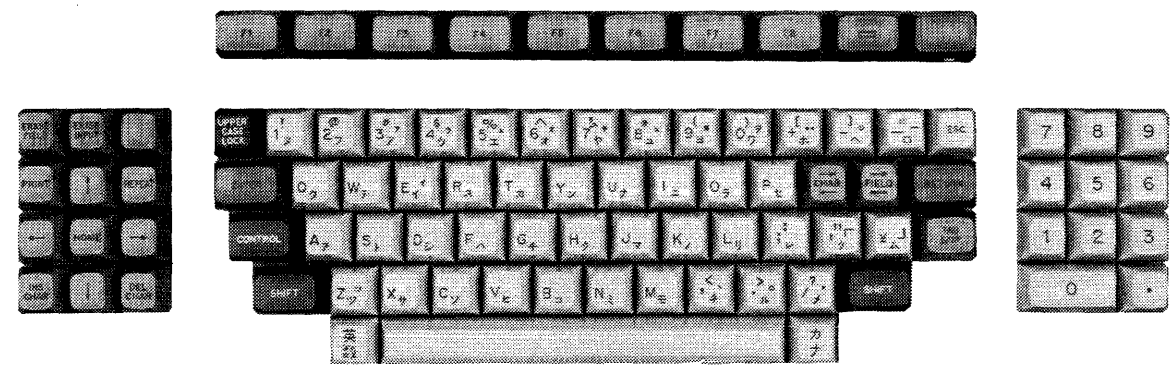


Figure F-1. Japanese Katakana Model 911 VDT Keyboard Arrangement

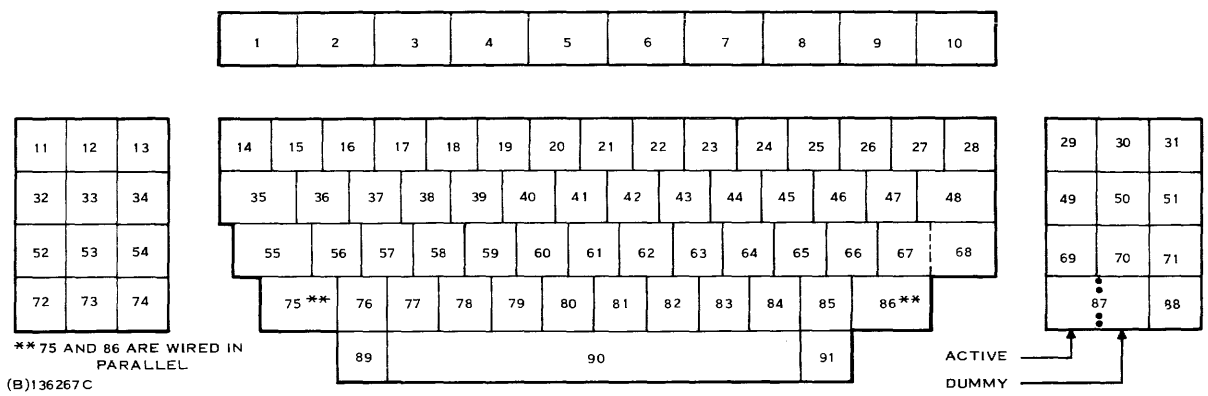


Figure F-2. Japanese Model 911 VDT Keyboard with Keys Numbered

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 1 of 11)

KEY NUMBER	KEY LEGEND	MODE *					
		N	UCL	S	UK	SK	C
1	F1	92	92	92	92	92	92
2	F2	93	93	93	93	93	93
3	F3	94	94	94	94	94	94
4	F4	95	95	95	95	95	95
5	F5	96	96	96	96	96	96
6	F6	97	97	97	97	97	97
7	F7	98	98	98	98	98	98
8	F8	99	99	99	99	99	99
9	CMD	9B	9B	9B	9B	9B	9B

* N = LOWER CASE ALPHA
UCL = UPPER CASE LOCK ALPHA
S = SHIFT
UK = UNSHIFTED KATAKANA
SK = SHIFT KATAKANA
C = CONTROL

(A) 140709 (1/11)

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 2 of 11)

KEY NUMBER	KEY LEGEND	MODE *					
		N	UCL	S	UK	SK	C
10		9C	9C	9C	9C	9C	9C
11	ERASE FIELD	80	80	80	80	80	80
12	ERASE INPUT	81	81	81	81	81	81
13		9F	9F	9F	9F	9F	9F
14	UPPER CASE LOCK						
15	! 1 ｱ	31	31	21	C7	00	90
16	@ 2 ﾂ	32	32	40	CC	00	91
17	# 3 ﾃ ﾇ	33	33	23	B1	A7	00
18	$ 4 ﾄ ｶﾞ	34	34	24	B3	A9	A1

(A) 140709 (2/11)

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 3 of 11)

KEY NUMBER	KEY LEGEND	MODE *					
		N	UCL	S	UK	SK	C
19	5 % エ オ	35	35	25	B4	AA	8D
20	6 ^ ヲ ナ	36	36	5E	B5	AB	8E
21	7 & ヲ ハ	37	37	26	D4	AC	8F
22	8 * ユ ヨ	38	38	2A	D5	AD	7C
23	9 (ヨ ム	39	39	28	D6	AE	60
24	0) ワ ヲ	30	30	29	DC	A6	7E
25	+ [ホ ヽ\	2B	2B	5B	CE	DE	1D
26	-] ゜ へ	2D	2D	5D	CD	DF	7F
27	— = ロ ン	5F	5F	3D	DB	B0	5C

(A) 140709 (3/11)

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 4 of 11)

KEY NUMBER	KEY LEGEND	MODE *					
		N	UCL	S	UK	SK	C
28	ESC	1B	1B	1B	1B	1B	1B
29	7	37	37	37	37	37	37
30	8	38	38	38	38	38	38
31	9	39	39	39	39	39	39
32	PRINT	9A	9A	9A	9A	9A	9A
33	↑	89	89	89	89	89	89
34	REPEAT						
35	ENTER	A0	A0	A0	A0	A0	A0
36	Q ｸ	71	51	51	C0	00	11

(A) 140709 (4/11)

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 5 of 11)

KEY NUMBER	KEY LEGEND	MODE *					
		N	UCL	S	UK	SK	C
37	W テ	77	57	57	C3	00	17
38	E イ ィ	65	45	45	B2	A8	05
39	R ス	72	52	52	BD	00	12
40	T カ	74	54	54	B6	00	14
41	Y ン	79	59	59	DD	00	19
42	U ナ	75	55	55	C5	00	15
43	I ニ	69	49	49	C6	00	09
44	O ラ	6F	4F	4F	D7	00	0F
45	P ト	70	50	50	BE	00	10

(A) 140709 (5/11)

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 6 of 11)

KEY NUMBER	KEY LEGEND	MODE*					
		N	UCL	S	UK	SK	C
46	→ CHAR ←	88	88	8A	88	8A	88
47	→ FIELD ←	87	87	8C	87	8C	87
48	RETURN	0D	0D	0D	0D	0D	0D
49	4	34	34	34	34	34	34
50	5	35	35	35	35	35	35
51	6	36	36	36	36	36	36
52	←	88	88	88	88	88	88
53	HOME	82	82	82	82	82	82
54	→	8A	8A	8A	8A	8A	8A

(A) 140709 (6/11)

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 7 of 11)

KEY NUMBER	KEY LEGEND	MODE *					
		N	UCL	S	UK	SK	C
55	CONTROL						
56	A チ	61	41	41	C1	00	01
57	S ト	73	53	53	C4	00	13
58	D シ	64	44	44	BC	00	04
59	F ハ	66	46	46	CA	00	06
60	G キ	67	47	47	B7	00	07
61	H ク	68	48	48	B8	00	08
62	J マ	6A	4A	4A	CF	00	0A
63	K ノ	6B	4B	4B	C9	00	0B

(A) 140709 (7/11)

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 8 of 11)

KEY NUMBER	KEY LEGEND	MODE *					
		N	UCL	S	UK	SK	C
64	L)	6C	4C	4C	D8	00	0C
65	; : ヽ	3B	3B	3A	DA	00	7B
66	\ 1 4 「	27	27	22	B9	A2	7D
67	¥ 4 」	5C	5C	00	D1	A3	00
68	TAB SKIP	85	85	83	85	83	85
69	1	31	31	31	31	31	31
70	2	32	32	32	32	32	32
71	3	33	33	33	33	33	33
72	INS CHAR	86	86	86	86	86	86

(A) 140709 (8/11)

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 9 of 11)

KEY NUMBER	KEY LEGEND	MODE *					
		N	UCL	S	UK	SK	C
73	↓	8B	8B	8B	8B	8B	8B
74	DEL CHAR	84	84	84	84	84	84
75	SHIFT						
76	Z ツ	7A	5A	5A	C2	AF	1A
77	X サ	78	58	58	BB	00	18
78	C ソ	63	43	43	BF	00	03
79	V ヒ	76	56	56	CB	00	16
80	B コ	62	42	42	BA	00	02
81	N ン	6E	4E	4E	D0	00	0E

(A) 140709 (9/11)

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 10 of 11)

KEY NUMBER	KEY LEGEND	MODE *					
		N	UCL	S	UK	SK	C
82	M ﾓ	6D	4D	4D	D3	00	0D
83	, ﾈ ヽ	2C	2C	3C	C8	A4	1C
84	. ﾙ o	2E	2E	3E	D9	A1	1E
85	? / ﾒ .	2F	2F	3F	D2	A5	1F
86	SHIFT						
87	0	30	30	30	30	30	30
88	.	2E	2E	2E	2E	2E	2E
89	ﾔ ﾒ ﾄ						
90		20	20	20	20	20	20

(A) 140709 (10/11)

Table F-1. Japanese Katakana Model 911 VDT Keyboard Special Character Set Hexadecimal Code Outputs (Sheet 11 of 11)

KEY NUMBER	KEY LEGEND	MODE *					
		N	UCL	S	UK	SK	C
91	力 ナ						

(A) 140709 (11/11)

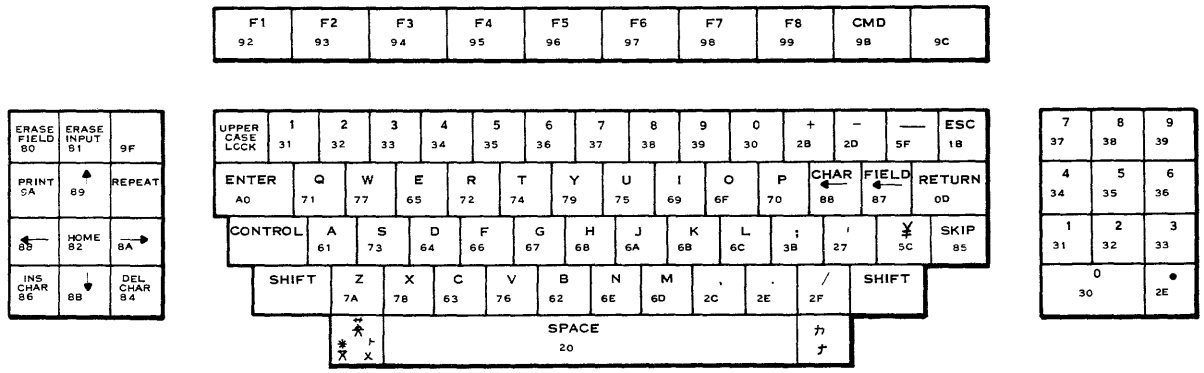


Figure F-3. Japanese Keyboard Showing Lowercase Alpha Mode Character Positions and Hexadecimal Codes

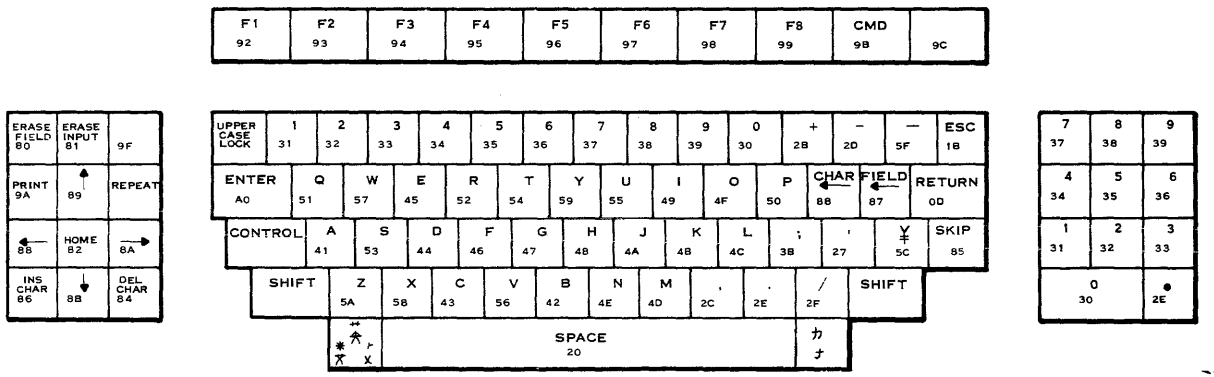


Figure F-4. Japanese Keyboard Showing Uppercase Lock Alpha Mode Character Positions and Hexadecimal Codes

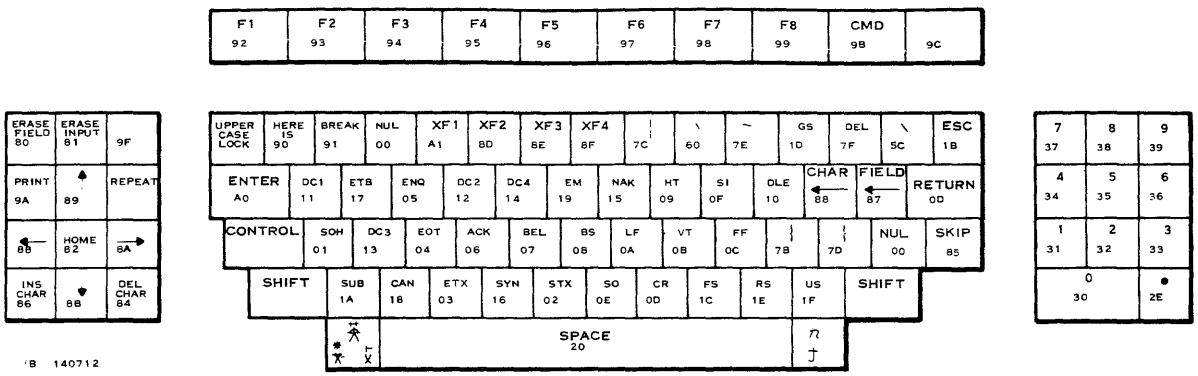


Figure F-5. Japanese Keyboard Showing Control Character Positions and Hexadecimal Codes

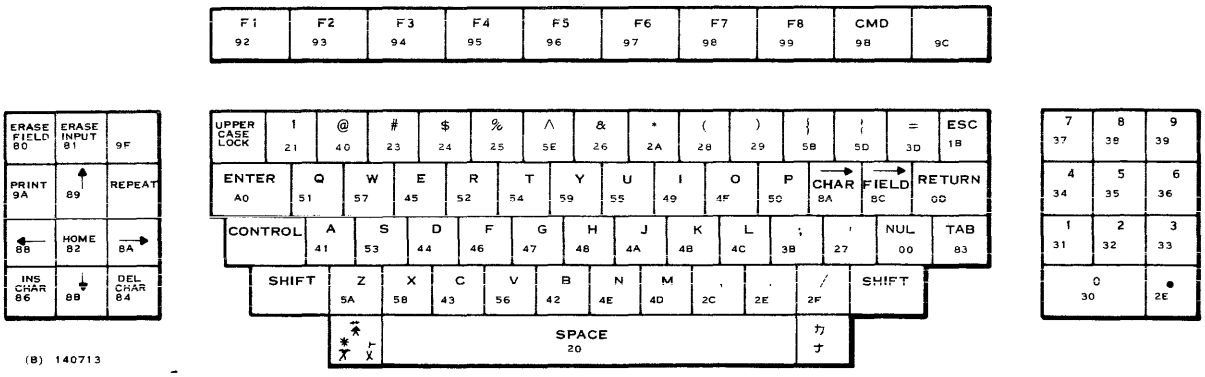


Figure F-6. Japanese Keyboard Showing Shift Mode Alpha Character Positions and Hexadecimal Codes

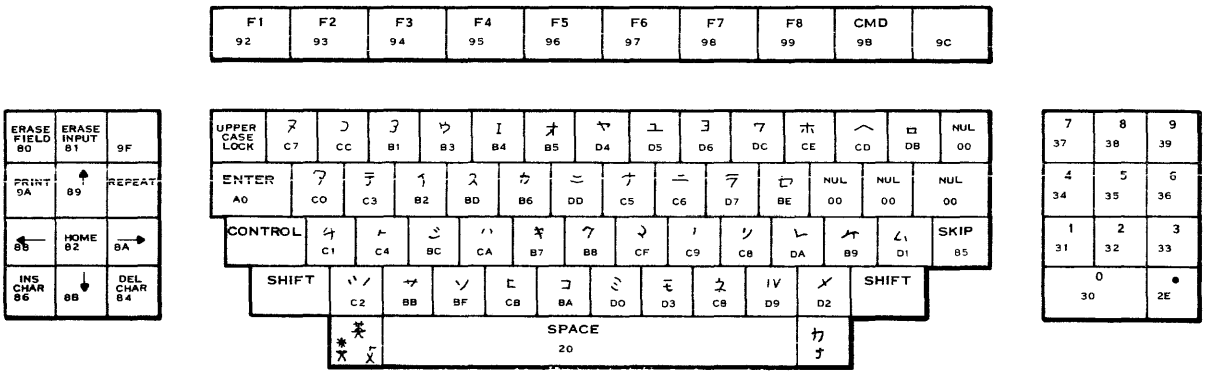


Figure F-7. Japanese Keyboard Showing Unshifted Katakana Character Positions and Hexadecimal Codes

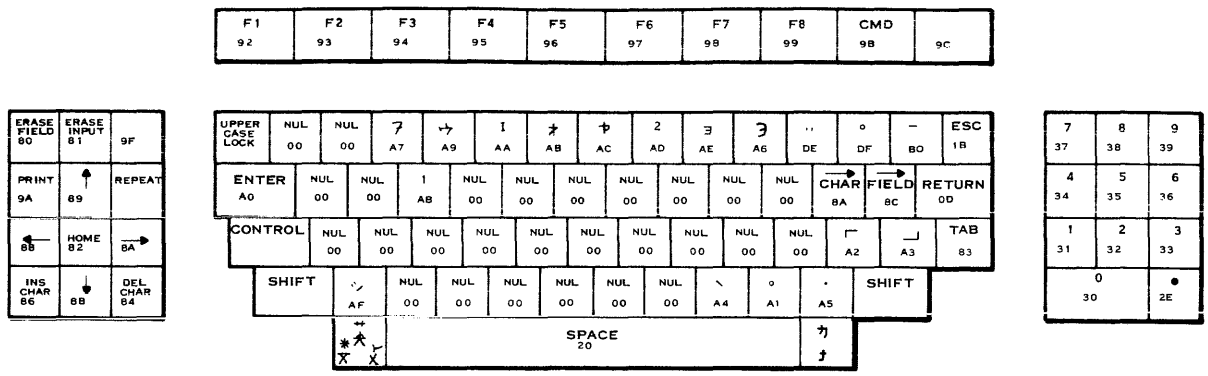


Figure F-8. Japanese Keyboard Showing Shifted Katakana Character Positions and Hexadecimal Codes

Table F-2. Japanese Katakana Modified ASCII (JIS-8) and Special Character Set

				b8	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				b7	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				b6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				b5	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
b4	b3	b2	b1		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0	0	NUL	DLE	SP	0	Q	P	\	p	ERASE FIELD	HERE IS	ENTER	−	タ	ミ		
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q	ERASE INPUT		｡	ｱ	チ	ム		
0	0	1	0	2	STX	DC2	"	2	B	R	b	r	HOME	F1	「	イ	ツ	メ		
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s	TAB	F2	」	ウ	テ	モ		
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t	DEL CHAR	F3	、	エ	ト	ヤ		
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u	SKIP	F4	・	オ	ナ	ユ		
0	1	1	0	6	ALK	SYN	&	6	F	V	f	v	INS CHAR	F5	ヲ	カ	ニ	ヨ		
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w	FIELD ←	F6	ｧ	キ	ヌ	ラ		
1	0	0	0	8	BS	CAN	(	8	H	X	h	x	CHAR ←	F7	ｨ	ク	ネ	リ		
1	0	0	1	9	HT	EM	)	9	I	Y	i	y	↑	F8	ｳ	ケ	ノ	ル		
1	0	1	0	A	LF	SUB	*	:	J	Z	j	z	CHAR →	PRINT	ｴ	コ	ハ	レ		
1	0	1	1	B	VT	ESC	+	;	K	[	k	{	↓	CMD	ｵ	サ	ヒ	ロ		
1	1	0	0	C	FF	FS	,	<	L	¥	l	¦	FIELD →		ｬ	シ	フ	ワ		
1	1	0	1	D	CR	GS	−	=	M	]	m	}			ｭ	ス	ヘ	ン		
1	1	1	0	E	SO	RS	.	>	N	^	n	~			ｮ	セ	ホ	ﾞ		
1	1	1	1	F	SI	US	/	?	O	−	o	DEL			ｯ	ソ	マ	ﾟ		

(A)140716

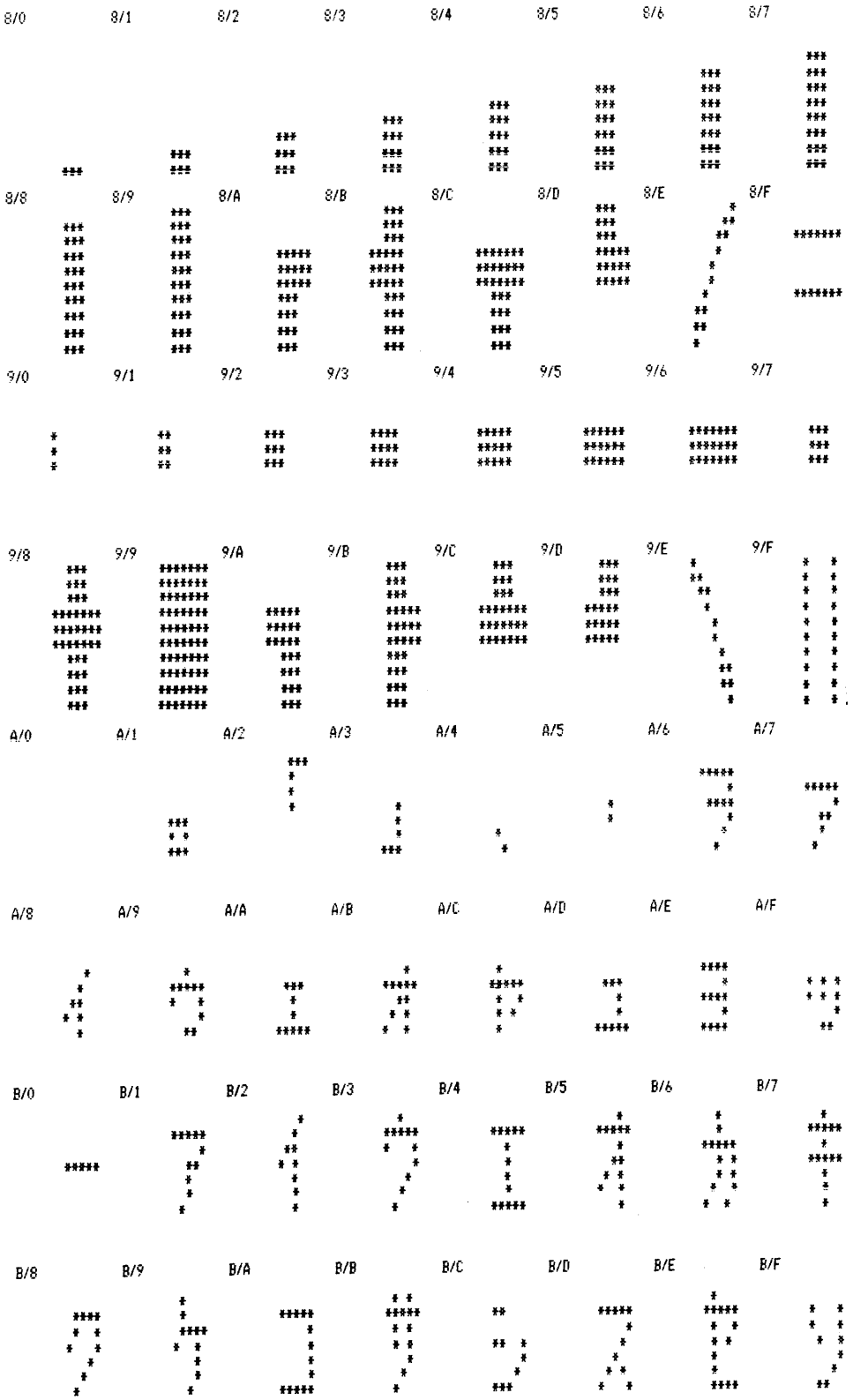


Figure F-9. Additional 128 Eight-Bit Characters Included in the Japanese Katakana Displayed Character Set (Sheet 1 of 2)

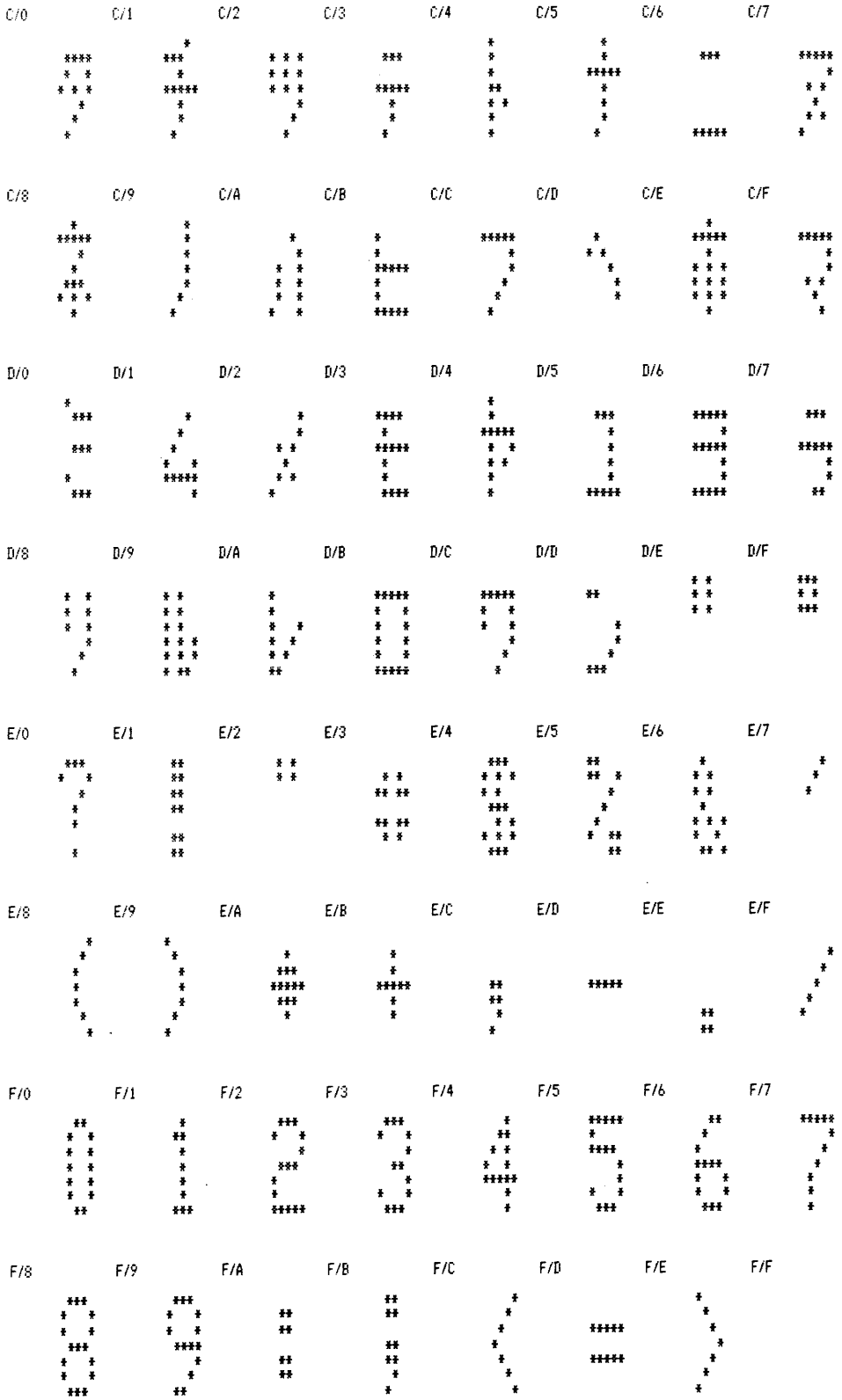


Figure F-9. Additional 128 Eight-Bit Characters Included in the Japanese Katakana Displayed Character Set (Sheet 2 of 2)

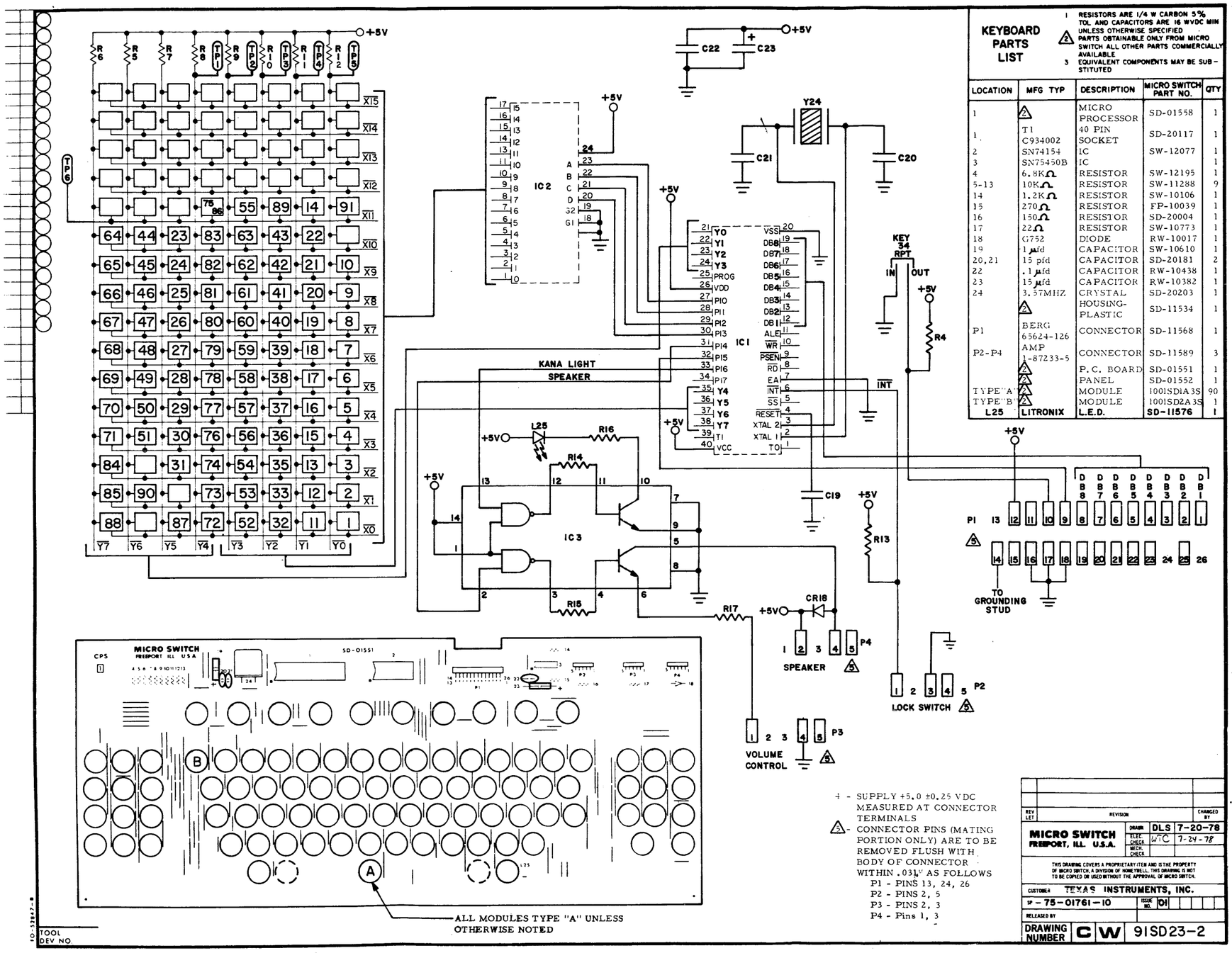


Figure F-10. Japanese Katakana Keyboard Assembly Logic Diagram and Contact Matrix

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

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  Tx-yy

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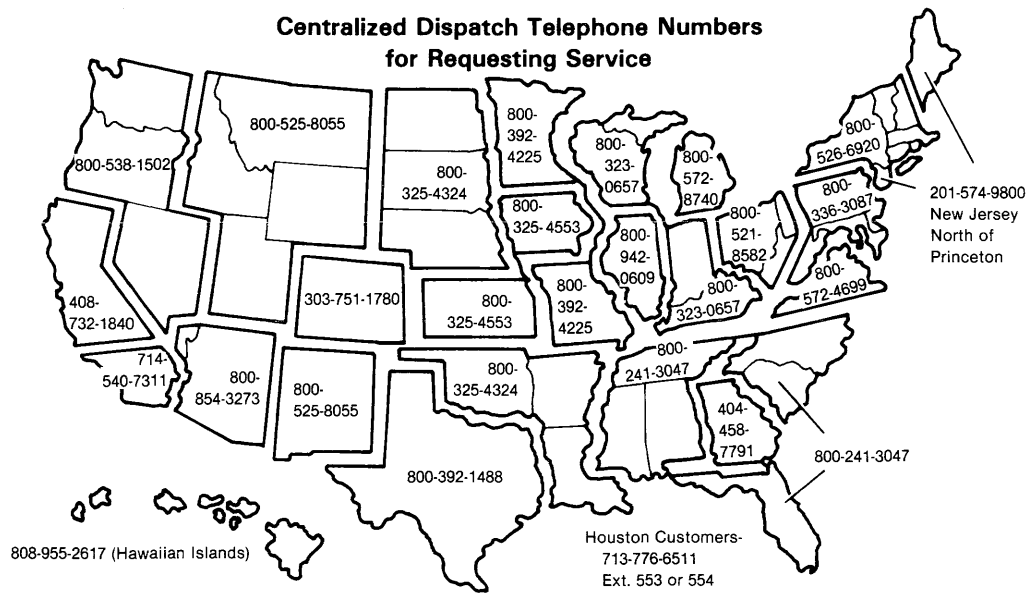

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