1

General Description

1.1 GENERAL

This section contains physical and functional descriptions of the Texas Instruments Two-Channel Asynchronous Interface Module, referred to as the CI402 throughout the remainder of this manual. This section also describes the interface between the CI402 and the host computer communications register unit (CRU), and the interfaces between the CI402 and supported communication devices.

Figure 1-1 is a photograph of the CI402 showing the location of the connectors and components.

1.2 PURPOSE OF EQUIPMENT

The CI402 provides a serial asynchronous interface that allows a Business System 600 or 800 series computer to communicate with two asynchronous modems or other asynchronous devices compatible with the Electronic Industries Association (EIA) standard RS-232C or the Consultative Committee on International Telephone and Telegraph (CCITT) recommendation V.24. The CI402 supports half- or full-duplex communications at speeds from 75 through 19.2K bits per second (bps) on each channel.

Connector P1 provides the interface between the host computer CRU and the CI402. Connectors P2 and P3 provide the following:

- Interfaces and full modem controls for asynchronous modems that are EIA RS-232C or CCITT V.24 compatible
- Interfaces for local peripheral devices such as printers and terminals that conform to RS-232C or CCITT V.24

1.3 PHYSICAL DESCRIPTION

The CI402 is implemented on a half-size printed wiring board (PWB). You must install the CI402 on the connector P1 side of a 990 computer or expansion chassis slot since it uses all 12 CRU address bits from the host. Not all of the address bits are available on the connector P2 side of a 990 computer or expansion chassis slot. The P1 side of the computer or expansion chassis is the left side as viewed from the side that is open for inserting boards into the chassis backpanel.

Bottom-edge connector P1, on the CI402, is an 80-pin male connector that installs into any of the 80-pin female connectors on the P1-side of a 990 chassis. Top-edge connectors P2 and P3 are 18-pin male connectors that mate with interconnecting cables for supported modems and peripheral devices.

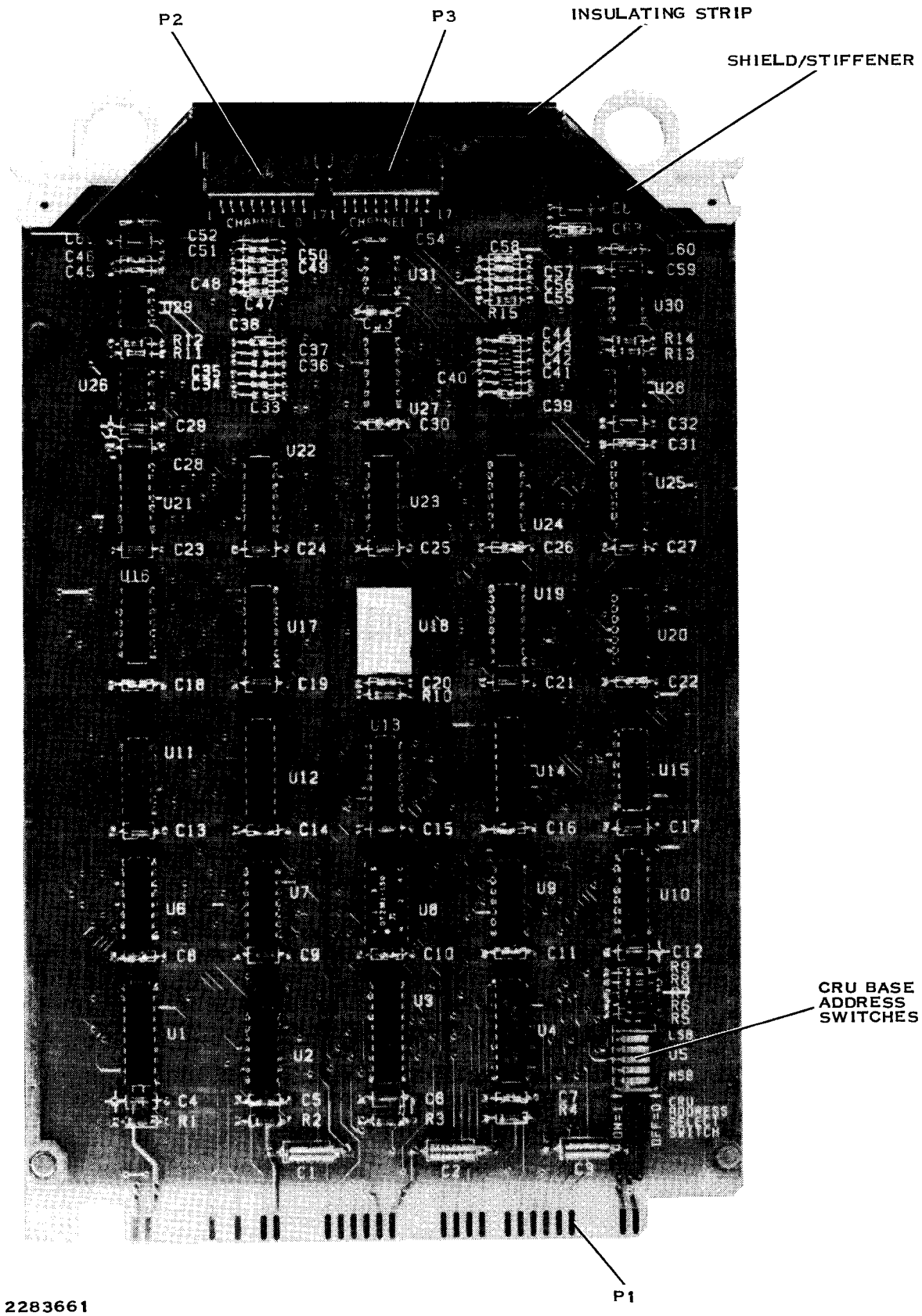

Figure 1-1. Two-Channel Asynchronous Interface Module

The CI402 has extensive electromagnetic interference (EMI) reduction features, including:

- Large power and ground buses in the power distribution matrix
- Extensive bypass capacitors
- Extensive decoupling of grounds
- A metal shield along the top edge of the PWB
- Shielded connectors

The major components of the CI402 are:

- Two MP9214 asynchronous communication controllers
- Two SN74LS251 data selectors
- Two SN74LS259 addressable latches
- Two SN74S373 transparent D-type latches
- One SN74LS682 comparator
- One SN74LS155 decoder
- One five-position dual inline pin (DIP) address-selection switch
- Interface drivers and receivers

1.3.1 CI402 Kits

Table 1-1 lists the components of the CI402 kits, part numbers 2303111-0001 and 2303111-0002.

Table 1-1. CI402 Kits

Kit Part Number	Component Part Number	Item
2303111-0001	2303105-0001	CI402 Two-Channel Asynchronous Interface Module
	2263895-9701	Two-Channel Asynchronous Interface Module (CI402) Installation and Operation Manual
	2303113-9901	CI402 System Test Procedure
	2303110-9901	CI402 Family Tree
	1602045-9701	TMS 9902 Asynchronous Communications Controller

Table 1-1. CI402 Kits (Continued)

Kit Part Number	Component Part Number	Item
2303111-0002	2303105-0001	CI402 Two-Channel Asynchronous Interface Module
	2263895-9701	Two-Channel Asynchronous Interface Module (CI402) Installation and Operation Manual
	2303113-9901	CI402 System Test Procedure
	2303110-9901	CI402 Family Tree
	1602045-9701	TMS 9902 Asynchronous Communications Controller
	2303070-0002	Cable Assembly (CI402 to external modem), 9.1 m (30 ft)

1.3.2 CI402 Cables

The cables described in Table 1-2 are available for use with the CI402.

Table 1-2. CI402 Cables

Part Number	Description
2303070-0002	CI402 to external modem, 9.1 m (30 ft)
2303070-0003	CI402 to external modem, 3.0 m (10 ft)
2303074-0001	CI402 to Model 810 Printer, 9.1 m (30 ft)
2303077-0001	CI402 to EIA terminal*, 9.1 m (30 ft)
2303096-0001	CI402 to TI internal modem, 0.5 m (1.5 ft)

Note:

*This cable mates with terminals and printers that have a 25-pin D-type EIA connector, including models 780, 820, 840, and 940.

1.4 FUNCTIONAL DESCRIPTION

Figure 1-2 is a functional block diagram of the CI402 showing the interface with the host computer on the left and the interfaces to supported communication devices on the right.

Communications between the host computer and the CI402 take place through the CRU of the host computer. The CRU is a bit-serial interface capable of transferring from 1 to 16 bits with the load communications register (LDCR) and store communications register (STCR) instructions. The CRU also provides the capabilities of manipulating single bits with the set bit to zero (SBZ) and set bit to one (SBO) instructions or of testing single bits with the test bit (TB) instruction.

The host computer writes transmit data and control information to the CI402 and reads received data and status information from it. The CI402 can generate interrupts when it needs interrupt service from the host computer if the host has previously enabled interrupts. If the host has not enabled interrupts, it must poll the CI402 to determine when service is needed.

1.4.1 Write Operation Overview

The host writes transmit data and/or control information to the MP9214s and the LS259 control latches on the CI402. To do this, the host places 12 bits of information on the 12 CRU address lines and generates STORECLK-. The most significant five bits of information contain the CRU base address of the CI402. These five bits are examined by the address comparison logic and if they contain the correct CRU base address for the CI402, the address comparison logic generates a board select signal.

The board select signal allows the control decoding logic on the CI402 to decode the remaining seven bits of information from the host computer. The control decoding logic uses a portion of the remaining seven bits to generate the strobe or enable for the device that the host computer is addressing. The other bits contain the address of the particular CRU bit being written by the host.

The clock delay logic stretches STORECLK- and sends a hold signal to the CRU address/data latch to latch the information from the host long enough to meet the setup time of the MP9214s. The clock delay logic also generates two delayed clock signals, CRUCLK and CRUCLK-, that are used to clock information into the MP9214s and into the control decoding logic.

Information written to the MP9214s includes:

- Programming information for the MP9214
- EIA interface control information
- Data to be transmitted via the communication channels

Information written to the LS259 control latches includes:

- EIA interface control information
- Half-duplex/full-duplex selection
- Interrupt enables
- Communication channel enables

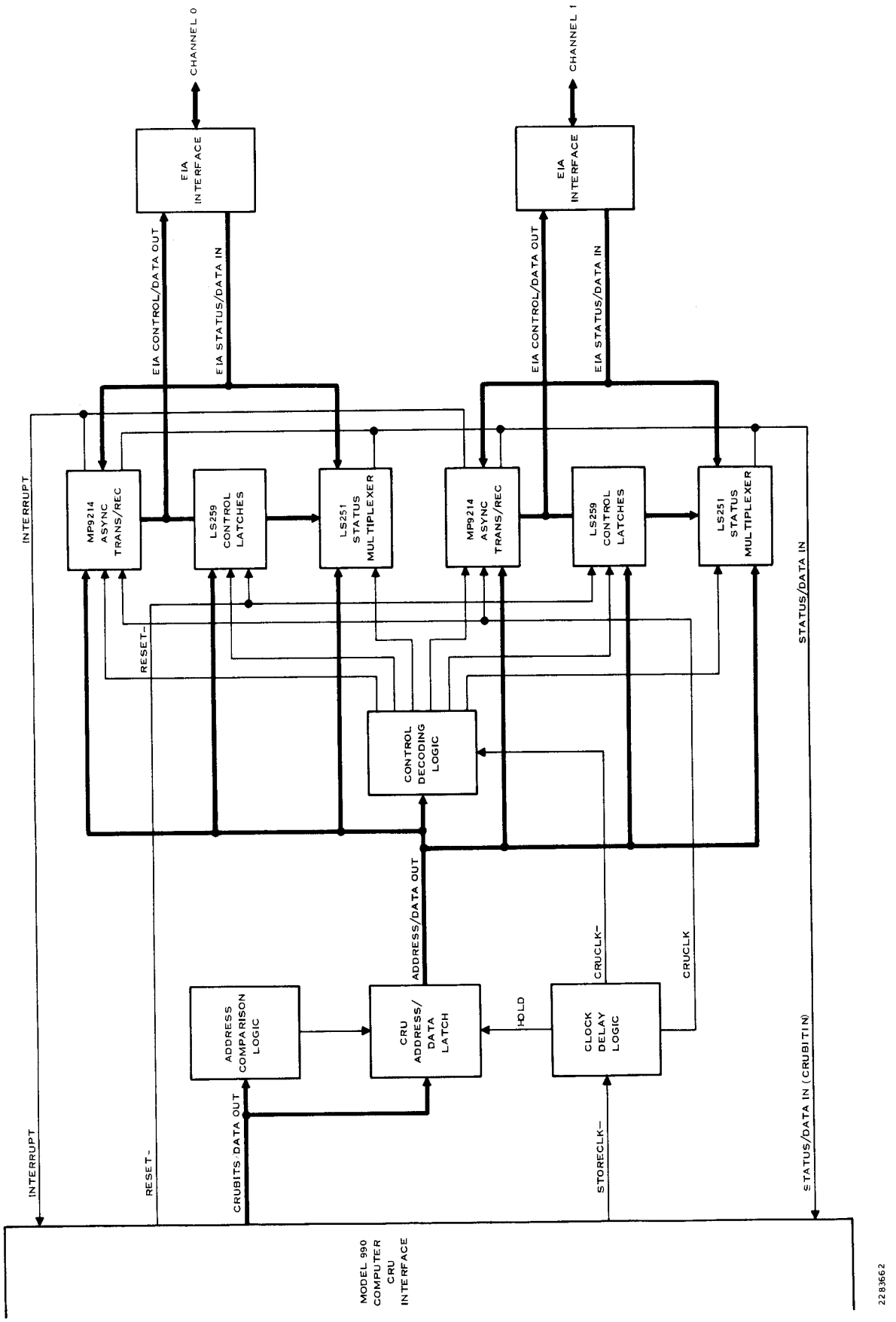

Figure 1-2. CI402 Functional Block Diagram

1.4.2 Read Operation Overview

The host computer reads interface and CI402 status information from the LS251 status multiplexers and MP9214 asynchronous communication controllers. Additionally, the host reads data received via the communication channels from the MP9214s.

The host begins read operations by placing 12 bits of information on the CRU address lines. It does not generate STORECLK- for read operations. The address comparison logic checks the most significant five bits for the correct CRU base address of the CI402 and if they contain the correct address, issues the board select signal that allows the other seven bits of information from the host computer to be decoded and used.

The remaining CRU bits are used to select the particular multiplexer bit or MP9214 location to be read by the host. Information from the addressed bit or location is enabled onto the CRU input line where it is read by the host computer.

1.5 CI402 INTERFACES

The left side of Figure 1-3 shows the signals that comprise the interface between the host computer CRU and the CI402. The right side of Figure 1-3 shows the interface signals between the CI402 and supported modems or other EIA RS-232C or CCITT V.24 compatible devices. The following paragraphs provide details of these interfaces and define the use of the signals.

1.5.1 CI402 to Host Computer Interface

The CI402 board is installed in the host computer chassis or in a CRU expansion chassis where it obtains power and shares access to the host computer CRU with other CRU-controlled devices. Instructions for installing the CI402 in the host computer or expansion chassis and configuring the interrupts and address switches are included in Section 2. The CI402/host computer CRU interface conforms to the requirements of the *990 Computer Family CRU Specification*, part number 945105. Table 1-3 lists the connector pin assignments and the functions of the CI402/host computer CRU interface signals.

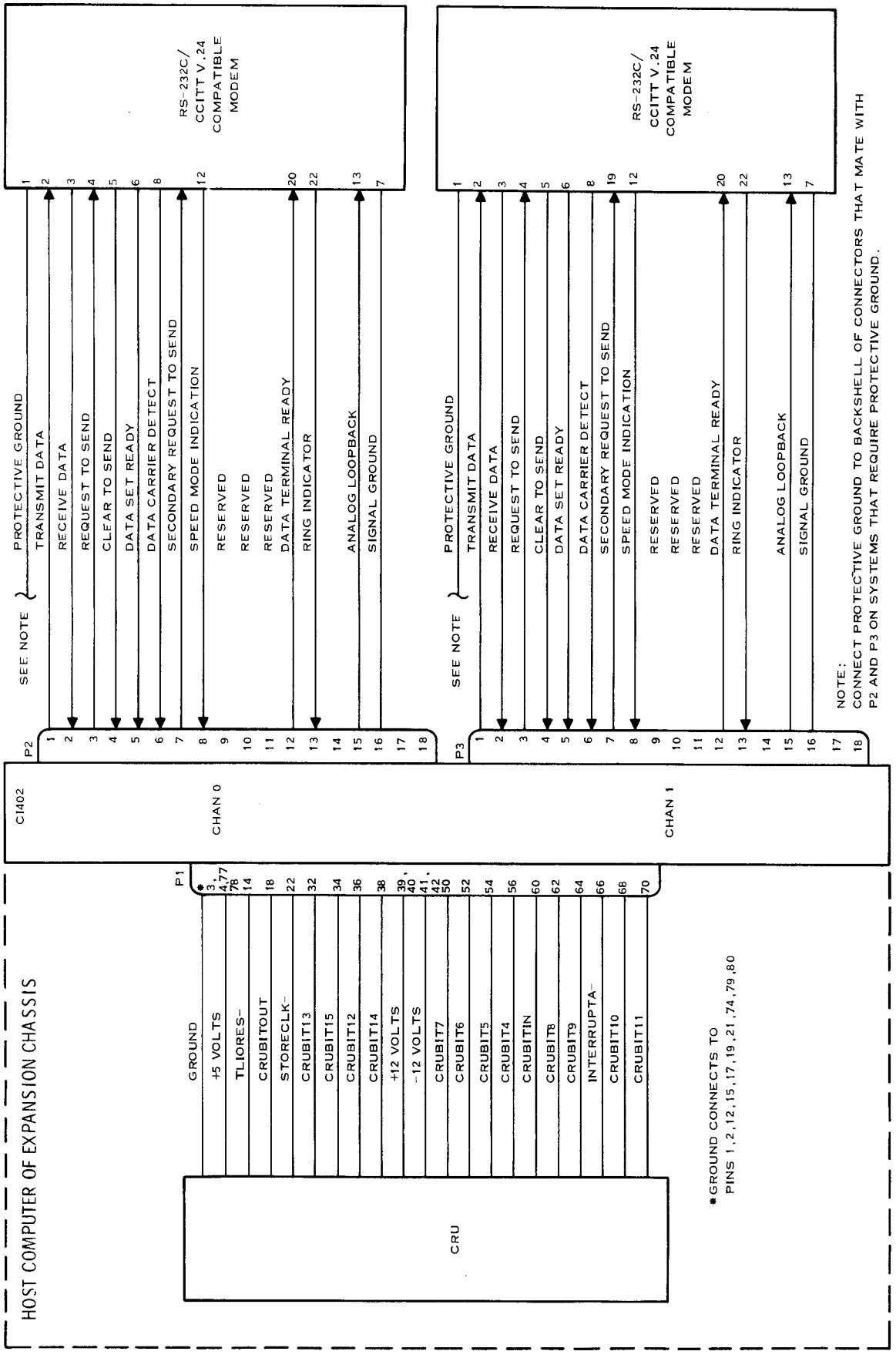

Figure 1-3. CI402 Interface Signals

Table 1-3. CI402/Host Computer CRU Interface Signals

Signature	P1 Pin Number	Function
CRUBIT 4	56	
CRUBIT 5	54	The host computer uses these five bits to select the CRU base address of the CI402.
CRUBIT 6	52	
CRUBIT 7	50	
CRUBIT 8	62	
CRUBIT 9	64	
CRUBIT 10	68	
CRUBIT 11	70	The host computer uses these seven bits to control the CI402 after the CRU base address is selected by bits 4 through 8.
CRUBIT 12	36	
CRUBIT 13	32	
CRUBIT 14	38	
CRUBIT 15	34	
STORECLK-	22	This signal indicates that the host is performing a write operation. It clocks data into the device addressed by the host.
CRUBITOUT	18	The host computer transfers serial data to the CI402 via this line.
CRUBITIN	60	The host computer reads serial data from the CI402 via this line.
INTERRUPTA-	66	The CI402 requests interrupt service by setting this signal to its true (low) state if the host computer has enabled interrupts.
TLIORES-	14	The host computer resets the LS259 control latches on the CI402 with this signal.

1.5.2 CI402 to Communication Device Interface

Connectors P2 and P3 provide the EIA RS-232C/CCITT V.24 interface between the CI402 and compatible communication devices or peripheral devices. The interface signals at connectors P2 and P3 have the following characteristics:

- The receiver circuitry can withstand ± 25 volts.
- The drivers are limited to ± 6 volts.
- A positive voltage greater than + 3 volts equals binary zero, signal space, or control on.
- A voltage more negative than -3 volts equals binary one, signal mark, or control off.

Table 1-4 lists the connector pin assignments and the functions of the signals at CI402 connectors P2 and P3. Table 1-4 also lists pin assignments for data circuit terminating equipment (DCE), such as modems, that conform to EIA standard RS-232C or CCITT recommendation V.24. The EIA and CCITT designations for equivalent circuit functions are listed beside each pin where an equivalent function exists.

Table 1-4. EIA Interface Connector (P2 and P3) Pin Assignments

P2 or P3 Pin Number	DCE Pin Number	CCITT	EIA	Function
Backshell	1	101.0	AA	Protective Ground
1	2	103.0	BA	Transmit Data
2	3	104.0	BB	Receive Data
3	4	105.0	CA	Request To Send
4	5	106.0	CB	Clear To Send
5	6	107.0	CC	Data Set Ready
16	7	102.0	AB	Signal Ground
6	8	109.0	CF	Data Carrier Detect
N/C	9			Reserved
N/C	10			Reserved
N/C	11			Reserved
8	12	122.0	CI	Speed Indication
15	13			Analog Loopback
9	14			Reserved
10	15			Reserved
11	17			Reserved
N/C	18			Reserved
7	19	120.0	SCA	Secondary Request To Send
12	20	108.2	CD	Data Terminal Ready
N/C	21			Reserved
13	22	125.0	CE	Ring Indicator
N/C	23			Spare
14	24			Reserved
N/C	25			Reserved
17	N/C			Reserved
18	N/C			Polarization key

Table 1-5 presents detailed descriptions of the interface signals at CI402 connectors P2 and P3. The direction of information flow is indicated where it is applicable. The data terminal equipment (DTE) includes the host computer and the CI402. The DCE is the modem, or if no modem is involved, the peripheral device with which the host computer is communicating.

Table 1-5. EIA Interface Signal Descriptions

Signal Name	P2/P3 Pin Number	Function
Protective Ground	Backshell	Connected to connector backshell on systems that require use of a protective ground.
Transmit Data DTE to DCE	1	The CI402 generates the signals on this circuit and transfers them to the DCE for transmission to the remote data terminal. This circuit is held in the marking condition during intervals between characters and when no data is being transmitted. The following four signals must be in the on condition before data is transmitted: request to send (CA) clear to send (CB) data set ready (CC) data terminal ready (CD)
Receive Data DCE to DTE	2	The DCE generates the signals on this circuit in response to data signals received from the remote terminal. This circuit is held in the marking condition when the signal data carrier detect (CF) is off. On a half-duplex channel, this circuit is held in the marking condition by the controller when circuit request to send (CA) is on and for a brief interval following the on-to-off transition of request to send (CA).
Request To Send DTE to DCE	3	This circuit conditions the DCE for data transmission. On a half-duplex circuit, it controls the direction of data transmission. A transition from off to on instructs the DCE to enter the transmit mode. The DCE responds by turning on the transmitter and transmitting a mark condition for a preset interval. Then, it turns on the clear to send (CB) signal, indicating that data can be transferred to the DCE on the transmit data (BA) circuit. The on-to-off transition of this circuit instructs the DCE to complete transmission and turn the transmitter off. An asynchronous modem with soft carrier turnoff selected transmits an out-of-band tone (900 Hz for a 202 modem) for a preset time interval and then turns the transmitter off.
Clear to Send DCE to DTE	4	The on condition of this circuit indicates that the DCE is ready to transmit data received on the transmit data (BA) circuit. The on-to-off and off-to-on transitions of this circuit are in response to transitions on circuit request to send (CA).

Table 1-5. EIA Interface Signal Descriptions (Continued)

Signal Name	P2/P3 Pin Number	Function
Data Set Ready DCE to DTE	5	The on condition of this circuit informs the CI402 that the DCE is connected to a data channel and all control circuits are valid. The on condition of this circuit indicates that the following conditions exist: • The local modem is connected to a data channel (off hook in switched service). • The local modem is not in talk or dial mode. • The local modem has completed any timing functions required by the switched system to complete call establishment. This circuit is in the off condition at all other times, indicating to the CI402 that all signals other than ring indicator (CE) should be disregarded.
Data Carrier Detect DCE to DTE	6	The on condition of this circuit indicates that the DCE is receiving a signal that meets its suitability criteria and that receive data (BB) is valid. The off condition indicates that the DCE is not receiving a signal from the remote terminal or the received signal is not suitable for demodulation. On half-duplex channels, this signal is held in the off condition whenever request to send (CA) is on and for a brief interval after the on-to-off transition of request to send.
Secondary Request To Send DTE to DCE	7	The on condition of this signal requests the modem to transmit a tone on the secondary channel (also called the reverse channel, supervisory channel, or backward channel). TI internal modems do not provide this feature.
Speed Mode Indication DCE to DTE	8	Dual-speed modems use this signal to indicate which speed is active. The on condition indicates that the modem is in the high-speed mode. This option is not available on TI internal modems.

Table 1-5. EIA Interface Signal Descriptions (Continued)

Signal Name	P2/P3 Pin Number	Function
Data Terminal Ready DTE to DCE	12	Signals on this circuit control switching the DCE to the communication channel. The on condition prepares the DCE to be connected to the communication channel and maintains the connection established by external means, such as manual call origination, manual answering, or automatic call origination. TI internal modems and most external modems automatically answer an incoming call if circuit data terminal ready (CD) is on and a ringing signal is detected. The off condition of circuit data terminal ready (CD) causes the DCE to be disconnected from the communication channel. In switched network applications, after circuit data terminal ready (CD) is turned off, it is not turned on again until circuit data set ready (CC) is turned off by the DCE.
Ring Indicator DCE to DTE	13	The on condition of this circuit indicates reception of a ringing signal on the communication channel. The on condition is approximately coincident with the on segment of the ringing signal.
Analog Loopback DTE to DCE	15	The on condition of this circuit instructs compatible modems to disconnect from the telephone network and connect the transmitter output to the receiver input. On TI internal modems, all interface circuits except data set ready (CC) operate as in normal full-duplex mode. Data set ready is forced off while the modem is in analog loopback. This circuit allows the host computer to exercise the CI402 and the local modem in a local test mode. The off condition of this circuit returns the modem to normal operation.
Signal Ground	16	This signal establishes the signal common reference potential for unbalanced signals between the CI402 and the DCE.
Keying Pin	17	This pin keys an RS-232C cable to CI402 connectors P2 and P3.
Spare	18	Pin 18 is a spare.

2

Installation

2.1 GENERAL

This section describes how to unpack, install, and perform initial checkout of the CI402. It includes power and environmental requirements of the board to aid in planning the installation.

This section also includes illustrations and descriptions of the CI402 in typical applications, including the part numbers of the cables required for each configuration. The last part of this section describes the recommended method of checking the CI402 for proper operation after you have installed it.

2.2 UNPACKING AND INSPECTION

The CI402 is shipped either as a kit (part number 2303111-0001 or 2303111-0002) or as a part of a system where it is already installed in a Business System 600 or 800 series computer. If the CI402 is already installed in a computer, use the unpacking and inspection instructions in the *Model 990A13 Chassis Maintenance Manual, General Description.*

If the CI402 is shipped as a kit, it is shipped in a cardboard container with the board housed in a rigid Styrofoam* container. Unpack the kit and inspect it as follows:

1. Before unpacking the cardboard shipping box, inspect it for evidence of damage such as crumpled corners, tears, water stains, and so forth.

2. Open the cardboard container and remove the Styrofoam packaged circuit board.

3. Carefully remove the CI402 from the Styrofoam container and verify that the part number matches the number listed in Table 1-1.

4. Inspect the board for any loose or damaged components, cracks in the board, or loose material lodged between components that could cause a short circuit.

5. If any optional cables or parts were ordered, verify that their part numbers match those on the shipping list and inspect them carefully for damage.

* Trademark of the Dow Chemical Company.

2.3 PLANNING

The CI420 board requires one half-slot location on the P1 side of a 990 computer chassis or CRU expansion chassis. The CI402 must be installed on the P1 (left) side of the chassis since it uses all 12 CRU address bits from the host and not all of them are available on the P2 side. From this slot on the P1 side of the chassis, the CI402 obtains the power necessary for operation and interfaces with the CRU in the host computer. The power requirements for the board are as follows:

+5 ± 0.15 Vdc	0.500 A
+12 ± 0.36 Vdc	0.060 A
-12 ± 0.72 Vdc	0.065 A

Table 2-1 presents the environmental requirements of the CI402. Verify that the characteristics of the board are compatible with the planned environment.

Table 2-1. CI402 Environmental Requirements

Operating temperature	0° C (32° F) to 65° C (149° F)
Shipping temperature	-40° C (-40° F) to 70° C (158° F)
Humidity (operating)	5 to 85% noncondensing
Humidity (nonoperating)	5 to 95%
Altitude	0 m to +3049 m (0 to +10,000 ft)
Shock (operating)	1g
Shock (shipping)	15g to shipping container
Vibration (operating)	1g 5 to 80 Hz, 0.3g 80 to 500 Hz

2.4 INSTALLATION

The following instructions for installing the CI402 apply when the board is packaged and shipped separately from the host computer.

Before you install the board in the host computer or CRU expansion chassis, you must do the following:

- Select a suitable chassis slot
- Ensure that the interrupt level jumpers are configured to allow communication between the software in the host computer and the CI402
- Set the CI402 CRU base address switches — take care to select an unused CRU base address
- Inform the system software of the CRU base address and interrupt level assigned to the CI402

The following paragraphs explain how to accomplish these tasks.

CAUTION

Always turn off power to the computer when installing or removing any circuit board from the chassis to prevent damage to the computer or to the board.

2.4.1 Selecting a Chassis Slot for the CI402

You can install the CI402 in any available half-slot location on the P1 side of the host computer chassis or in any one of seven possible CRU expansion chassis.

2.4.2 Interrupt Connections

Interrupt connections required to interface peripheral equipment to a Business System computer are usually made before the system is delivered to the customer. These interrupt assignments are coordinated with the software supplied with the system so the software can communicate with and control the peripheral device. If the CI402 is not purchased as part of a system, you must modify the interrupt connections as part of the board installation.

The method of modifying interrupts varies with the chassis in which the CI402 is to be installed. You can install the CI402 in a 6-slot, 13-slot, or 17-slot chassis used with earlier Texas Instruments computer systems or in the new 13-slot 990A13 chassis introduced in 1982 with the Business System 600 and 800 series computer systems. A manual describing how to modify interrupts for installation of boards is shipped with each of the different chassis. The following describes which manual you should use.

- If you are installing the CI402 in a 6-slot or 13-slot chassis, refer to the *Model 990/10 Computer System Hardware Reference Manual*
- If you are installing the CI402 in a 17-slot chassis, refer to the *Model 990/12 Computer Hardware User's Manual*
- If you are installing the CI402 in a 990A13 chassis, refer to the *Model 990A13 Chassis Maintenance Manual, General Description*

You can find the part numbers of the referenced manuals in the Preface.

2.4.3 Setting the CRU Base Address Switches

The CRU base address switches are located in the lower right corner of the component side of the CI402. The five switches control logic levels (0 or 1) that are compared to information in bits 4 through 8 of the 12-bit CRU address word from the host computer as shown in Figure 2-1.

Table 2-2 lists the switch settings for all CRU base addresses within the legal range of >08XX through >1BXX. The contents of bits 9 through 15 of the CRU address word are not used for CRU base address comparison and are represented as Xs in the table.

You can install the CI402 in the host computer chassis or in any of seven possible CRU expansion chassis and assign it any of the CRU base addresses listed in Table 2-2.

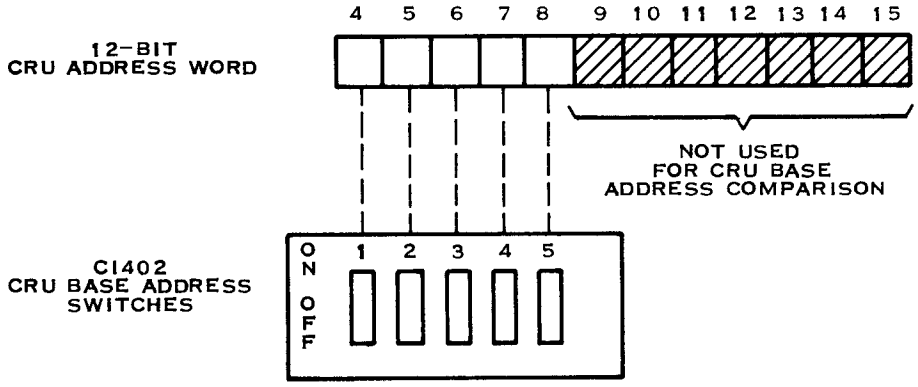

Figure 2-1. CRU Base Address Switches

NOTE

Take care not to assign the CI402 a CRU base address that is already in use by another CRU device. Each CI402 must be assigned a unique address from Table 2-2.

Table 2-2. CRU Base Addresses and Switch Settings

CRU Base Address	Switch Setting 1	2	3	4	5
>08XX	off	on	off	off	off
>09XX	off	on	off	off	on
>0AXX	off	on	off	on	off
>0BXX[1]	off	on	off	on	on
>0CXX	off	on	on	off	off
>0DXX	off	on	on	off	on
>0EXX	off	on	on	on	off
>0FXX[1]	off	on	on	on	on
>10XX	on	off	off	off	off
>11XX	on	off	off	off	on
>12XX	on	off	off	on	off
>13XX[1]	on	off	off	on	on
>14XX	on	off	on	off	off
>15XX	on	off	on	off	on
>16XX	on	off	on	on	off
>17XX[1,2]	on	off	on	on	on
>18XX	on	on	off	off	off
>19XX	on	on	off	off	on
>1AXX	on	on	off	on	off
>1BXX[1]	on	on	off	on	on

Notes:

The Xs represent bits that are used in selection of the CRU base address.

A maximum of 20 CI402 boards can be added to an S800 system. A maximum of 19 can be added to an S600 system.

[1] These addresses are preferred.

[2] This address is not available on S600 systems or on any system that has a 990/10A CPU.

2.4.4 Installing the CI402

After you have selected a chassis slot, modified the interrupts, and set the CRU base address switches on the CI402, you can proceed to install it in the selected slot. If the selected slot does not already have a center card guide installed, you will have to install one before installing the CI402. Information on installing center card guides can be found in the chassis manuals referenced earlier in this section.

CI402 boards and other shielded boards are shipped from the factory with an insulator sleeve installed on the upper lip of the shield-stiffener. If the CI402 is installed in a chassis with conventional (unshielded) boards, leave the insulator in place to protect the board above the CI402 from shorting to the metal shield. When the CI402 is installed with other shielded boards, remove the insulator from the upper lip of the shield by sliding it off as shown in Figure 2-2.

CI402 boards equipped with ejectors of the type shown in Figure 2-3 will not seat properly in some chassis. If you encounter difficulty seating the board, clip the tabs off the ejectors as indicated in Figure 2-3.

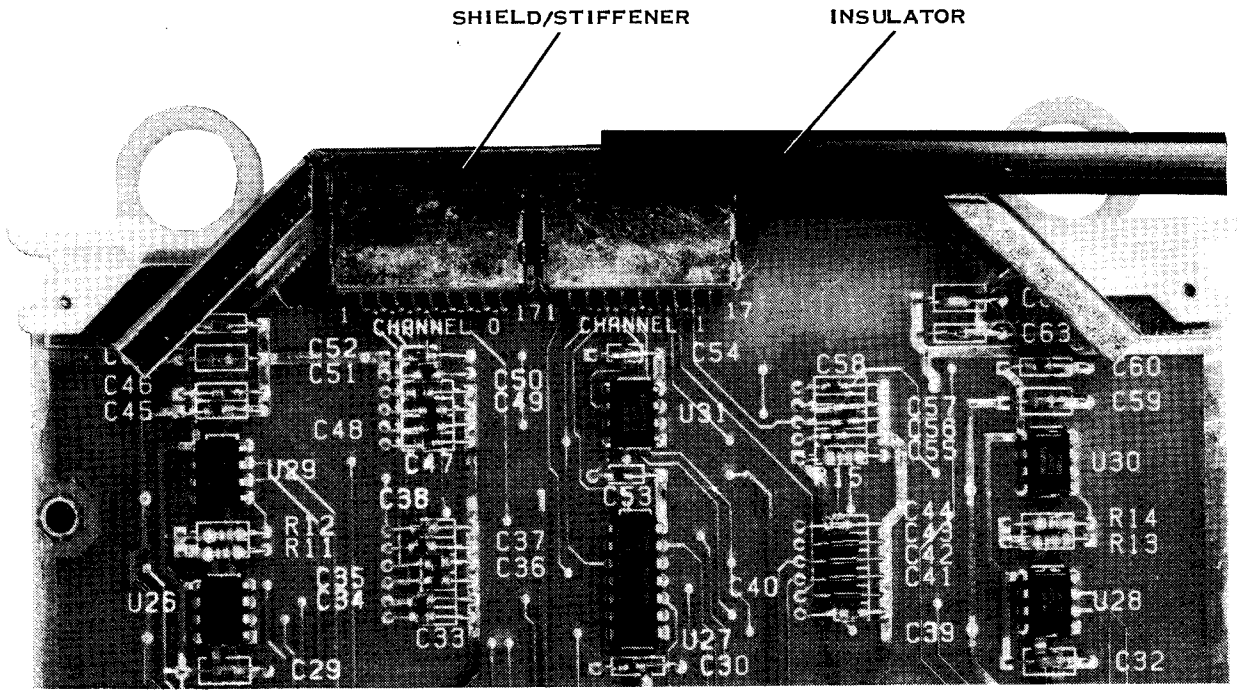

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Figure 2-2. Removing the Insulator from the CI402

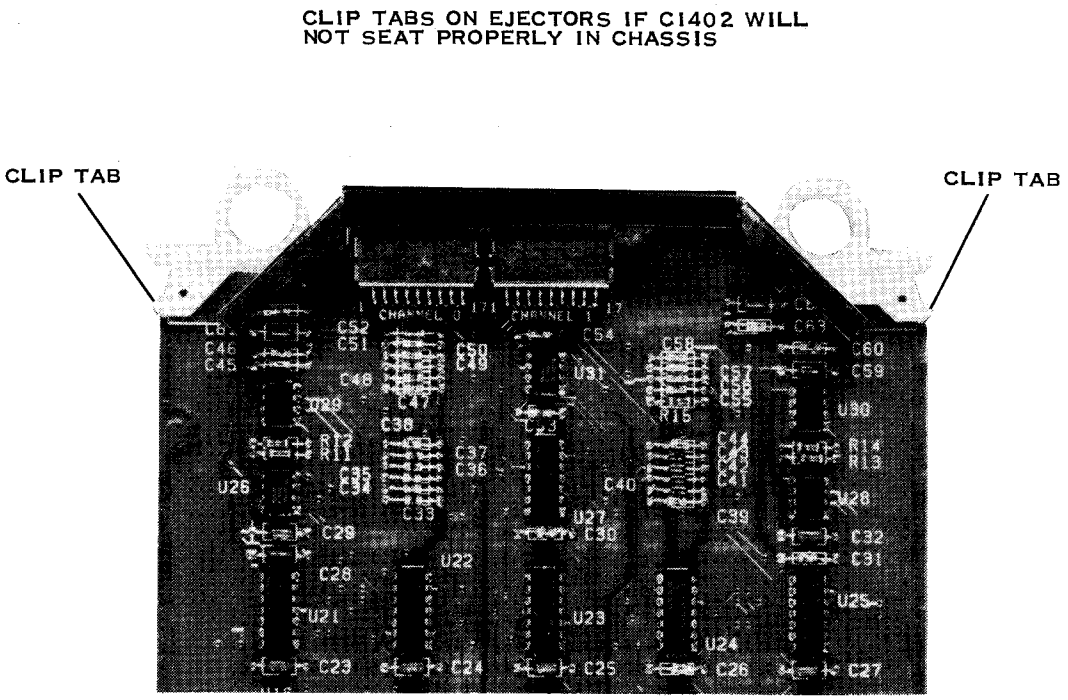

Figure 2-3. Special Installation Problems

2.4.5 Software Considerations

The system software must be informed of the CRU base address and CRU interrupt level assigned to the CI402. This requires the system to be regenerated in most cases. Refer to the software manuals shipped with the system software for information on reconfiguring the system to recognize and communicate with the CI402.

2.4.6 Cable Connections

The cable connections for the CI402 vary with its intended use. Figure 2-4 shows the CI402 in some typical applications, including the part numbers of the interconnecting cables required for each configuration. Use of the CI402 is not limited to the applications shown.

Sheet 1 of Figure 2-4 shows the CI402 being used to support communications on a dial-up network. The system on the left side of sheet 1 of Figure 2-4 shows the CI402 connected to a TI internal asynchronous modem and an automatic calling unit (ACU). This combination provides software-controlled automatic calling and answering but requires use of a data access arrangement (DAA) since the TI internal modem is not Federal Communications Commission (FCC) registered. This system also shows one of the channels of the CI402 being used to interface a Model 810 Printer to the host computer.

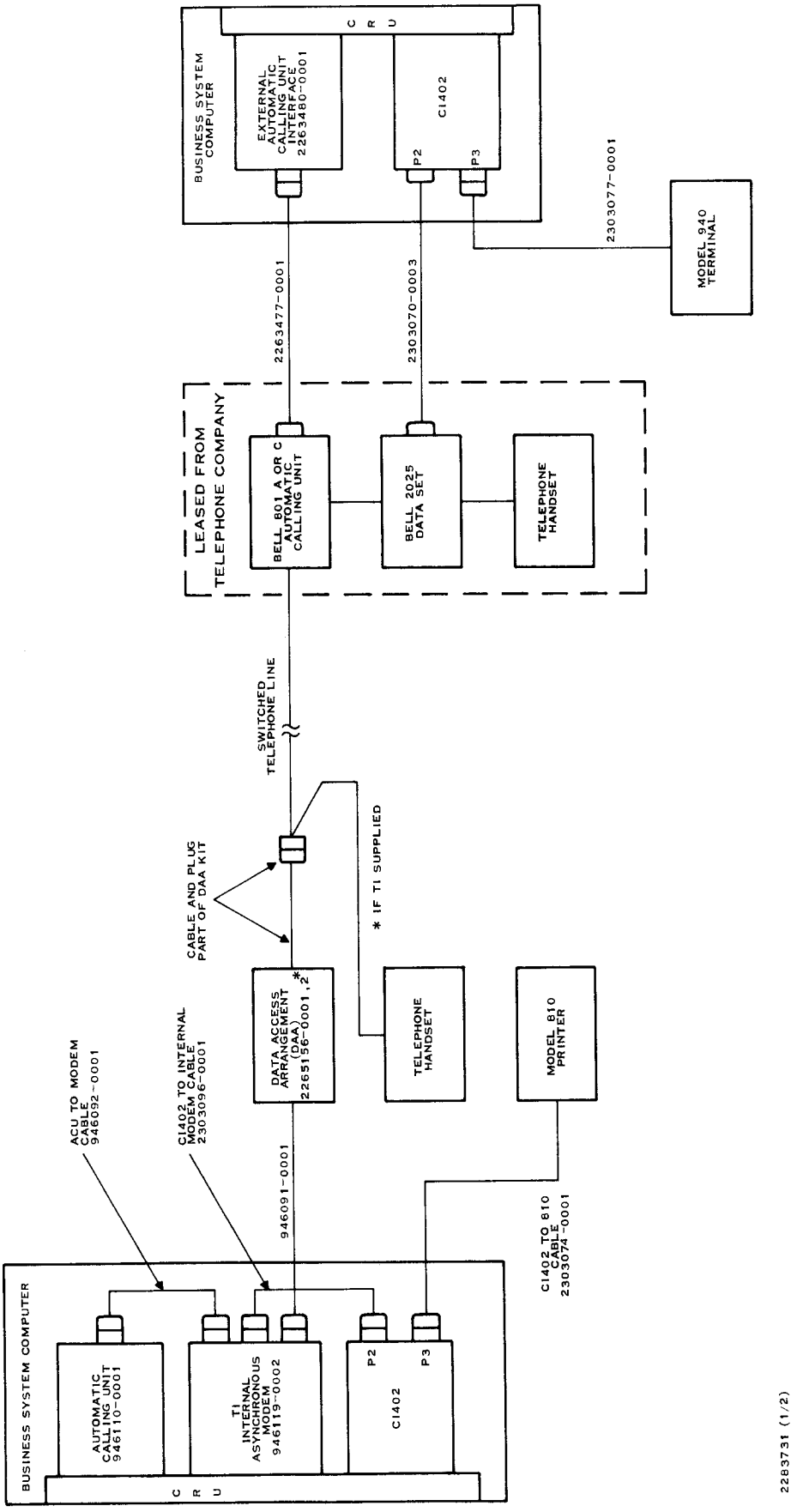

Figure 2-4. Typical Applications of the CI402 (Sheet 1 of 2)

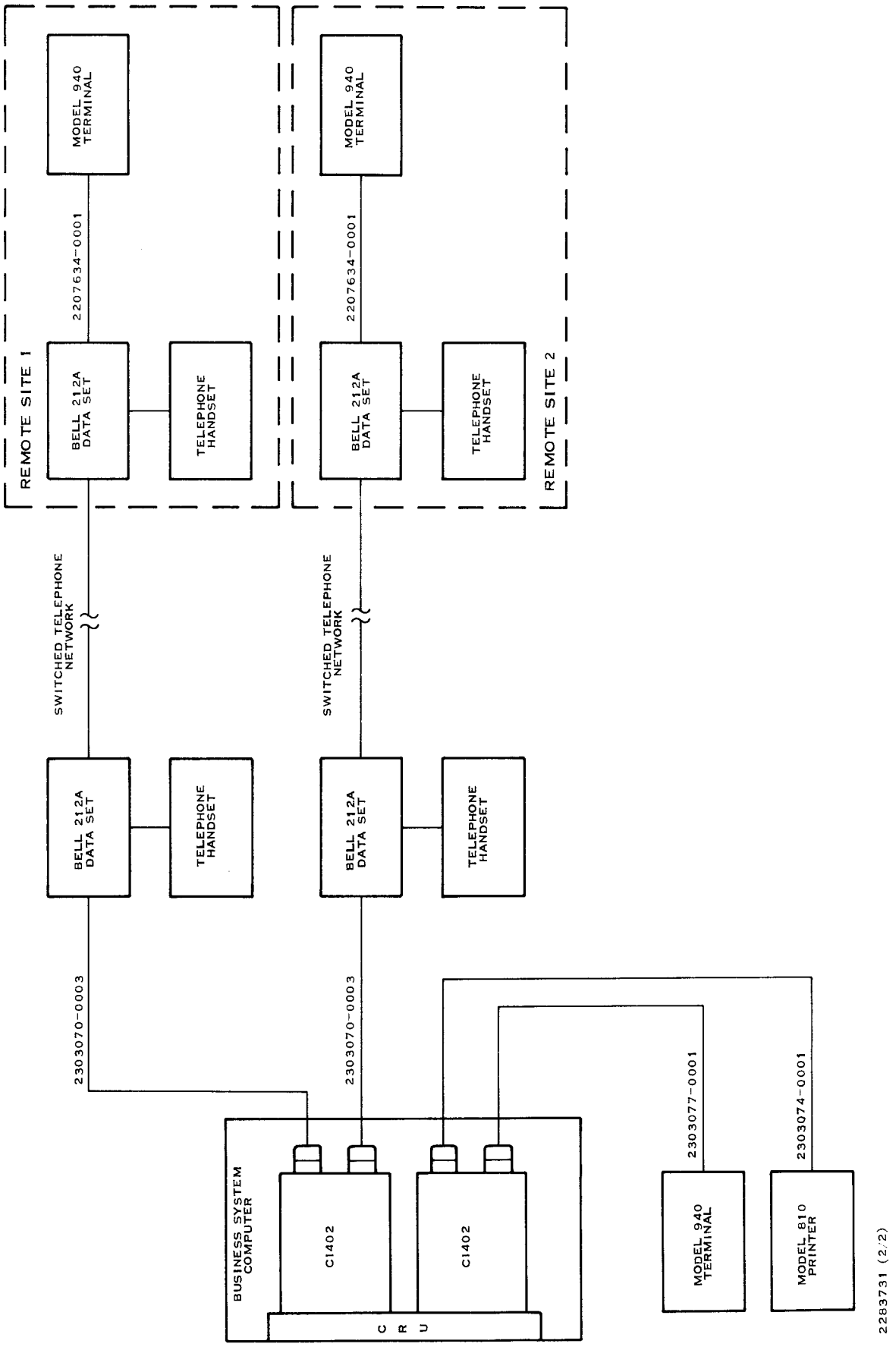

Figure 2-4. Typical Applications of the CI402 (Sheet 2 of 2)

The companion system on the right side of sheet 1 shows the CI402 being used with equipment leased from the telephone company. In this case, an external automatic calling unit interface (EACUI) is used with the Bell 801 ACU to provide software-controlled call dialing and answering. Notice that a DAA is not required since the equipment leased from the telephone company is FCC-registered.

Sheet 2 of Figure 2-4 shows two CI402s being used to provide an interface between the host computer and two dial-up networks plus a local terminal and printer. Each remote site has a Bell data set and a Model 940 Electronic Video Terminal (EVT).

2.4.7 Compatible Modems

The CI402 supports use of the TI internal 202-type asynchronous modem as well as Bell 103, 113, 202, and 212A modems. The CI402 is also compatible with most other manufacturer's asynchronous modems that comply with EIA standard RS-232C.

2.5 CHECKOUT

After you install the CI402 in the host computer or expansion chassis as described in this section, check it for proper operation by loading and executing the CI402 diagnostic, COM90X. The instructions for loading the diagnostic are found in the *Model 990 Computer Unit Diagnostics Handbook, Volume 1*, part number 945400-9701. Volume 6 of the diagnostics handbook (part number 945400-9706) contains a program description of COM90X and explains how to use the tests included in the diagnostic.

The diagnostic consists of a series of tests that thoroughly test the hardware on the CI402, starting with the CRU interface logic and working through the logic for the two communication channels. The diagnostic also includes tests that verify proper operation of the communication line and some of the components of the communication system, depending upon how the system is configured.

After you load and initialize the diagnostic, messages displayed on the CRT guide you through the tests. The CRT displays error messages whenever the tests encounter problems on the board or in the system. The error messages usually indicate the area of the problem or the failing component.

3

Programming

3.1 GENERAL

The CI402 is programmed through the CRU of the host computer with the standard set of CRU instructions. The CI402 occupies 128 bits of host CRU address space; 64 bits for each channel. The MP9214 asynchronous communication controllers occupy the first 32 bits of the 64 bits assigned to each channel.

3.2 CRU ADDRESSING

Table 3-1 lists the CRU addresses of the addressable bits for channels 0 and 1 on the CI402. To address any bit listed, replace the Xs in Table 3-1 with the CRU base address of the CI402. For example, if the CRU base address of the CI402 is >1BXX, you can enable communication channel 0 by writing a 1 (SBO instruction) to >1B4E. You can check to see if channel 0 is enabled by issuing a test bit (TB) instruction to >1B4E.

Table 3-1. CI402 CRU Bit Definitions

CRU Bit (Decimal)	CRU Address (Hexadecimal)	CRU Input	CRU Output
		Channel 0	
0-31	>XX00 - >XX3E	MP9214	MP9214
32	>XX40	Data Carrier Detect	Data Terminal Ready
33	>XX42	Ring Indicator	Analog Loopback
34	>XX44	Speed Indication	Secondary RTS
35	>XX46	Logic 1 = MP9214	Unused[1]
36	>XX48	Logic 0 = 4 MHz	Unused[1]
37	>XX4A	Half Duplex[2]	Half Duplex[2]
38	>XX4C	Interrupt Enable	Interrupt Enable
39	>XX4E	Comm Enable	Comm Enable
40-63	>XX50 - >XX7E	Reserved	Reserved

Table 3-1. CI402 CRU Bit Definitions (Continued)

CRU Bit (Decimal)	CRU Address (Hexadecimal)	CRU Input	CRU Output
		Channel 1	
64-95	>XX80 - >XXBE	MP9214	MP9214
96	>XXC0	Data Carrier Detect	Data Terminal Ready
97	>XXC2	Ring Indicator	Analog Loopback
98	>XXC4	Speed Indication	Secondary RTS
99	>XXC6	Logic 1 = MP9214	Unused[1]
100	>XXC8	Logic 0 = 4 MHz	Unused[1]
101	>XXCA	Half Duplex[2]	Half Duplex[2]
102	>XXCC	Interrupt Enable	Interrupt Enable
103	>XXCE	Comm Enable	Comm Enable
104-127	>XXD0 - >XXFE	Reserved	Reserved

Notes:

XX in the CRU address is replaced by the CRU base address of the CI402.

Refer to the TMS 9902 manual included in the kit for definitions of the individual bits assigned to the MP9214.

All unused bits are held at logic 1 level.

[1] The bits at addresses >XXC6, >XXC8, >XX46, and >XX48 can be checked with the TB instruction but cannot be changed by writing to these addresses.

[2] A logic 0 written to >XX4A or >XXCA sets the full-duplex mode for the particular channel. A logic 1 sets the half-duplex mode. When testing these bits for status, a logic 0 indicates the full-duplex mode has been set; a logic 1 indicates the half-duplex mode.

In Table 3-1, CRU input refers to the host computer reading information from the CI402, such as when a TB instruction is issued to determine the status of a signal. CRU output refers to the host computer writing to the CI402 as in the example just presented where a 1 was written to the communication channel enable bit.

If you are not certain of the CRU base address of the CI402, you can compare the setting of the CRU base address switches to Table 2-2 in Section 2 to determine the CRU base address.

Notice in Table 3-1 that writing to several of the addresses sets or clears one of the interface signals while issuing a TB instruction to the same address checks the status of a different interface signal. For instance, writing to >XX40 sets or clears data terminal ready for channel 0 while issuing a TB instruction to the same address checks the status of the data carrier detect signal for channel 0. The information at addresses >XX46, >XX48, >XXC6, and >XXC8 allows the host computer to read the configuration of the communication controllers on each channel and the clock but the values cannot be changed by writing to these addresses.

3.3 PROGRAMMING THE MP9214s

Most of the programming for the CI402 consists of the instructions required to set up the desired operating parameters of the MP9214 asynchronous communication controllers for channels 0 and 1. The TMS 9902 manual included in the CI402 kit contains detailed information on programming the MP9214s plus examples of code that can be used for most operations. The MP9214s used on the CI402 are specially selected TMS 9902 asynchronous communication controllers. The programming characteristics of the MP9214s are identical to the TMS 9902s.

3.3.1 MP9214 Data Rate Register Settings

The MP9214s are capable of transmitting at one rate and receiving at a different rate since they have separate transmitter and receiver data rate registers. You can set separate transmit and receive baud rates by writing different values to the two data rate registers.

The TMS 9902 manual presents a formula for calculating the hexadecimal values that must be placed in the transmitter and receiver data rate registers to establish the baud rate of the MP9214s. Table 3-2 lists hexadecimal values for commonly-used baud rates to save you the trouble of calculating each one. Only the eleven least significant bits of the 12-bit value are placed in the register; the most significant bit is discarded. For example, to set a baud rate of 75, the hexadecimal value written to the registers is 741, which is a binary value of 0111 0100 0001. The leftmost 0 is discarded and the other 11 bits are written to the register.

Table 3-2. MP9214 Data Rate Register Settings

Baud Rate	Hexadecimal Value	Binary Value
75.0	741	0111 0100 0001
110.0	638	0110 0011 1000
134.5	5D1	0101 1101 0001
150.0	5A1	0101 1010 0001
200.0	539	0101 0011 1001
300.0	4D0	0100 1101 0000
600.0	341	0011 0100 0001
1200.0	1A1	0001 1010 0001
1800.0	116	0001 0001 0110
2400.0	0D0	0000 1101 0000
3600.0	08B	0000 1000 1011
4800.0	068	0000 0110 1000
7200.0	045	0000 0100 0101
9600.0	034	0000 0011 0100
19200.0	01A	0000 0001 1010

3.3.2 MP9214 Control Register

Bit 3 of the control register in the MP9214s must always be set to a 1 for the CI402 to operate properly due to use of the 4-MHz clock.

Alphabetical Index

Introduction

HOW TO USE INDEX

The index, table of contents, list of illustrations, and list of tables are used in conjunction to obtain the location of the desired subject. Once the subject or topic has been located in the index, use the appropriate paragraph number, figure number, or table number to obtain the corresponding page number from the table of contents, list of illustrations, or list of tables.

INDEX ENTRIES

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections — Reference to Sections of the manual appear as "Sections x" with the symbol x representing any numeric quantity.

- Appendixes — Reference to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.

- Paragraphs — Reference to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph may be found.

- Tables — References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number.

  Tx-yy

- Figures — References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number.

  Fx-yy

- Other entries in the Index — References to other entries in the index preceded by the word "See" followed by the referenced entry.