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Model 990 Computer

Communications Interface Module

Depot Maintenance Manual

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PREFACE

This manual provides maintenance instructions for the Texas Instruments Communications Interface Module. The manual also provides theory of operation for the module. The information in this manual is divided into the following sections:

I. Theory of Operation - This section contains a detailed block diagram description of the Communication Interface Module, describes the module's interface with the Model 990 Computer, and provides a discussion of the module's operation.

II. Maintenance - This section provides troubleshooting and fault isolation procedures for the module.

Alphabetical Index - The alphabetical index provides an alphabetical listing of key words and concepts within the manual, and locates them for easy reference.

Additional information related to the Communications Interface Module may be found in the following documents:

Title	Part Number
990 Computer Family Systems Handbook	945250-9701
Model 990/4 Computer System Depot Maintenance Manual	945403-9701
Model 990/10 Computer System Depot Maintenance Manual	945404-9701
Model 990 Computer Family Maintenance Drawings	945421-9702
Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide	943441-9701
Model 990 Computer Communication System Installation and Operation	945409-9701

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SECTION I

THEORY OF OPERATION

1.1 GENERAL

This section provides a description of the functional operation of the Communications Interface Module. The description is supported by block diagrams, circuit diagrams, logic diagrams, flowcharts and timing diagrams. Detailed discussions of the circuits on the module and, finally, descriptions of the signals making up the interfaces between the module and a Model 990 Computer and a modem are also provided.

A general description of the Communications Interface Module is given in *Model 990 Computer Communication System Installation and Operation.* A complete logic diagram is in *Model 990 Computer Family Maintenance Drawings Volume II - Peripherals.*

Figure 1-1 shows the Communications Interface Module. Figure 1-2 is a functional block diagram of the module. The discussions in this section are based on figure 1-2.

1.2 OUTPUT AND INPUT WORDS

All communications interface module read and write operations are controlled by five output words and 5 input words. All write operations to the UC1671B are performed by addressing the desired output word, loading (LDCR) the desired contents of an output word onto the CRU interface, and issuing an SBO or SBZ to STROBE (except for output word 4). All read operations to the UC1671B are performed by addressing the input word, issuing an SBO instruction to STROBE (in the case of a UC1671B read) to load the contents of the word onto the CRU interface, and reading (STCR) the word or a bit (TB) of the word.

1.2.1 OUTPUT WORDS. Figure 1-3 illustrates the contents of the output words, and the following paragraphs describe the functions of those contents.

1.2.1.1 Output Word 0. Output word 0 is the only 16-bit output word. Its least significant eight bits are loaded onto the device access line (DAL) bus when the address (ADD,0-2,Q = 000) and strobe (STROBE=0) are loaded into the most significant eight bits.

Write Data (XDATA,0-7), bits 0-7 – the next data character to be written into the UC1671B transmitter holding register. XDATA0 is the least significant bit (LSB), and XDATA7 is the most significant bit (MSB) of the write data word. All write data words are LSB-justified with 0-fill.

Input/Output Word Address (ADD,0-2,Q), bits 8-10 – combined with STROBE, address each input or output word to direct the writing to output words and the reading of input words to and from the UC1671B. ADD,0-2,Q return to the 000 following each UC1671B read or write operation.

Strobe (STROBE), bit 11 – combined with ADD,0-2,Q directs the writing to output words and the reading of input words according to table 1-1.

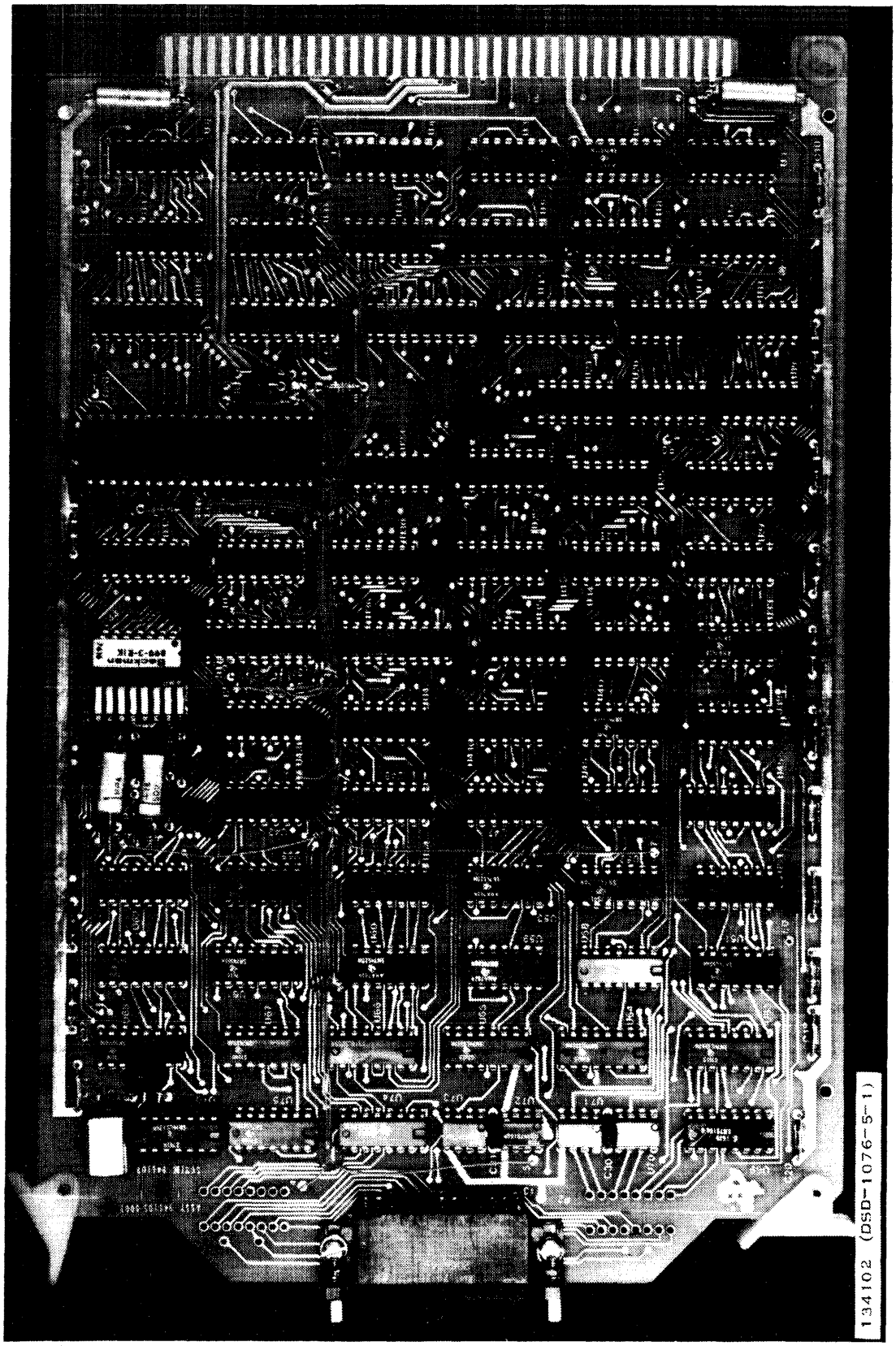

Figure 1-1. Communications Interface Module

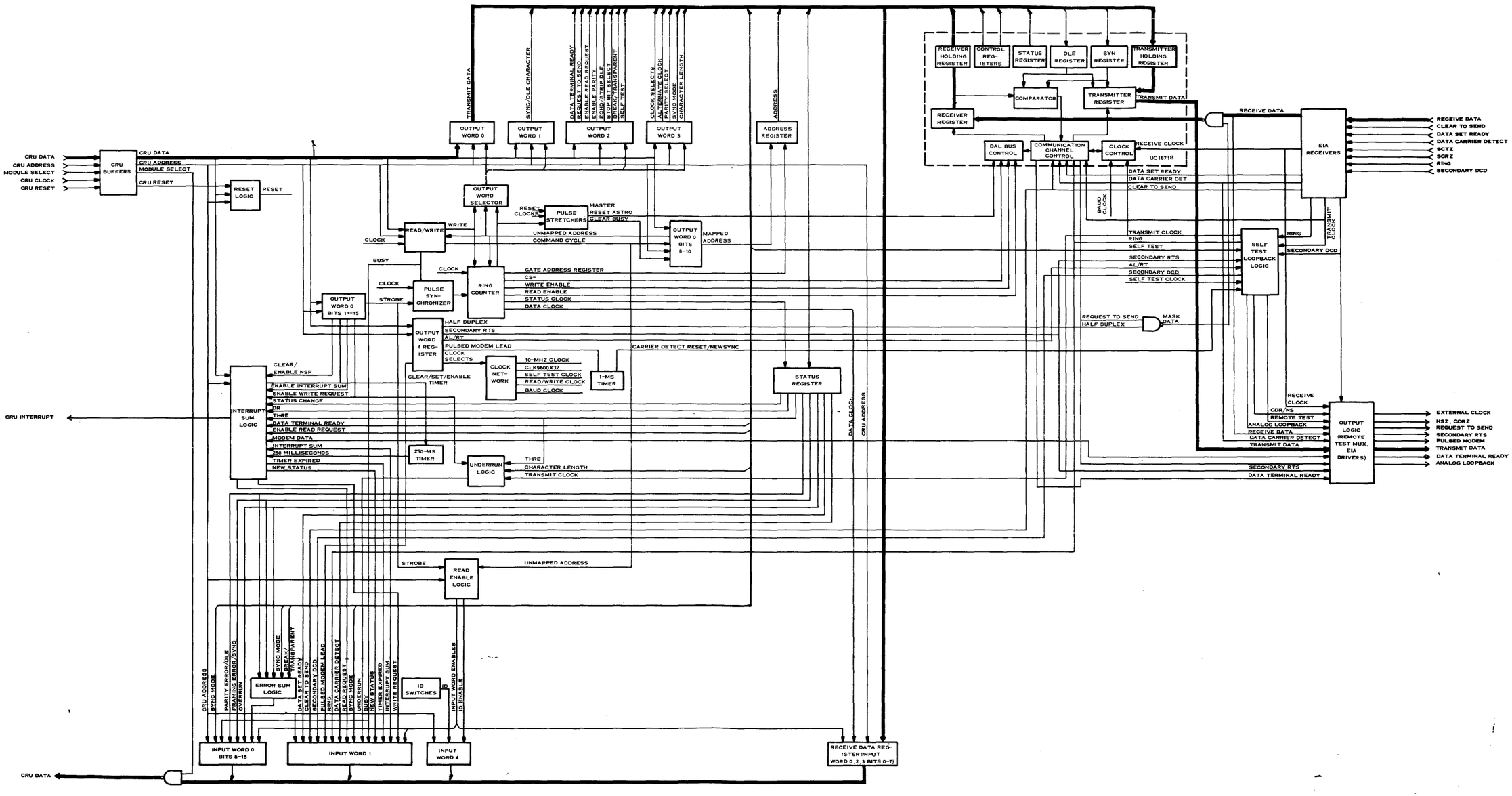

Figure 1-2. Communications Interface Module Functional Block Diagram

	OUTPUT WORD				
BIT	0	1	2	3	4
0	XDATA0	SYNC/DLE0	DTR	CLKSELA0	CLKSELB0
1	1	1	RTS	CLKSELA1	CLKSELB1
2	2	2	ENRRQ	CLKSELA2	SRTS
3	3	3	ENPARITY	ATCK/STPSYN	RESMDMO0
4	4	4	ECHO/STPDLE	PARITYSEL	RESMDMO1
5	5	5	SBS/XMITPAR	SYNCMODE	MR
6	6	6	BREAK/XPRNT	CHARLEN0	HALFDPLX
7	XDATA7	SYNC/DLE7	SELFTST	CHARLEN1	AL/RT
8	ADD0Q				
9	ADD1Q				
10	ADD2Q				
11	STROBE				
12	CLRENNSF				
13	CLRSETENTIM				
14	ENINTR				
15	ENWRQ				

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Figure 1-3. Output Word Contents

Table 1-1. ADD,0-2,Q/STROBE Addressing Scheme

ADD,0-2,Q	STROBE	Input or Output Word Addressed
210		
000	0	Output word 0 (Write data)
	1	Input word 1 (Read data, errors)
001	0	Output word 2
	1	Input word 2
010	1	Output word 1 (SYNC/DLE character)
100	0	Output word 3
	1	Input word 3
101	0	Output word 4 (Auxiliary register)
110	0	Input word 4 (Module ID)
011	1	Forces status scan cycle

Clear-Enable New Status Flag (CLRENNSF), bit 12 – enable setting the new status flag (NSFQ–). When set high, CLRENNSF resets the new status flag (input word 1, bit 12) (if set), and enables the new status flag to be set upon the occurrence of a new modem status condition. When low, CLRENNSF resets the new status flag (NSFQ–) (if set) and disables setting of the new status flag by a new modem condition.

Clear-Set-Enable Timer (CLRSETENTIM), bit 13 – controls the 250-millisecond timer. When CLRESETENTIM is set to logic 1, the timer expired flip-flop is cleared (if set) and a 250-millisecond timeout interval is initiated by the 250-millisecond timer and the timer expired flip-flop is enabled. At the end of the 250-millisecond interval, CLRSETENTIM = 1 allows the timer expired flip-flop to set bit 13 of input word 1 and produce an interrupt, INTRSUM, for the computer. When set to 0, CLRSETENTIM clears the timer expired flip-flop (if set) and disables setting of the timer expired flip-flop.

Enable Interrupt (ENINT), bit 14 – enables module interrupts (INTRSUM) to the CRU interface (INTERRUPTA–). If ENINT is not set, no interrupt can be received by the computer.

Enable Write Request (ENWRQ), bit 15 – enables setting of input word 1, bit 15 and write request interrupt. When set to 0, ENWRQ clears the underrun flip-flop (UNDERRUNQ).

1.2.1.2 **Output Word 1** Output word 1 contains the SYNC or DLE character to be loaded into the UC1671B SYNC/DLE register in the synchronous mode. It is loaded onto the DAL bus when ADD,0-2,Q = 010 and STROBE = 1.

The initial write to address 010_2 (ADD,0-2,Q) loads the SYNC character register in the UC1671B. If a DLE character is also to be loaded, it must be written by the next command cycle to the UC1671B with ADD,0-2,Q again equal 010_2. If only a SYNC character is to be loaded, ADD, 0-2, Q must not be set to 010_2 for the next cycle (This is the normal case, since ADD,0-2,Q are automatically reset to 000_2 at the end of the first SYNC cycle.) A DLE character load must be preceded by a SYNC character load.

1.2.1.3 **Output Word 2.** Output word 2 contains control signals. ADD,0-2,Q = 100 and STROBE = 0 loads it onto the DAL bus.

Data Terminal Ready (DTR), bit 0 – drives (through the UC1671B) the CD modem output (DTRZ) and enables changes in Data Set Ready (DSR), Data Carrier Detect (DCD), and Secondary Data Carrier Detect (SDCD) to be flagged by the new status flag.

Request to Send (RTS), bit 1 – controls the CA modem output (RTSZ). When RTS and Clear To Send (CTS) are both high, the transmitter portion of the UC1671B is enabled. If RTS goes low during a character transmission, the character in the UC1671B transmitter register will be completely transmitted before the transmission is terminated and before RTS to the modem is reset.

Enable Read Request (ENRRQ), bit 2 – enables setting of input word 1, bit 8 and enables UC1671B receiver section. When ENRRQ is low, bits 12 through 15 of input word 0 and bit 8 of input word 1 are reset. Toggling ENRRQ from high to low to high resynchronizes the UC1671B receiver section (synchronous mode).

Parity Enable (ENPARITY), bit 3 – enables parity checking and generation by the module (asynchronous mode) or parity checking only (synchronous mode). When ENPARITY is high, Odd Parity (output word 3, bit 4) selects odd or even parity. If the Character Length bits (bits 6 and 7 of output word 3) specify 8-bit characters, the parity bit replaces the MSB of the character.

Echo/DLE Strip (ECHO/STPDLE), bit 4 – enables the presentation of assembled received characters directly to the transmitted data (SDZ) output in place of data from the UC1671B transmitter holding register. The UC1671B receiver must be enabled by setting output word 2, bit 2 (ENRRQ = 1). Echo will not start until the transmitter is idle.

In the synchronous mode ECHO/STPDLE inhibits the transfer to the UC1671B receiver holding register of assembled receiver register data that matches the contents of the UC1671B DLE register. Parity checking is also disabled.

Stop Bit Select/SYNC Transmit Parity Enable/Force DLE (SBS/XMITPAR/FORCEDLE), bit 5 – causes 1 stop bit to be transmitted at the end of each character in the asynchronous mode. SBS/XMITPAR/FORCEDLE = 0 causes transmission of 1.5 stop bits per 5-bit character and two stop bits per 6-, 7-, or 8-bit character.

In the synchronous mode, SBS/XMITPAR/FORCEDLE = 1 with output word 2, bit 6 = 0 enables transmit parity. If both SBS/XMITPAR/FORCEDLE and output word 2, bit 6 are logic 1, a DLE character is transmitted prior to transmitting the character in the UC1671B transmitter holding register.

Break/Transparent (BREAK/XPRNT), bit 6 – starting at the end of any character currently being transmitted, holds the transmitted data (SDZ) output in a spacing condition when the transmitter is enabled in the asynchronous mode. Normal transmitter timing is not interrupted.

In the synchronous mode, BREAK/XPRNT conditions the UC1671B transmitter for transparent transmission. A DLE-SYNC character sequence comprises the idle fill, and a DLE character may be force-transmitted ahead of any character by setting SBS/XMITPAR/FORCEDLE = 1.

Self-Test (SELFTEST), bit 7 – places the module in the digital loopback mode (see tables 1-3 and 1-4).

1.2.1.4 **Output Word 3.** Output word 3 should be written to the UC1671B by ADD,0-2,Q = 001 and STROBE = 0 only while both the transmitter and receiver are idle. Otherwise, any other character being transmitted or received will be questionable. The contents of output word 3 are as follow:

Clock Select A0 - A2 (CLKSELA,0-2), bits 0-2 – select the transmit and receive baud rates as shown in table 1-2.

Alternate Clock/Strip SYNC (ATCK/STPSYN), bit 3 – In the asynchronous mode, ATCK/STPSYN selects the same clock for both transmit and receive functions and should be set high to avoid selection of no (0 bit/second) receive clock. ATCK/STPSYN causes SYNC characters to be deleted from the received data in synchronous mode.

Odd Parity Select (PARITYSEL), bit 4 – selects even (PARITYSEL = 0) or odd (PARITYSEL = 1) parity when parity is enabled (ENPARITY).

Synchronous Mode Select (SYNCMODE), bit 5 – selects synchronous (SYNCMODE = 1) or asynchronous (SYNCMODE = 0) mode of operation, including synchronous versus asynchronous data formatting.

Table 1-2. Baud Rate Selection

Clock Selection Code CLKSEL				Nonimal Baud Rate
B1	B0	A1	A0	
0	0	0	0	200
0	0	0	1	100
0	0	1	0	50
0	0	1	1	25
0	1	0	0	600
0	1	0	1	300
0	1	1	0	150
0	1	1	1	75
1	0	0	0	880
1	0	0	1	440
1	0	1	0	220
1	0	1	1	110
1	1	0	0	9600
1	1	0	1	4800
1	1	1	0	2400
1	1	1	1	1200

Character Length Select (CHARLEN,0,1), bits 6,7 – select character length for communication as follows:

CHARLEN,0,1	Character Length
01	(bits)
00	8
01	7
10	6
11	5

NOTE

Character length refers to the number of bits in the data, plus parity. If parity is disabled, character length equals the number of data bits. If parity is enabled, character length equals the number of data bits plus one except for 8-bit characters for which character length is always 8.

1.2.1.5 **Output Word 4** Output word 4 is written by ADD,0-2,Q = 101. No STROBE reference is necessary since output word 4 is not written to the UC1671B. Add,0-2,Q are not automatically reset to 000_2. The contents of output word 4 are as follow:

Clock Select B0, B1 (CLKSELB,0,1), bits 0, 1 – select, with CLKSELA,0,1, one of 16 baud rates to be used as transmit and receive clocks when a 32X clock is selected (CLKSELA2 = 1). Table 1-2 lists the baud rates for the various combinations of CLKSELA,0,1 and CLKSELB,0,1.

Secondary Request to Send (SRTS), bit 2 – directly drives the Secondary Request to Send (SRTSZ) output to the modem. SRTS is used in most applications to establish circuit assurance.

Reserved Modem Lead Output (RESMDMO0), bit 3 – directly drives the Reserved Modem output (RSVZ). This signal is reserved for use with the customers external modem and enables (RESMDMO0 = 1) the audio monitor on the Texas Instruments synchronous or asynchronous modems.

Pulsed Modem Lead (RESMDMO1), bit 4 – initiates a 1-millisecond pulse to the modem (NSZ and CDRZ).

Master Reset (MR), bit 5 – clears all status and control (except input modem leads) the reset (inactive) state. MR is a pulse and is automatically returned to the reset state by the module.

Half-Duplex (HALFDPLX), bit 6 – disables transmit data echo (local copy) function for half-duplex operation, by maintaining the received data input to the UC1671B at a logic 1 level while RTS = 1.

Analog Loopback/Remote Test (AL/RT), bit 7 – combines with Self-Test (output word 2, bit 7) to produce the loopback conditions shown in tables 1-3 and 1-4. A manual override switch on the module selects the remote test function regardless of the states of SELFTST or AL/RT.

Table 1-3. Self-Test/Analog/Remote Test Loopback Configurations

SELFTST	AL/RT	Loopback Configuration
0	0	No loopback (normal operation)
0	1	Analog loopback only
1	0	Self-test only
1	1	Self-test, Remote test-

Table 1-4. Signals Looped Back For Self Test, Remote Test, and Loopback Connector

Mode/Connector	Signal	Looped Back As
Self-Test	DTR	DSRI
	RTS	DCDI
	RTS	CTS (within UC1671B)
	SERXMITDATA	SERRCVDATA
	SRTS	SDCDMX
	CDR/NEWSYN	RINGMX
	SLFTSTCLK	XMITCLKMX
	AL/RT	R/T
	"0"	A/L
Remote Test	SERRCVDATAX	XMITDATAMX
	"1"	DTRMX
	SDCD	SRTSMX
	DCD	RTSMX
Loopback Connector	DTRZ	DSRZ
	RTSZ	CTSZ
	RTSZ	DCDZ
	SRTSZ	SDCDZ
	NSZ	RINGZ
	SDZ	RDZ

1.2.2 **INPUT WORDS.** Figure 1-4 illustrates the contents of the input words, and the following paragraphs describe the functions of those contents.

1.2.2.1 **Input Word 0.** Input word 0 is one of two 16-bit input words. Bits 0 through 7 of input word 0 contain the data character received from the modem. Bits 8 through 15 contain status information. Input word 0 is read from the DAL bus by setting ADD,0-2,Q = 000 (output word 0, bits 8-10) and STROBE = 1 (output word 0, bit 11). Following are descriptions of the bits of input word 0.

Read Data Word (RCVDATA,0-7), bits 0-7 – byte input from UC1671B to CRU via STCR instruction in response to SBO STROBE. If output word 3, bits 6, 7 (CHARLEN,0,1) specifies a character length of less than eight bits, `RCVDATA,0-7, - is LSB-justified with 0-fill. RRQ must be set to read a valid read data word.

Sync Mode (SYNCMODE), bit 9 – output word 3, bit 5.

	INPUT WORD				
BIT	0	1	2	3	4
0	RCVDATA0	DSR1	DTR	CLKSELA0	ID0
1	1	CTS	RTS	CLKSELA1	1
2	2	SDCDMX	ENRRQ	CLKSELA2	2
3	3	RESMDMOO	ENPARITY	ATCK/STPSYN	3
4	4	RINGMX	ECHO/STPDLE	PARITYSEL	4
5	5	DCD1	SBS/XMITPAR	SYNCMODE	5
6	6	NOT USED	BREAK/XPRNT	CHARLEN0	6
7	RCVDATA7	NOT USED	SELFTST	CHARLEN1	ID7
8	NOT USED	RRQ			
9	SYNCMODE	SYNCMODE			
10	NOT USED	UNDERRUNQ			
11	R/WBUSYQ	R/WBUSYQ			
12	PE/DLEDTCT	NSFQ			
13	FE/SYNDTCT	TIMEXQ			
14	OVERRUN	INTRSUM			
15	RCVERRORSUM	WRQ			

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Figure 1-4. Input Word Contents

Read or Write Busy (R/WBUSYQ), bit 11 – indicates that the module is busy processing a software-directed read or write command. If R/WBUSYQ is inactive, normal reading or writing can be done. Before continuing processing, R/WBUSYQ should be examined to ensure that no read or write operation is pending completion.

Parity Error/DLE Detect (PE/DLEDTCT), bit 12 – active when output word 2, bit 3 is active and a parity error has been detected in the last character received by the UC1671B receive register. PE/DLEDTCT is driven inactive when STROBE for input word 0 goes low. For synchronous communications when output word 2, bit 4 is enabled, the receiver parity check is disabled, and PE/DLEDTCT goes high if the character immediately preceding the character currently in the UC1671B receiver holding register matched the DLE character.

Framing Error/SYNC Detect (FE/SYNDTCT), bit 13 – indicates, for asynchronous communications, detection of a 0 stop bit that should have been a 1. FE/SYNDTCT becomes inactive when STROBE for input word 0 goes low. For synchronous communications, FE/SYNDTCT is active when the contents of the UC1671B receiver register match the SYNC character.

Overrun (OVERRUN), bit 14 – indicates that an attempt has been made to load a new character into the UC1671B receive register before the current character has been read by the computer, causing loss of the new character. OVERRUN goes inactive with a status scan cycle or when the UC1671B receiver is disabled.

Receive Error Summary (RCVERRORSUM), bit 15 – indicates at least one of the following conditions:

- PE/DLEDTCT = 1 in nontransparent mode
- FE/SYNDTCT = 1 in asynchronous mode
- OVERRUN = 1

1.2.2.2 **Input Word 1.** Input word 1 is a 16-bit word that may be read when ADD,0-2,Q = 000 and STROBE = 0.

Data Set Ready (DSR), bit 0 – indicates the state of DSRZ from modem.

Clear to Send (CTS), bit 1 – indicates the state of CTSZ from the modem. When CTS is active, data transmission from the computer is enabled.

Secondary Data Carrier Detect (SDCDMX), bit 2 – indicates the state of SDCDZ from the modem. SDCDMX indicates the detection of a 387-Hertz carrier on the communication line.

Reserved Modem Lead Output (RESMDMO0) bit 3 – indicates the status of output word 4, bit 3.

Ring (RINGMX), bit 4 – indicates the state of RINGZ from the modem.

Data Carrier Detect (DCD), bit 5 – indicates the state of DCDZ from the modem.

Read Request (RRQ) bit 8 – an interrupt condition that occurs when the UC1671B receiver holding register is loaded with a data character and ENRRQ (output word 2, bit 2) is active. RRQ is cleared when Read Data Word (input word 0, bits 0-7) is read from the UC1671B.

Synchronous Mode (SYNCMODE), bit 9 – contents of output word 3, bit 5 that indicates whether asynchronous (SYNCMODE = 0) or synchronous (SYNCMODE = 1) communication is enabled.

Underrun (UNDERRUNQ), bit 10 – defined for synchronous communication only. UNDERRUNQ indicates that the UC1671B transmitter holding register has been empty for at least one character time (the time required to serially transmit one character) and has had to insert fill characters into the transmitted data stream. UNDERRUNQ is made inactive by driving ENWRQ = 0, and is defined for 8-bit characters only.

Read or Write Busy (R/WBUSYQ), bit 11 – indicates that the module is busy processing a software-directed read or write command. If R/WBUSYQ is inactive, normal reading or writing can be performed. Before continuing processing, R/WBUSYQ should be examined to ensure that no read or write operation is being performed.

New Status Flag (NSFQ), bit 12 – indicates a change of state in one of the following modem signals when CLRENNSF (output word 0, bit 12) is active:

- DSRZ
- SDCDZ
- DCDZ

  } 0 → 1 or 1 → 0, while DTR = 1

- RINGZ 0 → 1 only

Timer Expired (TIMEXQ), bit 13 – indicates that the most recent 250-millisecond interval started by CLRSETENTIM (output word 0, bit 13) has expired.

Interrupt Summary (INTRSUM), bit 14 – indicates at least one of the following conditions:

- RRQ = 1
- WRQ = 1
- TIMEXQ = 1
- NSFQ = 1

Write Request (WRQ), bit 15 – indicates that the UC1671B transmitter holding register is emptied while ENWRQ (output word 0, bit 15), RTS (output word 2, bit 1) and CTS (input word 1, bit 1) are active. WRQ is cleared when a data character is written to the UC1671B transmitter holding register or when RTS is disabled.

1.2.2.3 **Input Word 2.** Input word 2 contains the current contents of UC1671B register C1 as determined by the most recent write to output word 2. Input word 2 is read when ADD,0-2,Q = 100 and STROBE = 1.

NOTE

The self-test bit (bit 7) is inverted between the output and input words.

1.2.2.4 **Input Word 3.** Input word 3 indicates the current contents of UC1671B register C2, as determined by the most recent write to output word 3. Input word 3 is read when ADD,0-2,Q = 001 and STROBE = 1

1.2.2.5 **Input Word 4.** Input word 4 contains the module ID code set by the ID switches. Bit 0 is the LSB. Input word 4 is read when ADD,0-2,Q = 011 and STROBE = 0. No STROBE reference is needed to read the ID.

1.3 DATA FORMAT

The Communications Interface Module accepts 5-, 6-, 7-, or 8-bit data characters from the computer. Character length is software determined in the host computer.

During asynchronous communication, the module produces start, parity, and stop bits and attaches them to the data characters before transmitting the characters to the modem. The module checks the parity of data characters received from the modem, then strips (removes) the start, parity, and stop bits from the characters prior to providing them to the computer..

During synchronous communication, only the parity bit is assembled to write data characters and stripped from read data characters.

The parity bit immediately precedes the MSB of the data character, except for an 8-bit character, in which case the parity bit *replaces* the MSB of the character.

One, one and a half, or two stop bits are selected by output word 2, bit 5.

Figure 1-5 illustrates the data format.

1.4 STATUS SCAN CYCLE

The status scan cycle is a 2-part cycle produced continuously while power is active to the module (except when interrupted by a command or forced by setting STROBE = 1 with ADD,0-2,0 = 110).

During the first part of the cycle, the ring counter toggles CS– to the UC1671B and causes SELADD– to enable the address register onto the DAL bus along with the hardwired ID ("0"). The address register contents are preset to point to the status register.

Figure 1-6 shows the ring counter logic.

During the second portion of the status scan cycle, the UC1671B loads eight bits of status information onto the DAL bus for the status register and STATCLK– loads the information into the status register. Read request, write request, and new status interrupts are loaded into the status register. All other status register bits are meaningless unless a data transfer is taking place.

1.5 DATA TRANSMISSION

To transmit data characters to the modem, software executing in the computer loads the address of output word 0 onto CRU interface, loads the character to be transferred via an LDCR instruction, and sets STROBE = 0. REFSTRBCK– in the read/write control logic sets the busy flag, R/WBUSYQ. The busy flag directs the synchronization of STROBE with the status scanner (ASTROCYEN and COMMDCYQ) to allow the next available write cycle to write data to the UC1671B instead of executing a status scan cycle.

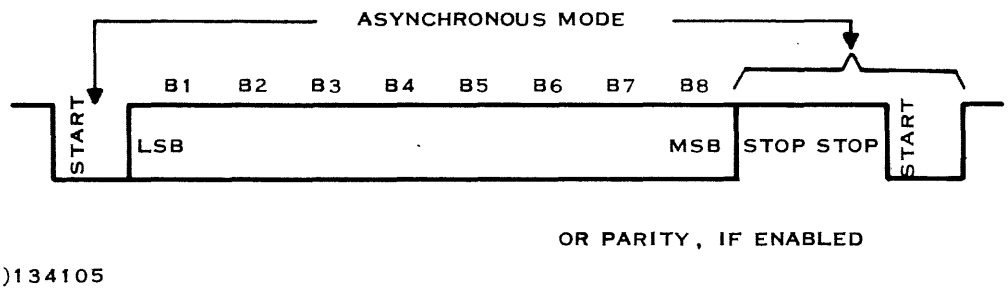

Figure 1-5. Communication System Data Format

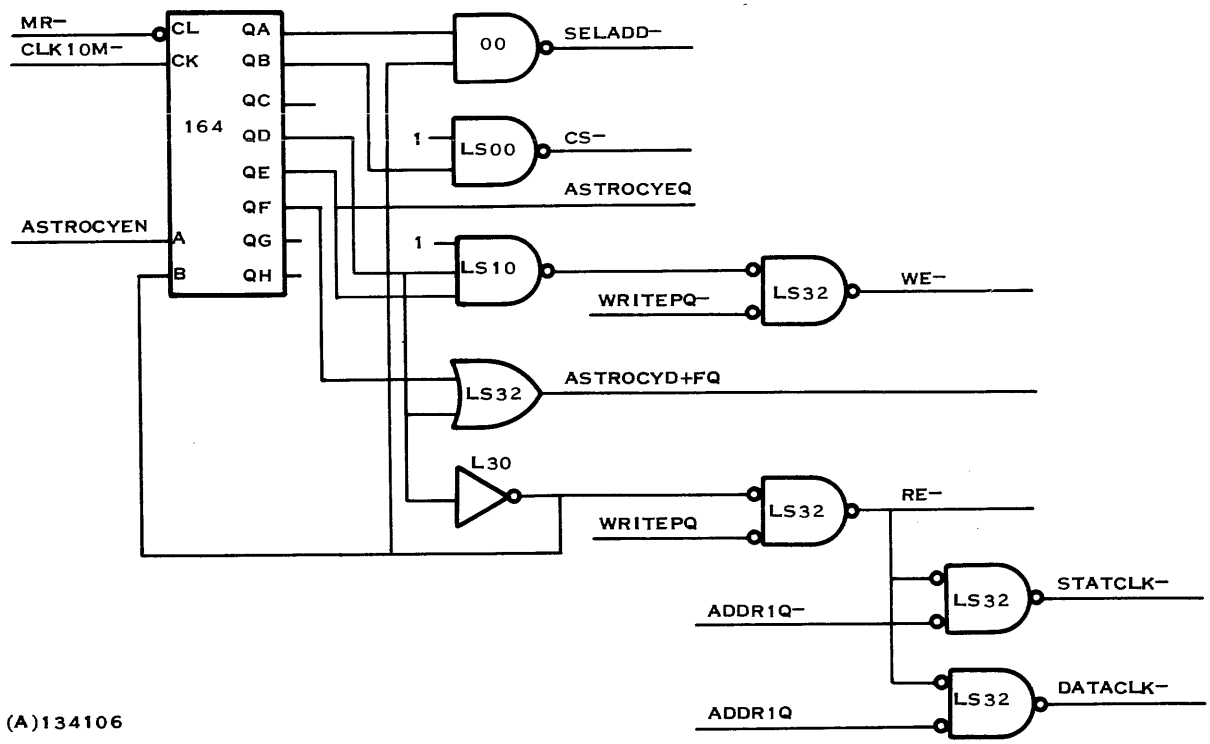

Figure 1-6. Ring Counter Logic

At the beginning of a data transmission cycle, CS– conditions the UC1671B for either a read or write cycle. The address of the UC1671B register to receive the data is loaded onto the DAL bus and the write flip-flop (WRITEQ) gates WE– to the UC1671B. WE– and the address on the DAL bus prepare the UC1671B to receive data into the addressed register. The appropriate output word is loaded onto the DAL bus by the ring counter and held there for one character cycle time (300 nanoseconds). The address in the address register is then reset (CLRBUSY–) to point to the status register, ADD,0-2,Q is reset (CLRBUSY–) to 000, and the module returns to a status scan cycle.

1.6 DATA RECEPTION

To read data from the module, software addresses the word to be read and sets STROBE appropriately. Read/write control logic detects the STROBE reference (REFSTRBCK–) and examines the address to determine if a SYNC/DLE character is being written. If a read operation is indicated, the ring counter issues a CS– pulse to condition the UC1671B for a read or write operation. The address of the register to be read is loaded onto the DAL bus and RE– pulsed. The UC1671B responds by placing the contents of the addressed register on the DAL bus. The ring counter (DATACLK–) clocks the UC1671B data into the data register. STROBE = 1 inhibits further ASTROCYEN pulses. Thus, the status scan cycle is inhibited and the validity of any error signals is ensured. The computer reads the desired input word by issuing an STCR instruction.

Following completion of the read cycle, the address in the address register is reset (CLRBUSY–) to point to the status register, ADD,0-2,Q is reset (CLRBUSY–) to 000, and the module returns to a status scan cycle.

1.7 UC1671B

The UC1671B is the heart of the Communications Interface Module. The remainder of the logic on the module provides timing and input/output circuitry to support the UC1671B. The UC1671B provides the following capabilities for both asynchronous and synchronous communications:

- full-duplex operation
- 0- to 1-million baud rates
- 8 selectable clock rates
- TTL-compatible logic
- on-line diagnostic capability
- transmission parity error detection
- overrun detection
- selectable 5- to 8-bit characters

The following capabilities are provided for synchronous communications:

- programmable SYN and DLE character stripping
- programmable SYN and DLE fill

Additionally, the following capabilities are provided for asynchronous communications:

- line break detection and generation
- 1, 1 1/2, or 2 stop bit selection
- automatic serial echo mode

Figures 1-7 and 1-8 are flowcharts for the UC1671B receive and transmit modes, respectively.

1.8 MODULE LOGIC DESCRIPTIONS

The following paragraphs describe the module's circuits

1.8.1 CLOCK NETWORK. The Communications Interface Module clock network consists of a voltage-controlled oscillator set to produce two complementary 9.8304-megahertz square waves, five counters to frequency-divide the primary clock signals, and a multiplexer to select the baud rate clock to control reception and transmission rates. Figure 1-9 illustrates the clock network.

1.8.2 RING COUNTER. The ring counter (figure 1-6) is an 8-bit parallel-out serial shift register with combinational logic that provides the proper sequencing for read and write operations. Figure 1-10 is a timing diagram for a read/write cycle. Figure 1-11 shows the detailed UC1671B read/write timing and illustrates the gate propagation delays not shown in figure 1-10.

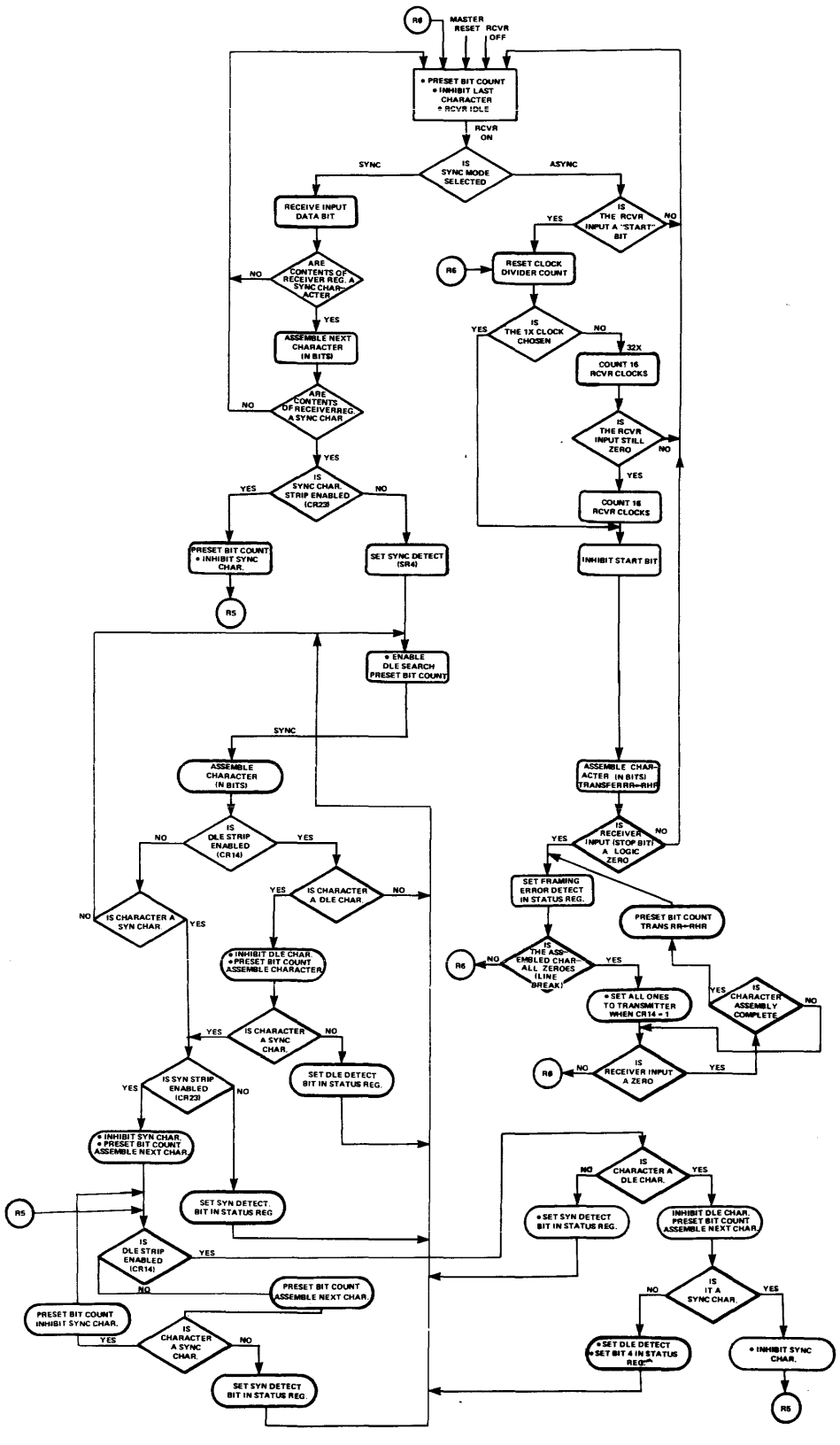

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Figure 1-7. UC1671B Receive Flowchart

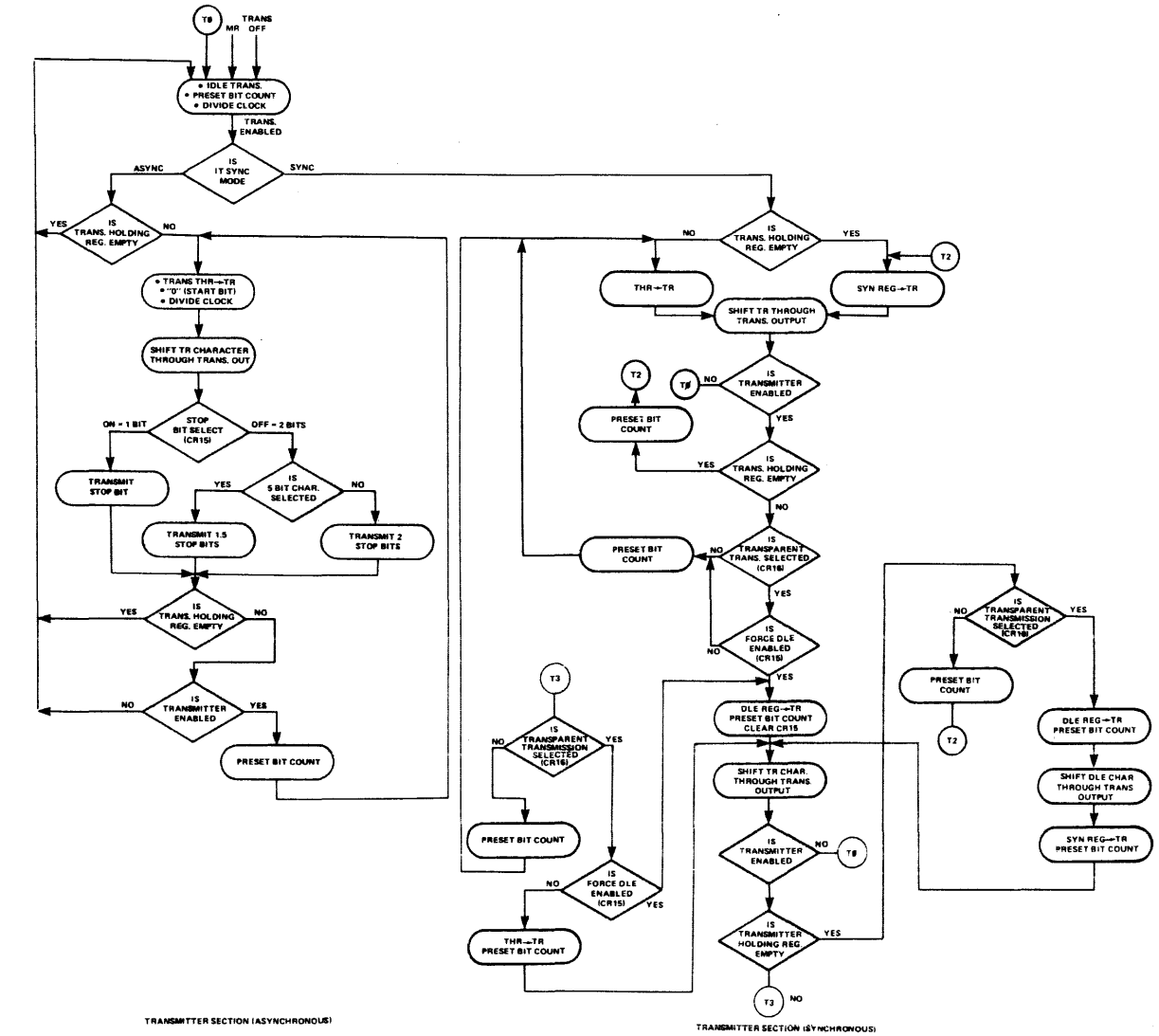


Figure 1-8. UC1671B Transmit Flowchart

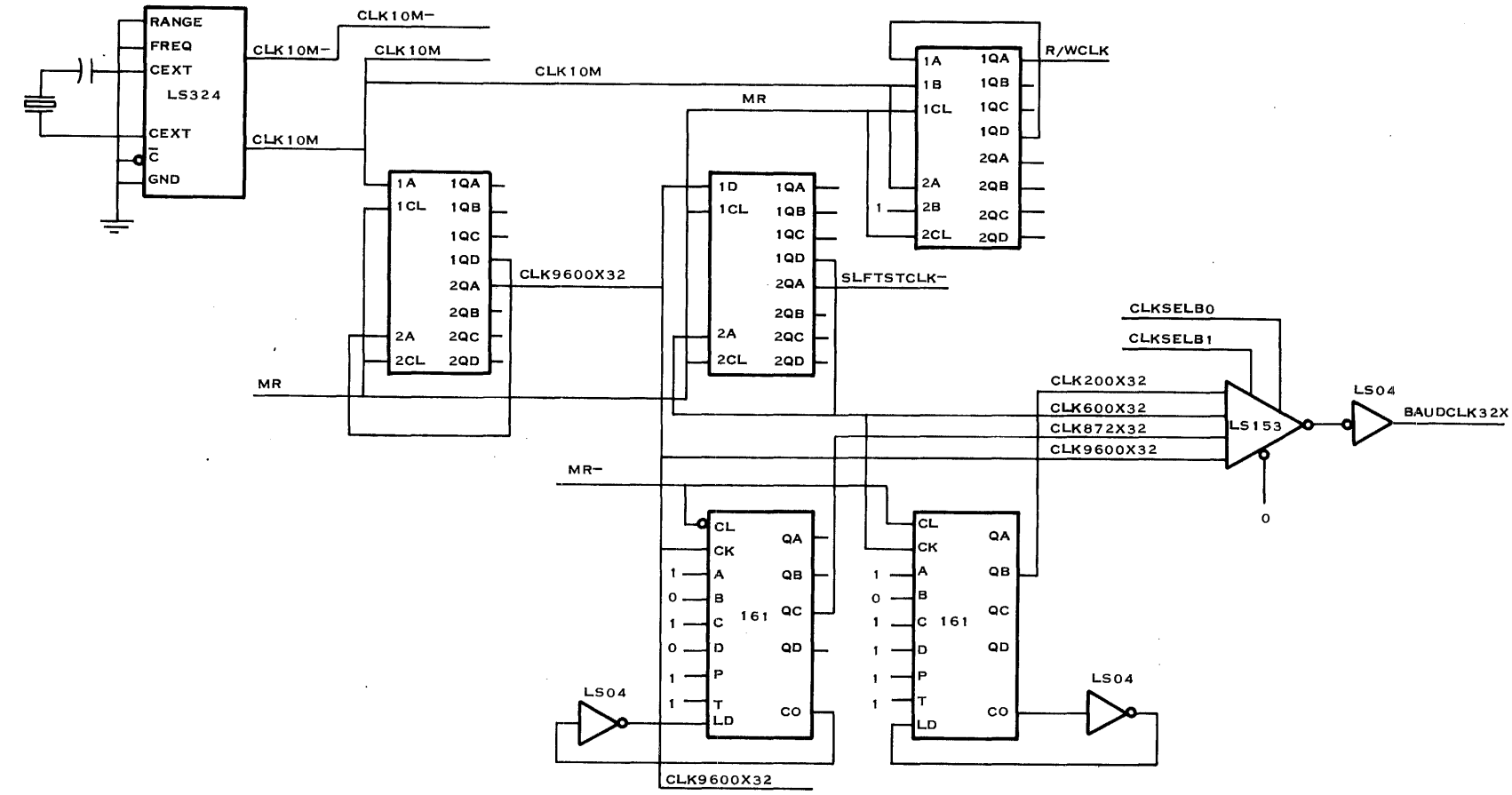


Figure 1-9. Clock Network

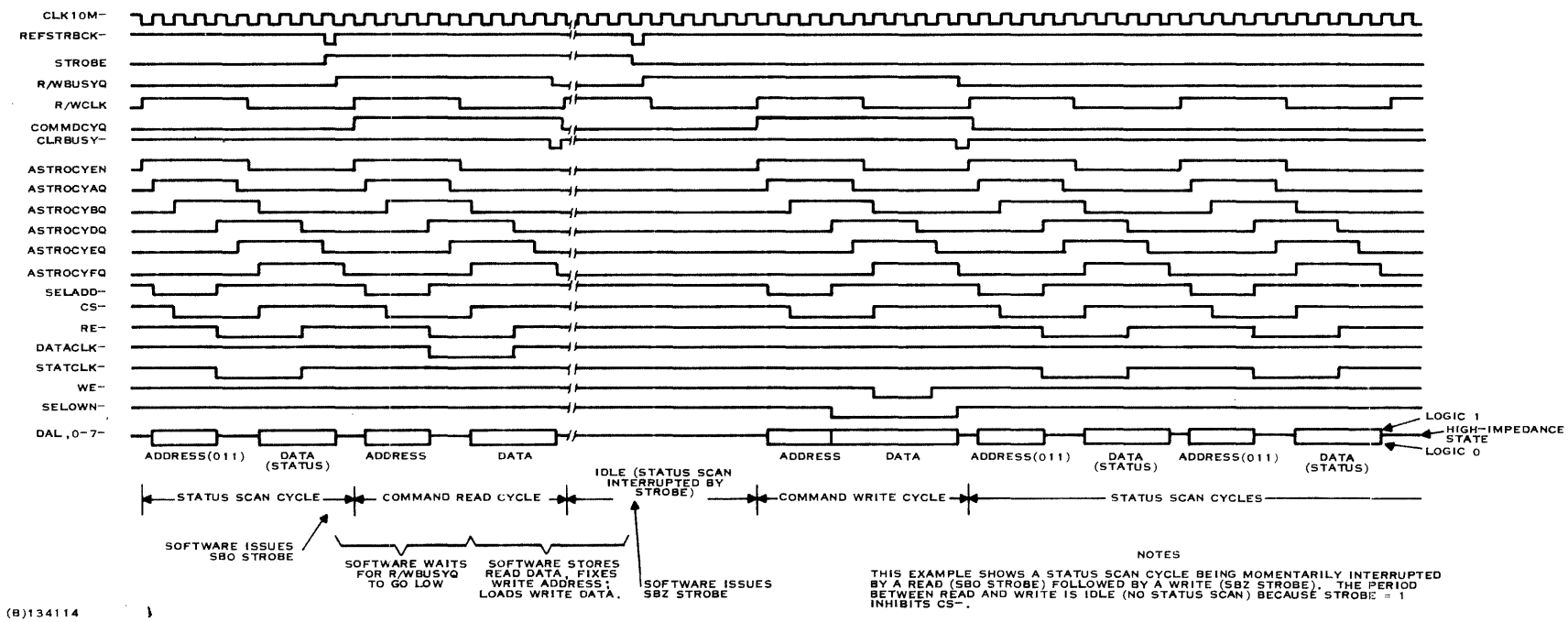
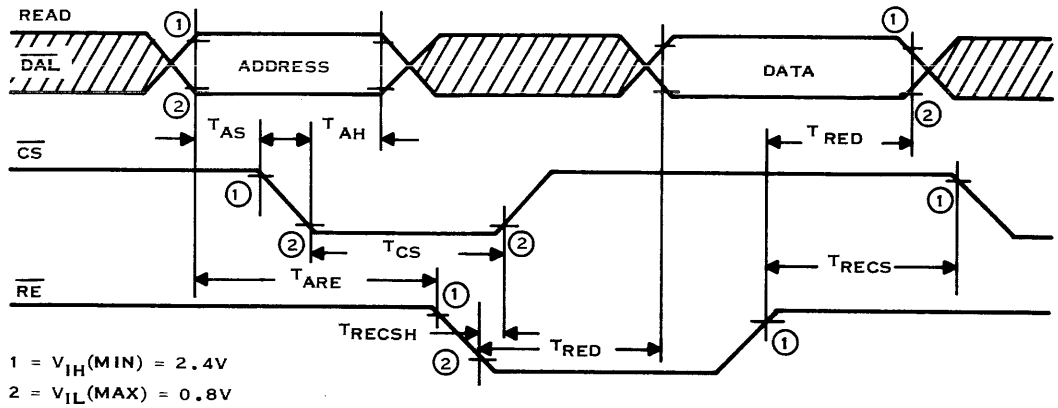
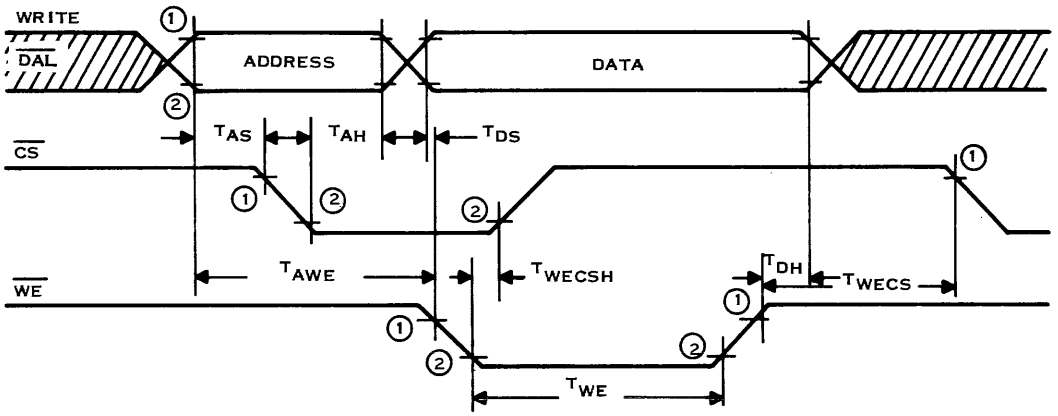


Figure 1-10. Read/Write Cycle Timing Diagram





AC CHARACTERISTICS

T_A=Ø° C TO 70° C, V_{DD}=+12.ØV±0.6V, ±V_{BB}=−5.ØV±0.25V, V_{CC}=+5.0±.25V, V_{SS}=ØV

CL_{MAX} =20pf

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{AS}	ADDRESS SET-UP TIME	0	100		ns	
T_{AH}	ADDRESS HOLD TIME	150	200		ns	
T_{CS}	$\overline{CS}$ WIDTH	250	400		ns	
READ						
T_{ARE}	ADDRESS AND $\overline{RE}$ SPACING	250	300		ns	
T_{RECSH}	$\overline{RE}$ AND $\overline{CS}$ OVER LAP	20	200		ns	
T_{RECS}	$\overline{RE}$ TO $\overline{CS}$ SPACING	250	400		ns	
T_{RED}	$\overline{RE}$ TO DATA OUT DELAY			180	ns	C_L = 20
WRITE						
T_{AWE}	ADDRESS TO $\overline{WE}$ SPACING	250	300		ns	
T_{WECSH}	$\overline{WE}$ AND $\overline{CS}$ OVER LAP	20	100		ns	
T_{WE}	$\overline{WE}$ WIDTH	200	300	1000	ns	
T_{DS}	DATA SET-UP TIME	50	100		ns	
T_{DH}	DATA HOLD TIME	100	200		ns	
T_{WECS}	$\overline{WE}$ TO $\overline{CS}$ SPACING	250	400		ns	

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Figure 1-11. Detailed UC1671B Read/Write Timing

1.8.3 **UNDERRUN LOGIC.** Underrun logic monitors Write Request Enable (ENWRQ) and Character Length (CHARLEN1) to produce Underrun, an indication that the UC1671B has had to insert fill characters into the transmitted data stream because the transmitter holding register has been empty for at least one character time.

1.8.4 **OUTPUT WORD REGISTERS.** Six 8-bit addressable latches make up four 8-bit and one 16-bit registers for the five output words (figure 1-3) used by the communication system. The output word being written is determined by software and addressed by bits 8-10 of output word 0. The contents of the output word registers are enabled onto the DAL bus by write enable logic.

1.8.5 **READ/WRITE CONTROL LOGIC.** Read/write control logic consists of five flip-flops and combinational logic that produces signals to direct read and write operations and to provide a busy indication to inhibit reading and writing to the UC1671B. Figure 1-12 illustrates read/write control logic.

1.8.6 **WRITE ENABLE LOGIC.** Write enable logic is a 3-to-8 line data selector that decodes the outputs of the address latches to produce six signals to enable the write operation and individually select the output word to be written. Figure 1-13 shows the write enable logic.

1.8.7 **OUTPUT WORD 3-STATE DRIVERS.** The output word drivers invert the parallel outputs of the output word registers and place it on the DAL bus when enabled by the output word selector. There is no driver for output word 4 because that register's contents provide features not related to the UC1671B. Since output words 0 and 1 are contained in the same register, one driver is provided for both words.

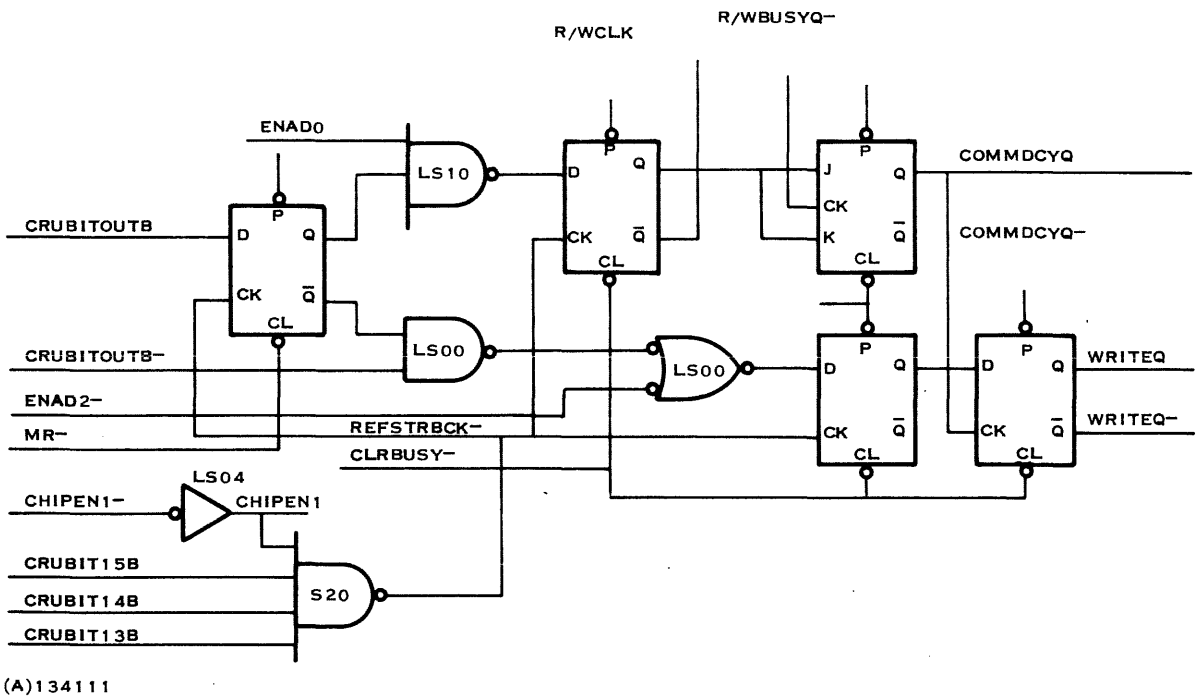

Figure 1-12. Read/Write Control Logic

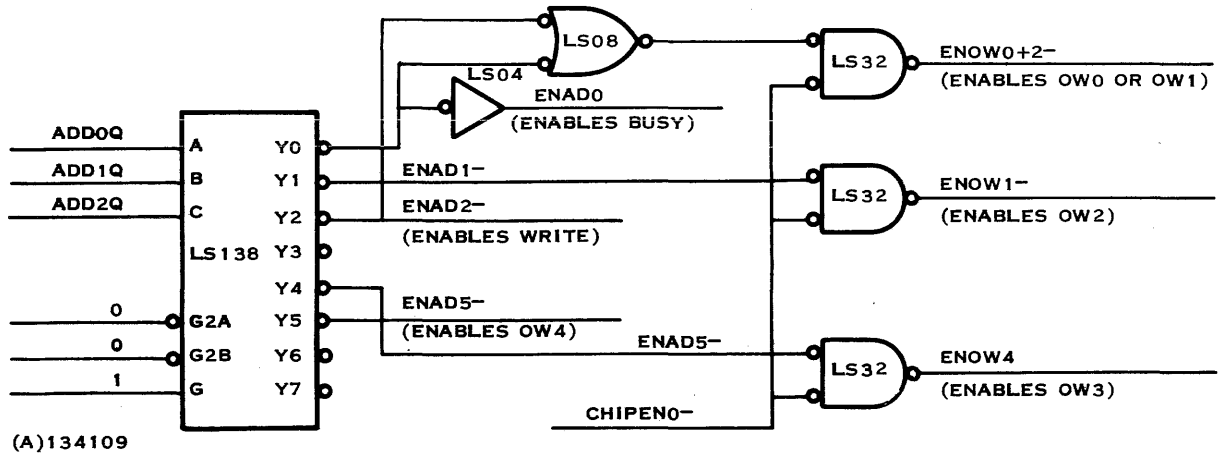

Figure 1-13. Write Enable Logic

1.8.8 **250-MILLISECOND TIMER.** The 250-millisecond timer produces a software-controlled 250-millisecond delay before producing an interrupt to the computer. The delay may be used to time events (RTS-CTS (line turnaround) delay, data transfer, etc.) under direct software control.

1.8.9 **INTERRUPT LOGIC.** Figure 1-14 illustrates the logic that detects interrupt conditions to provide to the computer and/or load into input word 1, bit 14.

1.8.10 **RECEIVE DATA REGISTER.** The receive data register is an 8-bit flip-flop register that is loaded with data from the DAL bus when clocked by DATACLK–. The receive data register contents are available to the input word multiplexer.

1.8.11 **INPUT WORD REGISTERS.** Five multiplexers pass data and status signals from module logic serially to the CRU interface to be read by the computer. Each bit of each multiplexer is addressable by software.

1.8.12 **ANALOG LOOPBACK/REMOTE TEST LOGIC.** Analog loopback/remote test logic monitors Self Test and Analog Loopback/Remote Test from output word 4 and directs the module to enter either the analog loopback mode or the remote test mode. The remote test feature allows the remote processor to verify data transmission and reception (over a 4-wire line). The analog loopback feature allows the local processor to verify local data set operation.

1.9 INTERFACES

Figure 1-15 depicts the Communications Interface Module's interfaces with a Model 990 Computer and a modem. The following paragraphs describe the signals.

1.9.1 **COMPUTER/MODULE INTERFACE SIGNALS.** Following are descriptions of the signals on the interface between the computer and the module.

CRU Address (CRUBIT,12-15) – CRU address bits that specify one of 16 inputs or 16 outputs to be read or written.

Module Select (MODSELA–) – a low-active signal set by addressing the CRU base address of the module. MODSELA– enables the module for read or write.

CRU Clock (STORECLK–) – a low-active signal that indicates that data from the computer (CRUBITOUT) is valid. Data is accepted by the module on the rising edge of STORECLK–.

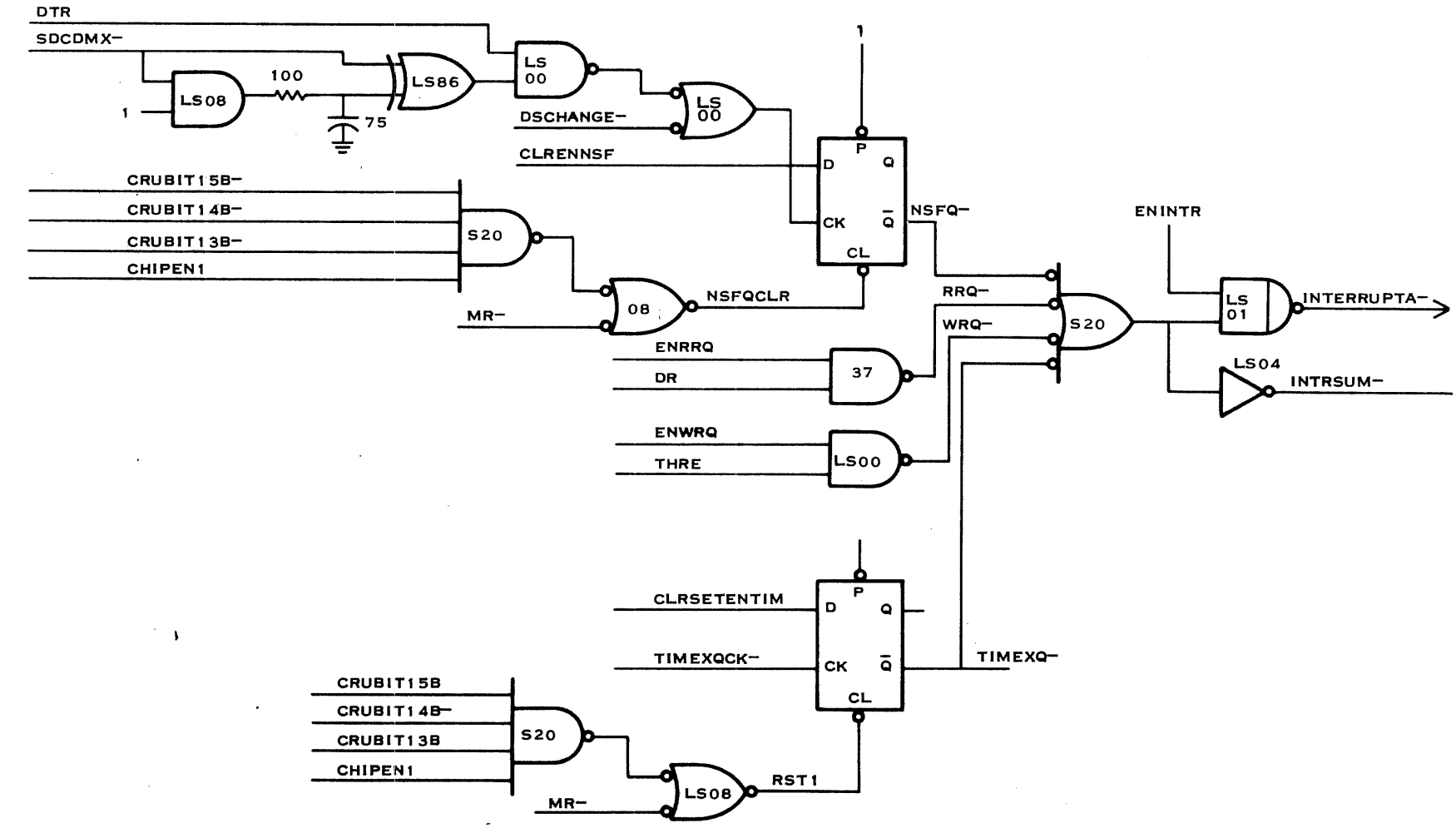

Figure 1-14. Interrupt Logic

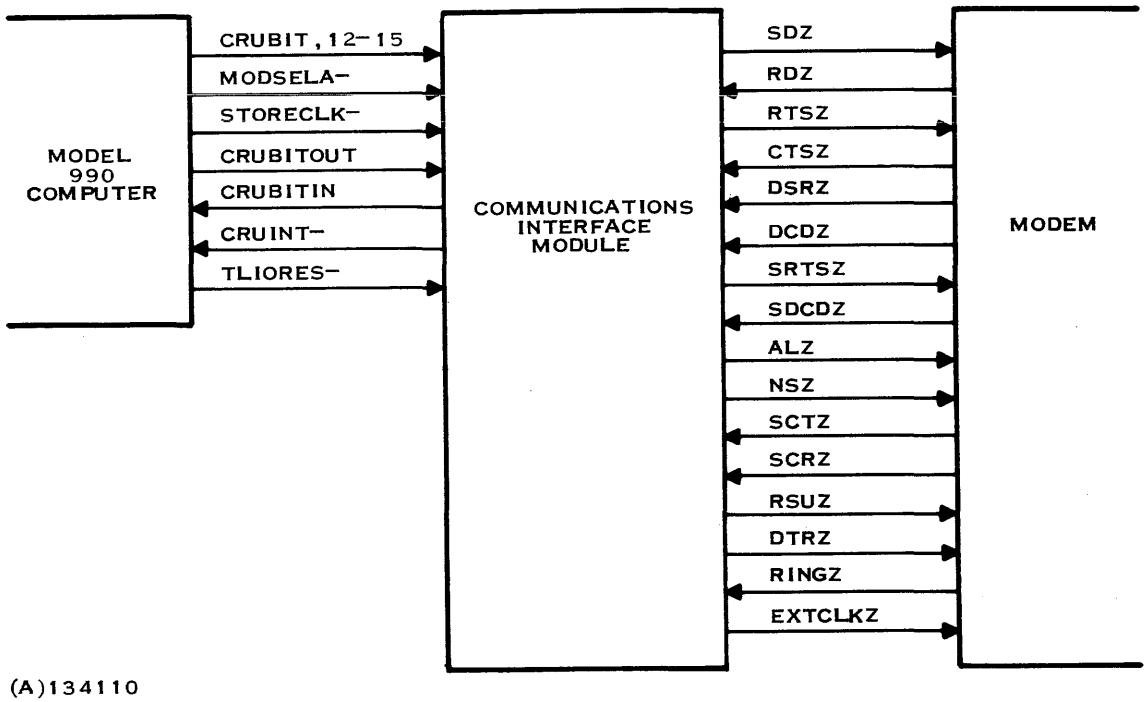

Figure 1-15. Communications Interface Module Interface Signals

Serial Output Data (CRUBITOUT) – serial data from the computer. The data is latched and converted to parallel format to represent the output words of the module.

Serial Input Data (CRUBITIN) – serial data representing data characters from the modem, status conditions, or diagnostic information requested by the computer.

CRU Interrupt (INTERRUPTA–) – a low-active signal from the module that indicates that at least one enabled interrupt condition exists on the module.

Reset (TLIORST–) – a low-active signal from the computer that initializes the module.

1.9.2 MODULE/MODEM INTERFACE SIGNALS. Following are descriptions of the signals on the interface between the module and the modem. The logic levels of these signals conform to EIA Standard RS-232-C.

Transmitted Data (SDZ) – serial data originated by the computer for the modem.

Received Data (RDZ) – serial data received from the modem.

Request to Send (RTSZ) – a high-active signal that notifies the modem that the module is ready to transmit data.

Clear to Send (CTSZ) – the modem's indication to the module that the modem and the telephone line are prepared to receive data from the module.

Data Set Ready (DSRZ) – a high-active signal from the modem that notifies the module that the modem is ready (response to DTR).

Received Line Signal Detector (DCDZ) – a high-active signal from the modem indicating the presence of a signal on the telephone line that is suitable for demodulation.

Secondary Request to Send (SRTSZ) – a high-active signal to the modem used to provide circuit assurance for some half-duplex operations.

Secondary Received Line Signal Detector (SDCDE) – signal from the modem in response to SRTS that indicates detection of a 387-Hertz carrier on the telephone line. This signal is used for circuit assurance.

Analog Loopback Enable (ALZ) – a high-active signal that enables transmitted data to be sent from the module to the modem and returned for examination. Data is looped back at the modem's telephone line terminals.

Carrier Detect Reset/New Sync (CDRZ/NSZ) – a high-active signal produced as a result of setting the Pulsed Modem Output Lead (output word 4, bit 4). A 1-millisecond high-active pulse used by multidrop network masters to resynchronize synchronous (NS) or asynchronous (CDR) slaves.

Transmit Clock (SCTZ) – the signal produced by a synchronous modem to clock transmit data to the modem.

Receive Clock (SCRZ) – synchronous baud clock produced by a synchronous modem to clock receive data to the module.

Reserved Lead (RSVZ) – reserved for customer modem output signal. Reserved lead is driven by output word 4, bit 3. RSVZ turns on AUDIO MONITOR on a Texas Instruments internal modem.

Data Terminal Ready (DTRZ) – a high-active signal to the modem to indicate readiness of the computer (terminal). DTRZ is also used to answer incoming calls on a switched network without automatic answer.

Ring Indicator (RINGZ) – a high-active signal from the modem representing the ring of an incoming call on a switched network.

Transmit Clock External (EXTCLKZ) – a baud clock produced by the module to synchronize and phase transmit and receive rates in remote test mode.

SECTION II

MAINTENANCE

2.1 GENERAL

This section describes the maintenance philosophy for the Communications Interface Module and provides troubleshooting procedures to allow fault isolation to the component level. Component replacement procedures are given in *Model 990/4 Computer System Depot Maintenance* and *Model 990/10 Computer System Depot Maintenance Manual.*

2.2 MAINTENANCE PHILOSOPHY

Depot maintenance for the Communications Interface Module is based on the use of a diagnostic test executing in a hot mock-up system incorporating a Model 990 series computer, a Model 990 Maintenance Unit and a combination dual-trace oscilloscope/digital multimeter as shown in figures 2-1 and 2-2.

The Communications Interface Module is tested by using the Communications Interface Module Performance Demonstration Test (part number 945455) and its error messages to troubleshoot the module. Component-level fault isolation is accomplished by using the test to establish scoping loops through the module's circuitry and checking the logic with the aid of the logic diagram in *Model 990 Computer Family Maintenance Drawings.*

2.3 SPECIAL TEST EQUIPMENT

The special test equipment required to perform depot maintenance on the Communications Interface Module includes:

- Model 990 Computer Hot Mock-up System
- Test Connector (part number 948550)

Operating instructions for the hot mock-up system are provided in *Model 990/4 Computer System Depot Maintenance Manual* and *Model 990/10 Computer System Depot Maintenance Manual.*

NOTE

Refer to the manufacturer-supplied user manuals for oscilloscope/digital multimeter operating procedures.

2.3.1 TEST CONNECTOR. The module must be tested with a special test connector or modem attached. Any tests which cannot be meaningfully performed without either the test connector or modem are skipped and indicated by printing "TEST n SKIPPED".

2.4 MAINTENANCE PROCEDURES

Maintenance procedures for the module consist of a preliminary checkout to determine if any problems exist which can be visually detected, and fault isolation procedures to locate faulty circuit components. The following paragraphs describe those procedures.

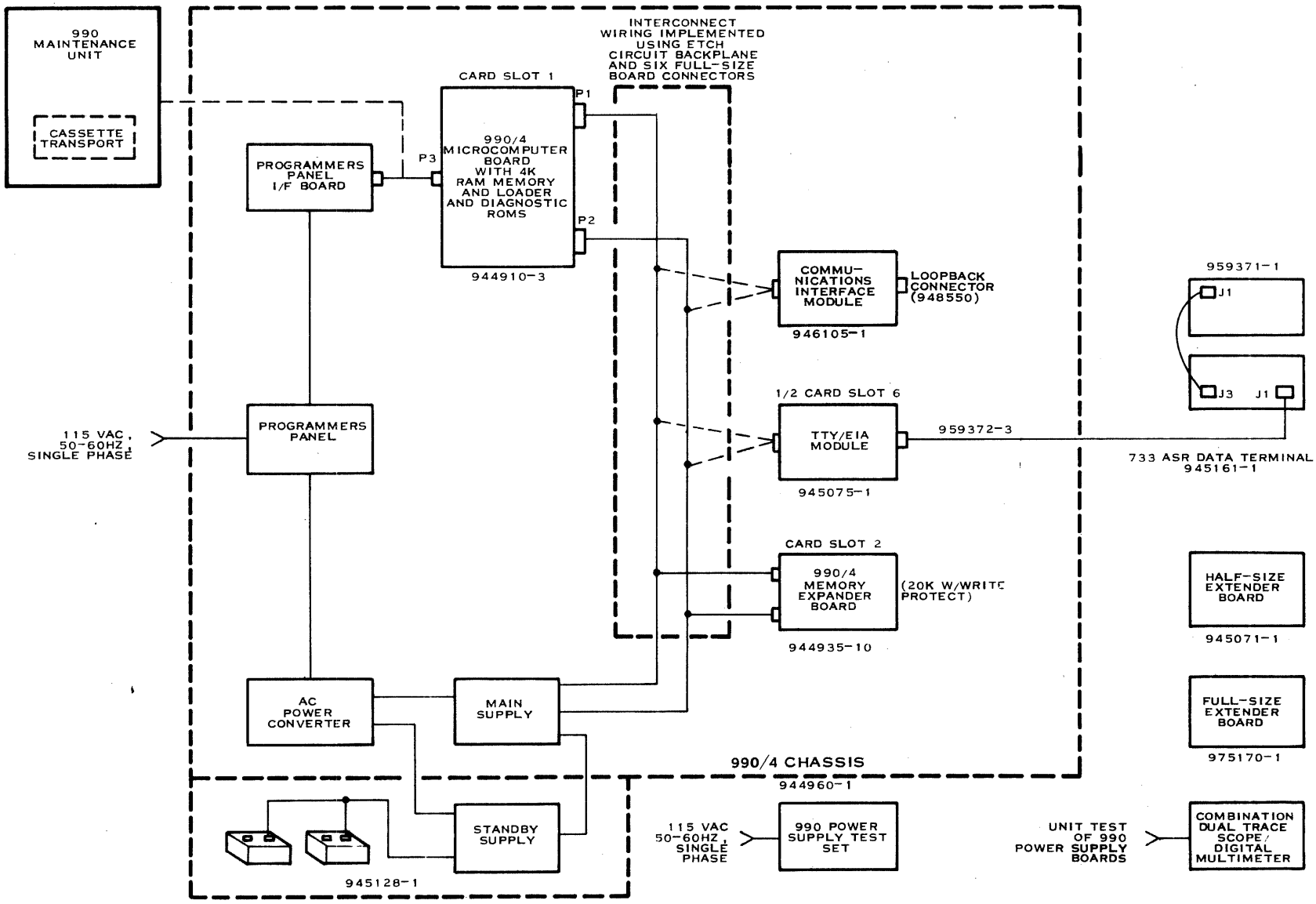

Figure 2-1. Model 990/4 Computer Hot Mock-Up System

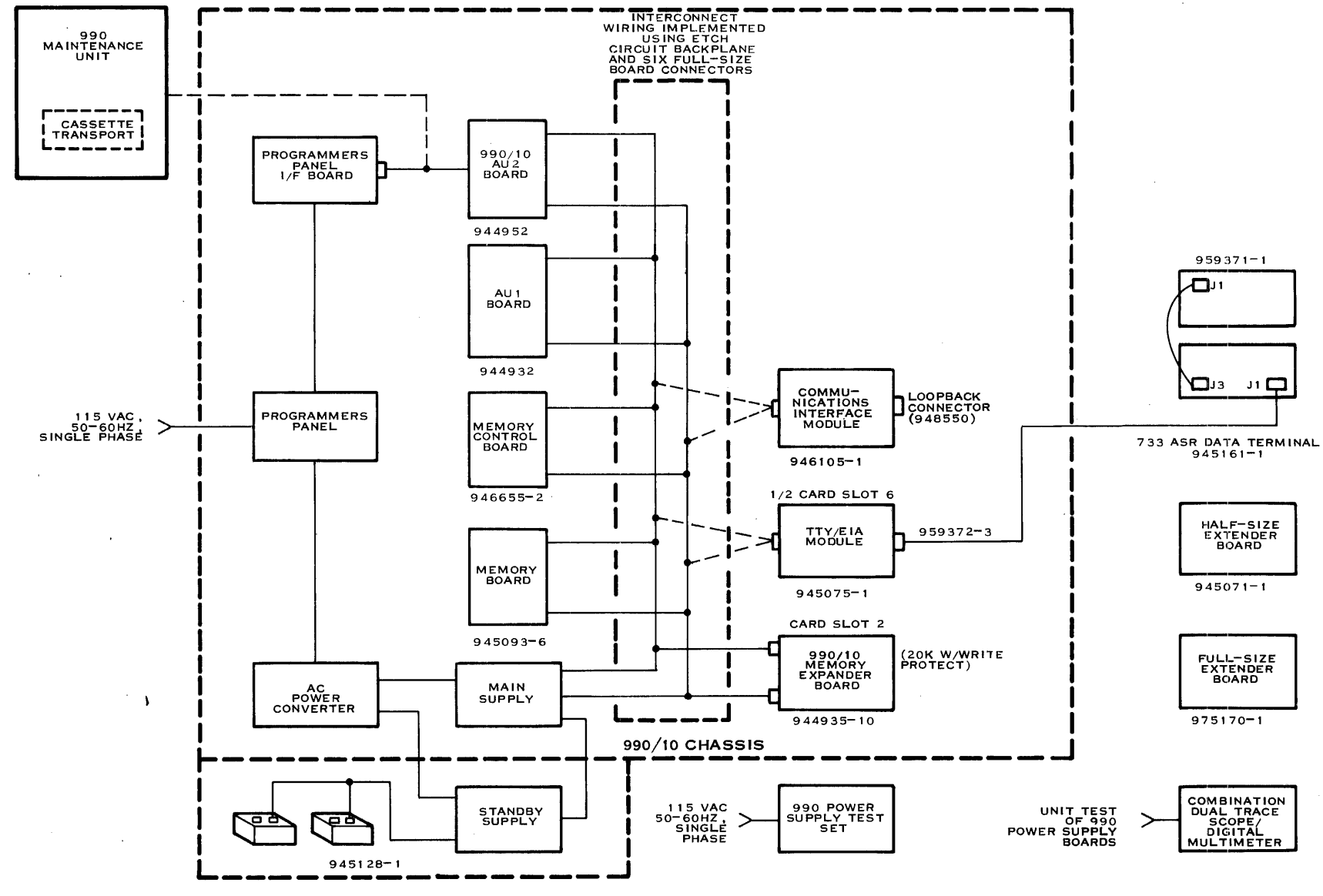

Figure 2-2. Model 990/10 Computer Hot Mock-Up System

2.4.1 **PRELIMINARY CHECKOUT.** Upon receipt of a suspect module from the field maintenance facility, visually inspect the board for the following:

- broken board
- loose or missing components
- damaged (broken) components, wires, etc.
- breaks in the etched circuitry
- foreign materials lodged between package pins that may cause short circuits

If a thorough visual inspection indicates no problem, perform the following steps to prepare for troubleshooting and fault isolation procedures.

1. Turn off all ac power to the hot mock-up system.
2. Place the interface module on an extender board and insert the combination into an available CRU slot.
3. Connect the test connector or proceed to step 4.
4. Connect the modem cable to the module (optional).
5. Note the CRU base address and interrupt address associated with the CRU slot being used. These will be important to the troubleshooting procedure.

2.4.2 **FAULT ISOLATION PROCEDURES.** Fault isolation consists of executing the Communication Interface Module Test noting any error messages obtained during execution of the test, and using the test to establish scoping loops through the logic.

Instructions for loading the diagnostic are in *PD, CRCOMM, Communications Interface Module Test/10 and/4-990* (part number 945455-9901).

General troubleshooting procedures are as follows:

1. Set up the performance demonstration test to suppress header and error messages by reinitializing (IS verb).
2. Use LT verb, specifying failed test, to loop on the test which failed.
3. Attach oscilloscope Channel A probe to MR– for synchronization.
4. Set the time base on the oscilloscope so that two MR– pulses (approximately 60-nanoseconds wide) are visible on the screen.
5. Use oscilloscope Channel B probe to trace circuit path exercised by LT (test).
6. Examine signals in scoping loop realizing that the time interval on the oscilloscope screen is one cycle time through the failing test.

The performance demonstration test error messages are, in most instances, self-explanatory and pinpoint the failure, if not the cause. When used to establish scoping loops, a given test toggles a minimal number of bits or performs a minimal number of functions. The exceptions are tests 12 through 15 which perform time-consuming data transfers. The details of the operations performed in tests 12 through 15 are checked by prior tests so that failures of these tests most probably indicate faulty EIA drivers (tests 14 or 15) or clock circuits faults.

If the frequency of the master clock (9.8304 MHz) is out of tolerance, the data transfer may take a longer or shorter time than expected and cause failure of a test.

The clock circuitry can be checked by the following procedures:

1. Set the oscilloscope time base to 20 nanoseconds per division.
2. Set oscilloscope for positive-edge triggering.
3. Connect Channel A probe to pin 6 of the SN74LS324N (in 14-pin socket).
4. Verify cycle time (threshold $\approx$ 2 Vdc) of 102 $\pm$ 2 nanoseconds.

NOTE

Error and header messages must be suppressed in accordance with PD, CRCOMM to ensure a loop short enough to scope.

2.4.2.1 Scoping Loops. A scoping loop is a short repetetive software program which establishes and maintains a set of conditions in the circuitry under observation so that an error of normally brief duration may be observed and isolated. Once an error message has been printed, determine which test was being performed from printout. Using the special verb, LT, cause the diagnostic to loop on that test and maintain the error condition. This establishes a scoping loop which may be probed until the faulty component is located.

NOTE

Probing should begin at the point indicated by the error message and proceed until the fault is located. Following are the tests performed by the diagnostic and used to establish scoping loops on the module:

Test 1
This test toggles RES MODEM LD OUT (OUTPUT WORD 4 - Bit 3) and SYNCMODE (OUTPUT WORD 3 - Bit 5) and tests the corresponding input for agreement.

Test 2
This test sets DTR and then toggles SRTS to determine if SDCD toggles in agreement. Then it checks to see if NSF (New Status Flag) and INTSUM are set and cleared properly by this condition.

Test 3
This test checks the 250-millisecond timer ($\overline{\text{TIMEXP}}$) for proper setting and clearing and checks the timing to within the design tolerance. It also checks INTSUM for proper setting and clearing.

Test 4
This test reads the ID switches on the Module and prints no message (except TEST 4 COMPLETE) unless the switches are set to other than >7F (that is switches 1-7 all closed ("ON")). In the event there is a discrepancy, it prints the switch ID as read and indicates an error.

Test 5
This test checks to ensure that the interrupt logic on the Module properly interrupts the processor when enabled, and not otherwise.

Test 6
This test writes an alternating pattern of (all "1" and all "0") bytes to OUTPUT WORDS 2 and 3, strobing each to the UC1671B. It then reads the UC1671B registers thus written back through the I/F to verify correct operation. Then it swaps bytes and repeats process.

NOTE

For further isolation of an error discovered by test 6, refer to paragraph 2.4.2.2.

Test 7
This test writes a "WALKING 1" pattern to OUTPUT WORDS 2 and 3, strobing each to the UC1671B. It then reads the UC1671B registers thus written back through the I/F to verify correct operation. Then it writes a "WALKING 0" pattern and repeats until a "1" and a "0" have been walked through all 8 bit positions.

NOTE

For further isolation of an error discovered by test 7, refer to paragraph 2.4.2.2.

Test 8
This test checks the correct operation of the 1 millisecond pulse used as Carrier Detect Reset on an asynchronous modem and Newsync on a synchronous modem. The PULSED MODEM LD (OUTPUT WORD 4 - Bit 4) bit is toggled various times to check proper setting of the RING INDICATOR input and timing is checked to within the design tolerances.

Test 9
This test checks the CDR/NEWSYNC EIA driver and the RING EIA receiver by toggling PULSED MODEM LD and checking RING for agreement.

Test A
This test toggles DTR and checks the toggling of DSR. It also checks to see if DSR setting causes NSF to set, when enabled.

Test B
This test toggles RTS and checks the toggling of CTS and DCD. It also checks to see if DCD setting causes NSF to set, when enabled.

Test C
This test toggles SRTS and checks the toggling of SDCD. It also checks to see if SDCD changes cause NSF to set, when enabled.

Test D

This test sets up the conditions which should cause WRQ to set, and then checks to see if WRQ sets when enabled, and resets when disabled. It also checks to see if INTSUM is set when WRQ = 1.

Test E

This test sets up a data transfer, but with RRQ disabled, thus forcing an OVERRUN condition. It tests for the OVERRUN bit being set and RCVERRSUM being set. It then enables RRQ and checks to see if RRQ goes from a zero to a one. It also receives the character transmitted and verifies that the transfer was done correctly.

Test F
This test writes the UC1671B's SYNC and DLE registers, and then uses the transparent idle fill feature to transmit a DLE/SYNC sequence. This constitutes a transmitter UNDERRUN condition; so, the UNDERRUN bit is tested for setting. Then the receiver is enabled and the DLE/SYNC sequence's proper transmission and reception is verified.

Test 10
This test enables the half-duplex bit (HALF-DUPLEX) which masks the receive data to a logic 1 and verifies that no RRQ interrupts are generated.

Test 11
This test forces a line break condition (transmitted data a constant space) and tests proper operation of the BREAK bit. Since the breaking condition also forces a parity error and framing error, these bits (PE and FE) and RCVERRSUM are also tested for proper setting.

Test 12
This test performs a series of 200-baud, 20-byte data transfers in SELF-TEST, ASYNCHRONOUS mode to verify data transfer capability. The transfer is performed 4 times and must be executed successfully (no error conditions) all four times in order to pass. Loopback paths are established within the UC1671B.

Test 13
This test performs a series of data transfers of 8 SYNC characters and 200 bytes of data at 9.6 Kbits/second in SELF-TEST, SYNCHRONOUS mode to verify data transfer capability. The transfer is performed 4 times and must be executed successfully (no error conditions) all four times in order to pass. Loopback paths are established within the UC1671B.

Test 14
This test performs a series of 100-byte data transfers at 1200 baud in AYSNCHRONOUS mode. Other test parameters are essentially the same as in Test 12, except that a modem or a loopback connector must be connected to the module.

Test 15
This test performs a series of transfers of 8 SYNC characters and 200 bytes of data at 2400 baud in SYNCHRONOUS mode. Other test parameters are essentially the same as in Test 13, except that a modem or a loopback connector must be connected to the module.

NOTE

Tests 13 and 15 use a clock-recovery method for synchronizing the data (unless a synchronous modem is used). Thus although the data format is synchronous the clocking scheme is essentially asynchronous.

NOTE

All tests first master-reset the Module so that all output CRU interface bits are zero, all registers are zero and all flip-flops are zero (inactive). This MR– pulse also provides a synchronize pulse for scoping loops.

2.4.2.2 **Special Scoping Loop.** When an error is encountered in either test 6 or 7, or both, during the diagnostic test sequence, a tighter loop is frequently required to isolate the failing component. The following program loop functions like tests 6 and 7, but allows selective writing or reading of only one register using a selected data pattern. In any of the selected loop patterns, the data specified (in R1) is written to the addressable latch on the module, and then strobed to the ASTRO. During the read loop, the ASTRO register is read through the interface and into R2. The write loop and the combination write/read loop provide a reset (MR–) pulse on the module that can be used to synchronize the scope. Each loop is approximately 20 - 30 microseconds long and provides good resolution of detail in the scoping loop. The basic code for the special loop is contained in figure 2-3. The following instructions describe the procedure for loading and modifying (patching) the program:

1. Load program into memory biased by a convenient value. Add the bias value to the locations in the modification procedures given below.

2. Alter the WP and base address (locations 2 and 6, respectively) if required.

3. Alter the data pattern to be written (contained in the most significant byte of location A) to the failing pattern detected in test 6 or 7.

4. Perform one of the following modifications to access either interface word 2 or 3:

   a) Word 2 – change locations 10_{16} and $1A_{16}$ from $1D0A_{16}$ to 1000_{16}.

   b) Word 3 – change locations E_{16} and 18_{16} from $1D08_{16}$ to 1000_{16}.

5. Select one of the following steps to execute a write loop, a read loop or a combination write/read loop, respectively:

   a) Write Loop – Set PC to 0 and select RUN.

   b) Read Loop – change location 16_{16} from $10FA_{16}$ to 1000_{16}; set PC to 0 and select RUN.

   c) Write/Read Loop – change location 16_{16} from $10FA_{16}$ to 1000_{16}; change location 22_{16} from $10FA_{16}$ to $10F4_{16}$; set PC to 0 and select RUN.

(RELATIVE) ADDRESS	(ABSOLUTE) OBJECT			COMMENTS
0000	02E0		LWPI >3800	LOAD WP
0002	3800			
0004	020C		LI R12,>140	LOAD BASE ADDRESS
0006	0140			
0008	0201		LI R1,>AA00	INITIALIZE DATA
000A	AA00			
000C	0360	LUP1	RSET	CLEAR I/F
000E	1D08		SBO 8	} SELECT OW
0010	1D0A		SBO A	
0012	3201		LDCR R1,8	LOAD DATA TO I/F
0014	1E0B		SBZ B	STROBE DATA TO ASTRO
0016	10FA		JMP LUP1	JUMP (WRITE LOOP)
0018	1D08	LUP2	SBO 8	} SELECT OW
001A	1D0A		SBO A	
001C	1D0B		SBO B	STROBE ASTRO
001E	3602		STCR R2,8	STORE DATA FROM I/F
0020	1E0B		SBZ B	CLOSE READ LOOP
0022	10FA		JMP LUP2	JUMP (READ LOOP)

Figure 2-3. Special Scoping Loop

APPENDIX A

SIGNATURE GLOSSARY

APPENDIX A

SIGNATURE GLOSSARY

Following is an alphabetical list of the signatures which could be confusing to someone not familiar with the Communications Interface Module.

ADD,0-2,Q – Address of output or input word software wishes to write to or read. Cleared at the end of any command cycle.

ADDR,0-2,Q – Latched address that refers to the unmapped latched UC1671B register address. Points to UC1671B register being addressed. Preset to point to UC1671B status register at the end of any command cycle.

ASTROCYAQ, ASTROCYBQ, ASTROCYDQ, ASTROCYEQ, ASTROCYFQ – 400-nanosecond wide ring counter outputs.

ASTROCYEN – Enable ring counter synchronously with R/WCLK.

CLK10M – 9.8304-MHz square wave.

CLK9600X32 – 9600 X 32 bits/second clock signal (Asynchronous data clocking is performed by the UC1671B utilizing a 32X clock.)

PSSTROBEQ – Past state of STROBE.

REFMR– – STORECLK– wide pulse on any SBO or SBZ to Master Reset.

REFSTRBCK – STORECLK– wide pulse on any SBO or SBZ to STROBE.

THRE – Transmitter holding register empty.

U/REN – Underrun enable.

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
- Appendixes - References to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.
- Paragraphs - References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.
- Tables - References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

  Tx-yy

- Figures - References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number:

  Fx-yy

- Other entries in the Index - References to other entries in the index are preceded by the word "See" followed by the referenced entry.

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USER'S RESPONSE SHEET

Manual Title: Model 990 Computer Communications Interface Module
Depot Maintenance Manual (945410-9701)

Manual Date: 1 April 1977 **Date of This Letter:** _____

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Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

Location in Manual	Comment/Suggestion
_____	_____
	_____
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