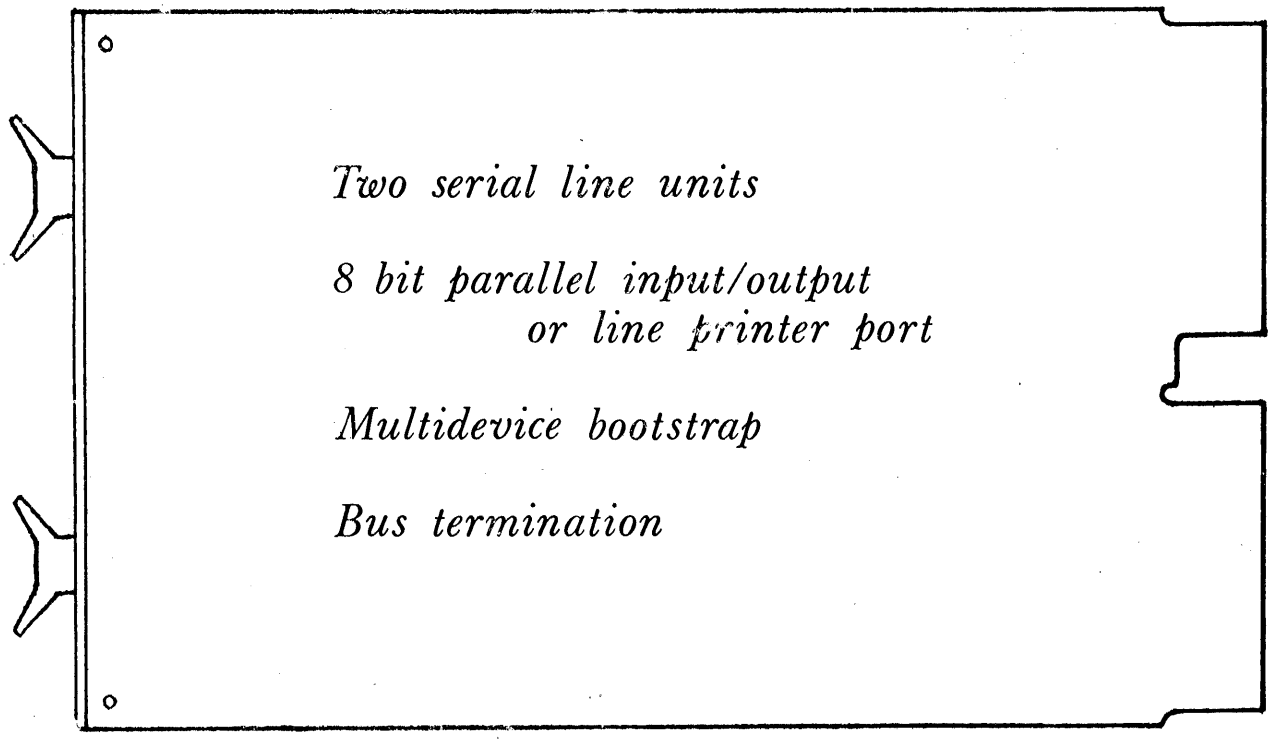
2SP
2SPB
2SPBT

Owner's Manual



Two serial line units

8 bit parallel input/output or line printer port

Multidevice bootstrap

Bus termination

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TABLE OF CONTENTS

Figures

Tables

FUNCTIONAL DESCRIPTION

The TECHNICAL MAGIC 2SPBT combines one parallel and two serial ports with an intelligent, multi-device bootstrap and Q-bus termination on a single dual-width board. This high density, multifunction board saves backplane space while allowing easy user configuration of its many options and is completely compatible with LSI-11.

The serial ports can be used as general purpose interfaces to serial peripheral devices using Electronic Industry Association (EIA) standard RS-232C, RS-423 or RS-422 communication protocol and are DEC DJV11-J compatible. One of the two serial ports can be configured as the console port to communicate with a local or remote terminal.

The parallel port can be used as a general purpose interface to parallel peripheral device using four-cycle Mueller handshake communication protocol. The parallel ports of two 2SPBTs can be connected directly together using industry standard mass-termination cable and connectors to create a high speed parallel communication link between two LSI-11s by simply inverting the cable at the end. The parallel port can also be configured as a printer port to drive a Centronics or Data Products compatible line printer.

All serial and parallel ports are hardware and software compatible with the LSI-11.

The bootstrap performs memory diagnostics and boots peripheral devices in a priority chain manner. If the first device in the priority chain list does not exist, it then boots the second device. If the device exits, the 2SPBT waits until the device is ready, and boots from it. Typing an escape on the console will proceed directly to the next device. The standard priority chain list is RK05 followed by RX01/RX02. Bootstraps for any standard DEC devices are available. Custom bootstraps can be written for any devices.

The bus terminator can be removed easily if the module is not used as a terminator.

THEORY OF OPERATION

GENERAL

This module has two serial ports which are implemented with two universal asynchronous receivers and transmitters (UART) associated with a baud rate generator and transceivers for EIA interface. The parallel port is implemented with an octal latch and two octal drivers with latches and gates to control handshake with the user device. The bootstrap and memory diagnostic program is stored in two bootstrap PROMs. The bus interface which performs address matching, vector forcing and control signals generating is implemented with a DEC Chipkit, two address PROMs, a vector PROM and three address decoders with some gates.

BUS INTERFACE

The bus interface is mainly handled by a DEC chipkit which has four transceiver logic chips, three interrupt logic chips and a protocol logic chip. The address matching is performed by the four transceiver logic chips which buffer the address lines into two address PROMs, compare against the user-assigned parallel port address and generate a match signal. The two address PROMs also compare the address lines against the programmed serial port and bootstrap addresses and generate match signals. These match signals are then interpreted by the address decoders which generate control signals that read from or write to the serial ports, the parallel port, or the bootstrap PROMs.

Vector forcing is performed by the three interrupt logic chips which generate vector request signals to a vector PROM when an interrupt request signal is received. The vector PROM sends the programmed interrupt vector to the transceiver chips which force this interrupt vector to the bus.

Bus timing is handled by the protocol logic chip which decides whether the operation is a read or a write.

SERIAL PORTS

Each serial port is implemented with a universal asynchronous receiver and transmitter (UART) which converts serial data to parallel data, converts parallel data to serial data, generates error signals, and sends interrupt request

signals. Serial data is received or transmitted through an EIA receiver or driver. Error signals are buffered through drivers to the high byte of the input buffer register. Interrupt request signals are sent to the interrupt logic chip to activate interrupts.

PARALLEL PORT

The parallel port is implemented with an octal latch and two octal drivers. The output data is stored in the octal latch by the control signal from the address decoders. Similarly, the output and input data are read through the octal tri-state drivers by the control signal. Handshake with the user device is controlled by latches and gates which interpret the request signal from and generate the acknowledge to the user device and generate interrupt request signals to the interrupt logic chip.

BOOTSTRAP

The bootstrap and memory diagnostics are contained in the two bootstrap PROMs.

The size of user random access memory (RAM) is calculated by the bootstrap program and printed on the console. The memory diagnostics are then run and numeric error messages are printed on the console if the memory fails the diagnostics.

After successful completion of the memory diagnostics, the bootstrap tries to boot the first device in the priority chain. If the first device does not exist, it is skipped and the next device in the priority chain is tried. If the first device is busy, it can be skipped by typing an escape on the console and the next device is tried. If the last device in the priority chain is tried and fails, the bootstrap is halted. The devices in the priority chain can be retried by typing a capital P. The standard priority chain list is RK05, RX01/RX02.

UNUSED BIT PROMS

Two open-collector PROMs are utilized to force the unused bits of the parallel and two serial ports read as zeros.

CONFIGURATION

GENERAL

Each function of this module can be disabled or enabled individually as best fits the user system. One of the serial ports (S1) can be configured as the console port and the parallel port can be configured as a printer port by the function switch. The individual function switch assignments are shown in Table 1. The device register bit assignments are shown in Figure 1. The jumper and switch locations are shown in Figure 2. Each function is described in the following paragraphs.

TABLE 1 FUNCTION SWITCH

SWITCH	FUNCTION	DESCRIPTION
1	BUSY	should be closed if there is no connection to Extra Received Bit on the parallel connector and a 74LS240 is at 1A
2	P/LP	closed to configure as a parallel port opened to configure as a printer port
3	512/256	closed to choose 512 word bootstrap space opened to choose 256 word bootstrap space
4	S1/CON	closed to configure as a second serial port opened to configure as the console port
5	RM	closed to disable the bootstrap
6	SOM	closed to disable the first serial port
7	S1M	closed to disable the second serial port
8	PM	closed to disable the parallel port

SERIAL PORT

The addresses and vectors of the two serial ports and the console port are fixed and stored in the address and vector PROM respectively. They can be programmed by the user or at the factory. The standard address and vector configuration is shown in Table 6.

The baud rate can be selected by the clock jumpers and baud rate switch as shown in Table 2. The communication interface protocol can be configured as RS-232C, RS-423 or RS-422 by changing the protocol jumpers and resistor as shown in Table 3. The slew rate for RS-232C and RS-423 is specified by the slew rate resistor as shown in Table 2 and the character format is specified by the parameter jumpers as shown in Table 4.

If the second serial port is set for console operation and a break character is received, the system will re-boot, halt or do nothing depending on the halt jumper as shown in Table 5.

TABLE 2 BAUD RATE SELECTION

JUMPERS				SWITCH				SLEW RATE RESISTOR R2	BAUD RATE
A	B	C	D	1	2	3	4		
I	R	R	R	C	C	C	C	1M OHM	50
I	R	R	R	C	C	C	O	1M OHM	75
I	R	R	R	C	C	O	C	1M OHM	110
I	R	R	R	C	C	O	O	1M OHM	134.5
I	R	R	R	C	O	C	C	1M OHM	150
I	R	R	R	C	O	C	O	1M OHM	300
I	R	R	R	C	O	O	C	1M OHM	600
I	R	R	R	C	O	O	O	820K OHM	1200
I	R	R	R	O	C	C	C	620K OHM	1800
I	R	R	R	O	C	C	O	560K OHM	2000
I	R	R	R	O	C	O	C	430K OHM	2400
I	R	R	R	O	C	O	O	330K OHM	3600
I	R	R	R	O	O	C	C	200K OHM	4800
I	R	R	R	O	O	C	O	160K OHM	7200
I	R	R	R	O	O	O	C	120K OHM	9600
I	R	R	R	O	O	O	O	51K OHM	19200
R	R	I	R	X	X	X	X	22K OHM	38400
R	I	R	R	X	X	X	X	10K OHM	76800
R	R	R	I	X	X	X	X		External clock

I=Inserted R=Removed
C=Closed O=Opened X=Don't care

The module outputs the selected internal clock with the jumper D inserted, unless the external clock is being used as input clock.

TABLE 3 SERIAL COMMUNICATION PROTOCOL

JUMPERS		R1 R3 RESISTOR	PROTOCOL
+	-		
L to C	C to R	680 OHM	RS-232C
L to C	C to R	none	RS-423
C to R	L to C	100 OHM	RS-422

L=Left R=Right C=Center

TABLE 4 SERIAL COMMUNICATION FORMAT (PARAMETER)

JUMPER	DESCRIPTION	
A	I=Odd parity	R=Even parity
B	I=7 data bits	R=8 data bits
C	I=1 stop bit	R=2 stop bits
D	I=Enable parity	R=Disable parity

I=Inserted R=Removed

TABLE 5 CONSOLE BREAK (HALT)

JUMPER	DESCRIPTION
L to C	Re-boot
R to C	Halt
N	Do nothing

L=Left R=right C=Center N=No Jumper

PARALLEL PORT

The addresses of the parallel and printer port can be assigned by inserting or removing the address jumpers. The vectors are fixed and stored in the vector PROM. Non-standard vectors can be specified by the user when ordering. The standard addresses and vectors of the parallel and line printer port are shown in Table 6.

TABLE 6 DEVICE STANDARD ADDRESS AND VECTOR

DEVICE	ADDRESS	VECTOR
Serial port S0	176500	300
S1	176510	310
Console port	177560	60
Parallel port	167770(*)	320
Printer port	177514(*)	200
Bootstrap	173000	

* This address can be specified by the address jumpers. Other addresses and vectors are fixed in the address and vector PROMs.

The parallel port can be configured as a parallel port with four-cycle Mueller handshake protocol, a printer port with Centronics interface or a printer port with Data Products interface by changing jumpers and a chip. This is shown in Table 7.

TABLE 7 PARALLEL COMMUNICATION PROTOCOL

SWITCH	JUMPERS				CHIP	DESCRIPTION
P/LP	XBIT	ACK	OUT	IO/O/I	1A	
C	T to C	T to C	T to C	N	LS240	*1
C	T to C	T to C	T to C	R to C	LS240	*2
C	T to C	T to C	T to C	L to C	LS240	*3
O	T to C	T to C	T to C	R to C	LS244	*4
O	B to C	B to C	B to C	R to C	LS240	*5

C=Closed O=Opened
T=top B=Bottom C=Center
L=Left R=Right C=Center N=No Jumper

*1=Parallel port with input only
*2=Parallel port with output only
*3=Parallel port with input and output both
*4=Printer port with Data Products interface
*5=Printer port with Centronics interface

BOOTSTRAP AND TERMINATOR

The starting address of the bootstrap is fixed and stored in the address PROM. The standard starting address of bootstrap is shown in Table 6. The numeric error messages of the memory diagnostics are listed in Table 8. Memory diagnostics may be continued by typing a capital P. The termination can be disabled by changing the termination jumper and removing the terminators as shown in Table 9.

TABLE 8 MEMORY DIAGNOSTICS ERROR MESSAGES

173062*	Error in writing the address to the bad location. R0 points to the bad memory location.
173112*	Error in writing 0 or 177777 to memory. R0 points to the bad memory location. R1 contains what was being written.

* These Addresses may differ slightly in custom versions of the bootstrap.

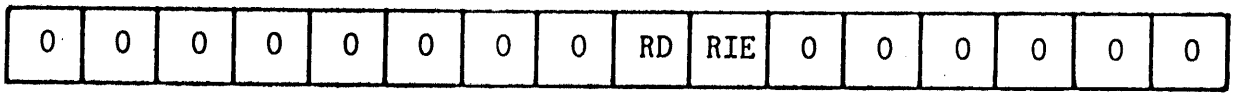
TABLE 9 TERMINATION SELECTION

JUMPER	TERMINATOR	DESCRIPTION
L to C	I	Enable termination
R to C	R	Disable termination

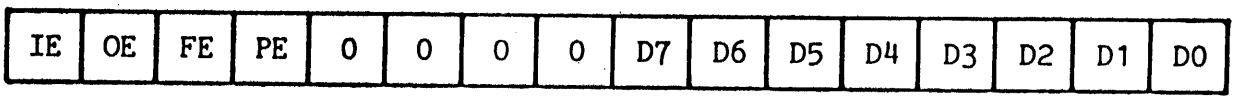
I=Inserted R=Removed
L=Left R=Right C=Center

FIGURE 1 DEVICE REGISTER DESCRIPTION

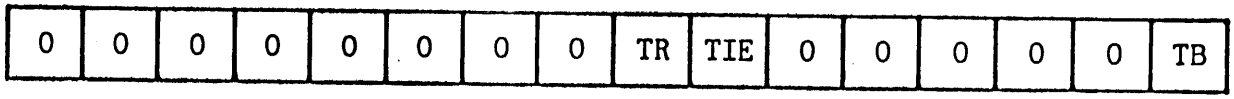
SERIAL PORTS



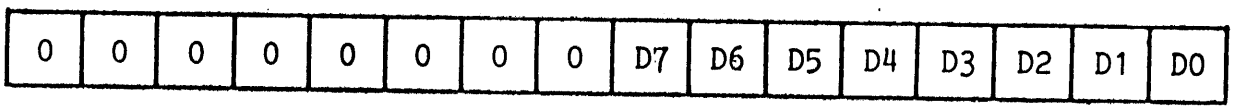
Bits	Code	Input Status Register Function	Access
8-15	0	not used	read as zero
7	RD	Receiver Done	read only
6	RIE	Receiver Interrupt Enable	read/write
0-5	0	not used	read as zero



Bits	Code	Input Buffer Register Functions	Access
15	IE	Input Error	read only
14	OE	Overrun Error	read only
13	FE	Framing Error	read only
12	PE	Parity Error	read only
8-11	0	not used	read as zero
0-7	D	Data	read only



Bits	Code	Output Status Register Functions	Access
8-15	0	not used	read as zero
7	TR	Transmit Ready	read only
6	TIE	Transmit Interrupt Enable	read/write
1-5	0	not used	read as zero
0	TB	Transmit Break	read/write



Bits	Code	Output Buffer Register Functions	Access
8-15	0	not used	read as zero
0-7	D	Data	write only

PARALLEL PORT

0	0	0	0	0	0	0	0	RD	RIE	0	0	0	0	0	0

Bits	Code	Input Status Register Function	Access
8-15	0	not used	read as zero
7	RD	Receiver Done	read only
6	RIE	Receiver Interrupt Enable	read/write
0-5	0	not used	read as zero

0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

Bits	Code	Input Buffer Register Functions	Access
8-15	0	not used	read as zero
0-7	D	Data	read only

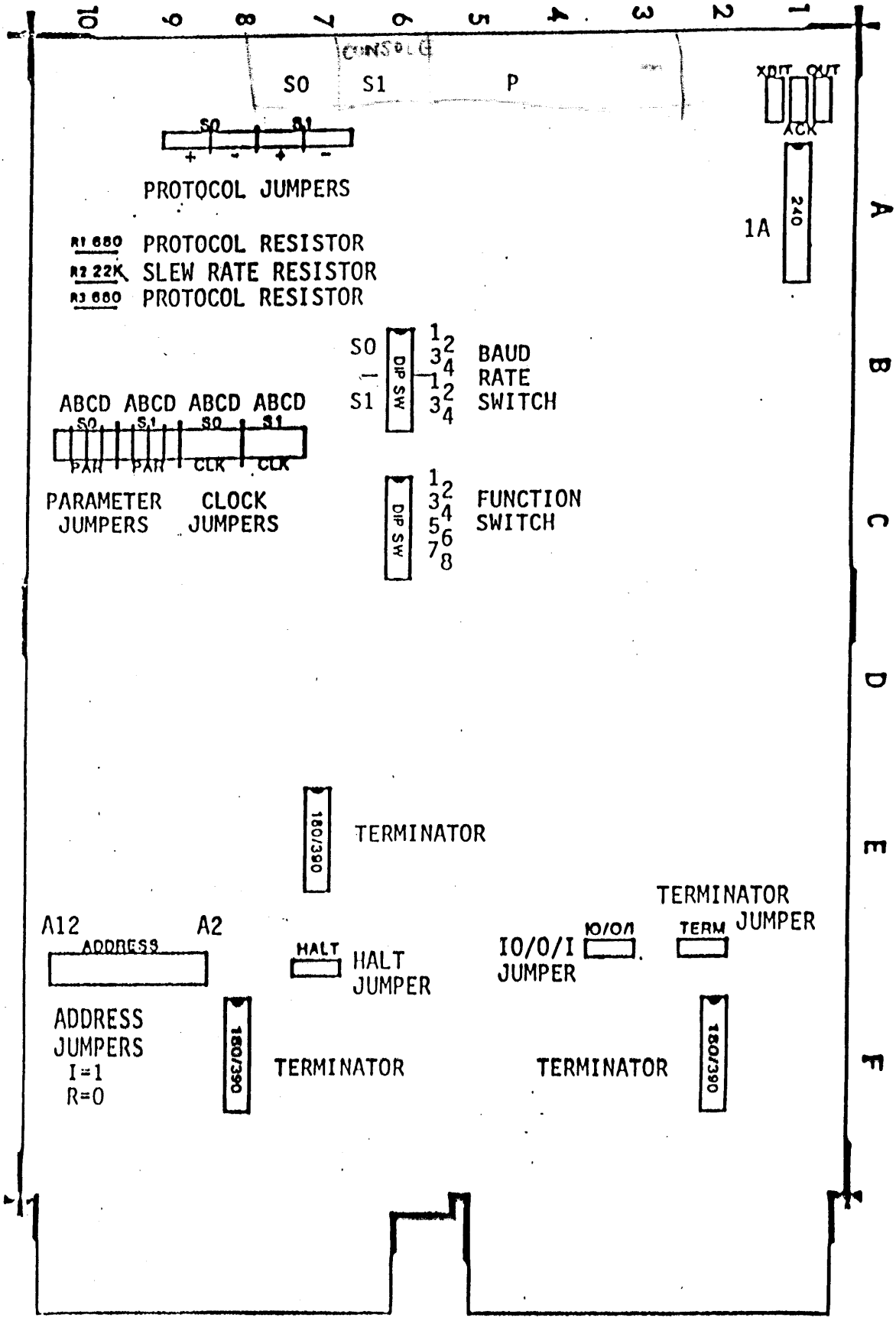
RF	0	0	0	0	0	0	0	TR	TIE	0	0	0	0	0	TF

Bits	Code	Output Status Register Functions	Access
15	RF	Extra Received Bit	read only
8-14	0	not used	read as zero
7	TR	Transmit Ready	read only
6	TIE	Transmit Interrupt Enable	read/write
1-5	0	not used	read as zero
0	TF	Extra Transmitted Bit	read/write

0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

Bits	Code	Output Buffer Register Functions	Access
8-15	0	not used	read as zero
0-7	D	Data	write only

FIGURE 2 JUMPER AND SWITCH LOCATION



PARTS LIST

WITHOUT BOOTSTRAP AND TERMINATION

QUANTITY	PART NUMBER	DESCRIPTION
10	0.047UF	bypass capacitor
1	3.3UF	filter capacitor
3	39UF	filter capacitor
1	0.1UF	filter capacitor
2	82PF	timing capacitor
1	470PF	timing capacitor
2	.47UF	charge pump capacitor
2	680 OHM	resistor
2	12K OHM	resistor
1	22K OHM	resistor
2	27K OHM	resistor
2	100 or 680 OHM	resistor
1	330 OHM x 15	resistor network
1	1K OHM x 15	resistor network
3	1N914B	diode
1	5.0688MHz	crystal
1	5036	baud generator
	or	
1	K1135	Hybrid baud generator
1	0.5A @ 12V	fuse
1	74LS00	quad nand gate
1	74LS08	quad and gate
1	74LS10	tri nand gate
2	74LS32	quad or gate
2	74LS74	dual flip-flop
3	74LS155	dual decoder
1	74LS175	quad flip-flop
1	74LS221	dual monostable multivibrator
1	74LS240	octal buffer
1	74LS240/244	octal buffer
4	74LS244	octal buffer
2	74LS273	octal latch
3	74LS367	hex driver
2	HD6402	UART
2	6331	32x8 open-collector PROM
2	6300	256x4 open-collector PROM
1	6309	256x8 tri-state PROM
1	75452	dual nand open-collector buffer
1	9636	RS-422 driver
1	9637	RS-422/423/232C receiver
1	9638	RS-423/232C driver
1	DS0026	charge pump driver
3	DC003	DEC interrupt logic chip
1	DC004	DEC protocol logic chip
4	DC005	DEC transceiver logic chip
2	8-position	DIP-switch

2	10316-01-445	16-pin socket
2	10320-01-445	20-pin socket
2	87567-1	10-pin header
1	87567-9	26-pin header

WITH BOOTSTRAP

plus

QUANTITY	PART NUMBER	DESCRIPTION
2	6309	256x8 tri-state PROM
2	10320-01-445	20-pin socket

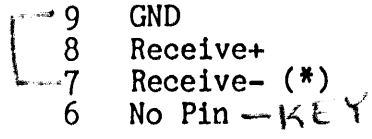
WITH TERMINATION

plus

QUANTITY	PART NUMBER	DESCRIPTION
3	180/390	termination
3	10316-01-445	16-pin socket

CONNECTOR PIN-OUT

SERIAL PORT



1	External Clock	10	+12V
2	GND	9	GND
3	Transmit+	8	Receive+
4	Transmit-	7	Receive- (*)
5	GND	6	No Pin — KEY

* Pin 7 should be grounded externally for RS-232C and RS-423

PARALLEL PORT

1	GND	26	GND
2	Output 0	25	Input 0
3	Output 1	24	Input 1
4	Output 2	23	Input 2
5	Output 3	22	Input 3
6	Output 4	21	Input 4
7	Output 5	20	Input 5
8	Output 6	19	Input 6
9	Output 7	18	Input 7
10	GND	17	GND
11	Request Output	16	Acknowledge Input
12	Acknowledge Output	15	Request Input
13	Extra Received Bit	14	Extra Transmitted Bit

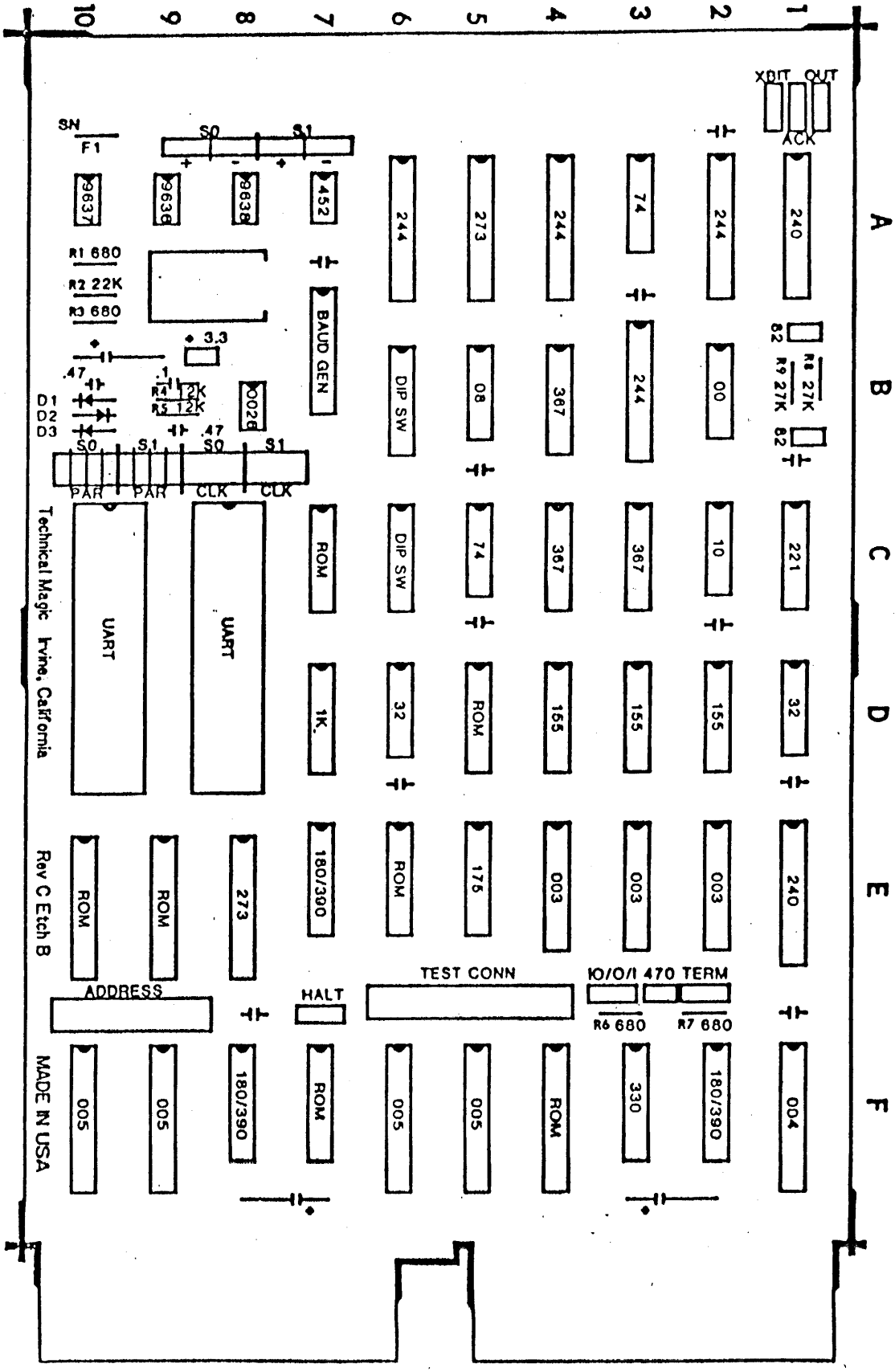
DATA PRODUCTS PRINTER PORT

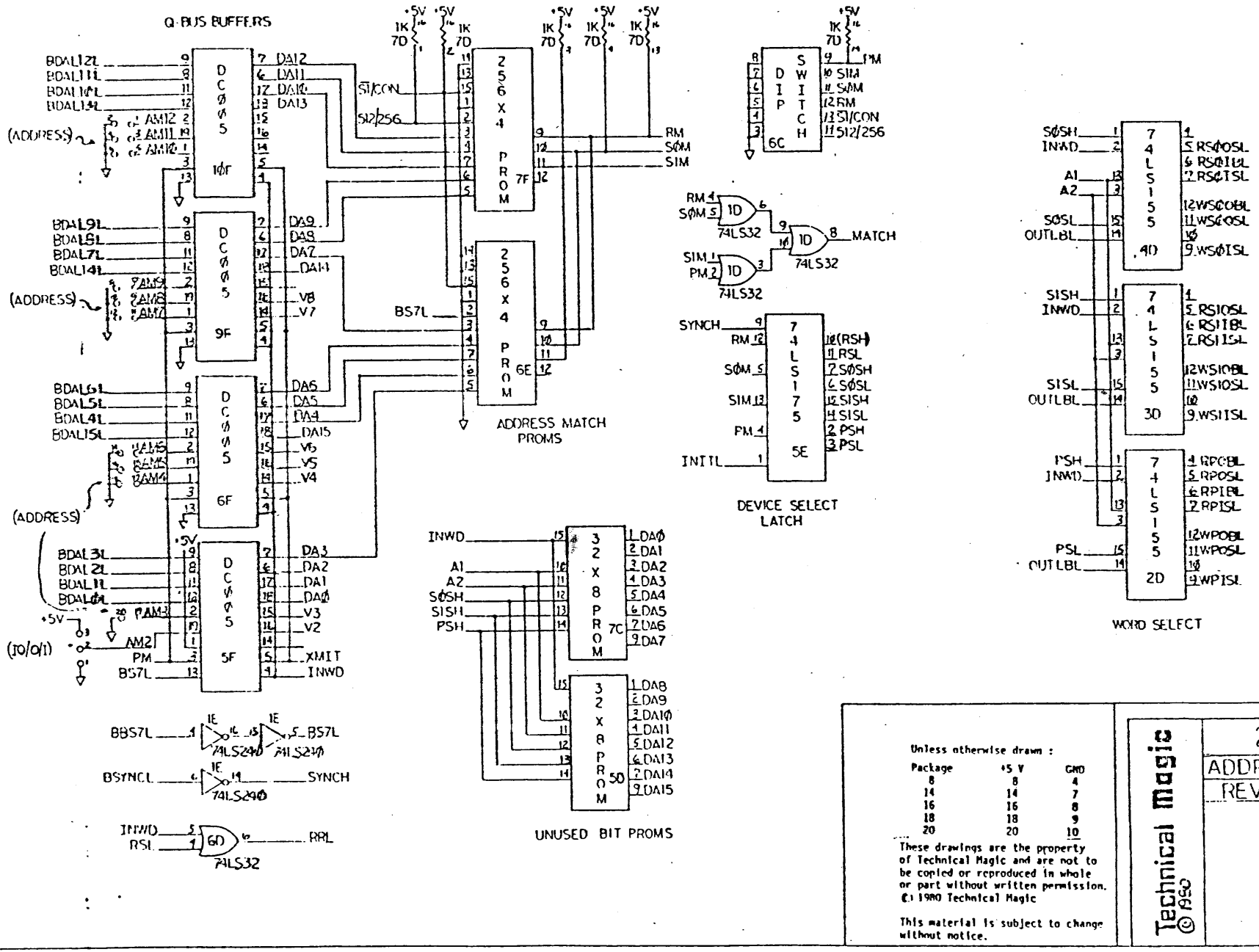
1	GND	26	NC
2	Data 1	25	NC
3	Data 2	24	NC
4	Data 3	23	NC
5	Data 4	22	NC
6	Data 5	21	NC
7	Data 6	20	NC
8	Data 7	19	NC
9	Data 8	18	NC
10	GND	17	NC
11	Demand	16	NC
12	Data Strobe	15	NC
13	Ready	14	NC

CENTRONICS PRINTER PORT

1	GND ——	16	
2	Data 1 ——	2	
3	Data 2 ——	3	
4	Data 3 ——	4	
5	Data 4 ——	5	
6	Data 5 ——	6	
7	Data 6 ——	7	
8	Data 7 ——	8	
9	Data 8 ——	9	
10	GND ——	17	
11	Acknlg ——	10	
12	Data Strobe ——	1	
13	Busy ——	11	
14	Input Prime ——	31 ?	
15	NC		
16	NC		
17	NC		
18	NC		
19	NC		
20	NC		
21	NC		
22	NC		
23	NC		
24	NC		
25	NC		
26	NC		

BOARD LAYOUT





Unless otherwise drawn :

Package	+5 V	GND
8	8	4
14	14	7
16	16	8
18	18	9
20	20	10

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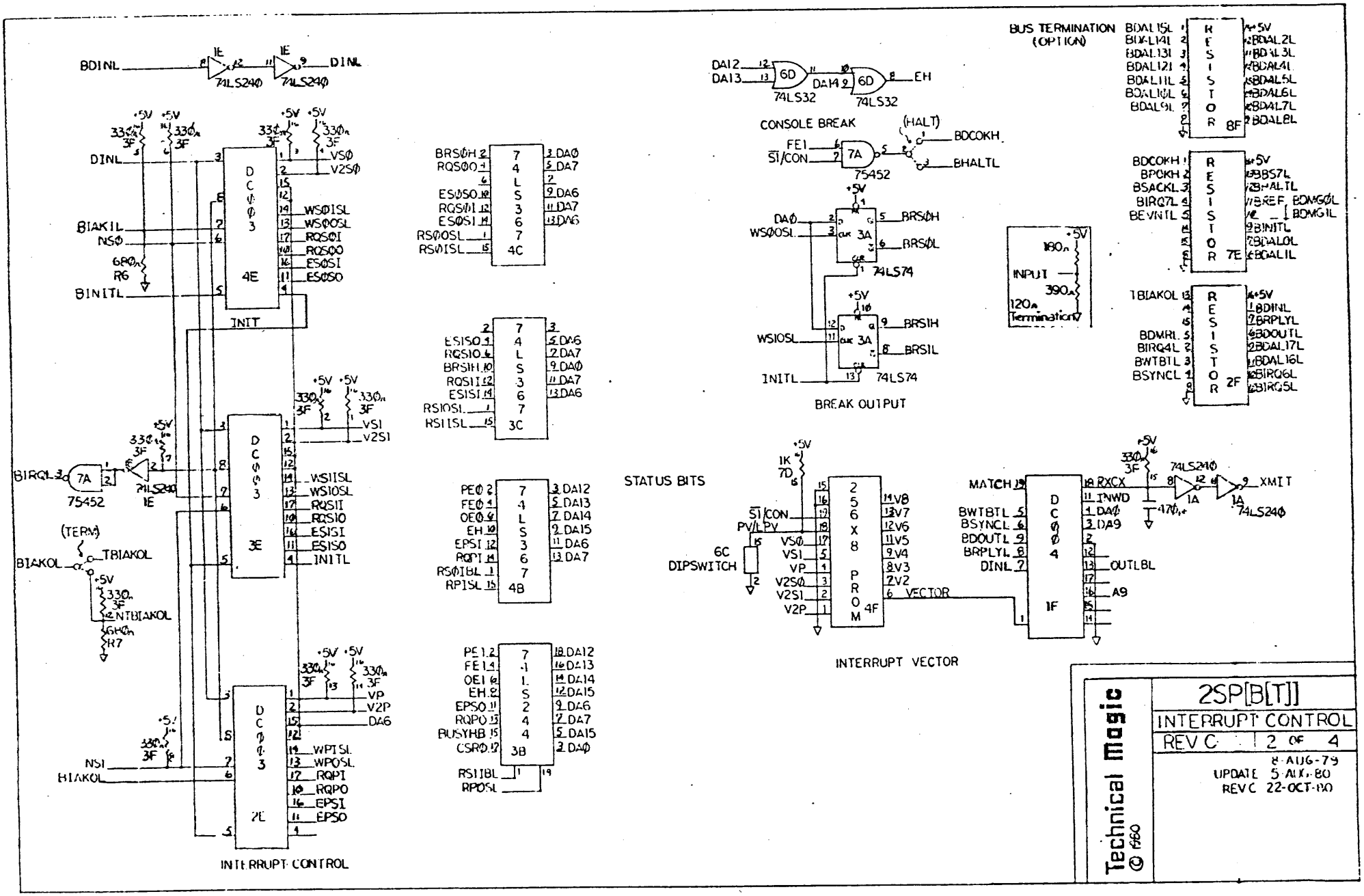
2SP[B[T]]

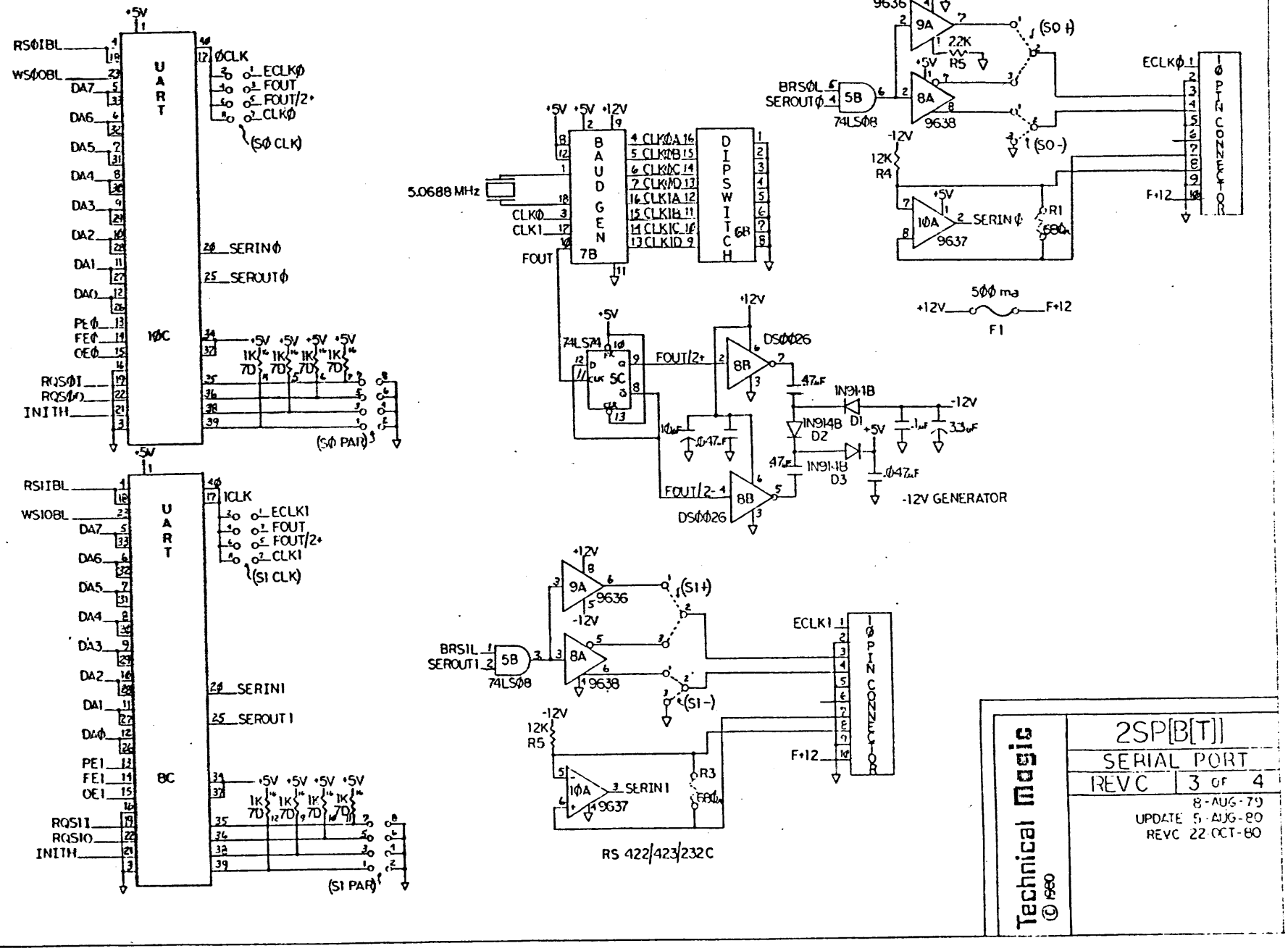
ADDRESS MATCH

REVC | 1 OF 4

8-AUG-79

UPDATE 5 AUG 81
REVC 22 OCT 81


BDINL
74LS240
DINL
INIT
INTERRUPT CONTROL
BUS TERMINATION (OPTION)
CONSOLE BREAK
(HALT)
BREAK OUTPUT
STATUS BITS
INTERRUPT VECTOR
Technical Magic
2SP[B[T]]
INTERRUPT CONTROL
REV C
2 OF 4
8-AUG-79
UPDATE 5-AUG-80
REV C 22-OCT-80



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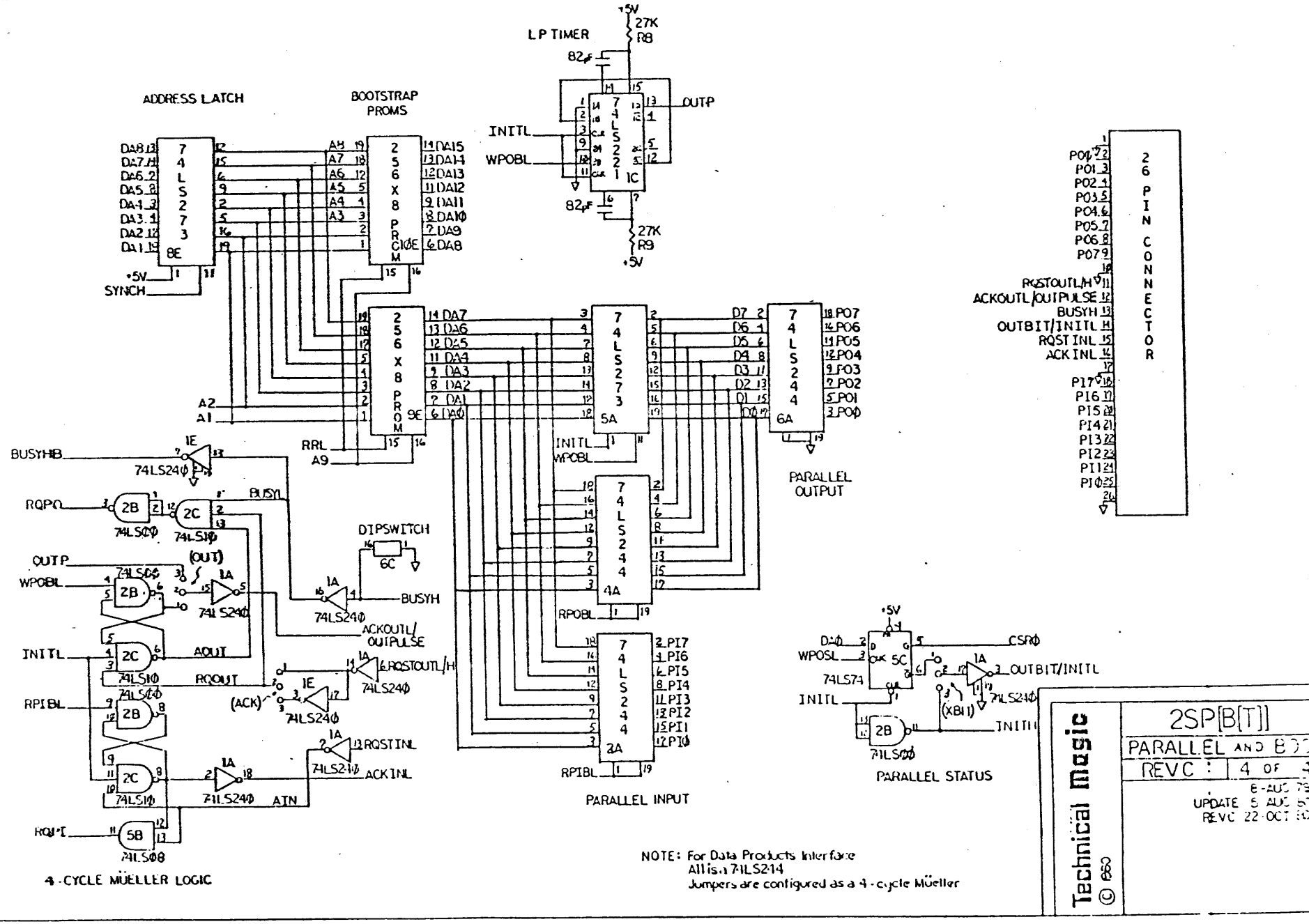
2SP[B[T]]

SERIAL PORT

REV C | 3 OF 4

8-AUG-79
UPDATE 5-AUG-80
REV C 22-OCT-80


ADDRESS LATCH
BOOTSTRAP PROMS
LP TIMER
+5V
27K R8
82pF
OUTP
INITL
WPOBL
82pF
27K R9
+5V
DA8 DA7 DA6 DA5 DA4 DA3 DA2 DA1
74LS273 8E
+5V SYNCH
A11 A7 A6 A5 A4 A3
256X8 PROM 9E
DA15 DA14 DA13 DA12 DA11 DA10 DA9 DA8
A2 A1
RRL A9
DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0
74LS273 5A
INITL WPOBL
D7 D6 D5 D4 D3 D2 D1 D0
74LS244 6A
PO7 PO6 PO5 PO4 PO3 PO2 PO1 PO0
PARALLEL OUTPUT
26 PIN CONNECTOR
PO0 PO1 PO2 PO3 PO4 PO5 PO6 PO7
RQSTOUTL/H
ACKOUTL/OUTPULSE
BUSYH
OUTBIT/INITL
RQSTINL
ACKINL
PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0
74LS244 4A
RPOBL
74LS244 2A
RPIBL
PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0
PARALLEL INPUT
BUSYHB
1E 74LS240
RQPO
2B 74LS00
2C 74LS10
BUSY
DIPSWITCH 6C
OUTP
WPOBL
(OUT)
1A 74LS240
BUSYH
ACKOUTL/ OUTPULSE
INITL
2C 74LS10
AOUT
RQOUT
RPIBL
2B 74LS00
(ACK)
1E 74LS240
1A 74LS240 RQSTOUTL/H
1A 74LS240 RQSTINL
2C 74LS10
1A 74LS240 AIN
ACKINL
RQPI
5B 74LS08
4-CYCLE MÜELLER LOGIC
+5V
D4 WPOSL
5C 74LS74
INITL
CSR0
1A 74LS240 OUTBIT/INITL
(XBII)
2B 74LS00 INITI
PARALLEL STATUS
NOTE: For Data Products Interface
All is a 74LS244
Jumpers are configured as a 4-cycle Müeller
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2SP[B[T]]
PARALLEL AND B
REVC : 4 OF
UPDATE 5 AUG
REVC 22 OCT

FOUR-CYCLE MUELLER HANDSHAKE PROTOCOL

Four-cycle Mueller handshake is an asynchronous communication protocol. A data transfer from one device to another requires two control lines and a data path. At each device, one control signal is an input and one control signal is an output. At the device receiving data, the output control signal is designated Input Acknowledge and the input control signal is called Input Request. At the device transmitting data, the output control signal is designated Output Request and the input control signal is called Output Acknowledge. To connect the transmitting device to the receiving device Input Acknowledge is tied to Output Request while Output Acknowledge is tied to Input Request. All of these control signals are active (asserted) at a logic low level except Input Acknowledge, which is active high. This exception makes possible the operation of this communication protocol.

Figure 3a shows a sample of two devices communicating via four-cycle Mueller handshake. The following is a step by step description of a data transfer from the transmitting device on the left to the receiving device on the right. The two controlling signals are labelled A and B and a timing diagram is shown in Figure 3b.

(1) Request Data Transmission

In the initial state, all outputs are inactive and no data is being passed. Since Input Acknowledge is low in the inactive state and is tied to Output Request, Output Request is asserted and the transmitting device is requested to generate data.

	TRANSMITTING DEVICE		RECEIVING DEVICE	
CONTROL	SIGNAL NAME	STATE	SIGNAL NAME	STATE
A LOW	Output Request	ACTIVE	Input Acknowledge	INACTIVE
B HIGH	Output Acknowledge	INACTIVE	Input Request	INACTIVE

(2) Request Data Reception

After the transmitting device places valid data on the data lines, the transmitting device asserts Output Acknowledge and therefore also asserts Input Request at the receiving device.

	TRANSMITTING DEVICE		RECEIVING DEVICE	
CONTROL	SIGNAL NAME	STATE	SIGNAL NAME	STATE
A LOW	Output Request	ACTIVE	Input Acknowledge	INACTIVE
B LOW	Output Acknowledge	ACTIVE	Input Request	ACTIVE

(3) End Data Reception

After the receiving device accepts data it asserts Input Acknowledge which thereby negates Output Request.

	TRANSMITTING DEVICE		RECEIVING DEVICE	
CONTROL	SIGNAL NAME	STATE	SIGNAL NAME	STATE
A HIGH	Output Request	INACTIVE	Input Acknowledge	ACTIVE
B LOW	Output Acknowledge	ACTIVE	Input Request	ACTIVE

(4) End Data Transmission

The inactive Output Request then causes the transmitting device to remove data from the data lines and to negate Output Acknowledge which thereby negates Input Request at the receiving device. The data transfer is now complete.

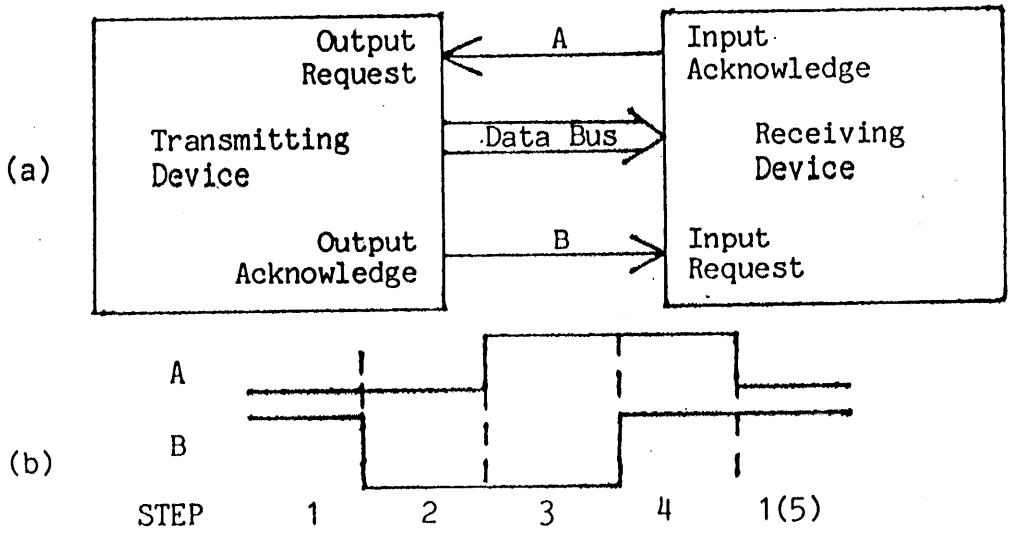
	TRANSMITTING DEVICE		RECEIVING DEVICE	
CONTROL	SIGNAL NAME	STATE	SIGNAL NAME	STATE
A HIGH	Output Request	INACTIVE	Input Acknowledge	ACTIVE
B HIGH	Output Acknowledge	INACTIVE	Input Request	INACTIVE

(5) Repeat Step (1)

The inactive Input Request at the receiving device then negates Input Acknowledge. Output Request is thereby asserted and another data transmission request cycle is initiated.

	TRANSMITTING DEVICE		RECEIVING DEVICE	
CONTROL	SIGNAL NAME	STATE	SIGNAL NAME	STATE
A LOW	Output Request	ACTIVE	Input Acknowledge	INACTIVE
B HIGH	Output Acknowledge	INACTIVE	Input Request	INACTIVE

FIGURE 3 FOUR-CYCLE MUELLER HANDSHAKE



SPECIFICATIONS

Name	Two Serial and One Parallel Ports with Bootstrap and Terminator
Identification	2SP[B[T]]
Dimensions	Dual-width card 5.187x8.5" (13.18x21.6cm)
Power requirements	2A @ 5V without termination 3A @ 5V with termination 100mA @12V
Operating temperature	0 to 50 Celsius 32 to 122 Fahrenheit
Serial communication rate	50, 75, 110,134.5, 150 300, 600, 1200, 1800, 2000 2400, 3600, 4800, 7200, 9600 19200,38400,76800 baud with external clock capability
Serial interface	EIA RS-232C, RS-423 or RS422
Parallel interface	four-cycle Mueller
Printer interface	Centronics or Data Products
Parallel output driver Sink current Source current	 24mA @ 0.5A -15mA @ 2.4A
Parallel input receiver Sink current Source current Hysteresis	 -200UA 20UA 200mV
Bus load	1
Construction	4 layer epoxy glass

WARRANTY

Technical Magic warrants to the original purchaser (Customer) of this Product that it is free from defects in materials and workmanship and meets the specifications applicable at time of manufacture. If any failure to meet specifications occurs within one (1) year of original purchase, Customer should contact Technical Magic by mail or telephone to obtain a Repair Number and then return Product, shipping prepaid, to Technical Magic. At its sole expense, Technical Magic will either repair or replace the defective Product and return it, shipping prepaid, to the Customer. Technical Magic's liability, to the extent allowed by law, shall be limited solely to replacement of Product, and this Warranty does not apply to any Product that has been abused, misused, or damaged.

Any Product not covered above may be returned to Technical Magic for prompt repair or refurbishment at our current Service Rate. Contact Technical Magic for further information.