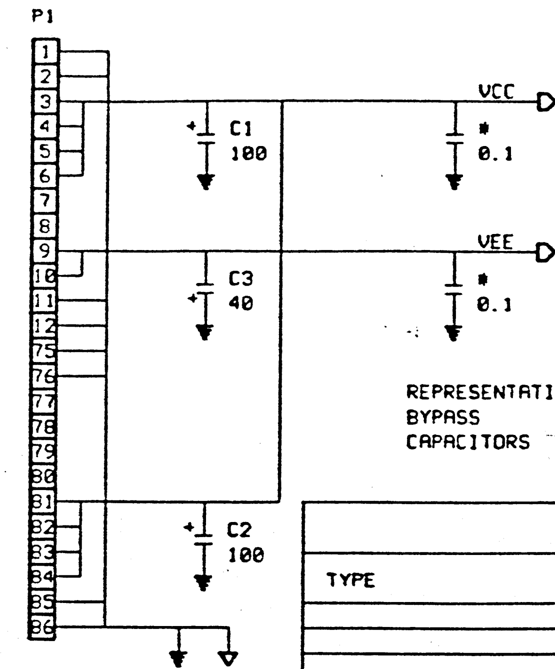
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	B	REVISE PER ECO # 776	7-6-86	[illegible]
	C	REV ECO # 1154	5/26/87	[illegible]

REFERENCE FILE

I.C. LEGEND

TYPE	CNT	GND	VCC	REFERENCE DESIGNATORS
7407	1	7	14	U29
74HC132	1	7	14	U102
74LS148	1	8	16	U9
74LS153	1	8	16	U116
74LS175	1	8	16	U80
74LS273	2	10	20	U113 U114
74LS365	1	8	16	U175
74LS366	2	8	16	U111 U112
74LS368	1	8	16	U123
74LS393	4	7	14	U1 U14 U144 U145
74LS652	12	12	24	U56-U59 U61-U68
74S244	1	10	20	U3
74F00	2	7	14	U50 U52
74F02	4	7	14	U34 U54 U78 U79
74F04	3	7	14	U28 U109 U124
74F10	2	7	14	U13 U99
74F20	2	7	14	U75 U115
74F32	1	7	14	U98
74F64	2	7	14	U73 U74
74F74	6	7	14	U25 U53 U55 U60 U77 U125
74F138	5	8	16	U70 U96 U100 U103 U104
74F174	1	8	16	U119
74F175	2	8	16	U81 U101
74F240	3	10	20	U146 U147 U148
74F245	4	10	20	U161 U162 U163 U164
74F374	4	10	20	U170 U171 U172 U173
74ALS244A	2	10	20	U110 U122
74ALS534	2	10	20	U30 U31
74ALS540	9	10	20	U5 U6 U7 U149 U165 U166 U167 U168 U169
74ALS541	10	10	20	U24 U51 U105 U106 U107 U108 U134 U135 U155 U156
74ALS640A	3	10	20	U10 U11 U12
74ALS645A	4	10	20	U120 U121 U138 U139
74AS30	1	7	14	U88
74AS652	4	12	24	U140-U143
PAL16L8A	2	10	20	U4 U27
PAL16L8A-2	6	10	20	U8 U85 U86 U89 U90 U117
PAL16L8-15	14	10	20	U35-U41 U71 U72 U83 U97 U136 U137 U174
PAL16R8-15	1	10	20	U82
PAL16R4	1	10	20	U76
PAL16R6-15	1	10	20	U26
PAL16C1	2	10	20	U32 U84
26LS29	3	5	1	U129 U133 U154
26LS32	5	8	16	U128 U150 U151 U152 U153
29824	1	12	24	U33
68020-16	1	*	*	U127
68681	2	20	40	U130 U131
146818A	1	12	24	U69
27256-20	4	14	28	U91 U92 U93 U94
27S29	1	10	20	U118
2148	4	9	18	U157 U158 U159 U160
MCM2016H-70	1	12	24	U95
1400-35	17	10	20	U15-U23 U42-U49
K1114 32MHZ	1	7	14	U126
K1114 8MHZ	1	7	14	U2



REPRESENTATIVE BYPASS CAPACITORS

DISCRETE LEGEND

TYPE	DESCRIPTION	CNT	REFERENCE DESIGNATORS
	33 OHM RESISTOR	2	R1 R18
	100 OHM RESISTOR	1	R4
	470 OHM RESISTOR	2	R12 R14
	680 OHM RESISTOR	2	R13 R15
	1K OHM RESISTOR	4	R9 R11 R16 R17
	2.2K OHM RESISTOR	2	R8 R10
	10K OHM RESISTOR	1	R6
	100K OHM RESISTOR	1	R5
	470K OHM RESISTOR	2	R2 R7
	22M OHM RESISTOR	1	R3
MSP06A01-101G	100 OHM PULLUP 6-PIN	1	RN5
MSP06A01-271G	270 OHM PULLUP 6-PIN	1	RN15
MSP10A01-222G	2.2K OHM PULLUP 10-PIN	2	RN1 RN7
MSP06A01-472G	4.7K OHM PULLUP 6-PIN	4	RN3 RN6 RN8 RN9
MSP10A01-472G	4.7K OHM PULLUP 10-PIN	4	RN2 RN4 RN13 RN14
MSP06A01-103G	10K OHM PULLUP 6-PIN	2	RN10 RN11
MSP08A01-103G	10K OHM PULLUP 8-PIN	1	RN12
SR151A100KAA	10 PF CAPACITOR	2	C7 C19
SR151A220KAA	22 PF CAPACITOR	1	C8
SR151A221KAA	220 PF CAPACITOR	11	C6 C9-C18
SR151A471KAA	470 PF CAPACITOR	1	C21
A5E104M	0.1 UF CAPACITOR	147	*
A5E104M	0.1 UF CAPACITOR	2	C4 C5
	10 UF CAPACITOR	1	C20
	40 UF CAPACITOR	1	C3
	100 UF CAPACITOR	2	C1 C2
1N914	SIGNAL DIODE	2	CR1 CR2
1N3595	SCHOTTKY DIODE	1	CR3
1N270	SCHOTTKY DIODE	1	CR4
555-4001	LED ARRAY	1	DS1
	32.768 KHZ CRYSTAL	1	Y1
	3.686 MHZ CRYSTAL	1	Y2
	16 PIN DIP SWITCH	2	S1 S2
LTC-7P	BATTERY	1	BT1

UNLESS OTHERWISE SHOWN:

1. RESISTANCE VALUES ARE IN OHMS
2. CAPACITANCE VALUES ARE IN MICROFARADS

APPLICATIONS				
-02	5000-561-XX	MULTI-USE	drw	
			chk K. Abele	4/7/86
			iss. K. Abele	4/7/86
DASH NO.	NEXT ASSEMBLY	USED ON	APPROVALS	DATE

SILICON GRAPHICS INC.

PCB SCHEMATIC, IP2

NOM.	DRAWING NUMBER	REV		
IP2	5000-558	C	14.NOV.1985	1.OF.20

P1. CONNECTIONS		
PIN	SIGNAL. NAME	SHEET
13	BBCLK\	18
14	BINIT\	10
15	BBPRN\	18
16	BBPRO\	18
17	BBUSY\	18
18	BBRE0\	18
19	BMRDC\	18
20	BMWTC\	18
21	BIORC\	18
22	BIOWC\	18
23	BXACK\	18
24		NC
25		NC
26		NC
27	BBHEN\	19
28	BA16\	19
29	BCBR0\	16
30	BA17\	19
31	BCCLK\	18
32	BA18\	19
33		NC
34	BA19\	19
35	BBINT6\	4
36	BBINT7\	4
37	BBINT4\	4
38	BBINT5\	4
39	BBINT2\	4
40	BBINT3\	4
41	BBINT0\	4
42	BBINT1\	4
43	BA14\	19
44	BA15\	19
45	BA12\	19
46	BA13\	19
47	BA10\	19
48	BA11\	19
49	BA8\	19
50	BA9\	19
51	BA6\	19
52	BA7\	19
53	BA4\	19
54	BA5\	19
55	BA2\	19
56	BA3\	19
57	BA0\	19
58	BA1\	19
59	BD14\	20
60	BD15\	20
61	BD12\	20
62	BD13\	20
63	BD10\	20
64	BD11\	20
65	BD8\	20
66	BD9\	20
67	BD6\	20
68	BD7\	20
69	BD4\	20
70	BD5\	20
71	BD2\	20
72	BD3\	20
73	BD0\	20
74	BD1\	20

NOTE: .P1. PINS. 1-12. AND. 75-86. ON. PAGE. 1

J1. CONNECTIONS		
PIN	SIGNAL. NAME	SHEET
1	DCD0\	6
2		NC
3	TXD0\	6
4	DTR0\	6
5	RXD0\	6
6		NC
7	JHALT\	4
8		NC
9		NC
10		NC
11		NC
12		NC
13	GND	6
14	DCD2\	7
15	CTS2\	7
16	RTS2\	7
17	TXD2\	7
18	RXD2\	7
19	DTR2\	7
20	DCD3\	7
21	CTS3\	7
22	RTS3\	7
23	TXD3\	7
24	RXD3\	7
25	DTR3\	7
26		NC
27		NC
28	TXD1\	6
29		NC
30	RXD1\	6
31		NC
32		NC
33		NC
34		NC
35	DCD1\	6
36	DTR1\	6
37	JDIAG0	10
38	GND	6
39	JDIAG1	10
40	JDIAG2	10
41	JDIAG3	10
42	CONF0	10
43	CONF1	10
44	CONF2	10
45	CONF3	10
46	CONF4	10
47	CONF5	10
48	CONF6	10
49	CONF7	10
50		NC
51		NC
52	MB2\	8
53	MB1\	8
54	MB0\	8
55	MX0\	8
56	MX1\	8
57	MY0\	8
58	MY1\	8
59	GND	6
60	NO	3

J2. CONNECTIONS		
PIN	SIGNAL. NAME	SHEET
1	MD0	20
2	MD1	20
3	GND	20
4	MD2	20
5	MD3	20
6	MD4	20
7	MD5	20
8	GND	20
9	MD6	20
10	MD7	20
11	MD8	20
12	MD9	20
13	GND	20
14	MD10	20
15	MD11	20
16	MD12	20
17	MD13	20
18	GND	20
19	MD14	20
20	MD15	20
21	MD16	20
22	MD17	20
23	GND	20
24	MD18	20
25	MD19	20
26	MD20	20
27	MD21	20
28	GND	20
29	MD22	20
30	MD23	20
31	MD24	20
32	MD25	20
33	GND	20
34	MD26	20
35	MD27	20
36	MD28	20
37	MD29	20
38	GND	20
39	MD30	20
40	MD31	20

P2. CONNECTIONS		
PIN	SIGNAL. NAME	SHEET
55	BA22\	19
56	BA23\	19
57	BA20\	19
58	BA21\	19

J3. CONNECTIONS		
PIN	SIGNAL. NAME	SHEET
1	MA2\	19
2	MA3\	19
3	GND	19
4	MA4\	19
5	MA5	19
6	MA6\	19
7	MA7\	19
8	GND	19
9	MA8\	19
10	MA9\	19
11	MA10\	19
12	MA11\	19
13	GND	19
14	MA12\	19
15	MA13\	19
16	MA14\	19
17	MA15\	19
18	GND	19
19	MA16\	19
20	MA17\	19
21	MA18\	19
22	MA19\	19
23	GND	19
24	MA20\	19
25	MA21\	19
26	MA22\	19
27	MA23\	19
28	GND	19
29	MA24\	19
30	MA25\	19
31	GND	17
32	PENAB\	17
33	GND	17
34	MULTIBUS\	17
35	GND	17
36	WRITE3\	17
37	WRITE2\	17
38	WRITE1\	17
39	WRITE0\	17
40	GND	17
41	TRAS\	17
42	GND	17
43	MOE\	17
44	GND	17
45	BAD\	4
46	GND	17
47	GND	17
48	GND	17
49	PERROR\	17
50	GND	17

J5. CONNECTIONS		
PIN	SIGNAL. NAME	SHEET
1	GND	13
2	FPAA0\	13
3	FPAA1\	13
4	GND	13
5	FPAA12\	13
6	FPAA13\	13
7	GND	13
8	FPAA14\	13
9	FPAA15\	13
10	GND	13
11	FPARE0\	13
12	GND	13
13	FPAACK\	13
14	GND	13
15	FPACLK\	13
16	GND	13
17	FPAWRITE	13
18	GND	13
19	FPAERROR\	13
20	GND	13

J5. CONNECTIONS		
PIN	SIGNAL. NAME	SHEET
1	GEDATA0	12
2	GEDATA1	12
3	GEDATA2	12
4	GEDATA3	12
5	GEDATA4	12
6	GEDATA5	12
7	GEDATA6	12
8	GEDATA7	12
9	GEDATA8	12
10	GEDATA9	12
11	GEDATA10	12
12	GEDATA11	12
13	GEDATA12	12
14	GEDATA13	12
15	GEDATA14	12
16	GEDATA15	12
17	GND	12
18	GND	12
19	GND	12
20	GND	12
21	GND	12
22	GND	12
23	JA12\	12
24	GND	12
25	GND	12
26	GND	12
27	REQOUT	12
28	GND	12
29	ACK IN	4
30	GND	12
31		NC
32	GND	12
33		NC
34	GND	12

5000-558	IP2 SCHEMATIC
5000-559	IP2 ARTWORK
5000-560	IP2 FAB. DRAWING
5000-561-xx	IP2 ASSEMBLY. DRAWING
5000-562	IP2 TEST. PROCEDURES
5000-563	IP2 FUNCTIONAL. DESCRIPTION

SILICON GRAPHICS INC.	REV	CONNECTOR. LEGEND	
IP2 5000-558	C	24. OCT. 1985	2. OF. 20

12A1 GEACK
17C1 CMACK
5B5 LOCAL16\
13C1 FPAACK
5D5 PORT16\
18B1 BUSACK\
5B5 LOCALACK\
4C1 VECTORACK\
6D1 7D1 UARTACK\
U75 F20
U73 F64
U74 F64
VCC
RN4 MSP10A01-472G
CLK LO\ 4B8
CLK HI\ 4B8
5B5 PORTB\
16B1 BERR\
RESET\
HALT\
U29 7407
U29 7407
H13
DSACK 0\
DSACK 1\
4A1 CPUCLK
4D1 IPL#\
J1
R4 100
C5 0.1
C4 0.1
R5 100K
CR2 1N914
CR1 1N914
7C1 WDOG
10B1 ENABWDOG
U102 HC132
18A1 SLAVEINIT\
U127 68020-16
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30 A31
DSACK 0 DSACK 1 BERR RESET HALT CDIS CLK AVEC IPL0 IPL1 IPL2 BR BGACK
AS DS R/W ECS OCS RMC DBEN
SIZ0 SIZ1 IPEND FC0 FC1 FC2 BG
DSACK 0\ 19A2
D# 4D1 12D8 15C8 20D8
VA# 4B8 5D8 13C8 14D8 19D8
U109 F04
AS 4C8 12A8 15B8
WRITE 5B8 8B8 11D8 15A8 16B3 18B8
WRITE2 17B8 20B8
FPAWRITE 13B8
AS\ 5D8 17D8
DS\ 5A8 12A8
WRITE\ 6D8 7D8 11D8
SIZE0 17B8 20B8
SIZE1 12B8 17B8 20B8
FC0 4C8
FC1 4C8
FC2 4C8 5D8 8B8 16B3 18B8
RTC RESET 9D8
INIT\ 6D8 7D8 9B8 10A8 12C8 17D8
HALT\ 10D3
INIT 12A8

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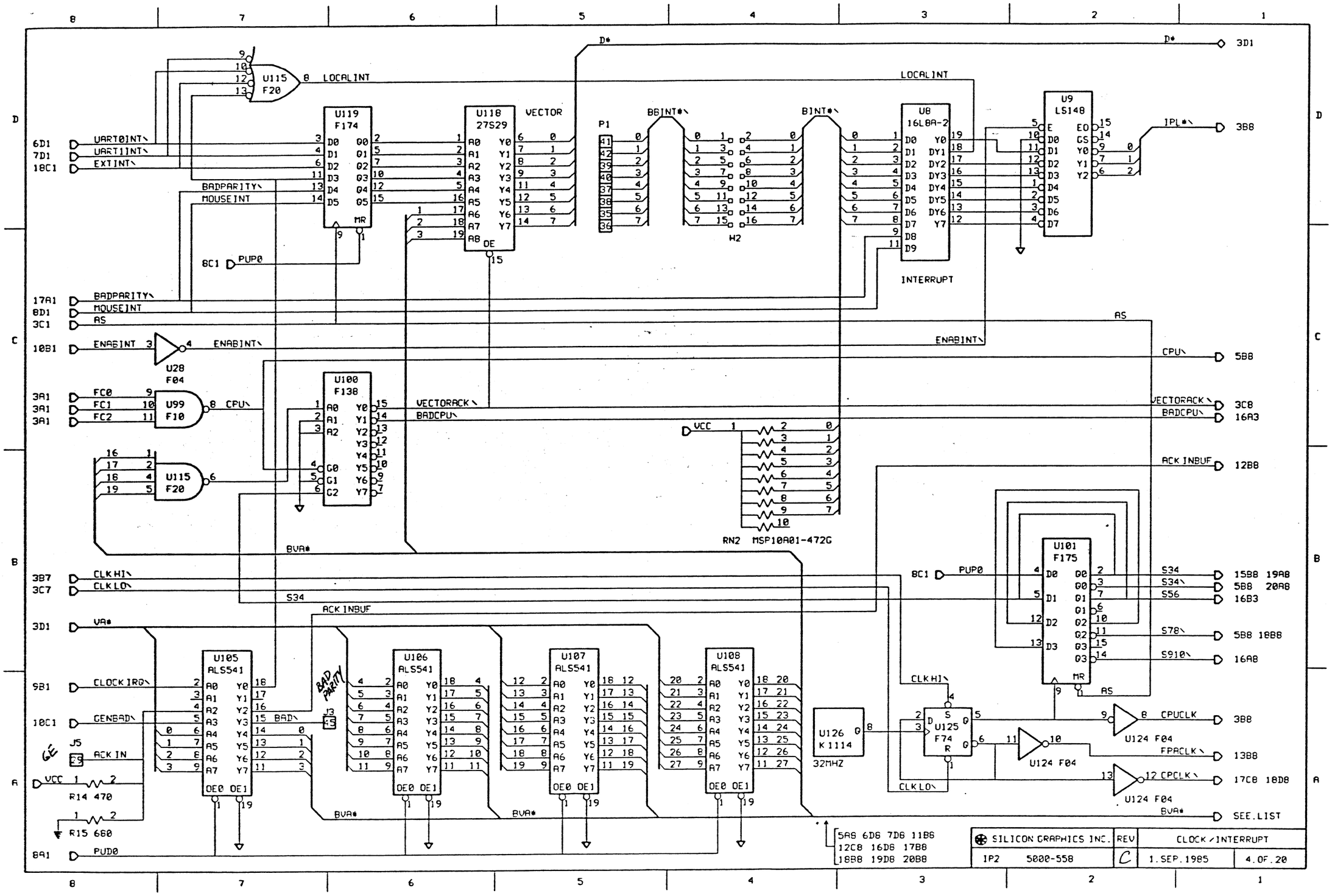
IP2 5000-556	C	1.SEP.1985 3.OF.20


U115 F20
U119 F174
U118 27S29
VECTOR
P1
B6INT#\
B1NT#\
U8 16L8A-2
INTERRUPT
U9 LS148
U28 F04
U99 F10
U100 F138
U101 F175
U105 ALS541
U106 ALS541
U107 ALS541
U108 ALS541
U125 F74
U126 K1114
32MHZ
U124 F04
RN2 MSP10A01-472G
R14 470
R15 680
J5
J3
H2
D*
LOCALINT
UART0INT\
UART1INT\
EXTINT\
BADPARITY\
MOUSEINT
PUP0
AS
ENABINT\
CPU\
VECTORACK\
BADCPU\
ACK INBUF
CLK HI\
CLK LO\
S34
VA*
CLOCK IRQ\
GENBAD\
ACK IN
PUD0
BAD PARITY
BVA*
IPL*\
CPUCLK
FPACLK\
CPCLK\
S34\
S56
S78\
S910\
SEE.LIST
5A8 6D8 7D8 11B6
12C8 16D8 17B8
18B8 19D8 20B8
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REV
C
CLOCK/INTERRUPT
IP2 5000-558
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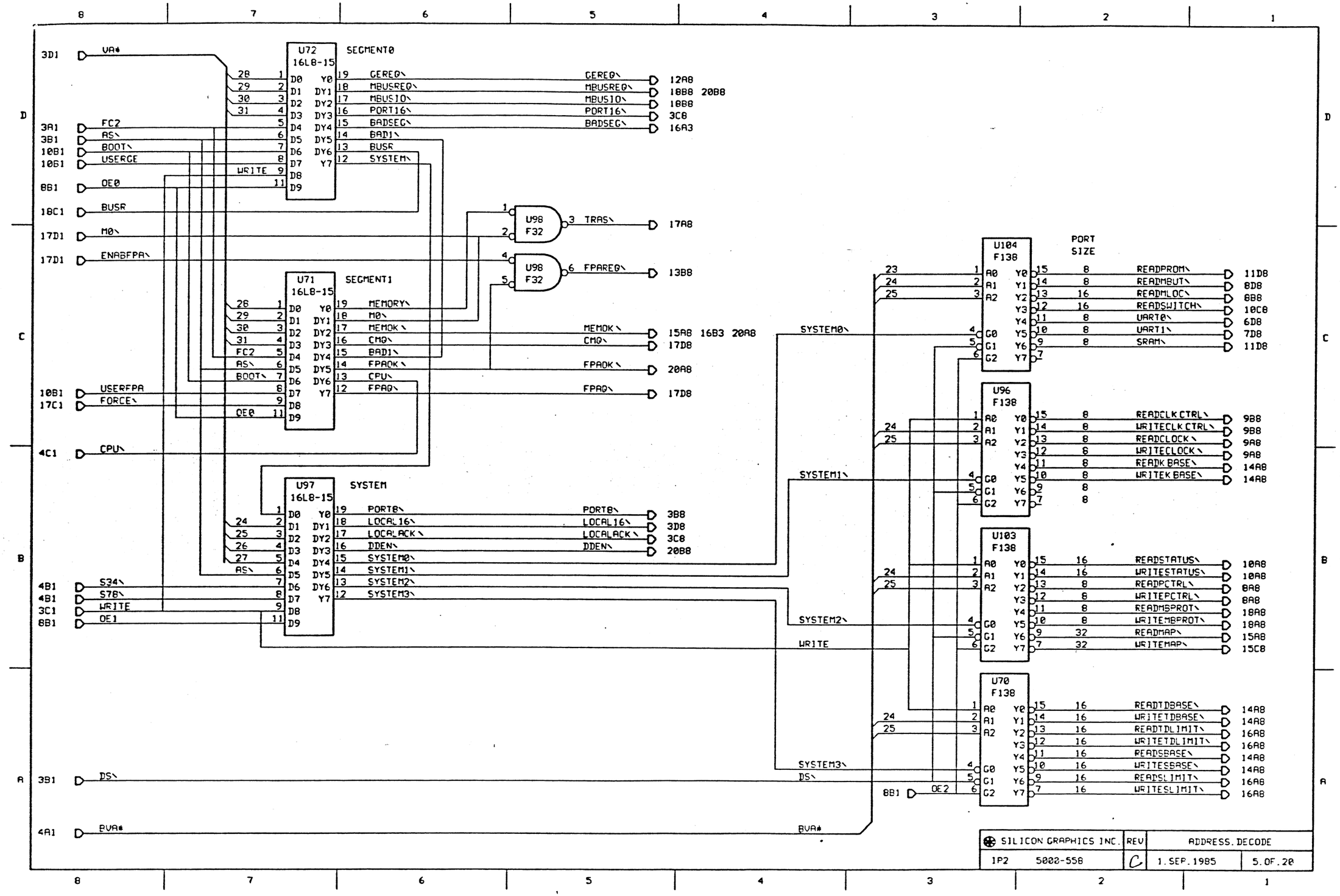
4.OF.20


U72
16L8-15
SEGMENT0
U71
16L8-15
SEGMENT1
U97
16L8-15
SYSTEM
U98
F32
U98
F32
U104
F138
PORT
SIZE
U96
F138
U103
F138
U70
F138
3D1 VA#
3A1 FC2
3B1 AS\
10B1 BOOT\
10B1 USERGE
WRITE
8B1 OE0
18C1 BUSR
17D1 M0\
17D1 ENABFPA\
10B1 USERFPA
17C1 FORCE\
OE0
4C1 CPU\
4B1 S34\
4B1 S78\
3C1 WRITE
8B1 OE1
3B1 DS\
4A1 BVA#
GERE0\ 12A8
MBUSREQ\ 18B8 20B8
MBUSIO\ 18B8
PORT16\ 3C8
BADSEG\ 16A3
TRAS\ 17A8
FPAREQ\ 13B8
MEMOK\ 15A8 16B3 20A8
CM0\ 17D8
FPAOK\ 20A8
FPA0\ 17D8
PORT8\ 3B8
LOCAL16\ 3D8
LOCALACK\ 3C8
DDEN\ 20B8
SYSTEM0\
SYSTEM1\
SYSTEM2\
SYSTEM3\
OE2
READPROM\ 11D8
READMBUT\ 8D8
READMLOC\ 8B8
READSWITCH\ 10C8
UART0\ 6D8
UART1\ 7D8
SRAM\ 11D8
READCLKCTRL\ 9B8
WRITECLKCTRL\ 9B8
READCLOCK\ 9A8
WRITECLOCK\ 9A8
READKBASE\ 14A8
WRITEKBASE\ 14A8
READSTATUS\ 10A8
WRITESTATUS\ 10A8
READPCTRL\ 8A8
WRITEPCTRL\ 8A8
READMBPROT\ 18A8
WRITEMBPROT\ 18A8
READMAP\ 15A8
WRITEMAP\ 15C8
READIDBASE\ 14A8
WRITEIDBASE\ 14A8
READIDLIMIT\ 16A8
WRITEIDLIMIT\ 16A8
READSBASE\ 14A8
WRITESBASE\ 14A8
READSLIMIT\ 16A8
WRITESLIMIT\ 16A8
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1P2 5000-558
C
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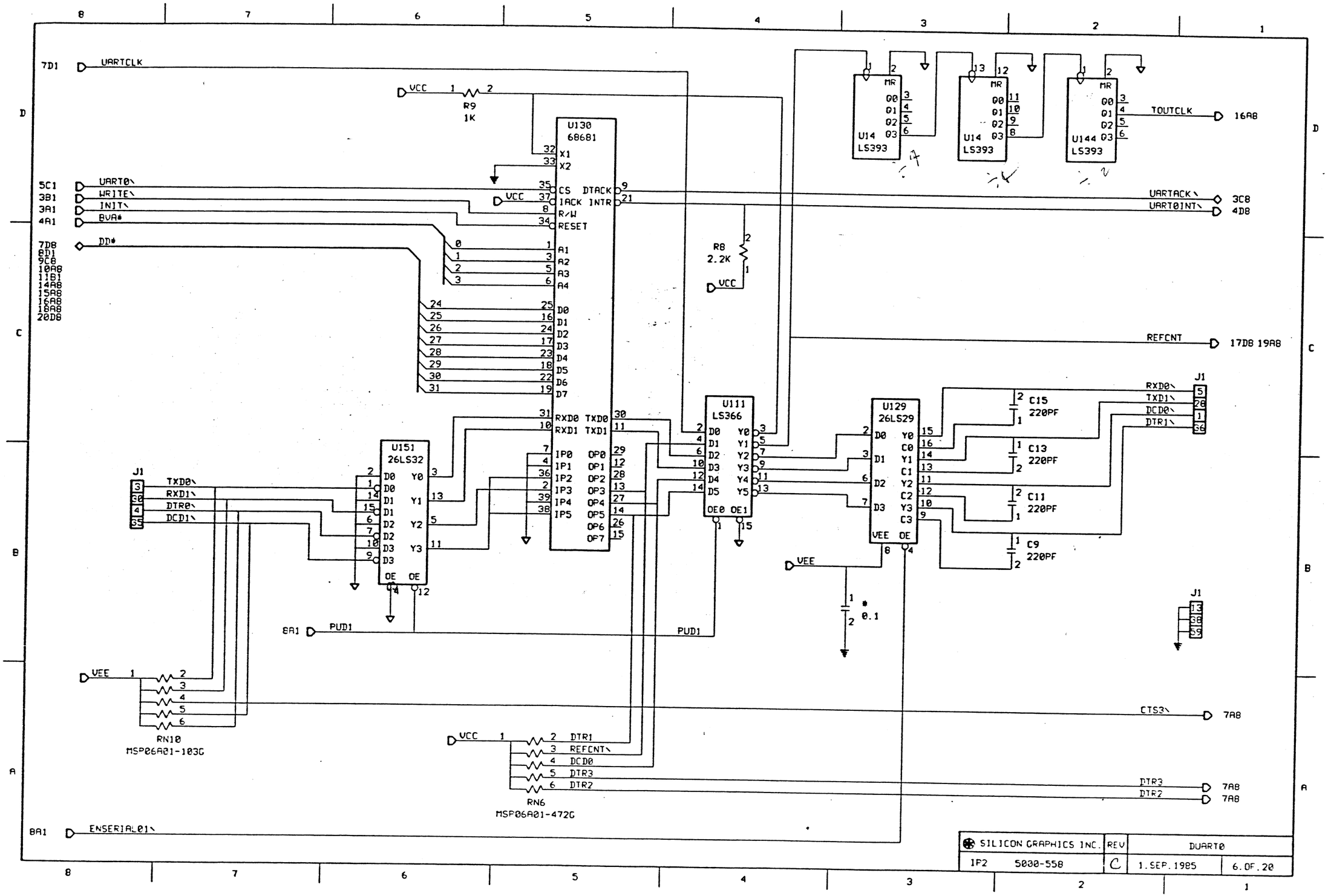
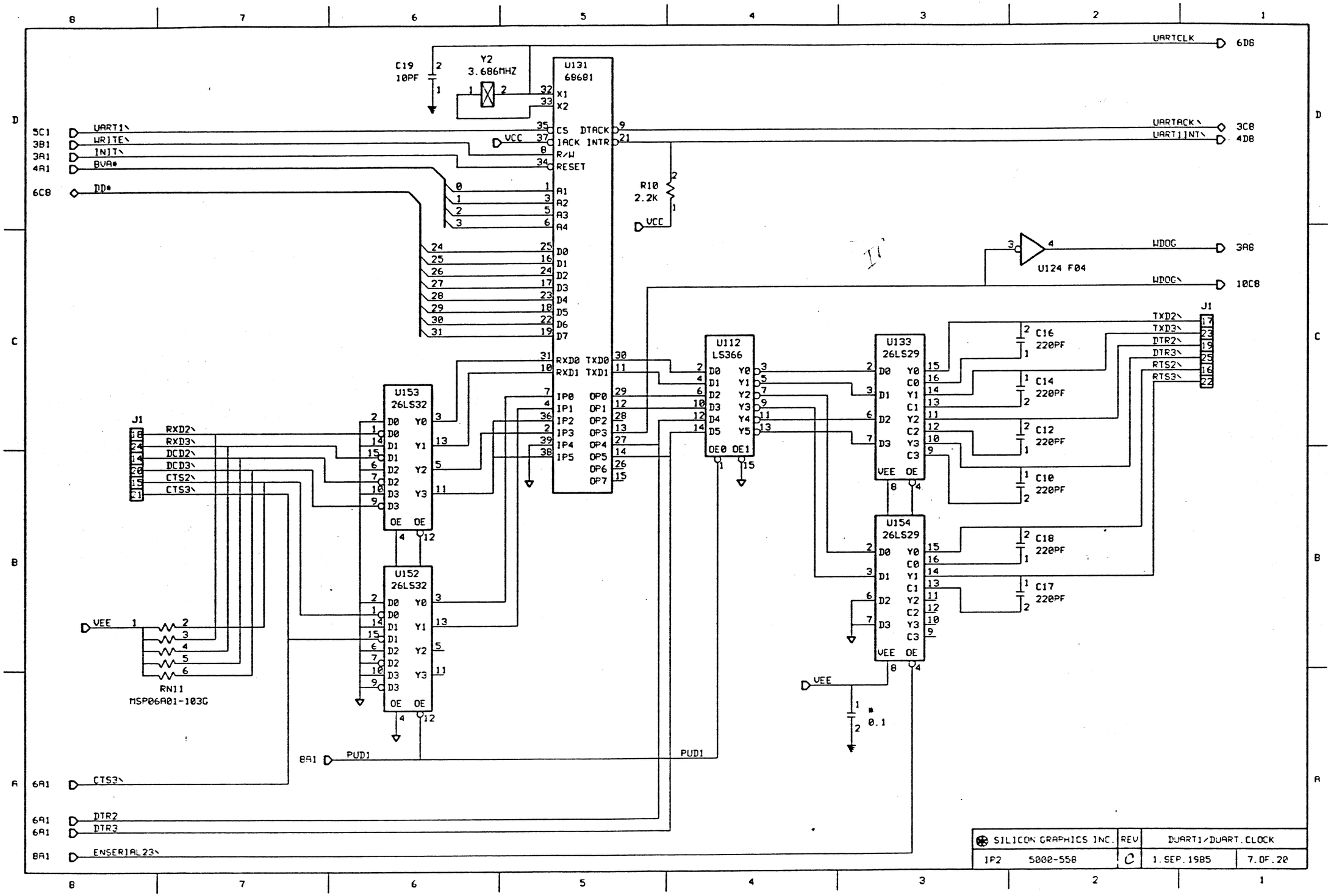
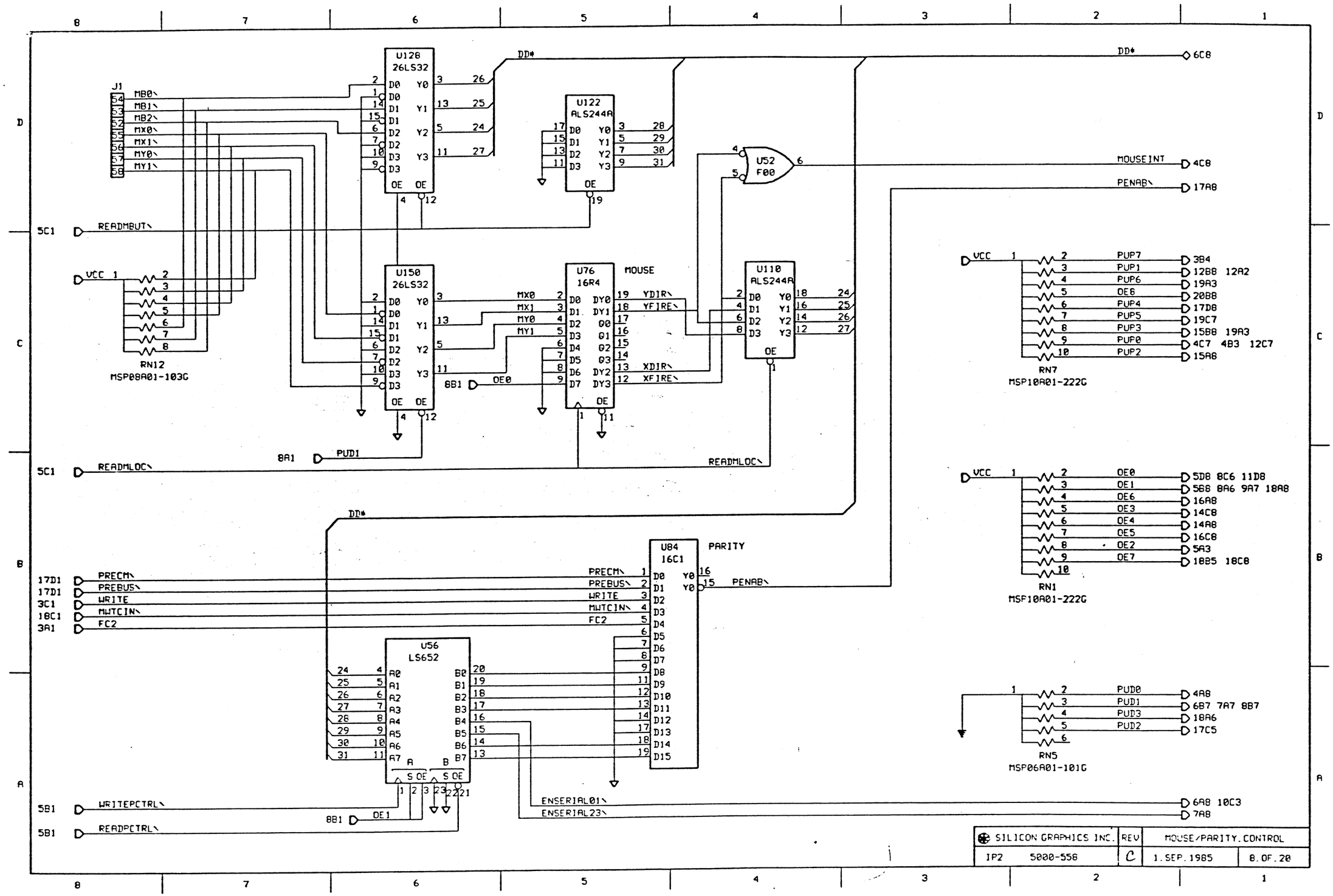
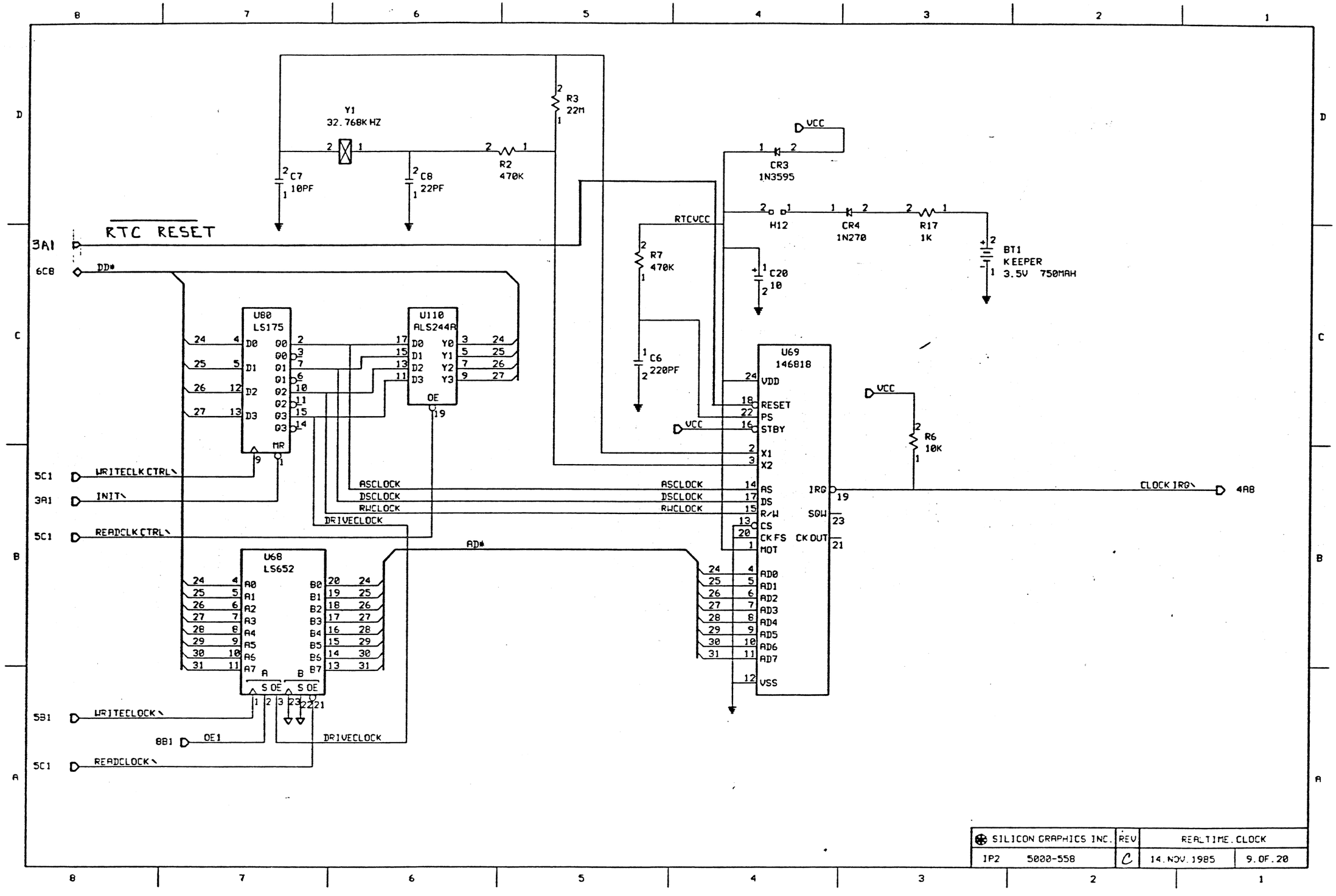
5. OF. 20


7D1 UARTCLK
VCC 1 2 R9 1K
U130 68681
32 X1
33 X2
5C1 UART0\
3B1 WRITE\
3A1 INIT\
4A1 BUA*
35 CS
VCC 37 IACK
8 R/W
34 RESET
DTACK 9
INTR 21
UARTACK\ 3C8
UART0INT\ 4D8
7D8 8D1 9C8 10A8 11B1 14A8 15A8 16A8 18A8 20D8 DD*
0 1 A1
1 3 A2
2 5 A3
3 6 A4
24 25 D0
25 16 D1
26 24 D2
27 17 D3
28 23 D4
29 18 D5
30 22 D6
31 19 D7
R8 2.2K
VCC
U1 U13 U1 MR D0 D1 D2 D3 U14 LS393 U144 LS393
TOUTCLK 16A8
REFCNT 17D8 19A8
31 RXD0 TXD0 30
10 RXD1 TXD1 11
7 4 36 2 39 38 IP0 IP1 IP2 IP3 IP4 IP5
29 12 28 13 27 14 26 15 OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7
U151 26LS32
J1 3 30 4 35 TXD0\ RXD1\ DTR0\ DCD1\
U111 LS366 OE0 OE1
U129 26LS29 C0 C1 C2 C3 VEE OE
C15 220PF
C13 220PF
C11 220PF
C9 220PF
RXD0\ TXD1\ DCD0\ DTR1\
VEE
0.1
8A1 PUD1
PUD1
VEE 1 2 3 4 5 6 RN10 MSP06A01-103G
VCC 1 2 DTR1 3 REFCNT\ 4 DCD0 5 DTR3 6 DTR2 RN6 MSP06A01-472G
CTS3\ 7A8
DTR3 7A8
DTR2 7A8
8A1 ENSERIAL01\
SILICON GRAPHICS INC.
REV C
DUART0
IP2 5000-558
1.SEP.1985
6.OF.20


C19
10PF
Y2
3.686MHZ
U131
68681
X1
X2
CS
IACK
R/W
RESET
DTACK
INTR
A1
A2
A3
A4
D0
D1
D2
D3
D4
D5
D6
D7
RXD0 TXD0
RXD1 TXD1
IP0
IP1
IP2
IP3
IP4
IP5
OP0
OP1
OP2
OP3
OP4
OP5
OP6
OP7
VCC
R10
2.2K
UARTCLK
6D8
UARTACK\
3C8
UARTJINT\
4D8
5C1
3B1
3A1
4A1
6C8
UART1\
WRITE\
INIT\
BVA*
DD*
U124 F04
WDOG
3A6
WDOG\
10C8
U112
LS366
U133
26LS29
U154
26LS29
D0
D1
D2
D3
D4
D5
Y0
Y1
Y2
Y3
Y4
Y5
C0
C1
C2
C3
OE0
OE1
VEE
OE
J1
TXD2\
TXD3\
DTR2\
DTR3\
RTS2\
RTS3\
C16
220PF
C14
220PF
C12
220PF
C10
220PF
C18
220PF
C17
220PF
U153
26LS32
U152
26LS32
RXD2\
RXD3\
DCD2\
DCD3\
CTS2\
CTS3\
RN11
MSP06A01-103G
0.1
8A1
PUD1
6A1
CTS3\
DTR2
DTR3
8A1
ENSERIAL23\
SILICON GRAPHICS INC.
REV
DUART1/DUART.CLOCK
IP2
5000-558
C
1.SEP.1985
7.OF.20

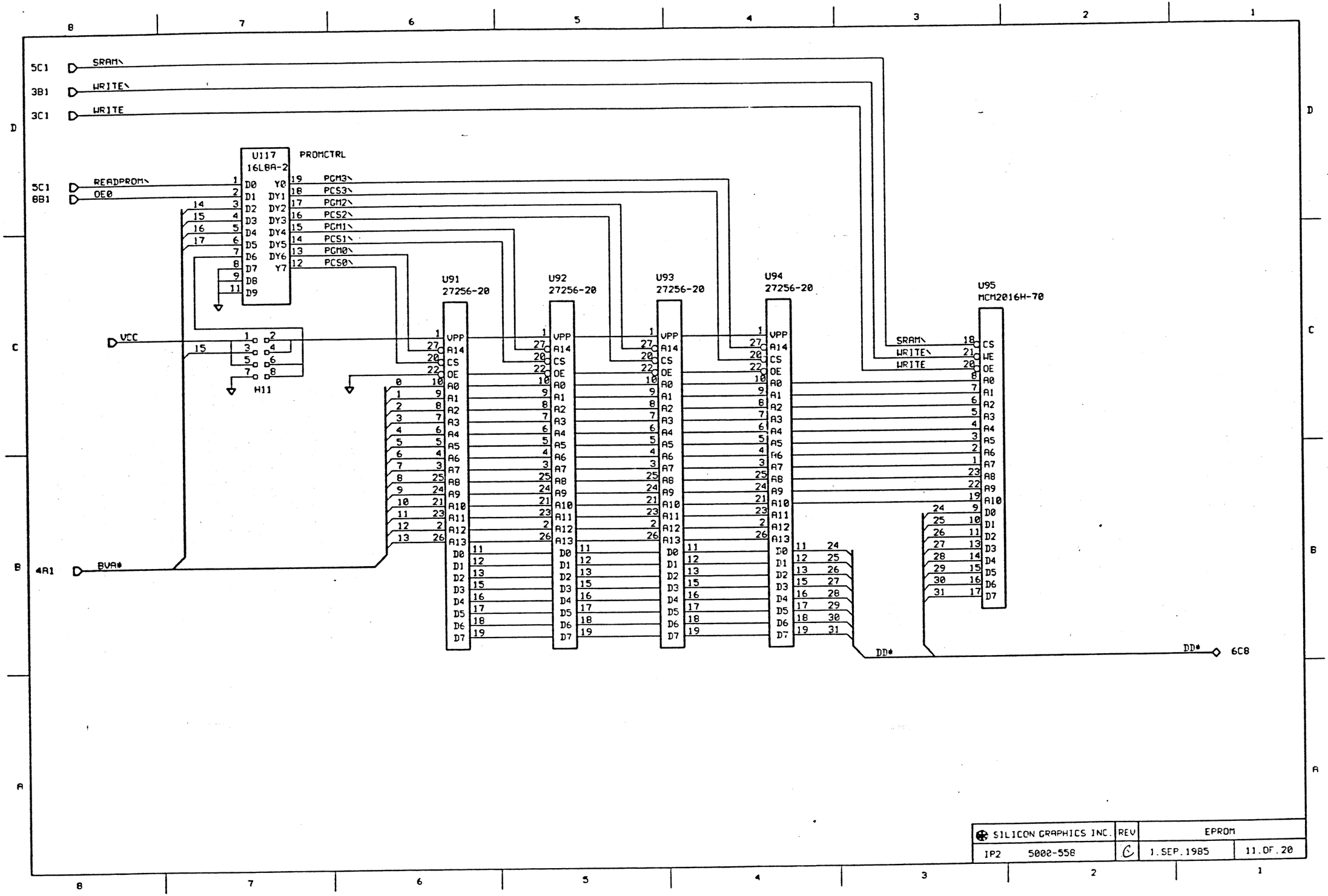

U128
26LS32
U122
ALS244A
U52
F00
U150
26LS32
U76
16R4
MOUSE
U110
ALS244A
U84
16C1
PARITY
U56
LS652
J1
RN12
MSP08A01-103G
RN7
MSP10A01-222G
RN1
MSP10A01-222G
RN5
MSP06A01-101G
DD*
6C8
MOUSEINT
4C8
PENAB\
17A8
READMBUT\
READMLOC\
PUD1
OE0
MX0
MX1
MY0
MY1
XDIR\
YDIR\
XFIRE\
YFIRE\
PRECM\
PREBUS\
WRITE
MWTCIN\
FC2
PENAB\
WRITEPCTRL\
READPCTRL\
OE1
ENSERIAL01\
ENSERIAL23\
6A8 10C3
7A8
SILICON GRAPHICS INC.
REV
MOUSE/PARITY.CONTROL
IP2 5000-558
C
1.SEP.1985
8.OF.20



SILICON GRAPHICS INC.	REV	REALTIME.CLOCK	
IP2 5000-558	C	14.NOV.1985	9.OF.20

J1
VCC
RN14
MSP10A01-472G
S1
SWITCH
SWCH16
S2
SWITCH
SWCH16
U156
ALS541
U155
ALS541
U175
LS365
JDIAG0
JDIAG1
JDIAG2
JDIAG3
HALT\
JHALT\
ENSERIAL01\
3A1
8A1
7C1
WDOG\
RN13 MSP10A01-472G
CONF*
CPUNO
READSWITCH\
5C1
DD*
17D1
PREBUS\
GENBAD\
U52
F00
4A8
CPUNO
18C8
BINIT\
P1
U28 F04
U29 7407
BINIT\
18B8
USERFPA
USERGE
SLAVE
ENABCBRQ
GEMASTER\
5C8
5D8
18C8
18B8
12C8
ENABWDOG
QUICK TOUT
ENABEXT
ENABINT
BOOT\
3A8
16A3
18C8
4C8
5D8
DIAG*
U113
LS273
U134
ALS541
U114
LS273
U135
ALS541
USERFPA
USERGE
SLAVE
ENABCBRQ
GEMASTER\
GENBAD
ENABWDOG
QUICK TOUT
ENABEXT
ENABINT
BOOT\
DS1
555-4001
RN15
MSP06A01-271C
VCC
6C8
5B1
3A1
5B1
DD*
WRITESTATUS\
INIT\
READSTATUS\
WRITESTATUS\
INIT\
READSTATUS\

SILICON GRAPHICS INC.	REV	SWITCHES. AND. STATUS	
IP2 5000-558	C	1. SEP. 1985	10. OF. 20


SRAM\
WRITE\
WRITE
5C1
3B1
3C1
U117
16L8A-2
PROMCTRL
READPROM\
OE0
5C1
8B1
D0 Y0
D1 DY1
D2 DY2
D3 DY3
D4 DY4
D5 DY5
D6 DY6
D7 Y7
D8
D9
PGM3\
PCS3\
PGM2\
PCS2\
PGM1\
PCS1\
PGM0\
PCS0\
VCC
H11
U91
27256-20
U92
27256-20
U93
27256-20
U94
27256-20
U95
MCM2016H-70
VPP
A14
CS
OE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
D0
D1
D2
D3
D4
D5
D6
D7
SRAM\
WRITE\
WRITE
CS
WE
OE
4A1
BVA#
DD#
DD#
6C8
SILICON GRAPHICS INC.
REV
EPROM
IP2 5000-558
C
1.SEP.1985
11.OF.20

GE PORT

U170 F374 — U172 F374 — U171 F374 — U173 F374

3D1 D*

10B1 GEMASTER\

8C1 PUP0

4A1 BVA*

3A1 INIT\

3B1 SIZE1

8C1 PUP1

4B1 ACK INBUF

3A1 INIT

5D5 GEREQ\

3C1 AS

3B1 DS\

U55 F74 R — U60 F74 R — U25 F74 R

U34 F02 — U54 F02 — U13 F10

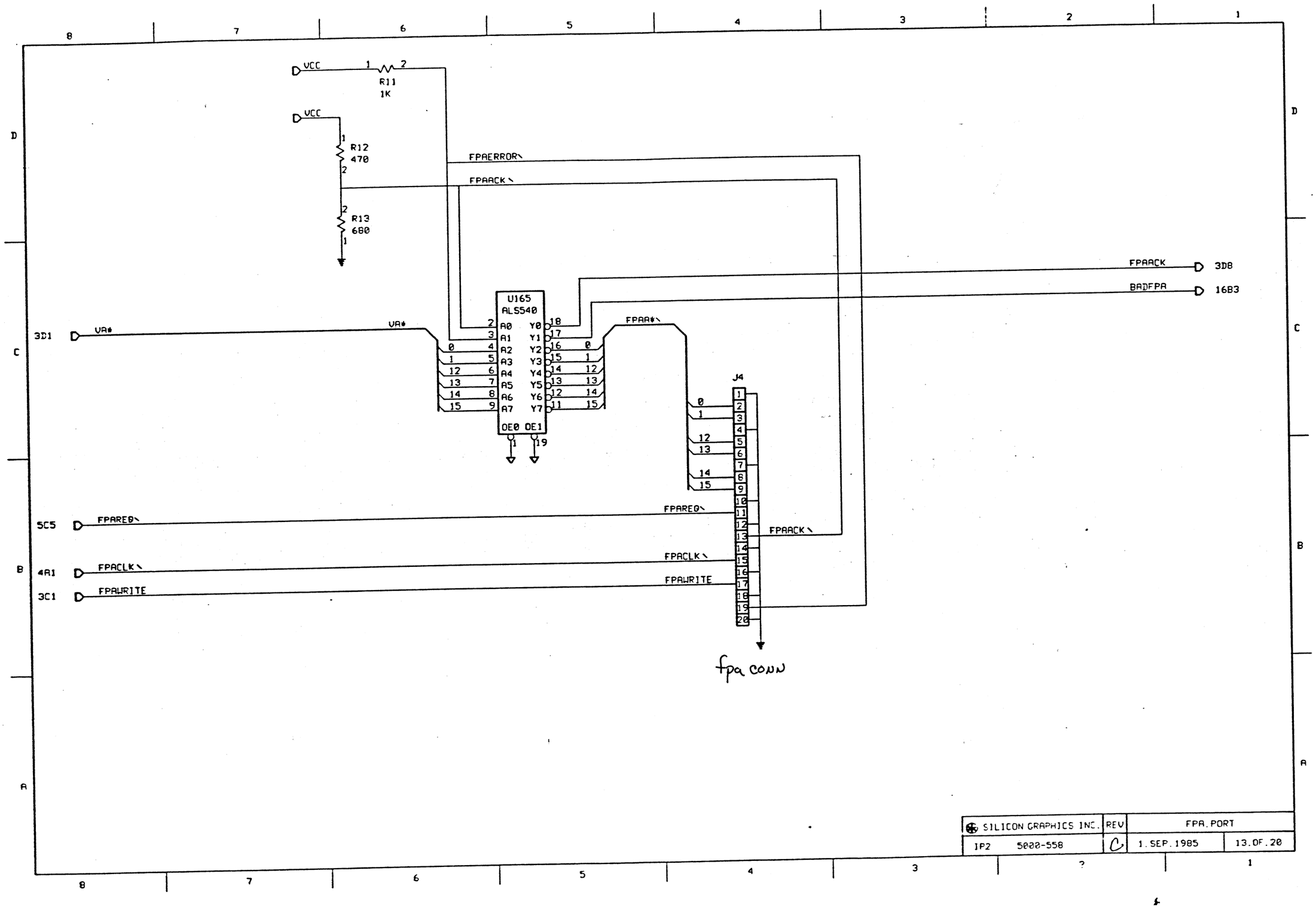
U123 LS368 — U98 F32 — U124 F04

C21 470PF

FIRSTREQ\ — SECONDREQ\ — GEDATA* — DOTWO\ — GESTART — GEACK — GEENAB\ — GEDONE\ — GEREADY\ — JA12\ — READOUT — ACK INBUF

GEACK 3D8

SILICON GRAPHICS INC.	REV	GE.PORT	
IP2 5000-558	C	24.OCT.1985	12.OF.20


VCC
R11
1K
VCC
R12
470
R13
680
FPAERROR\
FPAACK\
FPAACK
3D8
BADFPA
16B3
3D1
VA#
VA#
U165
ALS540
A0
A1
A2
A3
A4
A5
A6
A7
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
OE0
OE1
FPAA#\
J4
5C5
FPAREQ\
FPAREQ\
FPAACK\
4A1
FPACLK\
FPACLK\
3C1
FPAWRITE
FPAWRITE
fpa conn
SILICON GRAPHICS INC.
REV
FPA.PORT
IP2 5000-558
C
1.SEP.1985
13.OF.20

3D1 VA#

8B1 OE3

U37 16L8-15 MAPA1
U38 16L8-15 MAPA1
U39 16L8-15 MAPA1
U40 16L8-15 MAPA1
U41 16L8-15 MAPA1

MAPA#\ → 15D8

TDBASE#
KBASE#
SBASE#

This PAL necessary only for 256M virtual space

STACK\ → 16C8
KERNEL\ → 16C8

U35 16L8-15 MAPA0
U36 16L8-15 MAPA0

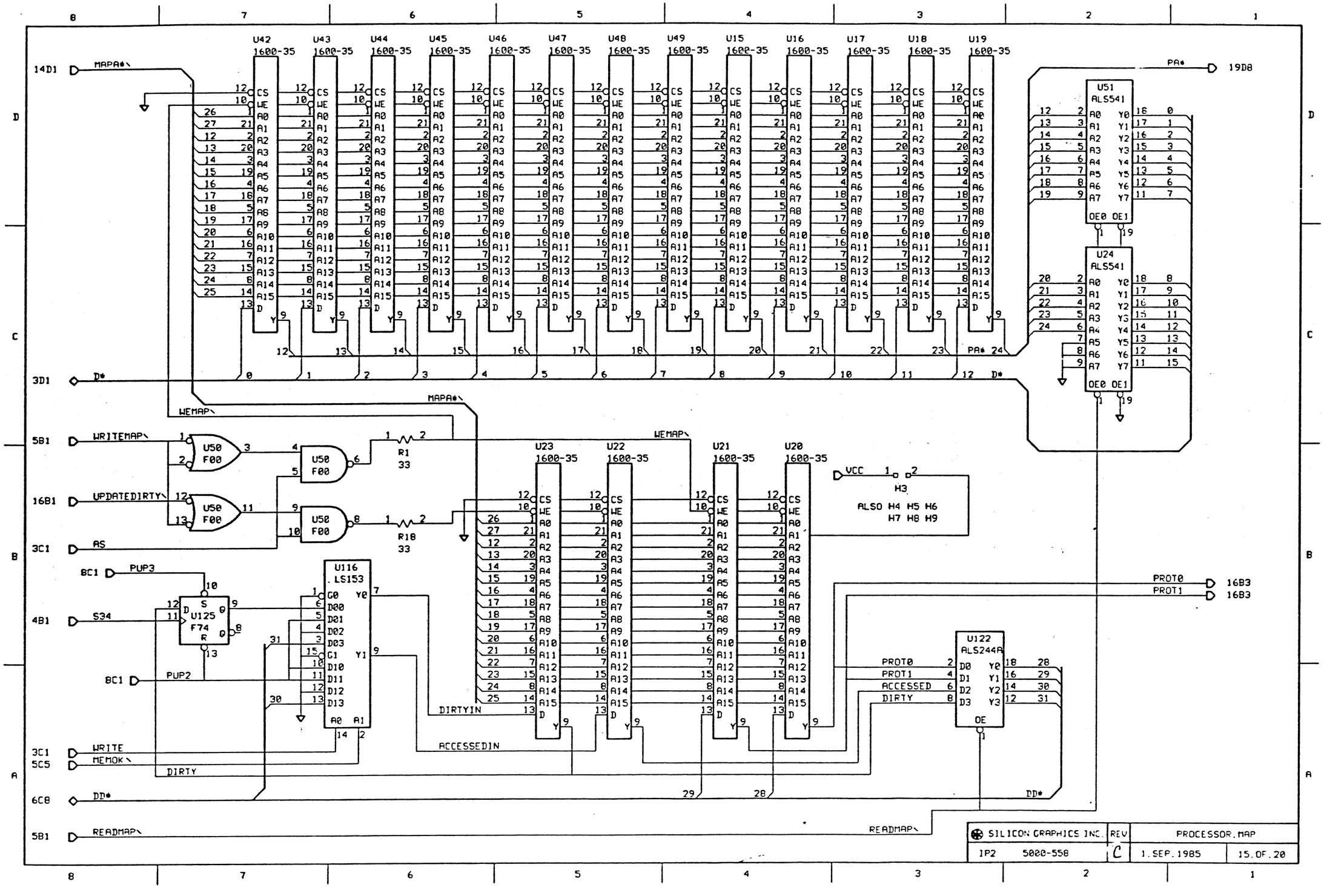
U64 LS652
U63 LS652
U67 LS652
U65 LS652
U66 LS652

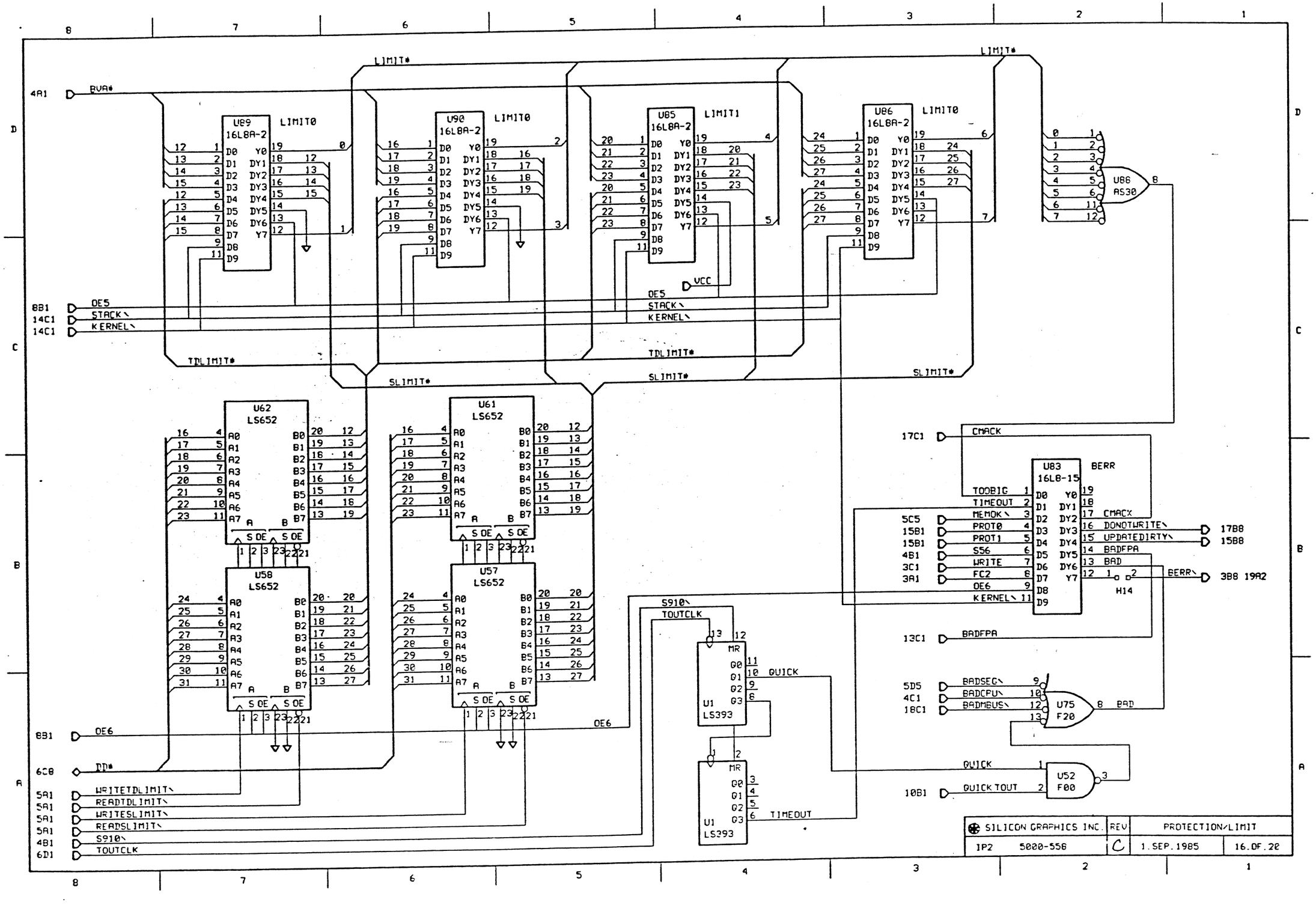
8B1 OE4

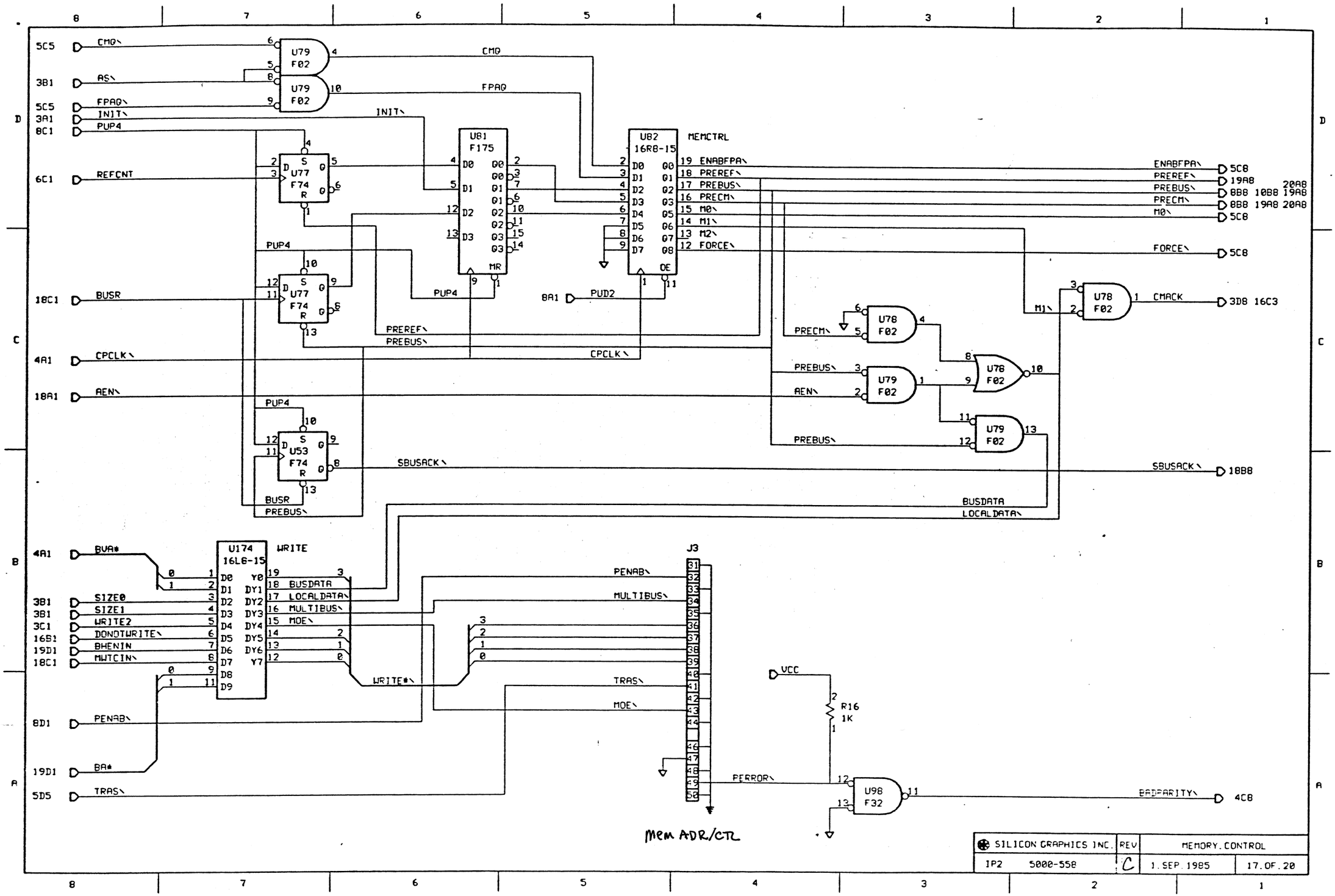
6C8 DD#

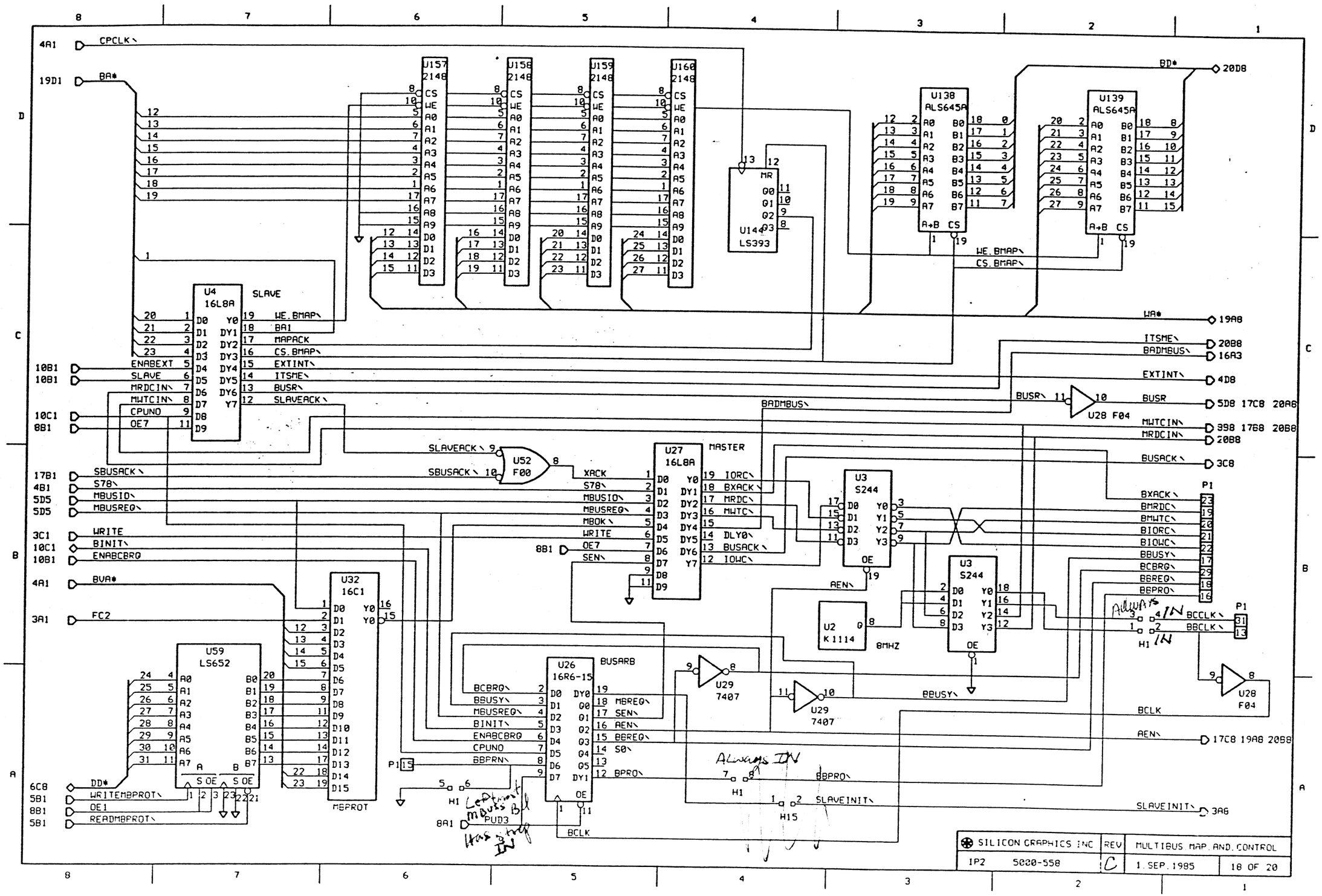
5A1 WRITETDBASE\
5A1 READTDBASE\
5A1 WRITESBASE\
5A1 READSBASE\
5B1 WRITEKBASE\
5B1 READKBASE\

SILICON GRAPHICS INC.	REV	MAP.ADDRESS.GENERATION	
IP2 5000-558	C	1.SEP.1985	14.OF.20


U42 1600-35
U43 1600-35
U44 1600-35
U45 1600-35
U46 1600-35
U47 1600-35
U48 1600-35
U49 1600-35
U15 1600-35
U16 1600-35
U17 1600-35
U18 1600-35
U19 1600-35
14D1 MAPA*\
3D1 D*
PA*
19D8
U51 ALS541
U24 ALS541
OE0 OE1
WEMAP\
MAPA*\
5B1 WRITEMAP\
16B1 UPDATEDIRTY\
3C1 AS
U50 F00
R1 33
R18 33
U23 1600-35
U22 1600-35
U21 1600-35
U20 1600-35
VCC
H3
ALSO H4 H5 H6 H7 H8 H9
8C1 PUP3
4B1 S34
8C1 PUP2
U125 F74
U116 LS153
PROT0
PROT1
16B3
U122 ALS244A
ACCESSED
DIRTY
DIRTYIN
ACCESSEDIN
3C1 WRITE
5C5 MEMOK\
6C8 DD*
5B1 READMAP\
SILICON GRAPHICS INC.
REV
PROCESSOR.MAP
IP2 5000-558
C
1.SEP.1985
15.OF.20


LIMIT*
4A1 BVA*
U89 16L8A-2 LIMIT0
U90 16L8A-2 LIMIT0
U85 16L8A-2 LIMIT1
U86 16L8A-2 LIMIT0
U86 AS30
VCC
8B1 OE5
14C1 STACK\
14C1 KERNEL\
TDLIMIT*
SLIMIT*
U62 LS652
U61 LS652
U58 LS652
U57 LS652
8B1 OE6
6C8 DD*
5A1 WRITETDLIMIT\
5A1 READTDLIMIT\
5A1 WRITESLIMIT\
5A1 READSLIMIT\
4B1 S910\
6D1 TOUTCLK
S910\
TOUTCLK
U1 LS393 QUICK
U1 LS393 TIMEOUT
17C1 CMACK
U83 16L8-15 BERR
TOOBIG
TIMEOUT
MEMOK\
PROT0
PROT1
S56
WRITE
FC2
OE6
KERNEL\
5C5
15B1
15B1
4B1
3C1
3A1
CMACK
DONOTWRITE\ 17B8
UPDATEDIRTY\ 15B8
BADFPA
BAD
BERR\ 3B8 19A2
H14
13C1 BADFPA
5D5 BADSEG\
4C1 BADCPU\
18C1 BADMBUS\
U75 F20 BAD
QUICK
10B1 QUICK TOUT
U52 F00
SILICON GRAPHICS INC.
REV
PROTECTION/LIMIT
1P2 5000-558
C
1.SEP.1985
16.OF.20


5C5 CM0\
3B1 AS\
5C5 FPA0\
3A1 INIT\
8C1 PUP4
6C1 REFCNT
18C1 BUSR
4A1 CPCLK\
18A1 AEN\
U79 F02
U77 F74
U53 F74
U81 F175
U82 16R8-15 MEMCTRL
U78 F02
U98 F32
U174 16L6-15 WRITE
CM0
FPA0
INIT\
PUP4
REFCNT
BUSR
PREREF\
PREBUS\
CPCLK\
AEN\
SBUSACK\
BUSDATA
LOCALDATA\
8A1 PUD2
ENABFPA\
PREREF\
PREBUS\
PRECM\
M0\
M1\
M2\
FORCE\
CMACK
PRECM\
PREBUS\
AEN\
5C8
19A8
20A8
8B8 10B8 19A8
8B8 19A8 20A8
3D8 16C3
SBUSACK\ 18B8
4A1 BVA*
3B1 SIZE0
3B1 SIZE1
3C1 WRITE2
16B1 DONOTWRITE\
19D1 BHENIN
18C1 MWTCIN\
8D1 PENAB\
19D1 BA*
5D5 TRAS\
WRITE#\
J3
PENAB\
MULTIBUS\
TRAS\
MOE\
VCC
R16 1K
PERROR\
BADPARITY\ 4C8
Mem ADR/CTL
SILICON GRAPHICS INC.
IP2 5000-558
REV C
MEMORY.CONTROL
1.SEP.1985
17.OF.20


4A1 CPCLK\
19D1 BA*
U157 2148
U158 2148
U159 2148
U160 2148
U144 LS393
U138 ALS645A
U139 ALS645A
BD* 20D8
WE.BMAP\
CS.BMAP\
WA* 19A8
U4 16L8A SLAVE
ENABEXT
SLAVE
MRDCIN\
MWTCIN\
CPUNO
OE7
10B1
10B1
10C1
8B1
ITSME\ 20B8
BADMBUS\ 16A3
EXTINT\ 4D8
BUSR\ 5D8 17C8 20A6
MWTCIN\ 39B 17B8 20B8
MRDCIN\ 20B8
BUSACK\ 3C8
U28 F04
U52 F00
SLAVEACK\
SBUSACK\
U27 16L8A MASTER
XACK
S78\
MBUSID\
MBUSREQ\
MBOK\
WRITE
OE7
SEN\
IORC\
BXACK\
IOWC\
DLY0\
BUSACK\
U3 S244
U2 K1114 8MHZ
AEN\
BBUSY\
BCLK
BCCLK\
BBCLK\
P1
BXACK\
BMRDC\
BMWTC\
BIORC\
BIOWC\
BBUSY\
BCBRQ\
BBREQ\
BBPRO\
17B1 SBUSACK\
4B1 S78\
5D5 MBUSID\
5D5 MBUSREQ\
3C1 WRITE
10C1 BINIT\
10B1 ENABCBRQ
4A1 BVA*
3A1 FC2
U32 16C1
U59 LS652
U26 16R6-15 BUSARB
BCBRQ\
BBUSY\
MBUSREQ\
BINIT\
ENABCBRQ
CPUNO
BBPRN\
MBREQ\
SEN\
AEN\
BBREQ\
S0\
BPRQ\
U29 7407
U29 7407
BBPRO\
SLAVEINIT\ 3A6
6C8 DD*
5B1 WRITEMBPROT\
8B1 OE1
5B1 READMBPROT\
MBPROT
8A1 PUD3
Always IN
Has strap IN
SILICON GRAPHICS INC
IP2 5000-558
REV C
MULTIBUS MAP AND CONTROL
1 SEP 1985
18 OF 20

MEM ADR/CTL

BBHEN\ — P1 27 — U28 F04

20B6 BHENOUT

20B6 BA0OUT

4A1 BVA*

3D1 VA*

15D1 PA*

MA#\

BA*\

BHENIN — 17B8 20B8

BA* — 17A8 18D8 20A8

U146 F240 — U147 F240 — U148 F240

U33 29824 — U31 ALS534 — U30 ALS534

PUP5 8C1

P1 — P2

U7 ALS540 — U6 ALS540 — U5 ALS540

U167 ALS540 — U168 ALS540 — U169 ALS540

VCC — RN3 MSP06A01-472G

U145 LS393 — MR

REFA*

U53 F74

PUP3 8C1

PUP6 8C1

U166 ALS540 — U149 ALS540

J3

VCC — RN8 MSP06A01-472G

RN9 MSP06A01-472G

3D1 DSACK0\

16B1 BERR\

17D1 PRECM\

4B1 S34

18A1 AEN\

17D1 PREBUS\

6C1 REFCNT

17D1 PREREF\

16C1 WA*

SILICON GRAPHICS INC.	REV	ADDRESS. BUFFERS	
IP2 5000-558	C	1. SEP. 1985	19. OF. 20

3D1 D*
18D1 BD*
6C8 DD*
3C1 WRITE2
5B5 DDEN\
4A1 BVA*
18C1 ITSME\
19D1 BHENIN\
3B1 SIZE0
3B1 SIZE1
5D5 MBUSREQ\
18C1 MRDCIN\
18C1 MWTCIN\
18A1 AEN\
8C1 OE8
17D1 PREBUS\
19D1 BA*
5C5 MEMOK\
17D1 PRECM\
18C1 BUSR
4B1 S34\
5C5 FPAOK\

U120 ALS645A
U121 ALS645A
U12 ALS640A
U10 ALS640A
U11 ALS640A
SWAP U136 16L8-15
MD U137 16L8-15
U140 AS652 THREE
U141 AS652 TWO
U142 AS652 ONE
U143 AS652 ZERO
U161 F245 THREE
U162 F245 TWO
U163 F245 ONE
U164 F245 ZERO
P1
J2
U28 F04

NOSWAP\ WRITE2 BVA0 BA0OUT BHENOUT BDIN\ SWAP\
19D8 19D8
BDMD MDBD01\ MDBD23\ USEREG MDEN\
MULTIBUS DATA
MEM DATA

SILICON GRAPHICS INC.	REV	DATA. BUFFERS
IP2 5000-558	C	1. SEP. 1985 — 20. OF. 20