R-3

DRUM STORAGE SYSTEM

REFERENCE MANUAL

Michael G. Hurley

University of California, Berkeley

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I. INTRODUCTION

The Drum Storage System consists of a 1.3 million word drum connected to the Berkeley Time Sharing System's SDS-930 Computer. The drum provides the computer with both secondary storage and core swapping capability. Records of up to 16,384 words can be transferred between the computer's core and the drum. The rate of transfer is 500,000 words per second.

The operation of the drum system is initiated by the computer. Once started, the drum is controlled by a list of commands in the computer's core memory. These commands cause the drum to perform record transfers, branch to a new command list, disconnect, and interrupt the computer. The drum system is provided with an independent path to the computer's core memory, thus allowing it to access the command list and perform record transfers independent of the computer's operation.

The computer is equipped with two separate 16,384 word core memories. One memory contains all even addresses and the other all odd addresses; thus, during a record transfer, the drum system alternately references the memories. While the drum is referencing one memory, the computer can reference the other. If they both attempt to reference the same memory, the computer reference is delayed one cycle. Memory reference interference is expected to cause the computer to operate at 70 per cent of its normal rate during record transfers.

II. COMPUTER INSTRUCTIONS TO DRUM SYSTEM

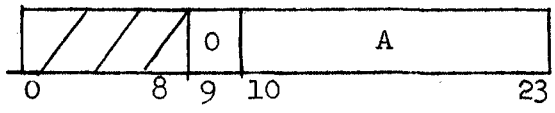
The computer uses one of three instructions to initiate operations within the drum system. Two of these instructions, start drum channel and read drum channel, are effective only when the drum system is in wait (inactive) status. The third, reset drum channel, is effective at all times.

START DRUM CHANNEL

EOM 00230004

When the drum system is in wait status and the computer executes this instruction, the system is energized and placed in command list mode. The system reads the contents of core location 20 and uses the address field of this word as a pointer to a drum channel command list. This command list must be stored in the lower 16K of core memory. The command list is then executed by the drum system. During the operation of the drum in command list mode, location 20 is used by the drum as a program counter and should not be altered.

Core location 20

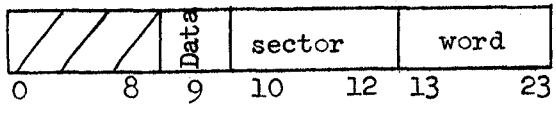


READ DRUM CHANNEL

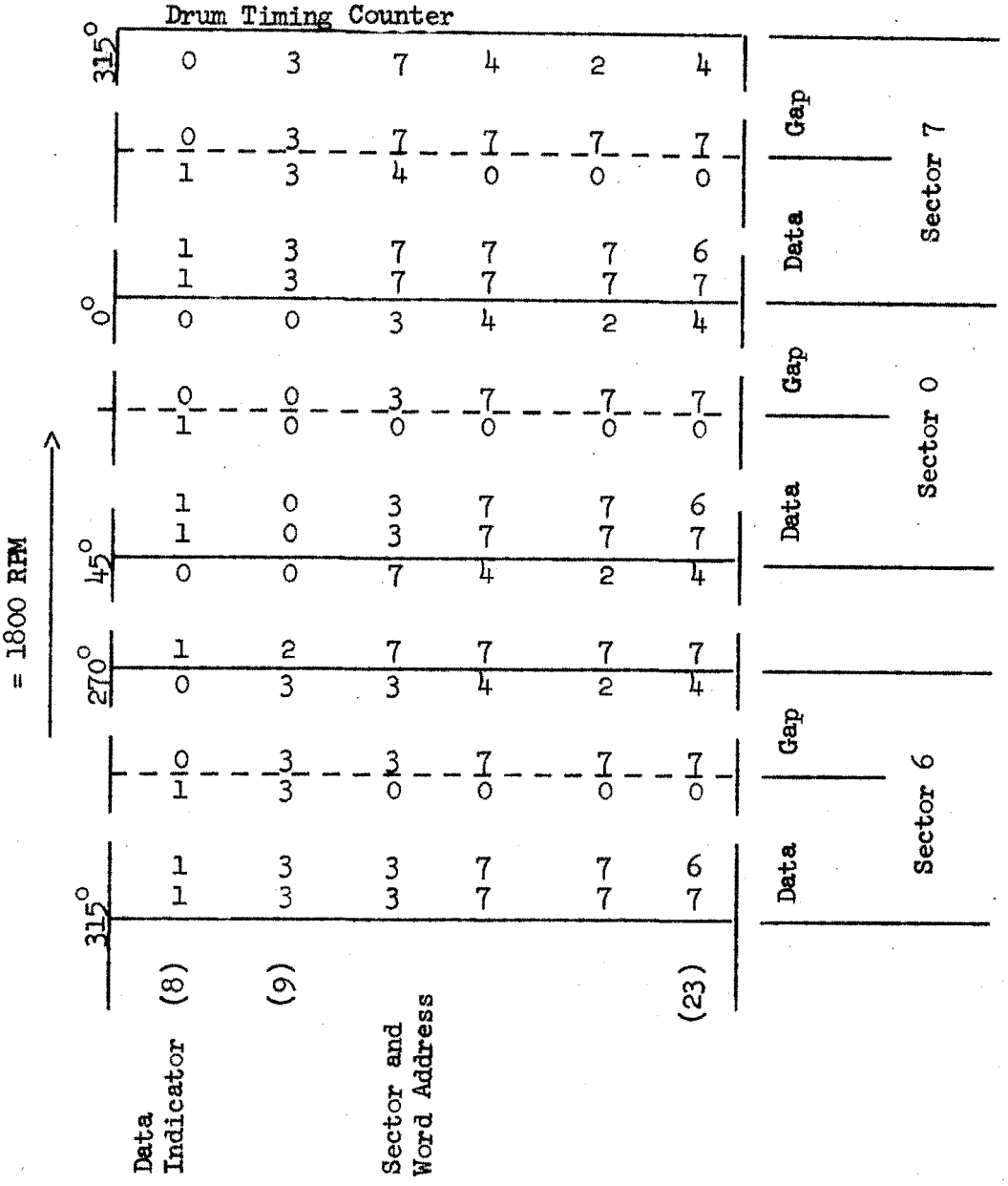
EOM 00230024

When the drum system is in wait status and the computer executes this instruction, the system places the present status of the drum timing counter in core location 21. The drum timing counter gives the location of the drum relative to the read/write heads. Figure 1 is a map of the drum. Each count of the drum timing counter represents one memory cycle of the SDS-930 Computer. Location 21 is loaded and the drum system returned to wait status two memory cycles after the execution of the EOM instruction.

Core location 21



See Figure 1.



Information is written on 84 bands around the drum. Each band is divided into 8 sectors. Each sector contains 2,048 words of storage and 236 words of gap (non-addressable memory). Bits 9 through 23 of the drum timing counter contain the word address of the location. Bit 8 indicates data or gap field.

FIGURE 1: DRUM ADDRESS MAP

RESET DRUM CHANNEL

EOM 00230044

When the computer executes this instruction all drum channel operations are immediately terminated and the system is placed in wait status. The drum error indicator is turned off.

III. COMPUTER TESTS OF DRUM SYSTEM

Two computer instructions are available to test the status of the drum system. These instructions can be executed at any time.

Drum Active Test:

SKIP IF DRUM CHANNEL IN WAIT STATUS

SKS 04030004

If the drum channel is in wait status, the computer skips the next instruction in sequence and executes the following instruction. If the drum channel is in active status, the computer executes the next instruction in sequence.

Drum Error Test:

SKIP IF DRUM CHANNEL ERROR INDICATOR NOT SET

SKS 04030024

If the drum channel error indicator is not set, the computer skips the next instruction in sequence and executes the following instruction. If the drum error indicator is set, the computer executes the next instruction in sequence. The drum error indicator is set when a parity error is detected during the transfer of a record from drum to core.

IV. DRUM SYSTEM COMMANDS

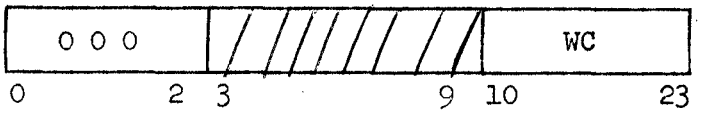
All drum system commands must be stored in the lower 16K of core memory.

DCTX - Drum Channel Transmit:

This command conditions the drum system for a record transter between drum and core. Because of the quantity of information needed to set up the channel, this command is three words in length. These words DCTA, DCTB, and DCTC are stored in three consecutive memory locations. The channel requires 18 word cycle times for setup prior to performing the transmission.

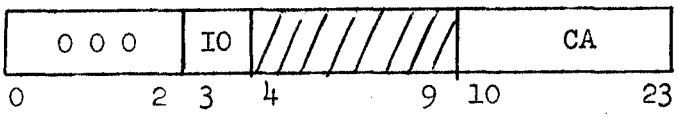
Execution time (19 + access time and transmission time) cycles

DCTA



WC = the length in words of the record transmitted by the DCTX command. All records on the drum include a control word which is automatically written immediately following the last word of the record. The control word contains parity on the record and provides a guard band between records. The control word is written in an addressable memory location. Thus, the programmer must allot WC+1 words for a record WC words in length; an exception is records where the last word is written in a drum location that is a multiple of 2,048, i.e., octal locations 0003777, 0007777, 0013777 - - - - - - 5177777. In these cases the control word is written in the non-addressable gap and an addressable drum location is not lost.

DCTB

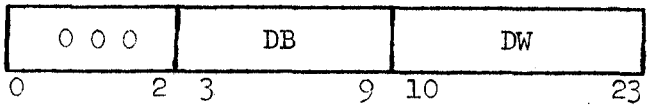


IO=1 Transfer record from core to drum.

IO=0 Transfer record from drum to core.

CA = the address in core of the first word of the record transmitted by the DCTX command.

DCTC



DB and DW define the drum starting location of the record transmitted by the DCTX command. DB selects one of the 84 drum bands; octal addresses 0 through 123 are used. DW defines one of 16,384 words within the band. Octal addresses 0000 through 37777 are used. During the transmission of a record when the end of a band is reached (i.e., word 37777) the drum band is automatically incremented by one and the remainder of the transmission is performed on the new band starting at location word 0000, thus providing continuous addressing within the drum system.

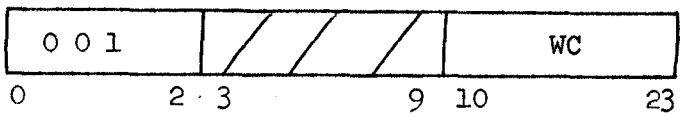
DCCT - Drum Channel Conditional Transmit:

This command is a conditional form of the DCTX command. If the parity indicator is off, the command acts like a DCTX and a record transfer is performed. If the parity indicator is on, the command acts like a DCDI command and the drum system is disconnected and the computer is interrupted. Due to the quantity of information needed to set up the channel,

this command is three words in length. These words are DCCT, DCTB and DCTC.

Execution time: Parity indicator off (19 + access time and transmission time) cycles; parity indicator on 8 cycles.

DCCT



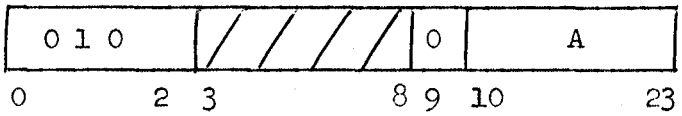
WC = See DCTA part of DCTX command.

DCTB and DCTC are the same as the DCTB and DCTB parts of the DCTX command.

DCBR - Drum Channel Branch:

This command causes the drum channel to take the next command from the core location specified in the address field of the command.

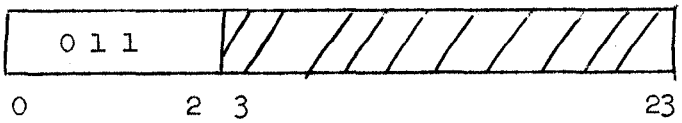
Execution time: 4 cycles



DCRP - Drum Channel Reset Parity Indicator:

This command causes the drum channel parity indicator to be reset.

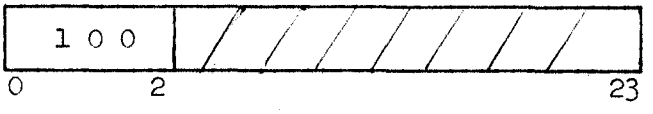
Execution time: 4 cycles



DCDX - Drum Channel Disconnect:

This command causes the drum channel to return to wait status. In wait status the drum channel is prepared to accept a new instruction from the computer.

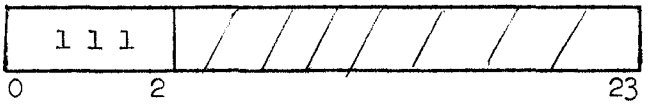
Execution time: 8 cycles



DCDI - Drum Channel Disconnect and Interrupt:

This command causes the drum channel to return to wait status and interrupt the computer. The location of this interrupt can be assigned in the ARPA POT/PIN MULTIPLEXER.

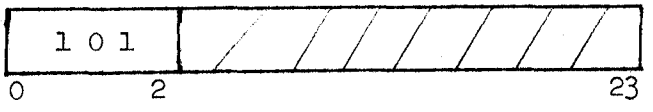
Execution time: 8 cycles



DCDC - Drum Channel Disconnect and Interrupt If Parity Indicator Set:

This command causes the drum channel to return to wait status and interrupt the computer if the drum parity indicator is set. This interrupt is the same interrupt used by the DCDI command.

Execution time: 8 cycles



V. SPECIAL FEATURES

Monitor Drum System:

The drum channel command counter is stored in core location 20. The command counter contains the address plus three of the command being executed by the drum system. By reading this location the computer can monitor the progress of the drum system.

Read or Write of Partial Record:

Records that are independently written on the drum can be read back with one command provided they are contiguous and the individual records are joined at a drum gap (See Figure 1). Thus, the following four records could be read as one record of 4,150 words starting at drum address 0273776. The reverse is also true had one record been written it could be read back as the four separate records shown.

Drum Starting Address	Word Count
0273776	2
0274000	2,048
0300000	2,048
0304000	52

The following changes have been made in the design of the drum storage system.

1. The drum channel command list must be stored in the lower 16K of core memory.
2. The sector gap has been changed from 100 words to 236 words in length.

Michael G. Hurley