This document was produced by SDC in performance of _____

NOTE *an internal working paper*

System Development Corporation/2500 Colorado Ave./Santa Monica, California

AUTHOR *[signature]*

G. A. Slaybaugh

DATE   PAGE 1 OF 1 PAGE

1 February 1962

Author Delivered

ICR READING AND WRITING

When the ICR is read or written, it is treated as a 45 bit register (plus parities). Bits S, 28 and 29 may be neither set nor sensed by arithmetic operations. These three bits may be set or sensed only through the use of PER or BSN instructions. Bit S is a spare, originally assigned to alarm 1. Bits 28 and 29 are for pause inactivity and loop inactivity. The PER-SEN codes relating to bits 28 and 29 are listed in N-17334. There are no active codes pertaining to bit S.

When writing (eg, STA) the ICR, if any of these three bits are "1's", the machine will ignore them except for adjusting the parity bit. When reading the ICR (eg, LDA), bits S, 28 and 29 always appear as "0's".