RAYTHEON

Division :	MISSILE SYSTEMS	Contract No.	
Operation :	Crosby Drive		
Department :	Data Processing Systems	Distribution :	aa
To :	S. Wallach D-B54	File No.	
From :	S. Nissen D-B54	Memo No. :	7675-97-74
Subject :	ROM Field Specification	Date :	Feb. 12, 1974
Ref :	7675-14-74	Revised :	2/8/74

The following memo defines the ROM fields which have been specified in detail for the PMU MINI. Each field controls a specific area of data flow. Names of units are taken from the PMU Master Block Diagram available by contacting M. Hereth at Ext. 2257. This memo supersedes any previously released , including the reference.

1. P REGISTER CONTROL (3 BITS)

RPC0	RPC1	RPC2	FUNCTION
0	0	0	Load AUBUS
0	0	1	*Load P Shifted Right
0	1	0	Load TMBUS
0	1	1	Increment P
1	0	0	Load AUBUS
1	0	1	*Load P Shifted Right
1	1	0	Load TMBUS
1	1	1	Load P (idle)

*End bits are derived from unswitched ADBUS

2. IA REGISTER CONTROL (3 BITS)

RIA0	RIA1	RIA2	FUNCTION
0	0	0	Load AUBUS
0	0	1	*Load AUBUS Shifted Right
0	1	0	Increment IA8-15
0	1	1	Increment IA
1	0	0	Load AUBUS
1	0	1	*Load AUBUS Shifted Right
1	1	0	Load TMBUS
1	1	1	Load IA (idle)

*End bits are specified in another memo.

3. IB REGISTER CONTROL (4 BITS)

The IB register control is divided into two levels, IB Select Control and IB Shift Control. The shifter shifts the selector output.

3. **IB REGISTER CONTROL** (cont.)

IB SELECT

RIB0	RIB1		SELECTION
0	0		IB
0	1		TMBUS
1	0		O
1	1		AUBUS

IB SHIFT

RIB2	RIB3		SHIFT
0	0		UNUSED
0	1		LEFT
1	0		RIGHT
1	1		NO SHIFT (TRANSFER)

For example, to idle IB, the code 0011 would be used.

4. **AD BUS SELECT CONTROL** (2 BITS)

The ADBUS Selector which feeds the switch is controlled by this field.

RAD0	RAD1		SELECTION
0	0		IB
0	1		SP
1	0		P
1	1		IA

5. **DT BUS SELECT CONTROL** (2 BITS)

RDT0	RDT1		SELECTION
0	0		IB
0	1		SP
1	0		P
1	1		IA

6. **AD SWITCH CONTROL** (1 BIT)

RADS		SELECTION
0		ADBUS
1		ADBUS Switched

7. **AUBUS CONTROL** (2 BITS)

RABL	RABH	AUBUS0-7	AUBUS8-15
0	0	DTBUS0-7	DTBUS8-15
0	1	AUF0-7	DTBUS8-15
1	0	DTBUS0-7	AUF8-15
1	1	AUF0-7	AUF8-15

. Note: AUF is the data output of the AU, but does not
exist separately from AUBUS. It is named here
for descriptive purposes only.

8. SP WRITE (1 BIT)

This line, when a 1 causes a SP write cycle to take place
from the AUBUS. When a 0, SP is read.

9. TM CONTROL (2 BITS)

Four possible TM cycles are defined. One is a TM Read
Cycle. A second is a TM Write Cycle. A third is a TM
Buffer Load Cycle. Finally, there is a TM Idle Cycle.

9A. TM Read Cycle (Code 01)

The address for the read must already have been loaded
into the address register on a previous clock. The read
cycle, once initiated will be carried to completion. ROM
flow will continue on the clock pulse following a data
available signal from TM. At this point, the data will
be in the data register. Any ROM step which subsequently
attempts a TM read or write cycle will cause the clock to
halt at that point, awaiting a TM not busy indication,
unless TM is not busy. Buffer load cycles will be allowed
to carry to completion, however, when the memory is busy
once data available has been received. The address register will
be loaded with new value on the clock pulse following data available

9B. TM Write Cycle (Code 11)

The address and data for the write must already have been
placed into the address and data registers on a previous
clock. The write cycle, once initiated will be carried to
completion. ROM flow will continue immediately. Any
ROM step which subsequently attempts a TM read or write
cycle will cause the clock to halt at that point, awaiting
a TM not busy indication, unless TM is not busy. Buffer
load cycles will be allowed to carry to completion,
however, when the memory is busy once a data accepted signal has
been received from TM. The data and address registers will be
loaded with a new value as in 9C on the clock pulse following data

9C. Buffer Load Cycle (Code 10) ——————————— accepted.

The data and address buffers will be loaded from external
ports on the next clock pulse.

9D. TM Idle (Code 00)

Actions initiated are continued. No new action is
initiated. Buffers are maintained, except a read cycle
will load the data register when data becomes available.

10. **SP ADDRESS CONTROL** (6 BITS)

The SP Address Control is primarily controlled by RSP0.
When RSP0 is 1, the SP address is set to be RSP1-5.
When RSP0 is 0, one of the following selections will be
made: RSP0 = 0 and RSP5 is used to enable sign extraction
on the DTBUS based on ØPSE.

RSP0=0	RSP1	RSP2	RSP3	RSP4		SP ADDRESS
	1	0	0	0	- 10	TMR23-27
	1	0	0	1	- 12	CP0-4
	1	0	1	0	- 14	0, SPR0-3
	1	0	1	1	- 16	SPARE
	1	1	0	0	- 18	SPD0, SPD1-4
	1	1	0	1	- 1A	SPD0-4
	1	1	1	0	- 1C	1, SPR0-3
	1	1	1	1	- 1E	00, TMR29-31
	0	ⓓ	ⓓ	ⓓ	- 00	SEE NOTE 2

NOTE 1: ⓓ is don't care
TMR is memory data register
CP is control panel
SPR is SP register for PMU instruction field
     bits 8 - 11.
SPD is register indirection SP field bits 27-31.

NOTE 2: Result is 0, TMR8-11 if TMR13-15 = 000
Result is 00, TMR13-15 if TMR13-15 ≠ 000.
RSP5 is ignored if TMR13-15 ≠ 000.

11. **M BUS CONTROL** (1 BIT)

RMBS	SELECTION
0	TMBUS
1	ADBUS SWITCHED

12. **TM SELECTOR CONTROLS** (5 BITS)

The TM Selector is defined as the TMBUS Selector and
Memory Selector in tandem. Control of these is merged.
The TMBUS is one input to the memory selector. It is
selected to appear at the memory unless one of the other
inputs to this selector is chosen. For these three selections,
the TMBUS is considered as undefined for the present. A
fifth bit of the selector is used only in conjunction with
bits 0-2 being 010. This bit should be 1 for all other cases.
Its effect when 0 is undefined at present. When used as 0
with 010, a flip-flop named HWSL controls the function selected.

Functions are shown as the outputs found on TMSL0-15, TMSL16-31,
TMSL32-35.

RTL0	RTL1	RTL2	RTL3	RTL4	HWSL	FUNCTION
0	0	0	0	1	$\emptyset$	AUBUS, TMR_L, DTAG
0	0	0	1	1	$\emptyset$	AP1, DTAG
0	0	1	0	1	$\emptyset$	AP2, DTAG
0	0	1	1	1	$\emptyset$	0, TMR_{LL}, DTAG
0	1	0	0	1	$\emptyset$	TMR_H, TMR_L, TMR_D
0	1	0	1	1	$\emptyset$	TMR_H, TMR_H, TMR_D
0	1	0	$\emptyset$	0	0	TMR_H, TMR_H, TMR_D
0	1	0	$\emptyset$	0	1	TMR_H, TMR_L, TMR_D
0	1	1	0	1	$\emptyset$	TMR_H, AUBUS, DTAG
0	1	1	1	1	$\emptyset$	TMR_H, CBTS, DTAG
1	0	0	0	1	$\emptyset$	Z, TMR_L, DTAG
1	0	0	1	1	$\emptyset$	Z, Z, DTAG
1	0	1	0	1	$\emptyset$	Z, AUBUS, DTAG
1	0	1	1	1	$\emptyset$	Z, Z, DTAG
1	1	0	0	1	$\emptyset$	TMR_H, TMR_L, AUBUS12-15
1	1	0	1	1	$\emptyset$	0, 0, DTAG
1	1	1	0	1	$\emptyset$	CP
1	1	1	1	1	$\emptyset$	CHANNEL

$\emptyset$ is don't care
AUBUS is 16 bits wide
TMR_H is TMR0-15
TMR_L is TMR16-31
TMR_D is TMR32-35
DTAG is generated by control (4 bits wide). It is equal to
    TMR_D if RAU4-5 = 01. It is equal to RAU5-7 if RAU 4 = 1
    It is an AP tag in the DPE configuration when RAU4-5 = 00.
    These will be defined later. RAU is AU control field.
AP1, AP2 are 32 bits wide
TMR_{LL} is TMR17-31, 0 (TMR_L LEFT SHIFTED)
CBTS is 12 0's, TMR_D
Z is HIGH IMPEDANCE
0 is 16 0's
CP is Control Panel
CHANNEL is 36 bits wide

13. **AU CONTROLS** (8 BITS)

AU Control lines are divided to control different parts of
the AU separately. If RAU3 = 1 and RAU4 = 0, the logical
functions are selected according to the following table.
Bits 1 and 2 are ignored.

RAU0	RAU5	RAU6	RAU7	FUNCTION
0	0	0	0	0
0	0	0	1	$\overline{R1.R2}$
0	0	1	0	$\overline{R1}.R2$
0	0	1	1	$\overline{R1}$
0	1	0	0	R1.R2
0	1	0	1	R2

13. AU CONTROLS (cont.)

RAU0	RAU5	RAU6	RAU7	FUNCTION
0	1	1	0	$\overline{R1 \oplus R2}$
0	1	1	1	$\overline{R1 + R2}$
1	0	0	0	$R1 . \overline{R2}$ — DT$\geq$M
1	0	0	1	$R1 \oplus R2$
1	0	1	0	$\overline{R2}$
1	0	1	1	$\overline{R1 + \overline{R2}}$
1	1	0	0	R1
1	1	0	1	$R1 + \underline{R2}$
1	1	1	0	$R1 + \overline{R2}$ — DT>M
1	1	1	1	1

R1 = register selected to DTBUS
R2 = register selected to ADBUS Switched, then MBUS.

If TM is selected to MBUS, substitute $\overline{TM}$ for R2 to obtain correct function.

1 is 16 1's
0 is 16 0's

If RAU3 = 0, and RAU1 or RAU2 = 1 and RAU4 = 0, then OPR register bits 2, 3, 6, 7 will select a logical function using the same table as above. RAU0,5,6,7 are ignored.

If RAU 3 = 0 and RAU1 = RAU2 = 0 and RAU4 = 0, an undefined operation will result.

When RAU4 = 1, an arithmetic function is selected. If RAU1, 2, 3 is not 000, then an arithmetic function is selected according to the following table.

RAU5	RAU6	RAU7	FUNCTION
0	0	0	$\overline{R2}$ PLUS 1
0	0	1	$\overline{R2}$ PLUS R1
0	1	0	1 PLUS 0
0	1	1	R1 PLUS 0
1	0	0	1 PLUS 1
1	0	1	R1 PLUS 1
1	1	0	R2 PLUS 1
1	1	1	R2 PLUS R1

0, 1, R1 and R2 are as for logicals.

Carry functioniong is controlled by bits 1, 2, 3.

RAU1	RAU2	RAU3	CARRY IN	CARRY TO BIT 7
0	0	1	CHFF	AC
0	1	0	0	AC
0	1	1	1	AC
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

AC implies a carry ACcross from bit 8 to bit 7. CHFF is a flip flop which retains the carry out of bit 0 from the previous AU function.

Bit 0 controls polarity of output. When bit 0 is 1, the functions are as listed in the table above. When bit 0 is 0, the output is inverted. Carry occurs before inversion.

When RAU1, 2, 3, 4 = 0001, an add - subtract step is indicated. An add or subtract function is selected ((R2 PLUS R1) or (R2 PLUS R1) respectively since TM is the input) according to the sign bits of the two operands as indicated by SGSP and TMR0 or TMR16. Selection of the appropriate TMR sign bit is automatic based on opcode bit 5 and the HWSL flip-flop. Also controlling add - subtract selection is opcode bit 7, which differentiates an add from a subtract operation code.

The polarity selection is set to be dependent on the carry out of the AU when subtract is selected. A true polarity results when there is a carry out. When an add is selected, a true polarity is also selected.

Carry is set to carry accross from bit 8 to bit 7. Carry in is set to end around (carry in = carry out) when a subtract is selected. Carry in is set to 0 otherwise.

14. **TM, SP SIGN SELECTORS** (3 BITS)

This sign selected by the SP sign selector and TM sign selector is as follows:

RSS0	RSS1	RSS2	SP SIGN	TM SIGN
0	0	0	0	0
0	0	1	1	0
0	1	0	NOTE 1	0
0	1	1	SGSP	0
1	0	0	SGSP⊕TB16	0
1	0	1	TB16	0
1	1	0	SGSP	0
1	1	1	AU00	TB16

NOTE 1: $AUAD \cdot SGSP + \overline{AUAD} \cdot (SGSP \oplus \overline{AC\emptyset 11})$

15. ADDRESS SELECT CONTROL (4 BITS)

The memory address register is fed through a selector to a shifting and swapping selector. The first stage selector is controlled directly as follows:

RTA0	RTA1	Selection
0	0	ADBUS SWITCHED
0	1	AUBUS
1	0	TM OUTPUT
1	1	SP

The shifter and swapper are controlled by a second two bit field as follows:

RAS0	RAS1	Function
0	0	ADSEL 0-15
0	1	PGS, ADSEL 0-7
1	0	PGS, EB, ADSEL 0-6
1	1	NOTE 1

ADSEL is selector output

PGS is virtual address page selector. This input is hardwired in the MINI to ADSEL8-15. EB is an end-bit which is hardwired to 0 in the MINI.

NOTE 1: Combinational determination of function is as follows:

EXTS	NEXT	MIDS	RRPS	Shift Control
1	0	0	0	T$\emptyset$05
0	0	0	0	$\emptyset$PR5 + INDR
0	0	1	0	$\emptyset$PR5 + T$\emptyset$12
0	1	0	0	T$\emptyset$05 + T$\emptyset$12
0	0	0	1	$\emptyset$PR5 + TM28

EXTS, RRPS, NEXT & MIDS are macro control lines (see later sections) Shifting occurs if the selected shift control is 0. Swapping occurs if the data addressing mode is virtual. (This second condition is hardwired to 1 (absolute) in the mini).

16. ITERATION COUNTER (1 BIT)

Loads of the iteration counter are accomplished through macrocontrol. Decrementing of the counter is controlled by this 1 bit field. A "0" will disable the decrement function. A load caused by other control will override this field.

17. MACRO CONTROL – MODIFIER FIELD (7BITS)

Many registers exist which are loaded in one ROM step out of all or are loaded based on a condition. Other control

lines are unique to one instruction. Thus, a field is
provided which enables one of 32 control lines to be selected
in a particular ROM Step. Not all are defined at this
time, but those for the MINI are described.

A two bit modifier field provides second level control
for some of the macros. The following macros have been
defined thus far.

1) ITST - Interval Timer Step. Control of the interval
   timer is modified during execution of an Interval
   Timer Control Instruction.

2) TSEN - A special register is selected to appear on
   the TMBUS according to the modifier field.

RMD0	RMD1	Selection
0	0	Interval Timer (for store interval timer)
0	1	Mask Constant (for bit test instructions)
1	$\emptyset$	Escape Address (for excape codes)

3) PROS - The Halt flop is reset for a proceed instruction.

4) RRPS - Register Replacement Step. The INDR and MREF
   flops are set according to TB28 and 17. SPD is loaded.
   HWSL is reset if no shift is defined for the address selector.

5) MSPS - Increment SPR. This is used in load and
   store multiple SP instructions.

6) FSTP - Main fetch step. The OPR, INDR, MREF, PMAP
   registers are loaded from TM0-7, 12, 32, 33. SPR is
   loaded from TM8-11.

   HWSL is set to 1 if this is a literal. Memory read,
   if specified, is inhibited for literals. The instruction
   trace trap is set if EXTI is 0 and TM34 is 1.

7) TRPS - Trap Step. The trap being honored is placed
   on the TMBUS. Its value is stored into the Pending
   Trap register PTR. The flop representing the trap
   being honored is reset. The TRPE flop is set.

8) TRSP - TRS steps. These perform the TRS and TRSK
   instructions.
        RMD selects one of two operations. When a 0, the
   present trap register is placed on the TMBUS along with
   the Halt and Kernel registers. These registers are

modified if RMD0=1. The present trap number
is set to the pending trap number if TRPE is set. When
RMD1=1, the P source register is placed on the bus. It
is loaded from I-source if RMD0=1 and EXTI = 1.

9) RSPP - These return the Stack - RMD1=0 returns the TMBUS
to the P-source register. RMD1=1 loads the trap and
Kernel registers from the TMBUS. According to the op-
code, the halt flop is reset or loaded from the TMBUS.

10) ØVFS - An overflow equation selected by RMD0 - 1 is
allowed to trap.

RMD0	RMD1	Overflow Equation
0	0	$AUOO$. $AUAD$
0	1	$AUOO$
1	0	$\overline{ADBZ}$ + $AUOO$
1	1	NOT USED

11) EXTS - An external interrupt is being processed. EXTI
is set. I-source is loaded from the channel.

12) MIDS - Memory Indirect Step reloads INDR and MREF
from TM bits 12 and 32. HWSL is set to 1 if a literal
is indicated.

13) SHFT - The ITC is loaded from TB26-31 for shifts.

14) ØBFS - One of four actions are selected according to
the modifier field.
   1) RMD0-1 = 00 - The output logic sends a data word to
      the active source with transmission type 011.
   2) RMD01=01 - The acknowledge line is raised on the
      input bus.
   3) RMD0=1. A command is sent. The destination is set
      to active source if the destination specified is FE.
      The transmission number is set to 100 or 101 depend-
      ing on RMD1= 0,1 respectively.

15) SHWS - The HWSL flop is set.

16) TTRS - Transfer if true. One of 16 conditions is selected according to the sequence control field RSQ0-3. The conditions are:

0) ITCZ
1) AD15
2) AD00
3) ADZF
4) CHFF
5) EQFL
6) ∅BSY
7) DATA
8) TM16
9) TMSG
10) MREF
11) EXTI
12) PAMF
13) IBEL   (IB00)
14) O
15) AUAD

If the condition is true (1), the address field, RNA0-9, is used as the transfer address (note that bits RNA0-1 are set to 00 in the MINI ROM). Otherwise, one of four alternate actions is taken according to RMD.

RMD0-1		Alternate Transfer
0	0	Present Address + 1
0	1	RNA0-8, $\overline{RNA9}$
1	0	STC0-9 (R∅M Stack Register)
1	1	spare

17) TFLS - Transfer if false. This acts as does TTRS, but transfers if the selected condition is false (0).

18) ILIT - An illegal instruction trap is generated.

0   N∅∅P - This is a macro which is reserved for no operations.

19) SSPS - The parity mask flop is loaded.

18. Sequence Control (4 bits) - Next address (10 bits)

This field acts with macros TTRS and TFLS above as described. When neither of these macros is selected, a special sequence condition is defined. The equations for these specials will not be detailed, but they have been assigned to specific codes.

0) UNCONDITIONAL TRANSFER TO RNA

1) UNUSED

2) RRDMEM (RMEM) - This is one of a number of fetchcycle

sequencings not delineated here. The name references a function used in the APL simulations.

    3) ROPCD (RPCD) - Trnasfer to one of many locations based on the operation code.

    4) DMFT - Transfer to 0, DAMF, RNA2-9. This selects a location in the MINI ROM or channel ROM depending on the data addressing mode.

    5) PMFT - Transfer to 0, PAMF, RNA2-9. This selects a location in the MINI ROM or channel ROM depending on the configuration.

    6) RCØMP -(CØMP) - A transfer to one of two locations is performed according to a complex condition. RMD is used to further define this, as is the opcode.

    7) RTRAN (TRFR) -This is similar to RCOMP, but uses opcode control only. It is used for conditional transfers.

    8) RREGIN (RGIN)

    9) RINIM (RNIM)

    10) RCOMP4 (RCMP) - Transfers to 00, RNA2-7, ADZF, EQFL

    11) R REGAD

    12) R RDOP

    13) RMIND

    14) RC3MU - Used for multiply to perform a conditional three way branch when RMDO-=0 and for shifts when RMDO=1.

    15) NEXT - This causes, in addition to a conditional multiway transfer, the setting and/or resetting of some control flip-flops. The output of the NEXT circuitry is Tri-stated to allow the MINI ROM to execute NEXT which selects virtual fetchcycle when PAMF=1 in the channel config-uration.

The ROM thus far defined is 70 bits. The PMU MINI may set RAU1 to 0 and RNA0-1 to 00 to reduce this to 67 bits. also,

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ROM Format

Presently identified fields can be pictured as follows:

0 2	3 5	6 9	10 11	12 13	14	15 16	17
P REG	IA REG	IB REG	AD BUS	DTBUS	ADSWITCH	AUBUS	SP WRITE
3	3	4	2	2	1	2	1

18 19	20 25	26	27 31	32 39	40 43	44
TM CYCLE	SP ADDRESS	M BUS	TM SELECT	AU	TM ADDRESS SELECT	ITC
2	6	1	5	8	4	1

45 47	48 52	53 54	55 65	65 68	69
TM, SP SIGNS	MACRO CONTROL	MACRO. MOD.	NEXT ADDRESS	SEQUENCE CONTROL	RS
3	5	2	10	4	1

S. Nissen
Dept. 7675/Ext. 2261

SN:mam
dc.-   E. Aaronson   D-B54
       M. Hereth   D-B54
       J. Hanlon   D-B54
       S. Nissen   D-B54 (3 copies)
       S. Wallach   D-B54 (2 copies)
       Dept. File   D-B54

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S. Nissen
Dept. 7675/Ext. 2261

SN:mam
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     J. Hanlon   D-B54
     S. Nissen   D-B54 (3 copies)
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