Quantum

PRODUCT DESCRIPTION

TECHNICAL REFERENCE MANUAL

Q500

5¼" Media Fixed Disk Drive

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Q500 SERIES®
DISK DRIVE

Technical Reference Manual

81-50466 Rev A

September 1984

QUANTUM CORPORATION

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WARRANTY

Quantum Model Q500 series disk drives are warranted against defects in material and workmanship for a period of one year from the date of shipment. The warranty includes parts and labor. This is a limited warranty and further details can be obtained from your Quantum sales representative. All requests for service should be directed to the Quantum service center in your area.

PATENTS

Product described herein is covered by Patent #4396959 and other U.S. and foreign pending patent applications.

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REVISION CONTROL RECORD

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PREFACE

DOCUMENT OBJECTIVE

The Quantum Q500 Disk Drive Technical Reference Manual describes the principles of operation, major circuits, component parts, maintenance, and applications of the Q500 drive.

INTENDED AUDIENCE

This manual is intended for experienced Design Engineers, Applications Engineers, Software Programmers, and Repair Technicians using the Q500 for OEM applications.

DOCUMENT STRUCTURE

Section 1 describes the principles of operation of the drive mechanics and electronics.

Section 2 contains schematics of the Q500 circuits.

Section 3 describes errors and media defects, self-diagnostics, track format, and other applications.

Section 4 summarizes maintenance procedures.

Section 5 includes an exploded parts diagram of the major subassemblies and a complete parts list for the Drive Control PCB.

ASSOCIATED DOCUMENTS

Additional information on the Q500 drive, including general specifications and installation procedures, is contained in the *Q500 Product Description OEM Manual.*

SECTION 1
PRINCIPLES OF OPERATION

1.1 MODEL Q500 BLOCK DIAGRAM

Figure 1-1 shows a block diagram of the Model Q500 Disk Drive. The spindle is driven from a dc motor mounted on the spindle shaft. The dc motor is powered by the +12V supplied to the drive via the P3 connector. The motor spindle rotates the disk at 3529 rpm. The read/write head stack assembly is mounted directly on the rotor of the rotary positioner assembly (proprietary to Quantum). The rotary positioner is driven by power drivers controlled by microprocessor-based circuitry on the control printed circuit board assembly (PCBA). Head stack track and position feedback signals are provided by an optical encoder and glass scale assembly via the encoder PCB. On-track thermal compensation is obtained from servo data written in a 290 μs wedge on Physical Disk Surface 3. Optical position feedback and a servo wedge (which gives a hard track center) allow all the disk surfaces to be used for data storage and yet remain soft-sectored. Read/write signals are obtained from or written to the disk via the head switching matrix on the encoder PCB and the heads mounted on the head stack. The drive control PCB contains the electronics for servo position decoding, the head stack positioner drive, the microprocessor that controls these functions, and the read/write amplification and drive.

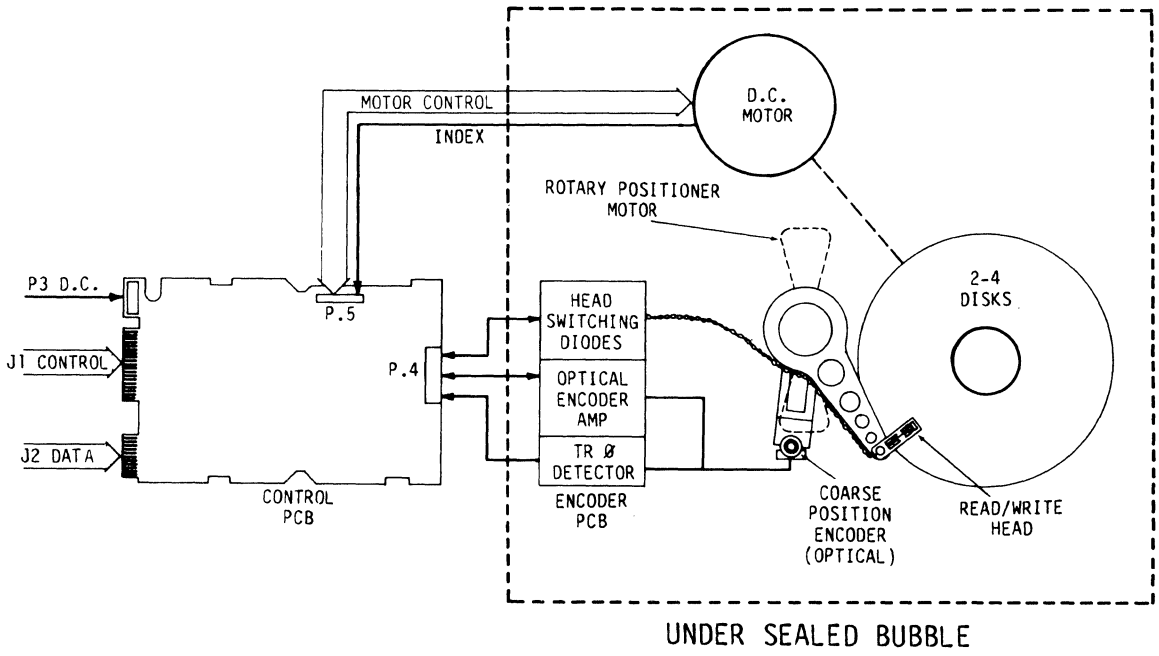

FIGURE 1-1
Model Q500 Block Diagram

1.2 MODEL Q500 DRIVE MECHANISM

The drive's mechanical subassemblies are sealed under a metal bubble. None of these subassemblies is adjustable and none can be repaired in the field. Refer to Figure 1-2 for an illustration of the mechanical components of the drive.

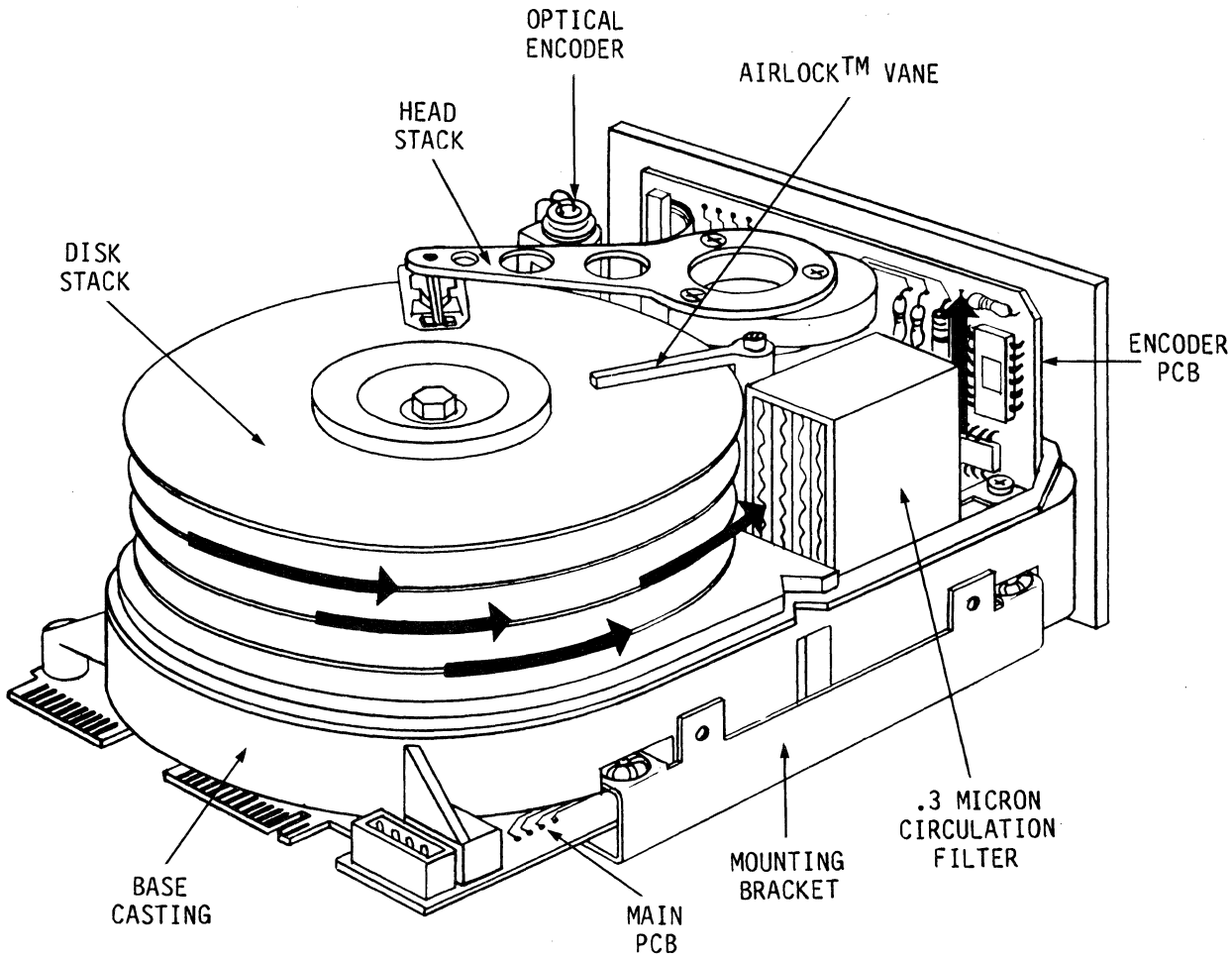

FIGURE 1-2
Model Q500 Mechanical Layout

1.2.1 OPTICAL ENCODER

The optical encoder is the position-sensing device that provides feedback for the closed-loop system that controls head stack positioning. The encoder assembly is clamped to a post in the base of the drive. The encoder consists of a housing, an infrared LED, an optical reticle, and a photo diode matrix.

The infrared LED is mounted in the housing above the reticle. The reticle, which sits above the photo diodes, acts as a light mask to control the amount of light reaching the photo diodes. The reticle is matched to an optical scale mounted on the head stack. As the head stack moves, light reaching the photo diodes varies according to the match between the glass scale and the reticle; the light intensity is decoded into position information. The clearance and angular position of the reticle relative to the scale are adjusted during manufacture.

1.2.2 ROTARY POSITIONER ASSEMBLY

The positioner used in the Q500 is a rotary torque actuator (a design proprietary to Quantum). The rotor of the positioner consists of two flat, triangular coils. These coils are molded so that they are perpendicular to the spindle shaft. This assembly is then mounted to the base so that the coils are suspended in a permanent magnetic field. The field is created by two magnetic segments — one mounted above the coils and one below. The segments are polarized so that current passing through the coils causes the positioner to rotate. Variations in current cause the positioner to rotate in either direction or to stop.

1.2.3 HEAD STACK ASSEMBLY

The head stack assembly is mounted directly on the rotor and consists of the heads, head arms and their counter balances, and the optical scale. The counter balances are castings whose shape and weight ensure that the center of the mass of the entire stack is at the center of the mounting hub. The optical scale is bonded to the second-to-lowest counter balance. the optical scale provides position feedback via the optical encoder (see section 1.2.1). The heads are Winchester slider-types with a .0011 inch track width. They are mounted to spring steel flexures staked to the head arm. The head conductors are flex cables routed in plastic guides and attached with an adhesive. All head stack assemblies have an upper and lower head arm assembly and may have one to three dual head arm assemblies A spring is attached from the head stack assembly to the casting and is used to pull the heads into the landing zone when no power is applied to the actuator.

1.2.4 DISK STACK ASSEMBLY

The disk stack assembly is secured to the dc spindle motor which is bolted to the base casting. The disk stack consists of disks, disk spacers, a disk clamp, and a grounding system for the spindle. Depending on the capacity of the drive, two to four disks and spacers are placed on the disk mounting hub and are clamped in place. The disks are made of an aluminum alloy with a magnetic oxide coating, which is polished and lubricated. The lubrication prevents head and media wear when the heads are in contact with the disk surface. Such contact only occurs outside the data area and when the disks are not rotating. The grounding system for the spindle consists of a steel button bonded to the bottom of the dc motor and a carbon button bonded to a spring contact on the control PCB.

1.2.5 BASE CASTING ASSEMBLY

The base casting is a single piece of cast aluminum alloy. The drives subassemblies are mounted on this base. It has two machined holes for mounting the motor/spindle assembly and the positioner assembly. The outside top edge is flat to ensure an airtight seal with the metal bubble cover. The optical encoder, encoder PCB, and the upper magnet plate for the rotary positioner assembly are mounted inside the bubble area. Mounting holes are also provided, outside the bubble area, for the control PCB and faceplate. A grounding lug allows connection between the chassis ground and logic/power ground if desired. Shock mount brackets are provided for isolation from shock and vibration.

1.2.6 DC DRIVE MOTOR

The Q500 is equipped with a dc spindle drive motor. The motor is controlled by a single-chip microprocessor. The dc motor assembly is bolted to the base casting and consists of a dc motor, a spindle-bearing assembly, a disk-mounting hub, and a ferro-fluid magnetic seal. This seal prevents outside air from entering the drive through the bearing bore or along the bearing shaft. Mounted in the dc motor are three Hall effect devices and an optical transducer which provide motor commutation, servo timing, and position feedback to the microprocessor. An index signal is generated from an LED/phototransistor pair; output is generated as a TTL lever from the motor. The LED shines light on the rim of the motor rotor; this light is reflected and the phototransistor detects it as INDEX when the unpainted portion of the rotor rim passes across the detector pair.

1.2.7 EMI BAND

A Winchester drive is sensitive to electromagnetic interference (EMI) due to the low signal level at the read/write heads. Therefore, it is necessary to shield the heads from EMI. On the Q500, most of the shielding is provided by the base casting and the cast cover. However, at the intersection of these two castings, a gap caused by the sealing gasket requires shielding. This is provided by a band (wire mesh attached to a rubber strip) placed over the gap and clamped in place with a stainless steel strap.

1.2.8 AIR FILTRATION

Because the Model Q500 is a Winchester-type drive, the heads fly very close to the media surface. The nominal flying height is 18 microinches, or roughly 1600 times smaller than the diameter of the period at the end of this sentence.

It is absolutely essential that the air circulating within the drive be kept clean and free of particles. The drive is assembled in a Class 100 purified air environment and then is sealed in a metal bubble. During the life of the drive, the rotating disks act as an air pump to force the air through two internal filters. Figure 1-2 shows the airflow in the enclosed area of the drive. The lowest pressure area within the drive is located at the top in the center of the spindle. A 0.3 micron breather filter is bonded in this area of the bubble. This filter allows outside air into the bubble enclosure to equalize internal and external pressures. The highest pressure area within the drive is located at the outer edges of the disks. Bonded to the AIRLOCK base at this location is another 0.3 micron filter called the circulation filter. Air is constantly pumped into the side of the filter nearest the disks and then filtered and expelled from the side of the filter away from the disks. This area of the drive is at a lower pressure than at the edge of the disks so that air will circulate through the filter. This ensures a continuous flow of filtered air as soon as the disks start to rotate. Because stringent cleanliness is required, the bubble and seals should not be tampered with.

1.2.9 AUTOMATIC ACTUATOR LOCK

A dedicated landing zone is used in the Q500 to ensure data integrity and prevent damage during shipment. AIRLOCK is an entirely mechanical means of locking the head stack in the landing zone; it is proprietary to Quantum. The AIRLOCK consists of an airvane mounted close to the edge of the disk stack, with an arm that intersects the actuator to hold the head stack in the landing zone when the disk is not rotating. As dc power is applied to the motor and the disk stack starts rotating, an airflow is generated around the disk. As airflow increases with disk rotation, the airvane and its arm will rotate, allowing the head stack to move freely out of the landing zone.

NOTE

The air-actuated lock (AIRLOCK) takes an average of 22 seconds and a maximum of 27 seconds to lock the actuator after dc power is removed.

1.3 DRIVE ELECTRONICS

1.3.1 GENERAL FEATURES

This section briefly describes the functions performed by the Model Q500 electronics. The drive electronics contain the following circuitry:

Interface Buffers

The interface buffers are drivers and receivers that buffer the control and data signals between the drive and the drive controller. The function of the various interface signals is described in Sections 1.3.2 and 1.3.3.

DC Power Circuits

The dc power circuitry provides power decoupling and regulation as well as the power-up reset signal.

Read/Write Circuits

The read/write circuitry provides the write current to record data and the circuits to detect recorded data.

Encoder PCBA

The encoder printed circuit board assembly contains the head switching matrix and the circuits that generate track position signals from the signals provided by the scale and optical encoder.

Servo Position Detection

The servo position detection circuitry uses the signals from the factory-recorded servo to fine position the heads.

Actuator Drive Circuits

The actuator drive circuits provide the power to drive the actuator to position the head stack assembly.

Actuator Microprocessor

The actuator microprocessor is a single-chip processor which controls the drive during its various modes of operation and uses the output of the encoder PCBA and servo position-detection circuitry to generate track position signals used to position the actuator.

Motor Microprocessor

The motor microprocessor is a single-chip processor which controls start-up and speed of the dc motor. It also provides index timing for the interface and performs write fault detection.

Motor Drive Circuit

The motor drive circuit provides the power to drive the spindle motor.

1.3.2 DATA INTERFACE

General Description

There are three signals on the data interface cable. None of these signals is multiplexed. One signal, DRIVE SELECTED, is a TTL open collector output. Two of the signals are differential: MFM WRITE DATA (input) and MFM READ DATA (output). The differential signals have the electrical characteristics described below.

Driver output current is 50 mA maximum on the driven line and 50 mA on the nondriven line. The output range is 0.5 to +3.5 Vdc. The receiver input voltage is 0.8 V to +2.0 Vdc on either line. The circuit will detect a differential voltage of 30 mV. Table 1-1 shows the pin designations of the data signals.

TABLE 1-1
Data Cable Pin Designations

GROUND RETURN	SIGNAL PIN	SIGNAL NAME
2	1	−DRIVE SELECTED
4	3	NA
6	5	NA
	7	RESERVED (To J1 Pin 16)
8		
	9	NA
	10	NA
11		
12		
	13	+MFM WRITE DATA
	14	−MFM WRITE DATA
16		
	17	+MFM ~~WRITE~~ DATA
	18	−MFM ~~WRITE~~ DATA
19		
20		

Driver Receiver

Figure 1-3 shows the recommended differential data signal driver/receiver combination. The maximum recommended cable length is 20 feet (6 m).

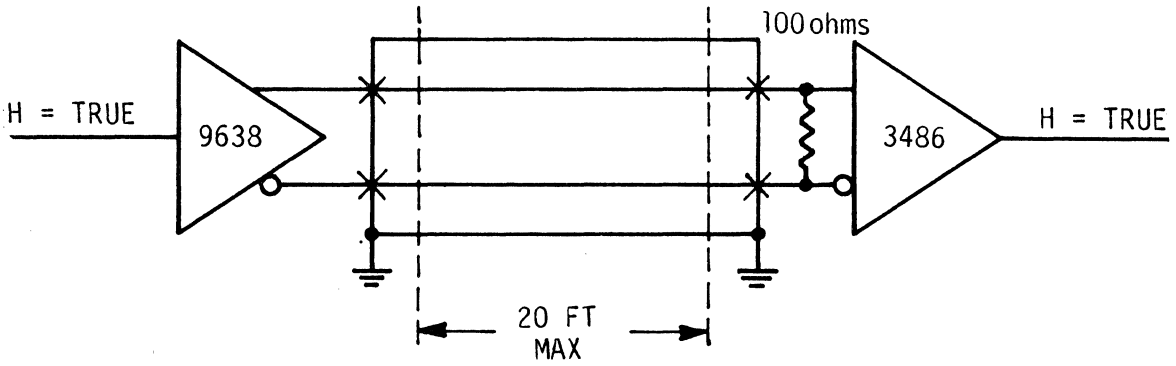

FIGURE 1-3
Data Signal Driver/Receiver

Data Signal Descriptions

The function of each of the three data signals is described below.

- MFM WRITE DATA — Provided the drive is selected and there is LO level on the WRITE GATE control line, the transition of the +MFM WRITE DATA line to a line more positive than the −MFM WRITE DATA line will cause a flux reversal to be written on the disk. Figure 1-4 shows the WRITE DATA timing.

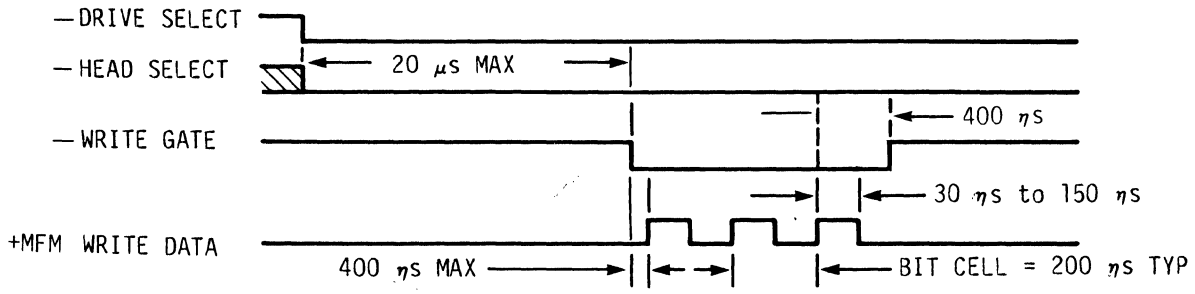

FIGURE 1-4
MFM Write Data Timing

- MFM READ DATA — Provided the drive is selected and there is a HI level on the WRITE GATE control line, the transition of the +MFM READ DATA line to a line more positive than the −MFM READ DATA line indicates that a flux reversal was detected on the track. Figure 1-5 shows the READ DATA timing.

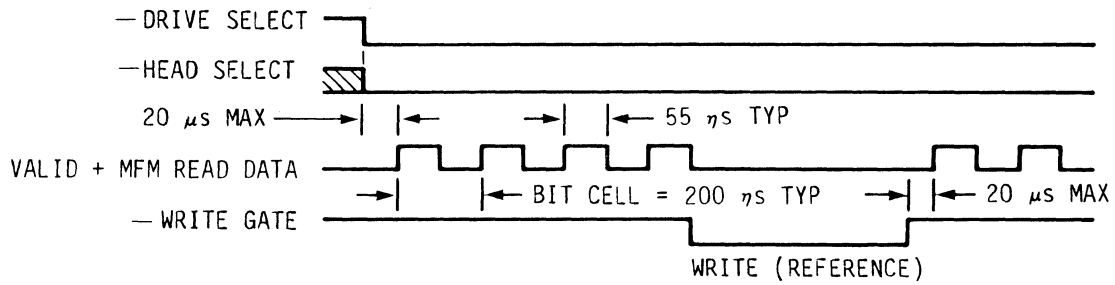

FIGURE 1-5
MFM Read Data Timing

- DRIVE SELECTED — This open collector line will go to a LO level when this drive is selected by the appropriate drive select line.

1.3.3 CONTROL SIGNAL DESCRIPTIONS

Unless otherwise stated, all control signals are enabled with DRIVE SELECT. The function of each of the fifteen control signals is described below. Table 1-2 summarizes the pin designations for the control signals.

TABLE 1-2
Control Cable Pin Designations

GROUND RETURN	SIGNAL PIN	SIGNAL NAME
1	2	-N/A (Reduced write current done automatically by microprocessor)
3	4	-Head Select 2^2
5	6	-Write Gate
7	8	-Seek Complete
9	10	-Track Ø
11	12	-Write Fault
13	14	-Head Select 2^0
15	16	-Reserved (to J2 PIN 7)
17	18	-Head Select 2^1
19	20	-Index
21	22	-Ready
23	24	-Step
25	26	-Drive Select 1
27	28	-Drive Select 2
29	30	-Drive Select 3
31	32	-Drive Select 4
33	34	-Direction In

Input Signals

- DRIVE SELECT 1,2,3, or 4 — A LO level on this line logically connects the drive to the control lines. Only one drive select line may be active at a time. The active DRIVE SELECT line selects the drive which has the matching drive select jumper installed.

- HEAD SELECT 2^0, 2^1, 2^2 — these three lines provide a binary code to select one of the heads. 2^0 is the least significant bit. The heads are numbered 0 through 7. When all lines are LO, head 7 is selected. Conversely, if all lines are HI, head 0 is selected.

- DIRECTION IN — a LO level on this line defines the R/W head motion as in, or toward the center of the disk (away from Track 000). A HI level on this line defines the R/W head motion as out, or toward the edge of the disk (toward Track 000). See Figures 1-6 and 1-7 for timing direction.

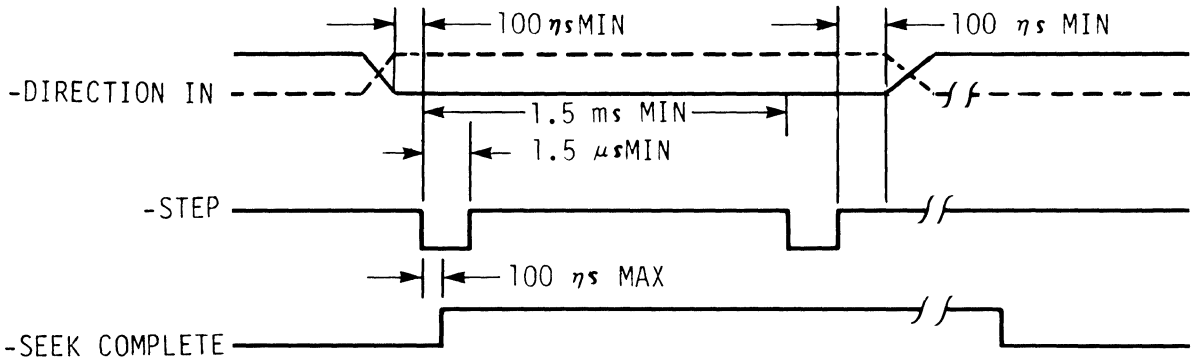

FIGURE 1-6
Single Step Mode Timing

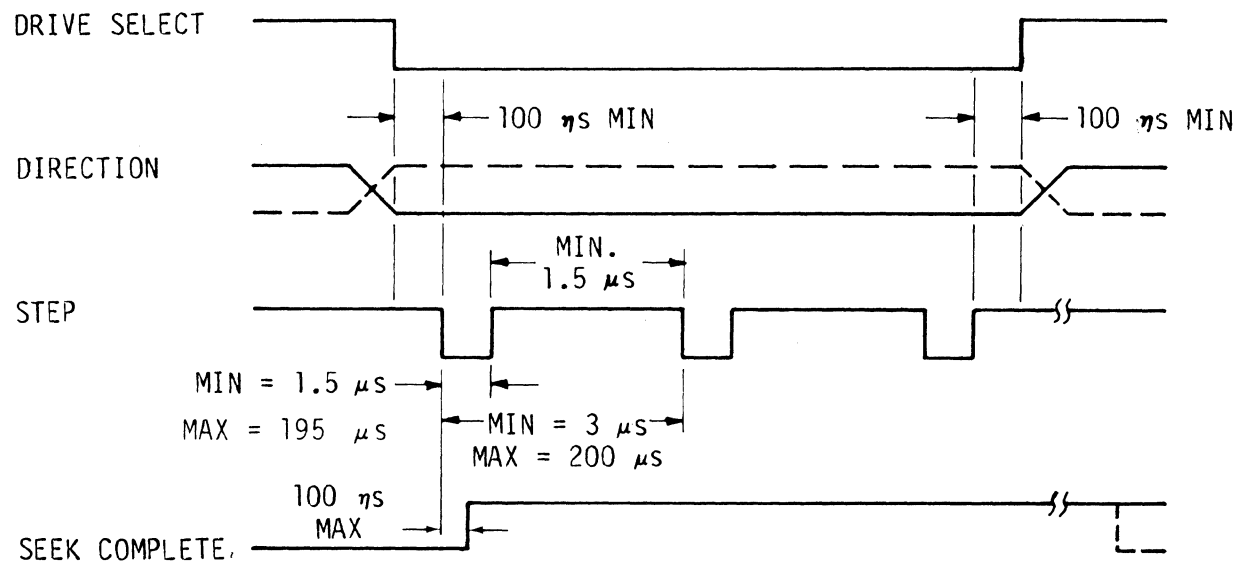

FIGURE 1-7
Buffered Step Mode Timing

- STEP — a LO pulse of at least 1.5 μs duration on this line causes the R/W head to move in the direction defined by the DIRECTION IN line. If step pulses occur at an internal equal to or greater than 1.5 ms between pulses, the heads will move at approximately the rate of incoming steps (single step mode). If the incoming step pulse rate is equal to or less than 200 μs between pulses, the pulses are buffered into a counter and motion occurs after the last step pulse is received (buffered mode). See Figures 1-6 and 1-7 for Step Timing.

- WRITE GATE — a LO level enables the write circuitry which allows data to be written on the disk.

Output Signals

- READY — a LO level on this line indicates the disks are up to speed and the interface signals are valid. When READY and SEEK COMPLETE are true, the drive is ready to read, write, or seek. (If a seek error occurs, READY will go false for approximately 60 μs. Then the drive will recalibrate itself and return the heads to TKØ, which can take up to 9 seconds.)

- WRITE FAULT — a LO level on this line indicates any of the following conditions have been sensed, and writing and reading have been inhibited:

  1. DRIVE SELECT is selected, WRITE GATE is true, and no write current is detected.

  2. Write current is detected and either WRITE GATE or DRIVE SELECT is unselected.

  3. DC voltages are too low, thresholds are set below the normal ranges of operation.

  4. Writing is attempted on heads 7 and 8 (in a 30-Mb drive) or heads 5, 6, 7, and 8 (in a 20-Mb drive).

  WRITE FAULT can be cleared by deselecting and reselecting the drive, or by cycling the power off, then on.

- INDEX — a LO pulse of approximately 50 μs once per revolution (or every 17 ms) indicates the beginning of a track. The leading edge of this pulse should be used for all timing requirements. See Figure 1-8 for INDEX timing.

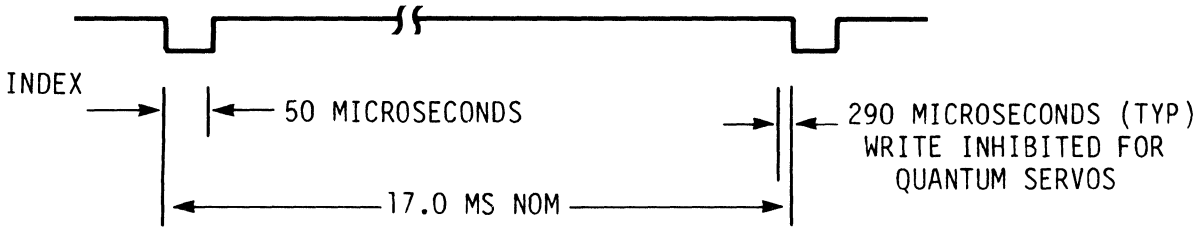

FIGURE 1-8
Index Timing

- SEEK COMPLETE — a LO level on this line indicates the R/W heads have settled on a cylinder and a read, write, or another seek may take place. Writing is inhibited while this signal is false (HI). (Seek complete may go false during recovery from a seek error.)

- TRACK Ø — a LO on this line indicates that the R/W heads are positioned at cylinder 000 (the outermost cylinder).

Figure 1-9 shows the general timing relationships between some of the control signals found in the Model Q500 during the POWER ON cycle of the drive.

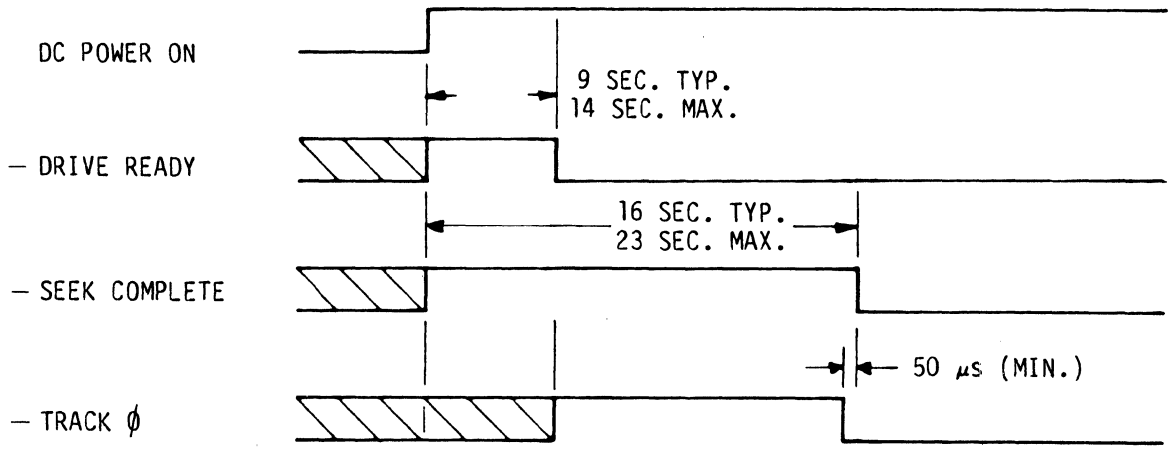

FIGURE 1-9
General Control Timing Requirements

1.3.4 POWER REQUIREMENTS

The voltage and current requirements of the dc power supplied to the drive are listed in Table 1-3. No power sequencing, either off or on, is required by the Q500. Figure 1-10 shows the start-up current profiles of the drive.

TABLE 1-3
DC Power Requirements

VOLTAGE NOMINAL	**12V**	**5V**
Current		
Typical	2.0A (Seeking)	.7A
Maximum	2.4A (Seeking)	1.0A
Maximum	4.5A (Motor Start 1 s)	
Regulation	±1.2V	±.25V
Ripple and Noise Maximum	100 mV P-P	50 mV P-P

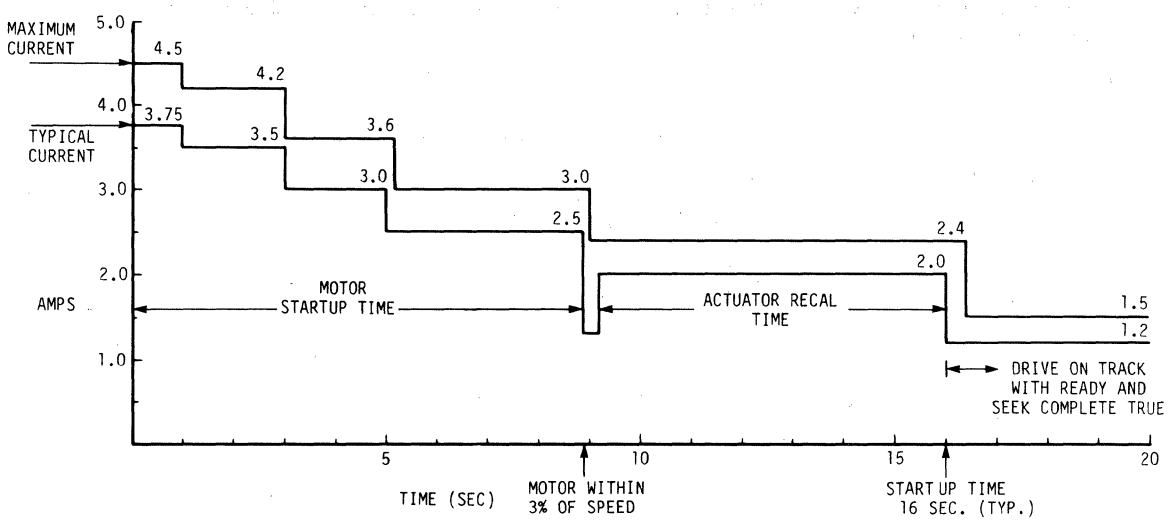

FIGURE 1-10
Drive Start-Up Current Profile (12V line)

1.3.5 INTERFACE AND DRIVE SELECT LOGIC

This logic performs three functions in the Q500:

1. Provides cable drivers and receivers for the interface signal
2. Allows for gating these signals with the DRIVE SELECT line
3. Provides for interface cable terminator on the last drive on the cable

Input signals for HEAD SELECT, DIRECTION IN, STEP, and WRITE GATE control signals are received by a 74LS244 at U15 and may be terminated by installing a 220/330 ohm resistor pack at RN3.

The DRIVE SELECT jumper block and the DRIVE SELECT terminator R46 and R47 are shown in coordinates 7B and 6B in Figure 2-2. Placing a jumper across point A causes continuous selection and is normally used for test purposes. Otherwise, when a LO signal on a DRIVE SELECT line matches with a jumper, reception is enabled of input signals STEP, DIRECTION IN, and HEAD SELECT signals 2^0 and 2^1. Additionally, an active DRIVE SELECT line causes the following to occur:

1. Front plate LED lights.
2. Outputs -SEEK COMPLETE, -TRACK0, -WRITE FAULT, -READY and -INDEX are enabled at interface connector J1.
3. -DRIVE SELECTED output at data cable (J2-1) goes active via U4-11.

The motor microprocessor also uses the state of DRIVE SELECT to determine Write Fault conditions.

1.3.6 ENCODER BOARD

Figure 1-11 is a functional block diagram of the encoder PCB. The board contains the components listed below:

- the diodes used for head switching
- a through-bubble connector (which connects to the head signals, actuator drive signals, and actuator position signals)
- the op amps used to condition the encoder photocell outputs
- the AGC amplifier used to control the infrared LED drive current

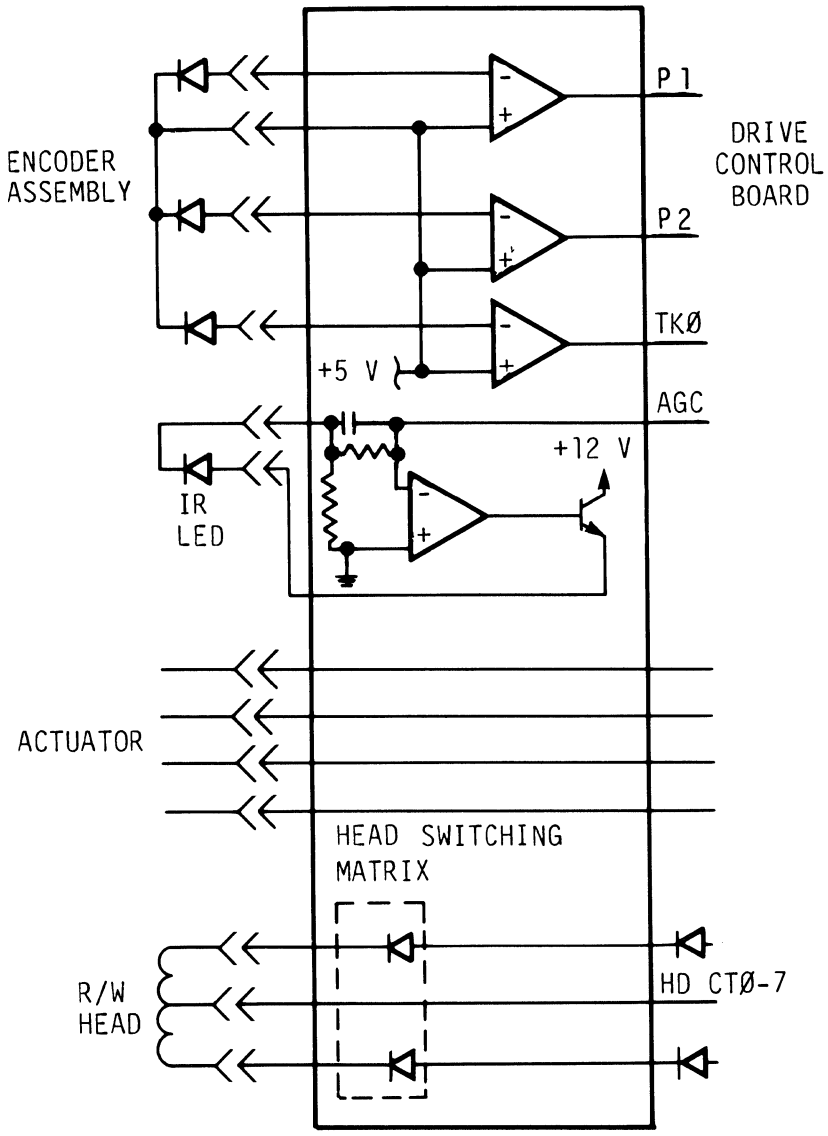

FIGURE 1-11
Encoder PCB Block Diagram

1.3.7 DRIVE CONTROL BOARD

Figure 1-12 is a functional block diagram of the drive control board. The board is mounted on the top of the drive. One end of the drive control board connects to the encoder PCB. The other end of the board has edge contact fingers for control signal and data interface connectors. The drive control board also has connectors for dc power, the dc spindle motor, and the faceplate LED.

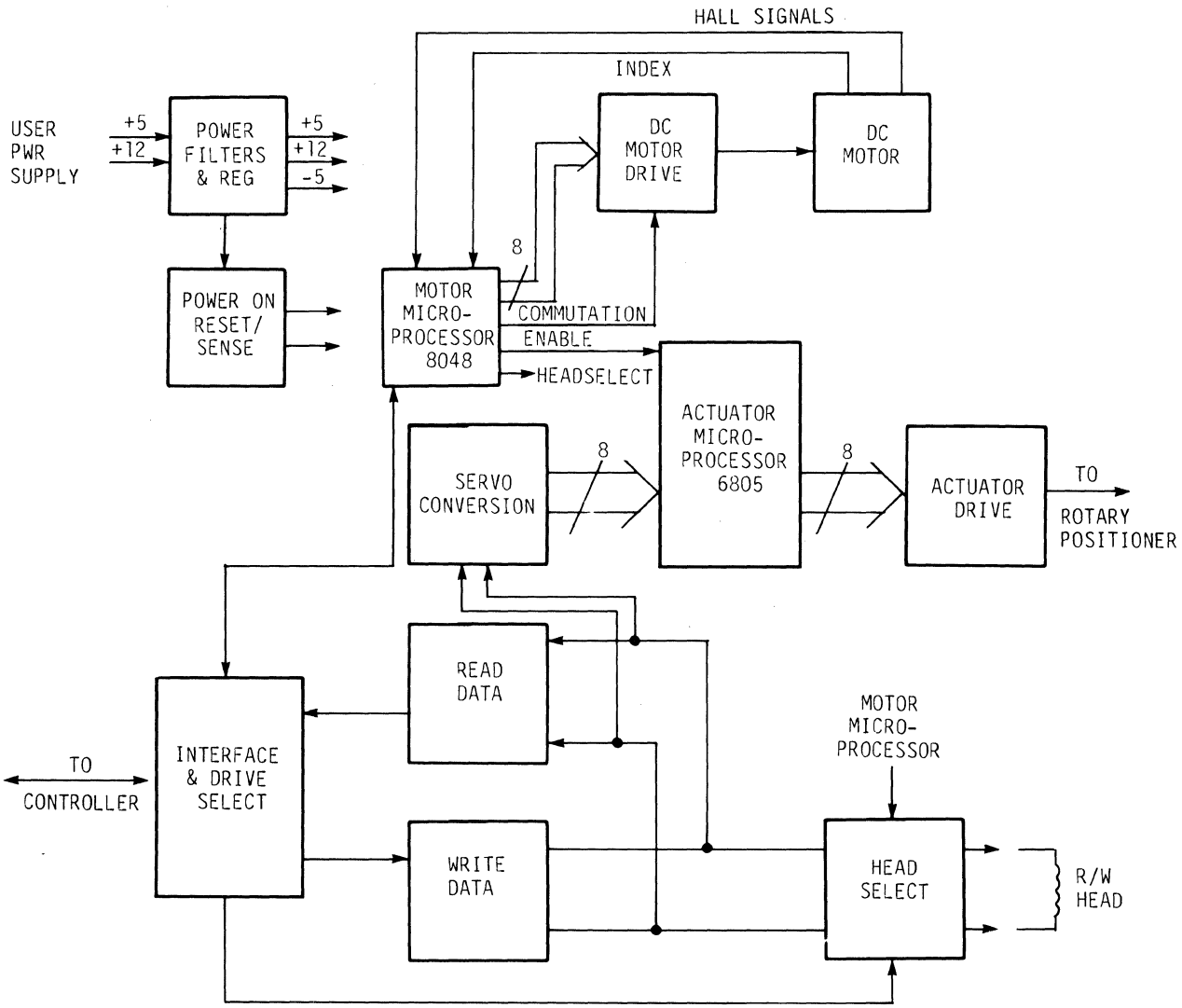

FIGURE 1-12
Drive Control PCB Block Diagram

Applying dc power to the drive starts the dc motor spinning after voltage levels have exceeded the minimum limit determined by the POR circuit. Once the voltage has exceeded this limit, the heads lift off the disk surface and fly above the landing zone. When the motor microprocessor (via the INDEX signal) detects that the dc motor speed is within 3% of nominal speed (3423 rpm), the motor microprocessor generates an UP TO SPEED signal to the actuator microprocessor to recalibrate the actuator to Track 0. When the actuator is recalibrated, the drive sets READY, Track 0 and SEEK COMPLETE signals at the control interface.

When -DRIVE SELECT "X" is driven true and matches the drive select jumper, the drive select logic enables the interface logic to gate control signals to and from the drive. The drive will read or write data on the selected head at the present track, depending on the state of the WRITE GATE line.

The track location of the heads may be changed by selecting the appropriate direction via the DIRECTION IN line and issuing step pulses. The step pulse can be sent in one of two modes: normal (single step) mode in which step pulses are sent less frequently than every 1.5 ms and buffered mode (in which step pulses are sent more frequently than every 200 μs).

1.3.8 AGC CIRCUIT

The AGC circuit is used to compensate for the effects of temperature and aging on the signals generated in the encoder assembly.

Figure 1-13 shows the AGC circuit. Section 1.2.1 describes the mechanical operation of the optical scale, reticle, and photo diode. Section 1.3.11 presents a description of how current is supplied to the LED by the actuator microprocessor.

A 347 Op amp drives the base of the 2N2222, which provides current to the LED.

The LED current, I_D is given by the equation:

$$I_D = I_0 + \frac{V_0}{100\Omega}$$

Since the inverting input is approximately ground,

$$V_0 = I_0\ (3.3\ k\Omega)$$

Therefore:

$$I_D = I_0 + \frac{I_0\ (3.3k\Omega)}{100\Omega} = 34(I_0)$$

The current through the LED is 34 times the DAC current I_o which is:

$$I_0 = I_{REF}\left(\frac{A1}{2} + \cdots \frac{A8}{256}\right)$$

where I_{REF} is provided by a hybrid circuit assembly that compensates for variations of LED intensity due to temperature change.

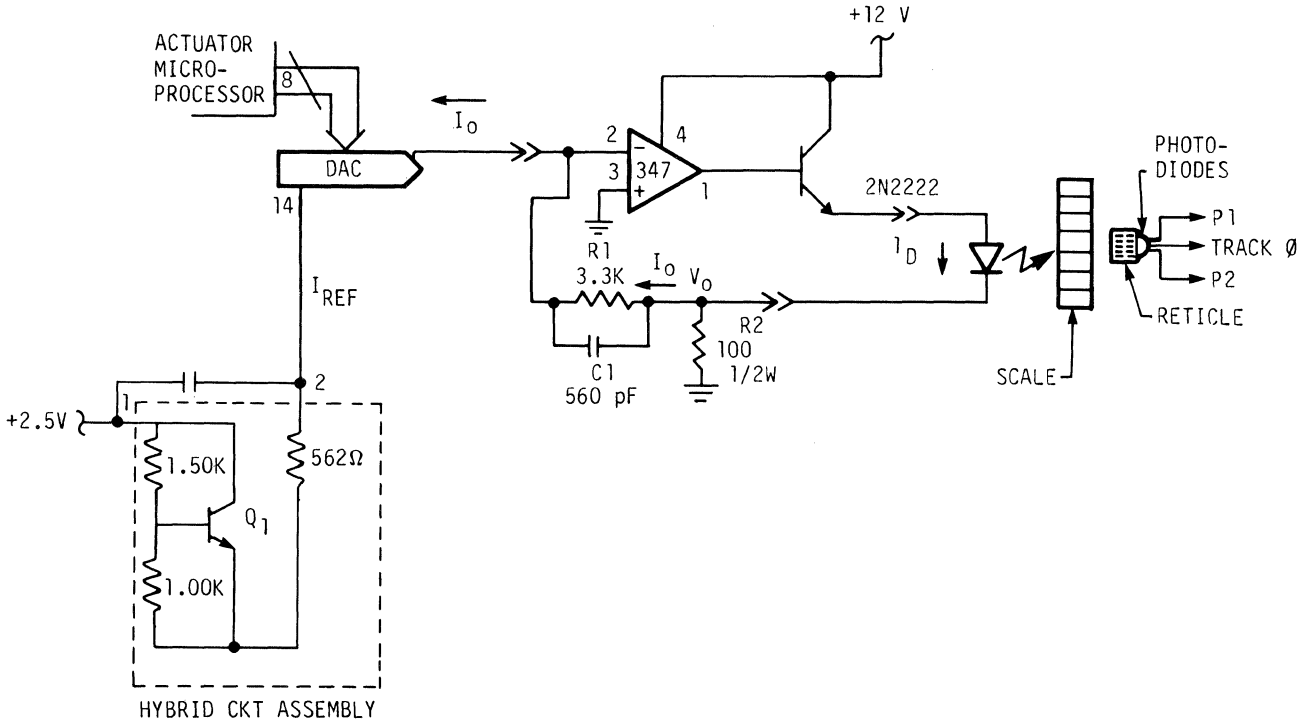

FIGURE 1-13
AGC Circuit

1.3.9 P1 AND P2 GENERATION

Refer to Figure 1-14 for a schematic illustration of P1 and P2 generation.

P1 and P2 are derived from two photo diodes located on the encoder PCB. The resulting signals determine coarse track position and track crossings. Section 1.2.1 describes the mechanical operation of the optical scale, reticle, and photo diode.

As the optical scale moves through the encoder gap, pseudo-sinusoidal signals are generated at P1 and P2 with a 90° phase difference created from the offset windows the reticle provides. The infrared light which passes through the scale/reticle filter causes a current to flow in each photo diode. This current varies since the amount of light detected by the photo diode varies with the movement of the scale. Current flow through the photo diode causes current flow in R3 and R5, which causes the voltage to swing proportionately at P1 and P2.

Sample P1 and P2 signals are shown in Figure 1-15. Four zero crossings (one corresponding to each peak of the signal) occur during a period on P1 and P2, marking the track center value. The track crossings are defined by the high and low switch points which are calculated during recalibration.

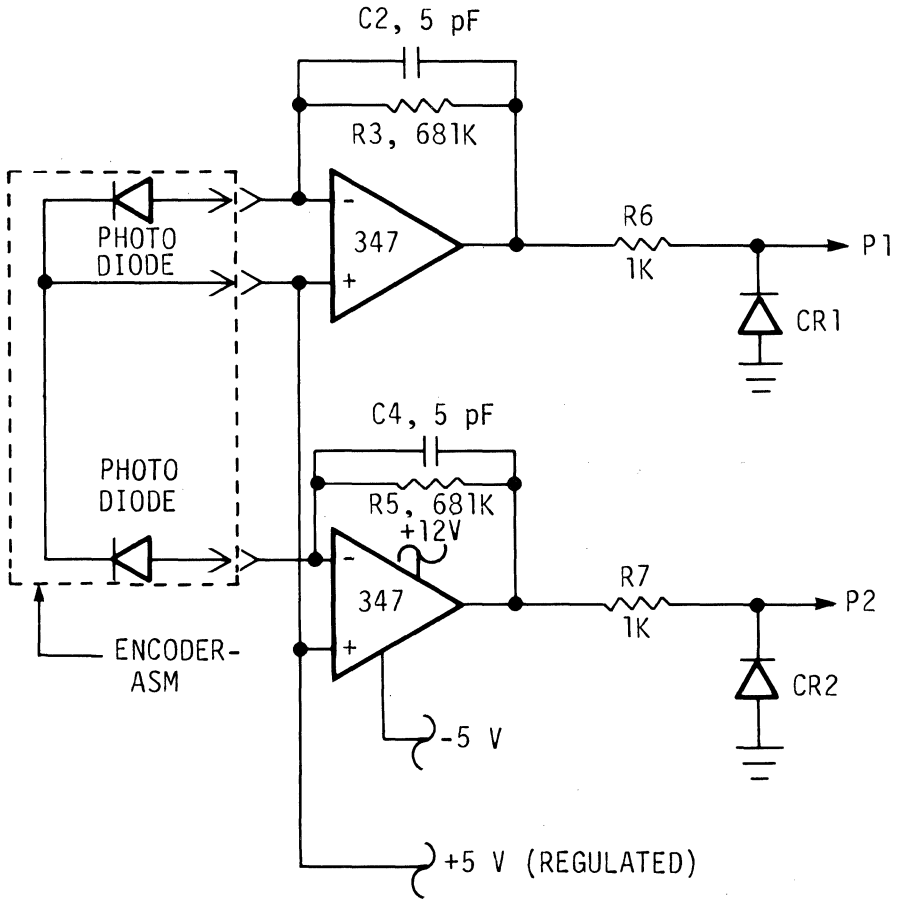

FIGURE 1-14
P1 and P2 Generation

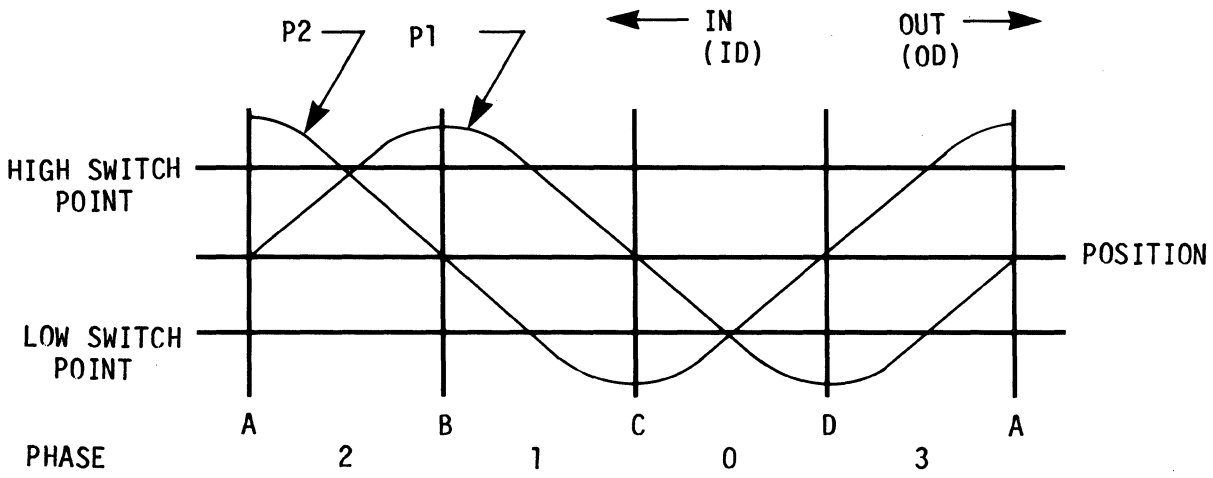

FIGURE 1-15
P1 and P2 Signals vs. Position

1.3.10 TRACK 0

A separate photocell determines Track 0 in the encoder assembly. An opaque rectangle on the scale restricts LED light from the photo diode when the signal is near Track 0. The phases of P1 and P2 signals determine the actual "rough" Track 0 location after the Track 0 signal was switched at some point within the "first" period of the P1 and P2 signals. An op amp is used to detect the photo diode current and drive the input of the actuator microprocessor (see Figure 1-16).

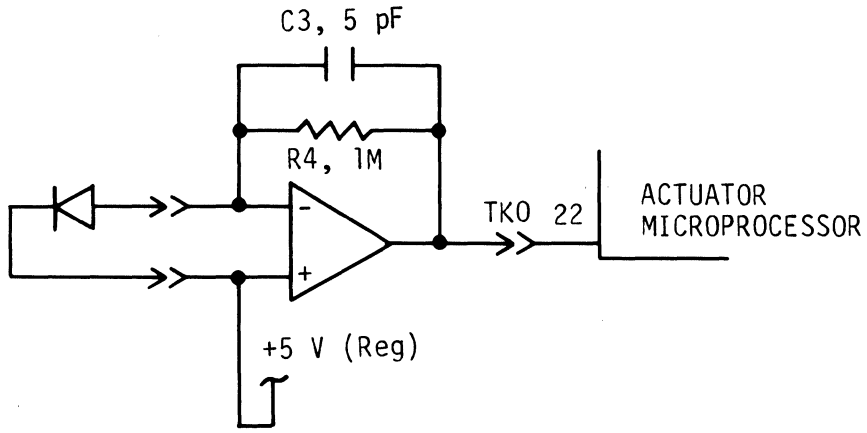

FIGURE 1-16
Track 0 Detector

When light enters the photo diode, current flows causing the output of the op amp to be low. When the light beam is broken by the Track 0 area on the scale, current no longer flows and the output of the op amp is 5V, signaling Track 0.

1.3.11 ACTUATOR POSITIONING CIRCUITS

Actuator Microprocessor

The actuator microprocessor is an 8-bit microcomputer with 112 bytes of RAM, time/counter, and I/O functions. It has 32 I/O lines, four of which are analog inputs (0-5V). The RAM includes registers for the I/O ports and timers. It has 3.8 kbytes of (E)PROM for program storage. Figure 1-17 illustrates the organization of the actuator microprocessor.

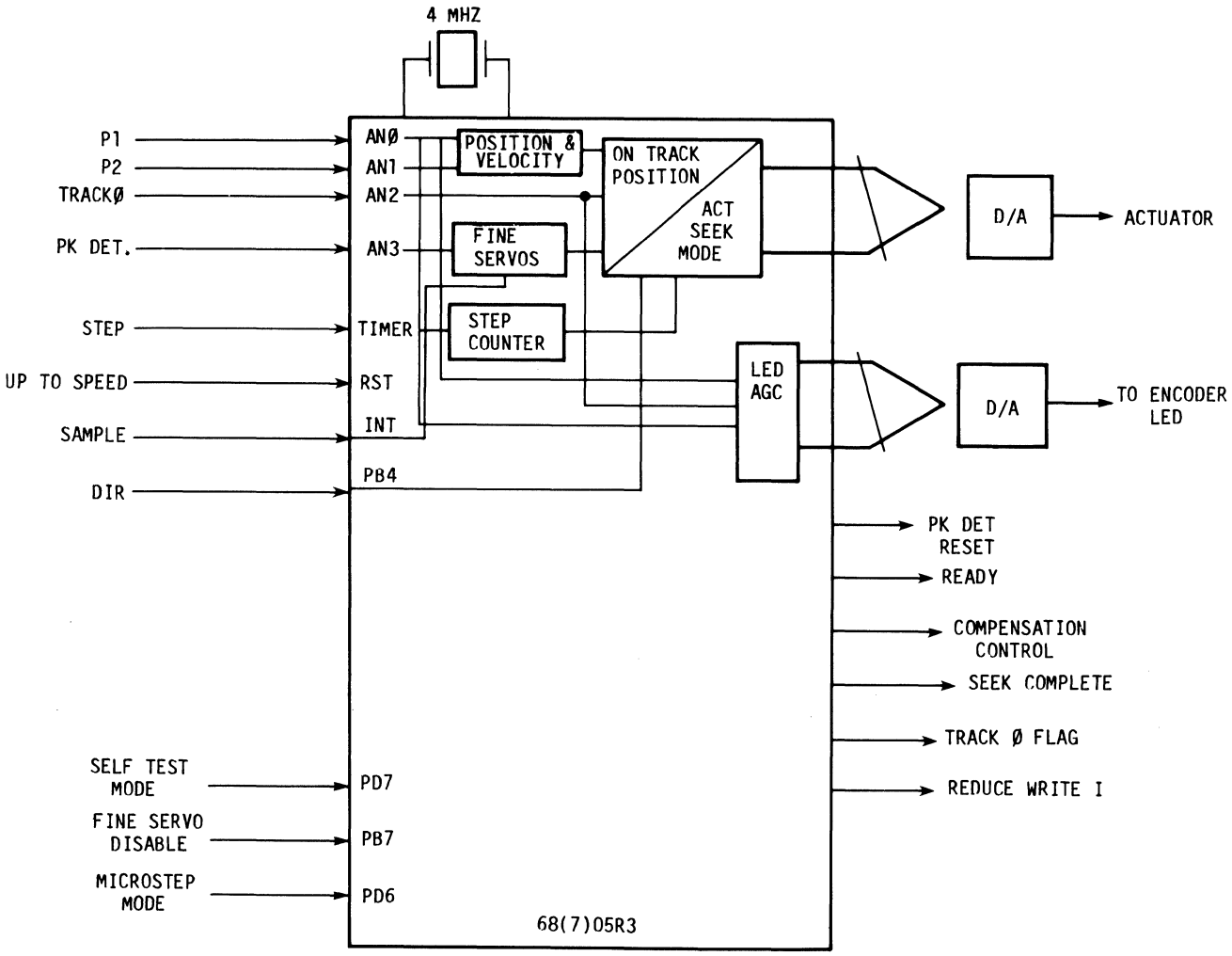

FIGURE 1-17
Actuator Microprocessor Block Diagram

Recalibration

Upon power-up, the microprocessor initializes certain I/O pins, RAM locations, and INTERRUPT lines. It then determines the phase orientation of the position signals, P1 and P2. The initial P1 and P2 position signals are then calibrated by adjusting their respective LED current values. The actuator then is stepped out to Track 0, which is located by the level of the Track 0 photocell and the relationship of the position signals, P1 and P2. A handshake is established with the 8048 dc motor microprocessor for index time. The zone timers are initialized and the zone table offsets are initialized to the present Track 0 values. At this point, positioning control of the actuator is passed to the main loop, SEEK COMPLETE is set, and the drive may seek at the command of the controller.

AGC Function

The actuator microprocessor performs the AGC function at index time and at the end of a seek. The LED current values for the P1 and P2 position signals are increased or decreased based on the value (level) of the Track 0 signal. This Track 0 reference level is originally stored in RAM during recalibration at approximately Track 256. The AGC function is not used when the position signals are within four tracks of Track 0, since the Track 0 signal begins the transition toward +5V beyond this point.

On Track Servoing (coarse)

The drive uses servoing to maintain the actuator in an on-track (stationary) position. The microprocessor controls head position by comparing the difference between the position signal voltage level (P1 or P2) and a reference value. The difference between these values is the error, and a correction value will be output from the microprocessor to the actuator DAC. This coarse servo loop occurs approximately every 150 μs or about 100 times per revolution.

Fine Servoing

The microprocessor applies fine servo correction to the reference value to compensate for changes in head positioning accuracy due to thermal conditions.

Once per revolution, 290 μs prior to USER INDEX, the drive peak detects and samples the factory-written servo bursts. The servo bursts consist of an A and B burst placed between the data tracks on surface 3. When reading the servo bursts (wedge time), the drive switches from the selected head to head 3. See the section on WEDGE and INDEX signals on page 1-69. After SEEK COMPLETE, the microprocessor limits fine servo corrections to the reference value to one DAC step per revolution. Prior to SEEK COMPLETE, the microprocessor sends the full value required for correction.

Thermal Zones

For long term temperature compensation, the 512 cylinders are divided into eight zones of 64 cylinders each. During driver operation the amplitude of the thermal offtrack correction factor (described above) is stored in a zone table in the actuator control microprocessor RAM. The necessity for eight thermal zones was derived from the inner track to the outer track differential thermal offtrack measurements. The quadrature nature of the optical encoder used in the Q500 dictates that the offtrack error will repeat every four tracks. Therefore, within each of the eight zones it is necessary to save four offtrack values, one for each of the four phases of the quadrature encoder (as described above). Thus, the zone table consists of 32 RAM bytes. The requirement for the zone table is to predict the thermal offset based on the lst time the actuator was positioned at that location. When a seek is initiated from one zone to another the current track thermal offset amplitude is stored in the zone table for future use. The destination track thermal offset correction factor is retrieved from the zone table and the head will settle to this predicted offset before seek complete is TRUE. This eliminates the need to wait for the once around fine servo information at the end of each seek, which would otherwise add an average of half a revolution to the seek time.

Upon power up the Q500 will automatically position the actuator at the outermost track, Track 0. Before seek complete is TRUE the fine servo information is read and the actuator position is updated accordingly. This offset amplitude at Track 0 is used to initialize all thermal zone locations. However, it is not accurate enough across the entire surface of the data area and is considered a rough initialization. Upon the first seek to a yet unvisited zone, seek complete will not be TRUE until the fine servo information had been read and the actuator position updated accordingly.

Ramped Mode Seeking

The ramped mode is used for single step seeks and buffered seeks of 17 or fewer tracks. In ramped mode, the actuator arm accelerates linearly until it is half the distance to its destination track.

Then the actuator arm decelerates linearly until it settles on the destination track. The actuator microprocessor controls positioning during a ramped mode seek by looking at the positive and negative slopes of the P1 and P2 signals (analog inputs).

When the STEP counter is loaded with fewer than 18 STEP pulses, the reference value is changed up or down depending on the desired direction of movement. On the first slope (of P1 or P2), the reference value is changed in increments of 8 DAC steps. When the limit of the first slope (HI or LO) is reached, the microprocessor looks at the next slope (P1 or P2) and begins to change the reference value in steps of 16. See Section 1.3.9 for an explanation of P1 and P2 signals. Each slope represents a track and, with each track crossed, the change in the reference value increases until the actuator reaches the halfway point. The microprocessor uses the reverse process to decelerate the actuator until it finally reaches the destination track.

Slew Mode Seeking

The slew mode of seeking is used for buffered seeks of 18 or more tracks. During the slew mode, the actuator is accelerated to a terminal velocity. This is controlled for the first half of the seek. During the second half of the seek, the actuator is decelerated to a velocity determined by the number of TRACKS TO GO.

If the seek length is an even number of tracks, the current position signal being servoed on will be the position signal used at the destination track. This will be the same phase or plus two phases.

If the seek length is an odd number of tracks, position signals switch and the first crossing of a switch point will decrease the number of TRACKS TO GO. This results in an even number of TRACKS TO GO. The position signal that was switched to becomes the destination position signal. Center crossings of this position signal are counted, decreasing the TRACKS TO GO by twos as with an even track seek.

Upon entering a slew mode seek, the terminal velocity is determined from a table. The number of analog-to-digital conversions between center crossings of the position signal provides the velocity feedback. To maintain this velocity, the full acceleration value is output to the actuator (00H or FFH, depending on direction) until the velocity is greater than desired. At that time, a coast value is issued to the actuator (which also depends on direction). Terminal velocity is maintained for half of the way to the destination track. At that time the full deceleration value is issued. While monitoring the time between center crossings (velocity) and the number of TRACKS TO GO, the seek profile table is followed down to the destination track, slowing down the actuator.

Prior to the beginning of any seek, the internal timer counter has been "primed" with the counter set at "1" and the timer interrupt enabled. With the receipt of the first step pulse the counter is decremented to zero, generating an interrupt.

Upon receipt of the first STEP pulse, the microprocessor saves the current prediction and other values. This is a buffered seek mode. Preparing to seek, the microprocessor rechecks the counter for any more STEP pulses. If more STEP pulses have been received, it will continue through a loop of approximately 200 μs, rechecking the last and current counter values until all STEP pulses are received. If, after the first STEP pulse, no additional steps were seen, the microprocessor would proceed in the single step mode.

The single step mode means STEP pulses are received by the drive with more than 1.5 μs between STEP pulses. Buffered mode seeks are defined as 3 to 200 μs between STEP pulses. However, STEP pulses issued between 200 μs and 1.5 ms will be accepted.

When entering the seek mode, the microprocessor also tests the condition of the microstep line. Microstep is used only for servo writing.

Buffered seeks of 17 or fewer tracks are handled as single steps in a ramped mode. An 18-track seek will take less time than a 17-track seek, therefore, because buffered seeks greater than 17 tracks are in the slew mode.

Actuator Drive Circuits

Figure 1-18 shows a block diagram of the actuator drive circuits. The microprocessor enables power to the amplifiers at power-up via the enable driver. Additionally, the microprocessor generates a series of 8 digital line-signals that correspond to specific currents to the actuator, as shown in Table 1-4.

TABLE 1-4
D/A Actuator Signals

DIGITAL	HEXIDECIMAL	CURRENT
11111111	(FF)	Full Outward Current
10000000	(80)	Zero Current (Coast)
00000000	(00)	Full Inward Current

A digital-to-analog converter (DAC) transforms the eight digital lines to a current that an op amp converts to voltage (TP 7). The voltage goes into a lead-lag compensator to stabilize the loop. Finally, the compensator output passes through voltage to current amplifiers that send current to the actuator.

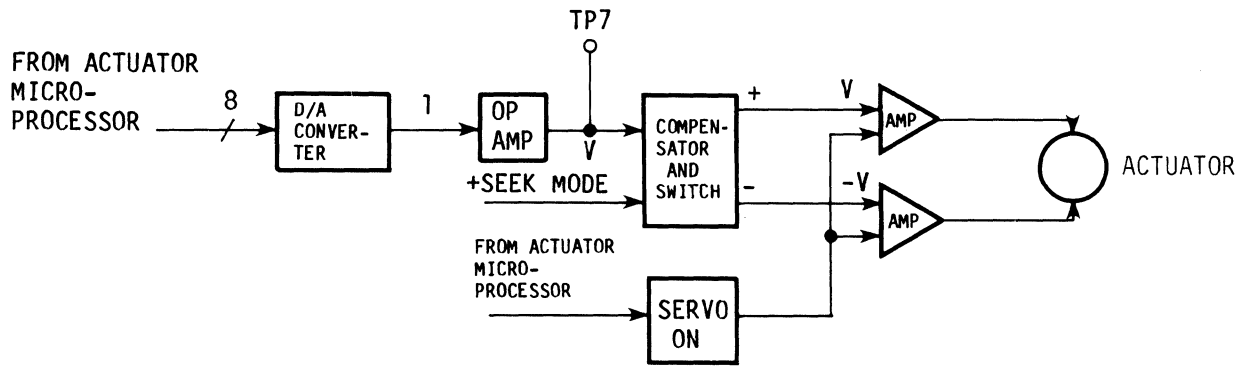

FIGURE 1-18
Actuator Drive Block Diagram

- Actuator Current

The actuator microprocessor U7 sends an 8-bit word to the actuator DAC U8 to select the actuator current as one of 256 values. The range of values is 128 steps of positive current for outward movement of the actuator (towards Track 0), and 128 steps of negative current for inward movement of the actuator (towards Track 511).

The actuator microprocessor controls the actuator current in two modes: seeking and servoing. The first mode in which the actuator microprocessor controls the actuator current is the seeking mode. Seeking can be further divided into two modes: slew mode and ramped mode. During slew mode, the current to the actuator is one of three values depending on the direction and acceleration/deceleration of the actuator. See Table 1-4.

During ramped mode seeking, the actuator current is incremented or decremented in eight DAC step increments to control velocity.

The second mode in which the actuator microprocessor controls the actuator current is the servoing mode. During servoing, the output current to the actuator is determined by the following expression (all values are in hex).

DACOUT = (REF − POS) + NOPOWER

where DACOUT is the 8-bit word to the DAC, U8; REF is the desired position signal value; POS is the measured position signal value; and NOPOWER is the DAC value that would result in no movement of the actuator (close to zero current).

- Actuator Drive Circuit

Figure 1-19 shows a schematic of the actuator drive circuit. R58 (4.02K) and the two resistors of RN9 (3.3K each) add up to 10.62K. This determines the full scale reference current Iref as well as reference voltages VR1 and VR2.

$$Iref = \frac{+10VB}{4.02k + 6.6k} = \frac{+10VB}{10.62k} = .94 \text{ mA full scale}$$

$$\text{Therefore, output current per step} = \frac{.94 \text{ mA}}{256} = 3.67\ \mu\text{A per DAC step.}$$

The output of the DAC is converted to a voltage by U21-A, LM324. The input to pin 3, VR1, is determined by R58 and the two 3.3K resistors of RN9.

$$VR_1 = \left(\frac{3.3k}{6.6K + 4.02k}\right) 10_{VB} = \left(\frac{3.3k}{10.62k}\right) 10_{VB} = 3.1V$$

The voltage at TP7 is determined by the gain resistors of RN9 which add up to 6.6K. The output voltage is:

TP7 voltage = 6.6K (I) + VR_1

Therefore minimum output is:

VR1 + 6.6K (0) = 3.1 + 0 = 3.1V

Full scale output is:

VR1 + 6.6K (.94 mA) = 3.1 + 6.2 = 9.3V

Output change per DAC step is 24.22 mV. Therefore, the range of the output voltage is 3.1V to 9.3V.

Capacitor C41, 6800PF in conjunction with the resistors in RN9 (6.6K) stabilize the output for high frequencies, as well as control the bandwidth of the driver stage.

U21-B is an inverting gain stage with compensation network formed by C42, .015 μF, and RN6, 6.8K. The compensation is needed to stabilize the transfer function during position control. The FET device, Q14, is used to disable this network during slew mode seeking.

The reference voltage for U21-B, C and U23, U24 is used to determine the output range of these stages. This reference, VR2 is:

$$VR_2 = \frac{6.6k}{10.62k} 10_{VB} = 6.2V$$

U21-C is another inverting unity gain stage to provide complementary drive, along with U21-B to the output drivers U23 and U24.

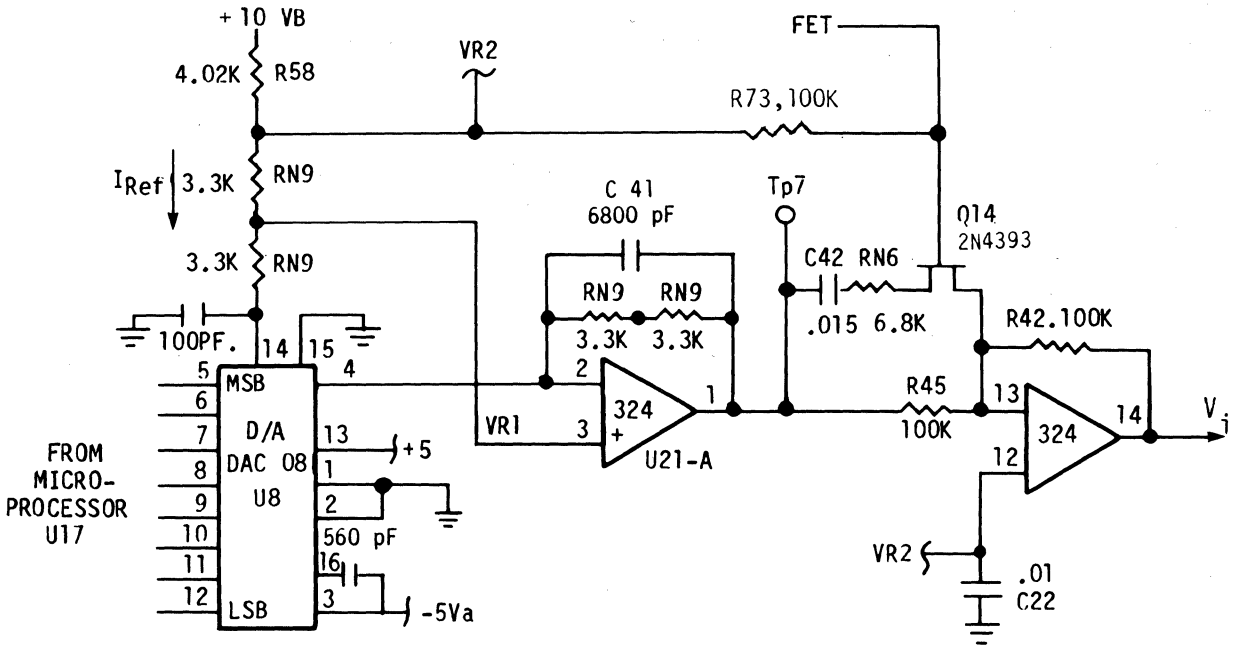

FIGURE 1-19
Actuator Drive Circuit

- **Actuator Drivers**

Figure 1-20 illustrates the actuator driver circuits. The actuator drivers receive input V_i from the previous compensation stage (U21-B). The voltage converts to current I_o according to $I_o = .32\ V_i$. VR2 = +6.2V which goes to the + input of the TDA 2030 power op amps.

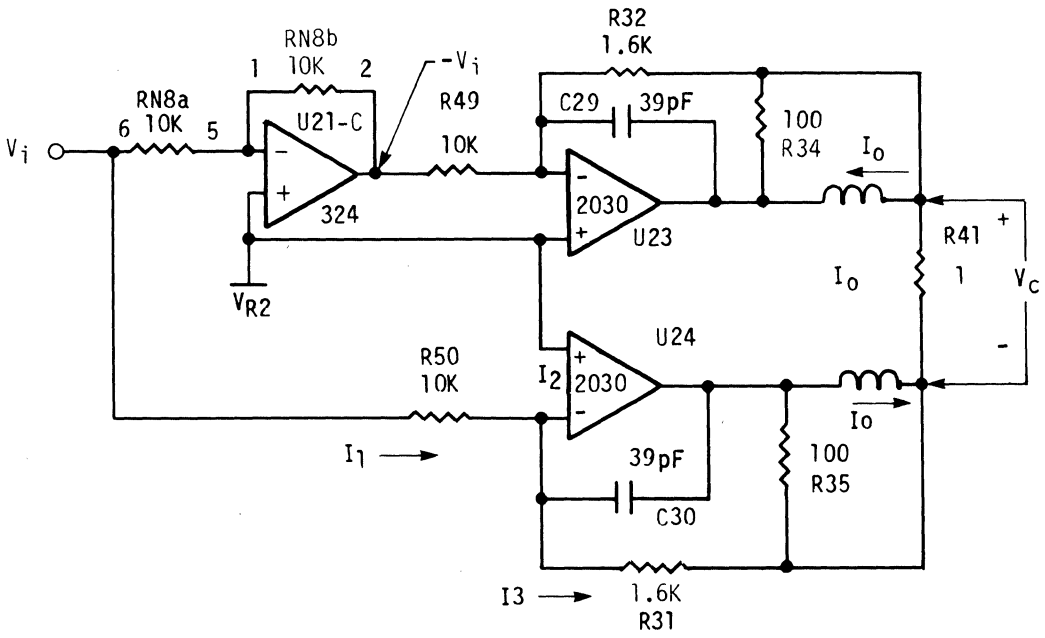

FIGURE 1-20
Actuator Driver Stage

The following summarizes the voltage and current relationships in this circuit:

$$I_2 = 0, \text{ therefore } I_1 = I_3$$

$$I_1 = \frac{V_i - 6.2V}{R50} = I_3 = \frac{6.2V - V_0}{R31}$$

Since R50 $\approx$ 6(R31), then $V_0 = .16(1V - V_i) + 6.2V \approx 6.4 - .16V_i$

A similar analysis shows that the voltage at the other side of R41 is $V_0 = 6.4V + .16V_i$.

Therefore,

$$I_0 = \frac{(6.4 - 16V_i) - (6.4V + .16V_i)}{RF1} = \frac{-.32V_i}{1\Omega} = -.32V_iA$$

In summary, for any voltage V_i, a current of $.32V_i$ A runs through the actuator coils to generate a torque. For example,

$V_i = 1V$

$I_0 = .32$ amp (produces an outward torque)

In summary, $V_i > VR2 = 6.2$ V produces an outward motion (toward Track 0) and $V_i < VR2 = 6.2$ V produces an inward motion (toward TK511).

Resistors R34 and R35 swamp out the effects of the inductance of the rotor coils. Capacitors C29 and C30 suppress high frequency oscillations.

Servo Read and Conversion Circuits

Figure 1-21 illustrates the servo peak detector circuit. The servo peak detector takes a 2.17 MHz sine wave input and finds the greatest positive voltage. The peak voltage is amplified and held in capacitor C12. The peak detector is reset by U19 (7406) which receives its input from the actuator microprocessor and discharges C12.

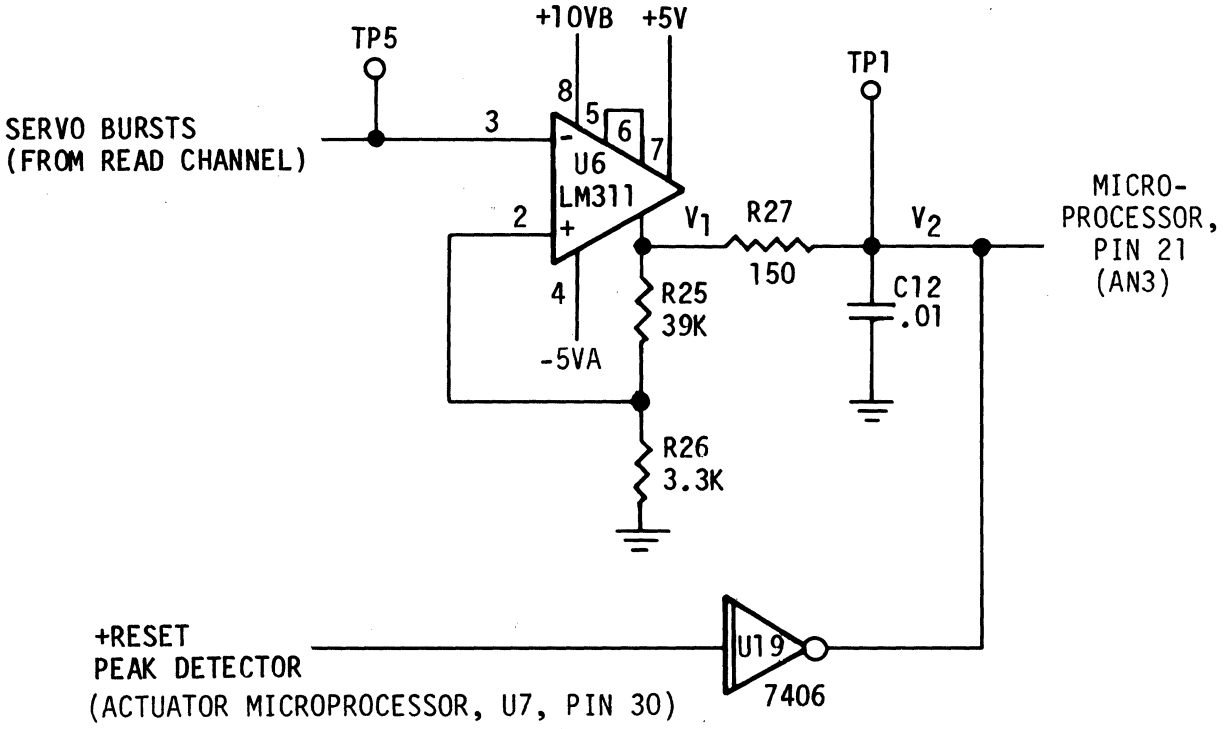

FIGURE 1-21
Servo Peak Detector

Figure 1-22 illustrates the servo peak detector waveforms.

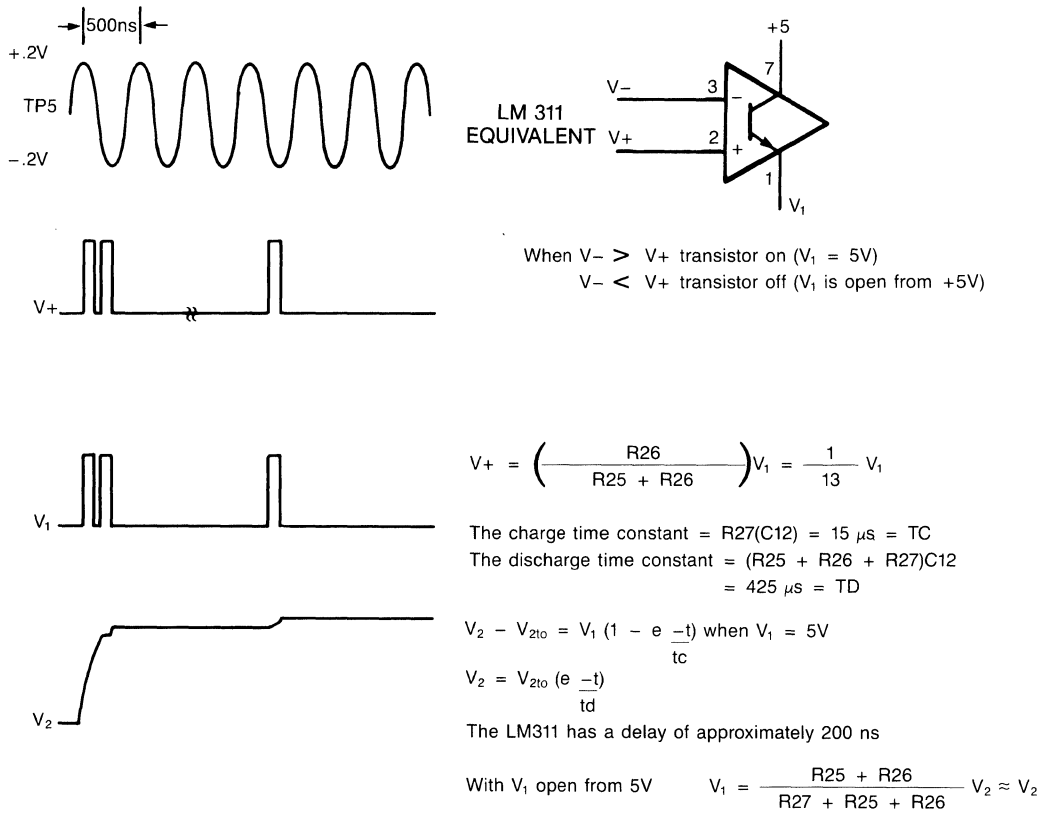

FIGURE 1-22
Servo Peak Detector Signals

1.3.12 HEAD SWITCHING MATRIX

Figure 1-23 is a simplified schematic of the head switching diode matrix for two heads.

Diodes CR9-CR12 are part of the head switching matrix. When the head switch IC grounds the head center tap (HDCT 0-7), the selected head is connected to the Read/Write circuits via one of the diode pairs. None of the other diode pairs is forward biased — this isolates the other heads from the selected head. Diodes CR1-CR4 are part of the Read/Write circuits and are used to isolate the Read and Write circuits from each other.

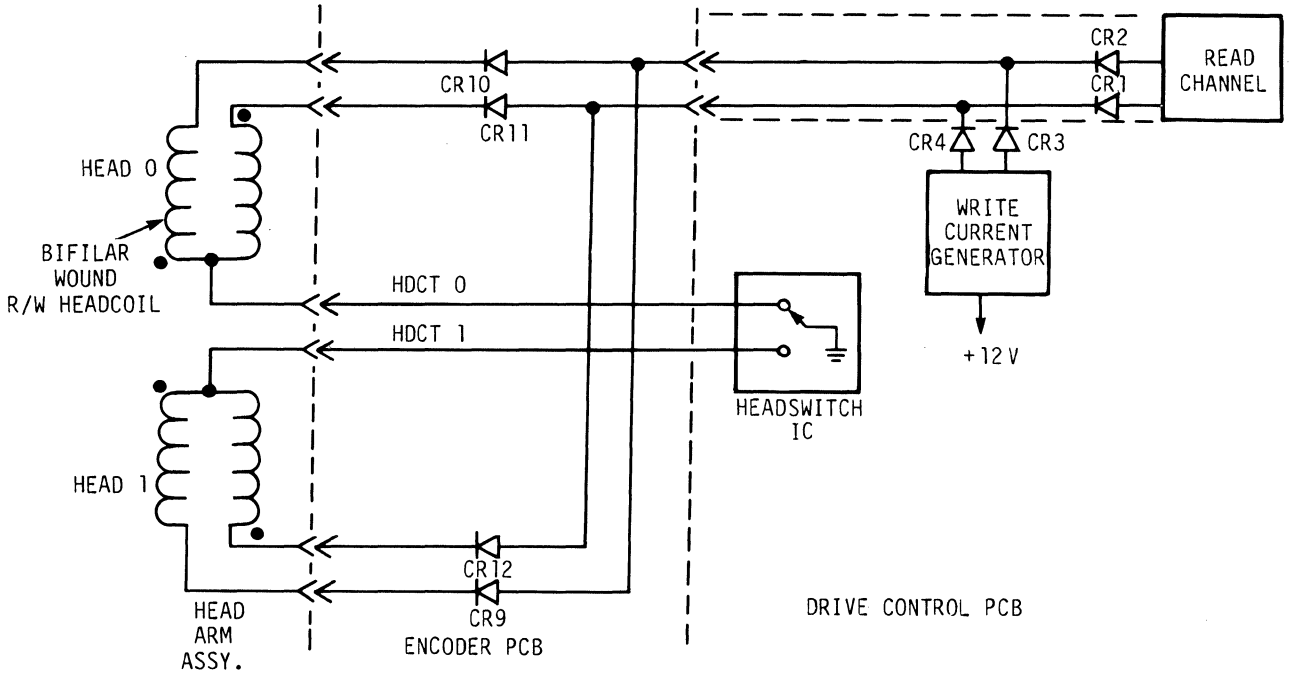

FIGURE 1-23
Head Switching Matrix

1.3.13 WRITE DATA CIRCUITS

Figure 1-24 is a functional block diagram of the write circuits found in the Q500. The write enable circuit ensures that:

1. The 5V logic voltage is present.

2. The drive is selected, SEEK COMPLETE is true, and it is not wedge time (to prevent writing in the servo area). See Figure 1-28 for the wedge timing diagram.

3. The WRITE GATE is active.

When these conditions are met, the write enable switch turns on the write current source.

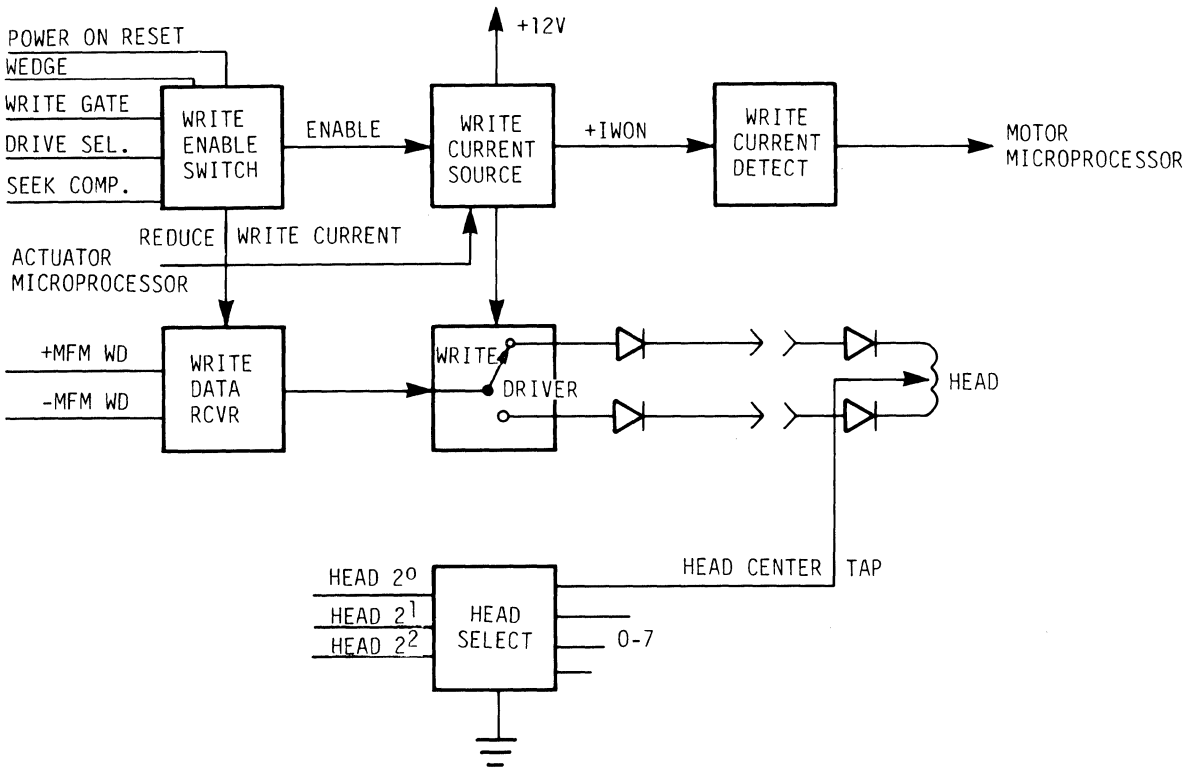

FIGURE 1-24
Write Circuit Block Diagram

When enabled, the write current source provides the write driver with 18 mA of write current. The circuit also provides a current-on signal that is used by the motor microprocessor to determine Write Fault. The write driver receives its switching input from the write data receiver. The write driver switches the write current into either end of the head coil whose center tap has been grounded by the head select switch. Refer to Figure 1-25 for a schematic illustration of the write data circuit.

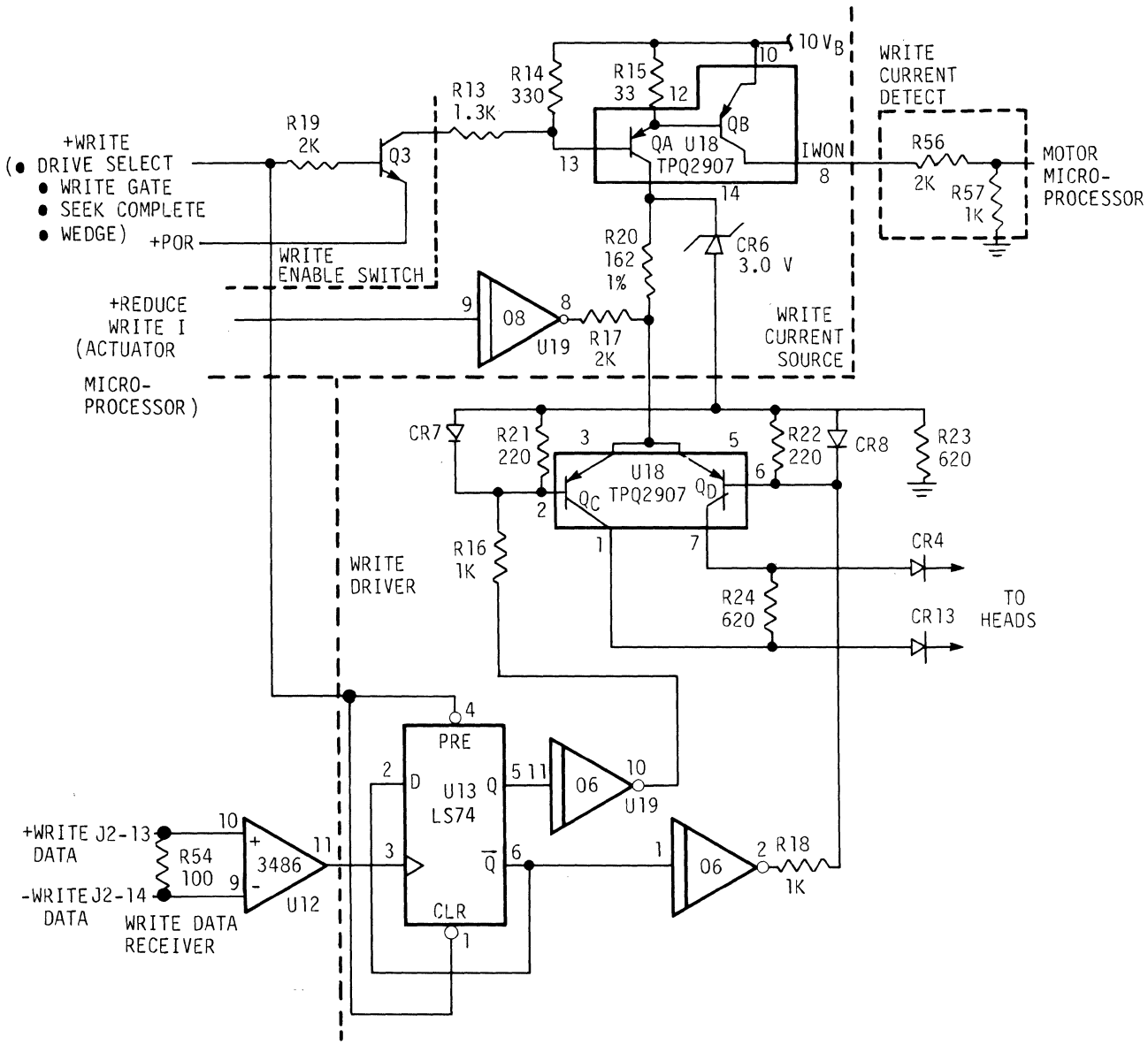

FIGURE 1-25
Write Data Circuit

Assuming that +POR is inactive and +WRITE = (DRIVE SELECT) (WRITE GATE) (SEEK COMPLETE) = HI, then Q_3 (in Figure 1-25) is turned on, providing base current to Q_A, which supplies the write current.

Q_B is turned on when Q_A is on, so current flows through the voltage divider R56/R57, creating a voltage which is detected by the motor microprocessor indicating active write current.

Write current is set by Zener diode CR6 and resistor R20 and is given by the equation:

$$\text{Iwrite} = \frac{V_C\,(Q_A) - V_E\,(Q_{C,D})}{R20}$$

$$= \frac{V_E\,(Q_{C,D}) - V_{BE}\,(Q_{C,D}) + V_{CR8} + V_{CR6} - V_E\,(Q_{C,D})}{R20}$$

$$= \frac{V_{CR6}}{R20} \qquad (\text{since } V_{BE}\,(Q_{C,D}) = V_{CR8})$$

$$= \frac{3\text{ V}}{162\Omega} \qquad 18\text{ mA}$$

Current direction in the head is switched by Q_C and Q_D. Write data enters a line receiver at the data interface whose output toggels an LS74 flip-flop, U13. The Q and $\overline{Q}$ outputs of the flip-flop are buffered and turned on either Q_C or Q_D. A write data pulse causes a switch in current direction through the head whose center tap has been grounded.

Write current is reduced automatically. At Cylinder 256, the actuator microprocessor sets the REDUCE WRITE I signal high; this grounds one end of R17 through inverting buffer U19. The other end of R17 is attached to the emitters of Q_C and Q_D. The Current sunk through R_{17} reduces the write current to the heads by approximately 20%.

1.3.14 READ DATA CIRCUITS

The block diagram in Figure 1-26 illustrates the functional elements of the Q500 read channel. When the head select switch connects the center tap of the selected head to ground, the diodes in the head coupling network become forward biased. Magnetic flux changes passing by the head induce current into the coil. This current is coupled through the head coupling diodes and appears as small differential voltage changes at the input of the amplifier. The amplifier boosts these changes that then travel through a low pass filter to eliminate unwanted high frequency noise. The signal is input to the differentiator, which converts the voltage peaks of the signal to zero voltage crossings. These zero voltage crossings represent the flux changes read from the disk. The differentiated signal passes through further low-pass filtering before being input to the zero crossing detector, where READ DATA pulses are created from the zero crossings. These READ DATA pulses are input to a line driver with differential output. The output of the line driver is the ± MFM READ DATA sent to the controller via the 20-conductor data cable.

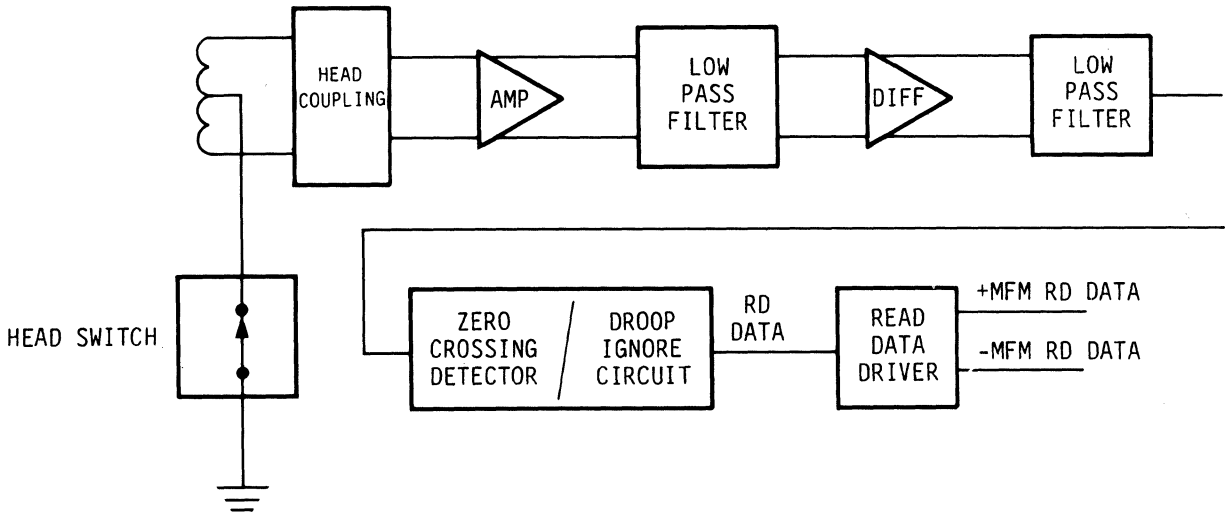

FIGURE 1-26
Read Channel Block Diagram

Figure 1-27 shows the front end of the read channel.

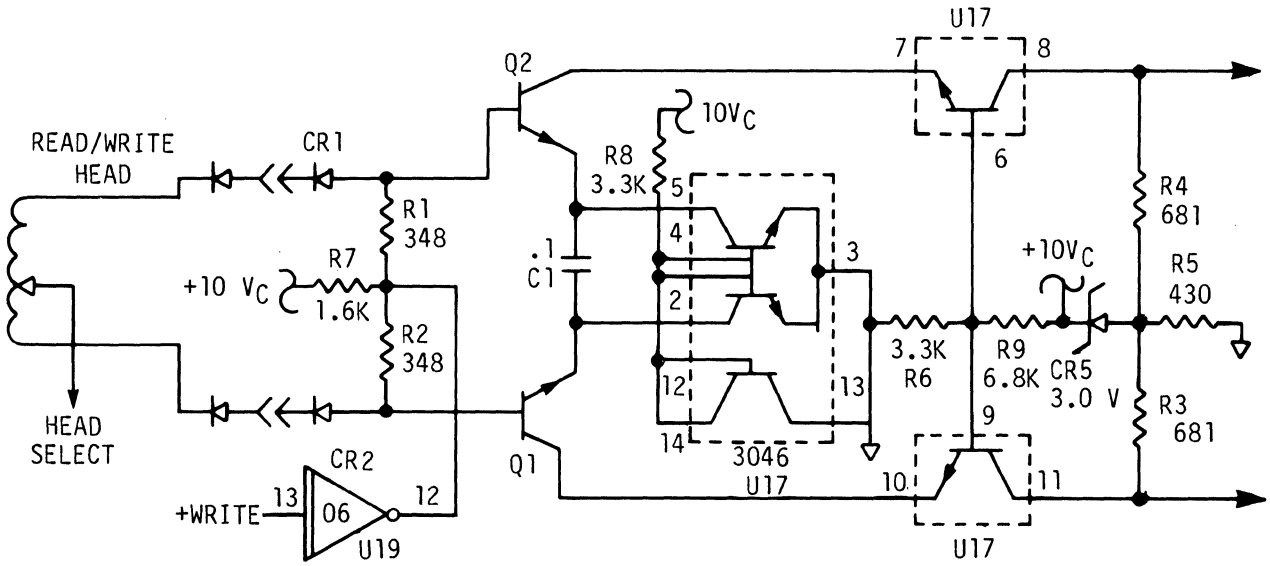

FIGURE 1-27
Read Channel Front End

When +WRITE goes HI, CR1 and CR2 become reversed bias, as U19 Pin 12 goes LO, thus preventing the write signal from entering the read channel. When +WRITE is LO, the READ signal flows differentially to Q_1 and Q_2. The three transistors of U17 provide current sources which bias Q_1 and Q_2 on. Refer to Figure 1-28.

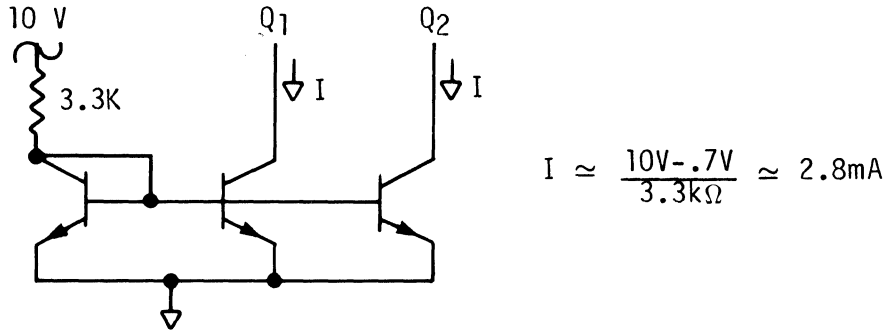

FIGURE 1-28
U17 Current Source

The remaining two transistors of U17 each couple with Q_1 or Q_2 to constitute a cascode amplifier, shown in a simplified version in Figure 1-29.

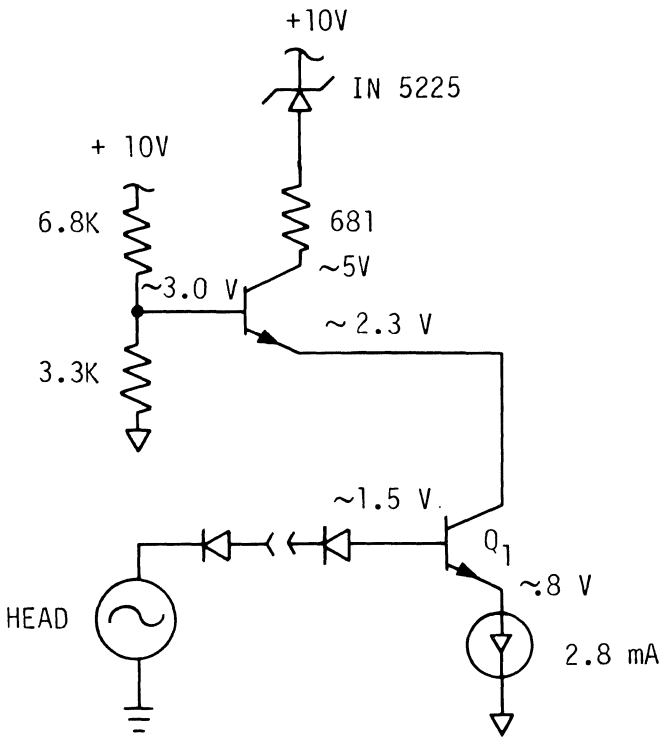

FIGURE 1-29
Cascode Amplifier

The cascode amplifier provides small-signal current gain = $h_{fe}(Q_1)$, or approximately 100.

Low Pass Filter/Differentiator

After being amplified, the READ signal is passed through low pass filtering before entering a differential amplifier where peaks (from flux transitions inducing head current) are converted to zero-crossings.

A 592 Differential Amplifier is used to perform the differentiation and provide voltage gain of 400. The output of the differentiator passes through two capacitors (C9 and C10) which remove the dc component from the signal. After further low pass filtering, the signal proceeds to the zero-crossing detector circuit. Figure 1-30 shows the low pass/differentiator circuitry.

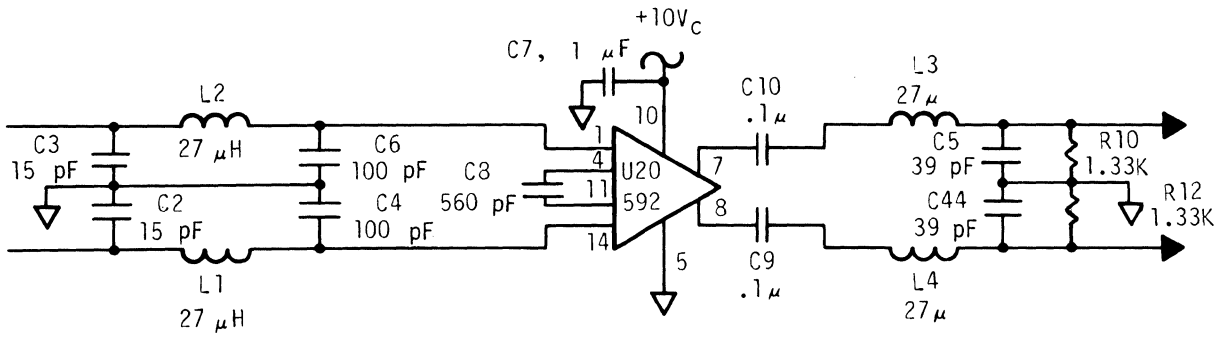

FIGURE 1-30
Low Pass Filter/Differentiator

Zero-Crossing Detector/Droop Ignore Circuit

Up to this point, the read channel has detected, amplified, and filtered the flux changes recorded on the disk and transformed the resultant voltage peaks through differentiation to zero-crossings for easy detection. The signal is now input to an 529/361 comparator which detects the zero-crossings and creates READ DATA pulses. Figure 1-31 shows the comparator and its simplified internal circuit.

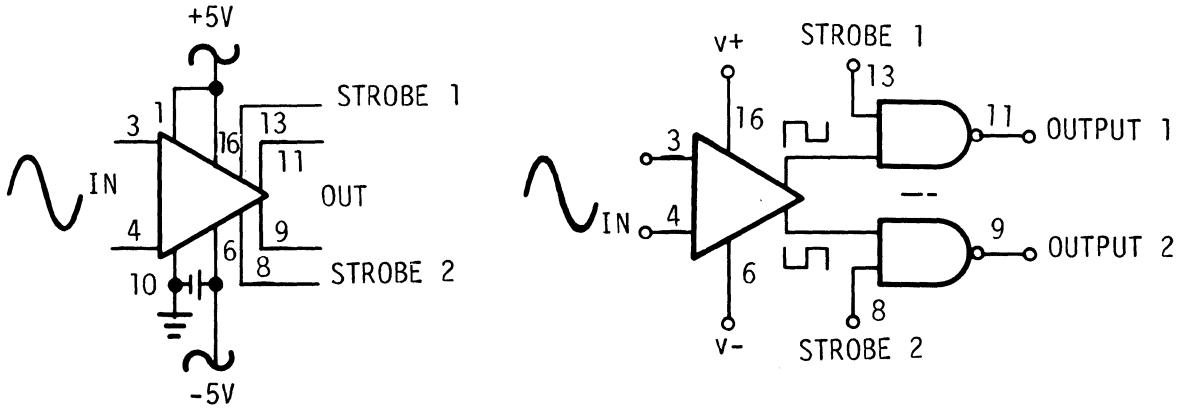

FIGURE 1-31
Comparator and Equivalent Internal Circuit

The end of the READ channel is shown in Figure 1-34, using the representation of the 529 comparator shown in Figure 1-31.

Placing the E7 jumper across BC, or at AB when point A is a logic zero, results in a simplified circuit output shown in Figure 1-32.

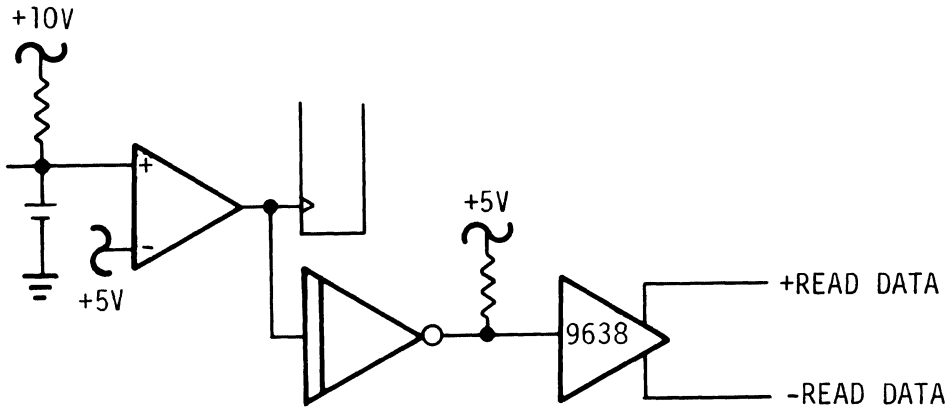

FIGURE 1-32
Simplified Circuit Output

Data Pulse Generation

For differentiated IF signal input, consider the droop ignore circuit waveforms found in the circuit illustrated in Figure 1-33. Figure 1-34 shows the droop ignore circuit. As the outputs of the 529 (Pin 9 or 11) zero-crossing detector go LO, the output of the open-collector NAND gate (U10) is allowed to go HI at a rate set by the RC time constant of R53 and C33. As the rising edge heads towards +10V, it breaks the threshold set for comparator 3486 (U12), which toggles the flip-flop (U13). When this threshold is broken, the strobe inputs (Pins 8 and 13) of the 529 change, and the output returns to HI (Pin 9 or 11), thereby forcing the NAND gate output (U10 Pin 6) to ground. The READ DATA pulse width is determined by the length of time that the signal at U10 Pin 6 is greater than the V− threshold of U12 (typically about 50 ns) set at approximately 3.0V by R55 and R77.

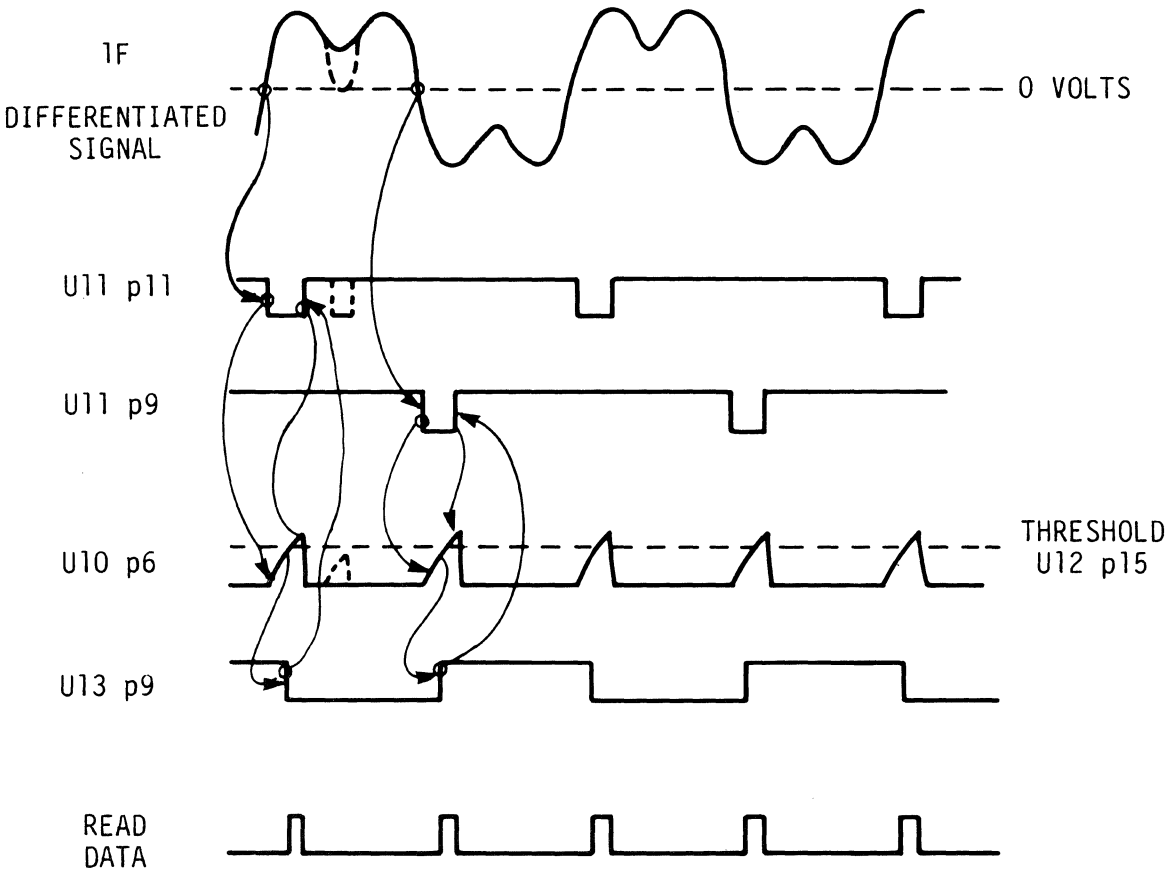

FIGURE 1-33
Droop Ignore Circuit Waveforms

Droop Ignore Circuit

The droop ignore circuit prevents the pulse train from generating false data pulses due to droop. Droop is the tendency of the differentiated signal to droop toward zero volts between flux transitions. Droop may occur while the drive reads low frequency data patterns from the disk and when noise or media imperfections cause the signal to cross zero between legitimate bits.

Figure 1-33 shows the signals generated for a differentiated IF signal. The droop is not crossing zero volts in this figure (which would be indicated by the signals shown inside the dotted lines). When the output of the zero-crossing detector changes to LO due to the droop, it causes the output of the NAND gate (U10) to rise. The RC time constant of R53 and C33 controls the time interval before the NAND gate signal crosses the threshold of U12, causing a READ DATA pulse. In the case of a droop zero-crossing, the output of the NAND gate does not have sufficient time to cross the threshold because the subsequent zero-crossing of the droop causes the output of the 529 to return to HI, forcing U10 Pin 6 back to ground before U12 detects a bit.

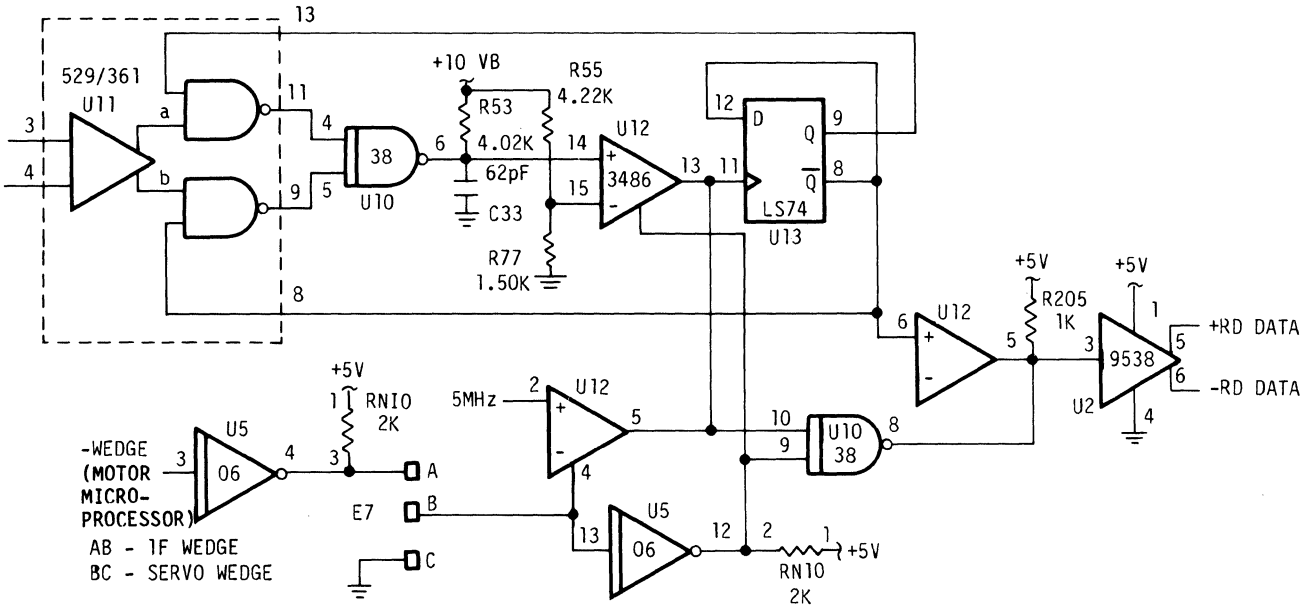

FIGURE 1-34
Zero-Crossing Detector/Droop Ignore Circuit

Options

When the user places the E7 jumper in the AB position, the motor microprocessor disables the 3486 comparator which normally clocks the flip-flop with the READ DATA pulses when wedge timing occurs. During wedge timing, two other 3486 comparators are enabled which apply a 5 MHz clock to the flip-flop. The $\overline{Q}$ output is sent to the READ DATA interface driver which puts a IF square wave on the READ DATA output lines.

If the user places the E7 jumper in the BC position, the signal read from the disk is output at all times.

1.3.15 MOTOR MICROPROCESSOR

The motor microprocessor performs three major funtions:

1. Motor-start and speed control
2. WEDGE/INDEX timing
3. Write Fault detection

Figure 1-35 is a block diagram showing the motor microprocessor functions. The microprocessor is an 8-bit microcomputer with 1 kilobyte of read-only memory (ROM), 64 bytes of RAM, 27 I/O lines, and an 8-bit timer.

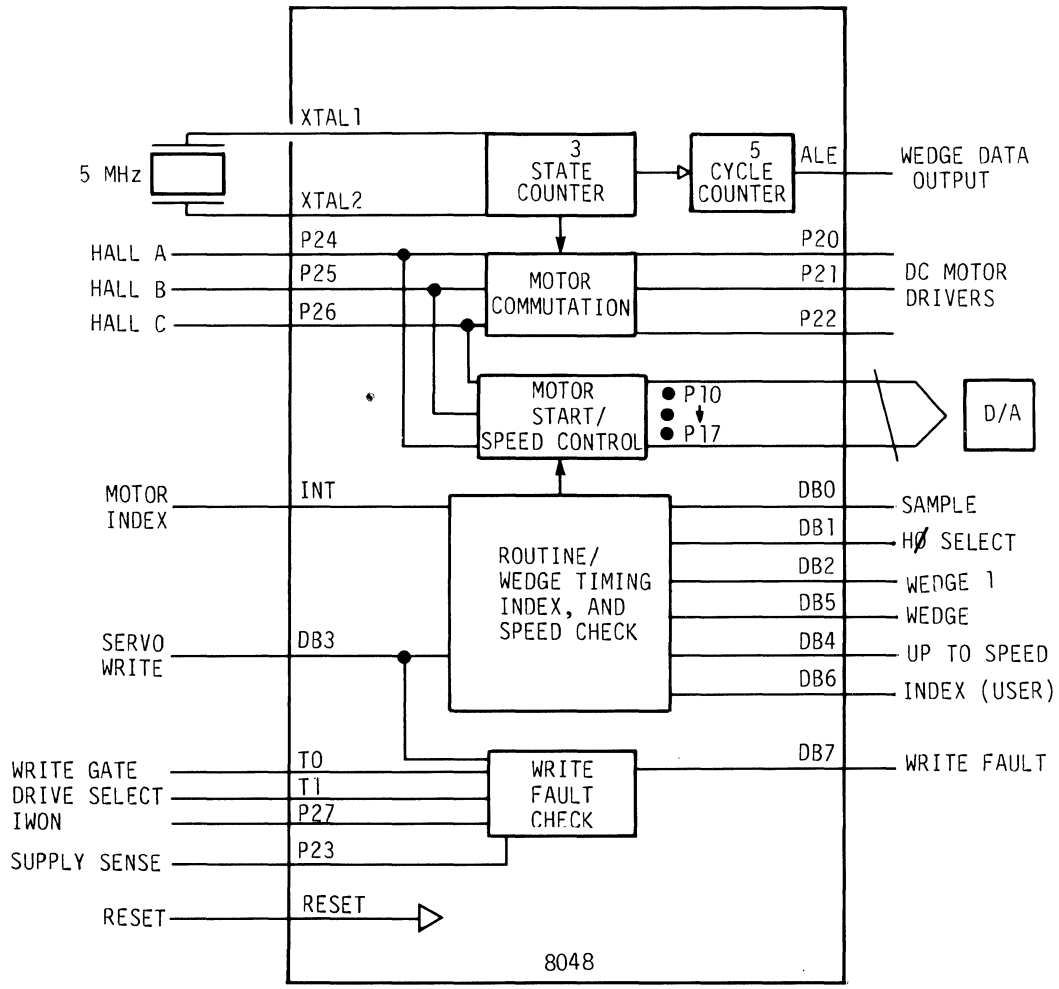

FIGURE 1-35
Motor Microprocessor Block Diagram

DC Motor Control

The motor subassembly provides information to the microprocessor about motor rotor position by means of three signals. As the motor rotates, the rotor magnets pass by Hall effect devices whose output is shaped by a 2901 comparator circuit (located on the PCB of the motor subassembly). The three position signals generated by the Hall effect devices are directly input to the microprocessor and are continually monitored. When the motor changes position (the input signals a change in state), the microprocessor changes the state of the three output signals accordingly to switch current through one of the three stator windings. Figure 1-36 illustrates the commutation timing for the sequence just described.

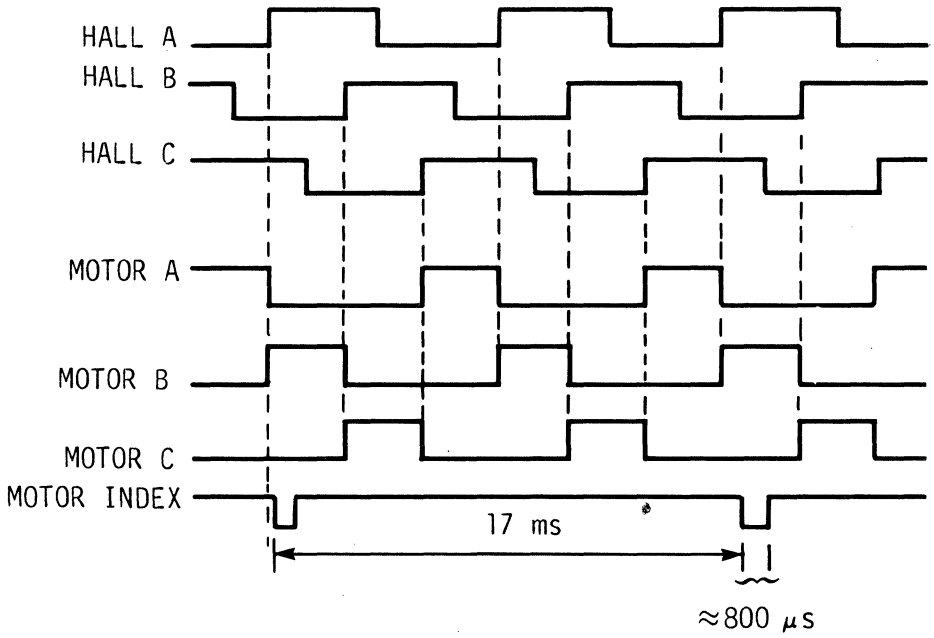

FIGURE 1-36
DC Motor Commutation Timing Diagram

Motor Current

The position-sensing subroutine controls the coil to which current is applied. The microprocessor determines the amount of current by sending an 8-bit word to a DAC; in this way, the microprocessor selects the motor current as one of 256 values.

The microprocessor controls the motor current in two modes: start-up and locked-on. (See page 1-67 for a discussion of the locked-on mode.) The first mode in which the microprocessor controls the motor current is the start-up mode. Start-up control is essentially open-loop. Once dc power has come up and the microprocessor has been initialized, it checks the Hall signals for motor movement. If no Hall change occurs, the motor is not moving and program execution jumps to the beginning of the motor-start routine. If a Hall change does occur, the microprocessor does a timing calculation to determine where to enter the motor-start program. The microprocessor checks for Hall changes to prevent over-accelerating a rotating motor.

Current is applied in decreasing steps during motor-start. A stationary motor begins at maximum current of 3.75A for one second. The microprocessor checks Hall states and monitors commutation. If no Hall change occurs, current is shut off for one second to allow the drivers to cool. The microprocessor repeats this sequence up to four times if the motor does not move. After the fifth try, the microprocessor aborts and lies idle, waiting for a power-on reset (POR).

Normally, after inital current is applied, this sequence follows:

3.5A for 2sec.
3.0A for 2sec.
2.5A for 40sec. (max)

While the above currents are applied, the microprocessor checks speed every tenth of a second in the commutation loop. When the speed is sufficient (36 Hall changes have occurred in 0.1 second), program execution transfers to the main loop. If, after 40 seconds, nominal speed is not attained, the microprocessor aborts and lies idle, waiting for a reset (POR).

The second mode in which the microprocessor controls the motor current is the locked-on mode. The locked-on mode occurs as program control transfers from the motor-start loop to the main loop; concurrently, the program control checks the states of the Hall signals and enters the main loop at the appropriate place. A two-byte register counts instruction cycles between index pulses to measure speed. When a Hall change occurs, the program performs commutation and jumps to the Write Fault subroutine (described on page 1-71).

Once per motor revolution, an index pulse causes an interrupt routine execution. At this time, the wedge-protect and index timing occur. The last part of the interrupt routine determines motor current.

The speed count registers are now checked. The INDEX period (motor speed) must be within or exceeding $\pm 3\%$ of nominal speed (17 ms) for more than two seconds for the UP-TO-SPEED line to register True or False. This line resets the actuator microprocessor (if False), causing READY to go False.

Next the microprocessor performs an algorithm using the speed count error to calculate the value for output to the DAC. This sets the motor current for the next revolution (2 amps, maximum). Control is returned to the main loop from the interrupt routine after the current value is output and speed count registers are reset.

DC Motor Drive Circuit

Figure 1-37 shows a schematic of the drive circuit. R66 and CR16 provide a reference voltage of 0.8V across R65, which gives the DAC its reference current of 0.6 mA. R68 creates an output voltage which is input to an op-amp (U21). When the DAC input from the microprocessor is 00 (hex), no current flows into Pin 4, so the output voltage (U21) is 0.8V. With FF (hex) at the DAC input, full scale current flows through R68; this sets the U21 input at 0V. The op-amp maintains the DAC voltage across R33; thus, the microprocessor can set the motor current from 0 to 4 amps in 256 steps.

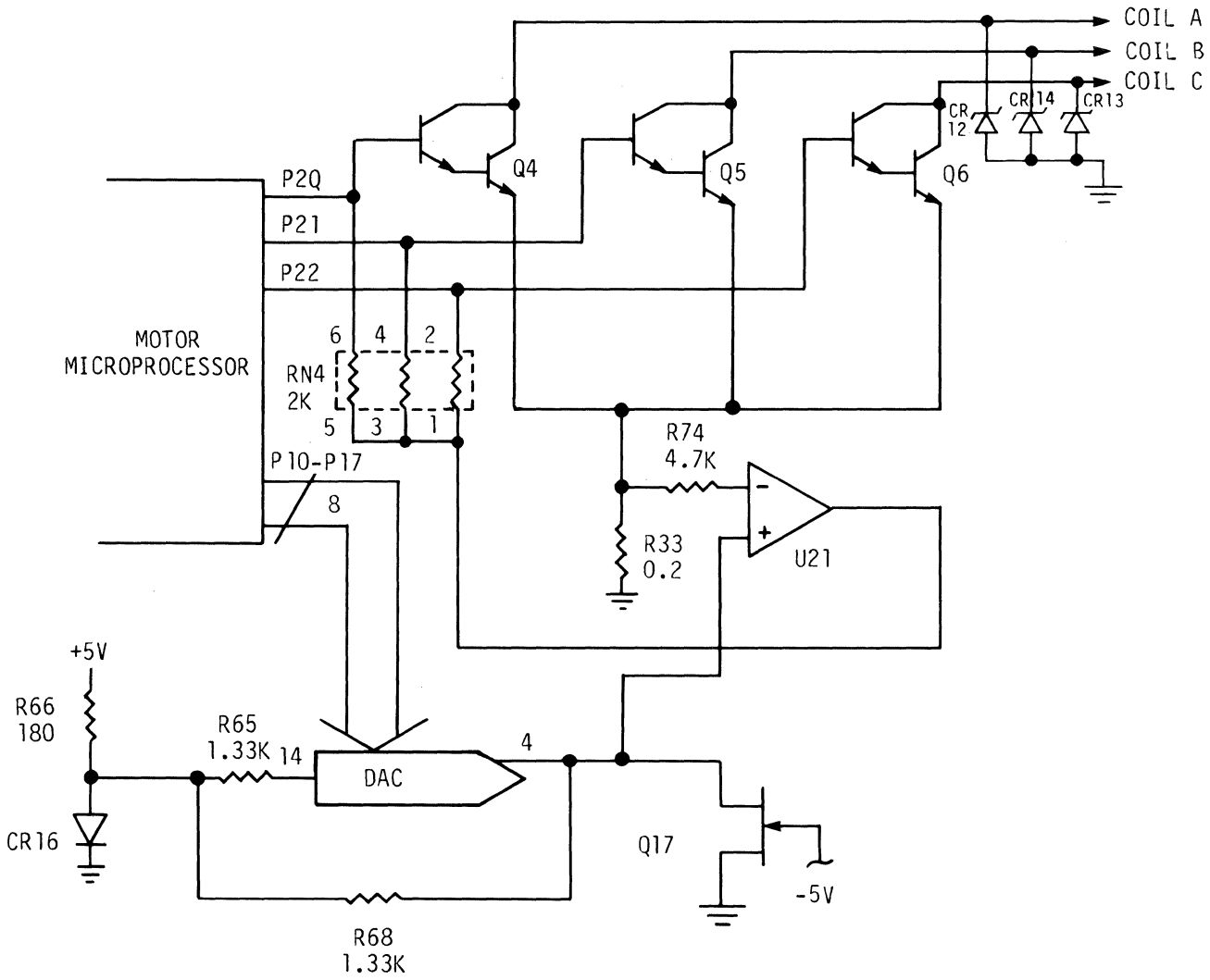

FIGURE 1-37
Motor Drive Circuit (Simplified)

FET Q17 clamps the DAC output to ground while the dc power supplies are rising. Signals at P20, 21 and 22 from the microprocessor are the commutation switches which send base current to one of the three Darlington transistors; these transistors sink current through their respective motor winding. Diodes CR12, 13, and 14 limit the turn-on transient to remain below the breakdown of the Q_4-Q_6 transistors.

WEDGE and INDEX Signals

The motor microprocessor software generates wedge timing. Beginning with a motor INDEX pulse (causing execution of the interrupt routine), the microprocessor generates three signals (WEDGE, WEDGE1, H0 SELECT) to disable the write drivers and the head select IC (U16), and to select the center tap of the servo head. (See Figure 1-38.) Another signal output by the microprocessor, SAMPLE, causes the actuator microprocessor to begin reading servo data. WEDGE 1 and H0 SELECT go inactive, which re-enables head select control to the interface. After a 30 μs delay to allow for head switch settling, USER INDEX is output to the interface. The E5 (servo-write) jumper disables the wedge-protect signals during power-up initialization of the microprocessor.

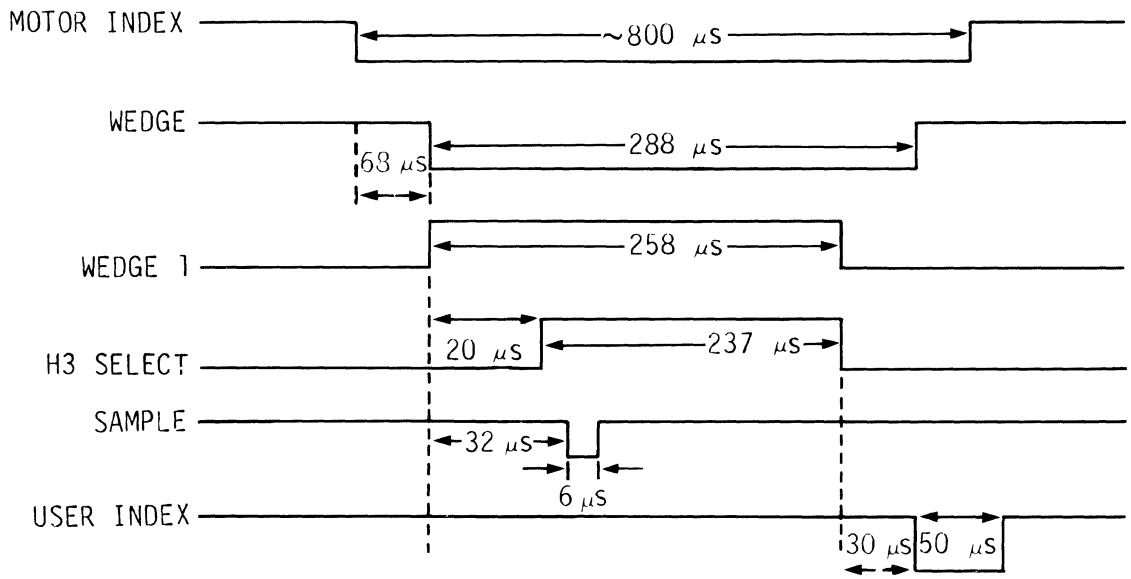

FIGURE 1-38
Wedge and Index Timing

Write Fault

After each motor commutation in the main loop, the microprocessor performs a Write Fault check (6 times per revolution). At the beginning of the Write Fault subroutine, a flag is cleared which becomes set if an interrupt (INDEX) occurs. This flag is checked at the end of the subroutine if a Write Fault was determined. If the flag was set, the Write Fault is considered invalid and is ignored; execution returns to the main loop.

To determine a Write Fault, the program first determines the states of −WRITE GATE and +IWON (Write Current On). Next, SUPPLY SENSE is checked for dc voltage levels (see Section 1.3.16, Power-On Reset and Power Sense). If the 5V is low or the 12V is low, SUPPLY SENSE is LO, causing a Write Fault. If −WRITE GATE had been determined HI, and +IWON LO, no fault occurs and the program returns to the main loop. With +IWON HI, the program rechecks −WRITE GATE, allowing for a single transition during the signal polling before issuing a Write Fault.

When −WRITE GATE is LO, the algorithms are more complex. Figure 1-39 shows a flow diagram of the sequence of events following a detection of −WRITE GATE LO.

After any Write Fault is issued, the wedge-protect logic is output continuously until the user resets the −WRITE FAULT line by deselecting the drive.

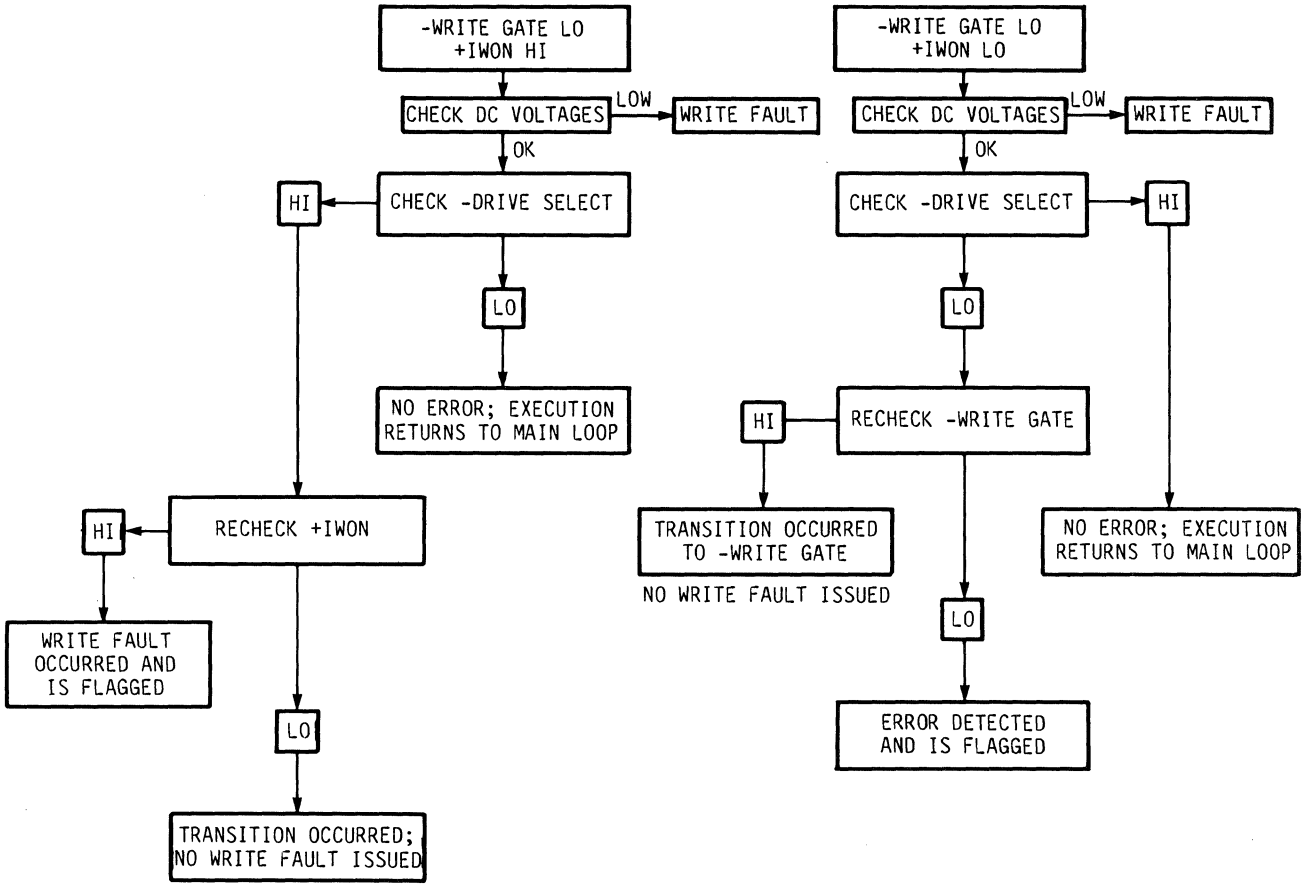

FIGURE 1-39
Write Fault Determination

1.3.16 POWER-ON RESET AND POWER SENSE

Figure 1-40 illustrates the power-on reset (POR) circuit.

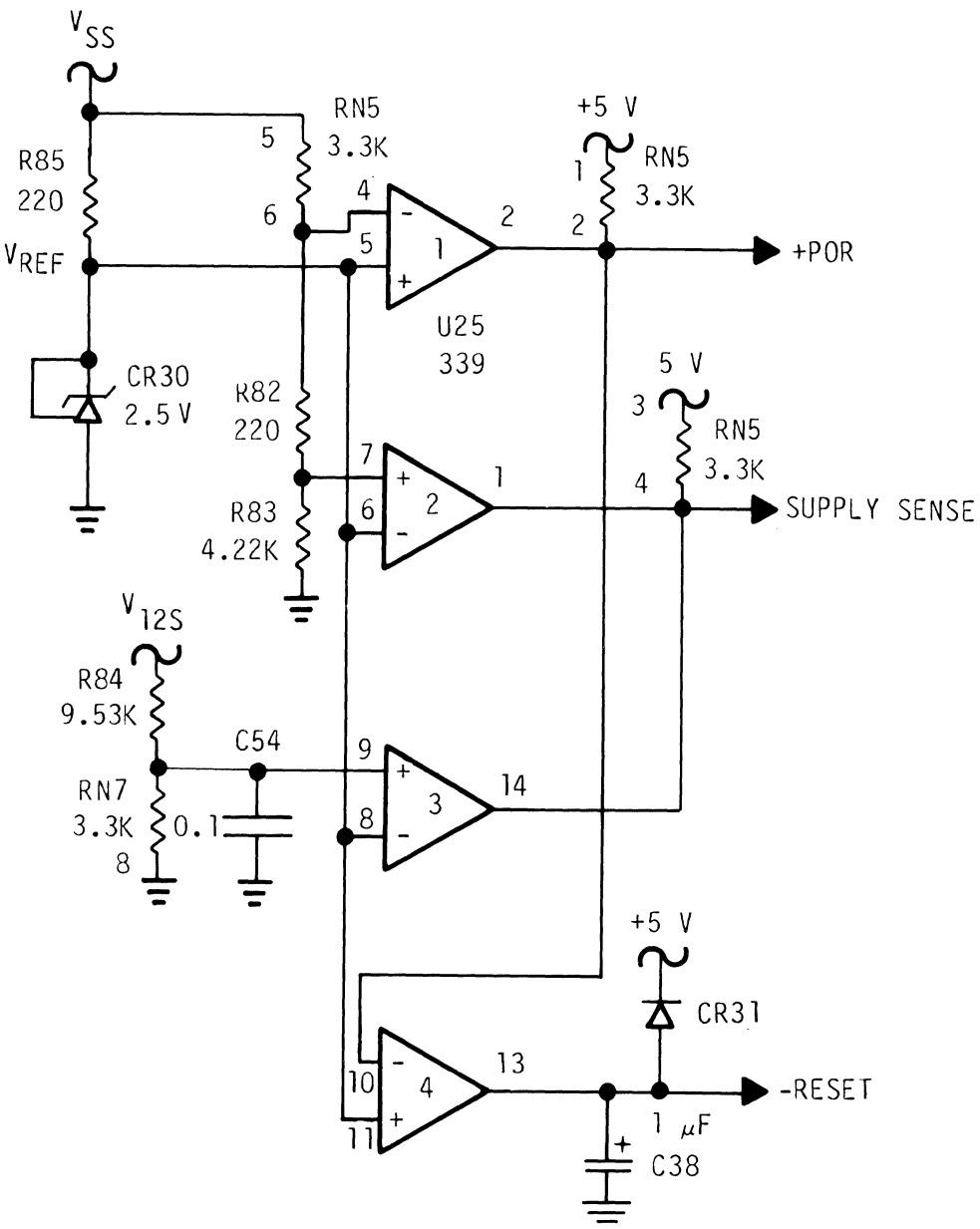

FIGURE 1-40
Power-On Reset Circuit

The comparator generates the +POR signal by comparing the 5V supply line V_{SS} to the reference voltage of CR30, 2.5V. Therefore:

$$V- \text{ @ Comp 1} = \frac{4.42}{7.72} (V_{SS}) \sim .57 (V_{SS})$$

As the supply voltage rises, $V_{REF} = V_{SS}$. Since, at comparator 1, $V- = 0.57 \times V_{SS}$ amd $V+ = V_{REF}$, the output of the comparator is HI until:

$$V_{SS} > \frac{2.5}{.57} V = 4.39V$$

When the supply reaches 4.39V, +POR becomes LO, which causes the output of comparator 4, -Reset, to become HI, delayed by capacitor C38.

The supply sense output is a wired AND condition of the outputs of comparators 2 and 3. Comparator 2 senses the 5V supply at the V+ input, with the 2.5V reference on the V− input. In this case, V+ is $4.2/7.72 \times V_{SS}$ supply or $.544 \times V_{SS}$ and switches HI when it exceeds 2.5V or when:

$$V_{SS} > \frac{2.5}{.544} V \sim 4.6V \qquad \text{(proving a tighter threshold for +POR)}$$

Comparator 3 senses the 12V supply against the reference 2.5V where:

$$V_+ = \frac{3.3}{12.83} \times V_{12} = .257 \times V_{12S}$$

Therefore, when

$$V_{12S} > \frac{2.5}{.257} V = 9.72V$$

the comparator 3 output switches to HI.

When both Comparators 2 and 3 have switched to HI, the output signal supply sense also switches to HI. Once HI, SUPPLY SENSE will switch to LO if the 5V supply dips to 4.6V (8% low) or if the 12V supply dips to 9.72V (19% low).

1.3.17 DC POWER, FILTER, AND REGULATORS

Refer to Figure 2-1 for locations of the dc power, filter, and regulators.

DC power is applied at connector P3. The two required dc voltages are +12V and +5V (see Table 1-3 on page 1-19 for specifications). Refer to Figure 1-10 for the start-up current profile from the 12V supply.

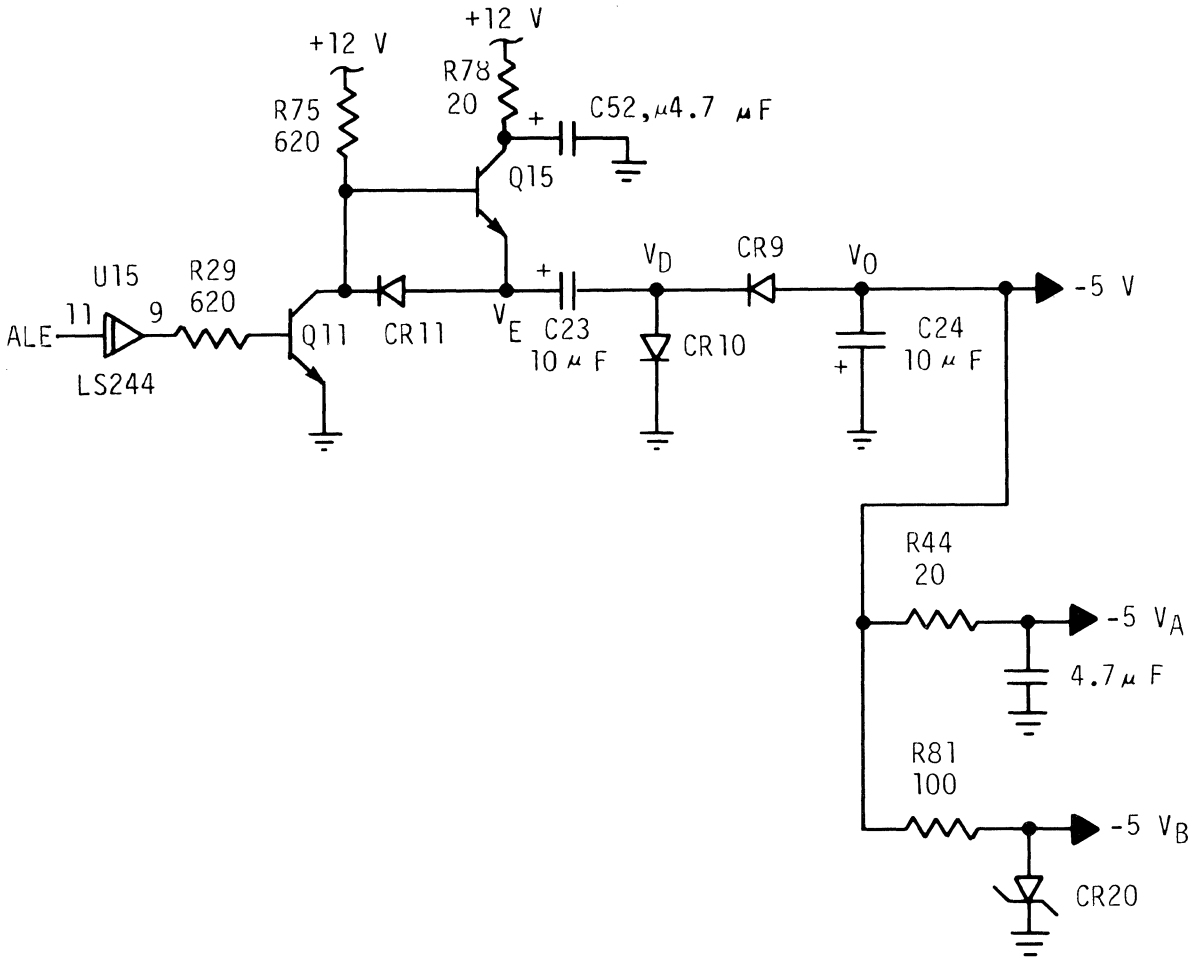

FIGURE 1-41
-5V Converter Circuit Schematic

DC Power Filter

Both 12V and 5V supplies are filtered through inductive beads and capacitors which form decoupling networks. 12V enters P3 at Pin 1 through L7 plus C25 and C27 decoupling capacitors. 5V enters P3 at Pin 4 through L8 with C32 and C13 providing decoupling with more decoupling capacitors distributed throughout the PCB. The 12V return is Pin 2 and the 5V return is Pin 3 of P3. The two ground returns are tied together by connector P3 on the PCB.

5V and 10V Regulated Supplies

Two series Zener diodes, CR17 and 18, each with 5.1V nominal voltage, create 10.2V at the base of transistor Q10. The base-emitter junction lowers the voltage; the Q_{10} emitter becomes the +10VB supply. Inductor L5 filters off +10VC; both 10V supplies are used in the read and write circuits. 10VC is input to VR12, a +5V regulator, which outputs the 5V regulated supply used by op-amps on the encoder PCB and dc motor, and used as a reference voltage for the actuator microprocessor.

−5V Power Supply

The −5V supply is generated by switching a voltage on and off at the input of a ladder circuit comprised of two capacitors (C23 and C24) and two diodes (CR9 and CR10). See Figure 1-41.

The motor microprocessor provides the switching signal via the ALE line, Pin 11. This signal is derived from the 5 MHz crystal, which is divided by 15 to provide a clock of 333 kHz with 25% duty cycle.

The switching signal is buffered by a 74LS244 line drive (U15, Pin 9) which provides base current to transistor Q11, switching it on and off. When the ALE signal is HI, Q11 is switched on to saturation and Q15 is off, since its base voltage is pulled down by Q11. The voltage at the emitter of Q_{15} (V_E) is about 1V, equal to the diode drop of CR11 plus the saturation voltage of Q11. When ALE switches LO, Q_{11} turns off and Q_{15} turns on causing V_E to jump to about 11V. This signal at V_E is the voltage switching, which generates the −5V level. Diode CR10 clamps node V_D to 0.7V (max). Since voltage will not change instantaneously across C23, V_D appears as the waveform in Figure 1-42.

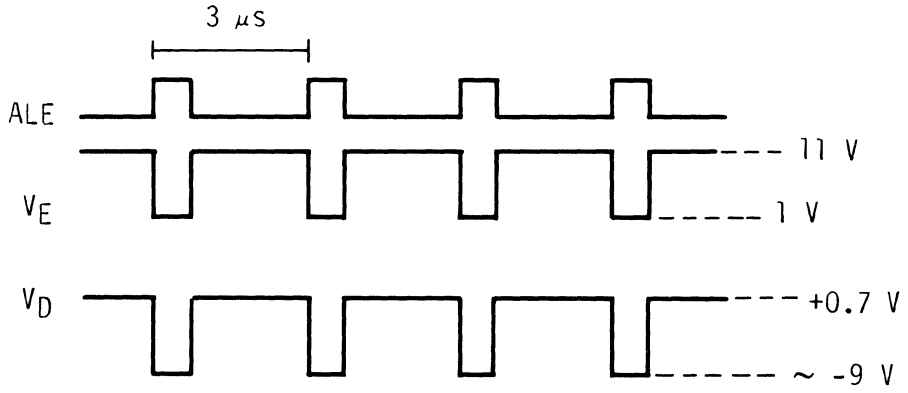

FIGURE 1-42
Waveform in -5V Converter Circuit

When V_E is HI, C23 is charged with approximately an 11V potential. When V_E switches to LO, C23 maintains the potential, forcing V_D to −10V. With node V_D at −10V, CR9 is forward-biased, putting V_D at roughly −9V. When V_D switches to 0.7V, C24 (which has been charged with the −9V drop) supplies current to the output. Thus, the output at V_O is about −8V. This voltage is then filtered with CR20, a 5.1V Zener diode to provide the $-5V_B$ supply.

SECTION 2
LOGIC CONVENTIONS AND CIRCUIT DIAGRAMS

2.1 INTRODUCTION

Quantum's logic diagrams emphasize the functions performed by the logic elements rather than the kinds of devices used. For example, a NAND gate may appear on a Quantum diagram as either a positive logic AND function with the output inverted (NAND), or as a negative logic OR function with the inputs inverted (NOR). This practice runs contrary to some logic drawing standards that require the use of the NAND symbol for both functions, but aids field service personnel in troubleshooting and system design engineers in understanding the principles of operation of the design.

This functional approach to logic symbology is basic to the logic documentation conventions employed by Quantum. The conventions that govern logic symbology, signal nomenclature, and other drawing standards that may help the reader interpret Quantum logic diagrams are discussed in the following paragraphs.

2.2 LOGIC SYMBOLOGY

The logic function symbols that Quantum uses in logic diagrams conform closely to those set forth in MIL-STD-806 or ANSI Y32.14-1973. Small scale integration (SSI) circuits are represented by their function symbol. Medium scale (MSI) and large scale (LSI) integration devices, such as shift registers, RAMs, ROMs, etc., are represented by rectangles with function labels. Since both positive and negative logic conventions can appear in a single diagram, the unfilled-circle negation symbol specified by MIL-STD-806 or ANSI Y32.14-1973 is used to distinguish between LO true and HI true signals.

Usually, all logic symbols are drawn with inputs on the left and outputs on the right. Some device symbols, such as flip-flops, show inputs and other external connections on the top and bottom of the symbol for clarity. Also, the drawings themselves usually show major signal flows from left to right, top to bottom. However, drawing layout restrictions occasionally require that the major signal to be drawn is in the reverse direction so that some symbols are drawn with a vertical orientation.

2.3 COMPONENT LOCATIONS

Quantum uses two component location systems. One, shown on the perimeter of the diagram, is useful in locating a portion of a circuit or a particular component on the diagram itself, and has no other meaning. The other involves the component identifiers. The identifier is a numbering code for locating that component on its printed circuit board; the identifier consists of an alpha character (denoting component type) followed by an assigned number. For example, R17 is the resistor assigned to be "17." Table 2-1 shows the component identifying codes.

TABLE 2-1
Q500 Component Codes

CODE	COMPONENT
C	Capacitor
CR	Diode
E	Jumper Option
L	Inductor
R	Resistor
RN	Resistor Network
U	Integrated Circuit
VR	Voltage Regulator
Y	Crystal
P	Connector
TP	Test Point
Q	Transistor
J	Interface

2.4 CIRCUIT DIAGRAMS

The schematic diagrams which follow represent the latest version of each circuit board in current production at the time of preparation of this manual.

There are two important part numbers associated with each circuit board in the Q500: the PCB assembly part number and the PCB part number.

1) The PCB assembly part number identifies the complete circuit board with components installed. This number is etched onto the top (component) side of the PCB. The revision letter of the board assembly is also etched on this side of the PCB also.

2) The PCB part number (fabrication number) is the part number of the blank PCB. This number is etched on the bottom (solder) side of the PCB. The revision letter of the fabrication is also etched on this side.

This section contains the following schematics:

Figure 2-1 Power-On Reset, Regulators, and Filters Circuits

Figure 2-2 Interface Control and Head Select Circuits

Figure 2-3 Read/Write Circuits

Figure 2-4 Actuator Positioning and Control Logic Circuits

Figure 2-5 Motor Microprocessor and Motor Driver Circuits

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS ARE IN MICROFARADS (UF)
2. ALL 0.1 UF CAPACITORS ARE +80%, -20%, 50V
3. ALL RESISTORS ARE IN OHMS.
4. ALL INDUCTORS ARE IN MICROHENRIES, ±10%
5. ALL DIODES ARE IN4152
6. ALL TRANSISTORS ARE PN2222A
7. —□ □— INDICATES JUMPER OPTION, —□-□— INDICATES CUT TRACE OPTION, —□ □— INDICATES SHORTING PLUG INSTALLED
8. +5V GND CONNECTIONS ARE PINS 14 AND 7 (14 PIN DIP), OR PINS 16 AND 8 (16 PIN DIP), OR PINS 20 AND 10 (20 PIN DIP), OR PIN 1 AND 4 (8 PIN DIP)
9. ALL CAPACITORS BELOW 1000 PF ARE 50V, ±5%

CONNECTOR REFERENCE SYMBOLS:

- P4 24 SOCKET INTERCONNECT
- J1 34 PIN CONTROL INTERFACE
- J2 20 PIN DATA INTERFACE
- P5 10 PIN DC MOTOR
- J8 2 PIN FRONT PANEL LED
- P3 4 PIN DC POWER INPUT

80-21012

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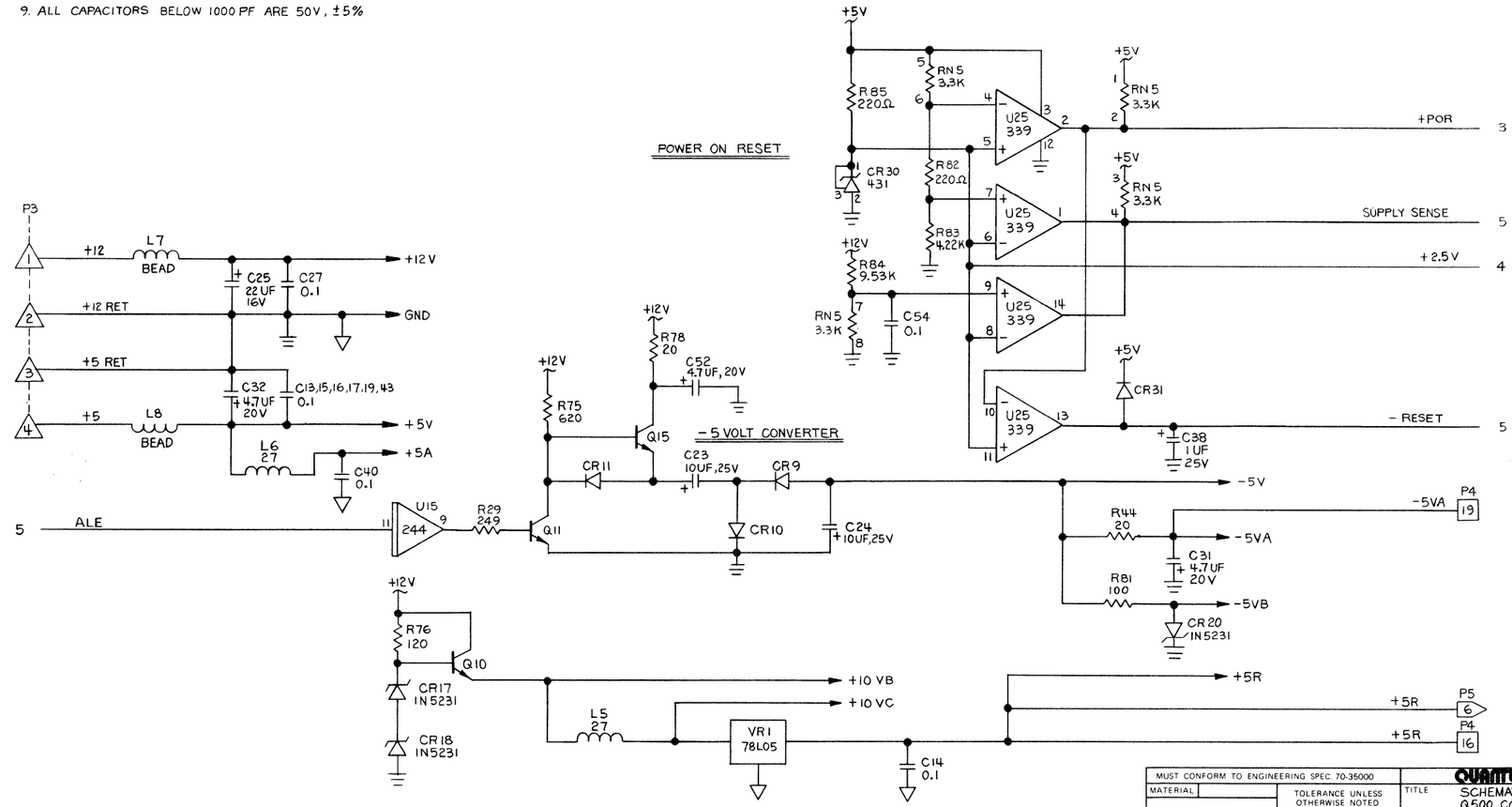

MUST CONFORM TO ENGINEERING SPEC 70-35000		QUANTUM CORPORATION	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE	SCHEMATIC, Q500 CONTROL
	LINEAR ± .XX / ± .XXX	DETAIL ALICE 10-10-83	RELEASED FOR ASSEMBLY
CASE DEPTH		DESIGN 3-15-84	20-2101 D
HARDNESS	ANGULAR ±	APPRO	SHEET 1 OF 5
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX	SCALE	.80-21012 REV A

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A2815

FIGURE 2-1
Power-On Reset, Regulators, and Filters Circuits

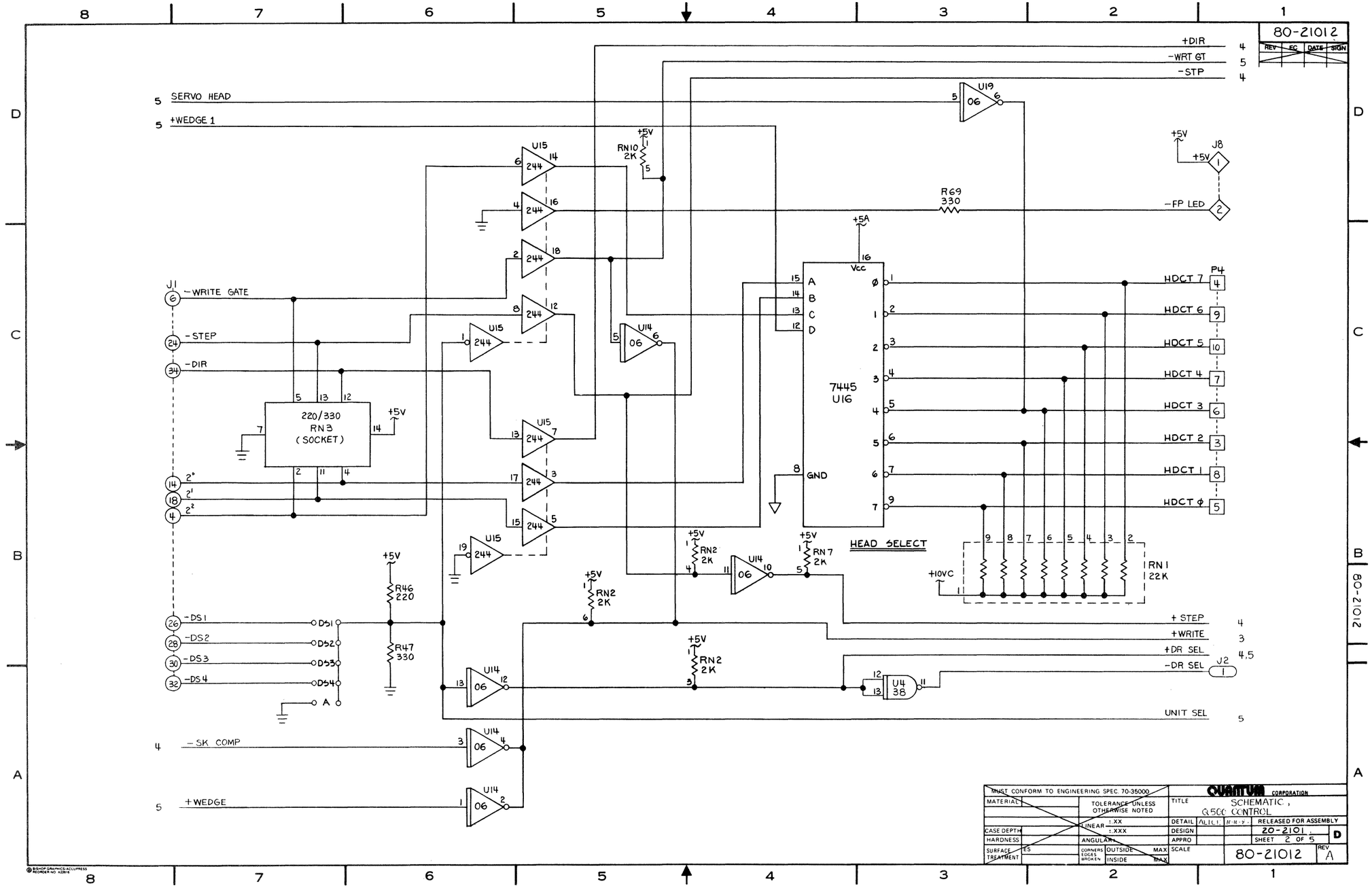

FIGURE 2-2
Interface Control and Head Select Circuits

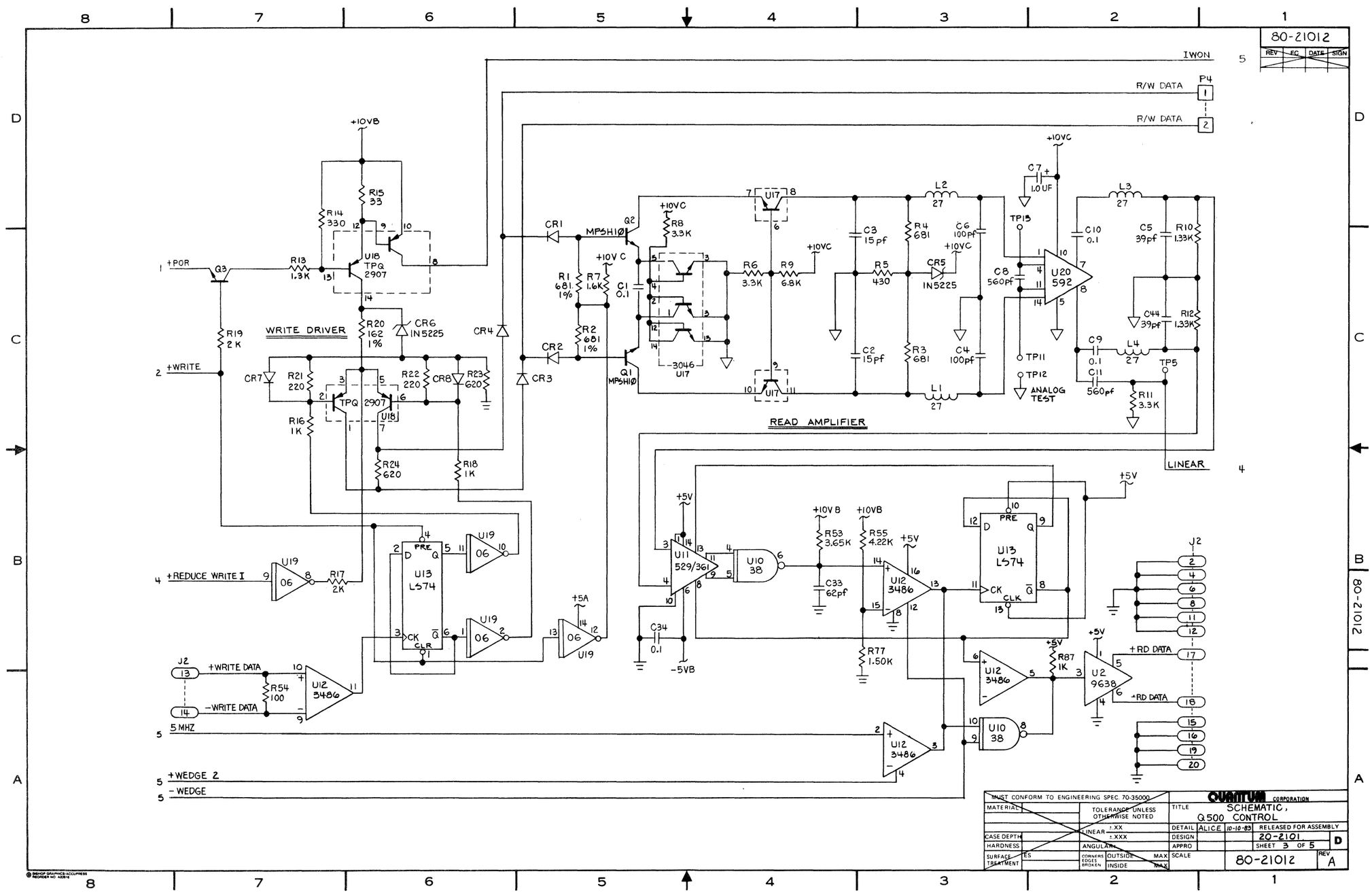

FIGURE 2-3
Read/Write Circuits

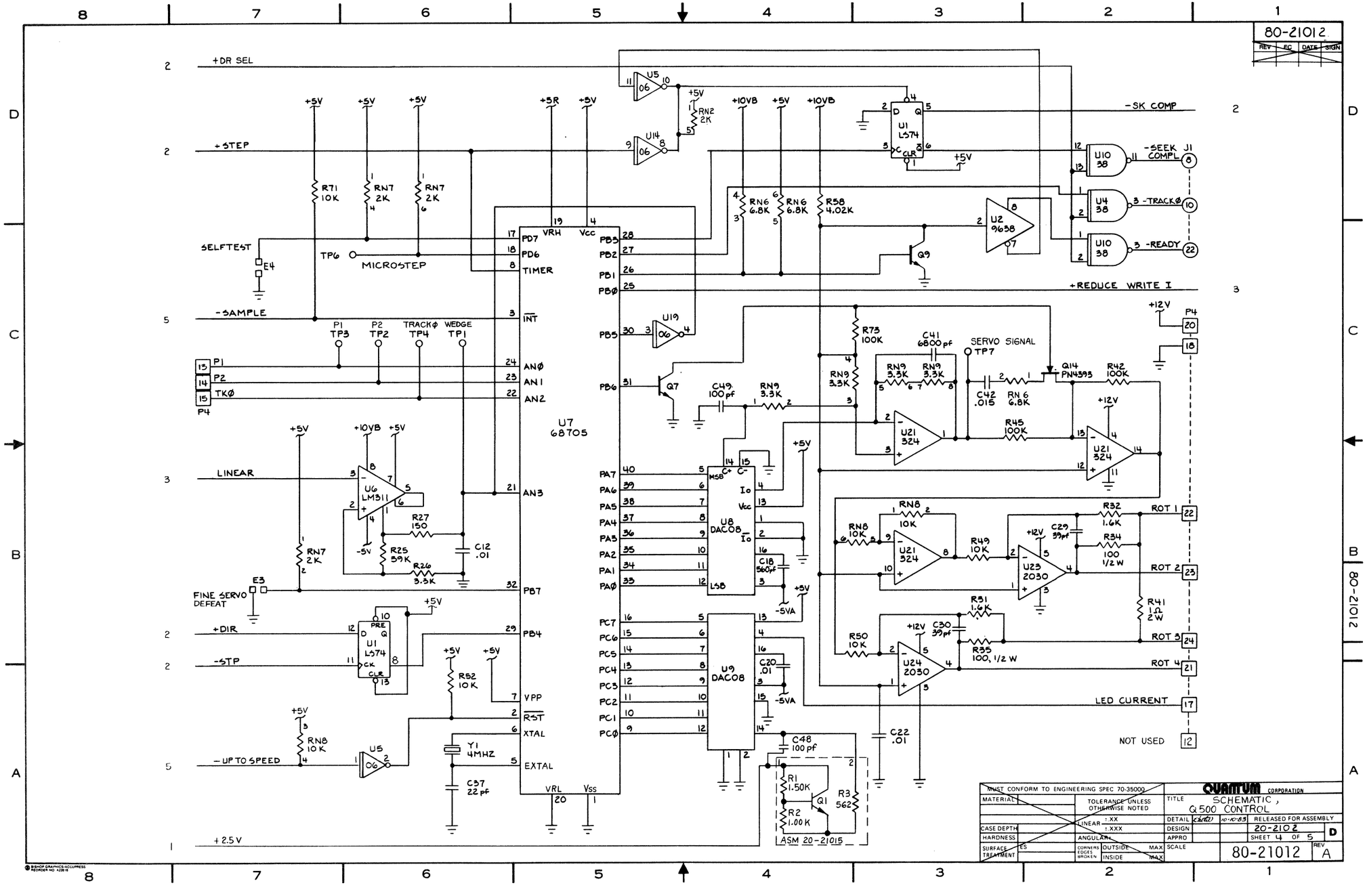

FIGURE 2-4
Actuator Positioning and Control Logic Circuits

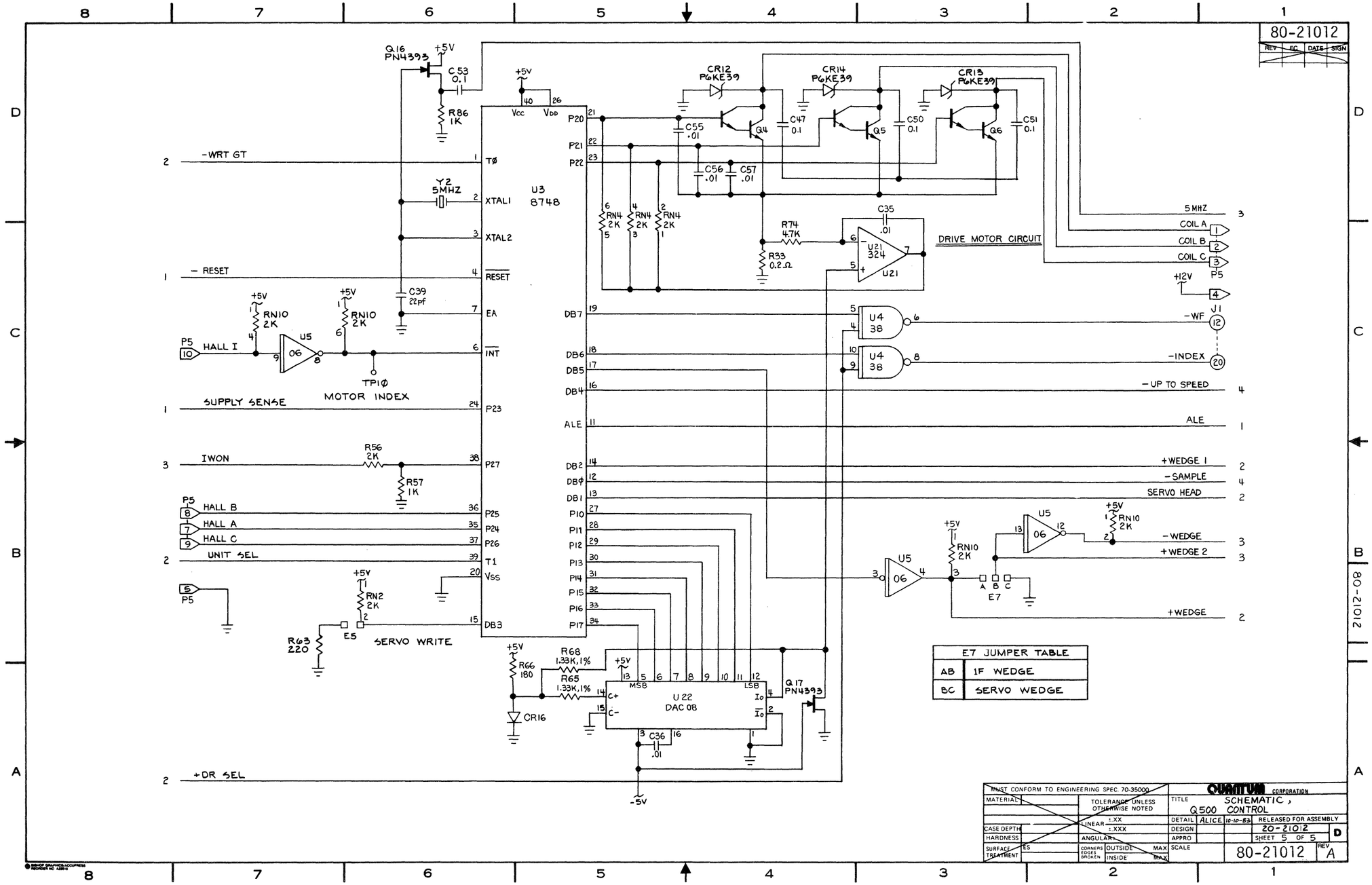

FIGURE 2-5
Motor Microprocessor and Motor Driver Circuits

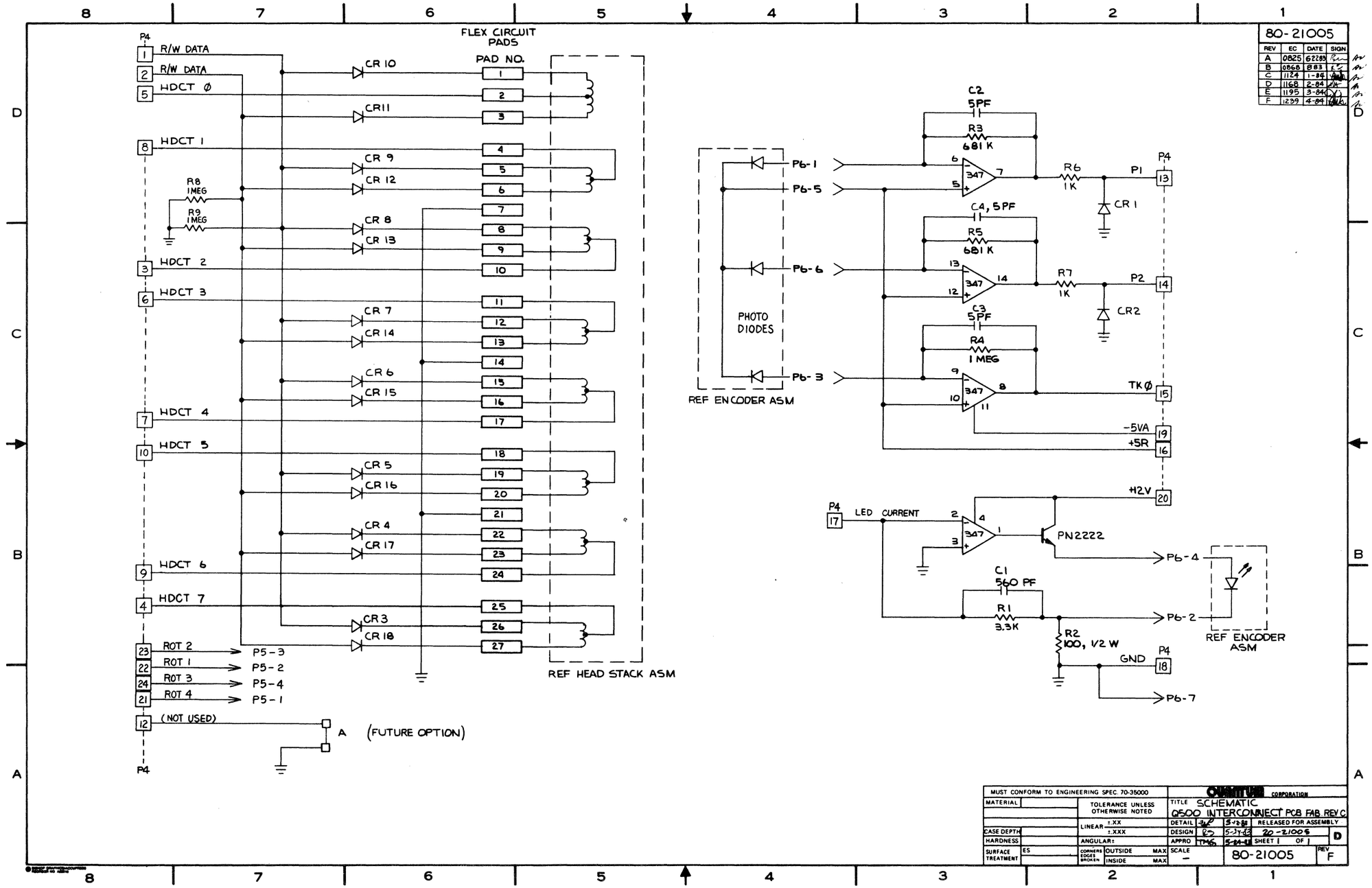

FIGURE 2-6
Encoder PCB (Under Bubble)

SECTION 3
APPLICATIONS

3.1 INTRODUCTION

The Q500 may be used in a number of different system applications. Each application of the drive will vary depending on system design, software, drive controller, cabinet design, etc. This section provides information on the key areas of the drive and drive usage that could affect the integration of the drive into the system.

3.2 SPECIAL CONSIDERATIONS

3.2.1 WRITE FAULT

The Q500 checks for a WRITE FAULT six times per revolution of the disk. The drive uses Hall Effect sensors as a trigger when checking for WRITE FAULT. During each check, the motor microprocessor polls DRIVE SELECT, WRITE GATE, and write current to determine whether to issue a WRITE FAULT at the interface. The dc voltage levels are also monitored by the motor microprocessor: if low, a WRITE FAULT is issued. A false WRITE FAULT could result if DRIVE SELECT, WRITE GATE, or write current change more than once while a check is in progress. To ensure against a false WRITE FAULT, the controller should always maintain WRITE GATE in either state more than 44 μs at a time (the cycle time for the WRITE FAULT routine). This allows time for the motor microprocessor to complete the WRITE FAULT routine before the state of WRITE GATE changes.

3.2.2 TRACK-TO-TRACK ACCESS TIME

The operating temperature of the drive affects the track-to-track access time of the Q500. Initially, the drive sets all the thermal zones during the first seek operation to a zone following a power-up. While the drive is cold, the zone timer times out quickly. If the heads cross a thermal zone boundary, the actuator microprocessor updates the servo infomation. If the new servo information differs significantly from the previously stored value, the microprocessor rereads the servos. Assuming the worst case (single step seek that crosses a zone boundary with the actuator arriving at the track just as the servo information has passed the head), the seek takes 49 ms (12 ms for the seek + 34 ms for servo update + 3 ms for correction.)

The initial track-to-track time for a cold drive must be accounted for in the seek time-out timer of the controller.

As the drive reaches operating temperature (in approximately 45 minutes), the zone timer extends to a maximum of 22 minutes. Thermally stable drives require fewer servo updates. When the drive approaches operating temperature and all zones have been updated at this temperature, track-to-track seek times will not exceed 12 ms.

3.3 ERRORS AND MEDIA DEFECTS

3.3.1 INTRODUCTION

An error is defined as any discrepancy between recorded data and recovered data. High density digital recording systems require a scheme for error detection and correction to enhance the performance and increase the reliability of the system. Disk storage systems record data as a precisely timed bit stream. A data separator uses this precise bit positioning to detect data bits during data recovery.

3.3.2 ERRORS

In these systems, three types of errors occur: drop-outs, drop-ins, and phase shifts.

A drop-in occurs when the system sees a bit when it was not expecting to see one. This happens when a media flaw causes a rise in signal amplitude. A drop-out is a bit that has shifted from its nominal position further than the data separator can tolerate due to a signal amplitude decrease. Phase shift defects are small shifts in the data signal that the data separator cannot tolerate; these defects have little or no effect on the signal amplitude.

The errors can be either "soft" (not readily repeatable) or "Hard" (repeatable with high probability). Soft errors are generally related to the signal-to-noise ratio of the system. They represent marginal conditions of the media, heads, read/write circuitry, and the controller and data separator circuits. Hard errors are most often due to defects, pits, scratches, or thin spots on the media. These defective media areas can be detected and identified by the track and position. Having this position information allows a user to skip these bad areas when recording data.

3.3.3 DEFECT DETECTION AND REPORTING

Quantum uses a unique analog media test system which measures both the amplitude and phase distortion of each bit that can be recorded on all tracks of all surfaces. The test system provides a defect map which is chipped with each drive. The defect location is identified on the map by cylinder number, head number, number of bytes from index, and number of bits in length. The numbers are given in decimal notation.

3.3.4 MEDIA QUALITY CRITERIA

Each drive that Quantum ships meets or exceeds the following standards of media quality:

1. Cylinder zero (0) will be free of defect areas.
2. No surface will have more than 10 defect areas.
3. No surface will have more than four tracks with multiple defect areas.
4. No drive will have more than one error per megabyte of unformatted storage capacity.

Quantum defines a defect area as an area equal to or less than 16 bits in length. Hence a defect area 17 bits in length counts as two defect areas and a defect area 16 bits in length counts as one defect area.

3.4 TRACK FORMATTING

3.4.1 INTRODUCTION

With the high transfer rates and large capacities of disk drives, data are normally stored in small, easily managed blocks. As the data are stored in a serial bit stream on a circular track, thse blocks can be thought of as segmenting the track. These segments are called sectors.

The method used to define the boundaries of these sectors classifies the drives as hard- or soft-sectored. A hard-sectored drive defines its sector boundaries by some fixed mechanical method. A soft-sectored drive has its sector boundaries defined by an identification (ID) field which is written on the track by the user. With either sectoring method, data bits cannot occupy all of the available bit positions on the track. Gaps must be placed between sectors to compensate for spindle speed and write oscillator tolerances and also to mask head-switching time, write-to-read recovery time, and the write update splice.

3.4.2 TRACK FORMAT

The position of the gaps between sectors and the length of these gaps and ID fields around the track is called a format. Formatting a drive is the process of writing this format on all tracks and surfaces of a drive.

The Q500 is a soft-sectored drive, and, as such, can use whatever format the user desires. In choosing or designing a format for the Q500, the following drive specifications must be considered:

1.	Head-switching time	20 μs maximum
2.	Write-to-read recovery time	20 μs maximum
3.	Spindle speed tolerances (Index timing)	±1% of the nominal Speed 3529 RPM
	A. Index Period:	17 ms ± 1%
	B. Index Drift:	The index edge with respect to data written by any head near index time will move less than 20 μs over conditions of age, environment, and voltage.
	C. Index Period Jitter:	The time variation between two successive index periods is ±8.0 μs maximum, but never a total of 15 μs for one revolution.
4.	Head, media, and read/write channel characteristics	These items are selected and optimized for MFM coding at a transfer rate of 5.0 Mbits/s.

3.4.3 SAMPLE FORMAT

The soft-sector format shown in Figure 3-1 is a slightly modified version of the IBM System 34 double density format commonly used on 8-inch floppy disk drives. Data are encoded using the modified frequency modulation (MFM) code.

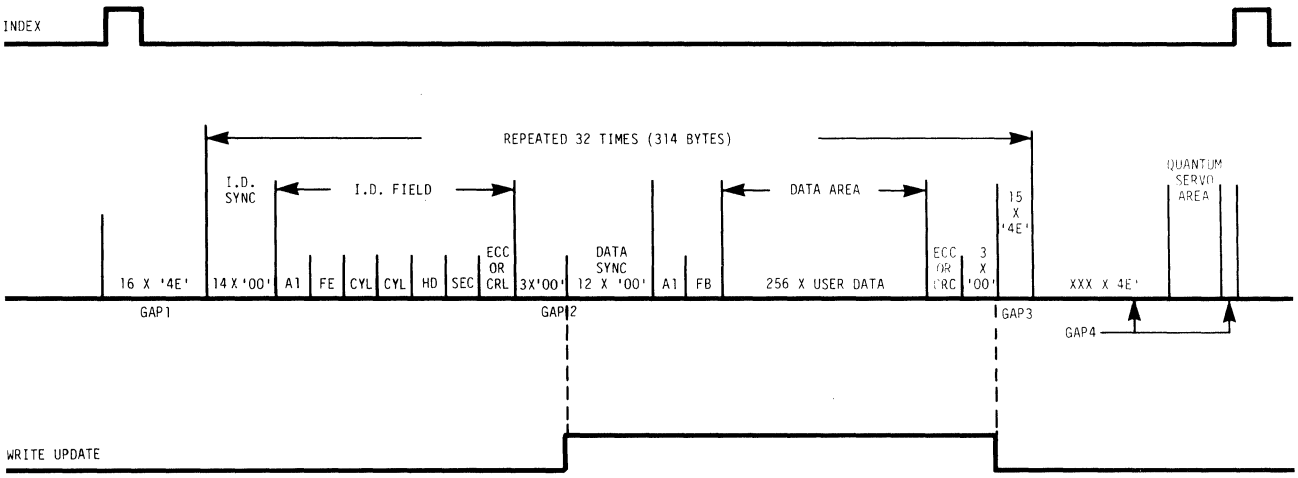

FIGURE 3-1
Sample Track Format

3.5 WRITE PRE-COMPENSATION

Recording data at high bit densities creates a phenomenon known as intersymbol interference. This occurs when two bits must be recorded closer to each other than to neighboring bits. When these two bits are read back, intersymbol interference causes the bits to appear to be shifted away from each other by an amount depending on head/media resolution. This is the major cause of bit shift in data recording systems. Other factors such as speed variations and random head, disk and circuit noise contribute to bit shift to lesser degrees. When bit shift is great enough, read errors occur.

Bit shift is density related and, therefore, more apparent on the shorter, innermost cylinders. The Q500 user may reduce bit shift by employing write precompensation when writing above cylinder 256. The Q500 automatically reduces write current by approximately 20 percent at cylinder 256. Write precompensation is a technique whereby the bit patterns that cause the greatest intersymbol interference are detected and those bits that are predicted to shift early or late are correspondingly written late or early. The recommended amount of precompensation for the Q500 is 12 ns for both early and late written bits.

Table 3-1 shows those bit patterns that require precompensation, the shift direction expected, the precompensation direction and the type (clock or data) pulse to write for MFM encoding.

TABLE 3-1
Write Precompensation

DATA PATTERN	EXPECTED SHIFT DIRECTION	PRE-COMPENSATE	TYPE OF PULSE
1 2 3 4	**For Data in Cell 3**	**Direction**	**To Write**
0 0 0 0	None	On Time	Clock
0 0 0 1	Late	Early	Clock
0 0 1 0	None	On Time	Data
0 0 1 1	Early	Late	Data
0 1 0 0	None	No Clock or Data Written	
0 1 0 1	None	No Clock or Data Written	
0 1 1 0	Late	Early	Data
0 1 1 1	None	On Time	Data
1 0 0 0	Early	Late	Clock
1 0 0 1	None	On Time	Clock
1 0 1 0	None	On Time	Date
1 0 1 1	Early	Late	Data
1 1 0 0	None	No Clock or Data Written	
1 1 0 1	None	No Clock or Data Written	
1 1 1 0	Late	Early	Data
1 1 1 1	None	On Time	Data

Data is encoded in the sequence 1,2,3,4 and written from Cell 3. Clock pulses are written positioned at the beginning of a cell time (200 ns), and data pulses are written in the center of a cell time.

3.6 GROUNDING PROCEDURES

The Q500 shock mount brackets are electrically isolated from the logic/power ground to separate the chassis ground of the system from the power ground at the drive. However, the base casting and bubble of the Q500 are connected to the logic/power ground. Quantum provides a grounding lug for optional connection between the chassis ground and the logic/power ground. When the grounding lug is used, Quantum recommends the use of a large diameter braid to ensure a low impedance path for higher frequency components.

3.7 EMI CONSIDERATIONS

System designers should ensure isolation from electromagnetic interference (EMI) caused by other peripherals, PCBs, or switching power supplies in proximity to the hard disk. EMI may result in random soft errors on the disk. To reduce most external EMI effects, the Q500 drive media and heads are enclosed in an aluminum bubble and base casting. In addition, the drive includes an EMI band to ensure good shielding of the gap between the base casting and the bubble.

EMI from a system may occasionally affect the Q500 despite these precautions. If a drive fails to meet the specified error rate when mounted in the system, but shows no problem when removed from the system (the connection is maintained through extended cables), external EMI effects can be assumed. Errors generated by external EMI can show up as constantly appearing, random, nonrepeating soft errors. These errors frequently occur at the inner cylinders where the signal-to-noise ratio is lowest.

When external EMI errors occur, take steps to isolate the EMI source and shield the drive as required. If the problem persists, contact Quantum's Technical Support Group for assistance.

3.8 DAISY-CHAIN TERMINATION

Up to four Q500 drives (or a combination of Q500 drives and other peripherals) may be daisy-chained to one control cable. In a daisy-chain, terminate the drive or peripheral at the end of the cable. Never terminate more than one device in the chain. If the peripheral at the end of the chain is not a Q500, make sure to terminate WRITE GATE, STEP, DIR, HEAD 2^0, HEAD 2^1, and HEAD 2^2 at the terminator. This procedure ensures proper operation of the Q500s in the chain.

3.9 SELF DIAGNOSTICS

A self diagnostic routine may be established by placing a jumper at E4. Use this self diagnostic to exercise the drive's ability to seek. This routine tests approximately 90 percent of the hardware and firmware, with the exception of the drive interface circuits and the firmware for step interrupt and the servowriter microstep mode.

When the self diagnostics detect an error, the microprocessor sends READY until the power is recycled. There are no retries during the self-diagnostic routine.

The self diagnostic routine detects the following errors:

1. Seek errors greater than a 14-track overshoot
2. Fine servos when the servo amplitude is too small
3. Improper track 0 level

The self diagnostic routine performs a butterfly seek. When self diagnostics are initiated, the microprocessor commands the actuator to go to track 256. Then the microprocessor initiates the following pattern of seeks: 256 to 255, 255 to 257, 257 to 254, 254 to 258. . .511 to 0. When the actuator returns to track 0, the process is repeated.

Fine servos, if enabled (no E3 jumper) are read between each seek.

SECTION 4
MAINTENANCE

4.1 GENERAL INFORMATION

Quantum has achieved high reliability in the Model Q500 through simplicity of mechanical design and extensive use of microelectronics. The Model Q500 is designed for fast, easy subassembly replacement with no adjustments, thereby significantly reducing downtime for unscheduled repairs.

The Model Q500 does not require any preventative maintenance.

4.2 MAINTENANCE PRECAUTIONS

Observe the following precautions during service to avoid personal injury and damage to the Model Q500.

1. DO NOT open or remove the metal bubble or its seals unless the drive is in a Class 100 clean environment. Removal of the bubble or its seals will void the warranty.

2. Exercise caution if operating the drive with the PCB unmounted (because of rotating spindle motor).

3. Do not lift the drive by the face plate or the PCB.

4. Avoid harsh shocks to the drive at any time.

5. To make sure the actuator is completely locked, do not move the drive for 27 seconds after dc power is removed.

4.3 JUMPERS AND TEST POINTS

Tables 4-1 and 4-2 define the jumpers and test points, respectively, Table 4-3 describes the connectors.

TABLE 4-1
Jumper Definitions

JUMPER	EFFECT
A	Continuous DRIVE SELECT when jumpered.
DS1	DRIVE SELECT 1
DS2	DRIVE SELECT 2
DS3	DRIVE SELECT 3
DS4	DRIVE SELECT 4
E3	When jumpered, disables servos and causes the drive to use only the glass scale for positioning; for diagnostic use only.
E4	When jumpered, causes the drive to perform a continuous seek diagnostic. If the drive stops seeking while the jumper is on, this indicates a possible drive problem.
E5	Quantum internal use only. Do not jumper. Warranty will be voided if jumpered.
E7-AB	Puts a IF square wave signal out to the data cables during the wedge time (290 μs prior to Index).
E7-BC	Puts IF servo bursts to the data cable during servo wedge time.

TABLE 4-2
Test Point Definitions

TEST POINT	EFFECT
TP1	Peak detected servo wedge information
TP2	P2 signal from optical encoder
TP3	P1 signal from optical encoder
TP4	Track 0 signal from optical encoder
TP5	Single-ended output of read channel
TP6	Microstep (Quantum use only)
TP7	Actuator control output
TP10	Raw index from the spindle motor
TP11	Differential amplifier input
TP12	Analog ground
TP13	Differential amplifier input

TABLE 4-3
Connector Descriptions

CONNECTOR	DESCRIPTION
J1	Control interface
J2	MFM data interface
J6	Ground tab on casting
J8	Front panel LED connector
P3	Power connector
P4	Encoder board connector
P5	Motor connector

4.4 LEVEL I MAINTENANCE

Level I maintenance consists of the following:

1. Unit replacement
2. Drive Control Circuit board exchange
3. External faceplate subassembly replacement

The following items should be available to personnel performing Level I maintenance on the Model Q500.

1. An assortment of hand tools adequate for electronic/mechanical repair
2. One drive control PCB: Quantum part number 20-21012
3. One front faceplate assembly: Quantum part number 75-50082
4. A #2 Phillips-tip screwdriver

4.5 LEVEL 2 MAINTENANCE

Level 2 maintenance consists of Level 1 maintenance plus the following:

1. Major disassembly and refurbishment of the drive
2. Repair of circuit boards

If you require Level 2 maintenance, please contact Quantum for information.

NOTE

The user's service activity should be limited to Level 1 procedures during the warranty period. The Quantum warranty is null and void when any Level 2 procedure has been attempted. In addition, no sub-bubble repairs are authorized. All time and material required to restore the drive to working order will be billed at prevailing rates.

SECTION 5
Q500 DESCRIPTION AND PARTS LIST

5.1 ILLUSTRATED PARTS

Figures 5-1 and 5-2 illustrate THE Q500 Disk Drive.

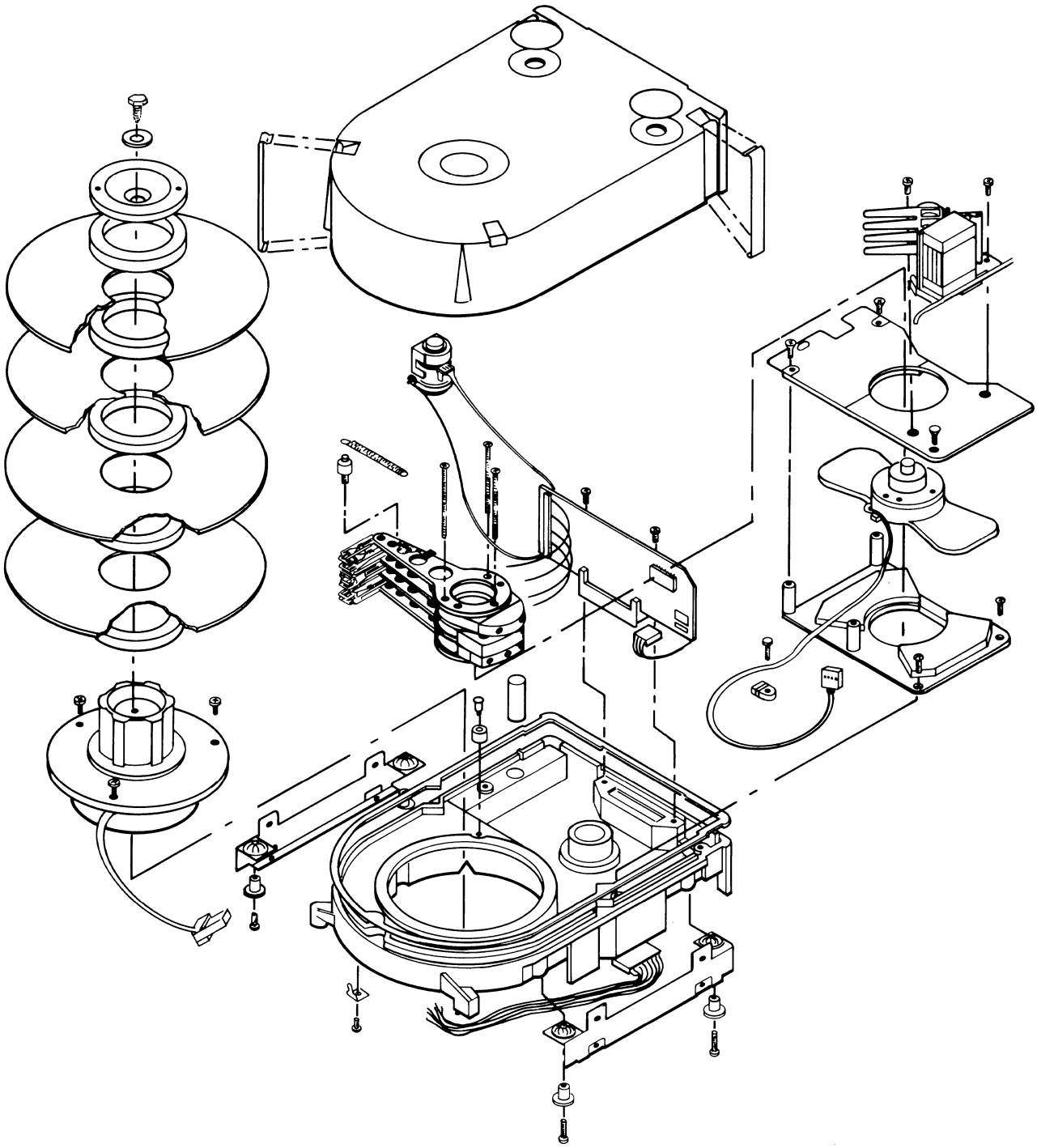

FIGURE 5-1
Q500 Exploded Parts Diagram

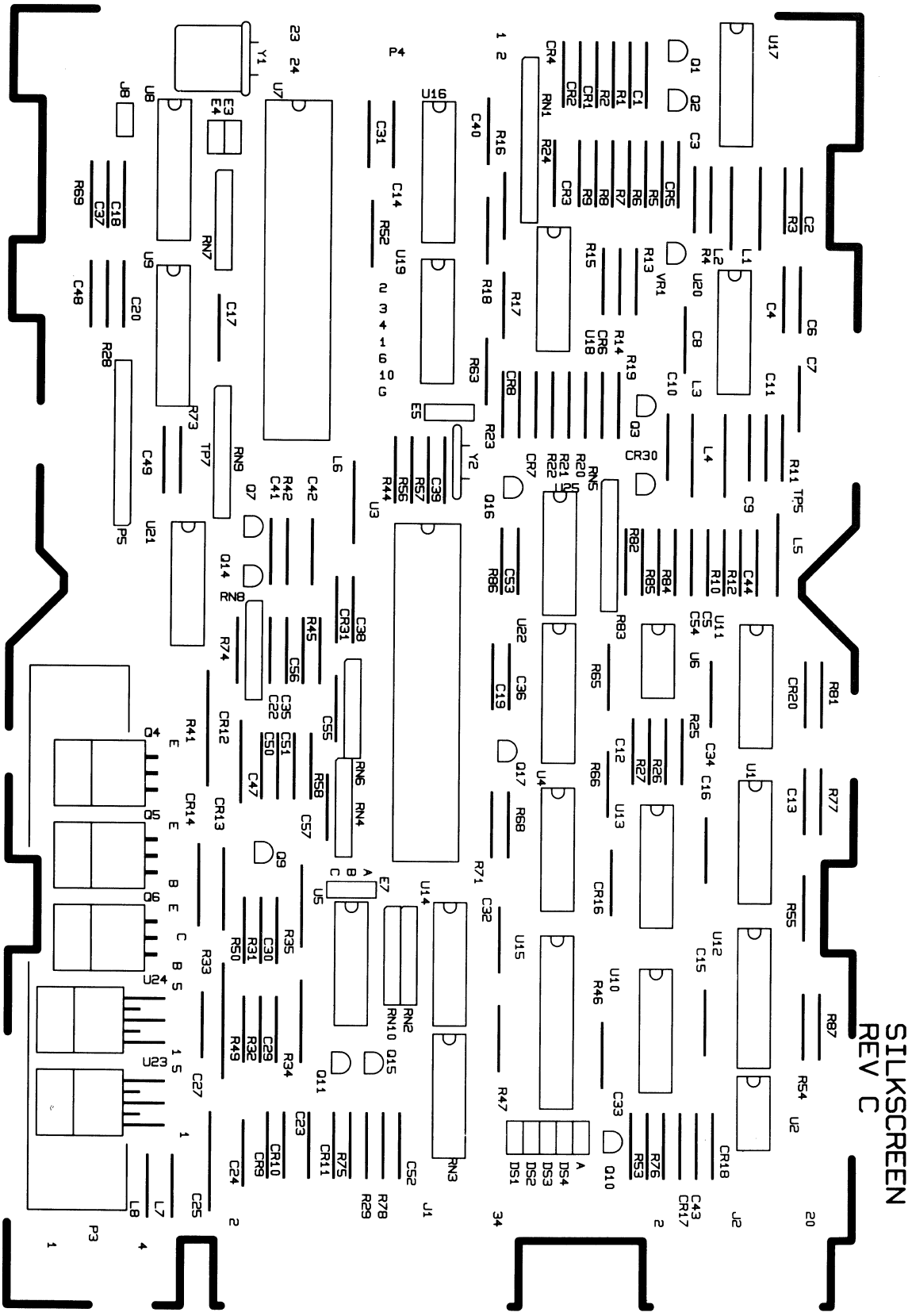

FIGURE 5-2
Drive Control PCB

5.2 PARTS LIST

This section lists the references and corresponding descriptions of the components of the drive control PCB.

Ref.	Description
RESISTORS	
R15	33 ohm ¼W 5%
R54, 81	100 ohm ¼W 5%
R21, 22, 46, 63, 82, 85	220 ohm ¼W 5%
R14, 47 69	330 ohm ¼W 5%
R5	430 ohm ¼W 5%
R23, 24, 75	620 ohm ¼W 5%
R16, 18 57, 86, 87	1.0 kohm ¼W 5%
R13	1.3 kohm ¼W 5%
R31, 32, 7	1.6 kohm ¼W 5%
R17, 19, 56	2.0 kohm ¼W 5%
R6, 8, 11, 26	3.3 kohm ¼W 5%
R25	39 kohm ¼W 5%
R9	6.8 kohm ¼W 5%

Ref.	Description
RESISTORS	
R74	4.7 kohm ¼W 5%
R49, 50 52, 71	10 kohm ¼W 5%
R44, 78	20 ohm ¼W 5%
R42, 45, 73	100 kohm ¼W 5%
R66	180 ohm ¼W 5%
R20	162 ohm ⅛W 1%
R77	1.5 kohm ⅛W 1%
R1, 2, 3, 4	681 ohm ⅛W 1%
R10, 12, 65, 68	1.33 kohm ⅛W 1
R76	120 ohm ¼W 5%
R34, 35	100 ohm ½W 5%
R33	0.2 ohm 3.0W 1% WW
R41	1.0 ohm 2.0W 5% MOX
R58, 53	4.02 kohm ⅛W 1%
R27	150 ohm ¼W 5%
R84	9.35 kohm, ⅛W, 1%
RN3	220/330 ohm DIP 14 Pin
R83, 55	4.22 kohm, ⅛W, 1%
RN2, 4, 7, 10	2.0 kohm 6 Pin 5 Res
RN9, 5	3.3 kohm 8 Pin 4 Res
RN8	10 kohm 6 Pin 3 Res
RN6	6.8 kohm 6 Pin 3 Res

Ref.	Description
CAPACITORS	
RN1	22 kohm 10 Pin 9 Res
R29	249 ohm ⅛W, 1%
C2, 3	15 pF Cer 50V 5% COG (NPO) AX
C5, 29, 30, 44	39 pF Cer 50V 5% COG (NPO) AX
C33	62 pF Cer 50V 5% COG (NPO) AX
C4, 6, 48, 49	100 pF Cer 50V 5% COG (NPO) AX
C8, 11, 18	560 pF Cer 50V 5% COG (NPO) AX
C41	6800 pF Cer 50V 10% x 7R
C37, 39	22 pF Cer 5% COG (NPO) AX
C42	0.015 uF Polyester 5% AX
C20, 22, 35, 36, 12, 55 56, 57	0.01 uF Cer X7R 10% AX
C1, 9 10, 13-17, 19, 27, 34, 40, 43, 47 50, 51, 53, 54	0.1 uF Cer Z5U +80% − 20% AX
C25	22 uF Elect 16V AX +50, −20%
C38, 7	1.0 uF T ant AX 20V .100 dia 20%
C32, 31, 52	4.7 uF T ant AX 20V .100 dia 20%
C23, 24	10 uF T ant AX 20V 20%
INDUCTORS	
L1-6	27 uH Shielded

Ref.	Description
TRANSISTORS	
Q1, 2	MPS-H10
Q4, 6	TIP 100
Q3, 7, 9, 10, 11, 15	PN2222A
Q14, 16 17	PN4393
DIODES	
CR5, 6	Zener 1N5225B 3.0V 0.5W AX 5%
CR17, 18, 20	Zener 1N5231B 5.1V 0.5W AX 5%
CR1-4, 7-11, 16, 31	IN4152 0.5W AX
CR12-14	Zener, P6KE39

Ref.	Part Number	Description
	INTEGRATED CIRCUITS	
U5, 14, 19		7406 Hex Buff Inv 14P
U4, 10		7438 Quad NAND Buff 14P
U16		7445 BCD-DEC Decoder 16P
U1, 13		74LS74A Dual FF 14P
U18		FPQ2907
U20		NE592 14P DIP
U8, 9, 22		DAC 0800E 16P
U6		LM311 N(P) 8P
U21		LM324
U15		74LS244
VR1		78L05 Regulator
U23, 24		TDA 2030H Op Amp Pwr
U17		3046N Transistor Array
U11		NE529/LM361 Comparator 14P DIP
U12		3486 Diff Line Receiver
U2		9638 A Dual Diff Line Driver 8P DIP
U25		339 Comparator
CR30		431 Shunt Regulator
U7	15-50411	Servo Q500 EPROM
U3	15-50171	Motor Q500 EPROM (REV B)

Ref.	Description
	MISCELLANEOUS
Y1	Crystal, 4 MHz
Y2	Crystal, 5 MHz
L7-8	Bead, Ferrite
Q4-6	TIP 100
U3, 7	Socket, IC 40 Pin
RN3	Socket, IC 14 Pin
RN 28	ASM-PCB TEMP COMP
P5	Header, 10 Pos Rt Angle
P4	Conn., 24 Pin Card Edge
P3	Conn., 4 Pin
J8	Header, 2 Pos Rt Label, Insulator Heatsink
Q23, 24	Screw, 4-40 × ¼
Q4-6	Screw, 2-56 × ¼ Insulator, Heatsink
Q4-6	Sil Pad
Q4-6	Washer, Shoulder Ins, Fiber
TP1-7, E5(2), G, TP10, E3(2), E4(2), E7(3), A(2), DS1-4(2ea)	Pin, Test Point
	Spindle Ground Spring Asm
DS1, E7	Plug, Shorting Tab, Ground PCB

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