QLogic Corporation

ISP1000/1000U Intelligent SCSI Processor

Data Sheet

Features

- Compliance with ANSI SCSI standard X3.131-1994
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Compliance with ANSI X3T10/1071D Fast-20 standard (ISP1000U)
- Supports fast and wide SCSI transfers (ISP1000)
- Supports fast, wide, and Ultra SCSI (Fast-20) transfers (ISP1000U)
- Initiator or target mode
- Onboard RISC processor to execute operations at the I/O control block level from the host memory
- No host intervention to execute SCSI operations from start to finish
- Simultaneous, multiple logical threads

Product Description

The ISP1000/1000U is a single-chip, highly integrated, bus master, SCSI I/O processor for use in SCSI applications. It interfaces the Sun Microsystems SBus to an ANSI fast and wide SCSI bus and contains an onboard RISC processor. The ISP1000/1000U is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention. The ISP1000/1000U block diagram is illustrated in figure 1.

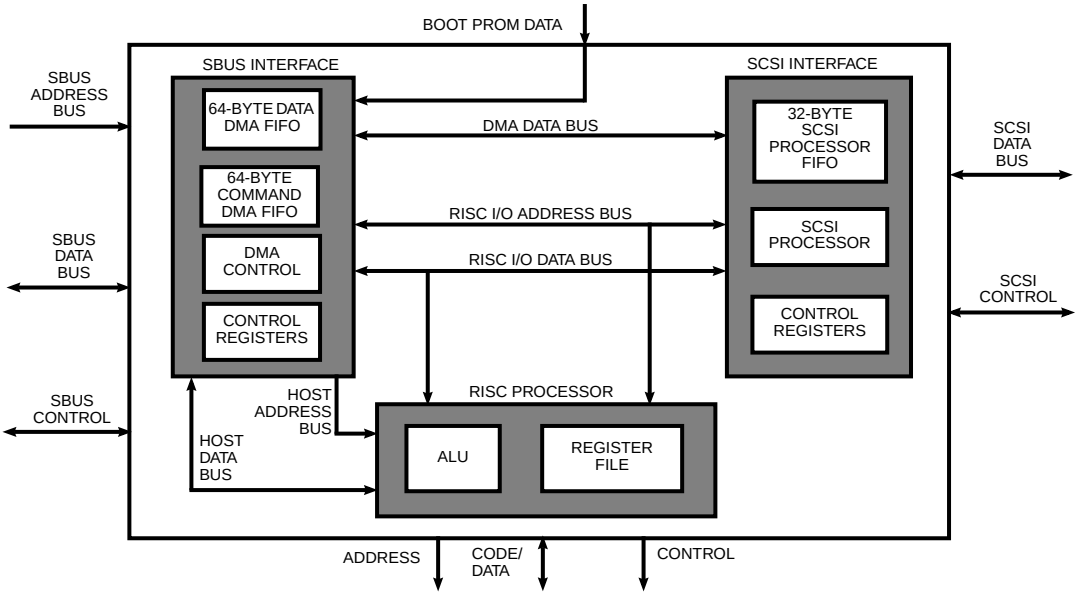


Figure 1. ISP1000/1000U Block Diagram

ISP Initiator Firmware

The ISP firmware implements a cooperative multitasking host adapter that provides the host with complete SCSI command and data transport capabilities, thus freeing the host from the demands of the SCSI bus protocol. The firmware provides two interfaces to the host: the command interface and the SCSI transport interface. The single-threaded command interface is intended for debugging, configuration, and error recovery. The multithreaded SCSI transport interface maximizes use of the SCSI and host buses, and ISP1000/1000U processing.

Subsystem Organization

To maximize I/O throughput and improve host and SCSI bus utilization, the ISP1000/1000U incorporates a high-speed, proprietary RISC processor; an intelligent SCSI bus controller (SCSI executive processor [SXP]); and a host bus dual-channel, first-party DMA controller. The SCSI bus controller and the host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance. The ISP1000/1000U RISC interface requires external program data memory.

The complete I/O subsystem solution using the ISP1000/1000U and associated supporting memory devices is shown in figure 2.

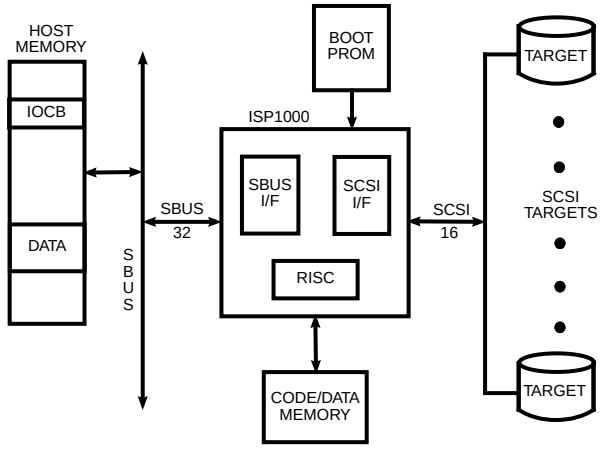


Figure 2. I/O Subsystem Design Using the ISP1000/1000U

Interfaces

The ISP1000/1000U interfaces consist of the RISC processor, SBus interface, SCSI executive processor, and FCODE boot PROM. Pins that support these interfaces and other chip operations are shown in figure 3.

RISC Processor

The RISC processor supports the following:

- High-speed instruction execution
- Flexible external memory support
- Programmable cycle time for external memory access
- Internal 16-bit wide data paths

One of the major features of the ISP1000/1000U is its ability to handle complete I/O transactions with no intervention from the host. This is accomplished with an onboard RISC processor. The ISP1000/1000U RISC processor controls the chip interfaces; executes simultaneous, multiple I/O control blocks (IOCB); and maintains the required thread information for each transfer.

The RISC memory interface is a 16-bit data path that provides access to RISC instructions, data, and I/O transactions. The RISC processor can access internal ROM as well as RAM and ROM external to the ISP1000/1000U. The first 4K words of address space are allocated for internal memory. The remaining 60K words of address space are allocated for external memory.

SBus Interface

The SBus interface supports the following:

- Address and control signals to operate as a 32-bit bus master DMA device
- Control signals to operate in 16-bit slave mode
- DMA FIFO management and data alignment, data assembly, and data disassembly
- Registers for bus ID, configuration, and DMA functions

The ISP1000/1000U interfaces directly with the Sun Microsystems SBus and operates as a 32-bit, direct virtual memory access (DVMA) master. This operation (32-bit DVMA) is accomplished through an SBus interface unit (SBIU) containing an onboard DMA controller. The SBIU generates and samples SBus control signals, generates host memory addresses, and facilitates data transfer between host memory and the onboard DMA FIFO. It also allows the host to access the ISP1000/1000U internal registers and communicate with the onboard RISC processor through the SBus slave mode operation.

The ISP1000/1000U onboard DMA controller consists of two independent DMA channels that initiate transactions on the SBus and transfer data between the host memory and the DMA FIFO. The two DMA channels are the command DMA channel and the data DMA channel. The command DMA channel has limited capability and is used mainly by the RISC processor for small transfers such as fetching commands from and writing status information to the host memory. The data DMA channel transfers data between the host memory and the SCSI bus.

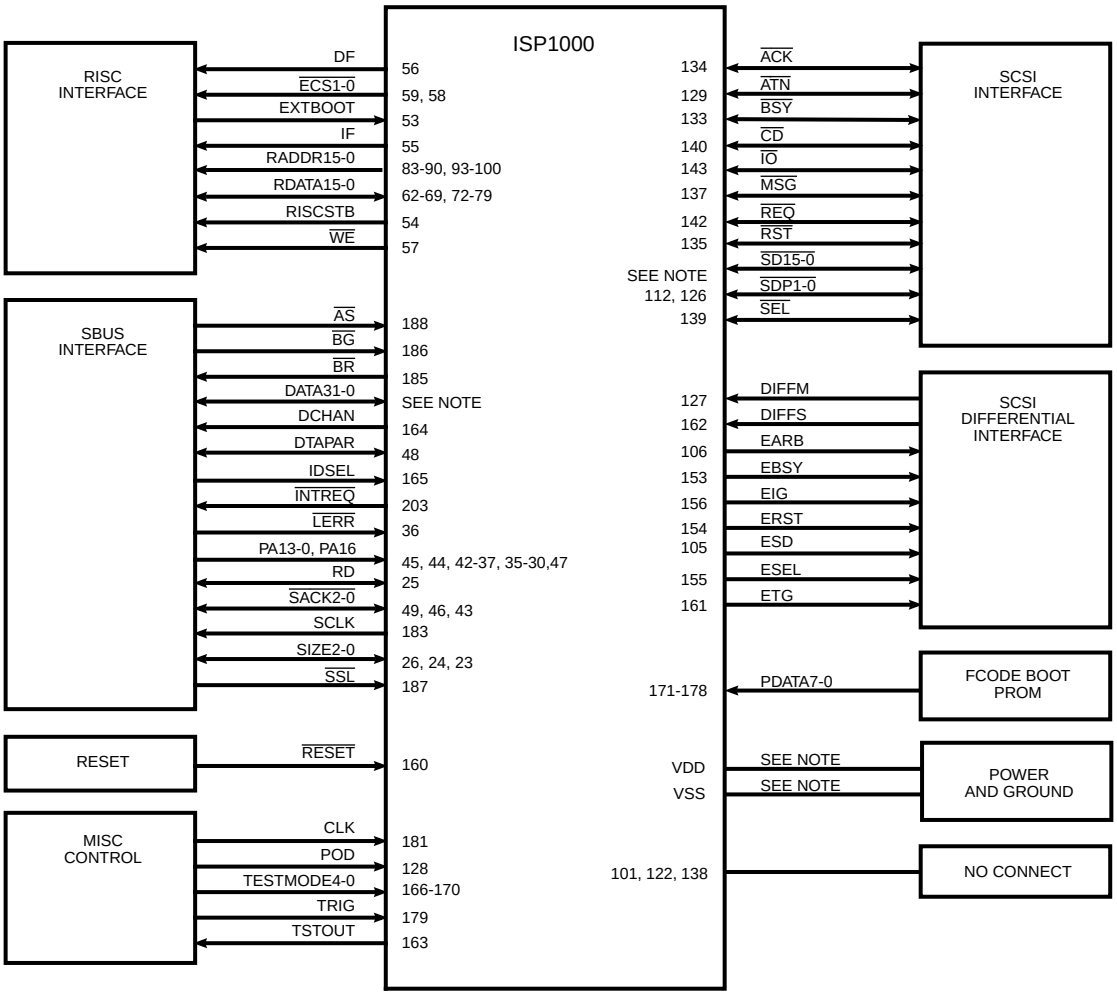
The SBIU internally arbitrates between the two channels and alternately services them. Each DMA channel has a set of registers that are programmed for transfers by the RISC processor.

SCSI Executive Processor

The SXP supports the following:

- SCSI A and P cable ready
- Asynchronous SCSI transfers up to 12 Mbytes/sec
- SCSI synchronous transfer rates:
  - 20 Mbytes/sec
  - 40 Mbytes/sec (Ultra SCSI; ISP1000U)
- Programmable SCSI processor
- On-chip data storage
- 32-bit, configurable transfer counter
- On-chip, single-ended SCSI transceivers (48-mA drivers)
- Diagnostic support

The SXP provides an autonomous, intelligent SCSI interface capable of handling complete SCSI operations. The SXP interrupts the RISC processor only to handle higher level functions such as threaded operations or error handling.



NOTE: DATA31-0 = 22-19, 16-10, 7-1, 205, 204, 202-196, 193-189
SD15-0 = 111, 109-107, 152, 150-148, 145, 124, 123, 121, 119-117, 113
VDD = 9, 18, 29, 51, 52, 60, 70, 81, 91, 103, 104, 116, 132, 144, 157, 159, 184, 194, 207, 208
VSS = 8, 17, 27, 28, 50, 61, 71, 80, 82, 92, 102, 110, 114, 115, 120, 125, 130, 131, 136, 141, 146, 147, 151, 158, 180, 182, 195, 206

Figure 3. ISP1000/1000U Functional Signal Grouping

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