MAN 1949

Prime Computer User Guide

For Diskette

PRIME COMPUTER INC., 145 PENNSYLVANIA AVENUE, FRAMINGHAM, MA 01701

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DISKETTE

USER GUIDE

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PRIME COMPUTER, INC.

[145 Pennsylvania Ave., Framingham, Mass., 01701]

Performance characteristics are
subject to change without notice.

CONTENTS

ILLUSTRATIONS

TABLES

FOREWORD

This user guide is the primary reference document for Prime Diskette storage systems.

For Diskette drive characteristics, installation, operation, and maintenance, this guide is supported by the vendor maintenance manual shipped with the equipment. See Section 1 for a list of the applicable manuals.

Because a disk system is integral to the operation of Prime's DOS and DOS/VM operating systems, the DOS-DOS/VM user guide is an important source of system-level programming information.

SECTION 1

INTRODUCTION

SCOPE

This user guide covers Prime Type 4300 Diskette storage devices.

This option comprises a controller, up to eight IBM compatible diskette drive devices, a power supply, and interconnecting cables. It is rack mountable. Only one device may be used at a time by the controller.

The storage medium is the IBM diskette used with the IBM 3540 or 3740 series systems or equivalent. The device is a moving head, contact recording small disk drive. It may be located up to 20 cable feet from the controller.

The controller is a microprogrammed typed based on Prime's microprogrammed controller. The user may specify two versions of microcode - Type 4300, a standard 256-word version, and Type 4301, a 512-word version that adds capabilities such as the Format command, the Verify command, and Micro-Verify.

REFERENCE DOCUMENTS

See Table 1-1.

FUNCTIONAL DESCRIPTION

Data Organization

Data may be organized on the diskette in three different ways: 1) the organization supported by DOS, DOS/VM, and RTOS (called the Prime Data Format); 2) the IBM data format; and 3) any user defined data format.

These three types of formats have some features in common. In all of them, the data on the diskette is organized into tracks and sectors. There are 77 tracks (numbered 0 through 76) on each diskette. Each track is divided into sectors having general organization shown below:

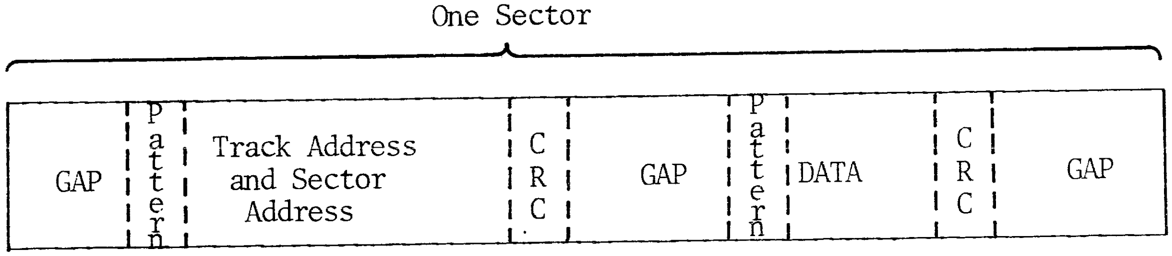


Table 1-1. Reference Documents

Title	Prime Stock No.
DEVICE VENDOR MANUALS	
Shugart Associates Model 900/901 Diskette Reference Manual	MAN 1919
Shugart Associates Guide to IBM Compabitility, SA0001	--
IBM EOM Diskette Specification	--
PRIME USER GUIDES	
Prime Installation and Maintenance Manual	MAN 1677
Macro Assembler User Guide	MAN 1673
System Reference User Guide	MAN 1671
Software Library User Guide	MAN 1880
Disk & Virtual Memory Operating System User Guide	MAN 1675
RTOS User Guide	MAN 1856
PRIME MAINTENANCE DATA SETS AND SPECIFICATIONS	
DSKTT1 (Diskette Test, Type 4300 Controller)	LST0772.002
Logic Diagrams for Type 4300 Diskette Controller	LDS 1810
Microcode Listing for Type 4300 Diskette Controller	MIC 1666
Microprogrammed Controller Specification	SPC 1409

The number of sectors per track, the sector addresses and the number of data words per sector vary among the three types of formats.

Prime Data Format

The Prime format has four sectors per track of 440 words each. These sectors are numbered one, seven, thirteen, and nineteen. Track zero is not used. Diskettes with this format may be created in two ways:

1. Run the MAKE program on an IBM Initialized diskette using either the Model 4300 controller (256 words of μ-code) or the Model 4301 controller (512 words of μ-code).

2. Create an equivalent to an IBM Initialized diskette from a blank or otherwise non-IBM Initialized diskette by using sense switch settings of the Test Program (DSKTT1) and the Model 4301 (512-word μ-code version); then run the MAKE program as above.

The Prime Data Format is the only diskette format that is supported with Prime standard software.

See the specifications below for more detailed information.

IBM Format

Both versions of the Diskette Option support IBM Formats and can produce IBM compatible diskettes. This format is not utilized by current software.

The IBM 3740 Diskette format is fairly complex and is described in great detail in the IBM and Shugart Associates publications. Basically, the format provides 26 sectors per track with 64 data words per sector. Track zero is used for control information, and tracks 74 through 76 are reserved as spare tracks in the case of permanent errors on other tracks.

IBM compatibility requires that an IBM Initialized Diskette be used and that data be written on tracks 1 through 76 only, maintaining the 64 word sectors.

To interchange data with IBM diskette systems, special attention must be paid to updating the diskette status information on track zero.

One may generate a diskette which is equivalent to an IBM Initialized Diskette using a Model 4301 (512-word μ-code) controller, by running a program to format the diskette. Note however, that special attention must be paid to track zero. See IBM document #GA 21-9190-1, File No. GENL-19 entitled IBM DISKETTE ORIGINAL EQUIPMENT MANUFACTURES INFORMATION for a detailed specification of the IBM format.

Other Formats

Users may define their own formats in either of two ways: 1) lengthening or shortening the sectors for which sector addresses are already prerecorded on a IBM Initialized Diskette (this can be done with either model of the controller), or 2) by using the Format command provided with the Model 4301 controller.

In the first case, the user must start a sector at a prerecorded sector address because the Model 4300 controller does not have the capability to create or alter the sector addresses. Thus, if fewer than 64 words per sector are required, the data is simply written using the Write command. Note however, that in this mode, there will never be more than 26 sectors per track.

If more than 64 words per sector are desired, the Write command with a larger range than 64 is specified. Now however, the sector or sectors (and the prerecorded sector addresses) following the one being written will be overwritten. Thus, fewer than 26 sectors will be available.

By using the Format command available with the Model 4301, the Format may be varied by rewriting the entire track including the sector addresses.

See Appendix B for a complete description of these modes of operation.

SPECIFICATIONS

The disk rotational speed is 360 RPM and the bit transfer rate is 249 kilobits/sec. The seek time is 10 n + 10 milliseconds (ms) where n is the number of tracks to go. The average rotational latency is 83 ms. Time to load the head is 50 ms. Other format performance specifications are summarized below:

	Prime	IBM	Other
Storage Capacity (16-bit words)	133.8K	123K	See Appendix E
Words per Disk	133.8K	123K	" " "
Words per Sector	440	64	" " "
Words per Track	1760	1664	" " "
Sectors per Drive	304	1924	" " "
Sectors per Track	4	26	" " "
Tracks per Drive available for data	76	74	77
Avg. Latency	87 ms	same	same
Track-to-Track Seek	20 ms	same	same

	Prime	IBM	Other
Avg. Seek	390 Ms	same	same
Max. Seek	770 Ms	"	"
Transfer Rate	250K bits/sec.	"	"
Drive Mounting	rack	"	"
IBM Disk Cartridge Equivalent	3740	"	"
Cartridge Loading	front	"	"

SYMBOLS AND ABBREVIATIONS

Number Representation:

100	100 decimal
'100	100 octal
$100	100 hexadecimal

SECTION 2

OPERATION

Common daily operating procedures for the diskette drives are summarized in this section for convenience. For other illustrations and complete details, refer to the vendor's device manuals listed in Section 1.

HANDLING DISKETTE

1. When the diskette is not in the drive, keep it in the outer envelope to protect all exposed magnetic surfaces. Replace storage envelopes when they become worn, cracked, or distorted.

2. Do not touch or attempt to clean any exposed magnetic (brown) surfaces when handling the diskette.

3. Do not flex, fold, bend, spindle, or otherwise distort the diskette. Mailing is hazardous, even with proper mailing containers.

4. Keep diskette away from heat, sunlight, magnetic fields, and ferromagnetic materials which might become magnetized. Do not, for instance, lay the diskette down near the head positioning mechanism of a large disk drive.

5. It is desirable to store the diskettes in the upright position.

6. Do not write on the plastic jacket with a lead pencil or ball-point pen. Use a felt tip pen. If labels are used, write on them before applying them to the diskette. Do not put labels over any of the exposed magnetic surfaces or holes in the diskette.

<u>Loading Diskette in Drive</u>:

1. Before inserting the diskette into the drive, make sure drive power is on so the spindle is rotating. (Drive power is turned on by the main power switch on the 19-inch chassis.)

2. To load the diskette, depress latch and insert the diskette with the label facing to the right, as shown in Figure 2-1. No damage will result if the diskette is inserted with the wrong orientation, but the drive will never go ready.

3. Be sure that the diskette is <u>fully</u> inserted into the drive before closing the door. This will prevent damaging the spindle hole. Move the latch handle to the left to lock diskette on drive spindle.

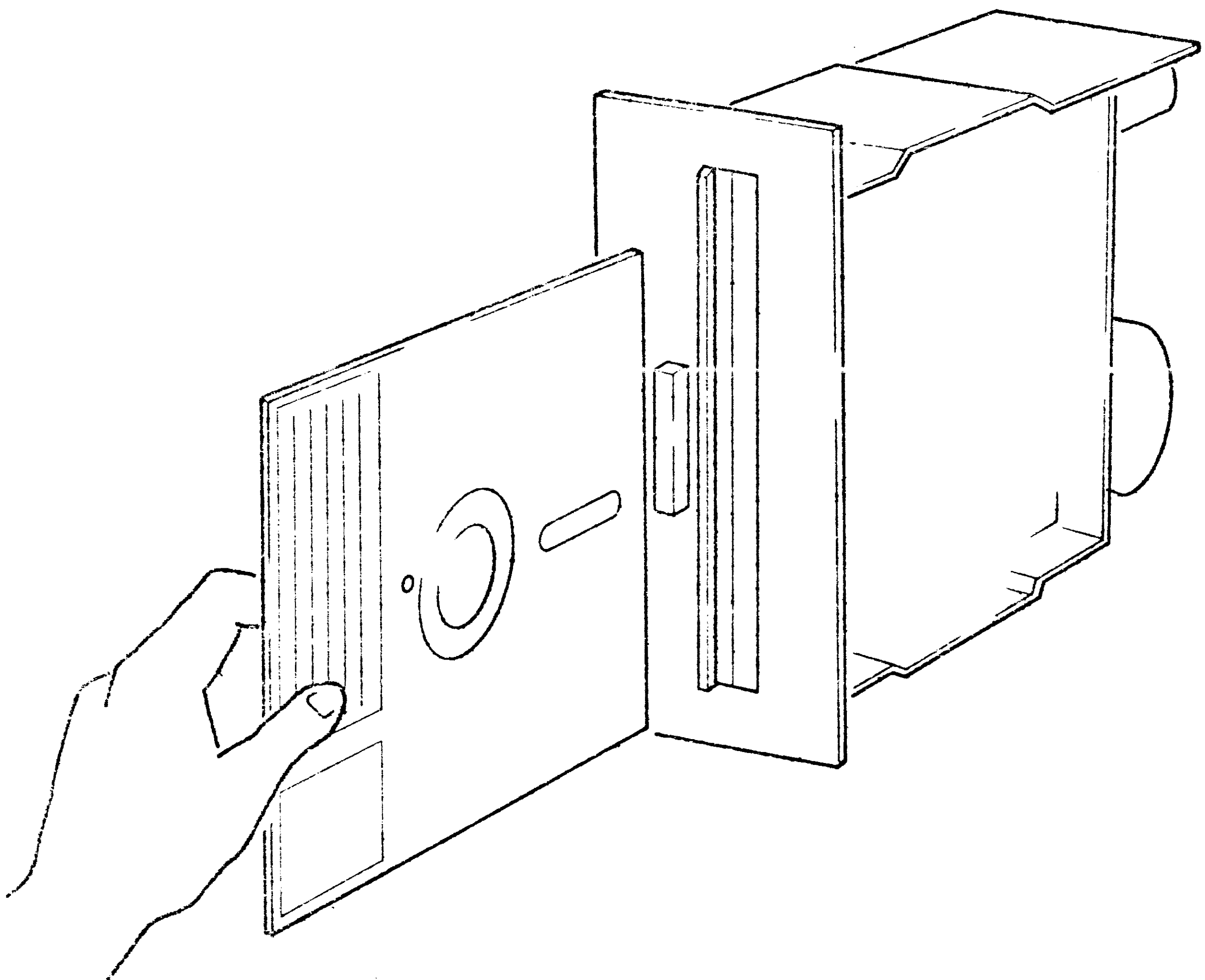


Figure 2-1. Loading Diskette in Drive

Write Protection: Prime diskettes may be write protected by punching a hole as shown in Figure 2-2. A standard hole punch may be used, but the official hole is smaller. When the hole is open, the diskette is protected; when covered, writing is allowed.

To override write protection, cover the hole with a tab of adhesive paper as shown in Figure 2-3. The paper must be opaque.

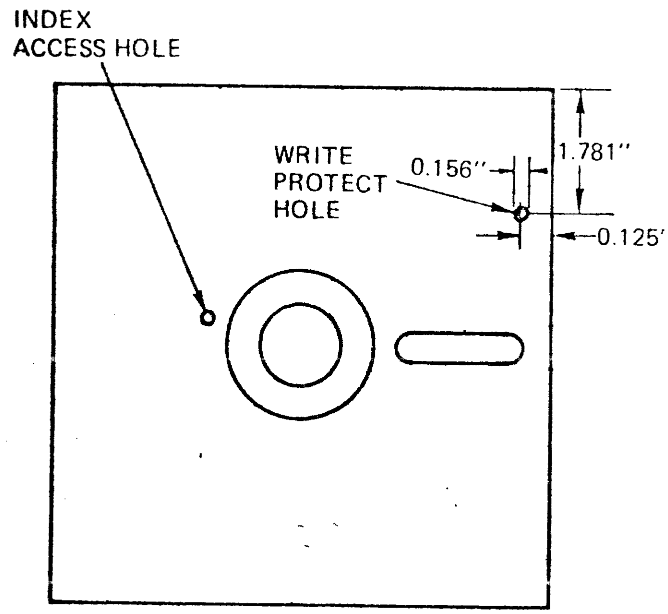


Figure 2-2. Write Protect Hole Specifications

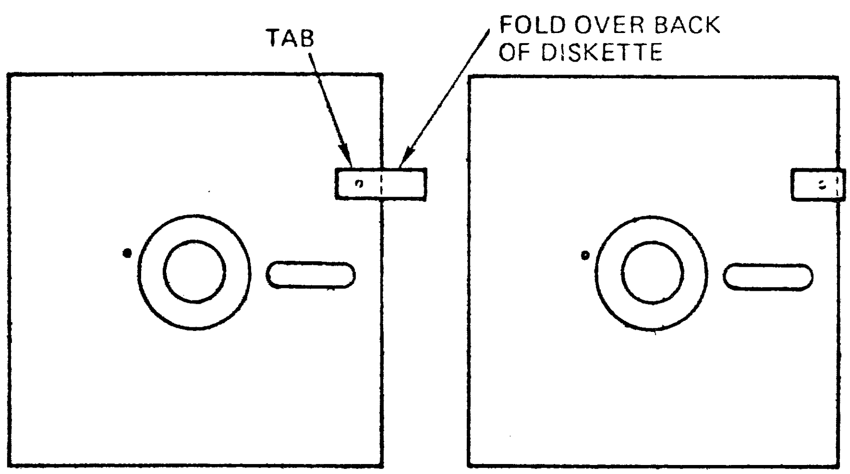


Figure 2-3. Disabling Write Protect Hole

SECTION 3

INSTALLATION AND CABLING

This section contains installation procedures for the Prime Diskette drive units.

INSTALLATION

Ordinarily, diskette drives are factory-installed and shipped in a standard Prime equipment cabinet. (See the Installation and Maintenance manual for standard configurations.) Factory-installed drives and associated power supplies are interconnected and ready to operate.

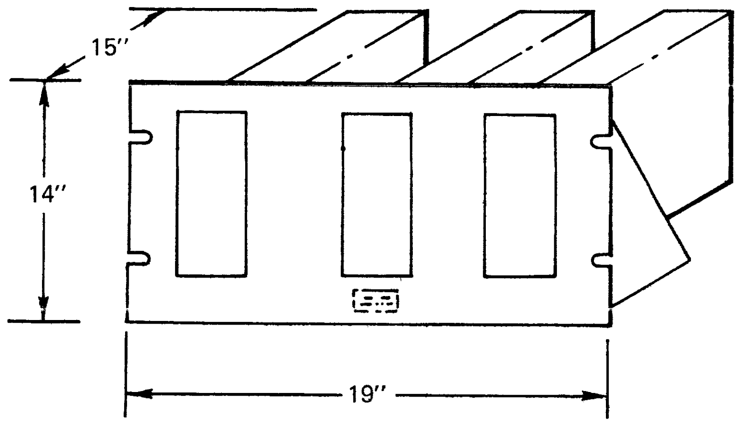
When diskette drives are shipped separately for installation by the user, the drive units are factory-mounted in a 19-inch panel assembly with main power switch. Up to three drives can be mounted on a single panel assembly. The power supply is mechanically separate and is intended to be mounted at the rear of a cabinet behind the diskette assembly for which it supplies ac and dc power. Figure 3-1 shows the dimensions of the diskette assembly and power supply. They may be mounted in any convenient way within reach of cable assemblies (described later).

Unpacking

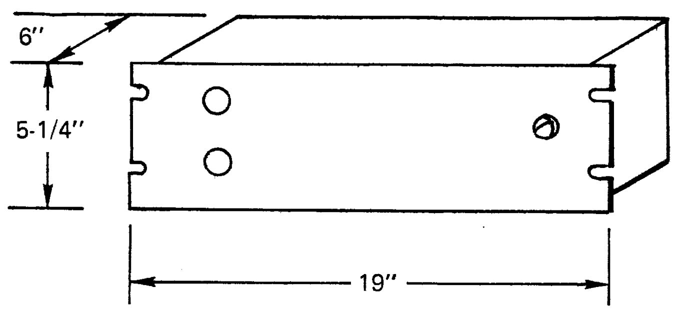
Diskette chassis assemblies and power supplies are shipped in standard domestic shipping containers. Cables are supplied disconnected in the same boxes. There are no special unpacking procedures. Observe any markings on the containers, start unpacking with the box right side up, and check packing materials for cables, mounting hardware, etc. If diskette drives are shipped separately, the heads may be secured or padded. Observe any packing instructions in the cartons.

CABLING

Cabling for a diskette assembly varies according to the number of drives supplied. Figure 3-2 shows the interconnections for a three-drive assembly. For one or two drives, omit the unnecessary cables. The AC power cable to the power supply is permanently attached to the chassis assembly at one end as is the main power cord. Figure 3-3 shows the locations of connectors at the rear of the each drive unit and on the power supply. All connectors are keyed except those to the unit selector switches. On the latter, make sure the two unused pins at one end of the cable connector are on top.

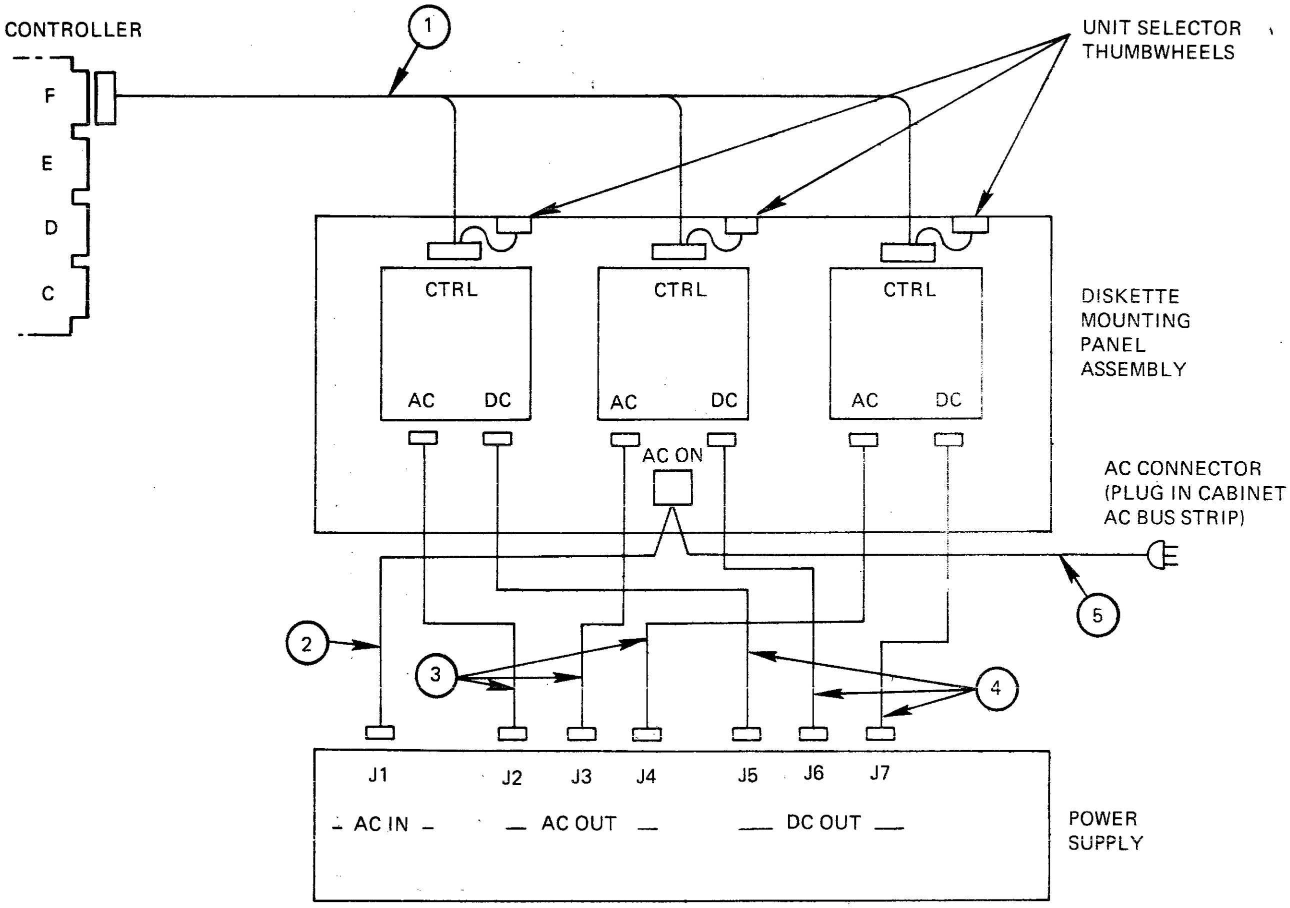


A. CHASSIS ASSEMBLY



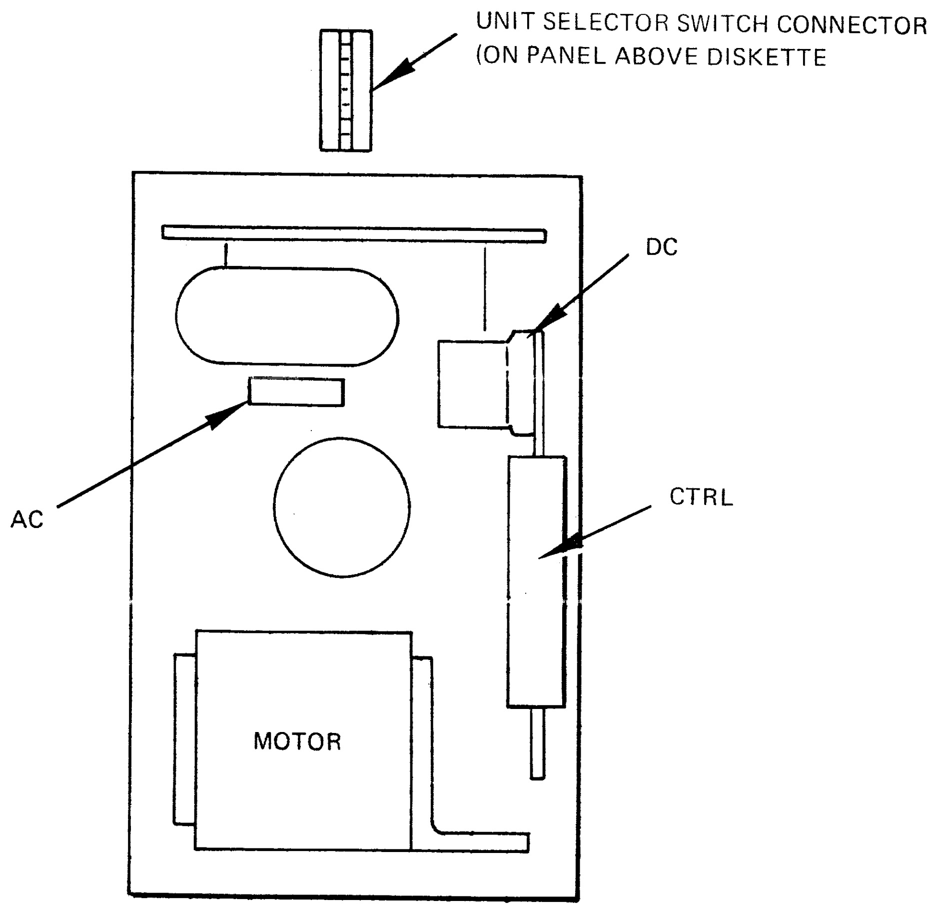
B. POWER SUPPLY

Figure 3-1. Diskette Chassis and Power Supply Dimensions

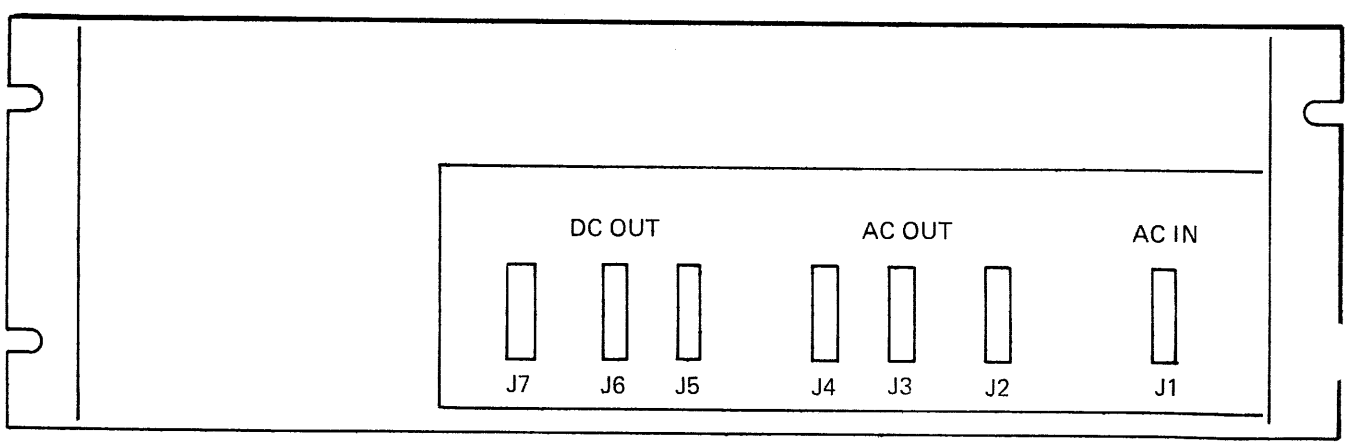


Item	Cable Complement	Length (Feet)
1	1 or 2 Diskette Drives: CBL1499-002 3 Diskette Drives: CBL1499-001	15 16
2	Power Switch Cable (Part of Diskette Panel Assembly)	3
3	AC Cables: CBL1437-001	3
4	DC Cables: CBL1438-001	3
5	Main Power Cable (Part of Diskette Panel Assembly)	6

Figure 3-2. Diskette Cabling



A. DISKETTE DRIVE UNIT



B. POWER SUPPLY

Figure 3-3. Diskette Drive Unit and Power Supply Connector Locations

SECTION 4

SYSTEM LEVEL PROGRAMMING

Standard Prime software that involves reading from or writing to the diskette is primarily file-oriented and is performed by the operating system (DOS, DOS/VM or RTOS). Complete information on the file system, file handling, and user calls to the disk-oriented features built into the operating system appears in Sections 2 and 5 of the DOS-DOS/VM User Guide.

FORTRAN formatted I/O to the diskette also assumes the presence of the operating system. Unit numbers 5 to 20 are directed to DOS file units and thus require operating system intervention to direct the read and write operations to the diskette controller.

Users requiring lower overhead and higher access speeds that can be provided by the DAM (Direct Access Method) file handling of DOS should investigate the Diskette resources of the Real Time Operating System. Section 5 contains assembly language programming information for the user who wishes to create custom drivers.

SECTION 5

ASSEMBLY LANGUAGE PROGRAMMING

CONTROLLER ORGANIZATION

The diskette controller is based on Prime's Microprogrammable Controller (MPC). The MPC is a microprogrammed peripheral interface with general-purpose registers, input/output device logic, and control timing features. In the Type 4300 controller, the general-purpose features are adapted to the specific control and data transfer needs of the Diskette drive units. Internal controller operations such as Seek, Read and Write are controlled by execution of a series of microprogrammed instructions encoded in the controllers Programmable Read-Only Memory (PROM). Such operations are initiated under CPU program control by programmed I/O instructions (OTA's, etc.). The assigned instructions are defined in this section. See Appendix D for a summary of all PIO instructions.

Register File

The controller includes a 32-byte register file for use as scratch locations by the microprogram. During operation, these are normally invisible to the CPU program. However, any pair of bytes may be read by an INA instruction to determine controller status or to input diagnostic information. Register file functions are summarized in Appendix C.

Interrupts

The controller requests an interrupt on completion of the operation initiated by any of the following commands:

OTA '00	Step Negative
'01	Step Positive
'03	Read
'04	Write
'05	Verify *
'07	Format *
'10	Locate

The request is cleared by OCP '14, OCP '17 or a master clear.

* Model 4301 only.

Controller Status

Register File Byte 2 contains the controller status, as follows:

Bit 1 Normal End of Instruction

2 Sector Not Found (read 28 ID's)

3 CRC Error in Sector ID

4a Track Number Error on Read, Write or Verify or

b Header Bytes not zero (a'la IBM) (512 word μ-code only) or

c Positioned on Track zero after an OTA 00 (step Neg)

5a Wrong OTA Code (512 word μ-code only)

b Device Not Ready

6 Deleted Data Mark Detected on Read

7a Data Overrun Error or

b Format is too many words

8a CRC Check Error in Data Field of a Read or Verify or

b File inoperable on Write or Format

c Write Protect during Write or Format

See Appendix A for expected status word values resulting from various controller operations.

Head Loading

The head is loaded under program control because the head should remain unloaded when reading or writing is not taking place. To save wear on the head and diskette, the head is unloaded by the controller automatically after 6 seconds if no accesses have been made. The controller only goes ready when the head is loaded. Thus, to find out if the device is ready, issue OTA select, OTA INA setup (status), INA00. If the Not Ready Status bit is a zero (i.e., bit 5 is not set), a diskette is in the selected device and it is up to speed with the head loaded and ready to be used.

Device Address

The standard controller device address is '12. (Only the function codes are specified in the following PIO instruction descriptions.)

PIO INSTRUCTIONS

OTA '00 Step Negative

Causes the controller to move the head one track toward the outside of the disk (toward Track 00). If the head is already positioned on Track 00, the head remains there and a status bit is set. An interrupt is generated at the completion of this command (after the head has moved).

A Register

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

When the controller interrupts, the controller is ready to receive the next command. No additional delays are required. These are taken care of by the controller. SKS '01 (Not Busy) should precede this OTA, because the Ready condition for this OTA does not include Busy.

<u>OTA '01</u> <u>Step Positive</u>

Causes the controller to move the head one track toward the inside of the disk (away from Track 00). An interrupt is generated at the completion of this command (after the head has moved). Attempts to step further than track 76 (77th track) should be avoided. If the head is positioned on a track greater than 76, no data is read and the μ-code hangs up. OCP initialize or Master Clear must then be given to clear this condition.

A Register

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

<u>OTA '02</u> <u>Select Device</u>

Steers the signals to/from the proper device. It must precede every Step, Read, Write, Verify or Format command if the device is to be different from the device used by the previous command. This command deselects and lifts the head of the previously selected device, and loads the head on the selected device.

The device number is bit encoded. Bit 9 is device one and bit 16 is device eight. Only one bit should be set. All zeroes will deselect all devices.

A Register

MBZ								1 - - - -Device- - - - - - - 8							
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

OTA '03 Read

Causes the controller to read the specified sector and track of the selected device. Reading continues until the end of range of the last channel (when chaining). The amount of data read must be exactly equal to the amount of data written in that sector or a check error will occur. Gather reads are allowed (up to seven) within the sector. Only one sector may be read. An interrupt is generated at the end of the instruction. The heads must be positioned prior to this command. A status error is generated if a read is attempted on the wrong track, i.e., one whose Sector ID does not agree with the command word.

A Register

Track No.								Sector No.							
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

A check error occurs if the number of words read differs from the number previously recorded.

OTA '04 Write

Causes the device to write the specified sector and track. Writing continues until the end of range of the last channel (chaining). A minimum range of two words must be written or chained. Scatter writes are allowed within the sector. An interrupt is generated at the end of the instruction. The heads must be positioned prior to this command. An error status will be generated if a write is attempted on the wrong track. The software must write the proper length sector as other sectors may be overwritten if the DMX range is too long. Specifically, a write sequence begins by the controller reading the Sector ID on the current track. When the sector number in the Sector ID matches the sector number in the command word (and the rest of the Sector ID information is deemed correct) writing begins in the gap following the sector ID.

A Register

Track No.								Sector No.							
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Data is written until the end of range and an end of chain (up to seven) are detected. The controller then writes the CRC and a final gap, terminates the command, and generates an interrupt request.

When done, the controller has overwritten an area of the disk following the Sector ID that is as large as required by the data and gaps. If another sector ID is overwritten, that sector is essentially destroyed. As an example, if sector one was originally 64 words and 65 words of data are written into sector one, sector two cannot be guaranteed to be available for reading or writing. Appendix B describes how this feature can be useful in generating a custom diskette format.

OTA '05 Verify (Optional)

Causes the device to read data from the specified sector and track, and from the CPU main memory and compare them bit for bit. The range(s) (chaining is allowed up to seven) of the output DMX transfer must be equal to the length of the data in the addressed sector. An error is generated if the sectors are not equal or if the head is not positioned on the correct track. The controller terminates the transfer immediately upon detecting an error. Thus, the DMX range indicates where the error occurred.

A Register

Track No.								Sector No.							
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

OTA '06 INA Setup

Selects the first of two register file locations to be read when the controller performs the next INA '00. This command must be issued prior to each INA because the controller will not respond ready to INA '00 unless OTA '06 precedes it.

A Register

											Reg. File Byte				
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

OTA '07 Format (Optional)

Causes the selected drive to write an entire track (wherever the heads are positioned) including all of the gaps and Sector ID's. The track is written in the format specified by the A register:

A Register

Track No.								No. of Sectors Per Track							
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

The DMX range specifies the number of words per sector. The DMX range and address must be set up after each sector. The entire track is overwritten in an IBM-like format. If the number of sectors is specified to be 26, the range of each sector is 64 words, and the data written is 64 words of $E5E5, then the track will look like an IBM initialized track (for tracks 01 through 76). Track 00 has other data but the same number of sectors and words per sector.

The sector numbers are written in the Sector ID's starting with 1, incrementing in each successive Sector ID, and ending with the sector number specified by the command. The specified track number will also be written in each Sector ID. For additional details, see Appendix B.

OTA '10 Locate

Causes the device to read the 'next address' header of the device currently selected on the track where the head is currently positioned. The current Device Number, Track Number and Sector Number are stored in the register file of the controller. (See Appendix C). The controller then goes 'not busy'. The information may be read by an INA '00 following an OTA '06.

A Register

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTA '14 DMA/C Channel

This OTA causes the controller to store the DMA/C channel number to be used for subsequent data transfers.

A Register

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Chain No.				C/A	Channel No.										

Bit 5: 1=DMC, 0=DMA

OTA '15 Micro-Verify (Optional)

Causes the micro-code to execute a fixed program which loads registers and checks data paths and operations within the controller. The controller becomes busy upon the receipt of this command and stays busy during its execution.

If no error is detected, a $80 or $88 is loaded into the status register and an interrupt request is generated. If an error is detected but the basic ROM control unit is functioning, a $77 is placed in the status register and an interrupt request is generated.

OTA '16 Interrupt Vector

This OTA transfers an interrupt vector to be used for subsequent interrupts:

A Register

Zeroes			Interrupt Vector												
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

OTA '17 Write Deleted Data Mark

Identical to OTA Write except that an IBM deleted data mark is written prior to the data field.

INA '00 Input Register File

Reads the contents of two adjacent register file locations. The byte specified by OTA '06 is the least significant byte and the next register file location is the most significant byte. See Appendix C for the register file contents.

SKS '00 Skip if INA 00 Ready

SKS '01 Skip if Not Busy

SKS '02 Skip if Format Sector Complete

SKS '04 Skip if Not Interrupting

OCP '15 Set Interrupt Mask

OCP '16 Clear Interrupt Mask

OCP '17 Initialize
(SKS Not Busy should precede this OCP)

PROGRAMMING EXAMPLE

The following key-in program example initializes the controller and reads sector 1 of track 1 of an IBM initialized diskette on device 1. It may be converted to write by changing location RW to a write command (OTA '0412). The program waits for the operation - complete interrupt and then displays the contents of any pair of register file locations selected by the sense switches. This feature may be used to display controller status or examine other register file locations for diagnostic purposes. To run the program, master clear, turn to RUN and press START. This example is a skeleton routine to demonstrate some major diskette functions; it is not intended as a model of preferred programming techniques.

```
                    (0001) *SAMPLE KEY-IN PROGRAM TO READ OR WRITE ONE DISKETTE SECTOR
                    (0002) *
            001000  (0003)          ORG     '1000
001000:     031712  (0004) START    OCP     '1712          INITIALIZE CONTROLLER
                    (0005) *   SET UP FOR END-OF-OPERATION INTERRUPT
001001: 02.001076A  (0006)          LDA     INTVEC
001002:     171612  (0007)          OTA     '1612
001003: 01.001002A  (0008)          JMP     *-1
001004: 02.001101A  (0009)          LDA     INTRPT
001005: 44.001076A  (0010)          STA*    INTVEC
001006:     000417  (0011)          EVIM
001007:     000401  (0012)          ENB
                    (0013) *   SELECT DEVICE
001010: 02.001100A  (0014)          LDA     DEVICE
001011:     170212  (0015)          OTA     '0212
001012: 01.001011A  (0016)          JMP     *-1
                    (0017) *   SET UP DMA CHANNEL
001013: 02.001077A  (0018)          LDA     DMASET
001014:     171412  (0019)          OTA     '1412
001015: 01.001014A  (0020)          JMP     *-1
001016: 02.001103A  (0021)          LDA     END            MEMORY BLOCK FOLLOWS PROGRAM
001017: 04.000021A  (0022)          STA     '21
001020: 02.001074A  (0023)          LDA     SECSIZ
001021: 04.000020A  (0024)          STA     '20
                    (0025) *   SEEK TO TRACK 1 (INTERRUPTS MASKED OFF)
001022:     140040  (0026)          CRA
001023:     070112  (0027) SEEK     SKS     '0112          CHECK IF CONTROLLER BUSY
001024: 01.001023A  (0028)          JMP     *-1
001025:     170012  (0029)          OTA     '0012          STEP NEGATIVE
001026: 01.001025A  (0030)          JMP     *-1
001027: 10.001063A  (0031)          JST     STAT
001030:     101263  (0032)          SAS     4              CHECK IF ON TRACK 0
001031: 01.001023A  (0033)          JMP     SEEK           NO
001032:     170112  (0034)          OTA     '0112          YES - STEP TO TRACK 1
001033: 01.001032A  (0035)          JMP     *-1
                    (0036)          EJCT
                    (0037) *   SET UP AND EXECUTE THE READ OR WRITE
001034: 10.001063A  (0038)          JST     STAT
001035:     100264  (0039)          SAR     5              MAKE SURE DEVICE IS READY
001036: 01.001034A  (0040)          JMP     *-2
001037: 02.001075A  (0041)          LDA     TRKSEC         SET UP TO EXECUTE THE READ OR WRITE
001040:     031412  (0042)          OCP     '1412          ACKNOWLEDGE ANY PENDING INTERRUPTS
001041:     031512  (0043)          OCP     '1512          MASK INTERRUPT ON
001042:     170312  (0044) RW       OTA     '0312          CHANGE TO OTA '0412 TO WRITE
001043: 01.001042A  (0045)          JMP     *-1
001044:     000001  (0046)          NOP
001045: 01.001044A  (0047)          JMP     *-1            WAIT FOR OPERATION COMPLETE INTERRUPT
                    (0048) *   END-OF-OPERATION INTERRUPT PROCESSOR. DISPLAYS CONTROLLER
                    (0049) *   REGISTER FILE LOCATION SELECTED BY SS11-16. SET SS16
                    (0050) *   TO DISPLAY STATUS.
001046:     000000  (0051) DISPL    BSZ     1
001047:     131620  (0052)          INA     '1620
001050: 03.001102A  (0053)          ANA     ='77
001051:     170612  (0054)          OTA     '0612
001052: 01.001051A  (0055)          JMP     *-1
001053:     070112  (0056)          SKS     '0112
001054: 01.001053A  (0057)          JMP     *-1
001055:     130012  (0058)          INA     '0012
001056: 01.001055A  (0059)          JMP     *-1
001057:     070112  (0060)          SKS     '0112
001060: 01.001057A  (0061)          JMP     *-1
001061:     171720  (0062)          OTA     '1720
001062: 01.001047A  (0063)          JMP     DISPL+1
                    (0064) *   STATUS SUBROUTINE
001063:     000000  (0065) STAT     BSZ     1
001064:     140040  (0066)          CRA                    SETUP TO INPUT STATUS BITS IN LEFT BYTE
001065:     141206  (0067)          A1A
001066:     170612  (0068)          OTA     '0612          SET UP TO INPUT STATUS WORD
001067: 01.001066A  (0069)          JMP     *-1
001070:     140040  (0070)          CRA
001071:     130012  (0071)          INA     '0012          GET THE STATUS WORD
001072: 01.001071A  (0072)          JMP     *-1
001073: 41.001063A  (0073)          JMP*    STAT
                    (0074)          EJCT
001074:     176000  (0075) SECSIZ   DATA    -64.LS.4       WORDS PER SECTOR (2'S COMP, LEFT JUSTIFIED)
001075:     000401  (0076) TRKSEC   OCT     401            SETUP WORD FOR TRACK 1 SECTOR 1
001076:     000101  (0077) INTVEC   OCT     101            INTERRUPT VECTOR
001077:     000020  (0078) DMASET   OCT     20             SELECT DMA (CHANNEL 20)
001100:     000200  (0079) DEVICE   OCT     200            DEVICE NUMBER (BIT 9 = DEVICE 1)
001101: 00.001046A  (0080) INTRPT   DAC     DISPL
001102: 00.000077A  (0081)          FIN

001103: 00.001104A  (0082) END      DAC     *+1
            001104  (0083)          END


DEVICE      001100A 0014   0079
DISPL       001046A 0051   0063   0080
DMASET      001077A 0018   0078
END         001103A 0021   0082
INTRPT      001101A 0009   0080
INTVEC      001076A 0006   0010   0077
RW          001042A 0044
SECSIZ      001074A 0023   0075
SEEK        001023A 0027   0033
START       001000A 0004
STAT        001063A 0031   0038   0065   0073
TRKSEC      001075A 0041   0076

0000 ERRORS (PMA-1090.016)
```

SECTION 6

TEST AND MAINTENANCE

TEST AND VERIFICATION

Prime supplies a standard test and verification program for factory and on-site checkout of this controller. The test is supplied in the T & M UFD of master disk Volume 1 or on paper tape:

Filename in T & M UFD	Paper Tape	Low	High	Start
DSKTT1	SLT0772.001	'66	'11777	'1000

The test assumes the presence of two diskette drives identified as devices 1 and 2. (The selector switches should be set to 1 and 2 accordingly.) Unit numbers and other test parameters can be altered by patching locations within the test as described in the listing.

The diskettes mounted in the drives should be Prime supplied, IBM initialized, Shugart SA100, or equivalent, without write protection. A diskette that has been reformatted in non-IBM format or run under DOS will not run the test program. A disk that is in IBM format but that does not contain IBM initialized data ($E5E5) may be reformatted by running the test with sense switch 5 up. A disk that is not in IBM format may also be completely reformatted by running the test with sense switches 5 and 10 up, provided the 4301 option is present.

CAUTION

> Always stop a write or format command by putting sense switch 8 up to stop on end of pass.

Make sense switch settings before starting the test. The default value is all switches reset; see the listing for the special options that can be selected by sense switches.

PREVENTIVE MAINTENANCE

Weekly

Run the Test and Verification Program (DSKTT1).

Yearly

Perform the diskette drive unit preventive maintenance described in the vendor's maintenance manual.

APPENDIX A

INTERPRETING STATUS WORDS

Tables A-1 and A-2 show the expected, error and illegal (not implemented) status bits for each instruction for both versions of the μ-code. Status is not returned except by those commands resulting in an interrupt at their completion. Thus, OTA Select, INA Setup DMX Channel, and Interrupt do not return status or cause an interrupt. Also note that undefined commands are not detected (OTA's 5, 7, 11, 12, 13 and 15) in the 256 word version. Thus $80 is the expected status from Step, Read, Write and Locate commands. This is also the expected status after a Verify or Format command in the 512 word μ-code.

1. The contents of RF 31 is 00XXXXXX in the case of the 256 word μ-code and 01XXXXXX in the case of the 512 word version, where XXXXXX represents the Rev number of the μ-code.

2. The status one receives after executing an OTA 05 or OTA 07 will be indeterminate in the case of the small version and normally $80 in the case of the 512 word version.

3. The status one receives after issuing OTA 11, 12, 13, 15 or 17 is indeterminate with the small μ-code but gives a $20 status in the case of the large μ-code.

If a deleted Data Mark is detected on a Read or Verify, the deleted Data Mark status bit will be set and the command will proceed normally.

Table A-1. Status Expectancy, 256 Word μ-Code

OTA Command / Status		SN 0	SP 1	SEL 2	R 3	W 4	U 5	INA 6	U 7	L 10	U 11	U 12	U 13	D 14	U 15	I 16	U 17
Normal	1	C	N	N	N	N	U	X	U	N	U	U	U	X	U	X	U
Sector Not Found	2	X	X	X	E	E	U	X	U	X	U	U	U	X	U	X	U
CRC in Ed	3	X	X	X	E	E	U	X	U	E	U	U	U	X	U	X	U
Trk # or T.Zero	4	C	X	X	E	E	U	X	U	X	U	U	U	X	U	X	U
Dev. No Rdy	5	E	E	E	E	E	U	X	U	E	U	U	U	X	U	X	U
Del. Data Mk	6	X	X	X	E	X	U	X	U	X	U	U	U	X	U	X	U
Data Ovrn	7	X	X	X	E	E	U	X	U	X	U	U	U	X	U	X	U
CRC or File Inop or W. Protect	8	X	X	X	E	C	U	X	U	X	U	U	U	X	U	X	U

Table A-2. Status Expectancy, 512 word μ-Code

OTA Command / Status		SN 0	SP 1	SEL 2	R 3	W 4	V 5	INA 6	F 7	L 10	U 11	U 12	U 13	D 14	MV 15	I 16	U 17
Normal	1	-	-	-	-	-	N	-	N	-	X	X	X	-	N	-	X
Sector Not F.	2	-	-	-	-	-	E	-	X	-	X	X	X	-	E	-	X
CRC in Ed	3	-	-	-	-	-	E	-	E	-	X	X	X	-	E	-	X
Trk # or T.Zero	4	-	-	-	-	-	E	-	E	-	X	X	X	-	E	-	X
Dev. Not Rdy	5	-	-	-	-	-	E	-	E	-	N	N	N	-	N	-	N
Del. Data Mk	6	-	-	-	-	-	E	-	E	-	X	X	X	-	E	-	X
Data Ovrn	7	-	-	-	-	-	E	-	E	-	X	X	X	-	E	-	X
CRC or File Inop or W. Protect	8	-	-	-	-	-	E	-	E	-	X	X	X	-	E	-	X

Legend

N = Normal Status (OK)

E = Error Status

C = Normal or Error Conditional on expected result

R = Should be zero range is equal to sector length
Should be one range is not equal to sector length

X = Undefined cannot occur without hardware or firmware failure

\- = Same as 256 word μ-code

U = Undefined

APPENDIX B

DETAILED PROGRAMMING RECOMMENDATIONS

USING VARIABLE SECTOR LENGTHS

Assume a user wants to define his own diskette record format, for example, four 512 word sectors per track. A 512 word sector could be written in sectors one, seven, thirteen and nineteen. All intermediate sectors will be overwritten. However, sectors twenty-five and twenty-six would still be available as sixty-four word sectors. When reading or rewriting these newly written sectors, one can specify the actual sector number (i.e., one, seven, thirteen, nineteen, twenty-five or twenty-six in this example). This process, of course, could be repeated whenever going from a given number of sectors to the same number or a fewer number. The salient point is that the Sector ID's are read during a write command but may be overwritten by a write of a previous sector.

Note that this process is performed using the Write command. The Format command does not read any Sector ID's and rewrites the entire track including the Sector ID's.

Also note that part of the gap in each sector that is Formatted (or Initialized in IBM parlance) is to allow for speed tolerances (.05 X number of words in the sector). An initialized diskette thus has 6.5 bytes (5%) in each sector gap for speed tolerance. If one was to rewrite a track, as in the example above, one would have to ensure that 51.2 (52) bytes are allowed per 512 word sector. Since this conglomerate sector spans the ID's, gaps, and Data fields of six 64 word sectors, there are not enough bits in the gaps allowed for speed tolerance. The controller writes the proper number of bits for 64 word sectors. One has to allow enough for these speed variations when writing longer sectors to accomodate this. Thus, one must use the gap formulae shown below to determine the proper mapping of new into old sectors.

Number of data words in an Initialized Sector

= 128 bytes

Number of gap bytes following the data and CRC in an Initialized Sector

= 33 bytes

Number of gap bytes following the data and CRC in an arbitrary sector must be

$$= 26.5 + \frac{\text{(number of data bytes)}}{20}$$

These extra gap bytes must be allowed for by writing shorter sectors.

As an example, if one wished to write four sectors per track in sectors one, seven, thirteen, and nineteen, each IBM sector has the bytes as shown below:

7	bytes ID
17	bytes Gap 2
1	byte Data Mark
128	bytes Data
2	bytes CRC
26.5	bytes End gap
6.5	bytes Speed tolerance gap
188	bytes Total per sector

or 128 bytes Data per sector
or 60 bytes Overhead per IBM sector
or 53.5 bytes Plus speed tolerance gap per sector of overhead

Thus, between sectors one and seven there were 188 X 6 = 1128 bytes of gap and data. The overhead required for the new larger 'sector one' is 53.5 bytes plus speed tolerance gap. Therefore, the amount of data that can be written in the new sector is determined as follows:

1128 - 53.5 = 1.05 X (number of data bytes)

Number of bytes = 1023

Number of words = 511

By setting the range equal to 511 and writing a 'sector one', the controller then writes a 511 word record and appends the correct CRC character. There will be enough bits following the CRC to guarantee that if the diskette drive meets the IBM speed tolerance spec of ± 2.4%, that no matter how many times the record is rewritten, the subsequent sector header (sector seven in this example) will never be overwritten. The speed tolerance of the drive is less than ±2.4%, so a slight increase in storage capacity can be allowed (i.e., 512 words can be recorded safely).

USING THE FORMAT COMMAND

The following detailed provisions apply to the optional FORMAT command (OTA '07):

1. The data range of each sector must be exact. That is, the check word will be written upon detection of end of range and end of chain (up to seven), and the next sector will begin. The minimum sector length is two words. The minimum DMX range allowed is also two.

2. Gather read is allowed within a sector, but each sector will chain the same way, i.e., the Chain number will be the same for each sector because of item 8.

3. The track number written in each Sector ID is what is transmitted to the controller during this OTA. No check is made by the controller to see if the heads are truly positioned on that track.

4. Data sectors of any length may be formatted (variable from sector to sector), but only one length will be IBM compatible., i.e., 64 words/sector, 26 sectors/track.

5. If the sectors are not 64 words long, then the data field of the sectors must have sufficient space for speed changes in them. This requires that during a Format, the data range of each sector be increased by .05 times the number of data words over 64. That is, the data buffer must be longer than the data to be written by

$$\frac{(\text{Number of words in the sector - 64})}{20} \text{words}$$

Later the sector must be rewritten to correct the length of the sector before it can be read correctly.

As an example, if one wishes to Format a track with four sectors, the equation below says that

$$4 = \frac{4888}{1.05B + 53}$$

$$\text{or} \quad B = 556 \text{ words per sector}$$

Thus 556 words of data may be put in each sector. However, the sectors written must be longer to provide for the speed variation. Each sector must be

$$\frac{556 - 64}{20} = 25$$

words longer. Thus, the range must be 581 words for each sector during the format. After the track is formatted, the CRC word will occur after 581 words of data. If the sectors are all then rewritten with a range of 556, the data will contain 556 words and the CRC will be written following the data. The sectors may then be treated as 556 word sectors from then on.

If this speed tolerance gap (of 25 words in the above example) were not provided, succeeding write operations may write over the next sector header.

If the sector is not rewritten (with a range of 556 in the above example) an attempt to read a record with the correct range (556 in the above example) would give a CRC error because the CRC character would be mispositioned (after 581 words in the above example). The sector could of course be read correctly as a 581-word sector.

Appendix E summarizes the above calculations for from 1 to 32 equal length sectors per track.

The relevant equations are:

$$Sf = \frac{4888}{B + 53.5} \qquad S = \frac{4888}{1.05B + 53.5}$$

where: Sf is the number of sectors of equal length during a Format
S is the number of sectors of equal length during a write.

B is the number of bytes of data per sector and that the controller writes 6.5 bytes of speed gap.

6. Data may be written in the sector from memory during a Format command.

7. After a sector has been written, this SKS flag '02 will be set so that the DMX Range and Address may be reset up. The SKS '02 will be set prior to the first sector. The SKS will skip for approximately 1 ms between each sector. The SKS will also skip following the last sector.

8. OTA '16 will only be accepted before the OTA '07. Thus, the DMX setup word (channel no., chain no. and DMA/C) will be the same for each sector on a given track.

ERROR HANDLING

Incorrect operating procedures, faulty programming, damaged diskettes, and "soft errors" created by airborne contaminants, random electrical noise, and other external causes can produce errors falsely attributed to drive failure or misadjustment.

Unless visual inspection of the drive discloses an obvious misalignment or broken part, attempt to repeat the fault with the original diskette, then attempt to duplicate fault on second diskette.

"Soft Error" Detection and Correction

Soft errors are usually caused by:

1. Airborne contaminants that pass between the read/write head and the disk. Usually these contaminants can be removed by the cartridge self-cleaning wiper.

2. Random electrical noise that usually lasts for a few microseconds.

3. Small defects in the written data and/or track not detected during the write operation that may cause a soft error during a read.

The following procedures are recommended to recover from the above mentioned soft errors:

1. Reread the track ten times or until such time as the data is recovered.

2. If data is not recovered after using step 1, access the head to the adjacent track in the same direction previously moved, then return to the desired track.

3. Repeat step 1.

4. If data is not recovered, the error is not recoverable.

Write Errors

If an error occurs during a write operation, it will be detected on the next revolution by doing a read or verify (optional) operation, commonly called a "write check". To correct the error, another write and verify operation must be done. If the write operation is not successful after ten (10) attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error still persists, the diskette should be swapped and the above procedure repeated. If the failure still exists, consider the drive defective. If the failure disappears, consider the original diskette defective and discard it.

One must take care not to initiate an operation which changes the Address Register, Data Register, or Mode Registers prior to the conclusion of their previous use. For instance, if DMX operation is initiated before a previously requested interrupt is processed, the interrupt vector will be lost.

APPENDIX C

REGISTER FILE CONTENTS

Abbreviations:

I = INA setup
S = Step
R = Read
W = Write
V = Verify
F = Format
L = Locate
MS = Most Significant
LS = Least Significant
WE = Write Deleted Data Mark

Table C-1. Register Files Accessible to Program

Register File	Description	Command
0	Data Right 9=16 LS DM Left and Right with clock IM, AM Left and Right with clock	R,W,V,F F,W F
1	Data Left 1-8 MS	R,W,V,F
2	Status Byte 1	All
3	Chain No.	R,W,V
4	Number of sector mark read looking for ID minus 53	R,W,V
5	CRCLS Being Calculated (1-8 IBM) LS	R,W,V,F
6	CRCMS Being Calculated (9-16 IBM) MS	R,W,V,F
7	Last ID Byte 12, 14 ID RF Limit N° (13) Bit count #F7	F R,W,V W
8	Sector ID Track Address Read Sector ID Track Address Written	R,W,V,L F R
9	Sector ID Zero (IBM) Read Sector ID Zero (IBM) Written	R,W,V,L F

Table C-1 (Cont)

Register File	Description	Command
10 $0A	Sector ID Sector Number Read Sector ID Sector Number Written	R,W.V,L F
11 $0B	Sector ID Zero (IBM) Read Sector ID Zero (IBM) Written	R,W,V F
12 $0C	Sector ID CRC Read LS Sector ID CRC Calculated	R,W,V F
13 $0D	Sector ID CRC Read MS Sector ID CRC Read Calculated	R,W,V F
14 $0E	DMA Channel # Right (LS) Initial	R,W,V,F
15 $0F	DMA Channel # Left (MS) Initial	R,W,V,F
16 $10	Interrupt Vector Right (LS)	R,W,V,L,F,S
17 $11	Interrupt Vector Left (MS)	R,W,V,L,F,S
18 $12	Current Output Byte Copy (to device)	All
19 $13	Current Device N° (to device)	All
20 $14	Data Mark ($01) on ID Read Data Mark ($01) on Data Read Data Mark ($80) in Data	R,W,V,L R,V W,F
21 $15	Delay Constant MS	All
22 $16	Delay Constant mid	All
23 $17	Delay Constant LS	All
24 $18	Temp Storage of F1 and W Protect Bits Data Bit Written Data Bit Read Track Zero Detect Mark $10	W,F W,F

Table C-1. (Cont)

Register File		Description	Command
25	$19	Track N° from OTA (A Reg Left Byte)	R,W,F,S,F All
26	$1A	Sector N° from OTA (A Reg Right Byte) Number of Sectors to be Formatted RF N° to be INA'd	R,W,V F INA
27		Const ($77) Turn Off Write Bit and Clear File Inoperable Reset (FIR) Device Ready Bit Const ($10) Input Mode Bit	W,F All I R
28	$1C	Command Switch ID Read & Format/W R = 1 W = 2 V = 3 F = $0C L = 0 WD = 2	R,W,F,L,F
29	$ID	Bit 15 Mark ($FD)	W,F
30	$IE	SKS Mark ($20) (DF) SKS Sector Done	F
31	$IF	μ-code Type and Rev # 8 7 6 1 Type Rev	All

Table C-2. Register Files Not Accessible to Program

Notes:

S = Step
R = Read
W = Write
V = Verify
F = Format

DR #	Description	Command
DR1	Chain # Copy	F
DR2	Temp Storage of RF# Written in Id Temp Storage of Mark Temp Storage of DRL (data left) Temp Storage of CRC	F W,F R W
DR3	Temp Storage of RF 28 (ID Search) Temp Storage of RF 27 Temp Storage of CRC	R,W,V INA Set W
DR4	Data Char Sector Limit Check	R,W,V,F F
DR5	Device Select	All
DR6	Output Byte to Device	All
DR7	Counter and RF Address	All
DB7		
DB8	Input Byte	All

Output Byte in MPC
(Byte 6)

	Bit	Function
MS	1	Write Data
	2	Erase Gate
	3	Write Gate
	4	Write Current Switch
	5	File Inop Reset
	6	Direction Select
	7	Step
LS	8	*

Input Byte in MPC
(Byte 8)

	Bit	Function
MS	1	Index
	2	Read Clock
	3	Read Data
	4	Track Zero
	5	Ready (?)
	6	File Protect
	7	File Inop
LS	8	**

* read clock on cable
** index on cable

APPENDIX D

PRIME DISKETTE COMMAND SUMMARY

Device Address = '12

*Generate Interrupt and Status

Function Code	OCP	SKS	INA	OTA
00	-	Skip if INA 00 Ready	Input Reg File	Step Neg *
01	-	Skip if not Busy	-	Step Pos *
02	-	Skip if End of Record in Format	-	Select Device
03	-	-	-	Read *
04	-	Skip if Not Interrupting	-	Write *
05	-	-	-	Verify (opt) *
06	-	-	-	INA Setup
07	-	-	-	Format (opt) *
10	-	-	-	Locate *
11	-	-	-	-
12	-	-	-	-
13	-	-	-	-
14	Ack Interrupt	-	-	DMA/C Channel
15	Set Int Mark	-	-	Micro-Verify
16	Clear Int Mark	-	-	Interrupt Vector
17	Initialize	-	-	Write Deleted Data Mark(opt) *

APPENDIX E

SECTOR SIZE TABLE

No. of Sectors	No. of Bytes/Sector Formatted	No. of Bytes/Sector Written
1	4834	4604
2	2390	2276
3	1576	1500
4	1168	1112
5	924	880
6	760	724
7	644	614
8	558	530
9	490	466
10	434	414
11	390	372
12	352	336
13	322	306
14	294	280
15	272	258
16	252	240
17	234	222
18	218	208
19	204	194
20	190	182
21	178	170
22	168	160
23	158	150
24	150	142
25	142	134
26	134	128
27	128	120
28	122	114
29	116	108
30	110	102
31	104	96
32	100	92

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