PEC

APPLICATION NOTES

MODELS 7X20, 6X60, 7X40, AND 6X40 TAPE TRANSPORTS

PERIPHERAL EQUIPMENT CORPORATION
Chatsworth, California 91311

Revised November 1969
Document 50259

PEC

FOREWORD

This document essentially details the parameters, usage, and pertinent interface data for the Models 7X20, 6X60, 7X40, and 6X40 Tape Transports. It should be used in conjunction with the equipment specifications and is intended for OEM applications.

PEC

I. GENERAL

The Models 7X20, 6X60, 7X40, and 6X40 Tape Transports are manufactured by PERIPHERAL EQUIPMENT CORPORATION, Chatsworth, California.

These models are IBM-compatible synchronous tape transports designed for applications where the connection of one or more transports is required in data acquisition or small-scale computer systems at minimum cost. The 7X20 and 7X40 standard tape speeds of 6.25 and 12.5 ips provide for data transfer rates of up to 10,000 bytes per second in either the forward or reverse direction. The 6X40 and 6X60 standard tape speeds of 12.5, 18.75, 25, and 37.5 ips provide for data transfer rates of up to 30,000 bytes per second in either the forward or reverse direction. The 7X20 and 6X60 transports use a single stack, read/write magnetic tape head; the 7X40 and 6X40 use a dual stack, simultaneous read-after-write head.

Separate configurations are available for operation in either the 9- or 7-track tape format as follows.

Model	Format	Density (bpi)	Data Transfer Rate (kHz) (Max.)
78X0-9	9 track	800	10.0
68X0-9	9 track	800	30.0
78X0-75	7 track	800/556	6.95 to 10.0
68X0-75	7 track	800/556	20.85 to 30.0
78X0-72	7 track	800/200	2.5 to 10.0
68X0-72	7 track	800/200	7.5 to 30.0
75X0-72	7 track	556/200	2.5 to 6.95
65X0-72	7 track	556/200	7.5 to 20.85

PEC

The design of the interface electronics is a feature of these transports. Up to four independently addressable transports can be attached to a system by a simple parallel connection to a common interface. This facilitates the expansion of an existing system and at the same time reduces cabling to a minimum.

This document is intended to supplement Product Specifications PEC 100750, 100762, 100872, and 100911. It supplies additional technical information and suggests techniques by which the transports may be integrated into the user's equipment. Note that the recommendations contained herein, particularly regarding IRG length and timing, are intended for computer-type applications where the overwriting of selected records on a pre-recorded tape is not required.

1-1. TAPE FORMATS

Details of the 9- and 7-track tape formats are shown in Figures 1 and 2.

1-2. LOAD PROCEDURE

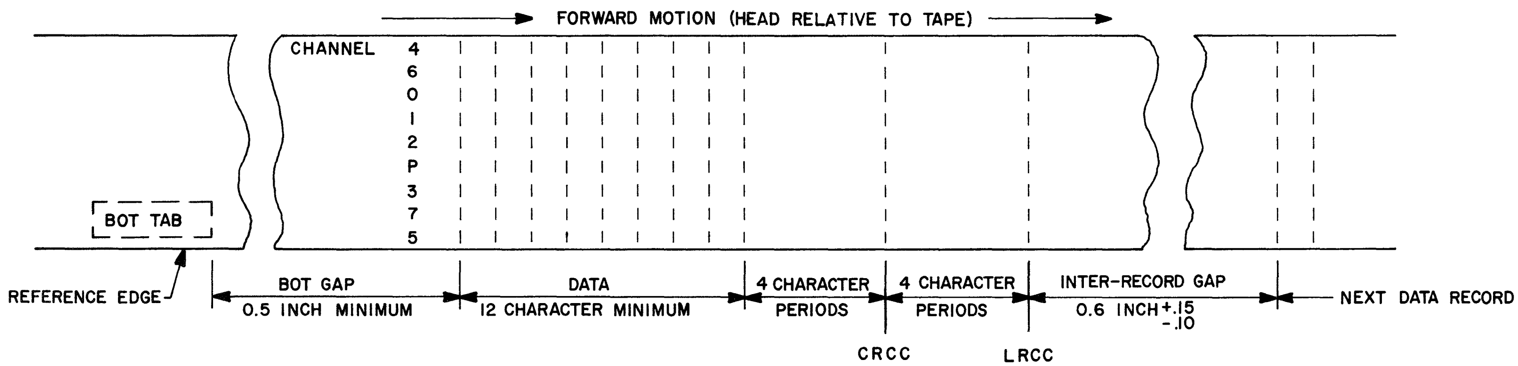
The following procedure is required to load a tape and prepare the transport for use.

(1) Turn the power on.

(2) Mount the file reel onto the transport, thread the tape, and place one turn on the take-up hub. Take up unnecessary slack.

Note

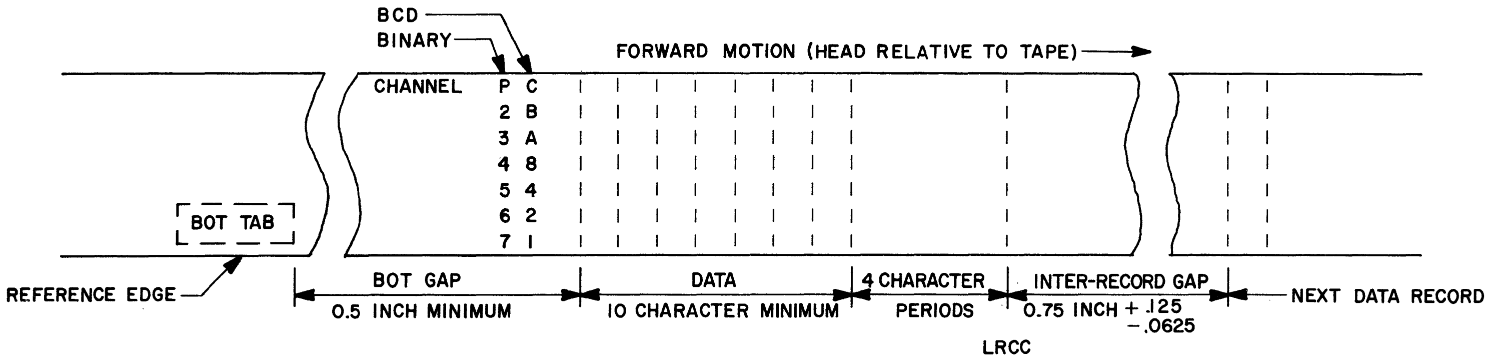
If writing is required, the file reel must be fitted with a Write Enable ring.



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE CRCC AND THE LRCC) IS EVEN. IN THE 9-TRACK FORMAT THE LRCC WILL NEVER BE AN ALL-ZEROES CHARACTER.
5. IT IS POSSIBLE FOR THIS CRCC CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED
6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE CRCC CONTAINS ALL ZEROES. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.6 INCH) FROM THE FOLLOWING RECORD.
7. DATA PACKING DENSITY IS FIXED AT 800 BITS PER INCH.

Figure 1. 9-Track Format



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 2 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) CONTAINS ODD DATA PARITY FOR BINARY TAPES, OR EVEN PARITY FOR BCD TAPES.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE LRCC) IS EVEN. IT IS POSSIBLE IN THE 7-TRACK FORMAT FOR THIS CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
5. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 4, 5, 6 AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.75 INCH) FROM THE FOLLOWING RECORD.
6. DATA PACKING DENSITY MAY BE 200, 556, OR 800 BITS PER INCH.

PEC

Figure 2. 7-Track Format

(3) Depress the LOAD control. This will complete an interlock and the tape will become tensioned.

(4) Depress the LOAD control again. The tape will move forward and come to rest at BOT. The LOAD indicator is lighted when the BOT tab is positioned under the photosensor unit. The LOAD control is now disabled and will remain disabled until the interlock is broken (usually when the tape is unloaded).

(5) Depress the ON LINE control. This can be done while the transport is still loading. The ON LINE indicator will light and the transport will become ready for use when the load operation is completed.

1-3. UNLOAD PROCEDURE

(1) Depress the ON LINE control to put the transport under manual control (ON LINE indicator is off).

(2) Depress the REWIND control. The tape will rewind and come to rest at BOT.

(3) Depress the REWIND control again. The tape will rewind from BOT until tape tension is lost at the physical beginning of tape.

Note

The REWIND control is always enabled in the off-line mode and will override a LOAD command, if that is currently in progress.

PEC

II. WRITE OPERATION

A write operation is one in which tape motion takes place with write current flowing in the read/write heads. Writing normally occurs in the forward direction for commands such as WRITE RECORD, WRITE FILE MARK, or ERASE. However, it is also possible to write in the reverse direction (e.g., reverse ERASE), but this is not a recommended procedure.

An interface line, SET WRITE STATUS (SWS), under the control of the customer, specifies whether a read or a write command is required. Shortly after a forward or reverse command (SYNCHRONOUS FORWARD (SFC) or SYNCHRONOUS REVERSE (SRC) is given at the beginning of each data transfer, the condition of SWS is sampled and stored in a control flip-flop (WRT) in the transport logic. If a write command is required, WRT is set true and turns on write current in the heads. For read commands, WRT is set false, turning off the write current.

WRT retains the present read/write status until it is overwritten at the beginning of the next command, or it is forcibly reset to the false state by one of the following.

(1) A REWIND command (RWC).

(2) Switching to the off-line mode, either by an OFF LINE command (OFFC) or by pressing the ON LINE control.

(3) Loss of interlock.

A command that involves a change of read/write status should not be given until tape motion has ceased.

2-1. WRITE FORWARD COMMAND

The following sequence of events will take place when writing a record in the 9-track format using a single stack head (Models 7X20 and 6X60) and a tape speed of 12.5 ips. Typical waveforms are shown in Figure 3.

(1) Wait for tape motion to cease, set SWS true.

(2) Set SFC true, starting tape motion. The WRT flip-flop will set true shortly afterwards.

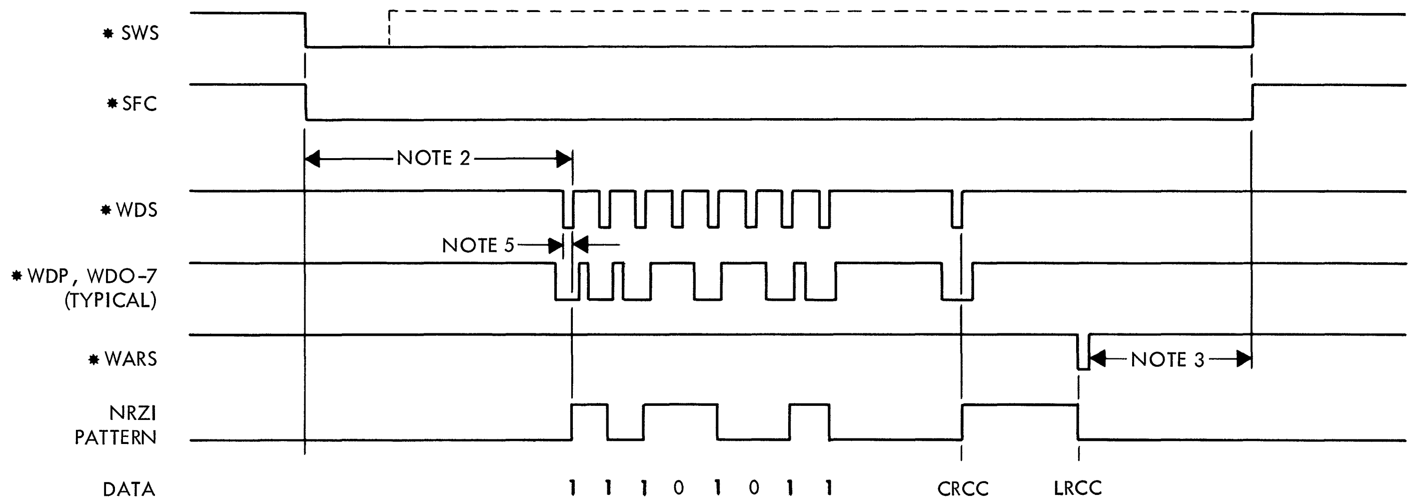
(3) Generate a pre-record delay as follows.
 (a) Write from BOT: 280 milliseconds.
 (b) WRITE FILE MARK: 280 milliseconds.
 (c) Write, not at BOT: 46 milliseconds.

(4) Generate WDS pulses together with appropriate data on WDP, WDO-7 for each data character to be written onto the tape. The frequency should be 10 kHz ±0.25 percent. (For a WRITE FILE MARK command, a single character is written with "1" bits in channels 3, 6, and 7.)

(5) Leave a 4-character gap, then generate an extra WDS pulse together with CRCC data on WDP, WDO-7. (CRCC is all zeros for WRITE FILE MARK.)

(6) Leave another 4-character gap, then generate a pulse on WARS. The leading edge of this pulse resets the write register in the transport, thus writing the LRCC onto the tape.

(7) Generate a post-record delay of 6 milliseconds. This delay ensures that the tape comes to rest further into the IRG



NOTES

1. CUSTOMER GENERATES THE WAVEFORMS MARKED*.
2. PRE-RECORD DELAY SHOULD BE 280 MILLISECONDS WHEN AT BOT OR FOR WRITE FILE MARK, 46-MILLISECONDS OTHERWISE.
3. POST-RECORD DELAY SHOULD ALWAYS BE 6 MILLISECONDS.
4. THE COMBINED PRE- AND POST-RECORD DELAYS DEFINE THE INTER-RECORD GAP.
5. WDS HAS A MINIMUM PULSE WIDTH OF 2 μSECONDS. WRITE DATA LINES WDP, WDO-7 MUST BE STEADY DURING, AND FOR 0.5 μSECOND EITHER SIDE OF WDS.
6. THE SWS LINE IS SET TRUE FOR WRITE COMMANDS ONLY. THIS WAVEFORM IS SAMPLED BY THE TRANSPORT LOGIC AT THE BEGINNING OF EACH DATA TRANSFER, AND MUST BE HELD STEADY FOR AT LEAST 20 μSECONDS AFTER THE LEADING EDGE OF SFC (OR SRC).
7. INTERFACE WAVEFORMS ARE SHOWN LOW-TRUE, AS THEY APPEAR ON THE INTERFACE CABLE.

PEC

Figure 3. Write Waveforms

than it would after a read operation. This prevents the possibility of unerased gap areas in a write, read reverse, read forward, write sequence of commands.

(8) Set SFC false. The tape decelerates and comes to rest after 30 milliseconds.

(9) WRT remains set and will continuously erase tape until some subsequent read, rewind, or off-line command is given (or the interlock is broken).

2-2. VERTICAL PARITY GENERATION

The vertical parity bit (VRC) recorded in channel P is generated so that the total number of "1" bits in each data character (not the CRCC or LRCC) is always odd.

2-3. CRC GENERATION

The CRCC is based on a modified cyclic code and provides a more rigorous method of error detection than using the VRC or LRC checks only. When reading, it can also be used in conjunction with the VRC and LRCC checks for error correction, provided that the errors are confined to a single channel.

The CRCC can be generated according to the following rules.

(1) Each data character is added to the contents of a CRC register (CRCR) without carry — each bit being exclusively OR'd to the corresponding bit of the CRCR.

(2) This information then undergoes a circular shift right of one place, such that each bit is copied into the adjacent CRCR flip-flop:

(CRCP → CRC0, etc.)

(3) If the bit entering CRCP is a "1", the bits entering CRC2, CRC3, CRC4, and CRC5 are inverted.

(4) Steps (1), (2), and (3) are repeated for each data character of the record.

(5) The contents of all CRCR positions, except CRC2 and CRC4, are inverted and the resultant character is written onto the tape.

Figure 4 shows a block diagram of a CRCR. Note that this circuit requires one clock pulse for each data character, and that no extra shift is required after the last data character.

If it is required to regenerate the CRCC during a READ REVERSE command, the significance of the data bits entering the CRCR must also be reversed.

The CRCC has the following properties.

(1) It can be an all-zeroes character.

(2) Its value is such that the LRCC always has odd parity (therefore the LRCC can never be all-zeroes).

(3) It has odd parity if there are an even number of data characters, or even parity for an odd number of data characters.

PEC

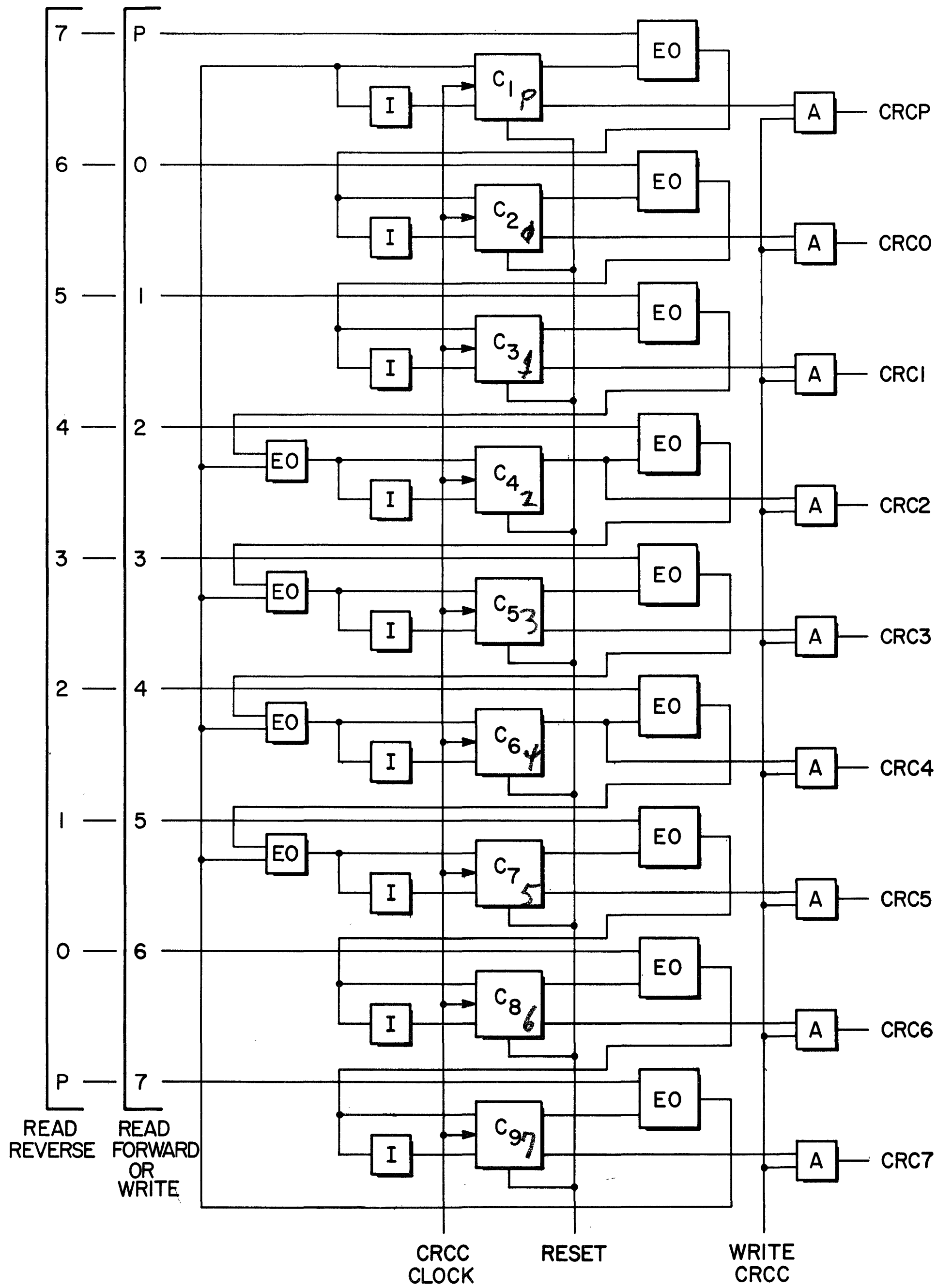


Figure 4. Cyclic Redundancy Check Register

For compatibility reasons, the correct CRCC should always be written onto tape, even though it is intended not to make use of it for read checking.

2-4. ERASING

Erasing is only required when it is necessary to abandon a specific area of tape after repeated write errors. This can be accomplished by using any one of the following methods.

(1) Backspace over the erroneous record and rewrite. For each iteration, the new record will be written approximately 0.125 inch further down the tape, leaving a longer IRG behind it.

(2) Backspace over the erroneous record, write file mark, backspace, then rewrite. This will leave an erased gap of about 4 inches.

(3) Erased gaps of any length can be generated by executing a dummy write command with the WDS line suppressed.

III. READ OPERATIONS

Reading can take place in either the forward or reverse direction.

For the Models 7X20 and 6X60 (single stack head), an interface line (RTH) under the customer's control selects one of two read circuit threshold levels as follows.

(1) RTH false: Low threshold. This level is normally selected.

(2) RTH true: High threshold. This is selected only for read-after-write data checks.

RTH must be held steady for the duration of each record.

For the Models 7X40 and 6X40 (dual stack read-after-write head), RTH is not used, and the read threshold is automatically controlled by the read/write status flip-flop (WRT).

The differential threshold provides a system margin for transport-to-transport compatibility and also gives limited protection against tape deterioration.

3-1. READ DATA

Although the individual bits of each data character are recorded simultaneously, they are read back from tape over a finite band of time. This skewing effect is caused by small static or dynamic misalignments of the tape path and by the effects of bit crowding.

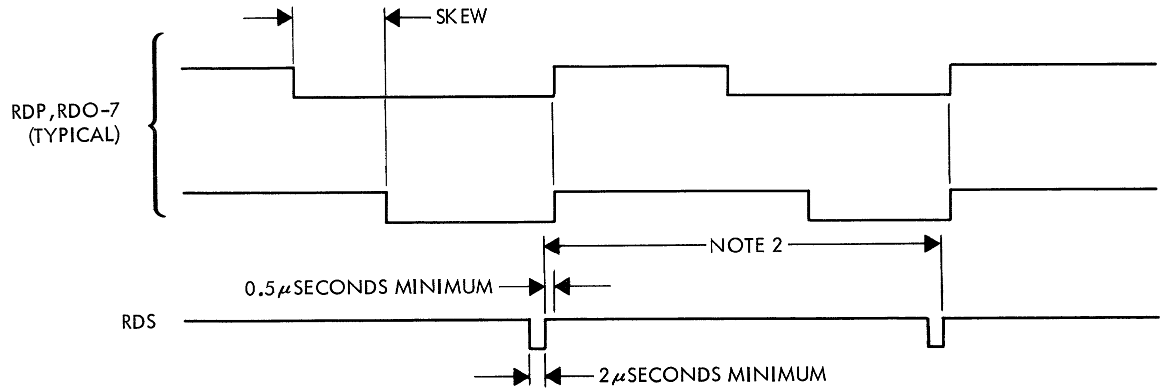
In this transport the static skew has been reduced to such a degree that individual deskew logic and adjustments for each track becomes unnecessary.

The transport read electronics first amplifies, then peak senses the read data from each track. This information is then copied into a skew register which assembles the 9 bits of each character into parallel form (see Figure 5). The outputs from the skew register are transmitted to the user's equipment on interface lines RDP, RDO-7.

Another interface line, READ DATA STROBE (RDS), is used to sample RDP, RDO-7. This waveform consists of a pulse for each character read from tape, and the trailing edge of each pulse should be used to sample the data lines.

3-2. READ FORWARD

One of the simplest and safest ways of implementing the read control logic is to make use of two "missing pulse detector" circuits. The first circuit continually looks for the gap between the last data character and the CRCC and has an optimum setting of 2-1/2 character periods. The second circuit searches for a 16-character gap at the end of the record. When this is found, the read circuits are disabled and a halt command is given to the transport. The second circuit makes sure that (except for the most massive of dropouts) the transport will always come to rest in a genuine IRG.



NOTES

1. RDP, RD0-7 SHOULD BE SAMPLED ON THE TRAILING EDGE OF EACH RDS PULSE.
2. CHARACTER PERIOD AVERAGES $\frac{1}{BV}$, WHERE B=DENSITY AND V=TAPE VELOCITY. HOWEVER, THIS CAN VARY CONSIDERABLY DUE TO THE COMBINED EFFECTS OF BIT CROWDING AND SKEW.
3. THESE WAVEFORMS ARE SHOWN LOW-TRUE, AS THEY APPEAR ON THE INTERFACE CABLE.

Figure 5. Read Data Waveforms

Typical read waveforms for such a scheme are shown in Figure 6. The sequence of events is as follows.

(1) Set SFC true.

(2) Generate a pre-record delay of 24 milliseconds (120 milliseconds at BOT) which suppresses read data while the tape is accelerating and the IRG is being traversed.

(3) Read data arrives and read data strobes are generated. The first strobe pulse activates both the gap detector and the end of record detector.

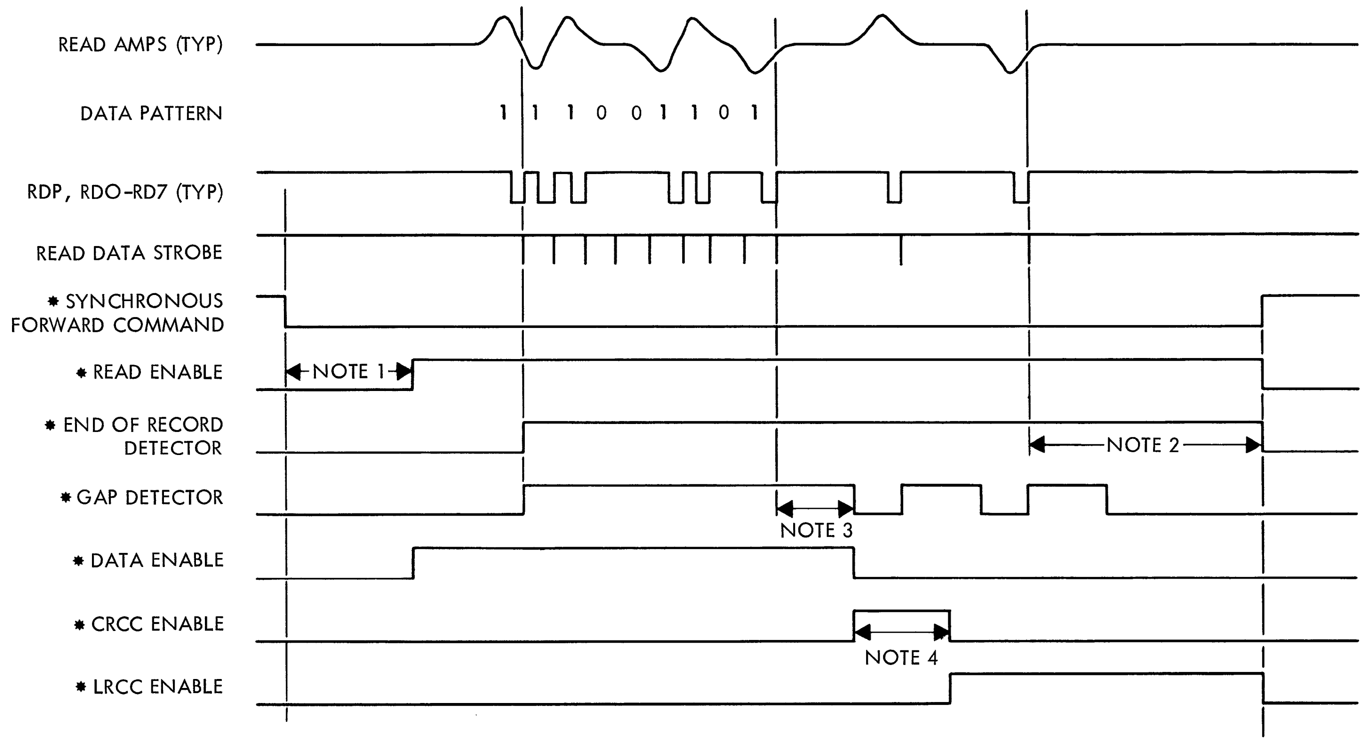
(4) Each character is processed in one or more of the following ways.

(a) Check for vertical parity error.
(b) Copy into the LRC check register.
(c) Copy into the CRC check register.
(d) Assemble into word or copy directly to memory.

(5) A gap of 2-1/2 character periods is detected. This triggers a delay of 3 character periods (300 μseconds). Any character occurring during this time can be treated as a CRCC and will be checked against the regenerated CRCC now held in the CRCR.

(6) All succeeding characters can be treated as a LRCC and will be checked against the contents of the LRC check register.

(7) A 16-character gap is detected. This disables the read logic and sets SFC false, stopping tape motion.



NOTES

1. THE PRE-RECORD DELAY SHOULD BE 120 MILLISECONDS WHEN AT BOT, OR 24 MILLISECONDS OTHERWISE. THIS GATES OUT UNWANTED READ DATA WHILE THE TRANSPORT IS ACCELERATING AND TRAVERSING THE IRG.
2. TAPE MOTION IS STOPPED AND THE READ CIRCUITS DISABLED WHEN A GAP OF 16 CHARACTER PERIODS IS DETECTED.
3. GAP DETECTOR DELAY IS 2-1/2 CHARACTER PERIODS.
4. THIS IS A FIXED DELAY OF 3 CHARACTER PERIODS. THE CRCC WILL OCCUR DURING THIS TIME.
5. CUSTOMER GENERATES THE WAVEFORMS MARKED*.
6. INTERFACE WAVEFORMS ARE SHOWN LOW-TRUE, AS THEY APPEAR ON THE INTERFACE CABLE.

Figure 6. Read Forward Waveforms

3-3. READ REVERSE

This can be implemented in a similar manner to read forward, except that special provision must be made because the LRCC and CRCC occur first. In addition, the significance of data bits entering the CRCR for check purposes must be reversed (see Figure 4).

A post-record delay of 6 milliseconds is required between the detection of end of record and the stopping of tape motion (setting SRC false). This will bring the tape to rest in the optimum position in the IRG for subsequent read or write commands.

3-4. FILE MARK DETECTION

Since it is generally required to detect a File Mark in either the forward or reverse direction, no use can be made of the 3-1/2 inch gap that separates it from the previous record on the tape.

To qualify as a File Mark, a record should meet the following conditions.

(1) It consists of a single data character.

(2) The data character has the required pattern (000010011 for 9-track, 0001111 for 7-track).

(3) There is no LRCC check error.

IV. INTER-RECORD GAP (IRG)

The position of the head relative to data when the transport comes to rest in the IRG is determined by the stop/start times and distances of the transport, together with the pre- and post-record delays mentioned earlier under the various commands.

These delays with suggested values for the two tape formats are summarized in Table 1 for the Models 7X20 and 6X60 for a tape speed of 12.5 ips.

With the Models 7X40 and 6X40 (dual stack head), the controller will usually be designed to perform a simultaneous read-after-write data check. Under these circumstances the termination of a write command is initiated not when the last character is written, but by detection of a 16-character gap in read data after all read checking has been completed. A normal write post-record delay of 6 milliseconds is then given before tape motion is stopped. The delay values shown in Table 1 are not affected, except for the write pre-record delay. For the Models 7X40 and 6X40, the bracketed figures should be used.

The IRG generated from a write-write sequence of commands can then be calculated as shown in Table 2.

For a read-write sequence of commands, the IRG will be 0.075 inch shorter for both of the tape formats.

The delays are usually implemented in the form of individual one-shot elements or are dealt with collectively using counter

Table 1

Pre-Record and Post-Record Delays*

Command	Pre-Record Delay (milliseconds)		Post-Record Delay (milliseconds)	
	9-track	7-track	9-track	7-track
READ FORWARD from BOT	120	120	0	0
READ FORWARD normal	24	24	0	0
READ REVERSE	24	24	6	16
WRITE from BOT	280	280	6	6
WRITE normal	46 (34)	56 (44) = .15" (32) = .3"	6	6
WRITE FILE MARK	280	280	6	6

* To calculate the above delays for other tape speeds scale inversely proportional to tape speed; i.e., WRITE from BOT at 37.5 ips =

$$\frac{12.5}{37.5} \times 280 = 93.3$$

Table 2

IRG Calculations

Description	9-track (inch)	7-track (inch)
6 milliseconds post-record delay at 12.5 ips	0.075	0.075
Stop distance	0.190	0.190
Start distance	0.190	0.190
Remainder of pre-record delay at 12.5 ips	0.200	0.325
TOTAL	0.655	0.780

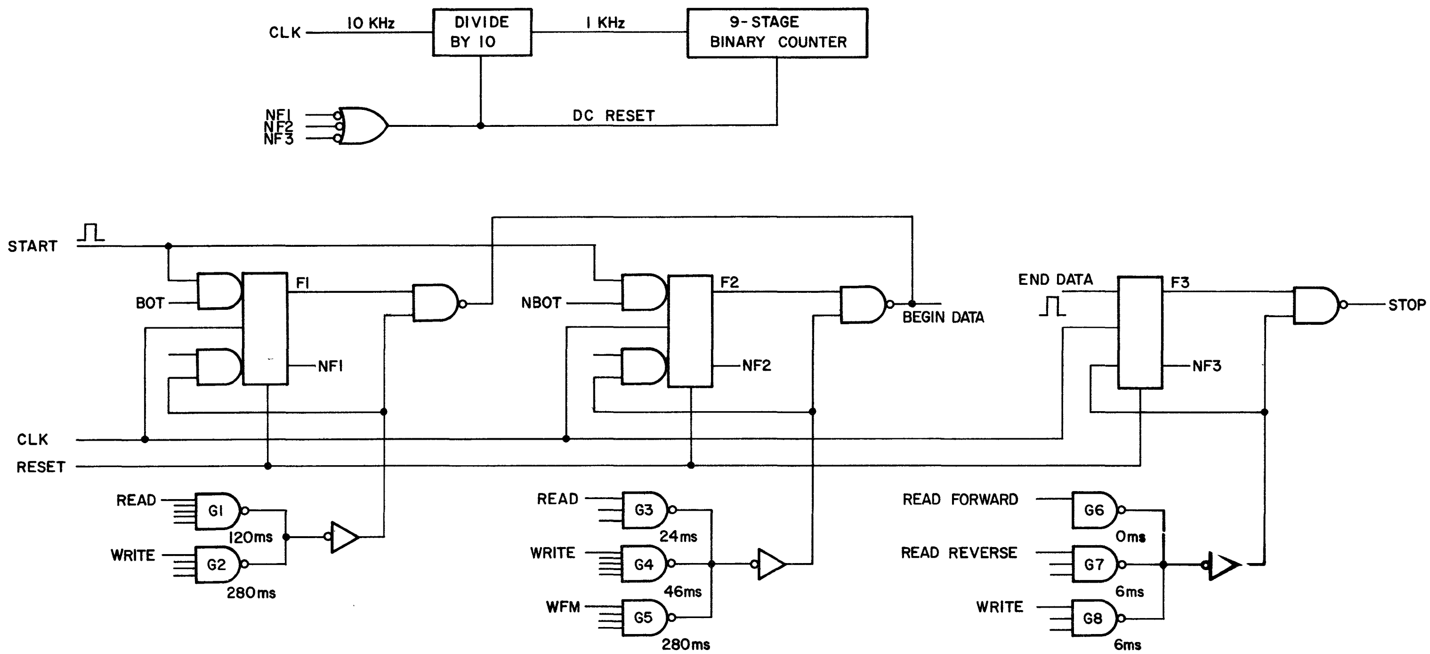
techniques. One-shots are generally more expensive, but offer greater flexibility for last minute changes to the delay periods.

The counter technique is entirely digital and has the added advantage that the same logic can be used with tape transports having different tape speeds by a simple change in clock frequency. Such a scheme is illustrated in Figure 7.

The sequence is initiated by a START pulse when SFC or SRC goes true. This sets F1 or F2, depending on whether or not the tape is at BOT; the 9-stage counter is now activated. When a count is reached corresponding to the pre-record delay for the particular command in progress, one of the gates (G1 through 5) is operated and both the flip-flop and counter are reset. A pulse is generated on BEGIN DATA which is used by the controller logic to initiate the transfer of data to or from tape.

On completion of the transfer, an END DATA pulse from the controller sets F3. The appropriate post-record delay is now generated in a similar manner as previously described using gates G6 through G8.

Finally, the STOP pulse resets SFC or SRC, which stops tape motion and terminates the command.



NOTES

CLK CAN BE THE SAME 10KHz CLOCK THAT IS USED TO GENERATE WDS PULSES.

Figure 7. Delay Generation — Counter Method

PEC

V. COMMAND SEPARATION

The Models 7X20, 6X60, 7X40, and 6X40 Tape Transports have no inherent program restrictions. However, for correct system operation the customer should ensure that tape motion has ceased before attempting to:

(1) Change tape direction. This preserves the integrity of transport stop/start times and distances for the users read and write logic.

(2) Change Read/Write Status. This prevents the possibility of unerased areas of tape being left in the IRG.

One method of achieving this is simply to separate all commands by at least the transport stop time (30 milliseconds). This method should be adequate for the majority of the transport's applications.

Alternatively, if maximum performance is required, additional logic can be added to detect the two conditions previously described. A new command, provided that it is of the same type and direction as the previous one, is then allowed to commence immediately, even though the transport may still be decelerating from the previous command. This is made possible by the characteristics of the transport's acceleration and deceleration ramps, which are such that all timing described in Section IV remains valid. The net result is a time saving of up to 30 milliseconds per command.

The only resultant side effect is that the IRG generated during write commands can be slightly longer than normal. This difference has a maximum value of 0.095 inch, and can usually be neglected in the interest of overall system performance. It is plotted in Figure 8 as a function of the command separation.

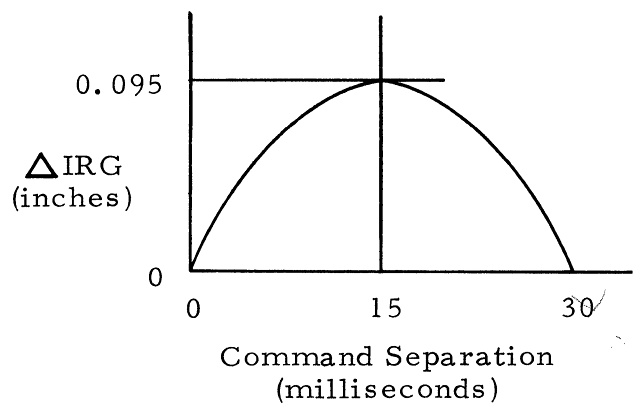


Figure 8. ΔIRG as a Function of the Command Separation

VI. INTERFACE

6-1. CIRCUIT CONFIGURATION

The circuit in Figure 9 is used.

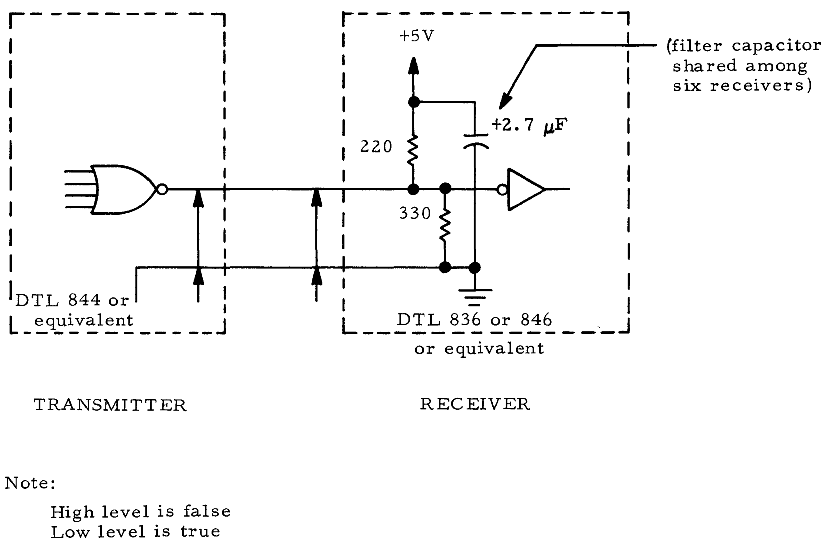


Figure 9. Interface Circuit

This design is based on the limited temperature range (0 to 75°C) of DTL 830 series integrated circuits. DTL 844 or 832 power gates are used as transmitters and DTL 836 inverters or DTL 846 dual input gates are used as receivers.

All signal inputs should be included in one harness and all outputs in a second harness. The maximum transmission distance is 20 feet. The two harnesses can be run in close proximity. The signals are transmitted by individual twisted pairs to reduce crosstalk.

The circuits are designed so that either a disconnected wire or removal of power at the transmitter results in a false signal being interpreted at the receiver end of the harness. The minimum recommended pulse width is 2 μseconds.

The twisted pairs should have the following characteristics.

(1) Maximum length of 20 feet.

(2) Not less than 1 twist per inch.

(3) 22 gauge or 24 gauge conductors with minimum insulation thickness of 0.01 inch.

It is important that the ground side of each twisted pair be grounded within 6 inches of the interface circuit to which it is connected.

The following figures give the noise margin remaining after accounting for worst-case crosstalk.

	0°C	25°C	50°C
Low Level (millivolts)	450	250	200
High Level (millivolts)	300	450	550

VII. SYSTEM CONFIGURATIONS

From one to four tape transports may be connected to a system provided the total cable length does not exceed 20 feet.

Line terminating resistors are required at the controller for all incoming signals and at the furthest removed transport for all outgoing signals.

A typical installation is shown in Figure 10.

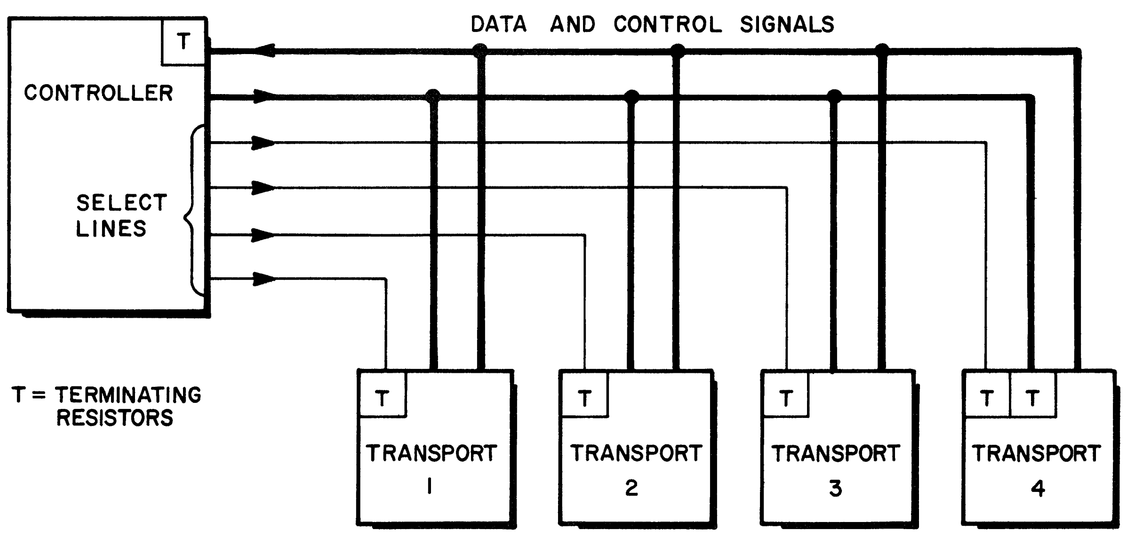


Figure 10. Daisy-Chain Connection

PEC

An individual SELECT line is provided for each transport in the system while all other interface signals are daisy-chained. No two SELECT lines may be true at the same time.

It is possible for the controller to execute any command on any transport and in any sequence.

Execution of an OFF LINE command (OFFC) will reset the ON LINE flip-flop in the selected transport. This transport will not respond to further external commands until it is manually placed on line again by the operator.

The status of a transport can be inspected by raising the appropriate SELECT line. The various status signals are summarized as follows.

ON LINE	Transport under remote control
RDY	Transport ready to accept remote commands.
RWD	Rewinding
EOT	End of Tape
LDP	Load Point (BOT)
FPT	File Protect (No Write Enable ring on file reel).
DDI	Density Indicator (7 track option only)

In some cases it may be desirable to have one transport in use and to have one or more others on standby, ready for quick interchange with the first without having to change the SELECT lines. This may be accomplished by a jumper connection in the transport logic which ANDs the incoming SELECT line with the ON LINE flip-flop.

Only one transport is allowed to be ON LINE at a time and this is the one that will communicate with the controller.

This configuration is shown in Figure 11.

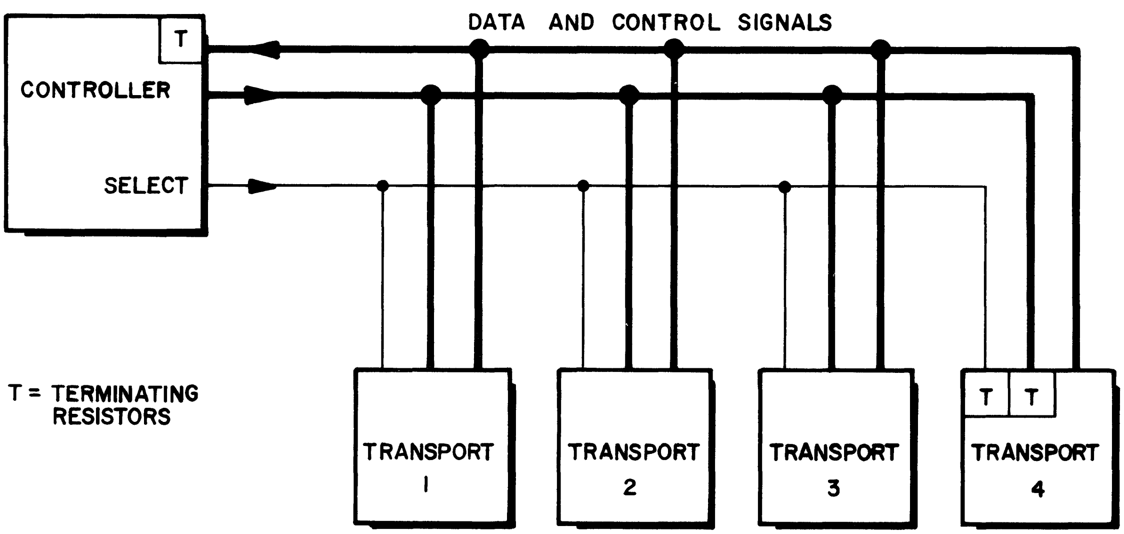


Figure 11. Alternate Connection Configuration