# MOTOROLA MCA 500/1300 ALS-TTL

## Semicustom IC Design Kit

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## TRADEMARKS

# ABOUT THIS MANUAL

This manual describes the Motorola MCA500/1300 Semicustom IC Design Kit, which consists of P-CAD's NX-M500 translator program and the Motorola MCA500/1300 ALS-TTL Macrocell Array Library.

The manual is divided into two sections: Section I describes the design kit and Section II describes the macrocell library.

**Section I, DESIGN KIT USER'S MANUAL**, contains the following:

**Chapter 1, INTRODUCTION**, provides an overview of the design kit and installation instructions.

**Chapter 2, PREPARING THE INPUT FILES**, gives instructions for creating the files to be input into the NX-M500 translator program.

**Chapter 3, TRANSLATING THE NETLIST**, gives instructions for using the NX-M500 program to translate netlists into LOGCAP files.

**Chapter 4, VIEWING THE OUTPUT FILES**, describes the NX-M500 output files.

**Section II, MOTOROLA MCA500/1300 ALS-TTL COMPONENT LIBRARY**, contains an overview and detailed descriptions of the macrocell components.

# NOTATION

This manual gives step-by-step procedures and examples. To make it easy for you to follow these procedures, we use the following notation.

---

**<xxxx>** Angle brackets around lowercase letters indicate a variable name that may be entered by the system or by you. For example:

<filename>.SCH

**[ ]** Square brackets indicate the name of a key. For example:

[Return]

**[Return]** [Return] indicates the key that is used to execute a command or accept an option. This key may be labeled differently, depending on your system. For example:

[RETURN], [↵], [Enter], [Enter ↵], [ENTER]

**[ ]-[ ]** Square brackets connected with a hyphen indicate keys that must be pressed simultaneously. For example:

Press [Ctrl]-[Alt]-[Del].

**UPPER** Uppercase letters indicate a command or an element that must be typed as shown. For example:

Type PCPLOTS and press [Return]

/ A forward slash separates main menu and submenu command combinations. For example:

DRAW/ARC

* An asterisk in a filename or in a filename extension indicates that any character(s) can occupy that position and all the remaining positions in the filename or extension. For example, the DOS command

DIR *.SYM

displays a list of all the filenames with the extension .SYM in the current directory.

**TESTFILE** TESTFILE is a sample filename, which you must replace with the filename you intend to use. For example:

Database Filename : TESTFILE.SCH
Netlist Filename : TESTFILE.NLT

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## SECTION I. DESIGN KIT USER'S MANUAL

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SECTION II. MOTOROLA MCA500/1300 ALS-TTL COMPONENT LIBRARY



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# CHAPTER 1. INTRODUCTION

The Motorola MCA500/1300 ALS-TTL Semicustom IC Design Kit consists of this manual and five diskettes containing the macrocell component library, the netlist files extracted by PC-NODES from each of the library components, and the NX-M500 translator program.

This manual is a guide to using the Motorola MCA500/1300 ALS-TTL Macrocell Array Library on the P-CAD design system. It assumes that you have the manuals for the P-CAD programs and are familiar with their use. If you are not yet familiar with the P-CAD system, we recommend that you complete the tutorials provided with the system before using the component library.

## OVERVIEW

This design kit, together with PC-CAPS, PC-NODES and PC-LINK, enables you to create a schematic design using Motorola ALS-TTL macrocell components. This design can be prepared for either PC-LOGS or Motorola's CAD system.

There are five stages in this process:

1. Using PC-CAPS, you prepare the schematic design. The design consists of one or more schematic files (<filename>.SCH), which are created by connecting symbols (<filename>.SYM) from the Motorola Macrocell Array Library.

2. Using PC-NODES, you extract a netlist (<filename>.NLT) from each schematic file. The design kit already contains netlists extracted from each macrocell component. Netlist files contain component and interconnection information for each schematic file or macrocell file.

3. After you extract all the netlists, you use PC-LINK to link all the netlists you intend to use into a single expanded netlist file (<filename>.XNL).

   You can use the expanded netlist as input into either PC-LOGS or the NX-M500 translator program. Use step 4 to use P-CAD's PC-LOGS program for local analysis or step 5 to use the Motorola CAD system for mainframe analysis.

4. To use PC-LOGS, input the expanded netlist into PRESIM, which outputs the <filename>.NET file for input to PC-LOGS and simulation by PC-LOGS and the POSTSIM postprocessor. PRESIM, PC-LOGS, and POSTSIM are described in their corresponding manuals.

5. To translate the design for the Motorola CAD system, input the expanded netlist into the NX-M500 translator program. NX-M500 outputs two files:

   - The Motorola-compatible LOGCAP file (<filename>.LCP) can be input into the LOGCAP program and other analysis tools in Motorola's CAD system.

   - The cross-reference file (<filename>.XRF) lists component aliases assigned by NX-M500 and used in the LOGCAP file.

Figure 1-1 illustrates the process described above.

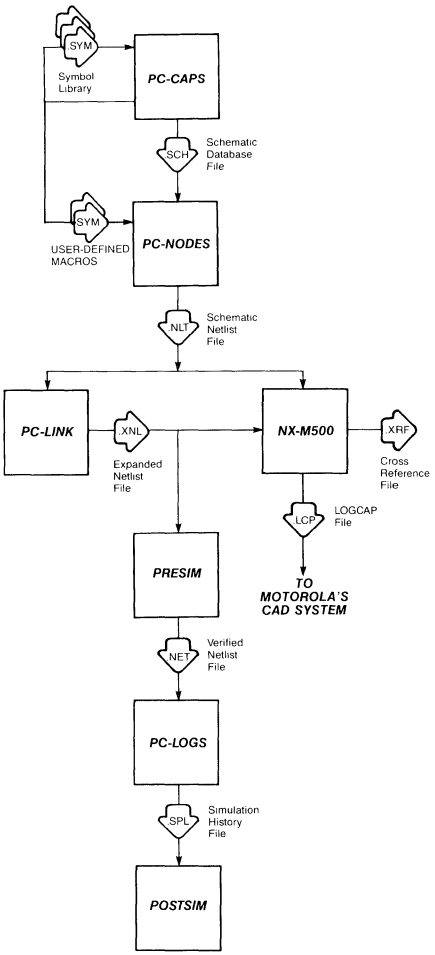



**Figure 1-1. Design Kit Data Flow**

## SYSTEM REQUIREMENTS

Before you can install the design kit, your computer system must have the following minimum configuration:

- IBM PC, PC/XT, PC/AT, TI PC, Tandy 2000 or equivalent
- 640K of RAM
- P-CAD supported graphics board and monitor
- DOS 2.0 or higher operating system
- CONFIG.SYS in the root directory, containing a BUFFERS value of at least 12 and a FILES value of at least 15
- The PCADDRV.SYS file (created automatically when you use the P-CAD INSTALL program) in the root directory and the appropriate loadable device driver files in the appropriate directory as specified in the PCADDRV.SYS file

## INSTALLATION

The design kit consists of five diskettes -- three diskettes containing the symbol library, one diskette of netlist files, and the NX-M500 diskette.

To install the design kit on your hard disk, follow the procedures below. These procedures assume that you are using the P-CAD-recommended directory structure.

First, create three new directories for the symbols and netlists by typing

```
MD \PCAD\MOTOROLA [Return]
MD \PCAD\MOTOROLA\M500 [Return]
MD \PCAD\MOTOROLA\M500\NLT [Return]
```

To install the symbol library, first change directories by typing

```
CD \PCAD\MOTOROLA\M500 [Return]
```

Then insert each of the three symbol diskettes into drive A in turn. For each diskette, copy the files by typing

```
COPY A:*.* [Return]
```

Remove each diskette after copying the files.

To install the netlist files, change directories by typing

```
CD \PCAD\MOTOROLA\M500\NLT [Return]
```

Then insert the netlist diskette into drive A, and copy the files by typing

```
COPY A:*.* [Return]
```

Remove the diskette.

To install the NX-M500 program first change to the \PCAD\EXE directory by typing

```
CD \PCAD\EXE [Return]
```

Then insert the NX-M500 program diskette into drive A and copy the file by typing

COPY A:NXM500.EXE [Return]

P-CAD suggests that you use the library and NX-M500 from a project directory created as a subdirectory of \PCAD\MOTOROLA.

# CHAPTER 2. PREPARING THE INPUT FILES

Preparing a design involves capturing the schematic using PC-CAPS, then generating, flattening, and linking netlists using PC-NODES and PC-LINK.

## CREATING THE SCHEMATIC

Use PC-CAPS to prepare the schematics. Make all designs hierarchical. The topmost level should contain a symbol representing the functional design and PADIN and PADOUT symbols to represent input and output pins. NX-M500 extracts LOGCAP files from this top level. Use netlists extracted from the lower levels for PC-LOGS.

Unconnected input pins are allowed in schematics for LOGCAP files, but are not allowed in PC-LOGS. If you plan to simulate a design using PC-LOGS, connect the unconnected input pins to global nets called "CON1" for a logic high or "CON0" for a logic low. The stimulus command file for PC-LOGS must have statements that force the net "CON1" to a strong high level and "CON0" to a strong low level.

Net names can be from one to eight alphanumeric characters. If you want to name a net as an active low signal, use an apostrophe (') as the last character of the net name. PC-CAPS will display the net name with a bar over the top.

If your design has more than one sheet, assign the SHEET attribute to each sheet. To assign this attribute,

use the PC-CAPS ATTR/ACOM command in SYMB mode and type

SHEET=<sheet id>

where

**<sheet id>** is two characters (generally digits) and is unique for each sheet in the design.

### Input and Output Signals

Each circuit input requires a PADIN.SYM component. A net connected to the output pin of the PADIN.SYM component will be listed in the $INP statement of the LOGCAP output file. This signal can be viewed as the input signal to the circuit from an external source.

Each circuit output requires a PADOUT.SYM component. A net connected to the output pin of an output cell must be connected to the input pin of the PADOUT.SYM component. The actual output net is the net connected to the output pin of the PADOUT.SYM component. A net connected to the output pin of a PADOUT.SYM will be listed as an output signal on the $OUT statement of the LOGCAP output. This signal can be viewed as the output signal to the external environment.

Nets connected to the pins of the PADOUT symbols will also be listed as input and output signals in the $SUBU BOUT statement of the LOGCAP output.

### Bidirectional Pads

Each bidirectional pad must be modeled by a two-input Wired-AND, an input pad, and an output pad. The

Wired-AND must be represented by a WAND2.SYM symbol. An $AND statement will appear in the LOGCAP output file for each WAND2.SYM component in the circuit.

Figure 2-1 illustrates the use of Wired-AND components for bidirectional pads.

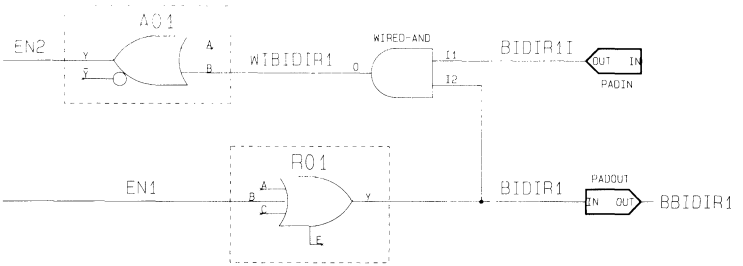



**Figure 2-1. Bidirectional Pad**

## Wired-OR

For each Wired-OR component used in the circuit, there must be one WOR.SYM with the appropriate number of inputs. The library provides WOR symbols for Wired-OR components with two to eight inputs. An $OR statement will appear in the LOGCAP output file for each WOR.SYM in the circuit.

## EXTRACTING AND LINKING THE NETLISTS

Run PC-NODES to extract a netlist for each network and sheet of a schematic. Use the instructions in the *PC-NODES User's Manual.* PC-NODES assigns names to unnamed nets and component instances, in the format UNsssnnn and UCsssnnn, respectively, where sss is the sheet ID assigned to the design using the SHEET attribute, and nnn is a number assigned sequentially starting with 000. If sheet IDs are not assigned or are not unique, the expanded netlist may contain several nets and/or components with the same name.

After you run PC-NODES, run PC-LINK to link all the sheet netlists and all the hierarchical component netlists together to create an expanded netlist suitable for either NX-M500 or PC-LOGS. Use the instructions in the *PC-LINK User's Manual.*

PC-LINK prompts you for a library path. This entry specifies alternate directories where PC-LINK will look for hierarchical netlist files (all Motorola ALS-TTL symbols are hierarchical). If the hierarchical netlists reside in more than one directory, enter all the directories, separating one from the next by a plus sign. If you are extracting a netlist for NX-M500, do not specify the path pointing to the library netlist files since the expanded netlist would then contain references to PC-LOGS primitives. When you run PC-LINK to extract a netlist for NX-M500, an error message will appear at the bottom of the screen. Review the PCLINK.MSG file; if all the errors indicate that the .NLT files for the Motorola ALS-TTL library components cannot be found, disregard the error messages and run NX-M500.

# CHAPTER 3. TRANSLATING THE NETLIST

This chapter describes the required conditions and procedures to configure and run NX-M500.

Before running NX-M500, be sure that:

- Your system is correctly configured.
- You have installed the NX-M500 program file (NXM500.EXE).
- You have assembled the schematic circuit.
- You have extracted and linked the netlist files.

To run NX-M500, be sure that you are in the appropriate directory and follow the steps below.

1. Type

   NXM500 [Return]

   The NX-M500 Title Screen appears. Press any key to continue. The system displays the NX-M500 Program Screen and prompts for the input netlist filename as shown in Figure 3-1.

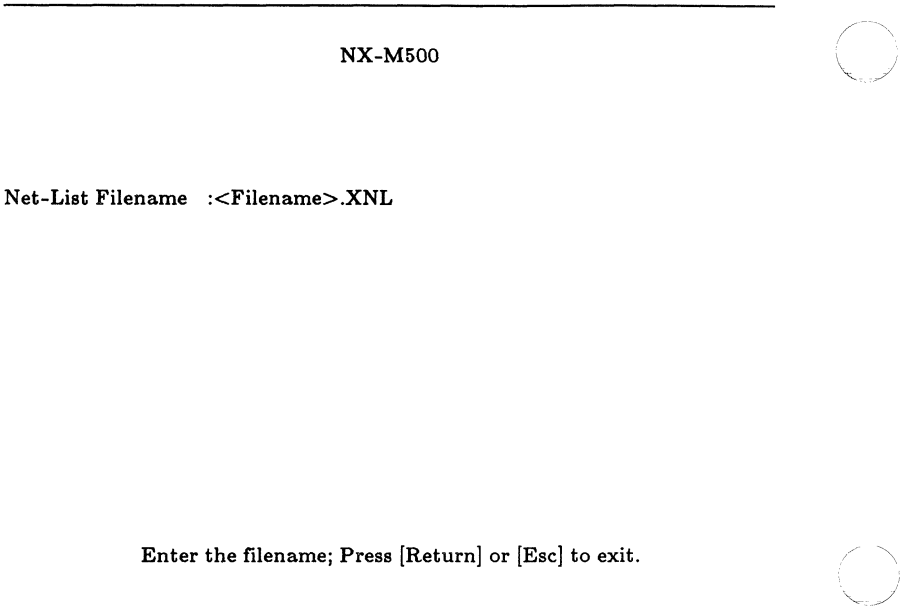



**Figure 3-1. NX-M500 Program Screen**

NOTE: At any prompt, if you decide not to continue with the program, press [Esc] to cancel and return to DOS.

2. Type the netlist filename and press [Return]. If you do not enter the filename extension, NX-M500 adds the .XNL extension.

   The system prompts for the output LOGCAP filename. The default is the input netlist filename with the .LCP extension.

3. Press [Return] to accept the default filename, or type another LOGCAP filename and press [Return].

The system prompts for the output cross-reference filename. The default is the input netlist filename with the .XRF extension as shown in Figure 3-2.

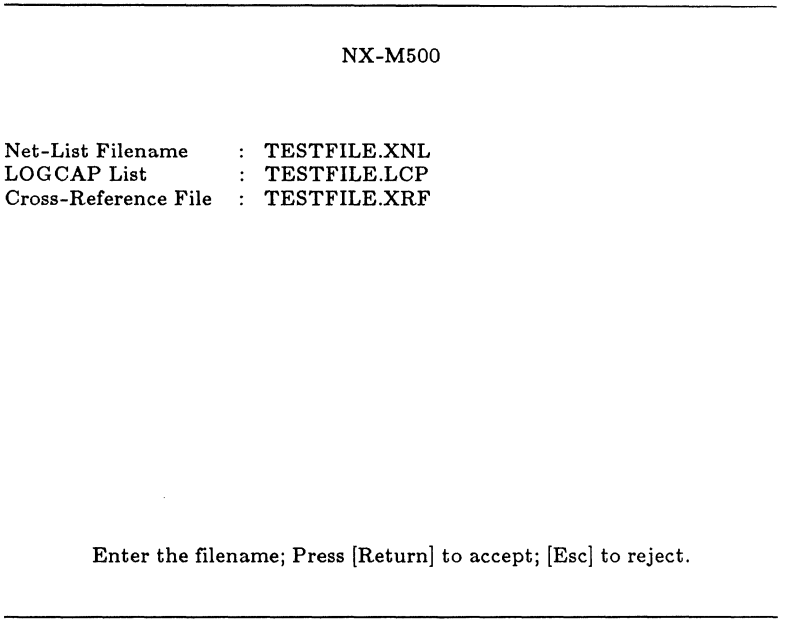



**Figure 3-2. Sample Program Screen**

4. Press [Return] to accept the default filename, or type another cross-reference filename and press [Return].

   NX-M500 sets up the netlist database environment and generates the LOGCAP netlist output. It displays progress reports and error messages on the lower section of the screen. When processing is complete, the system returns you to the Netlist prompt.

# CHAPTER 4. VIEWING THE OUTPUT FILES

The NX-M500 outputs two files, the LOGCAP netlist and the cross-reference files. The following sections describe these files.

## THE LOGCAP NETLIST

The basic LOGCAP statements are $NETWORK for network identification; $INP and $OUT for circuit inputs and outputs; and $AND, $OR, $SUBU, and $SUBU BOUT for macrocells and interconnects.

The following sections discuss these statements. An example of a schematic and the corresponding LOGCAP netlist output file are shown in the Design Example section. Refer to the sample netlist for examples of the statements.

### Conventions

The nets tied to the output pins are listed first. A slash separates the outputs from the inputs. An "&" indicates that the list is continued on the following line.

NX-M500 translates apostrophes, which PC-CAPS uses for netnames representing inverted signals, into the character "-". Apostrophes are invalid LOGCAP characters.

## $NETWORK Statement

$NETWORK is the first line in the LOGCAP netlist output. It denotes the type of file used to generate the LOGCAP netlist.

## $INP Statement

A single $INP statement directly follows the $NETWORK statement. NX-M500 uses the PADIN.SYM components for the inputs of the circuits being modeled. All nets connected to output pins of PADIN.SYM components are listed in the LOGCAP $INP statement as input signals. This signal can be viewed as the input signal to the circuit from an external source.

The format of the $INP statement is

$INP <net1> <net2> ... <netn>

where

**netn** is the name of a net connected to a PADIN.SYM output pin.

## $OUT Statement

A single $OUT statement follows directly after the $INP statement. NX-M500 uses the PADOUT.SYM components for the outputs of the circuit being modeled. All nets connected to output pins of PADOUT.SYM components are listed in the $OUT statement as output signals. The LOGCAP output signal can be viewed as the output signal to the external environment.

The format of the $OUT statement is

$OUT <net1> <net2> ... <netn>

where

**netn** is the name of a net connected to a PADOUT.SYM output pin.

### $AND Statement

NX-M500 generates a $AND statement for each WAND2.SYM component in the circuit. This symbol denotes a Wired-AND component with an I/O pin or a bidirectional pad with two inputs and one output.

The $AND statement lists the names of the nets tied to the input and output pins of the WAND2.SYM component and shows the number of inputs. The format of a $AND statement is

$AND 0 0
<outnet> 2 <innet1> <innet2>

where

**outnet** is the name of the net connected to the WAND2.SYM output pin.

**innet1** and **innet2** are the names of the nets connected to the WAND2.SYM input pins.

For example:

$AND 0 0
WIBIDIR1 2 BIDIR1I BIDIR1

## $OR Statement

The LOGCAP file contains a $OR statement for each WORx.SYM component (Wired-OR), where x is the number of nets Wire-ORed together. The $OR statement lists the names of the nets tied to the input and output pins of the WORx.SYM component and shows the number of inputs. A WORx.SYM component has one output and from two to eight inputs.
The format of a $OR statement is

```
$OR 0 0
<outnet> x <innet1> <innet2> ... <innetx>
```

where

**outnet** is the name of the net connected to the WORx.SYM output pin.

x is the number of input pins.

**innet1** through **innetx** are the names of the nets connected to the WORx.SYM input pins.

## $SUBU Statement

The LOGCAP file contains one $SUBU statement for each component (cell) in the circuit. Each $SUBU statement gives the definition name of the component and the names of the nets tied to the component input and output pins.

The format of a $SUBU statement is

```
$SUBU <compname>
<outnet1> <outnet2> ... <outnetn> / &
<innet1> <innet2> ... <innetm>
```

where

**compname** is the name of the component.

**outnetn** is the name of a net connected to an output pin.

**innet1** through **innetm** are the names of nets connected to input pins.

NX-M500 lists an unused output pin as "UN0", "UN1", etc. It lists an unused input pin as "CON0", with the following exceptions:

The pin is called "CON1" if the component with the unused input pin has an attribute of FTYPE="INP".

The pin is called "CON1" if the component has an attribute of FTYPE="OUT" and the unused pin is an enable pin named "E".

The following is an example of a $SUBU statement in a LOGCAP netlist:

```
$SUBU A02
HN000013 UN0 / &
CEP CON1 CET
```

### $SUBU BOUT Statement

The LOGCAP file contains a $SUBU BOUT statement for each output signal listed in the LOGCAP $OUT statement. A $SUBU BOUT statement models the input and output signals of the PADOUT.SYM components.

The format of the $SUBU BOUT statement is

$SUBU BOUT
<outname> / <inname>

where

**outname** is the name of the net attached to the output pin of the PADOUT.SYM component.

**inname** is the name of the net attached to the input pin of the PADOUT.SYM component.

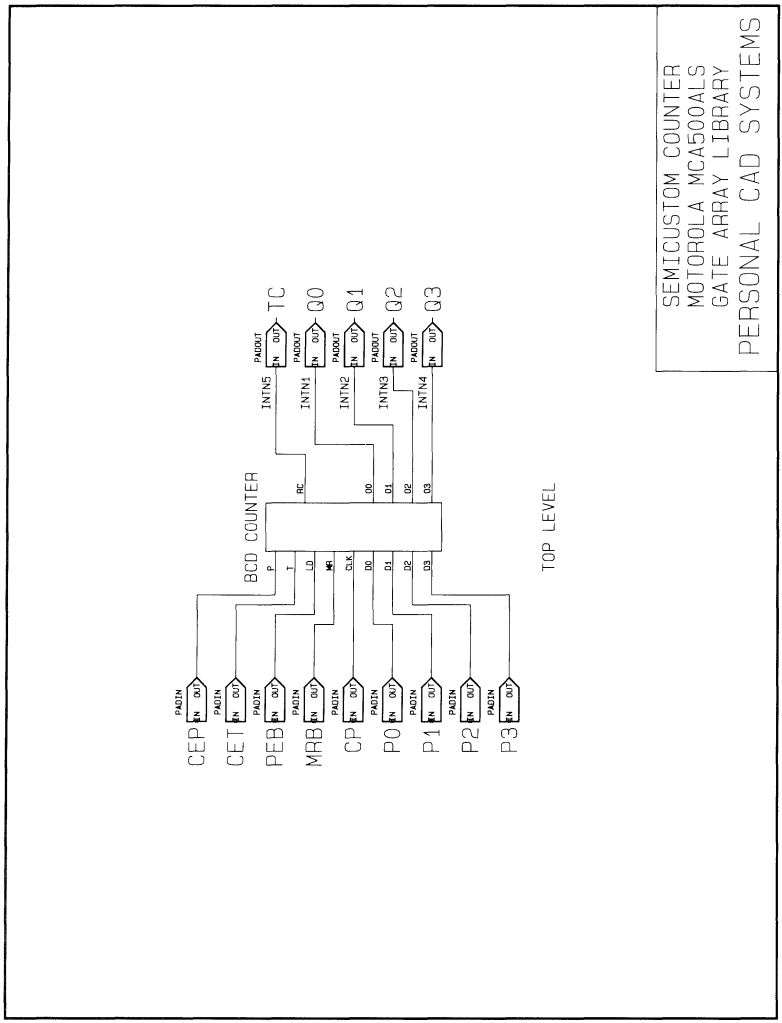
## THE CROSS-REFERENCE FILE

The cross-reference file created by NX-M500 lists all the names of nets and components renamed by NX-M500, and their aliases. The aliases are used in the LOGCAP output file. NX-M500 resolves duplicate default net and component names by changing the names to the form HNsssnnn and HCsssnnn, respectively, where sss is the sheet ID assigned with the SHEET attribute, and nnn is a three-digit number.

## DESIGN EXAMPLE

The following pages contain a design example showing a hierarchical design created using the ALS-TTL library and the resulting LOGCAP and cross-reference files output by NX-M500 for the design.

## Top Level Schematic

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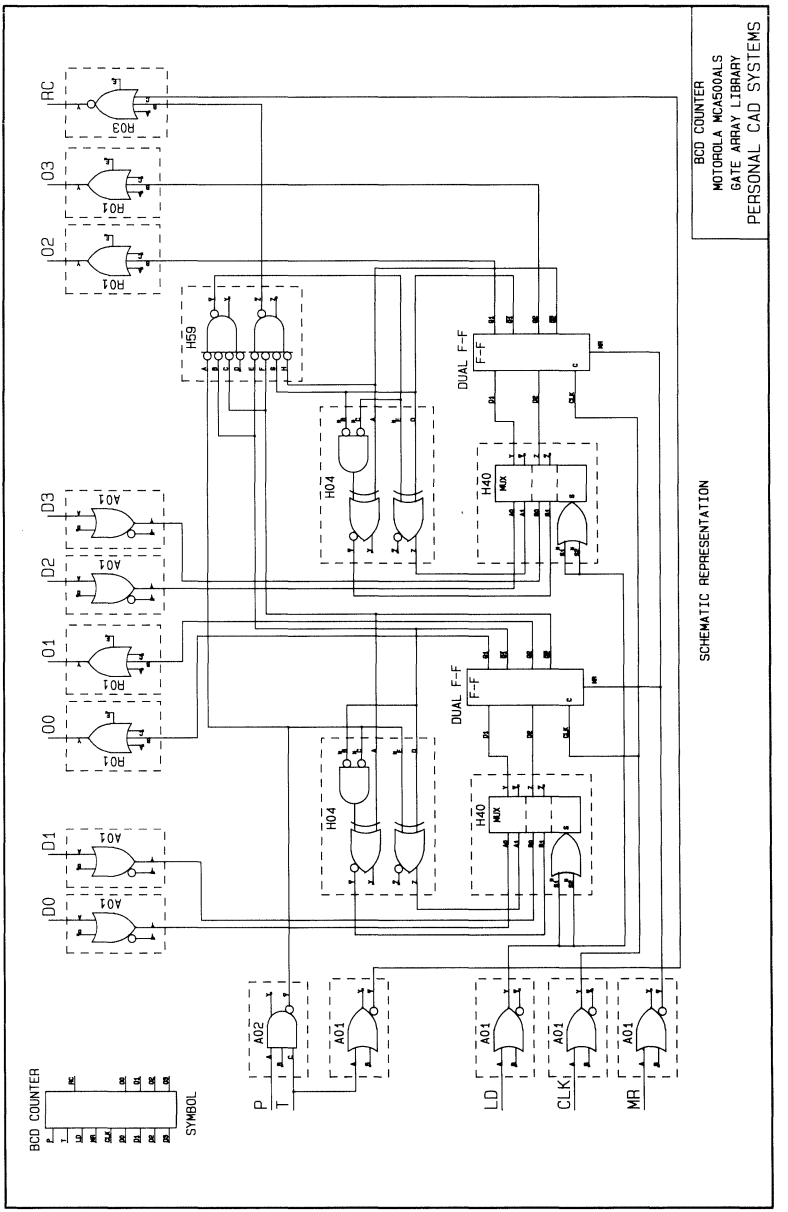
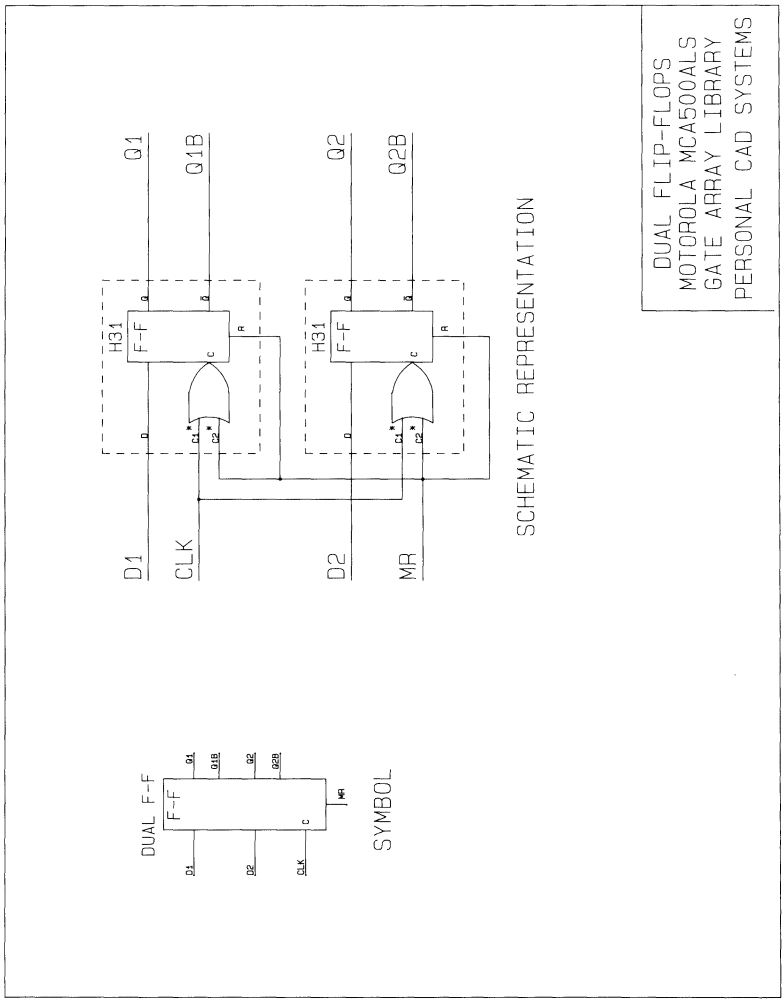
# Schematic Representation of BCD COUNTER




000-0139-00

## Schematic Representation of DUAL F-F

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## LOGCAP Netlist File

```
$$*********************************************************
$$                                                        *
$$   Copyright (C) 1983, 1986 - Personal CAD Systems, Inc. *
$$                                                        *
$$     Program  :   NX-M500  VERSION 1.31                 *
$$     Date     :   Jun 27 1986                           *
$$     Time     :   09:10:53 AM                           *
$$     File In  :   BCDMOT.XNL                            *
$$     File Out :   BCDMOT.LCP                            *
$$     Format   :   LOGCAP LIST                           *
$$                                                        *
$$*********************************************************


$NETWORK
$INP CEP CET PEB MRB CP P0 P1 P2 P3
$OUT TC Q0 Q1 Q2 Q3
$SUBU A01
UN0 HN000000 / &
PEB CON0
$SUBU A01
UN1 HN000001 / &
CP CON0
$SUBU A01
HN000002 UN2 / &
MRB CON0
$SUBU A01
HN000003 UN3 / &
CET CON0
$SUBU A02
HN000004 UN4 / &
CEP CON1 CET
$SUBU H31
HN000009 HN000010 / &
HN000001 HN000002 HN000006 HN000002
$SUBU H31
HN000007 HN000008 / &
```

```
HN000001 HN000002 HN000005 HN000002
$SUBU H31
HN000015 HN000016 / &
HN000001 HN000002 HN000012 HN000002
$SUBU H31
HN000013 HN000014 / &
HN000001 HN000002 HN000011 HN000002
$SUBU H40
HN000005 UN5 UN6 HN000006 / &
HN000000 HN000000 HN000017 HN000018 HN000019 HN000020
$SUBU H40
HN000011 UN7 UN8 HN000012 / &
HN000000 HN000000 HN000021 HN000022 HN000023 HN000024
$SUBU A01
UN9 HN000017 / &
P0 CON0
$SUBU A01
UN10 HN000019 / &
P1 CON0
$SUBU H04
HN000020 UN11 HN000018 UN12 / &
HN000008 HN000004 HN000010 HN000008 HN000004
$SUBU A01
UN13 HN000023 / &
P3 CON0
$SUBU A01
UN14 HN000021 / &
P2 CON0
$SUBU R01
INTN1 / &
CON0 HN000007 CON0 CON1
$SUBU R01
INTN2 / &
CON0 HN000009 CON0 CON1
$SUBU H04
HN000024 UN15 HN000022 UN16 / &
HN000014 HN000025 HN000016 HN000014 HN000025
```

```
$SUBU H59
HN000025 UN17 UN18 HN000026 / &
HN000004 HN000008 HN000010 CON0 HN000008 HN000010 HN000014
HN000016
$SUBU R01
INTN3 / &
CON0 HN000013 CON0 CON1
$SUBU R01
INTN4 / &
CON0 HN000015 CON0 CON1
$SUBU R03
INTN5 / &
CON0 HN000026 HN000003 CON1
$SUBU BOUT
TC / &
INTN5
$SUBU BOUT
Q0 / &
INTN1
$SUBU BOUT
Q1 / &
INTN2
$SUBU BOUT
Q2 / &
INTN3
$SUBU BOUT
Q3 / &
INTN4
```

## Cross-Reference File Created By NX-M500

```
************************************************************
*                                                          *
*           ALIAS NAME CROSS-REFERENCE                     *
*                                                          *
*                                                          *
*  NX-M500 Version 1.31                                    *
*                                                          *
*  Copyright (C) 1986 - Personal CAD Systems, Inc.         *
*                                                          *
*                                                          *
************************************************************


Net List Filename : BCDMOT.XNL

COMPONENT    SIGNAL     FULL PATH NAME

HC000000                = /UC000000/UC000000
             HN000000   = /UC000000/UN000006
HC000001                = /UC000000/UC000001
             HN000001   = /UC000000/UN000005
HC000002                = /UC000000/UC000002
             HN000002   = /UC000000/UN000004
HC000003                = /UC000000/UC000003
             HN000003   = /UC000000/UN000019
HC000004                = /UC000000/UC000004
             HN000004   = /UC000000/UN000013
HC000005                = /UC000000/UC000005
             HN000005   = /UC000000/UN000000
             HN000006   = /UC000000/UN000001
             HN000007   = /UC000000/UN000011
             HN000008   = /UC000000/UN000014
             HN000009   = /UC000000/UN000012
             HN000010   = /UC000000/UN000025
HC000006                = /UC000000/UC000005/UC000000
HC000007                = /UC000000/UC000005/UC000001
```

```
COMPONENT   SIGNAL     FULL PATH NAME
HC000008             = /UC000000/UC000006
            HN000011 = /UC000000/UN000002
            HN000012 = /UC000000/UN000003
            HN000013 = /UC000000/UN000020
            HN000014 = /UC000000/UN000026
            HN000015 = /UC000000/UN000021
            HN000016 = /UC000000/UN000023
HC000009             = /UC000000/UC000006/UC000000
HC000010             = /UC000000/UC000006/UC000001
HC000011             = /UC000000/UC000007
            HN000017 = /UC000000/UN000009
            HN000018 = /UC000000/UN000007
            HN000019 = /UC000000/UN000010
            HN000020 = /UC000000/UN000008
HC000012             = /UC000000/UC000008
            HN000021 = /UC000000/UN000017
            HN000022 = /UC000000/UN000015
            HN000023 = /UC000000/UN000018
            HN000024 = /UC000000/UN000016
HC000013             = /UC000000/UC000009
HC000014             = /UC000000/UC000010
HC000015             = /UC000000/UC000011
HC000016             = /UC000000/UC000012
HC000017             = /UC000000/UC000013
HC000018             = /UC000000/UC000014
HC000019             = /UC000000/UC000015
HC000020             = /UC000000/UC000016
            HN000025 = /UC000000/UN000024
HC000021             = /UC000000/UC000017
            HN000026 = /UC000000/UN000022
HC000022             = /UC000000/UC000018
HC000023             = /UC000000/UC000019
HC000024             = /UC000000/UC000020
```

## OVERVIEW

The library diskettes contain the following files for use with the PC-CAPS schematic capture program:

- Component files
- Special symbol files
- Netlist files for each component
- Standard-size drawing sheet files

## COMPONENT FILES

The Motorola MCA500/1300 ALS-TTL Macrocell Array Library contains all the components specified in the *Motorola MCA500ALS and MCA1300ALS TTL Macrocell Arrays Design Manual.*

Two types of attributes have been assigned to the library symbols for use with the NX-M500 program. These attributes are described below.

The first attribute has the form FTYPE="INP" or FTYPE="OUT". It is used with certain input or output cells that have one or more unconnected input pins or an unconnected enable pin named "E". In the LOGCAP $SUBU statement describing the cell inputs and output, the unconnected pins will be designated "CON0" or "CON1", as appropriate. Several examples are shown on the sample schematic and accompanying LOGCAP output.

The second attribute is used with an alternative symbol for a macrocell. The form of the attribute is ALT=<filename>, where filename is the macrocell ID.

For example, the M50 macrocell has two library symbols, M50.SYM and M50A.SYM. The alternative symbol, M50A, has the attribute ALT="M50" and will be shown in the LOGCAP output as "M50".

## SPECIAL SYMBOL FILES

In addition to the standard Motorola component symbols, the library includes special "noncomponent" symbols. Use these symbols with NX-M500 translate your design information into a LOGCAP format that is compatible with Motorola CAD systems. Each special symbol in the circuit is described on a line of the LOGCAP output. The symbols are:

**PADIN.SYM** - Represents a circuit input.

**PADOUT.SYM** - Represents a circuit output.

**WAND2.SYM** - Represents a wired-AND with two inputs.

**WOR2.SYM** through **WOR8.SYM** - Represent Wired-OR components with two to eight inputs.

## NETLIST FILES

Each symbol in the component library is hierarchical, composed of a network of PC-LOGS primitives. Each ALS-TTL macrocell in the library has an associated netlist file that contains all the network information of the simulation model.

## DRAWING SHEET FILES

The library includes standard-size drawing sheet files, ASIZE.SCH through ESIZE.SCH, for circuit design. These files provide the normal layer structure plus a drawing sheet border.

## LAYER STRUCTURE

The layer structure shown on this page is the default layer structure used by PC-CAPS. This layer structure was used to create the Motorola ALS-TTL symbols in this library.

Table 1. Default Layer Structure

| Layer | Name | Pen | Status | Use |
|---|---|---|---|---|
| 1 | WIRES | 1 | ABL A | Interconnecting wires |
| 2 | BUS | 1 | ABL | Not used |
| 3 | GATE | 2 | ON | Symbol geometrics |
| 4 | IEEE | 2 | OFF | Not used |
| 5 | PINFUN | 3 | OFF | Not used |
| 6 | PINNUM | 1 | OFF | Not used |
| 7 | PINNAM | 6 | ON | Pin names |
| 8 | PINCON | 4 | ON | Pin connections |

Table 1 Continued

| Layer | Name | Pen | Status | Use |
|---|---|---|---|---|
| 9 | REFDES | 2 | OFF | Not used |
| 10 | ATTR | 6 | OFF | Visible attributes |
| 11 | SDOT | 1 | OFF | Connect dots |
| 12 | DEVICE | 5 | ON | Macrocell ID |
| 13 | OUTLIN | 5 | ON | Component outlines |
| 14 | ATTR2 | 6 | OFF | Invisible attributes |
| 15 | NOTES | 6 | OFF | Not used |
| 16 | NETNAM | 4 | OFF | Net/signal names |
| 17 | CMPNAM | 5 | OFF | Component instance names |
| 18 | BORDER | 5 | OFF | Drawing/schematic border |

## COMPONENT LIST BY SEQUENCE

The component filename is the macrocell number plus the extension .SYM; for example, H01.SYM. "Page" refers to the page number of the component plot in the last section of this manual. "Disk" refers to the disk on which the component is stored.

| COMPONENT | DISK NO. | PLOT NO. | COMPONENT | DISK NO. | PLOT NO. |
|---|---|---|---|---|---|
| H01 | 1 | 1 | M28 | 1 | 28 |
| H02 | 1 | 2 | M29 | 1 | 29 |
| H03 | 1 | 3 | M30 | 2 | 30 |
| H04 | 1 | 4 | H31 | 2 | 31 |
| H05 | 1 | 5 | M32 | 2 | 32 |
| H06 | 1 | 6 | H33 | 2 | 33 |
| H07 | 1 | 7 | H34 | 2 | 34 |
| H08 | 1 | 8 | H35 | 2 | 35 |
| H09 | 1 | 9 | M36 | 2 | 36 |
| H10 | 1 | 10 | M37 | 2 | 37 |
| H11 | 1 | 11 | M38 | 2 | 38 |
| H12 | 1 | 12 | M39 | 2 | 39 |
| M13 | 1 | 13 | H40 | 2 | 40 |
| M14 | 1 | 14 | H41 | 2 | 41 |
| H15 | 1 | 15 | H42 | 2 | 42 |
| H16 | 1 | 16 | H43 | 2 | 43 |
| H17 | 1 | 17 | M44 | 2 | 44 |
| H18 | 1 | 18 | M45 | 2 | 45 |
| M19 | 1 | 19 | M46 | 2 | 46 |
| M20 | 1 | 20 | M47 | 2 | 47 |
| M21 | 1 | 21 | M48 | 2 | 48 |
| M22 | 1 | 22 | M49 | 2 | 49 |
| M23 | 1 | 23 | M50 | 2 | 50 |
| M24 | 1 | 24 | M50A | 2 | 51 |
| M25 | 1 | 25 | M51 | 2 | 52 |
| M26 | 1 | 26 | M51A | 2 | 53 |
| H27 | 1 | 27 | H52 | 2 | 54 |

| COMPONENT | DISK NO. | PLOT NO. | COMPONENT | DISK NO. | PLOT NO. |
|---|---|---|---|---|---|
| H52A | 2 | 55 | R01 | 3 | 77 |
| M53 | 2 | 56 | R02 | 3 | 78 |
| H54 | 2 | 57 | R03 | 3 | 79 |
| M55 | 2 | 58 | R04 | 3 | 80 |
| M56 | 2 | 59 | R05 | 3 | 81 |
| H57 | 2 | 60 | R06 | 3 | 82 |
| H58 | 2 | 61 | B01 | 3 | 83 |
| H59 | 2 | 62 | B02 | 3 | 84 |
| H60 | 3 | 63 | F01 | 3 | 85 |
| H61 | 3 | 64 | F02 | 3 | 86 |
| H62 | 3 | 65 | F03 | 3 | 87 |
| H63 | 3 | 66 | F04 | 3 | 88 |
| H64 | 3 | 67 | WAND2 | 3 | 89 |
| H65 | 3 | 68 | WOR2 | 3 | 90 |
| H66 | 3 | 69 | WOR3 | 3 | 91 |
| H67 | 3 | 70 | WOR4 | 3 | 92 |
| M68 | 3 | 71 | WOR5 | 3 | 93 |
| H69 | 3 | 72 | WOR6 | 3 | 94 |
| H81 | 3 | 73 | WOR7 | 3 | 95 |
| H82 | 3 | 74 | WOR8 | 3 | 96 |
| A01 | 3 | 75 | PADIN | 3 | 97 |
| A02 | 3 | 76 | PADOUT | 3 | 98 |

## COMPONENT LIST BY FUNCTION

The component filename is the macrocell number plus the extension .SYM; for example, H01.SYM.

GATES

| | |
|---|---|
| H01 | M22 |
| H02 | M23 |
| H03 | M24 |
| H04 | M25 |
| H05 | M26 |
| H06 | H27 |
| H07 | M28 |
| H08 | M29 |
| H09 | M30 |
| H10 | M55 |
| H11 | M56 |
| H12 | H57 |
| M13 | H58 |
| M14 | H59 |
| H15 | H60 |
| H16 | H61 |
| H17 | H62 |
| H18 | H63 |
| M19 | H64 |
| M20 | H65 |
| M21 | H66 |

FLIP-FLOPS

| | |
|---|---|
| H31 | Dual D F/F |
| M32 | D F/F with Mux |
| H81 | Dual D F/F with Diff, Clock and Data |
| H82 | Dual D F/F with Set and Reset |

## LATCHES

| | |
|---|---|
| H33 | Dual 2 Bit Latch |
| H34 | Dual Latch with Mux |
| H35 | Quad Latch |
| H67 | Dual Latch |

## MULTIPLEXERS

| | |
|---|---|
| M36 | 4 to 1 Mux with Enable |
| M37 | 4 to 1 Mux with Enable |
| M38 | 4 to 1 Mux with Enable |
| M39 | 4 to 1, 2 to 1 Mux |
| H40 | Quad 2 to 1 Mux, Com Sel |
| H41 | Quad 2 to 1 Mux |
| H42 | Quad 2 to 1 Mux with Enable |
| H43 | Dual 2 to 1 Mux |
| M68 | 4 to 1 Mux |
| H69 | Dual 2 to 1 Mux |

## DECODERS

| | |
|---|---|
| M44 | 1/4 Decoder (High) |
| M45 | 1/4 Decoder (Low) |
| M46 | 1/4 Decoder (High) |
| M47 | 1/4 Decoder (Low) |

## ADDERS

| | |
|---|---|
| M50 | Full Adder |
| M50A | Full Adder |
| M51 | Full Adder |
| M51A | Full Adder |
| H52 | Dual Full Adder |
| H52A | Dual Full Adder |
| M53 | Full Adder and Half Adder |
| H54 | Dual Half Adder |

## MISCELLANEOUS FUNCTIONS

| | |
|---|---|
| M48 | Priority Encoder |
| M49 | Priority Expander |

## MCA500ALS INPUT CELLS

A01
A02

## MCA500ALS OUTPUT CELLS

R01
R02
R03
R04
R05
R06

## MCA1300ALS INPUT CELLS

B01
B02

## MCA1300ALS OUTPUT CELLS

F01
F02
F03
F04

## SPECIAL COMPONENTS

| | |
|---|---|
| WAND2 | 2 Input Wired-AND |
| WOR2 | 2 Input Wired-OR |
| WOR3 | 3 Input Wired-OR |
| WOR4 | 4 Input Wired-OR |
| WOR5 | 5 Input Wired-OR |
| WOR6 | 6 Input Wired-OR |
| WOR7 | 7 Input Wired-OR |
| WOR8 | 8 Input Wired-OR |
| PADIN | Input Pad |
| PADOUT | Output Pad |

## COMPONENT PIN SEQUENCES

The component filename is the macrocell number plus the extension .SYM; for example, H01.SYM.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| H01: | Y' | Y | Z | Z' | A | B | C | | |
| | D | E | F | G | | | | | |
| H02: | Y | Y' | Z' | Z | A | B | C | | |
| | D | E | F | G | | | | | |
| H03: | Y | Y' | Z' | Z | A | B | C | | |
| | D | E | F | G | | | | | |
| H04: | Y' | Y | Z | Z' | B | C | A | D | E |
| H05: | Y | Y' | A | B | C | D | E | F | G |
| H06: | Y | Y' | A | B | C | D | E | F | |
| H07: | Y | B | C | A | D | E | F | | |
| H08: | Y | B | C | A | D | E | F | | |
| H09: | Y' | Y | A | B | C | D | | | |
| H10: | Y | Y' | A | B | C | | | | |
| H11: | Y | A | B | C | D | | | | |
| H12: | Y | A | B | C | D | | | | |
| M13: | Y | Y' | A | B | C | D | E | | |
| | F | G | H | I | J | K | L | | |

M14: Y' Y A B D E G
H J K C F I L

H15: Y Y' A B C D E F

H16: Y' Y A B C D E F

H17: Y Y' A B C D E F G

H18: Y A B C D E

M19: Y Z A B C D E
F G H

M20: Y Y' A B C D E
F G H I J K L

M21: Y Y' A B C D E
F G H I J K L

M22: Y Y' A B C D E
F G H I J K L

M23: Z Y' Y Z' A B C D
E F G H I J K

M24: Y Y' A B C D E F
G H I J K L M N

M25: Y Y' A B C D E F
G H I J L M N

M26: Y' Y A B C D E
F G H I J K L

H27: Y Y' A B C D E

M28: Y' Z' Y Z A B C D
E F G H I J K L

M29: Y' Y A B C D E
L F G H I J K

M30: Z' Y Z Y' A B C D
E F G H I J K

H31: Q Q' C1 C2 D R

M32: Q Q' C1 C2 D0 D1 S R

H33: Q0' Q0 Q1 Q1' E1 E2 D0 D1 R

H34: Q D0 D1 S E1 E2 R

H35: Q0' Q0 Q1 Q1' D0 D1 E0 E1

M36: Y A0 A1 A2 A3 S0 S1 E

M37: Y A0 A1 A2 A3 S0 S1 E

M38: Y A0 A1 A2 A3 S0 S1 E

M39: Y Z' Z A0 A1 A2 A3 B0
B1 S S0 S1

H40: Y Y' Z' Z S1 S2 A0 A1
B0 B1

H41: Y Y' Z' Z A0 A1 B0 B1
SA SB

H42: Y Z A0 A1 B0 B1 E S

H43: Y' Y A0 B0 A1 B1 S

M44: Y2 Y3 Y1 Y0 A0 A1 E

M45: Y3 Y2 Y0 Y1 A0 A1 E

M46: Y3 Y1 Y0 Y2 A0 A1 E

M47: Y3 Y2 Y0 Y1 A0 A1 E

M48: Y1 Y2 Y0 D0 D1 D2 D3

M49: Y1 Y2 Y3 Y0 H2 L0 L1
L2 H0 H1

M50: CO S B1 B2 A CI

M50A: CO S B1 B2 A CI

M51: S CO B1 B2 A CI

M51A: S CO B1 B2 A CI

H52: S CO B1 B2 A CI

H52A: S CO B1 B2 A CI

M53: P H1 H0 CO G A0
B0 A1 B1 CI

H54: CO S A1 A2 B1 B2

M55: Y A B C D E
F G S

M56: Y A B C D E
F G H I S

H57: Y A B C D

H58: Y A B C D

H59: Y' Y Z Z' A B
C D E F G H

H60: Y Y' Z' Z A B
C D E F G H

H61: Y Y' Z' Z A B
C D E F G H

H62: Y' Y Z Z' A B
C D E F

H63: Y' Y A B C D

H64: Y Y' A B C D

H65: Y Y' A B C D

H66: Y' Y A B C

H67: Q' Q D E

M68: Y A0 A1 A2 A3 S0 S1

H69: Y Y' A0 A1 SA

H81: Q Q' C+ C- D+ D- R1 R2

H82: Q' Q C1 C2 D R S

A01: Y' Y A B

A02: Y' Y A B C

R01: Y A B C E

R02: Y A B C E

R03: Y A B C E

R04: Y A B C E

R05: Y A B C

R06: Y A B C

B01: Y' Y A B

B02: Y Y' A B C

F01: Y A B C E

F02: Y A B C

F03: Y A B C E

F04: Y A B C

WAND2: O I1 I2

WOR2: O I1 I2

WOR3: O I1 I2 I3

WOR4: O I1 I2 I3 I4

WOR5: O I1 I2 I3 I4 I5

WOR6: O I1 I2 I3 I4 I5 I6

WOR7: O I1 I2 I3 I4 I5 I6 I7

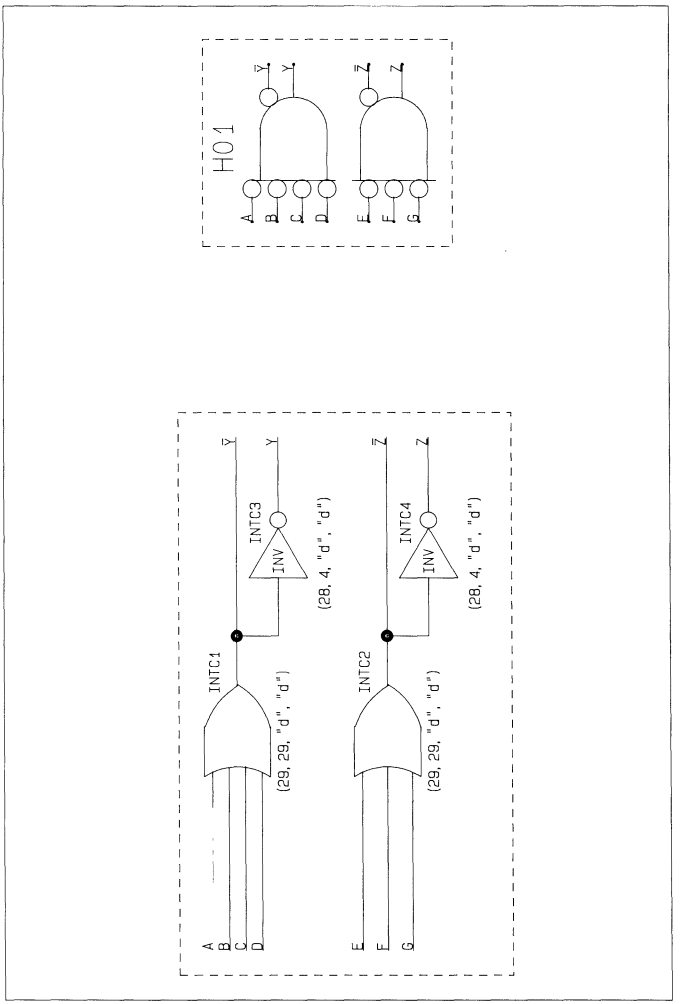
WOR8: O I1 I2 I3 I4 I5 I6 I7
I8

PADIN: OUT IN

PADOUT: OUT IN

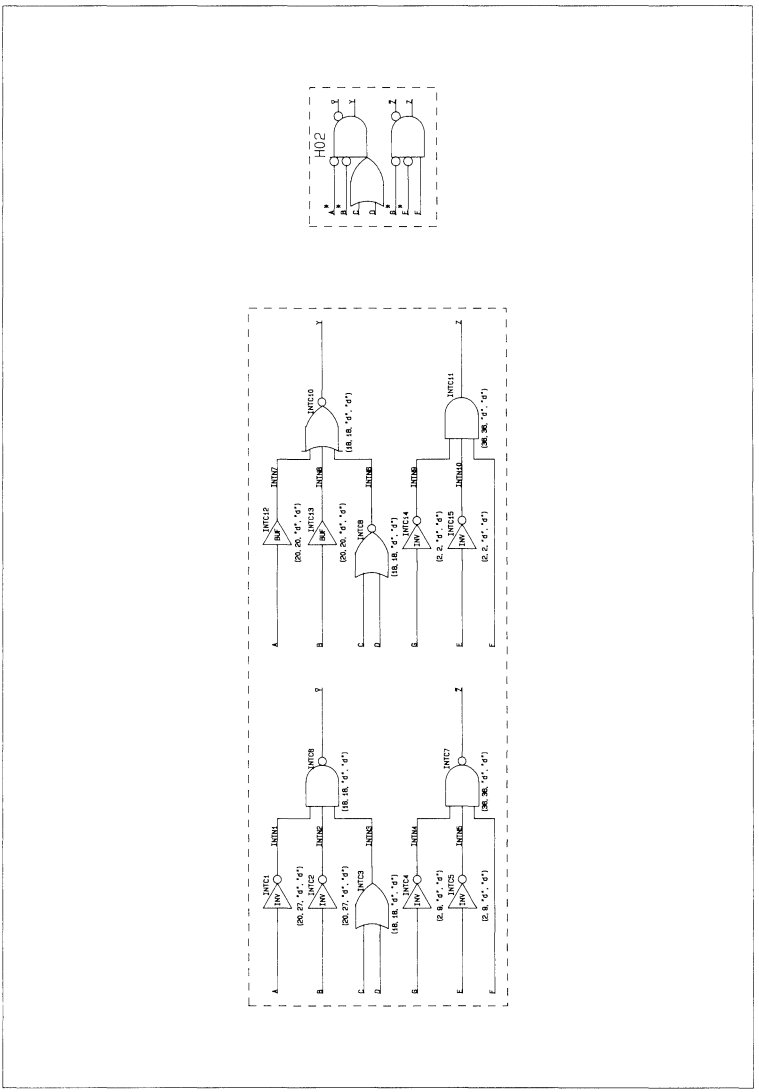
COMPONENT PLOTS

Plot 1



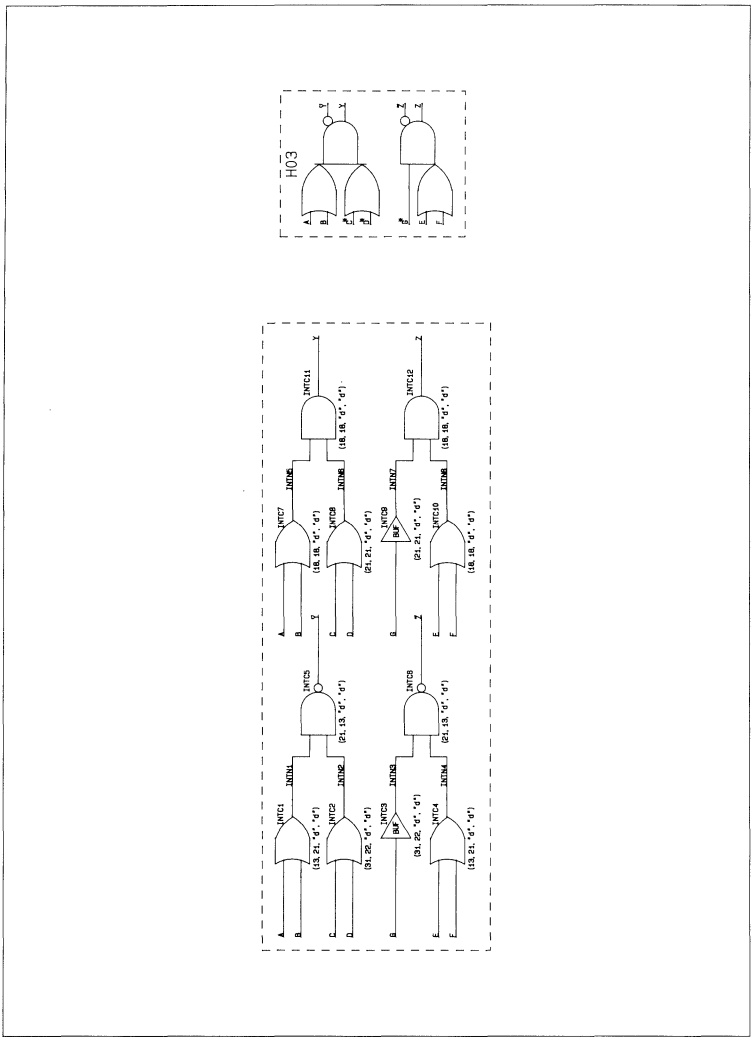
COMPONENT PLOTS

Plot 2



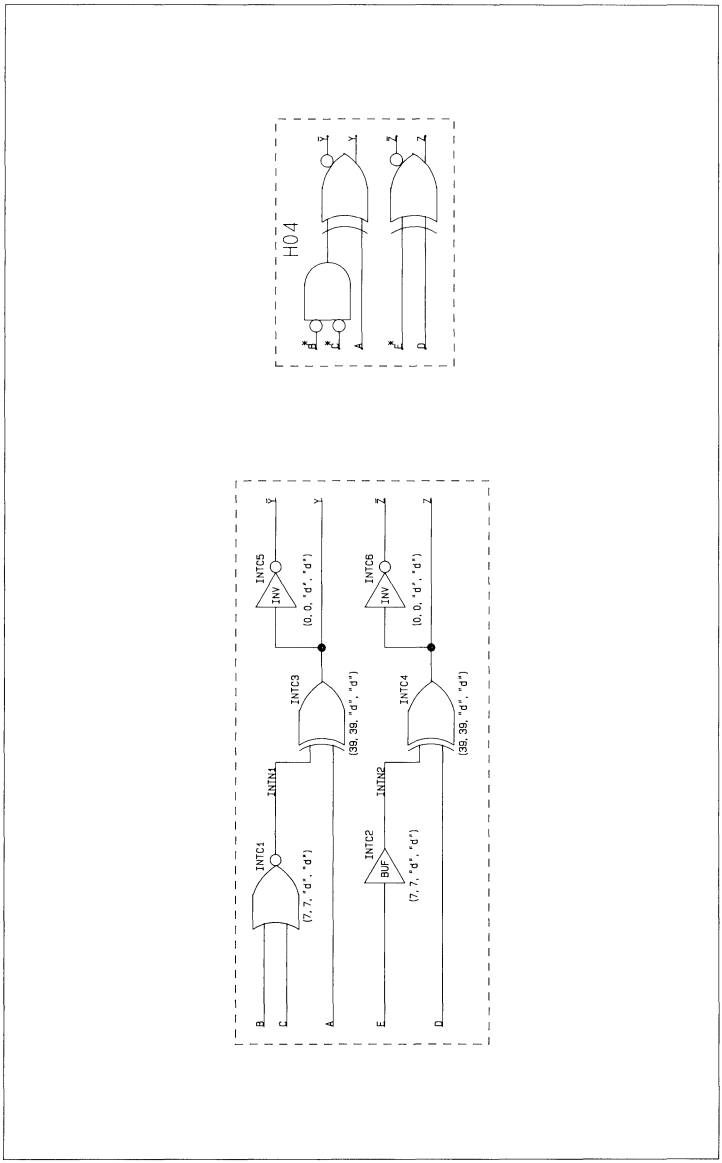
COMPONENT PLOTS

Plot 3



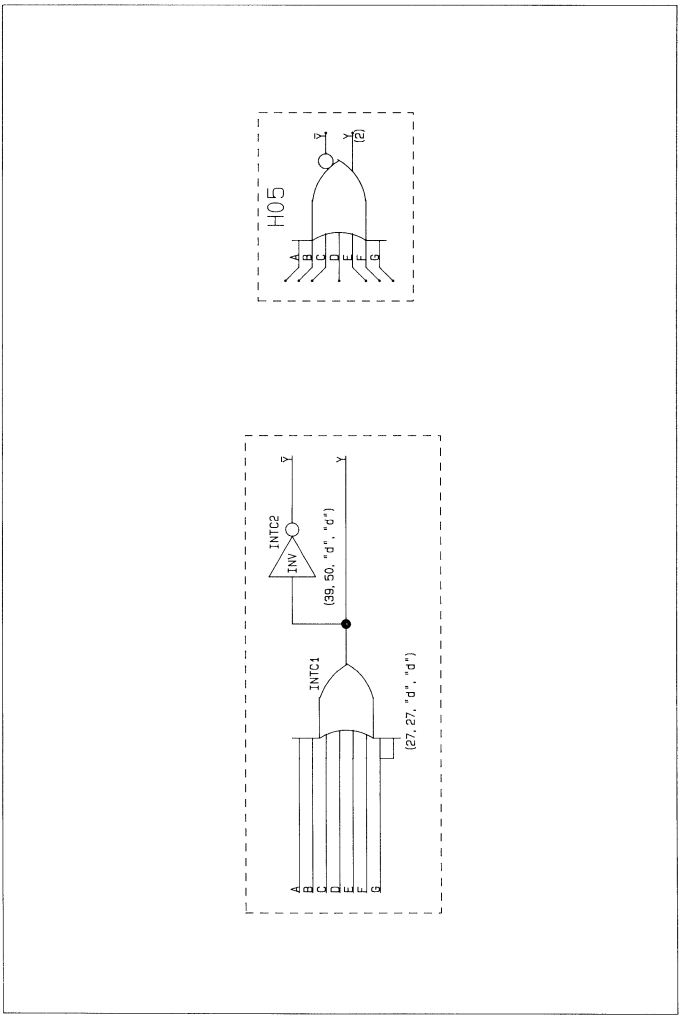
COMPONENT PLOTS

Plot 4



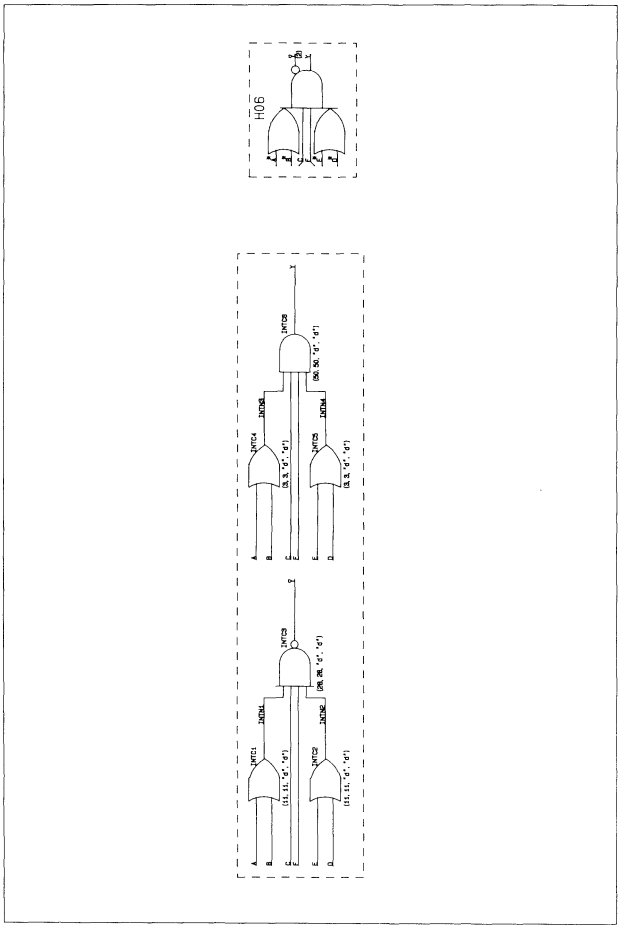
COMPONENT PLOTS

Plot 5



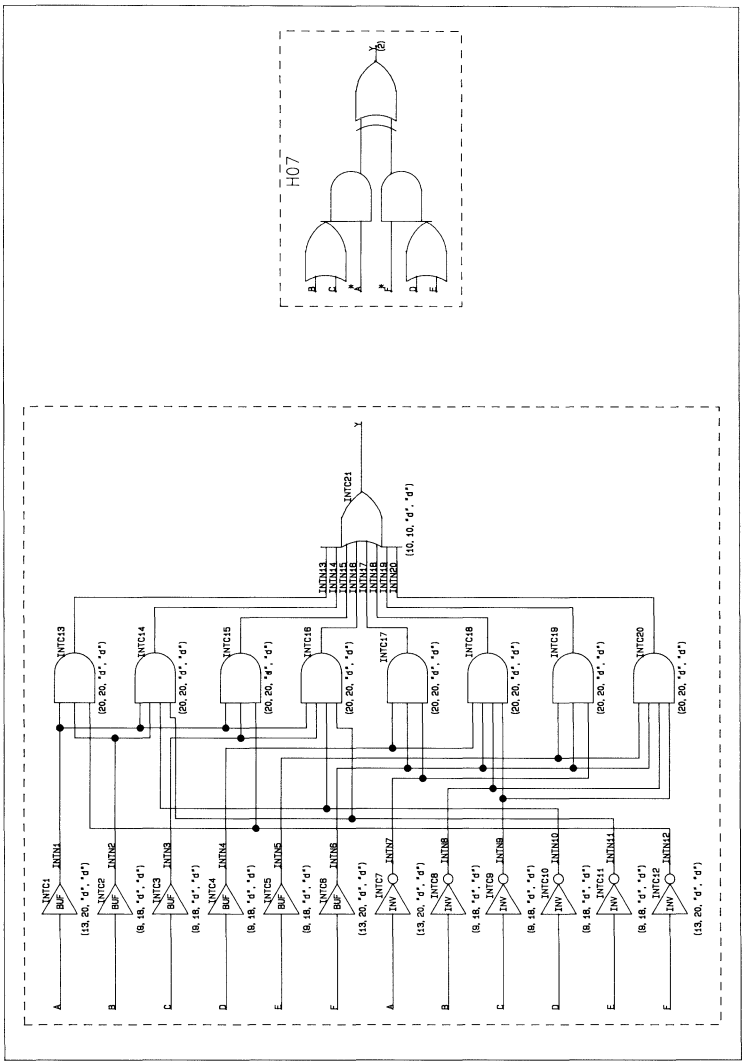
COMPONENT PLOTS

Plot 6



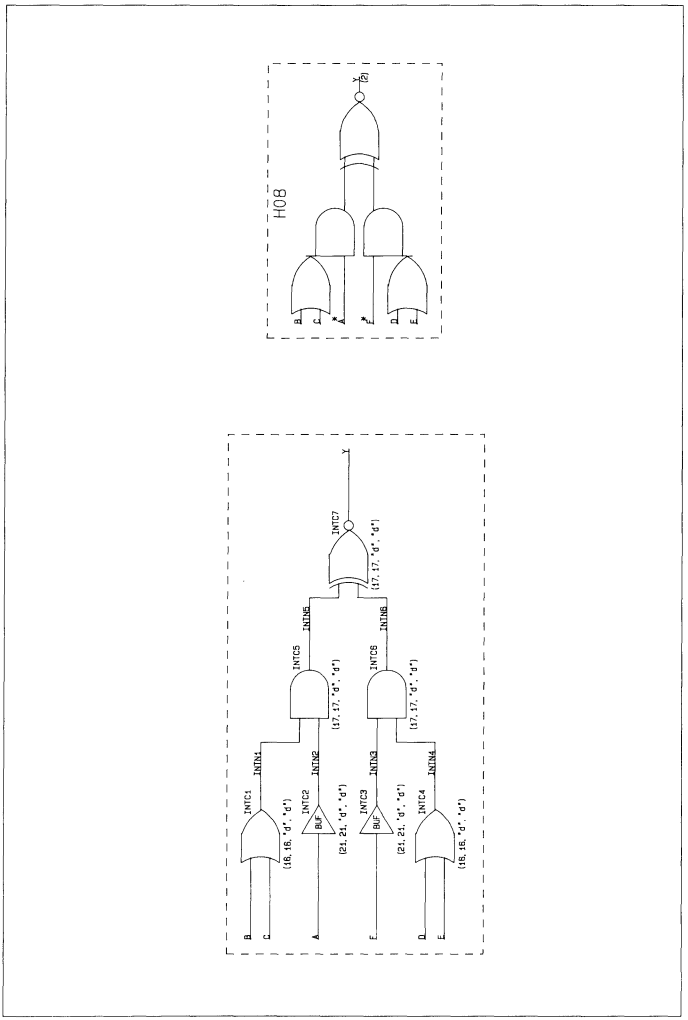
## COMPONENT PLOTS

Plot 7



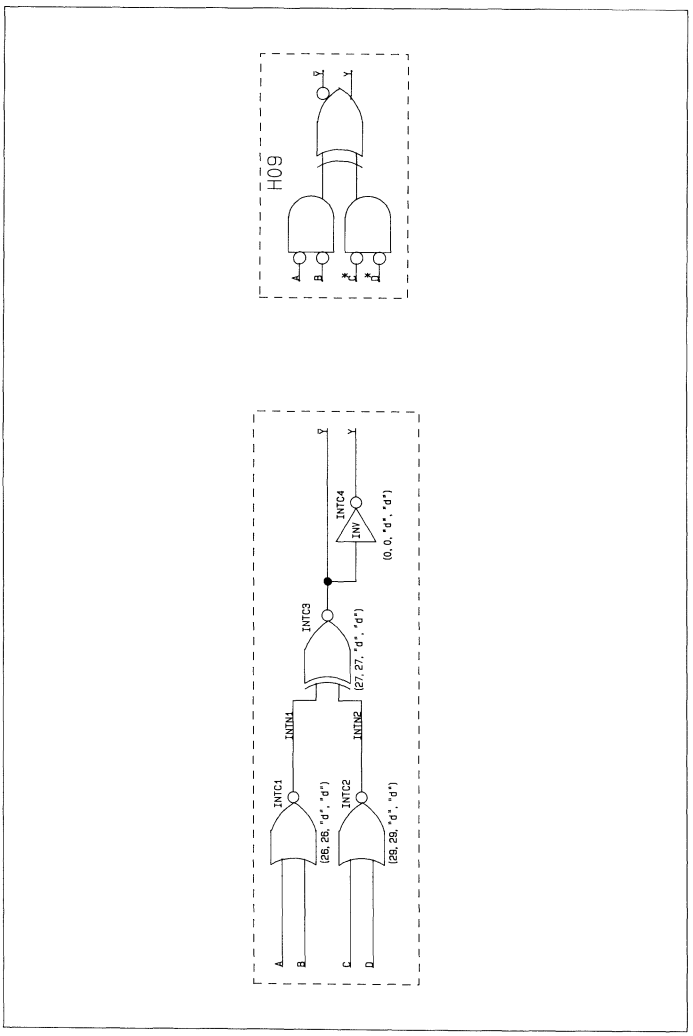
COMPONENT PLOTS

Plot 8



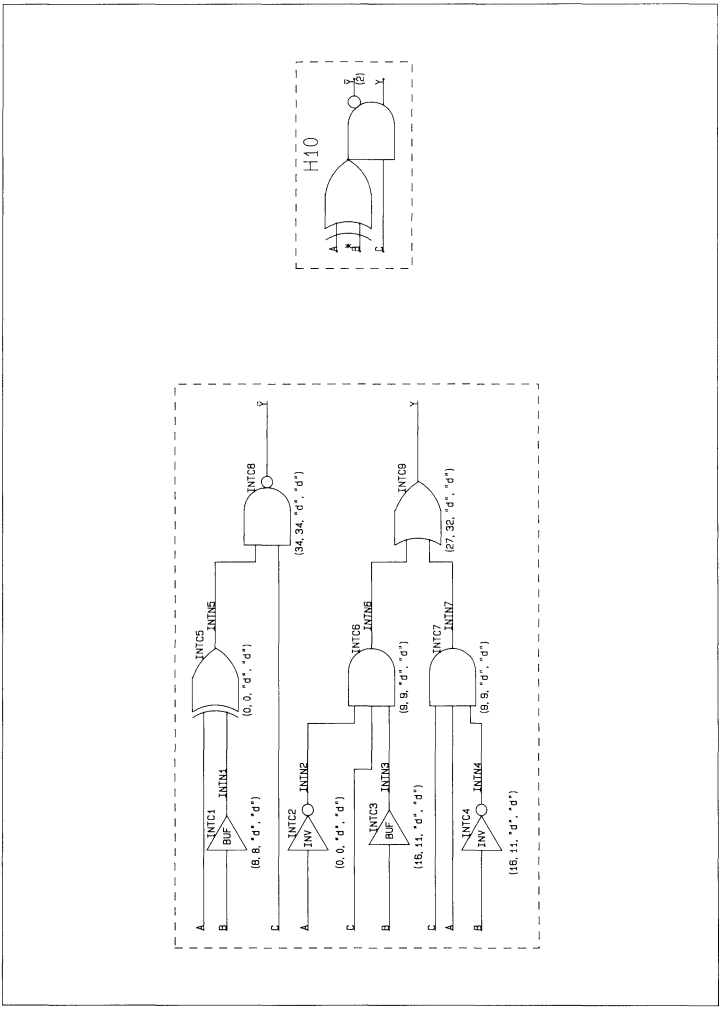
COMPONENT PLOTS

Plot 9



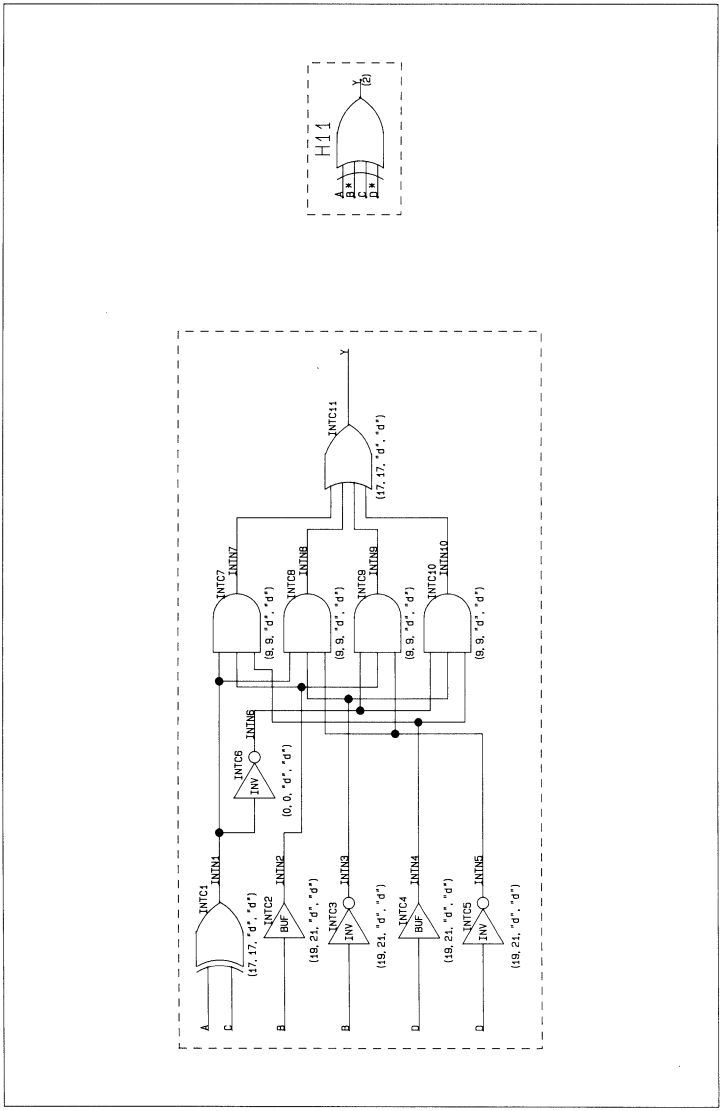
COMPONENT PLOTS

Plot 10



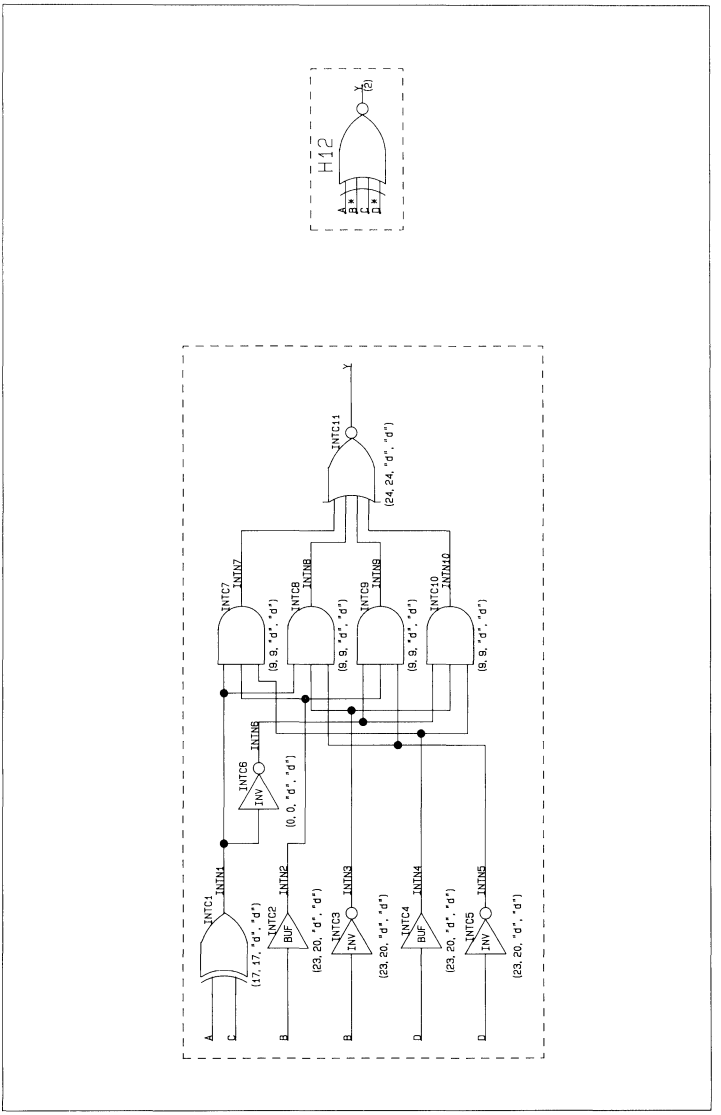
COMPONENT PLOTS

Plot 11



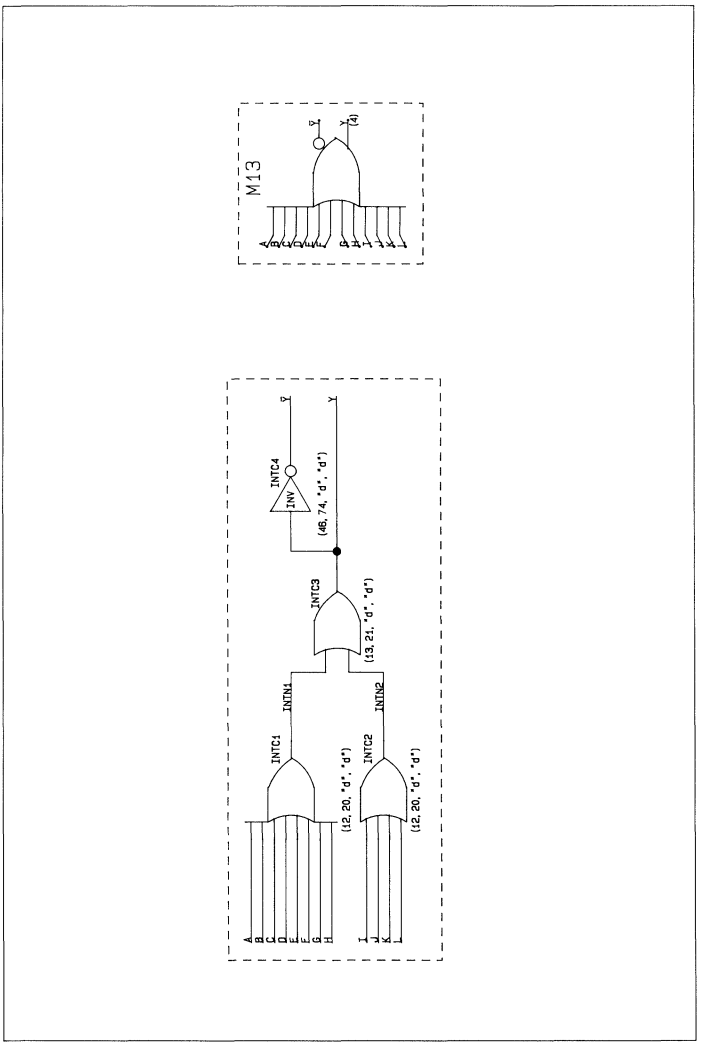
COMPONENT PLOTS

Plot 12



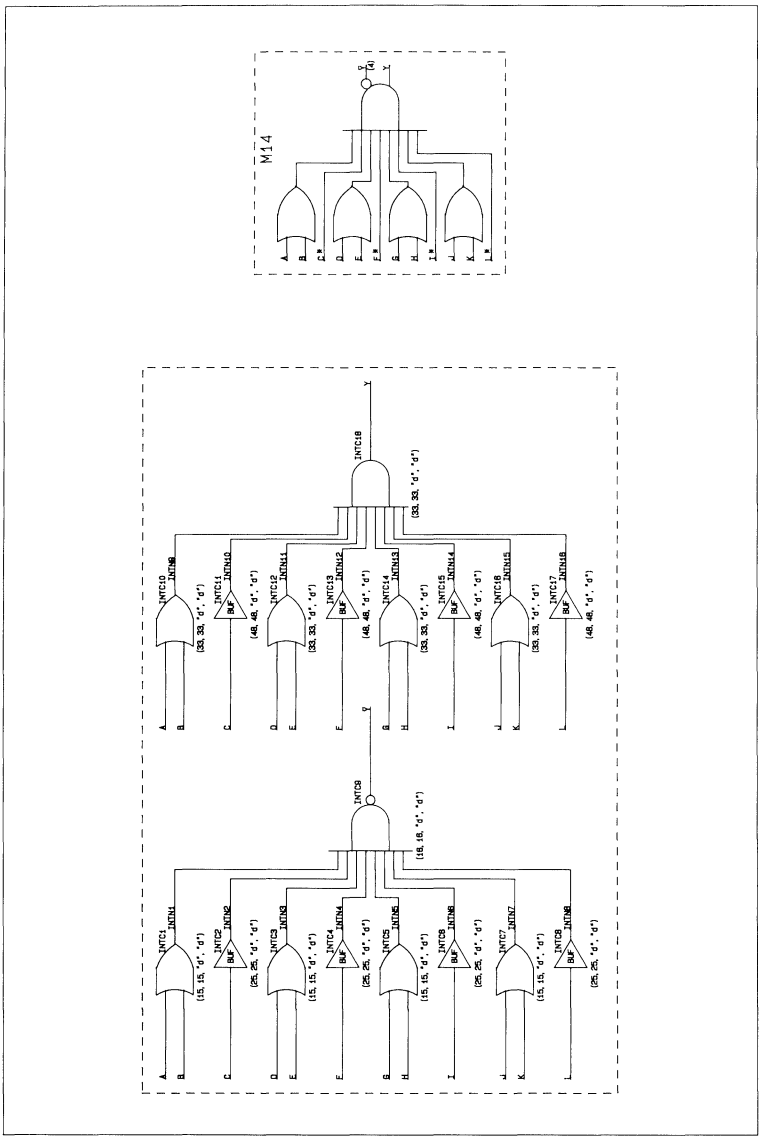
COMPONENT PLOTS

Plot 13



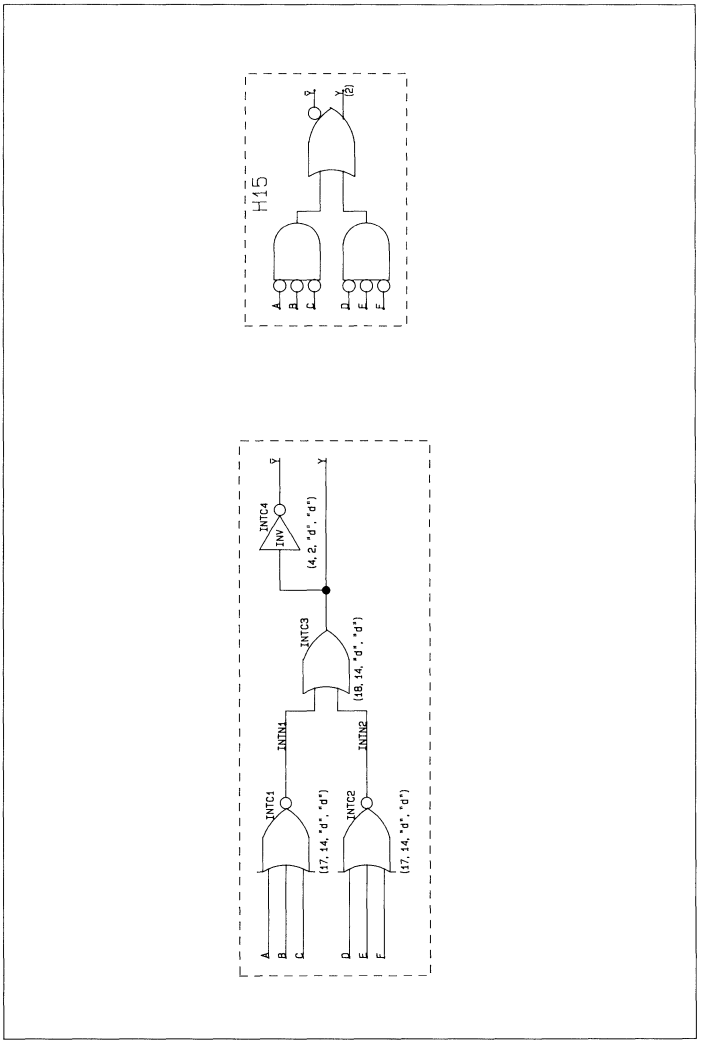
COMPONENT PLOTS

Plot 14



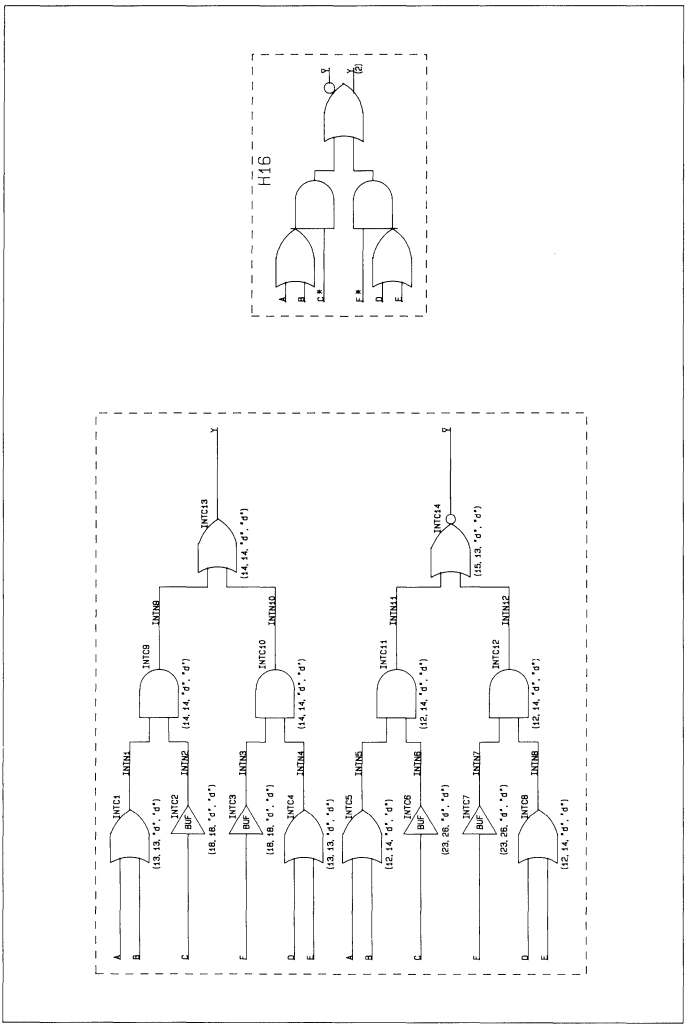
COMPONENT PLOTS

Plot 15

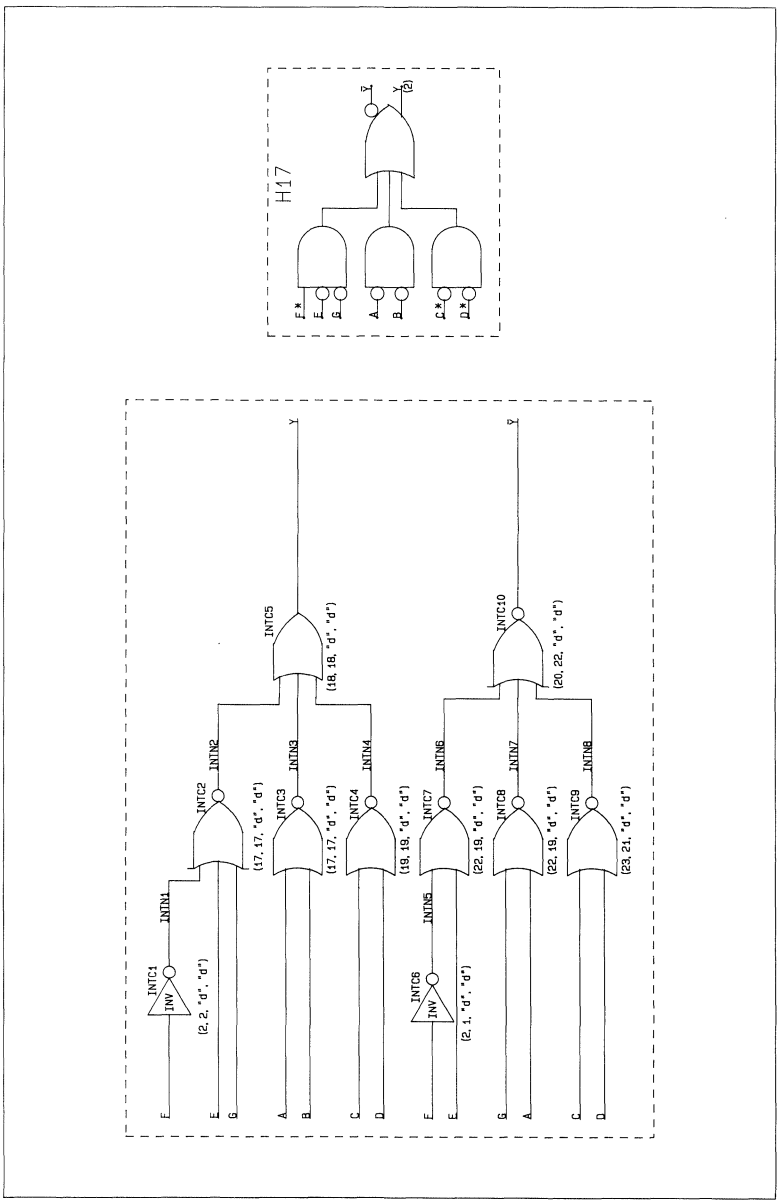


COMPONENT PLOTS

Plot 16



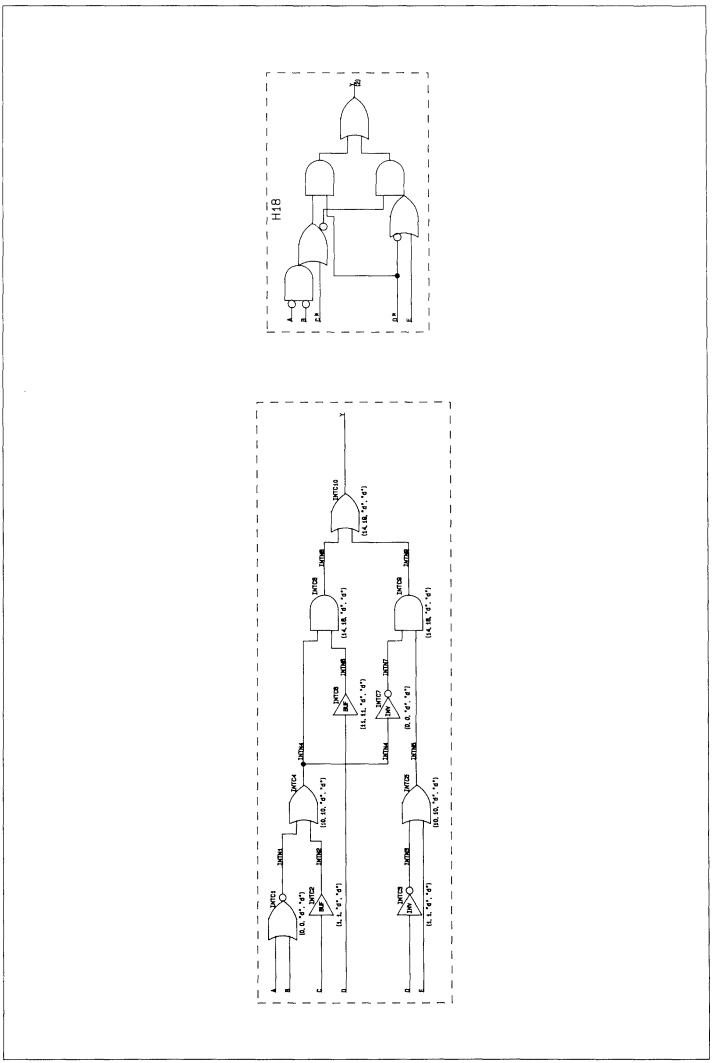
COMPONENT PLOTS Plot 17




000-0139-00

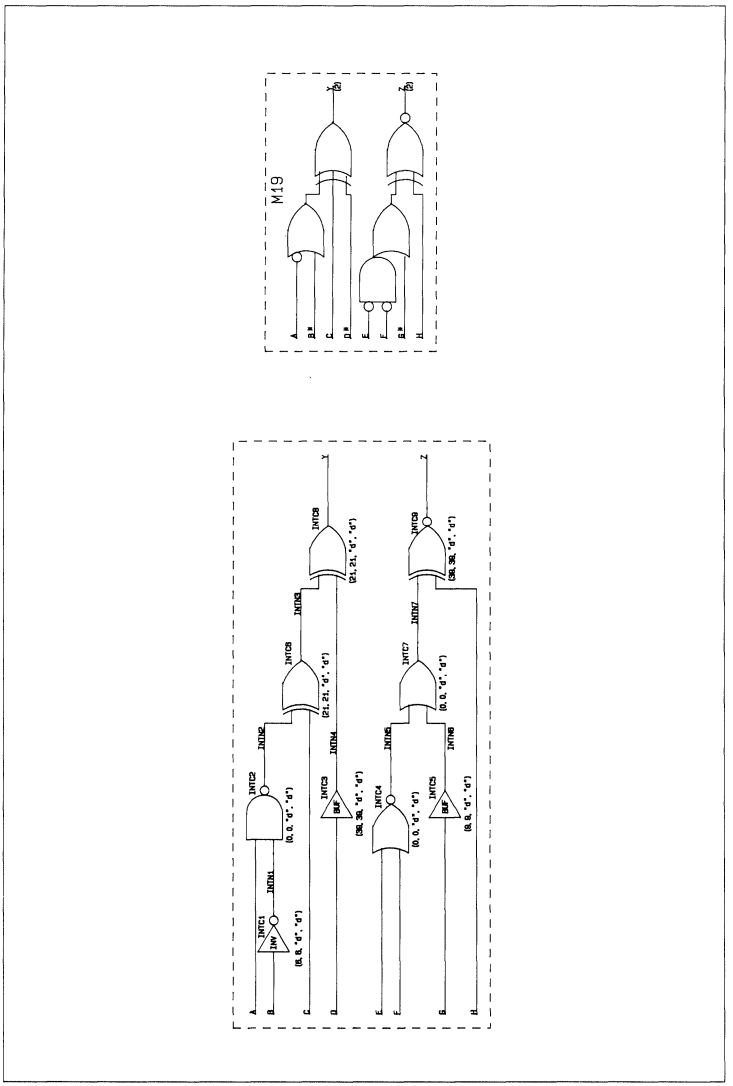
COMPONENT PLOTS

Plot 18



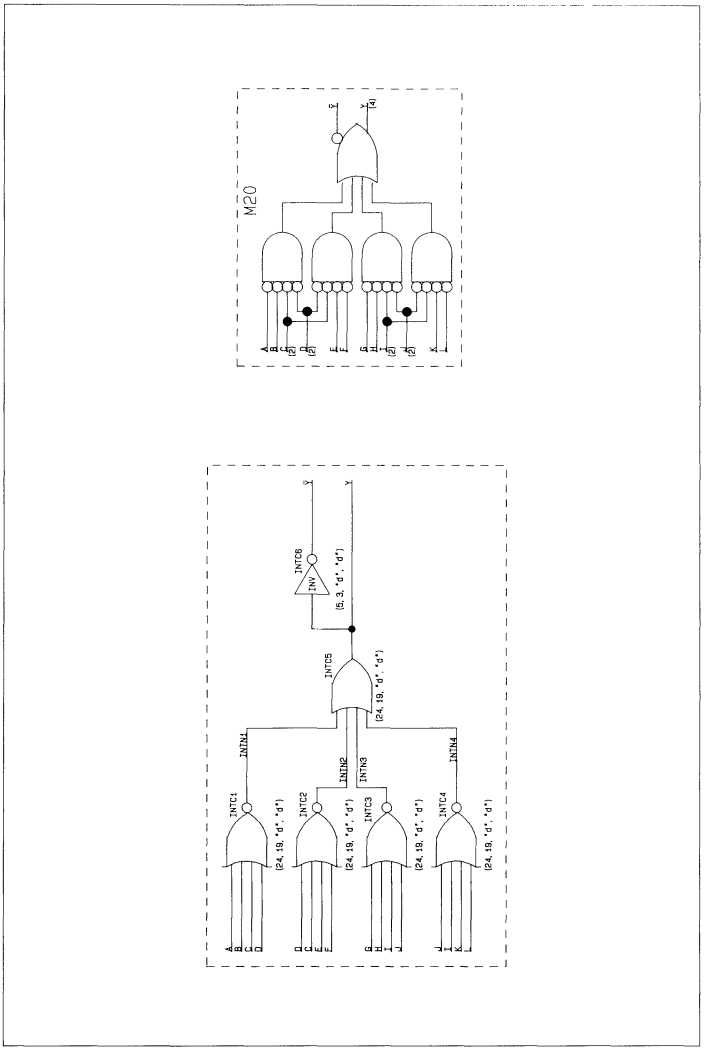
COMPONENT PLOTS

Plot 19



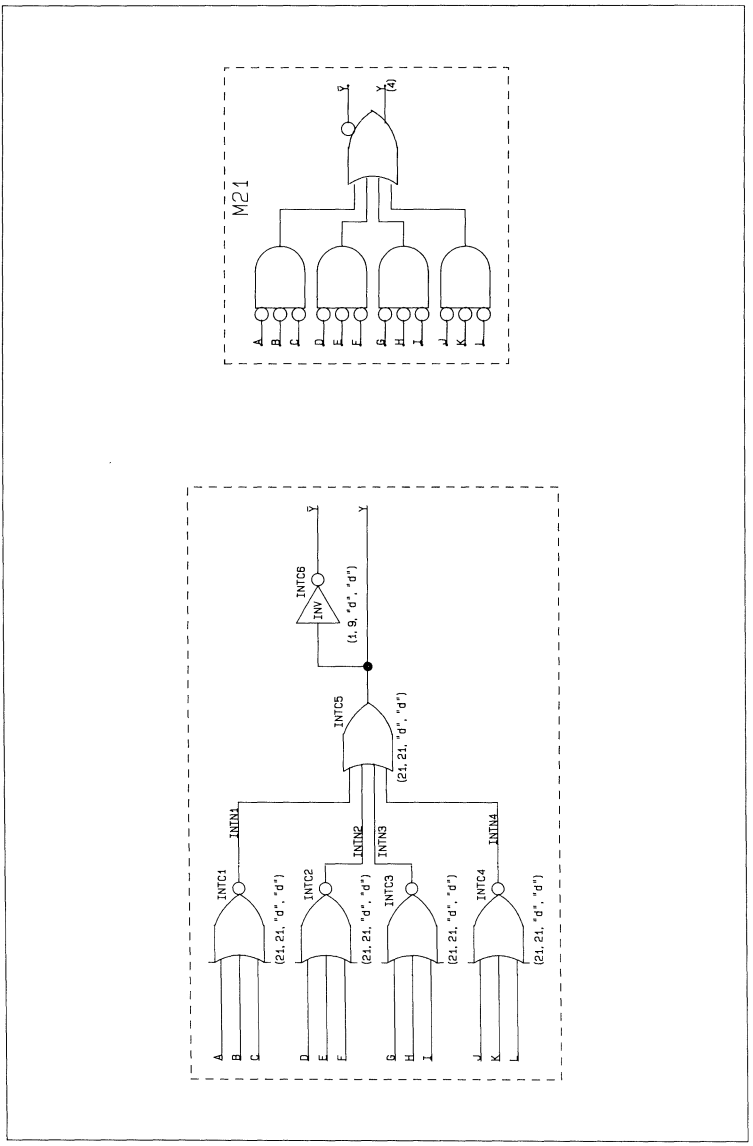
COMPONENT PLOTS

Plot 20



COMPONENT PLOTS

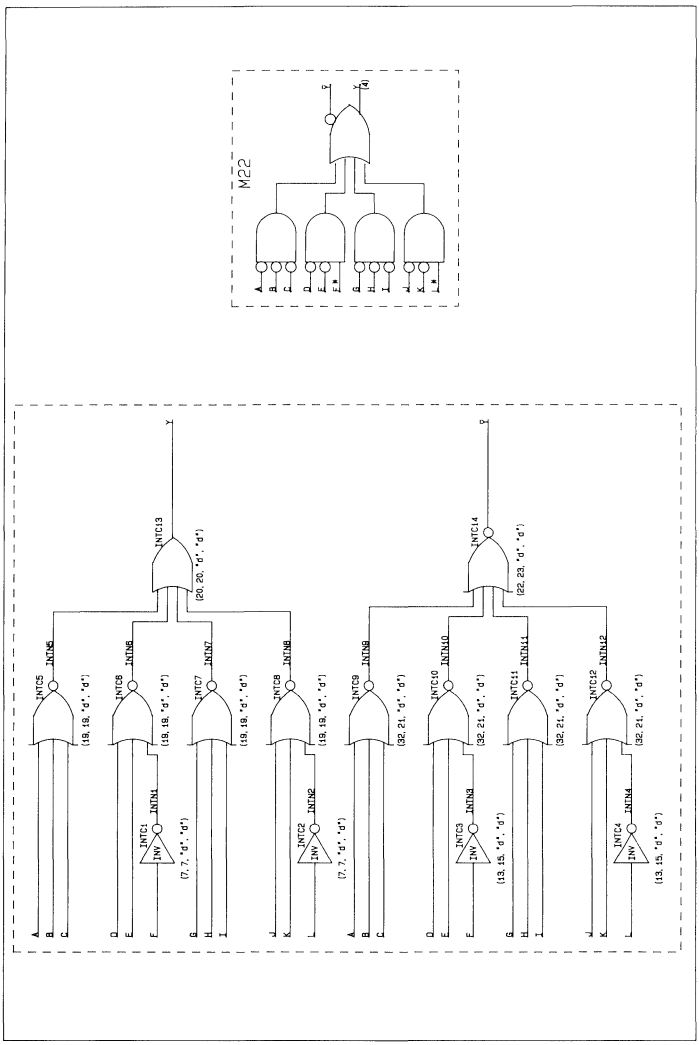
Plot 21




000-0139-00

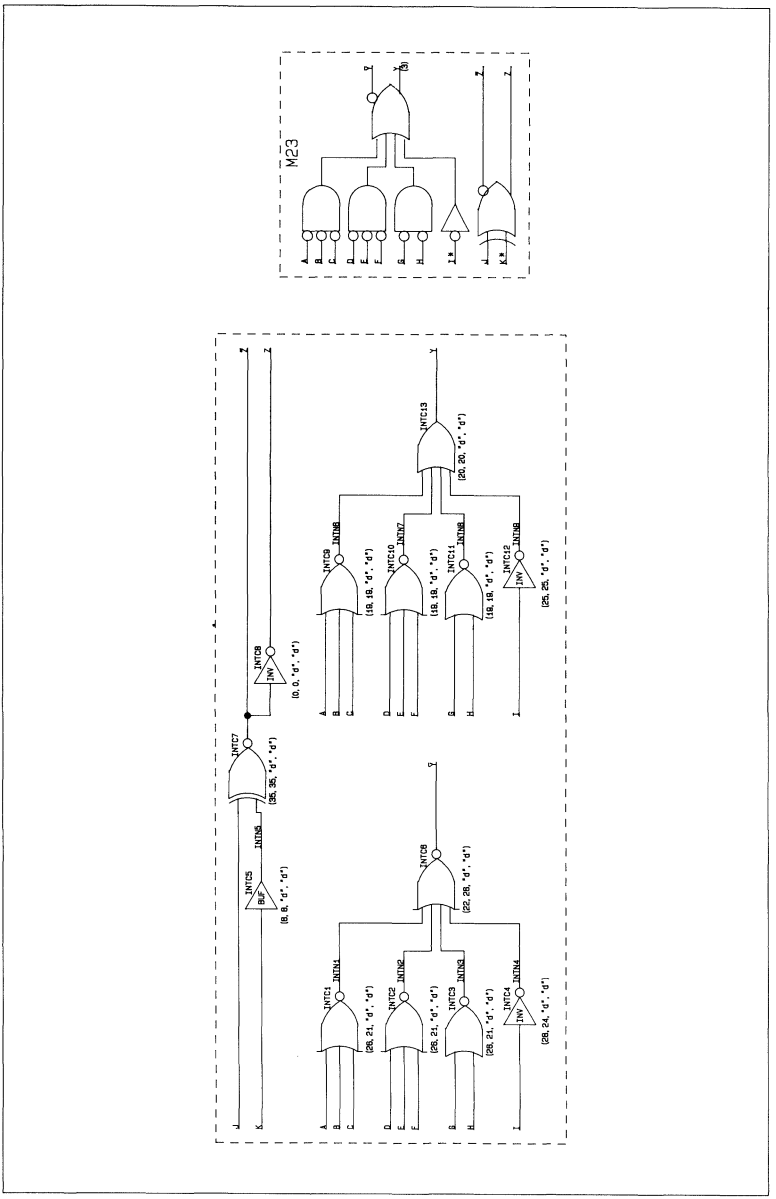
COMPONENT PLOTS

Plot 22



COMPONENT PLOTS

Plot 23

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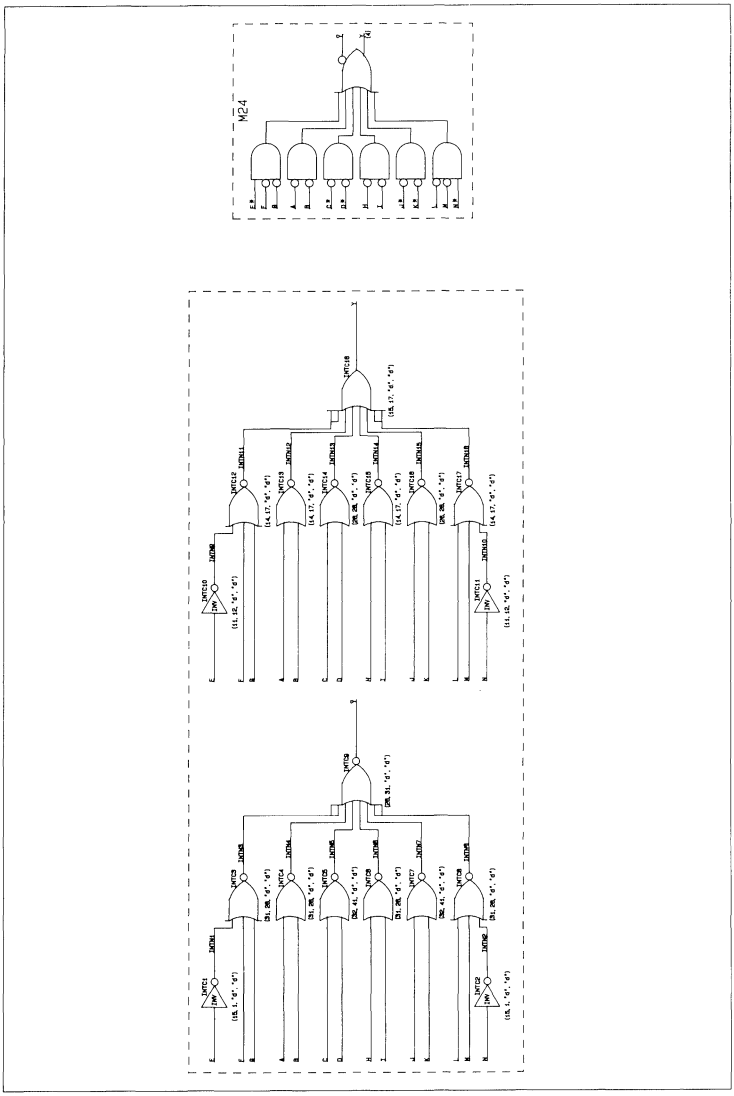
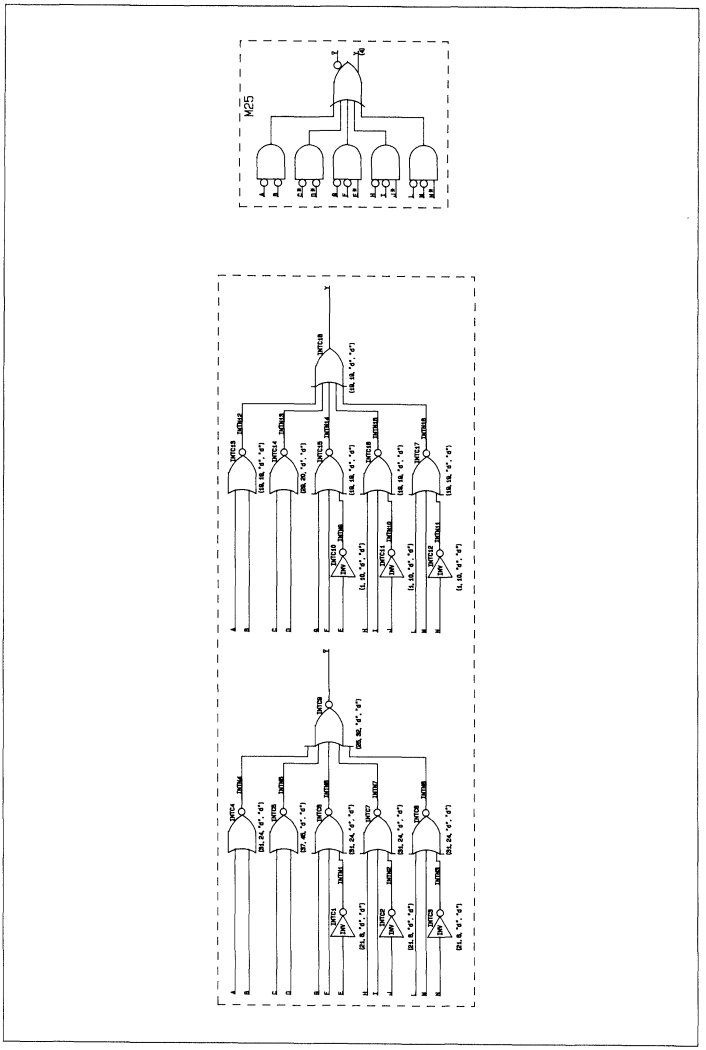
COMPONENT PLOTS

Plot 24



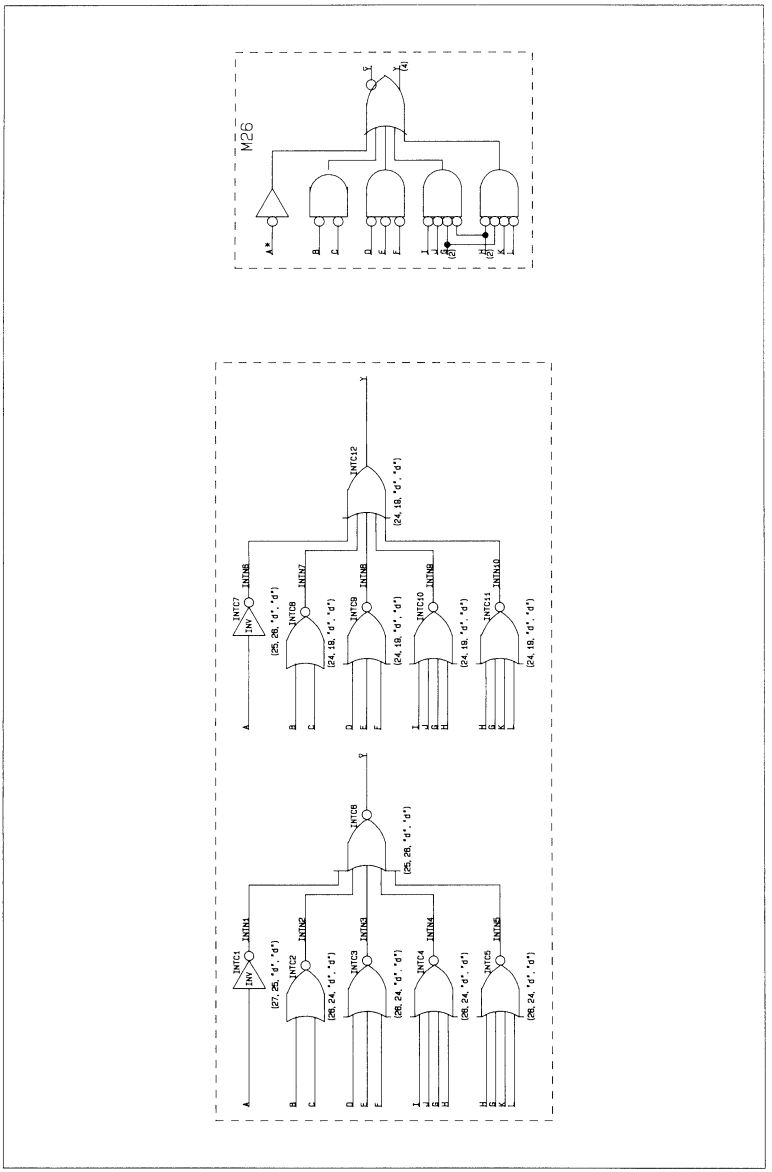
COMPONENT PLOTS

Plot 25



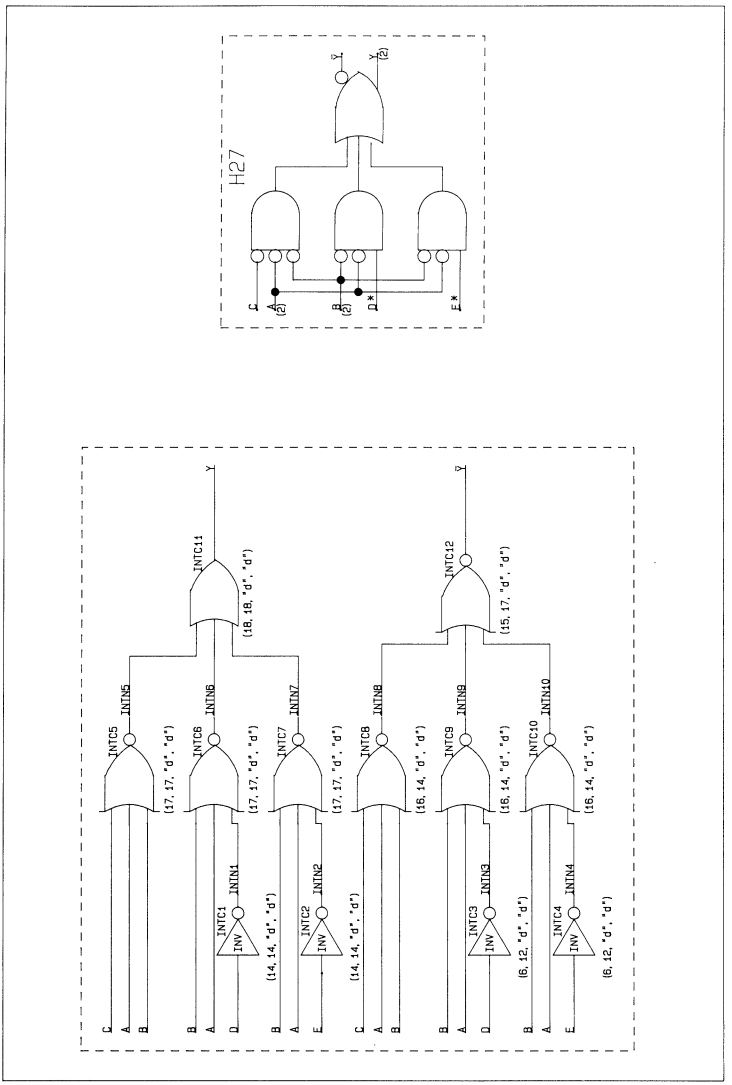
COMPONENT PLOTS

Plot 26



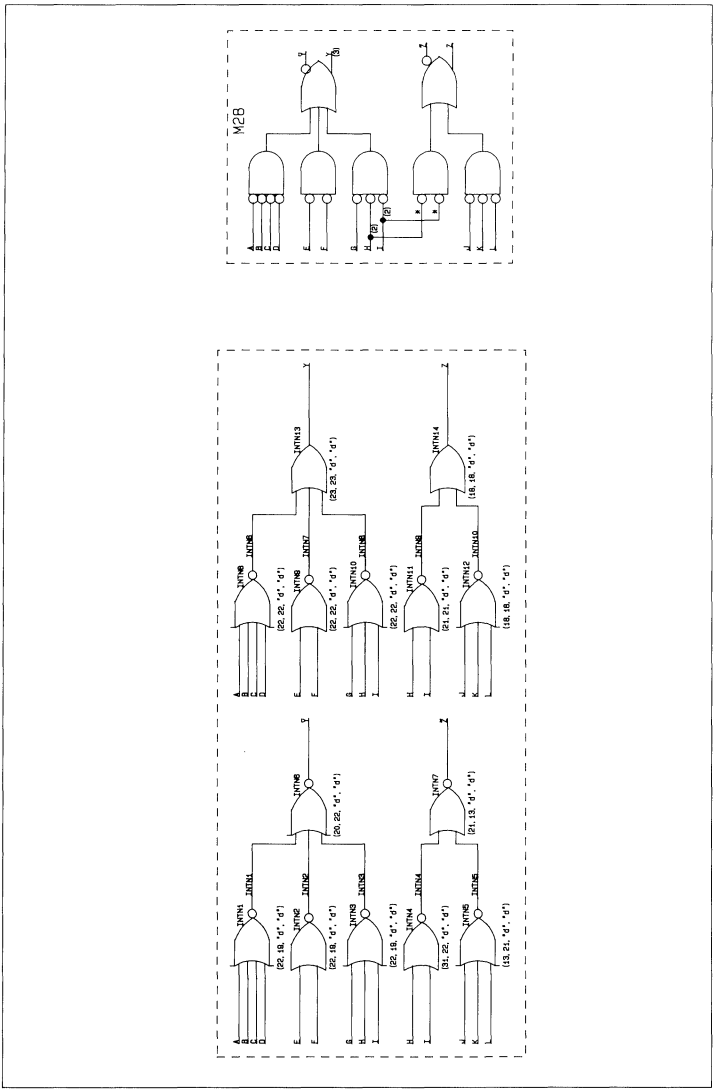
COMPONENT PLOTS

Plot 27



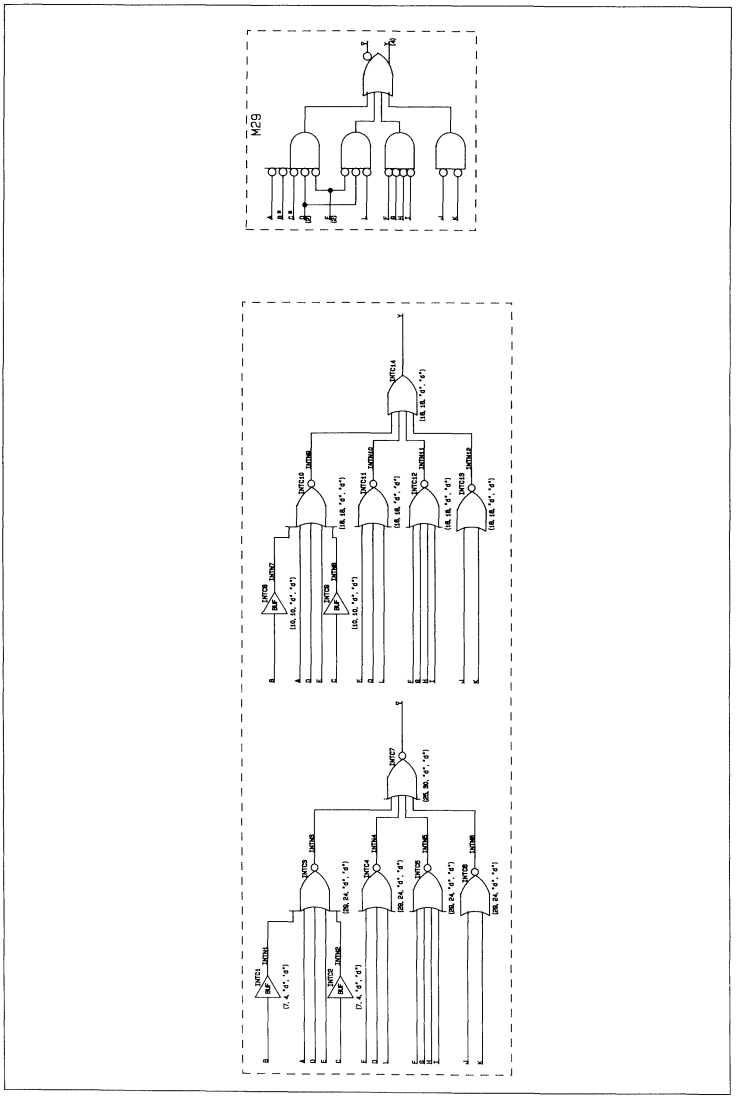
COMPONENT PLOTS

Plot 28



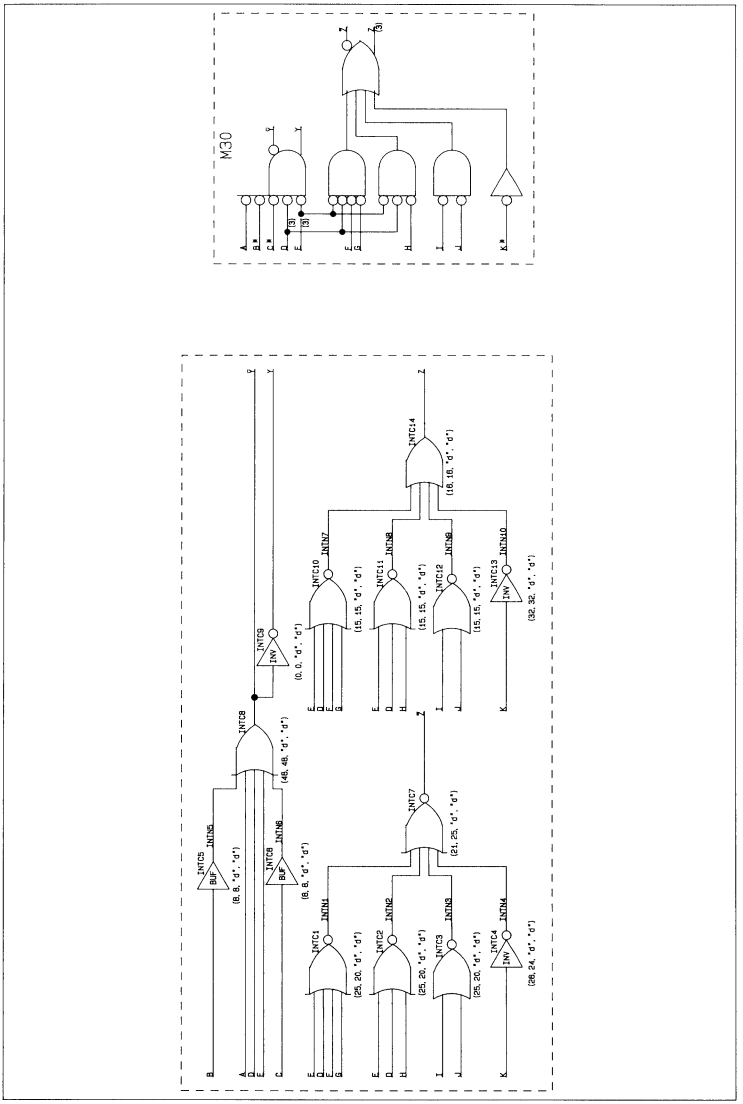
COMPONENT PLOTS

Plot 29



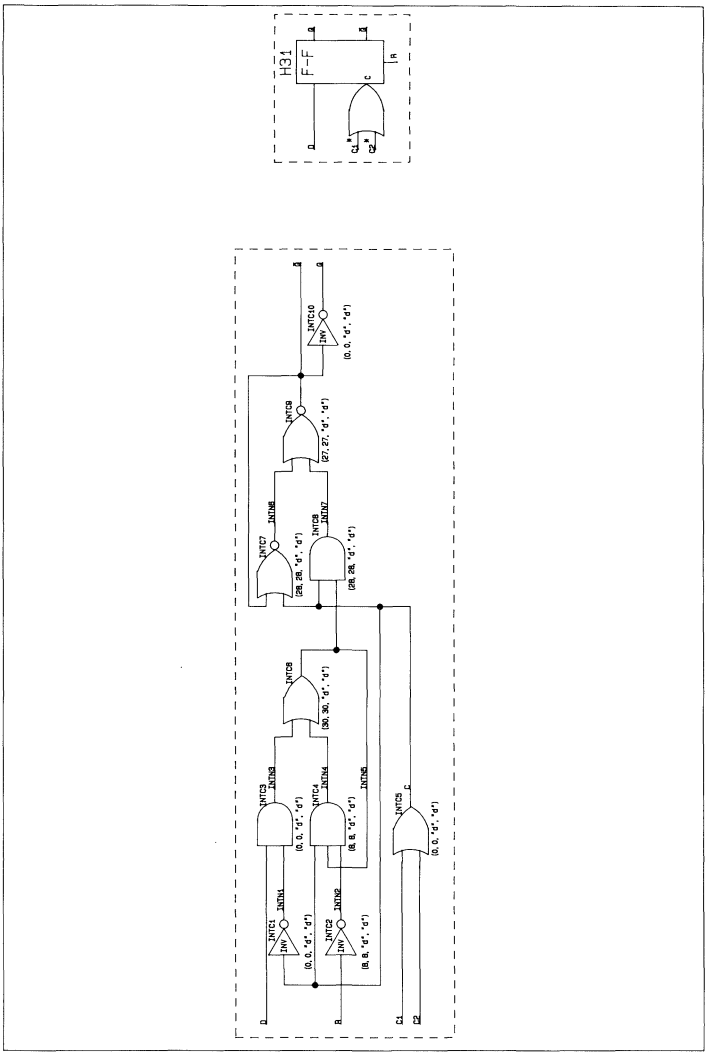
COMPONENT PLOTS

Plot 30



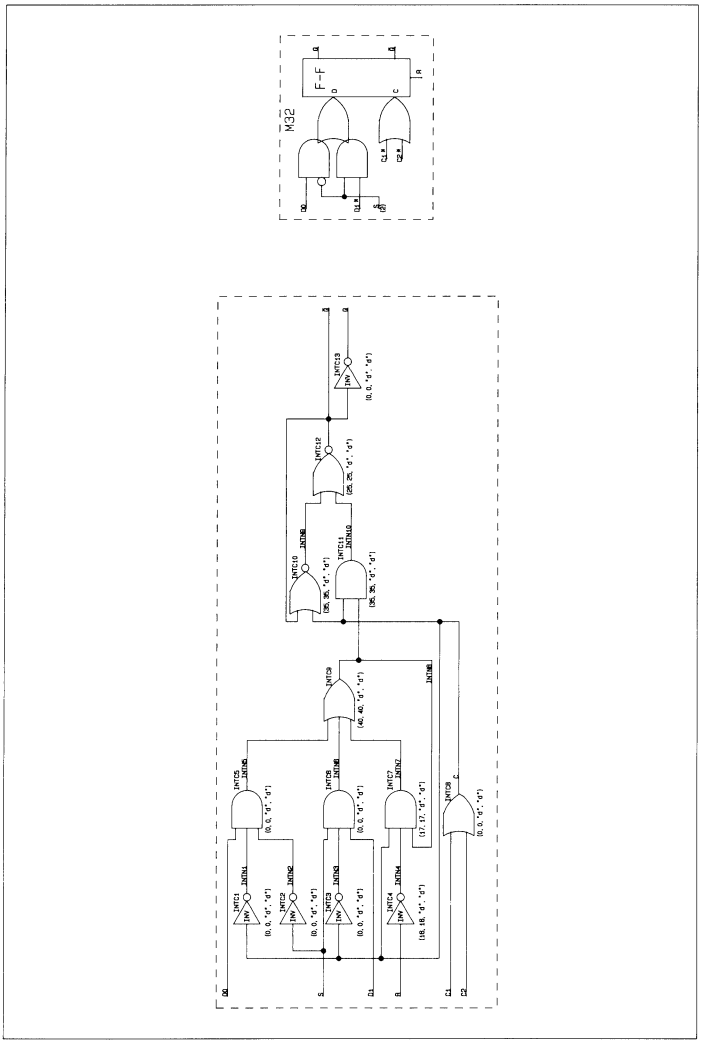
COMPONENT PLOTS

Plot 31



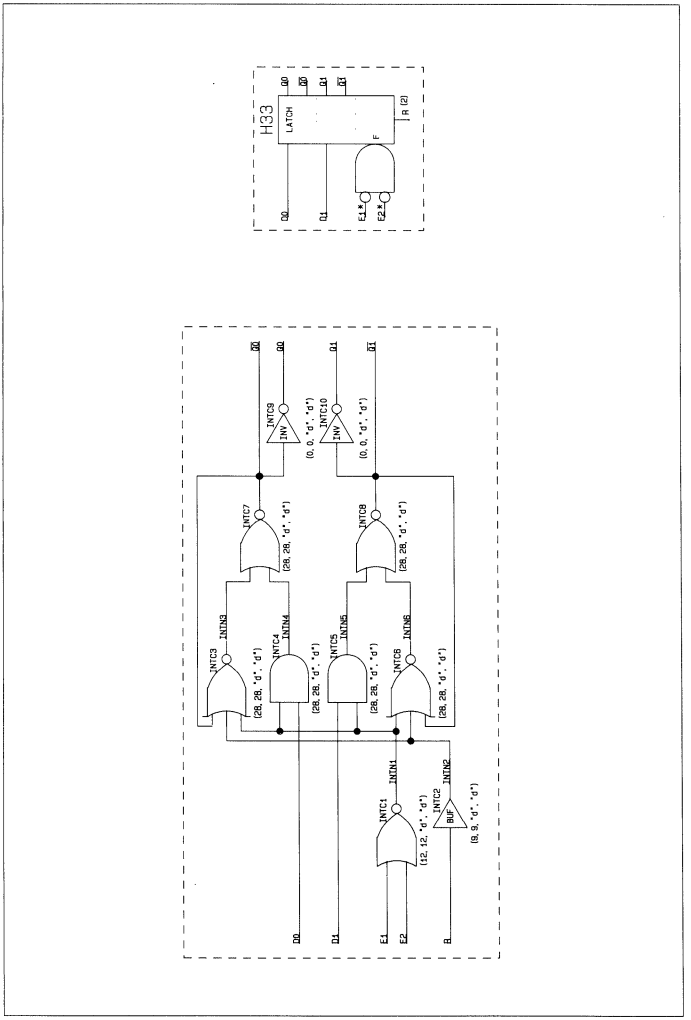
COMPONENT PLOTS

Plot 32



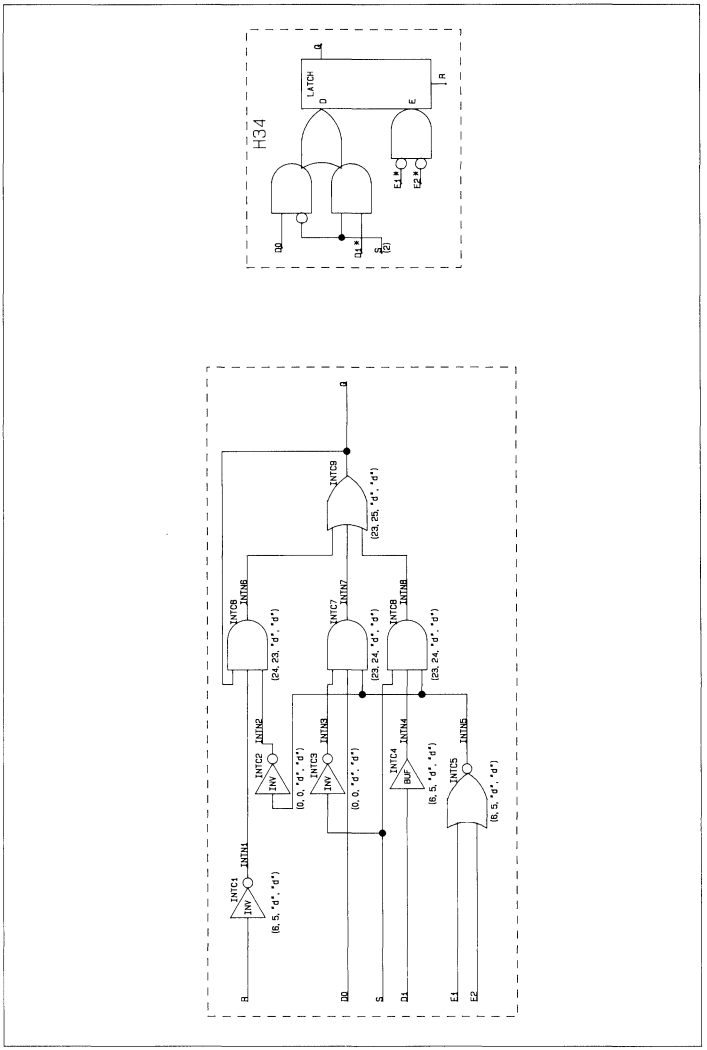
COMPONENT PLOTS

Plot 33



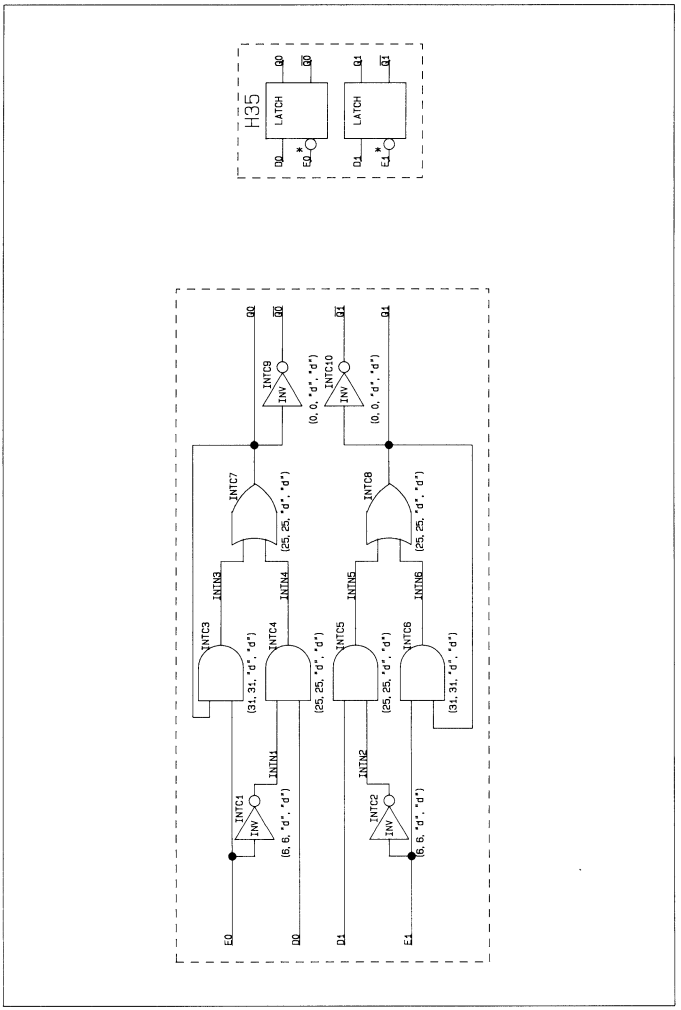
COMPONENT PLOTS

Plot 34



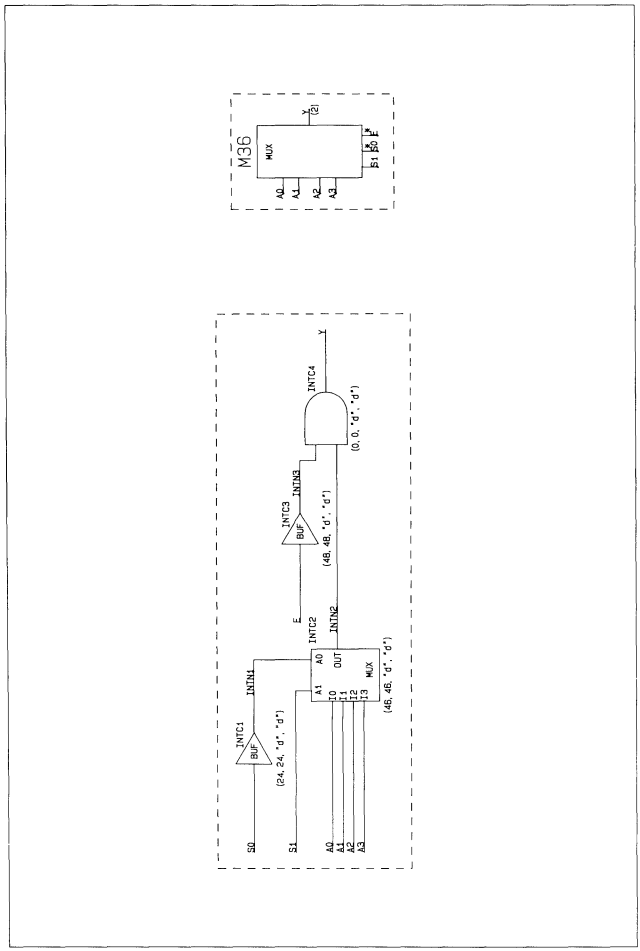
COMPONENT PLOTS

Plot 35



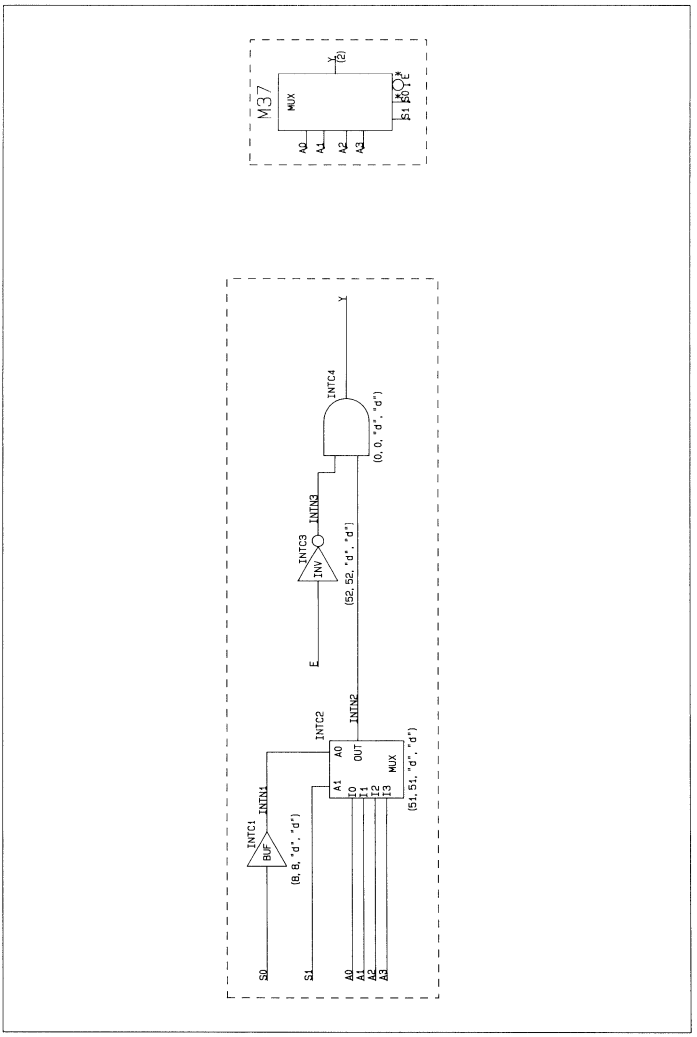
COMPONENT PLOTS

Plot 36



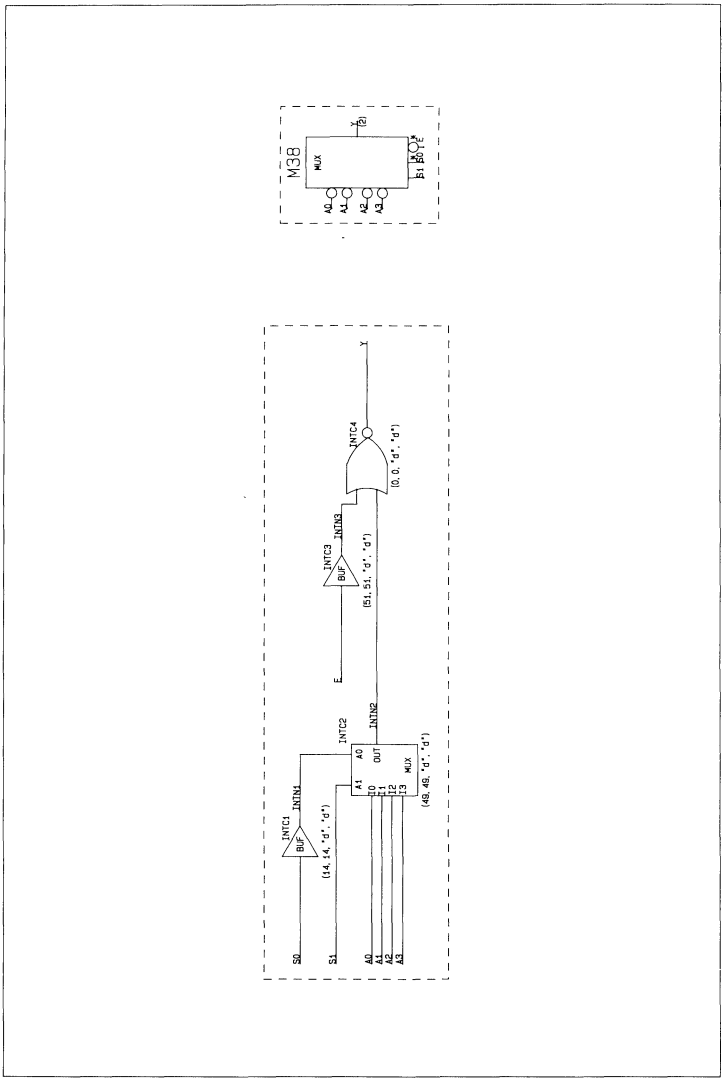
COMPONENT PLOTS

Plot 37



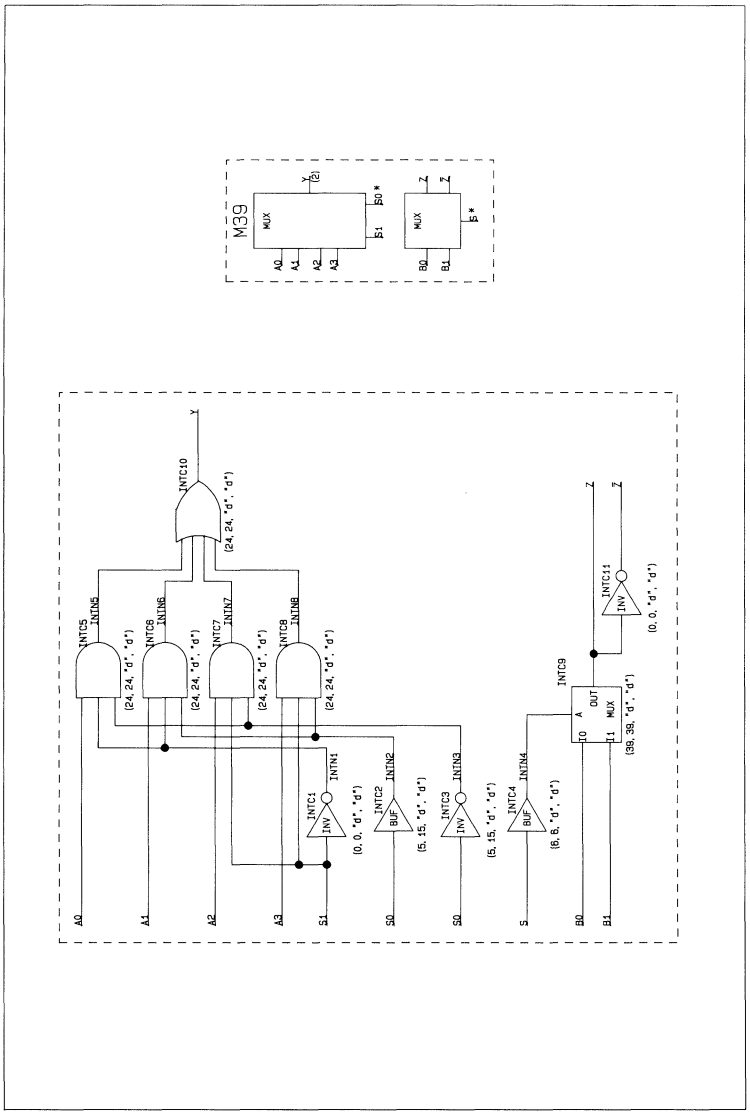
COMPONENT PLOTS

Plot 38



COMPONENT PLOTS

Plot 39

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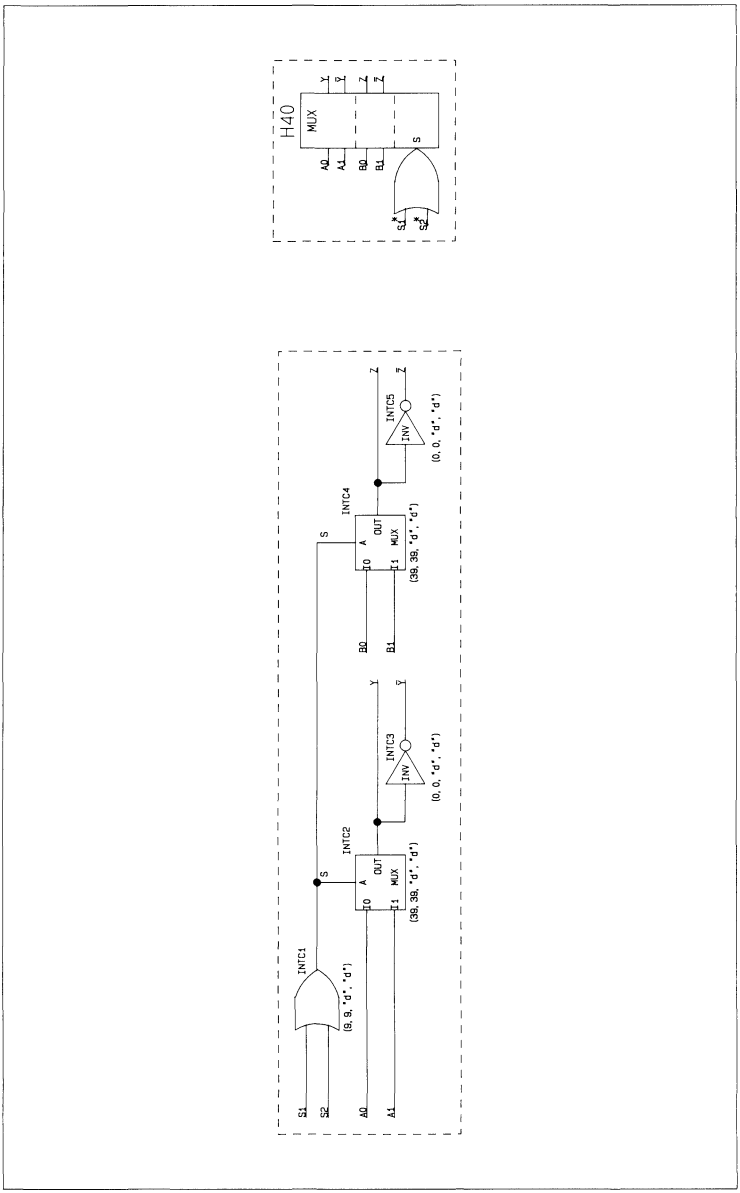
COMPONENT PLOTS

Plot 40

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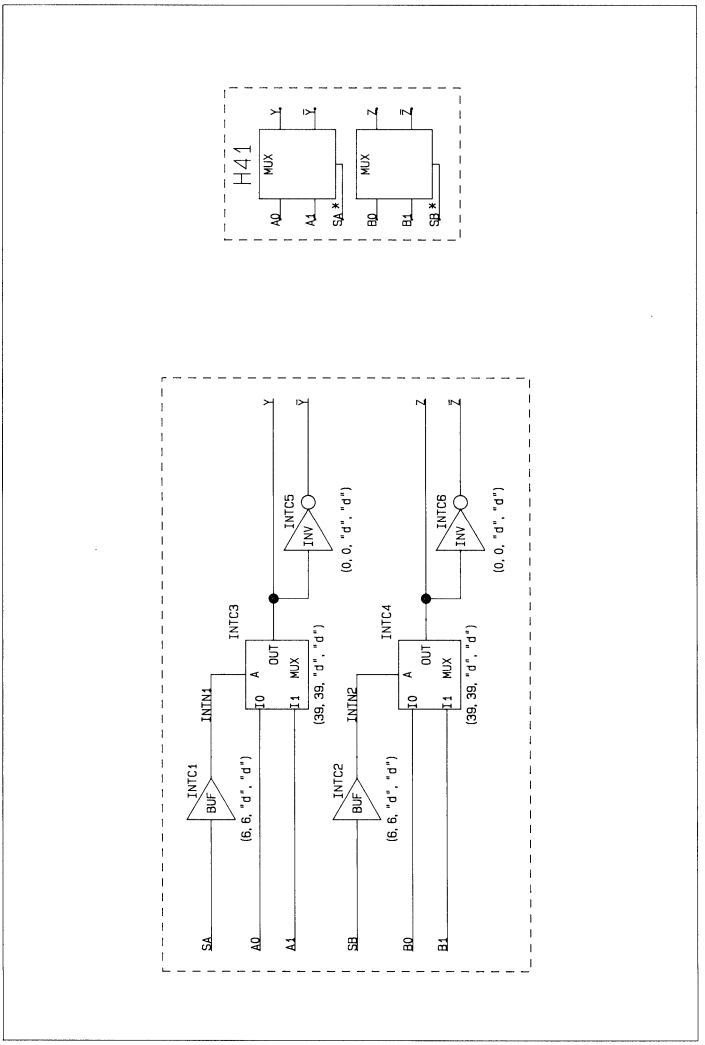
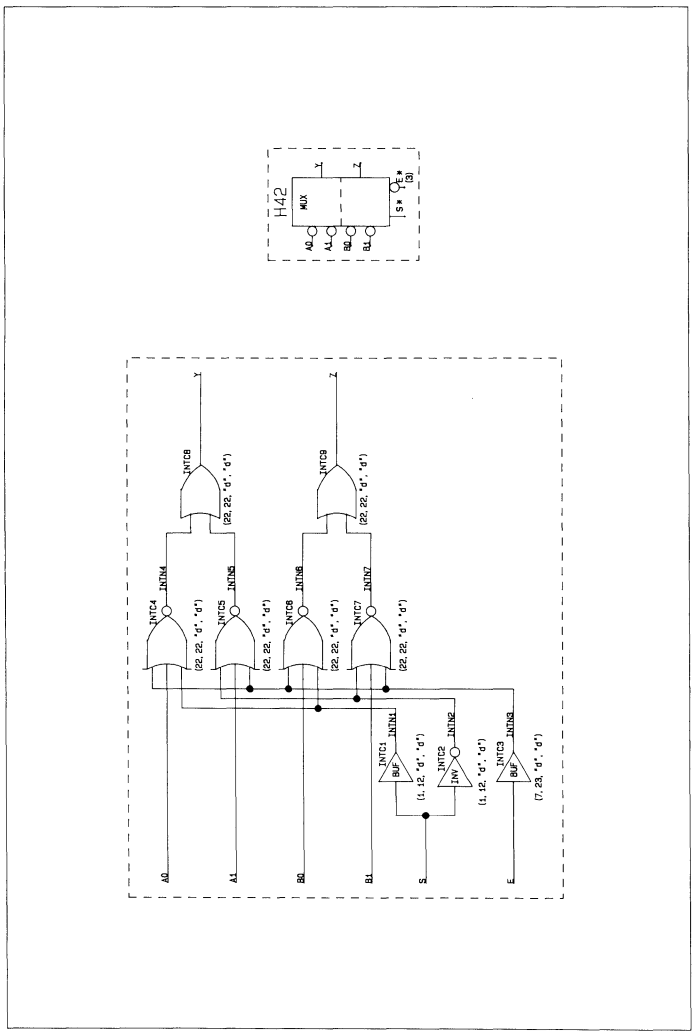
COMPONENT PLOTS

Plot 41



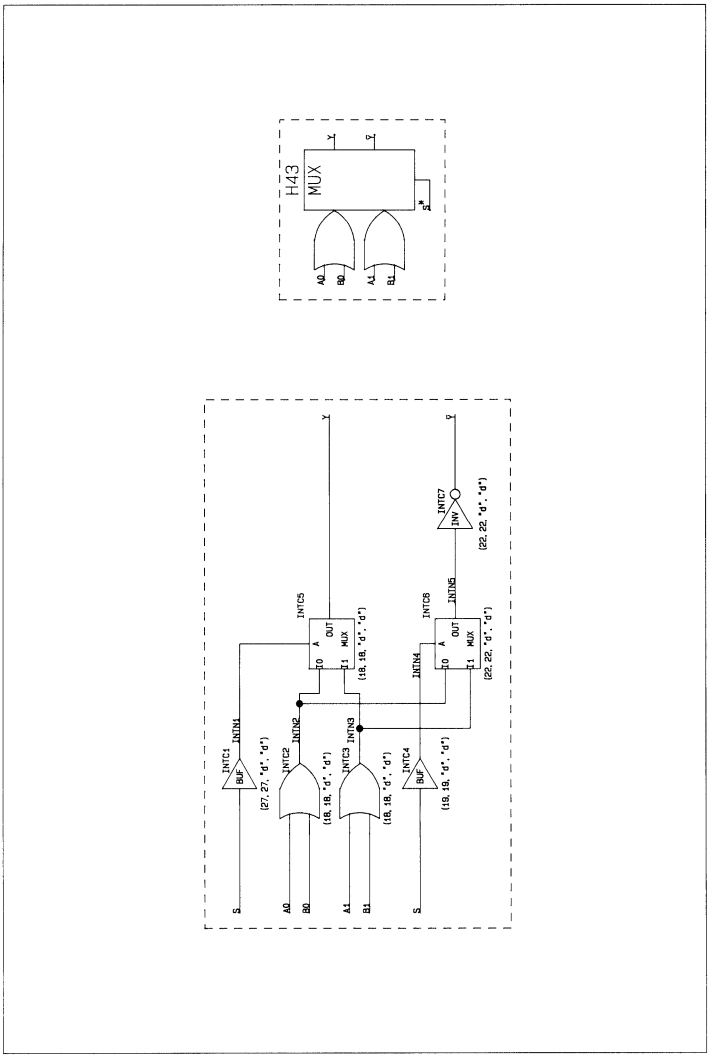
COMPONENT PLOTS

Plot 42



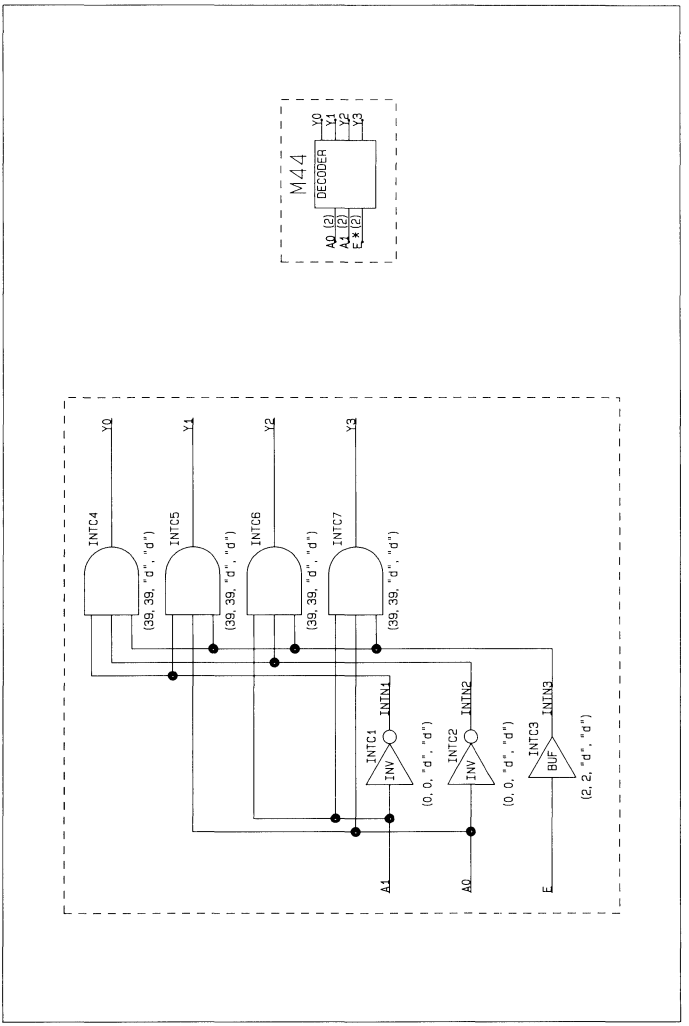
COMPONENT PLOTS

Plot 43



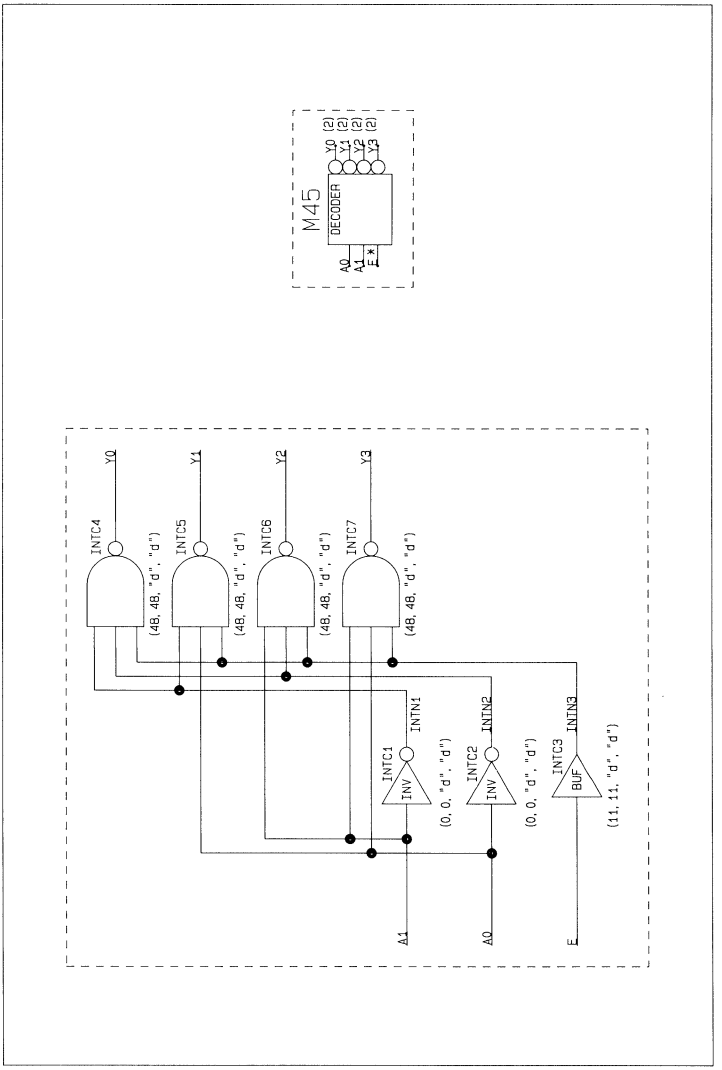
COMPONENT PLOTS

Plot 44



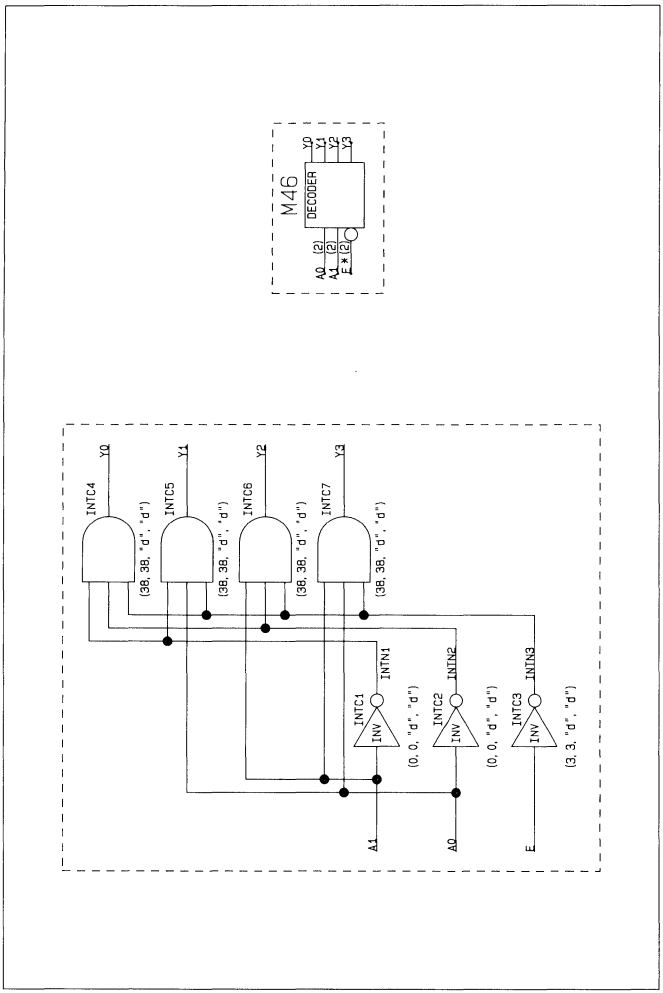
COMPONENT PLOTS

Plot 45

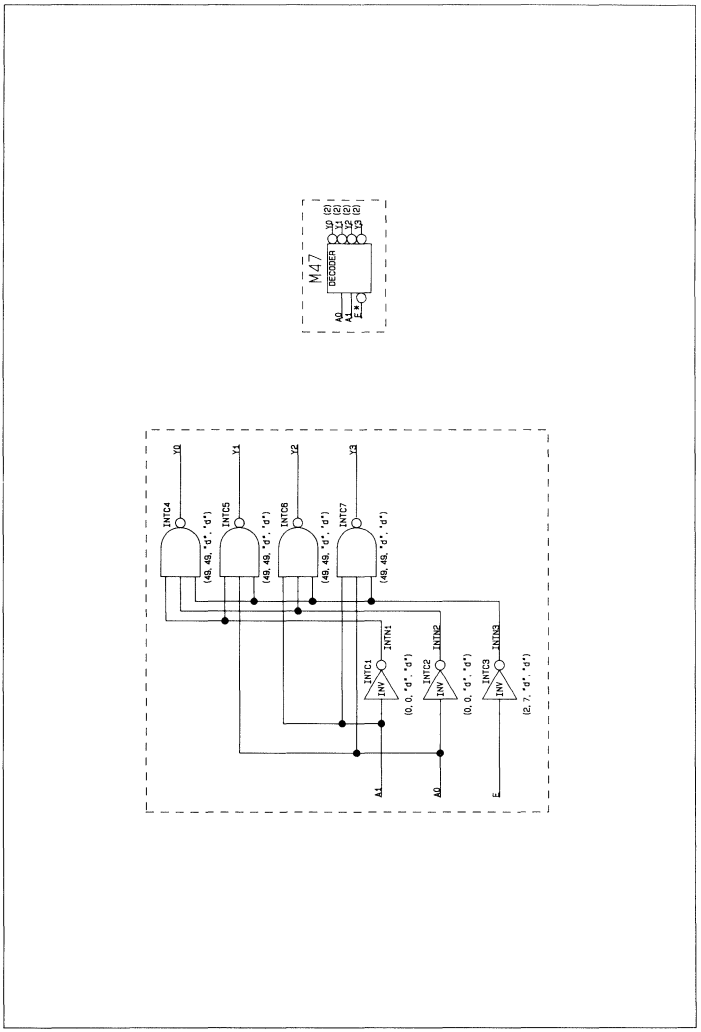


COMPONENT PLOTS

Plot 46

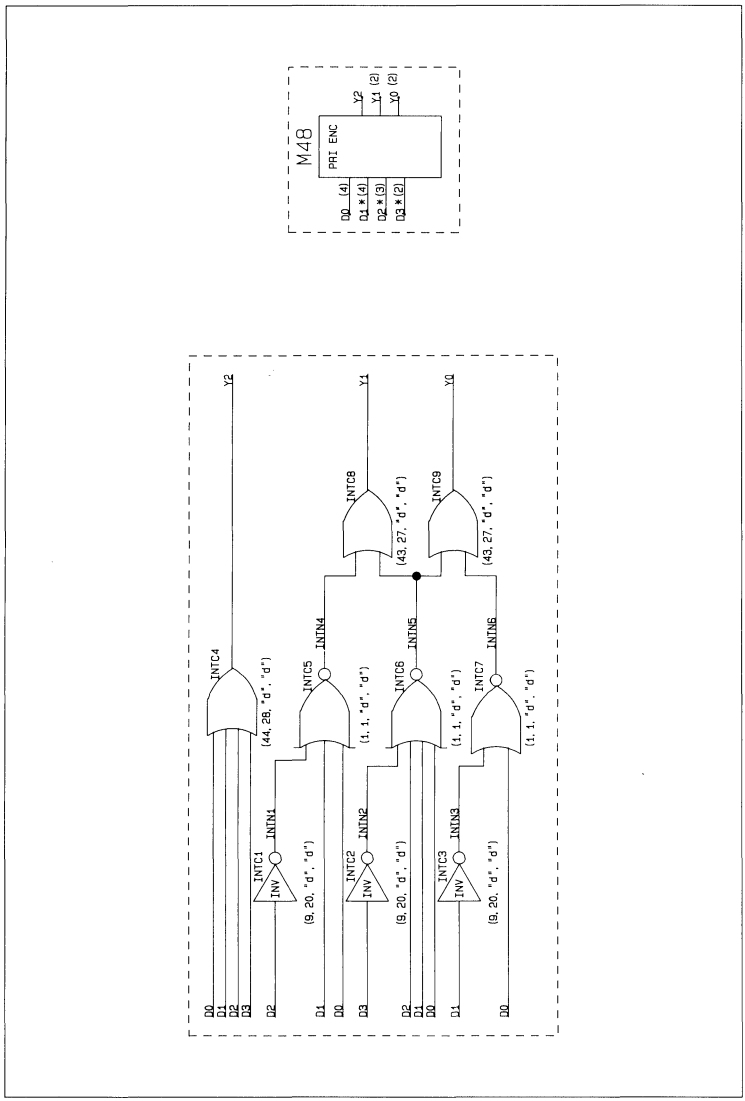


COMPONENT PLOTS Plot 47



COMPONENT PLOTS

Plot 48

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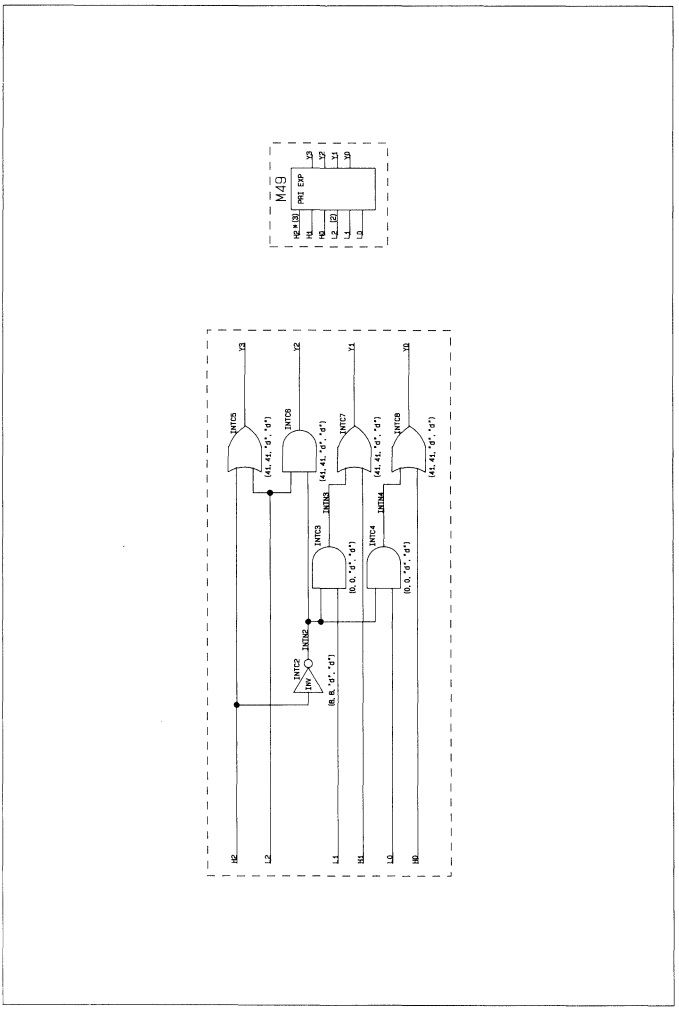
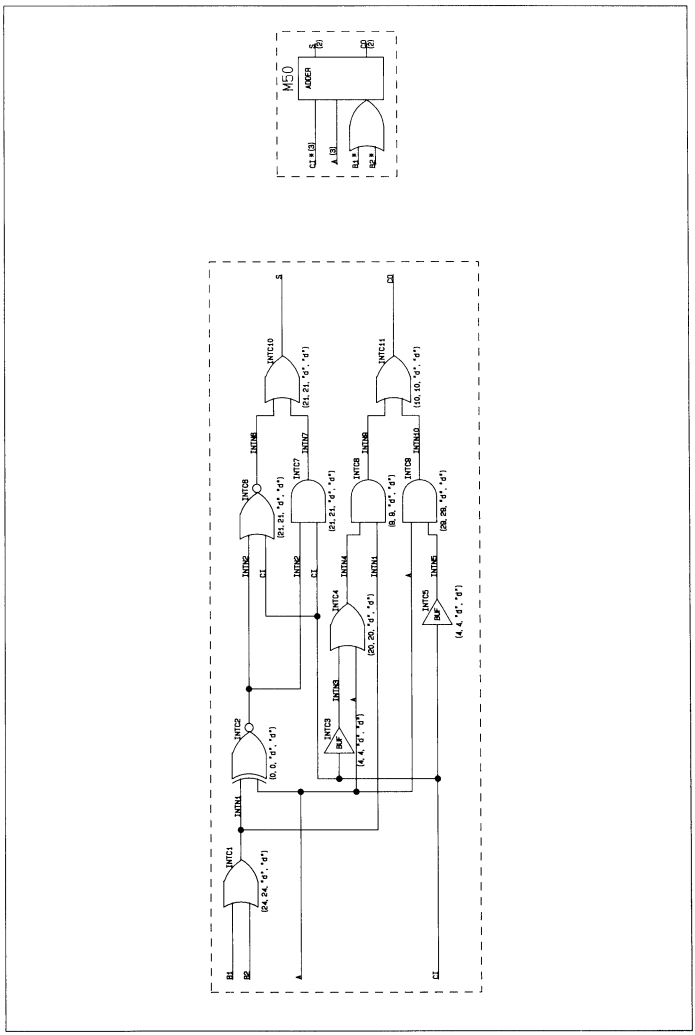
COMPONENT PLOTS

Plot 49



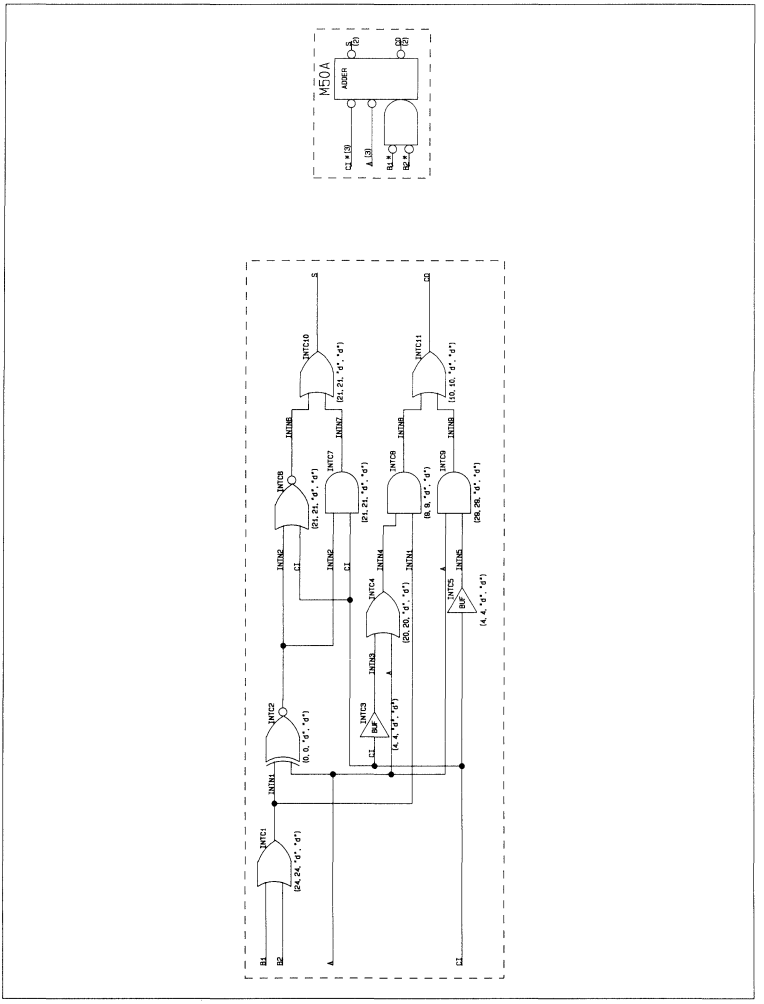
COMPONENT PLOTS

Plot 50



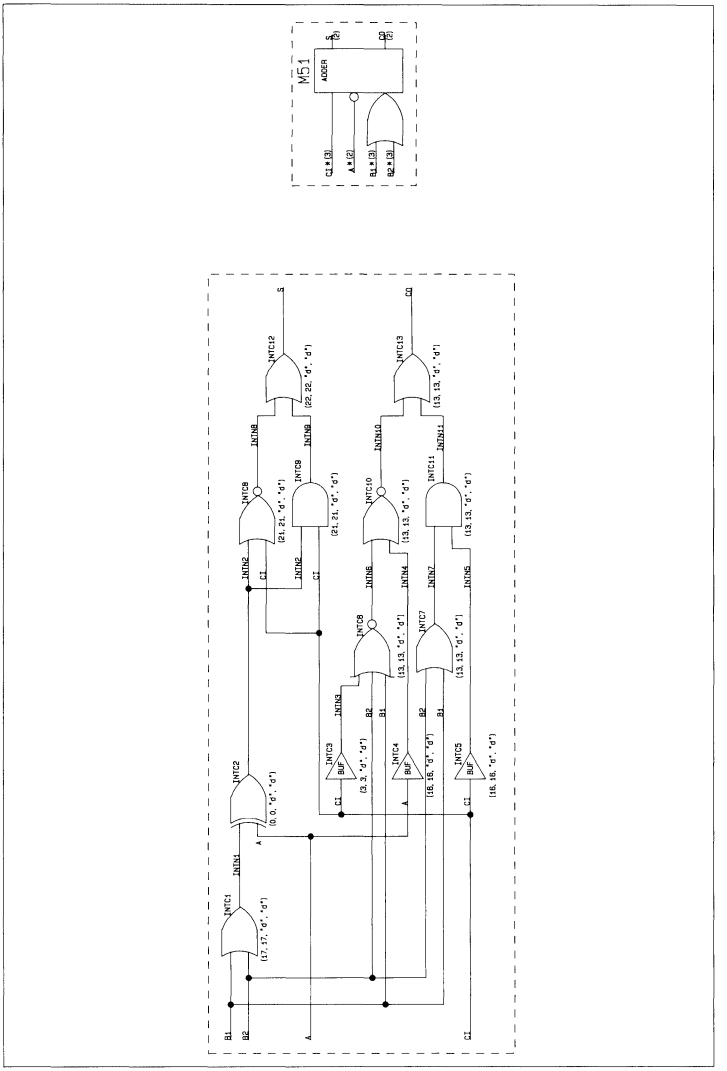
COMPONENT PLOTS

Plot 51



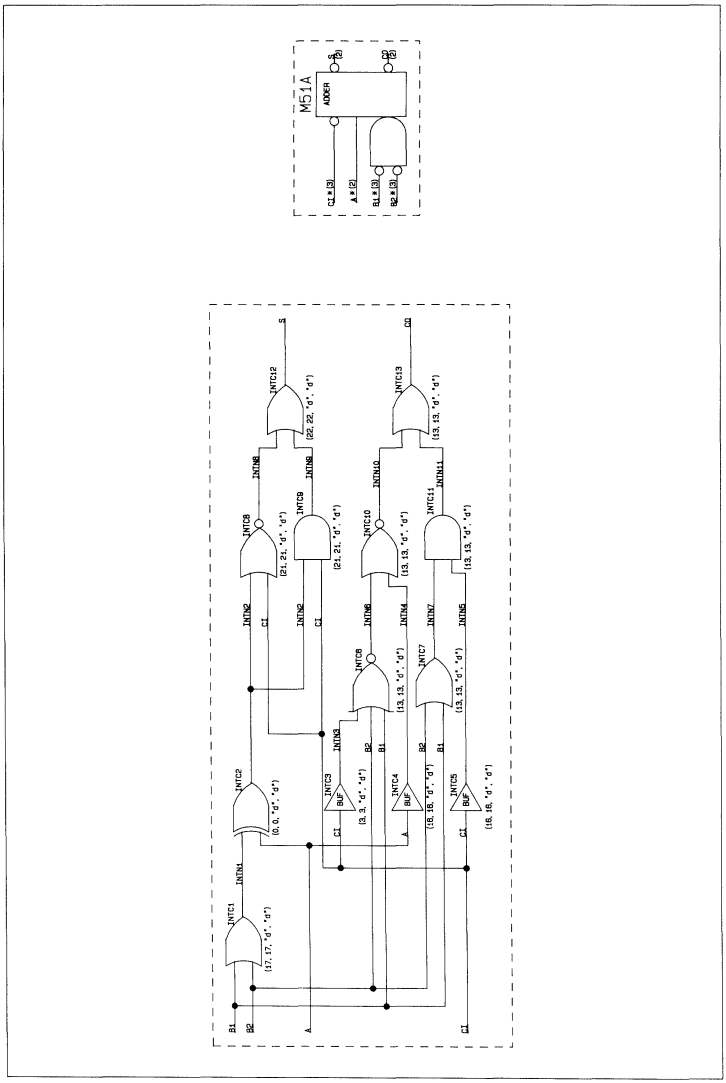
COMPONENT PLOTS

Plot 52



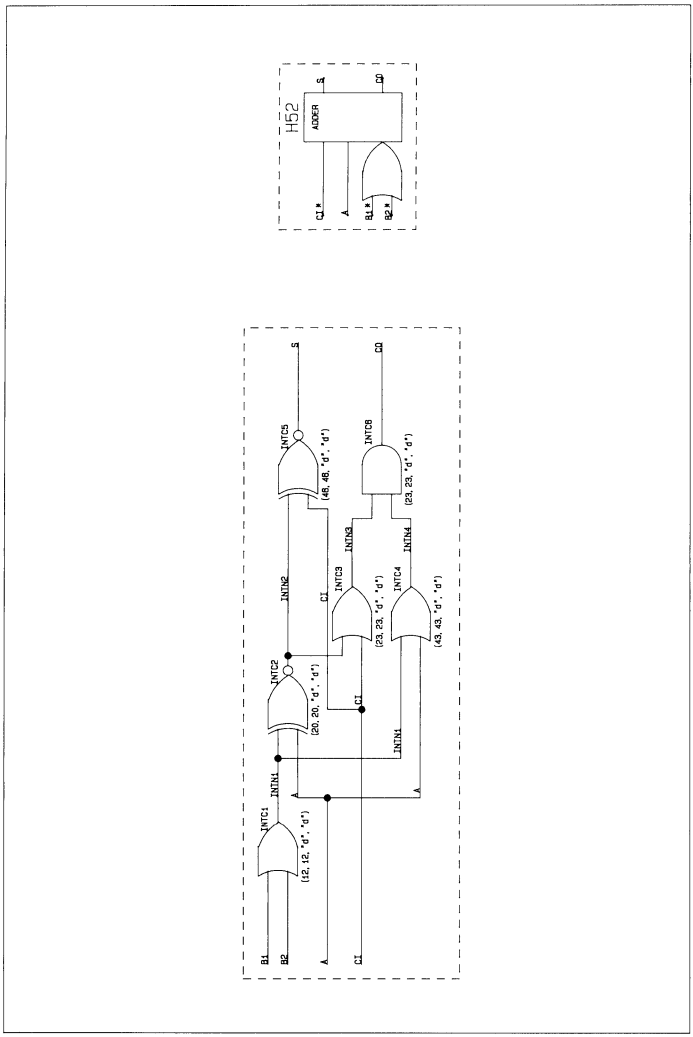
COMPONENT PLOTS

Plot 53



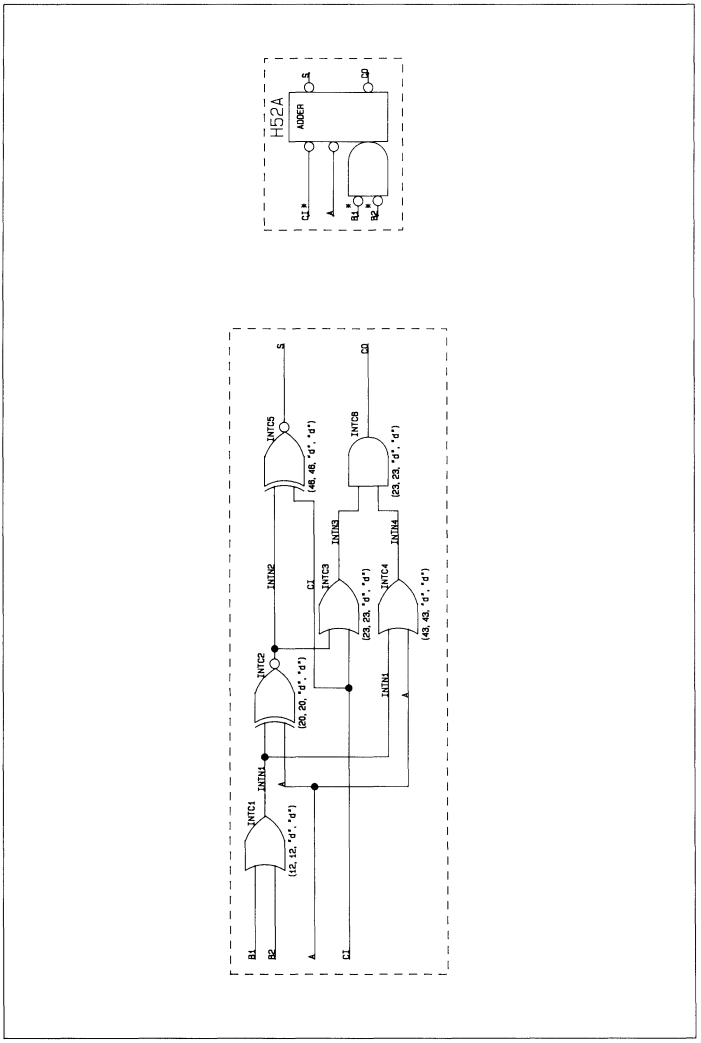
COMPONENT PLOTS

Plot 54



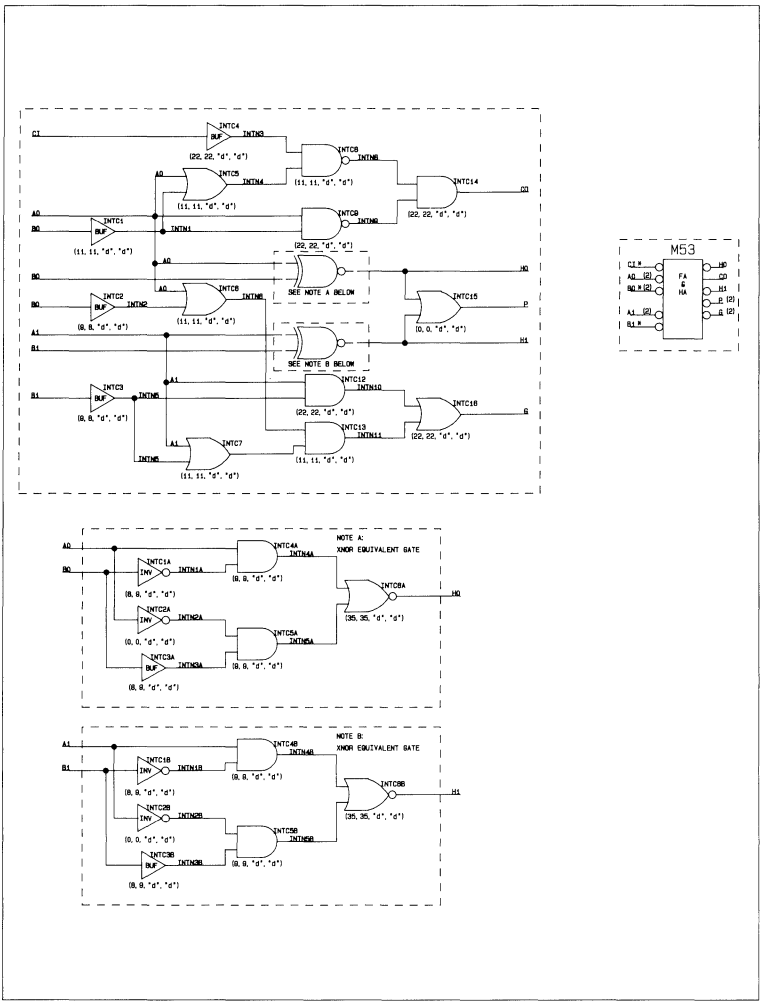
COMPONENT PLOTS

Plot 55



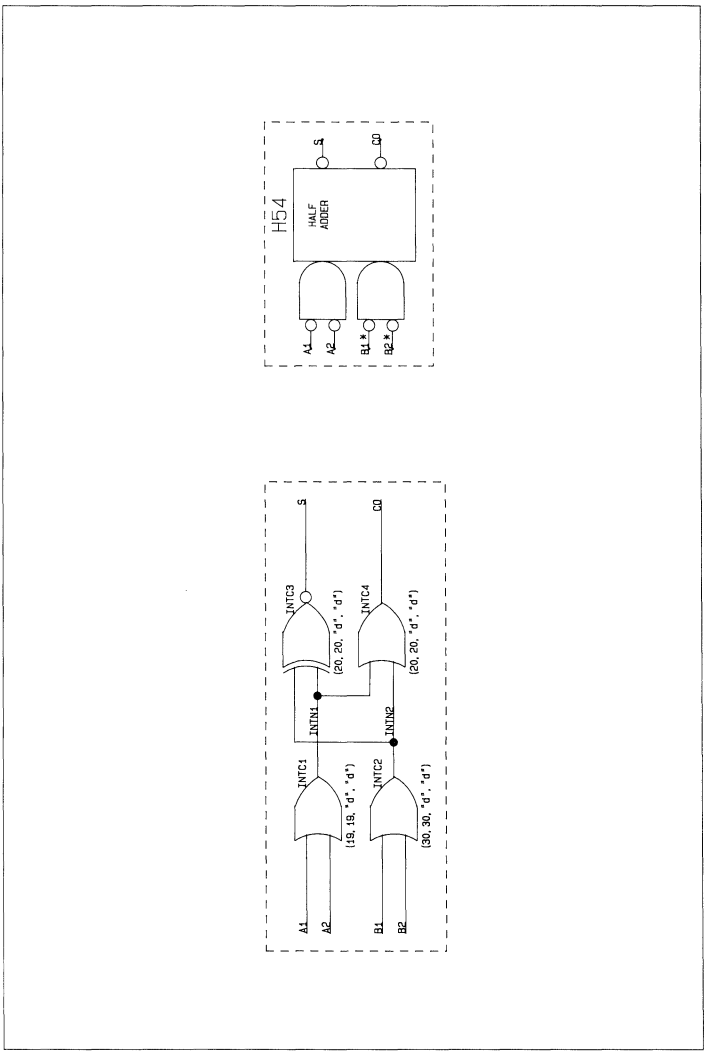
COMPONENT PLOTS

Plot 56



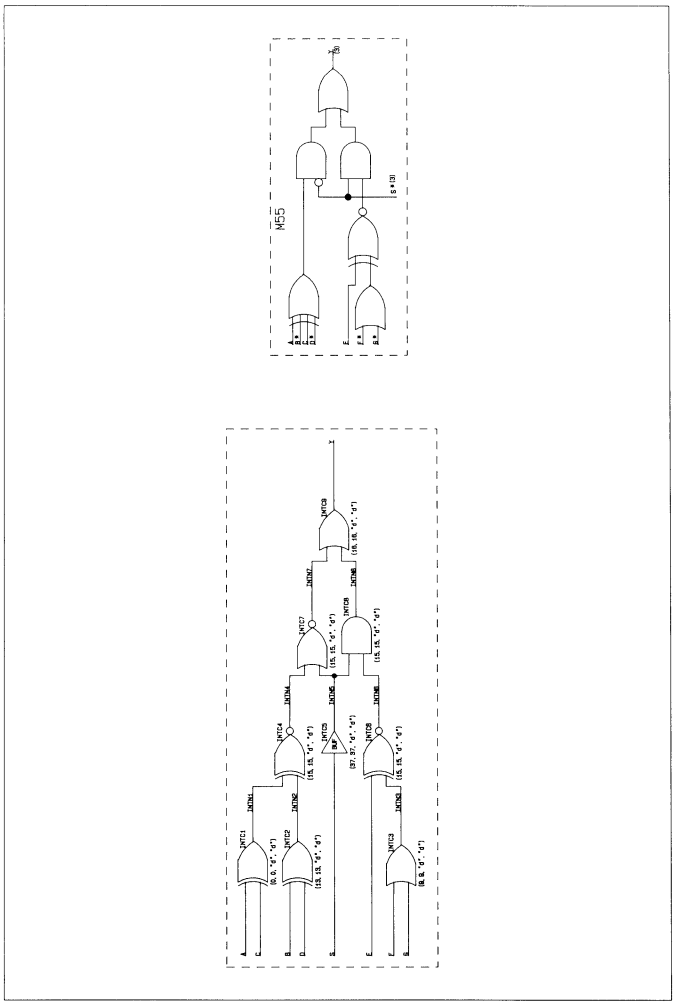
COMPONENT PLOTS

Plot 57



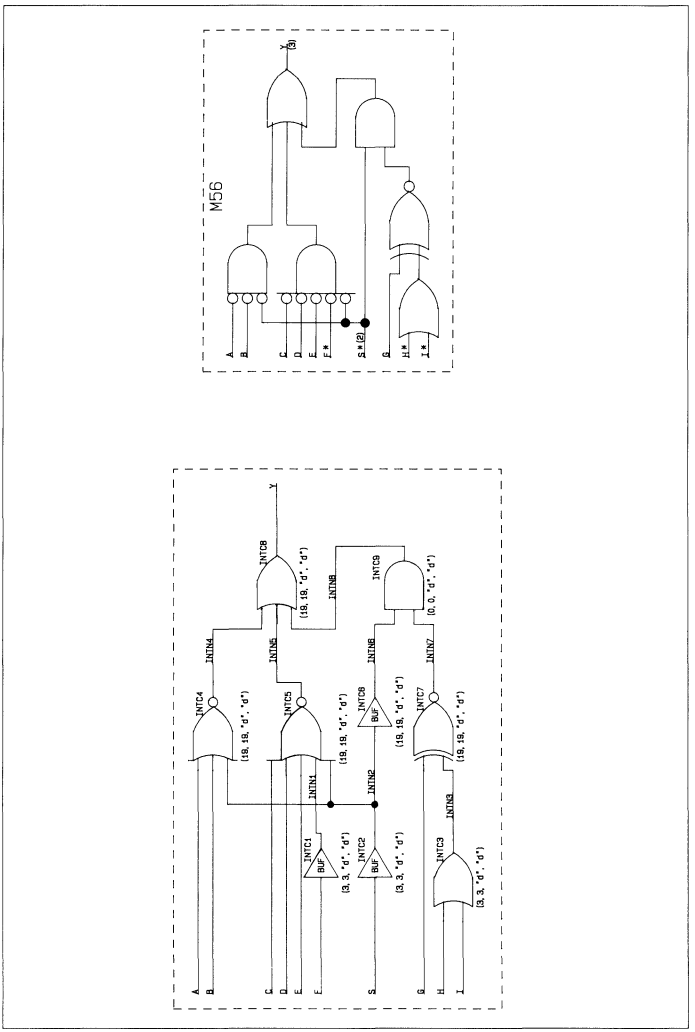
COMPONENT PLOTS

Plot 58



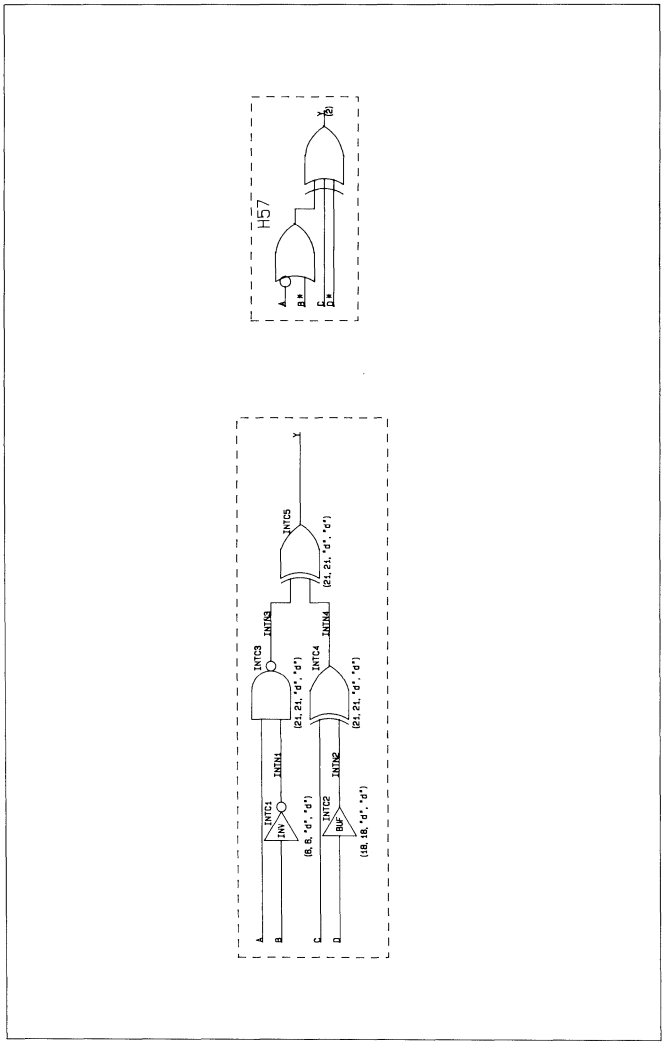
COMPONENT PLOTS

Plot 59



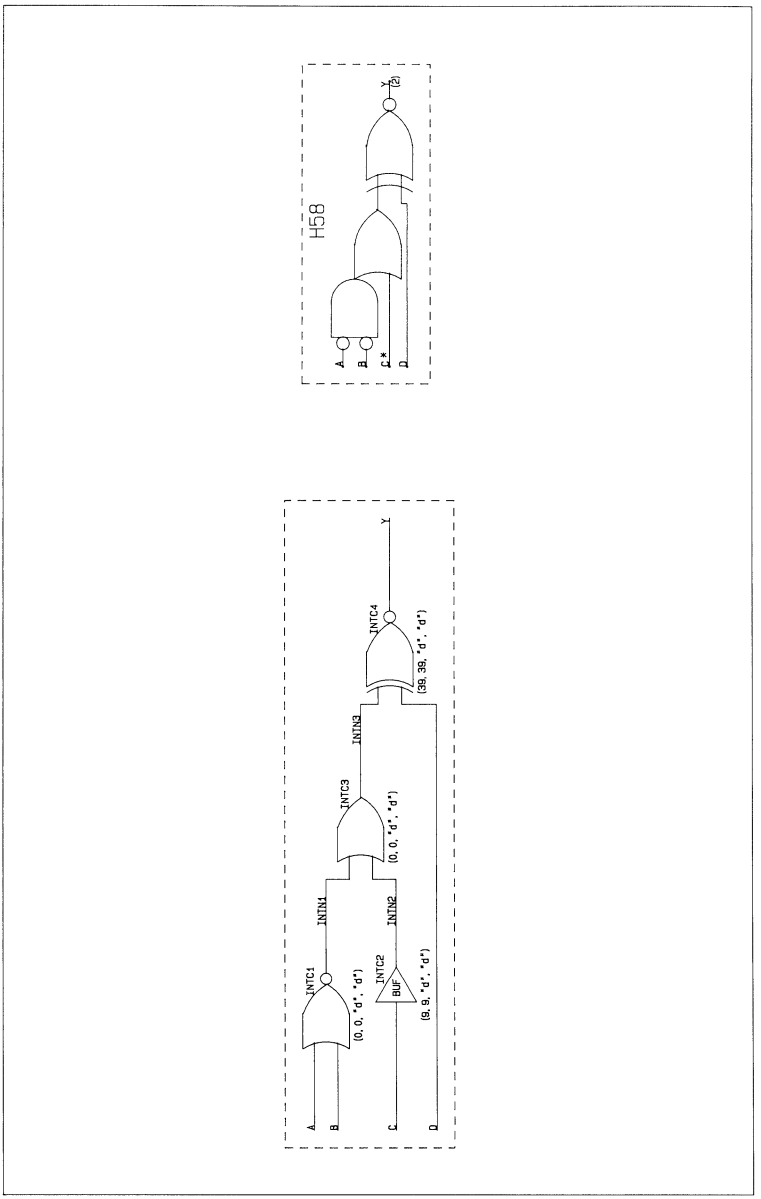
COMPONENT PLOTS

Plot 60



COMPONENT PLOTS

Plot 61

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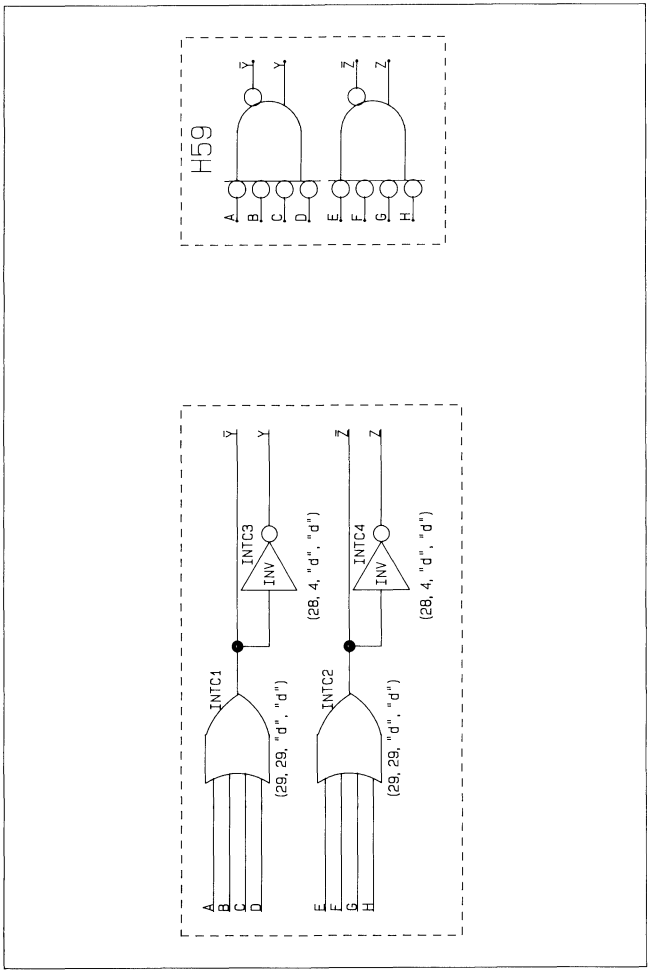
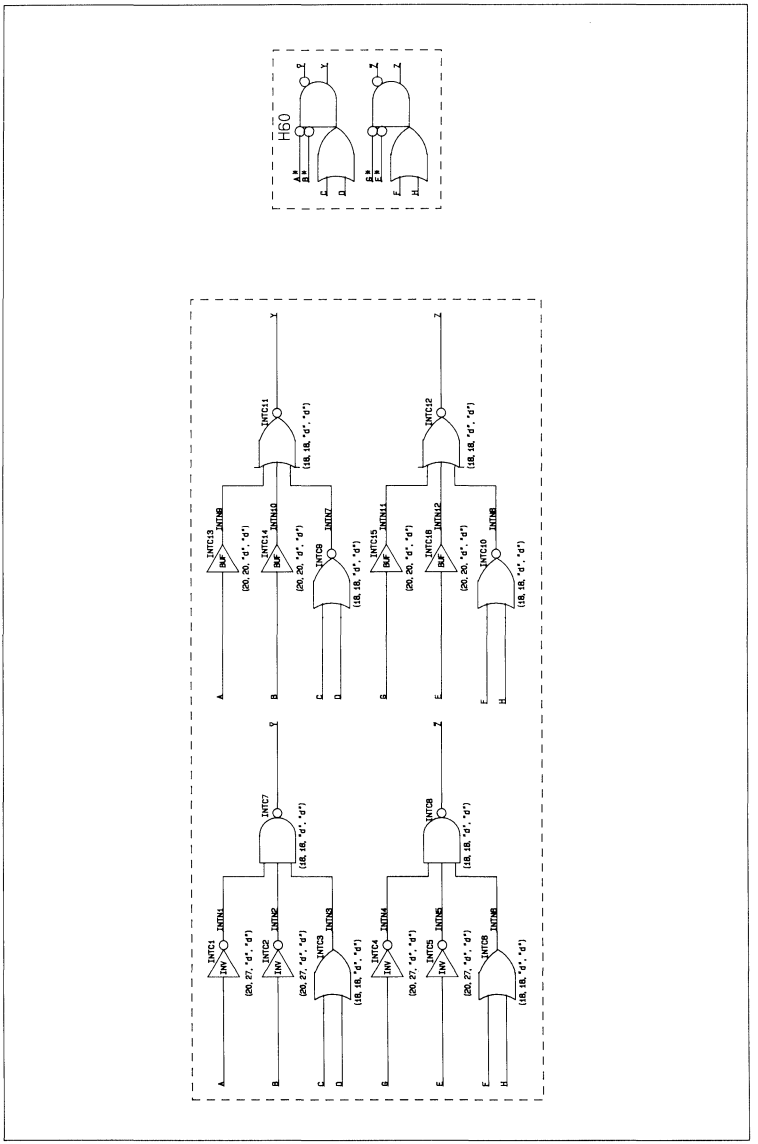
COMPONENT PLOTS

Plot 62



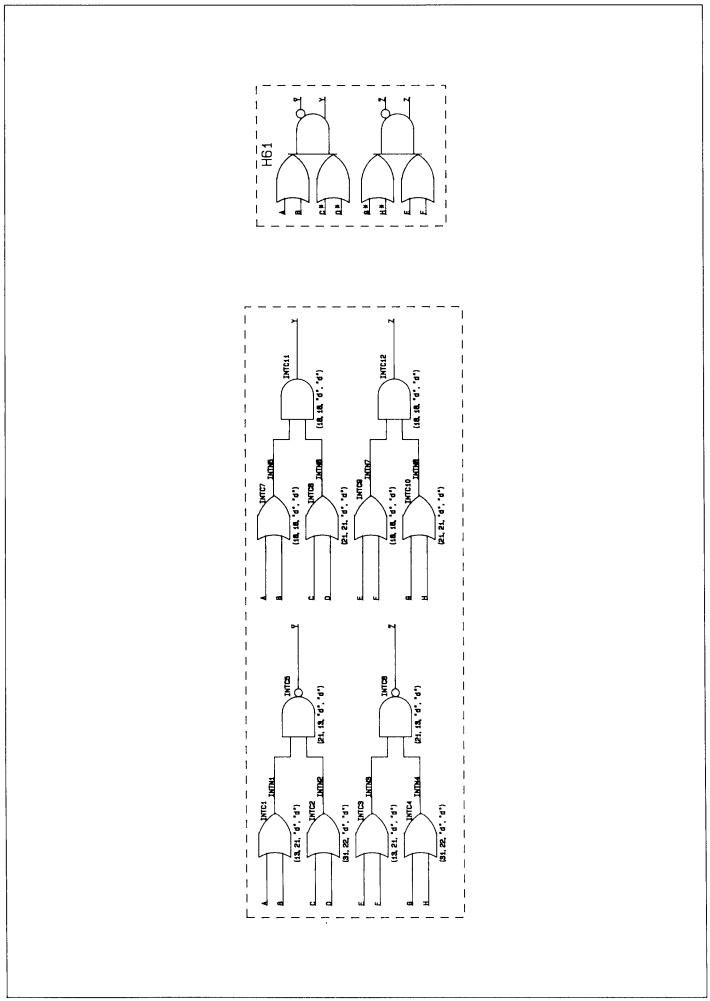
COMPONENT PLOTS

Plot 63

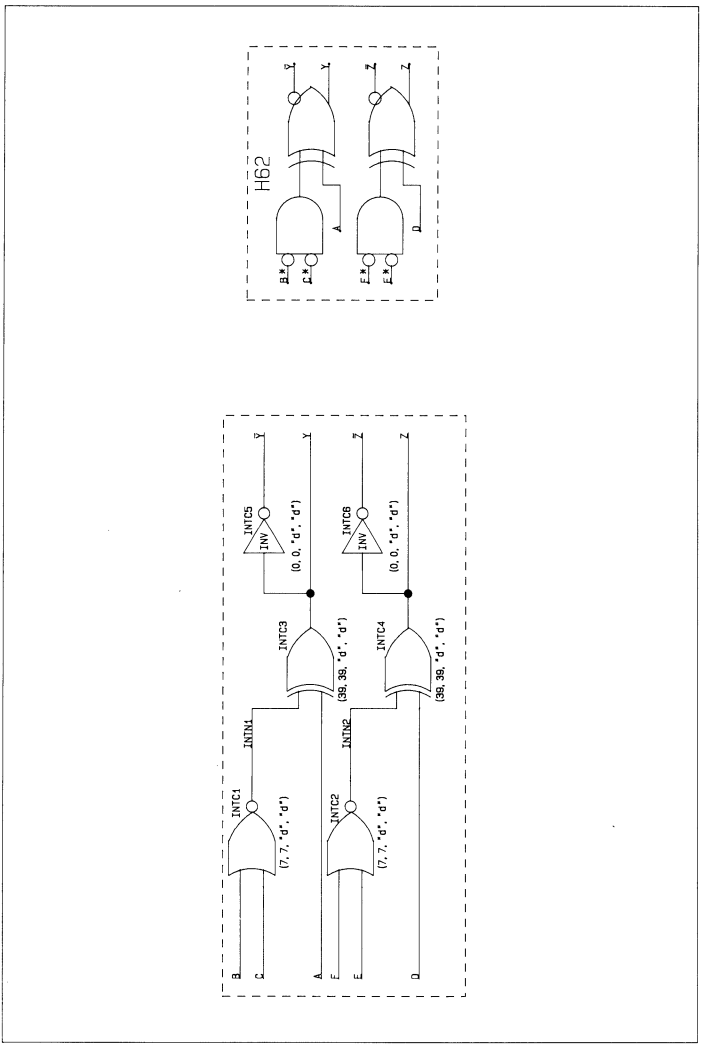


COMPONENT PLOTS

Plot 64

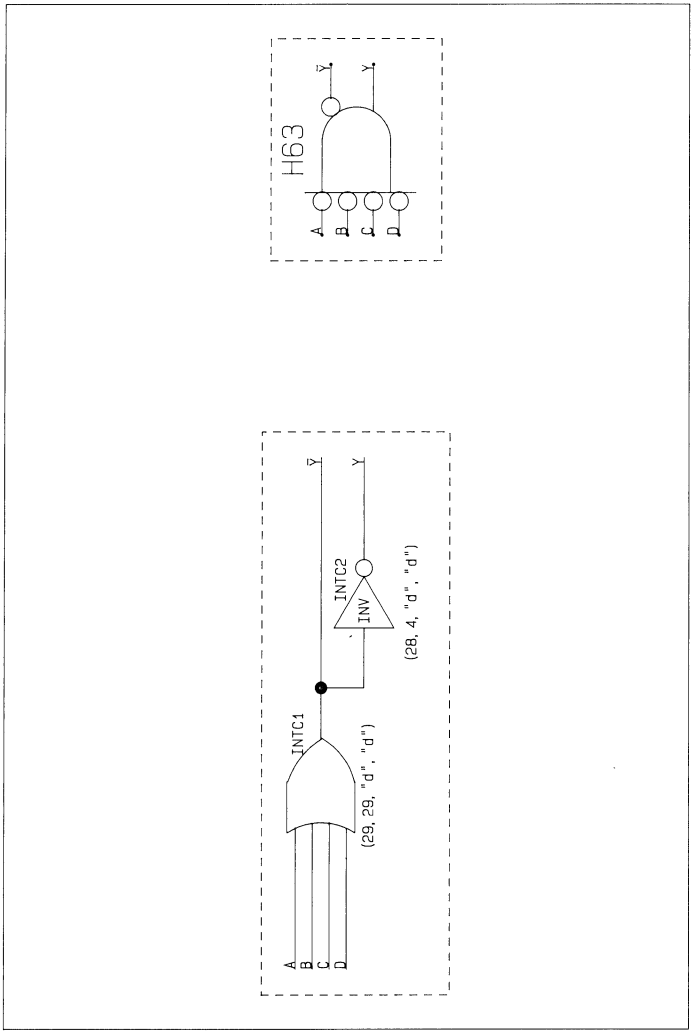


COMPONENT PLOTS Plot 65



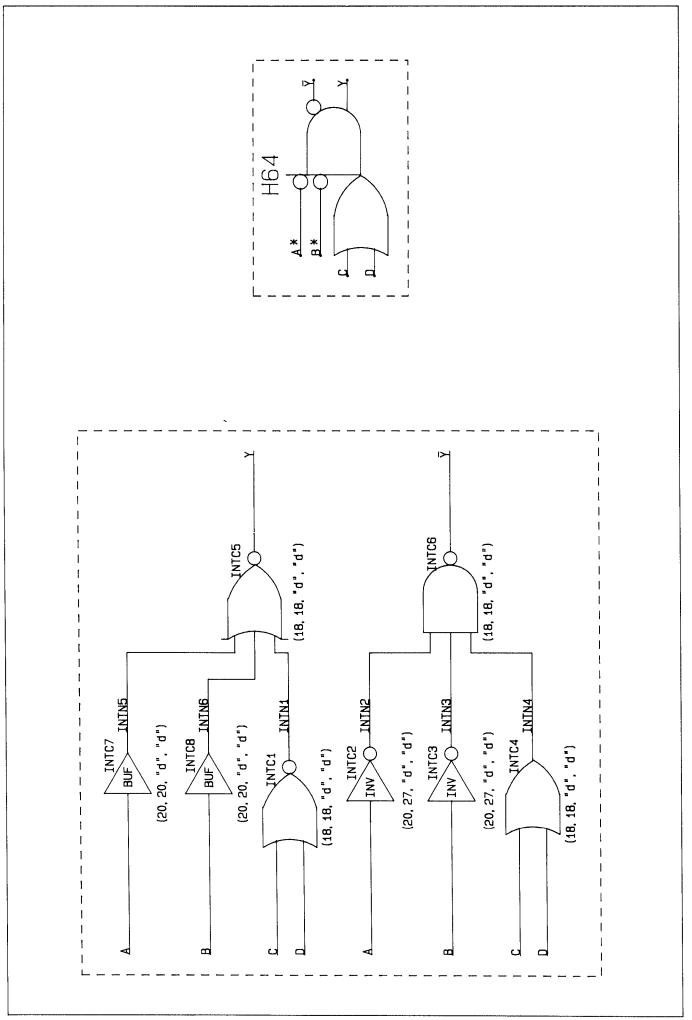
COMPONENT PLOTS

Plot 66



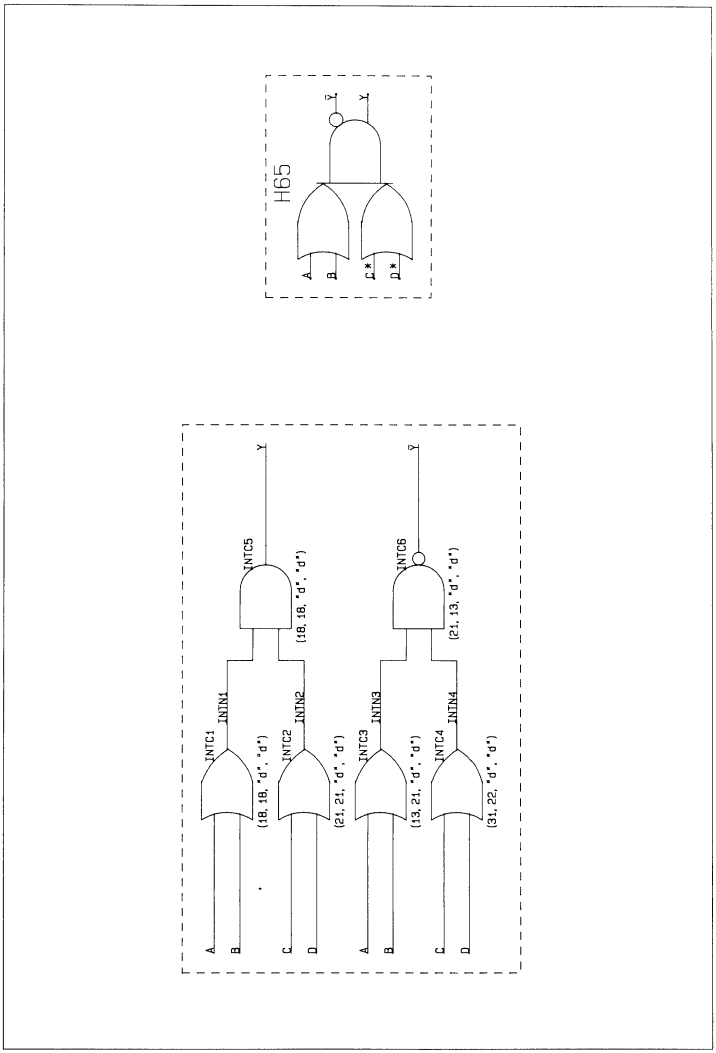
COMPONENT PLOTS

Plot 67



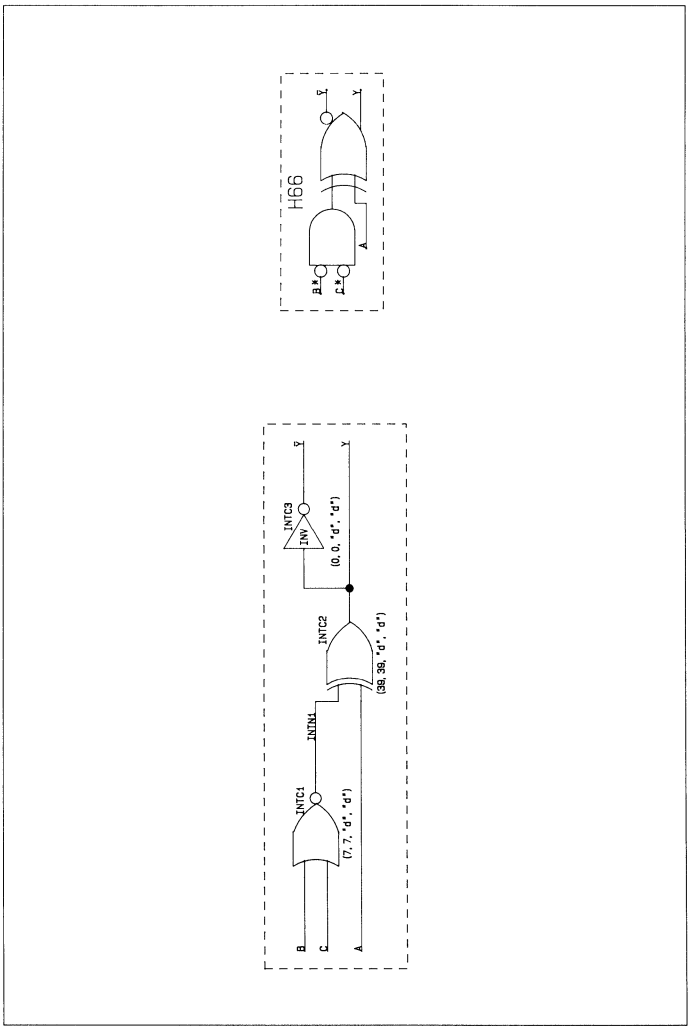
COMPONENT PLOTS

Plot 68



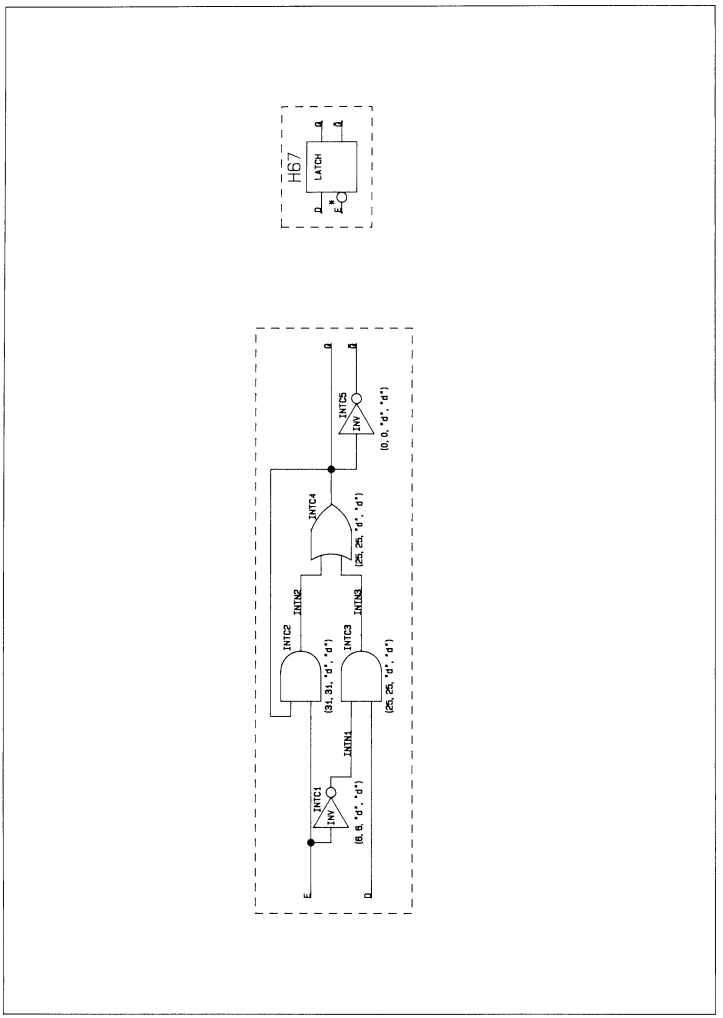
COMPONENT PLOTS

Plot 69



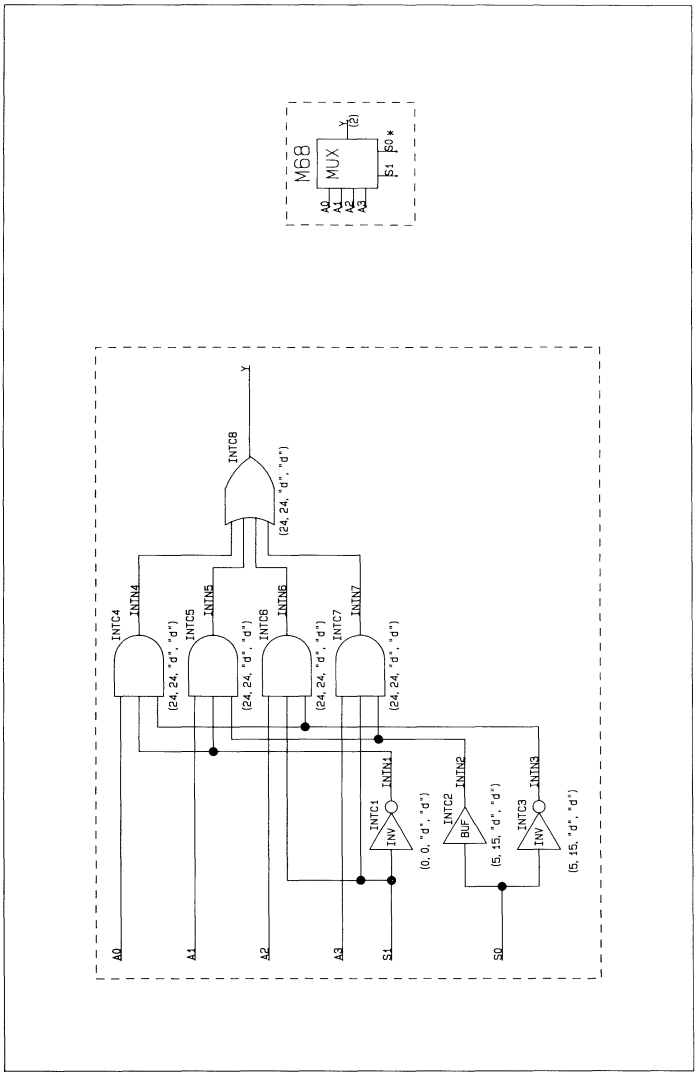
COMPONENT PLOTS

Plot 70



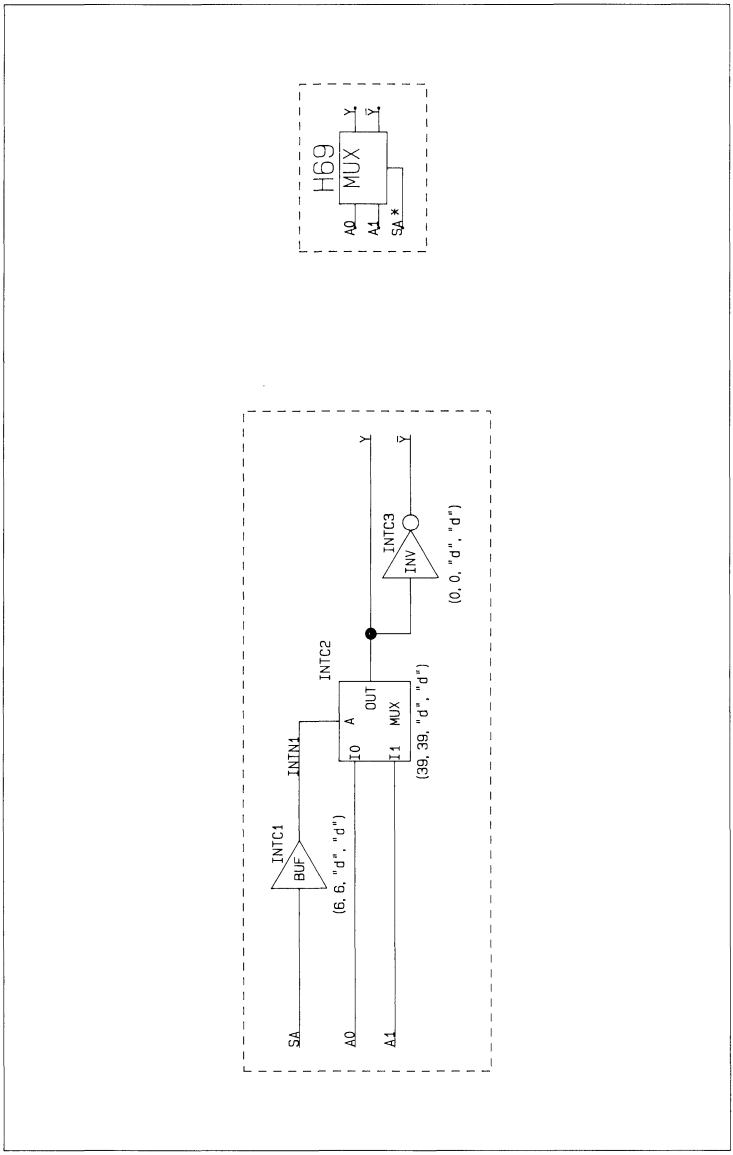
COMPONENT PLOTS

Plot 71



COMPONENT PLOTS

Plot 72

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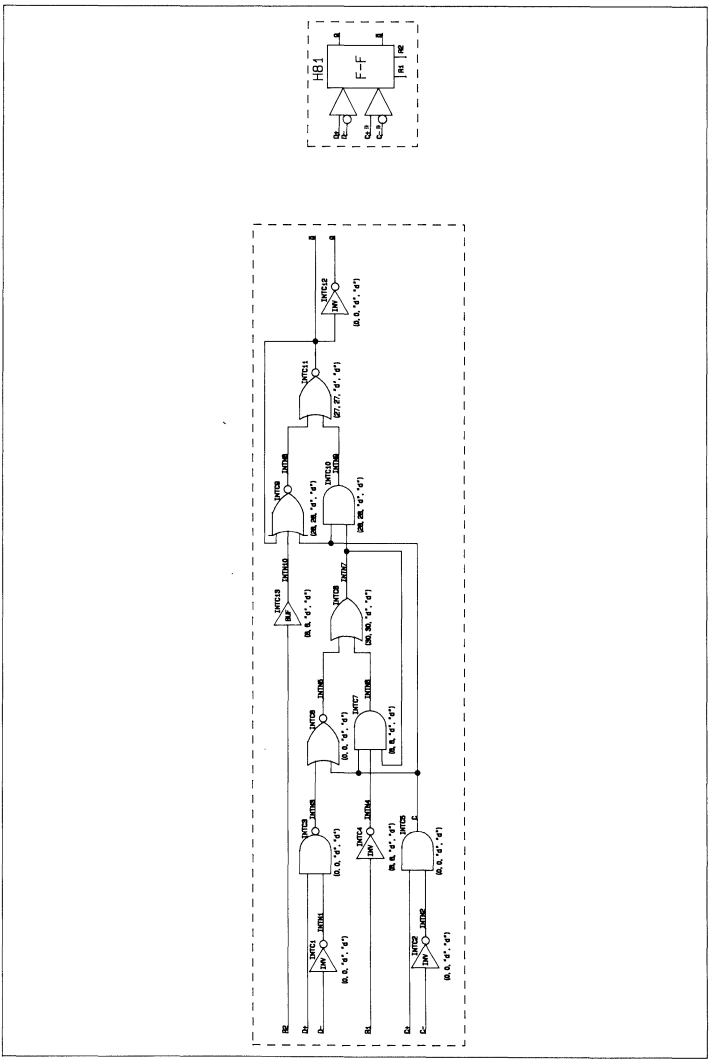
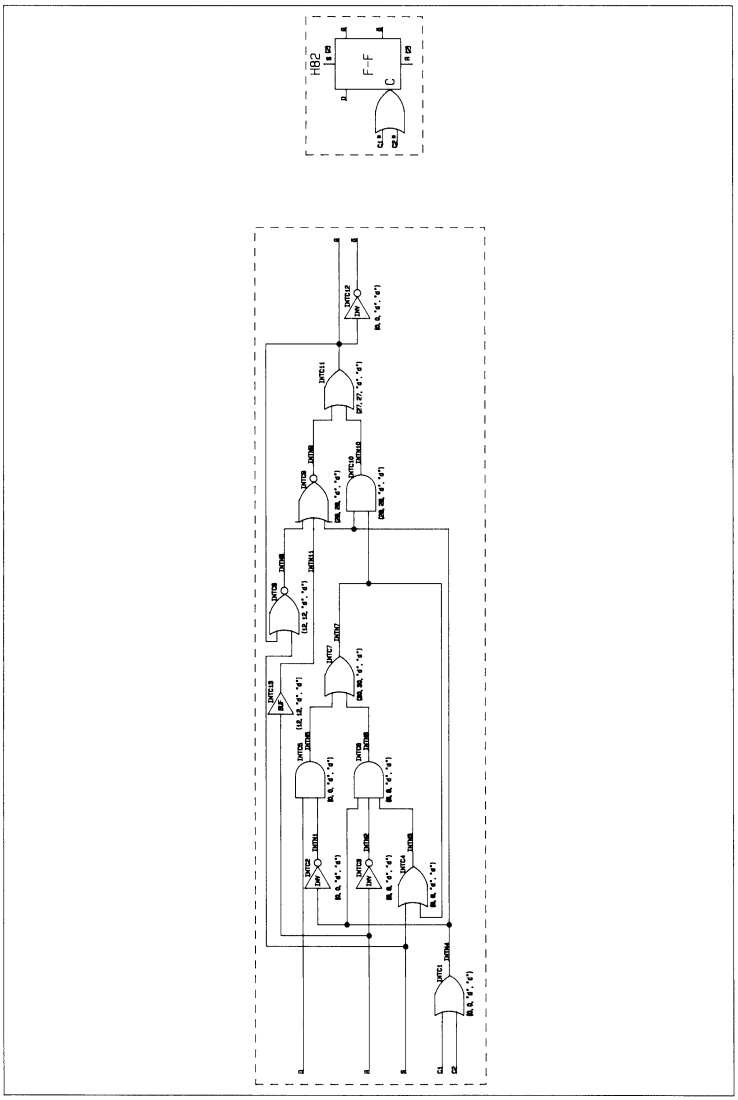
COMPONENT PLOTS Plot 73



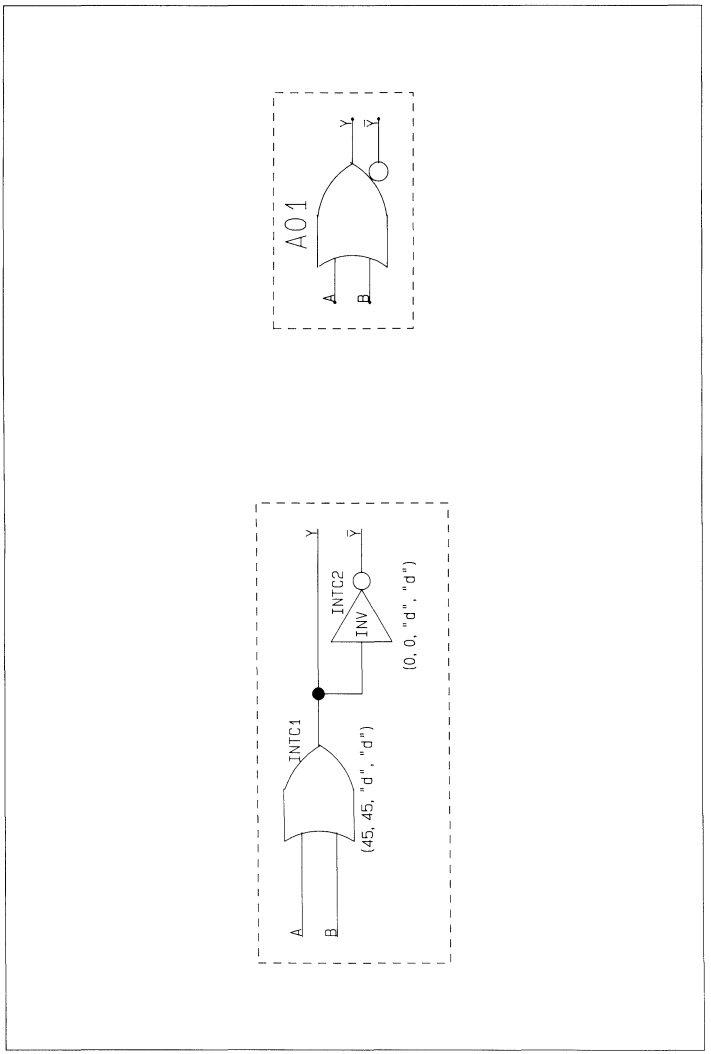
COMPONENT PLOTS

Plot 74



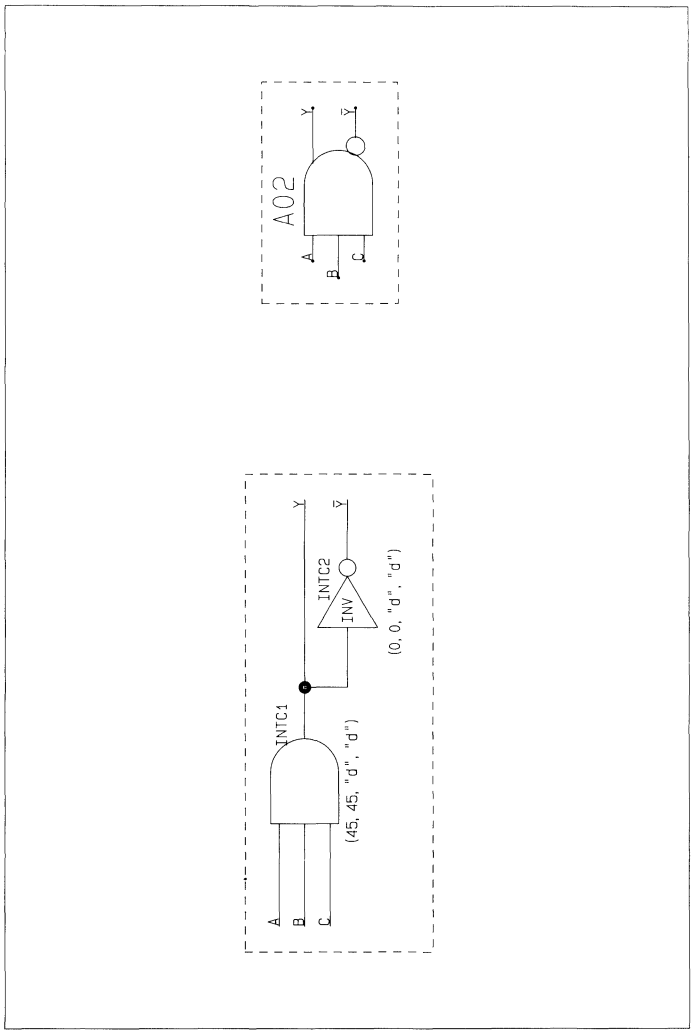
COMPONENT PLOTS

Plot 75



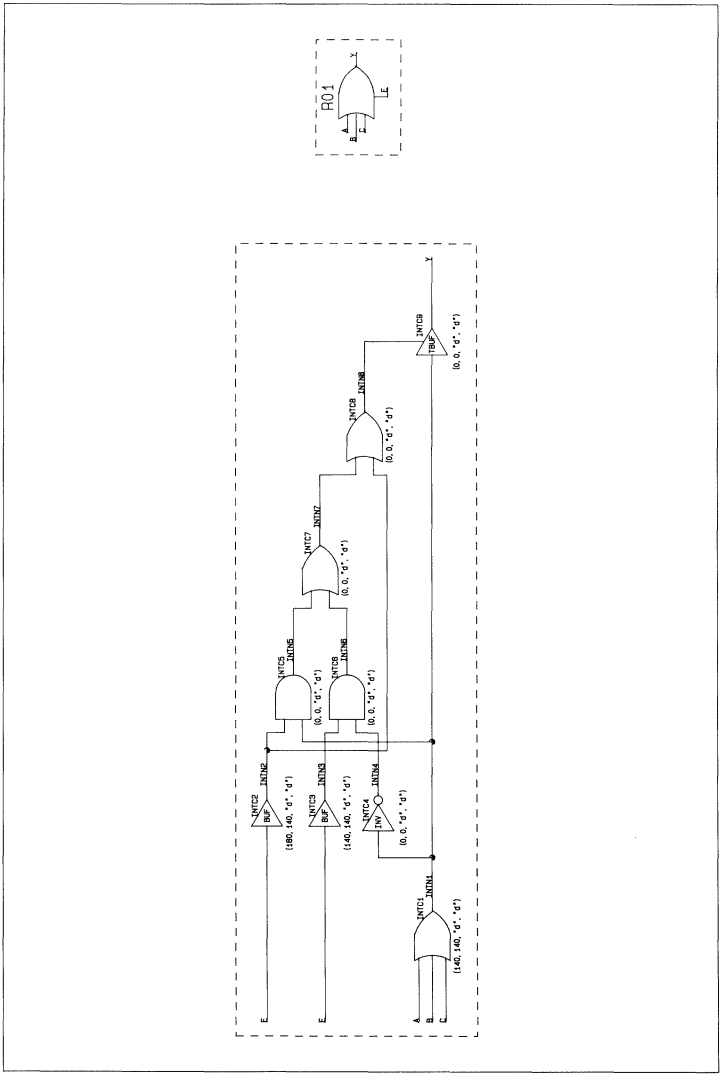
COMPONENT PLOTS

Plot 76



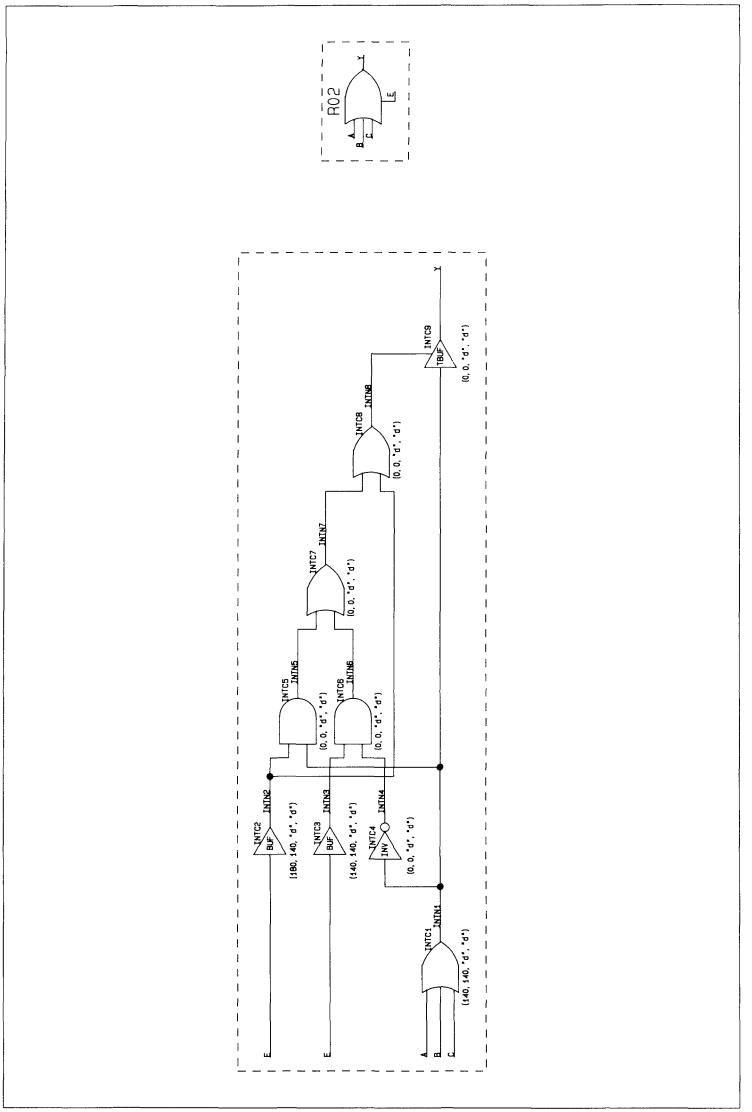
COMPONENT PLOTS

Plot 77



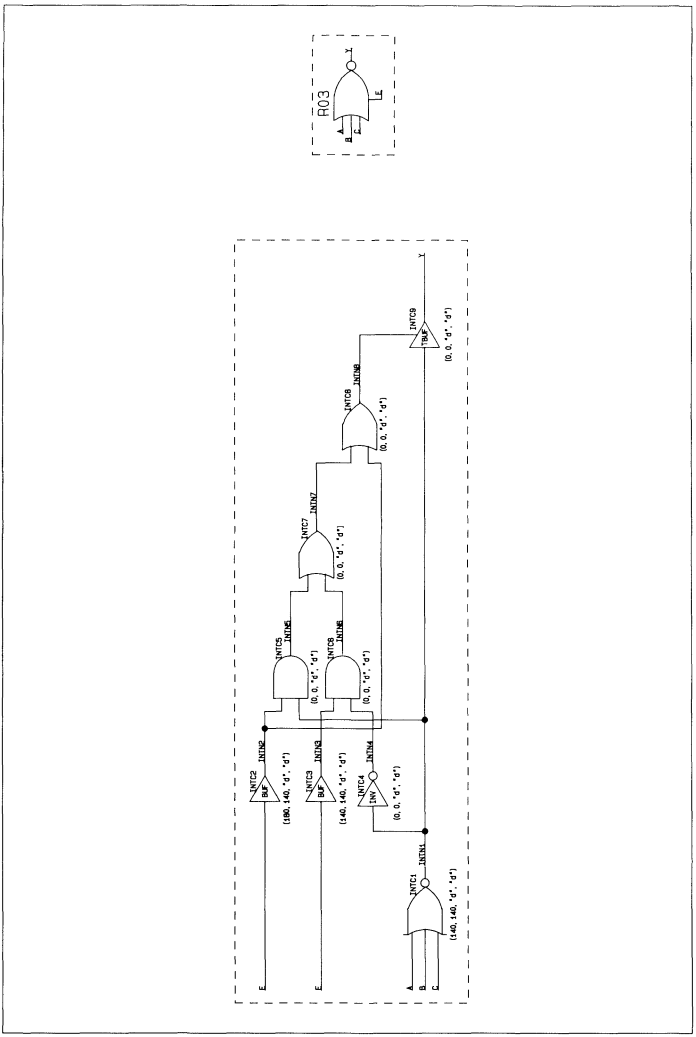
COMPONENT PLOTS

Plot 78



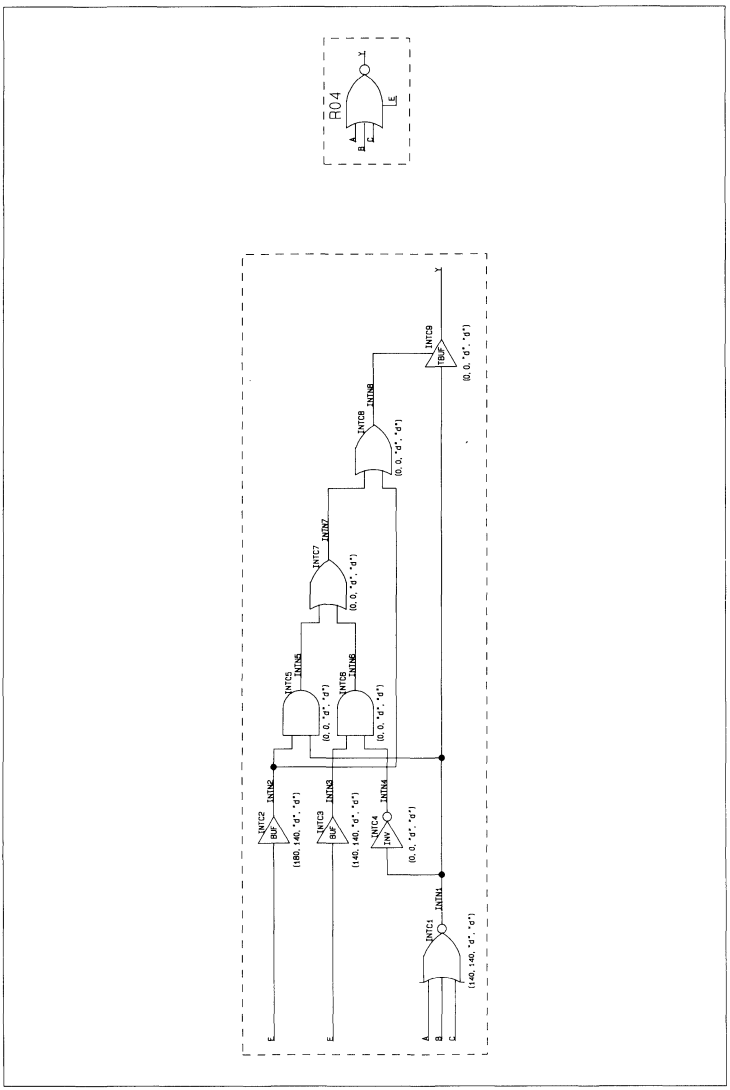
COMPONENT PLOTS

Plot 79



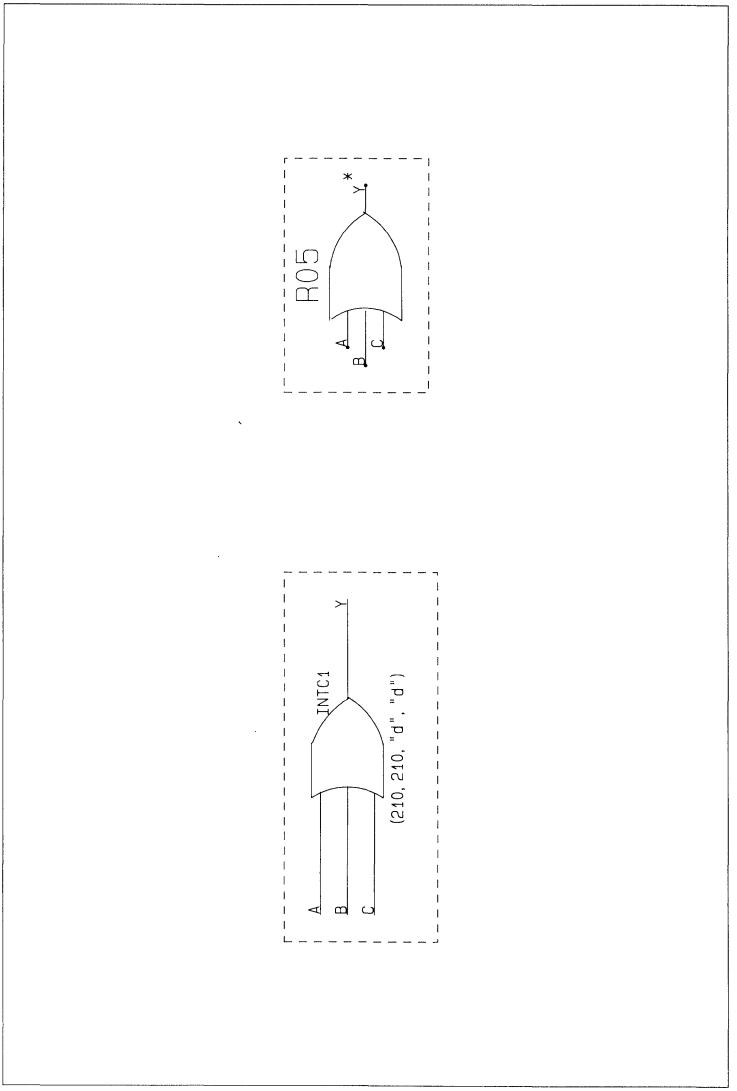
COMPONENT PLOTS

Plot 80



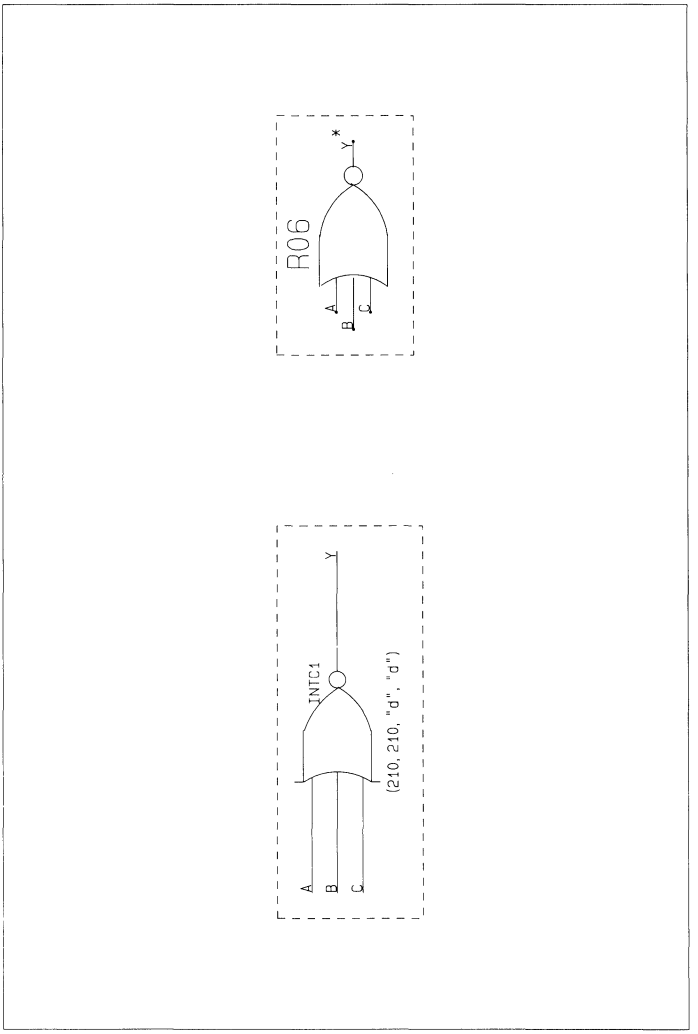
COMPONENT PLOTS

Plot 81



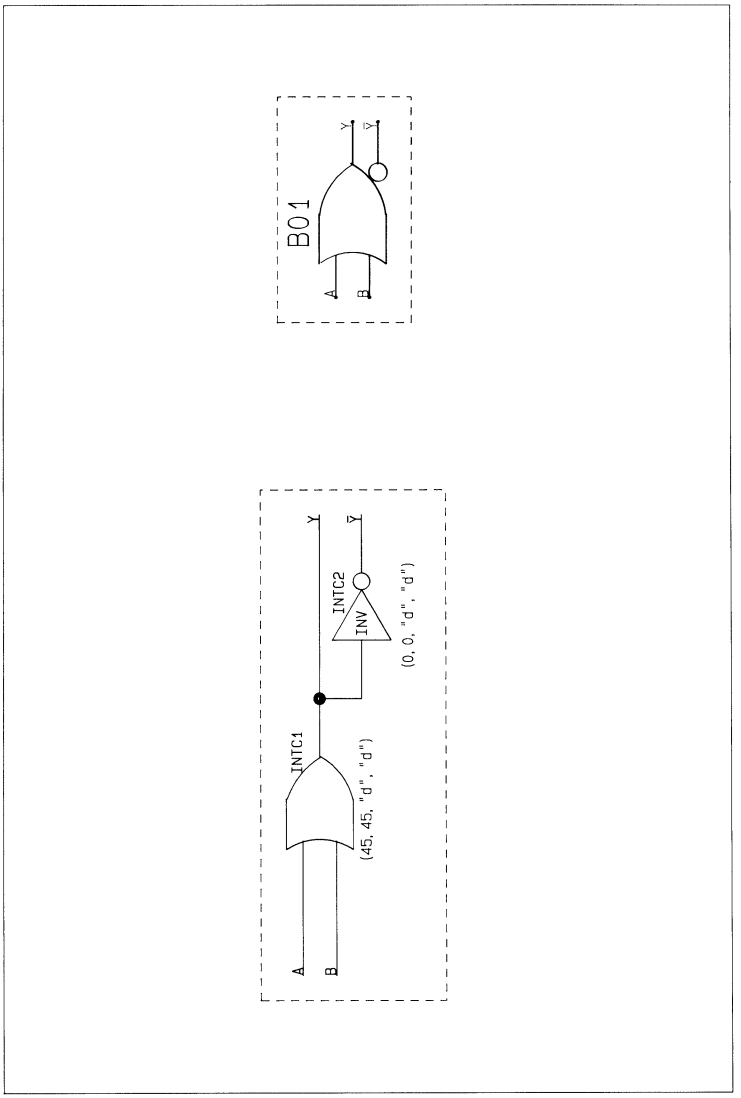
COMPONENT PLOTS

Plot 82



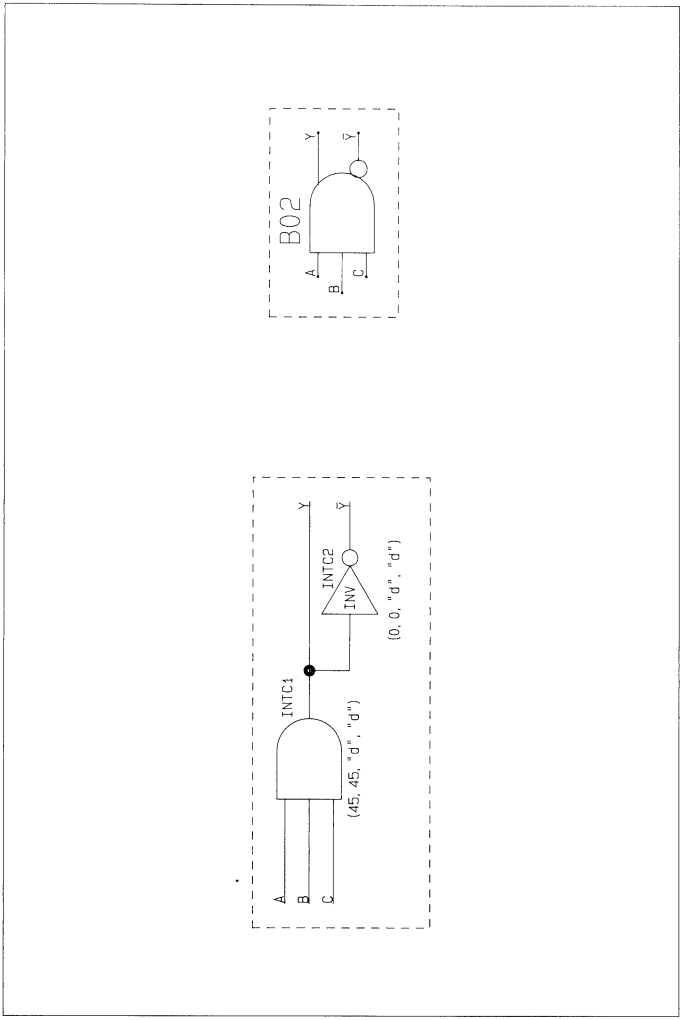
COMPONENT PLOTS

Plot 83



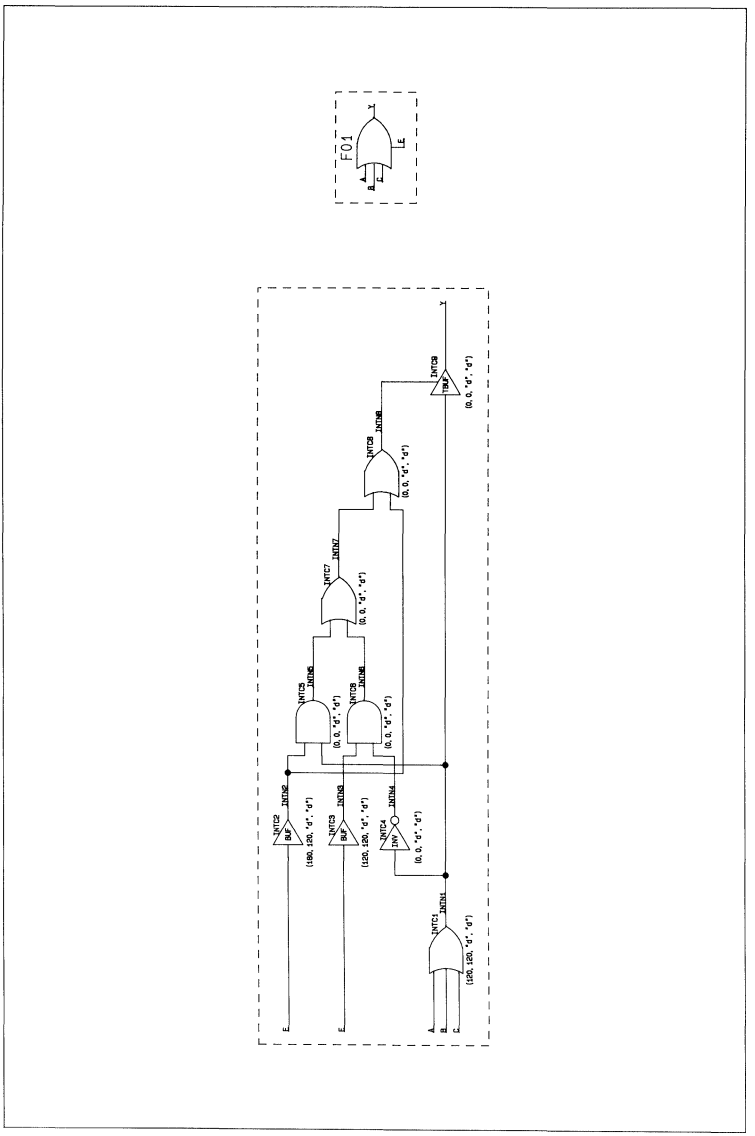
COMPONENT PLOTS

Plot 84



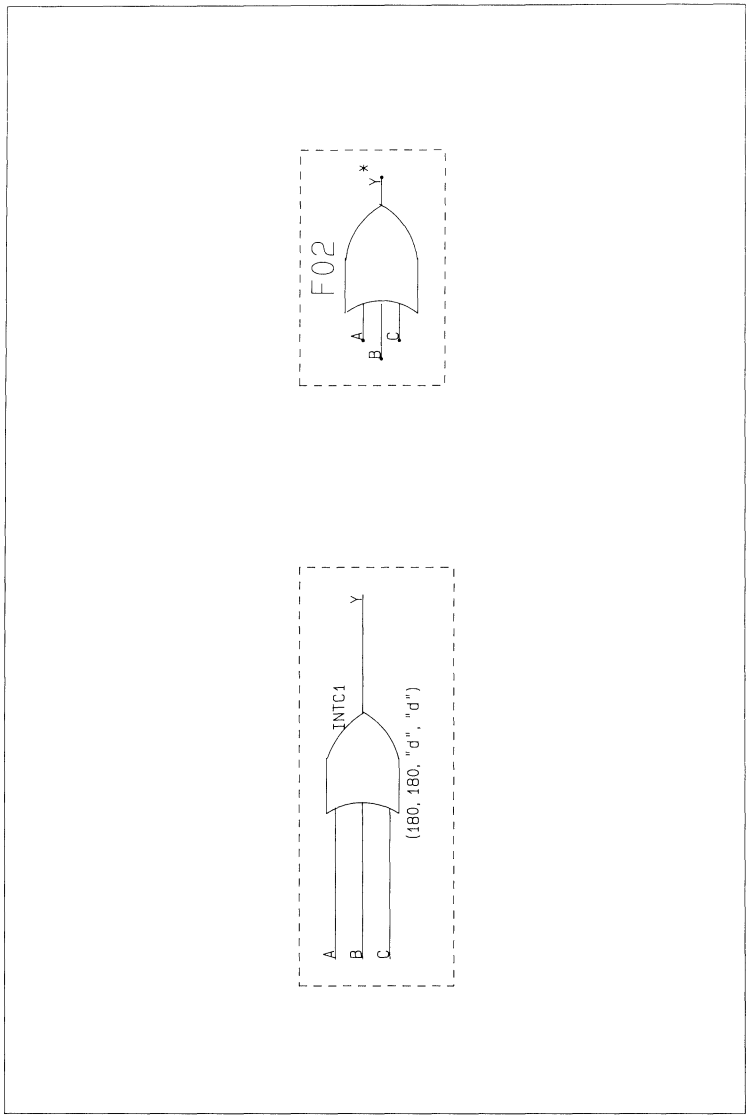
COMPONENT PLOTS

Plot 85



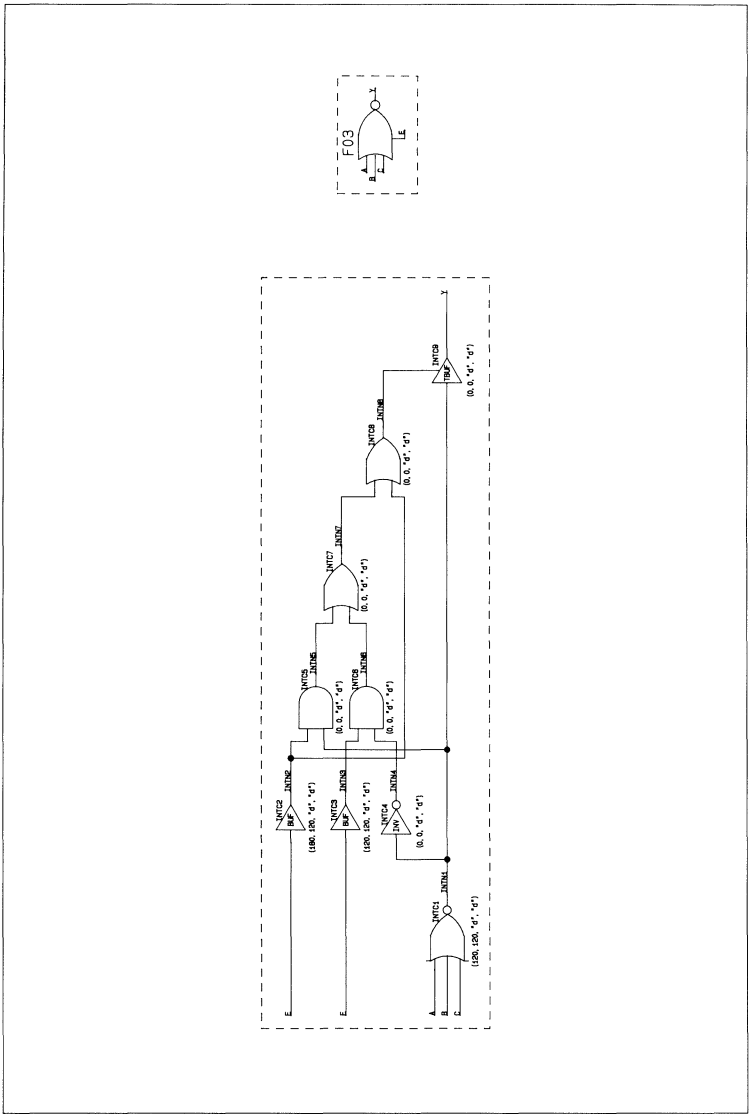
COMPONENT PLOTS

Plot 86



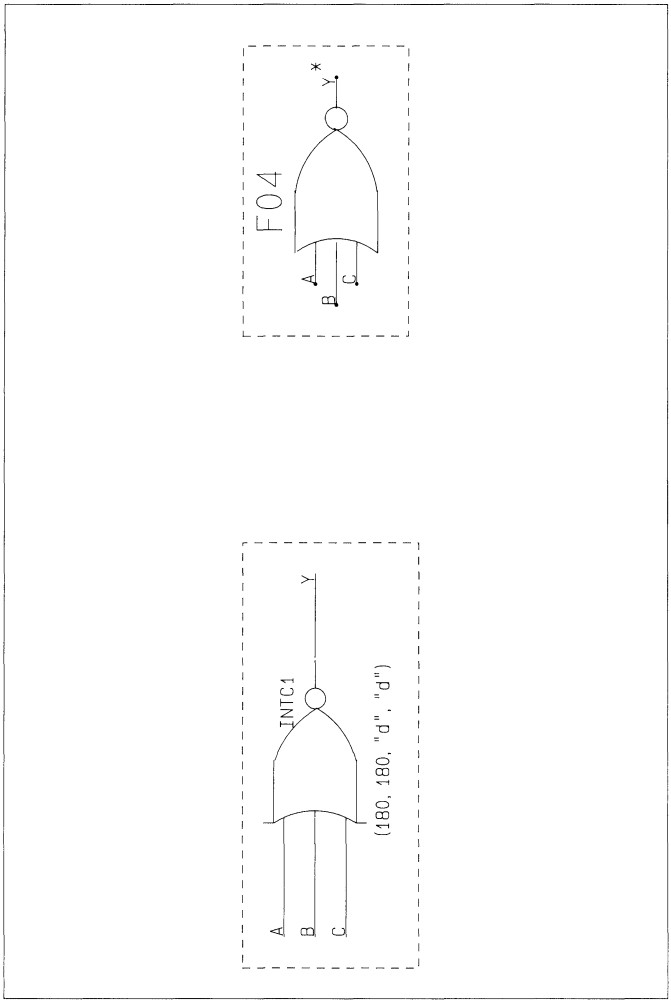
COMPONENT PLOTS

Plot 87



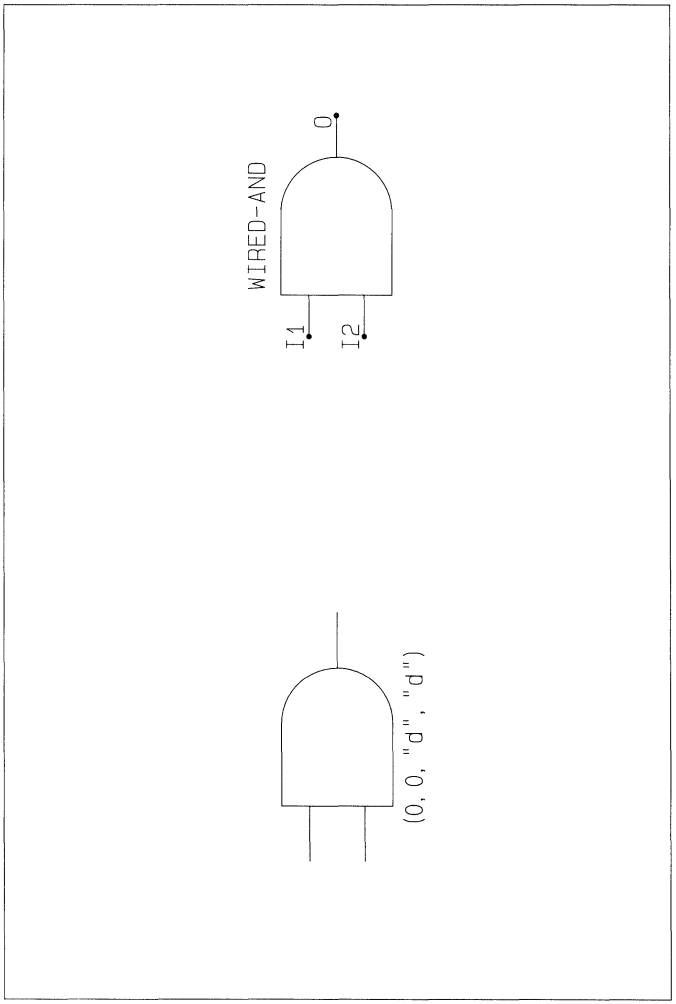
COMPONENT PLOTS

Plot 88



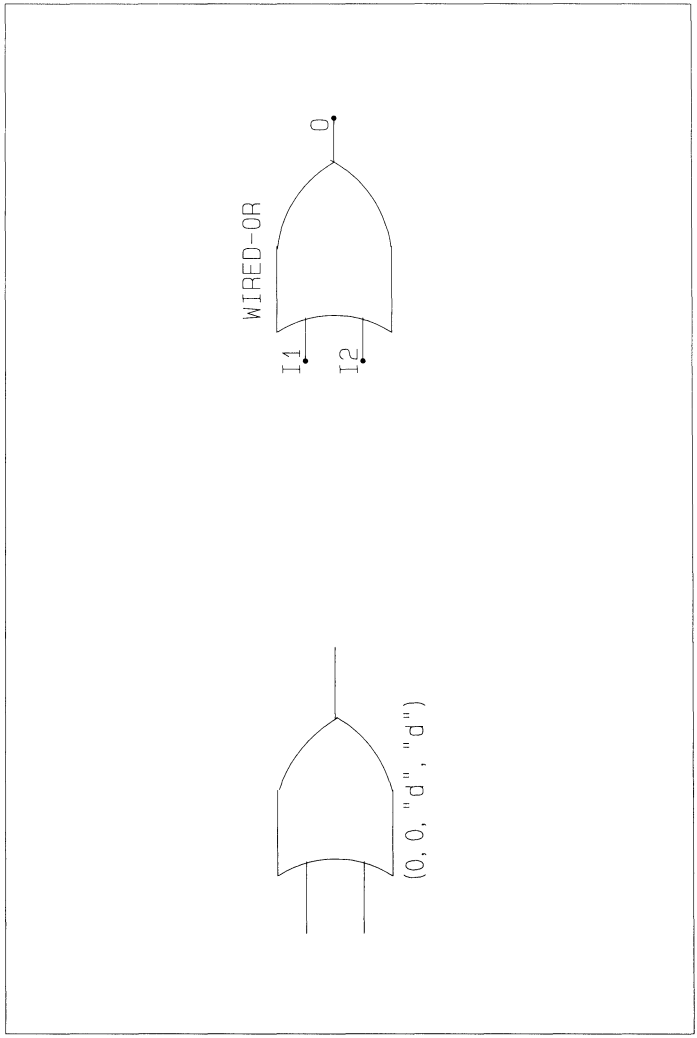
COMPONENT PLOTS

Plot 89



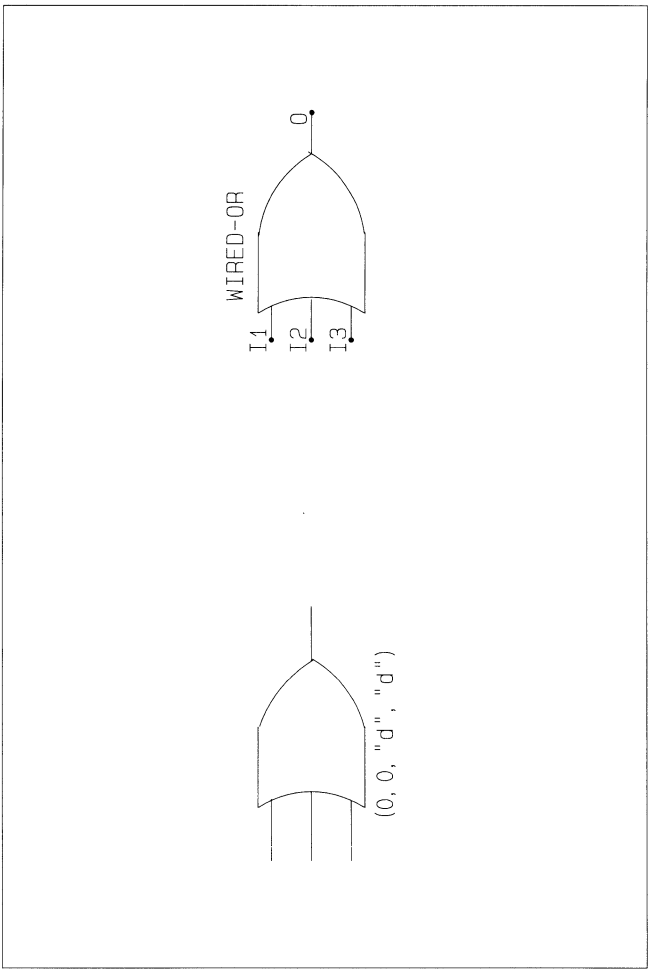
COMPONENT PLOTS

Plot 90



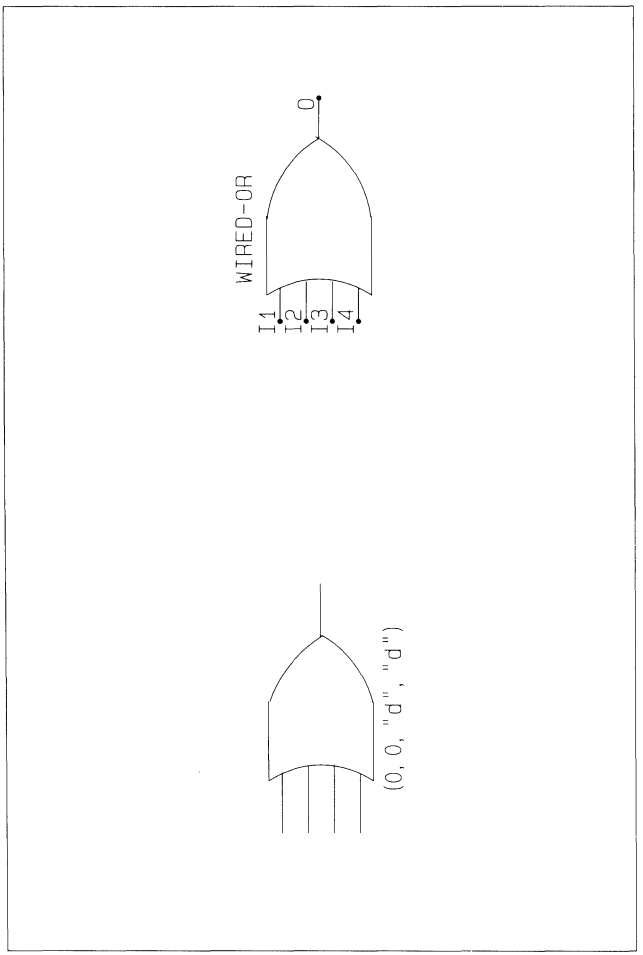
COMPONENT PLOTS

Plot 91



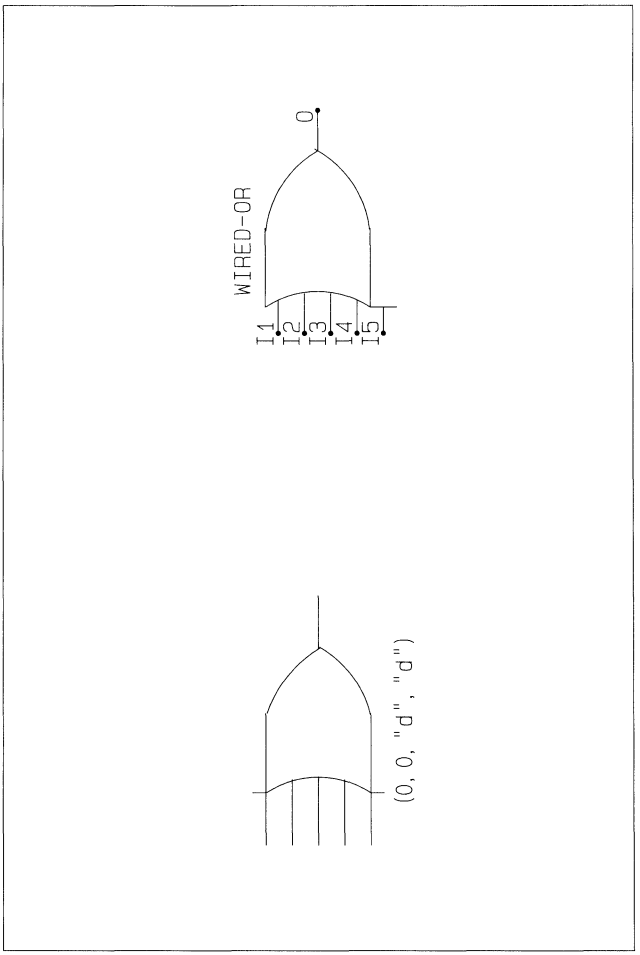
COMPONENT PLOTS

Plot 92



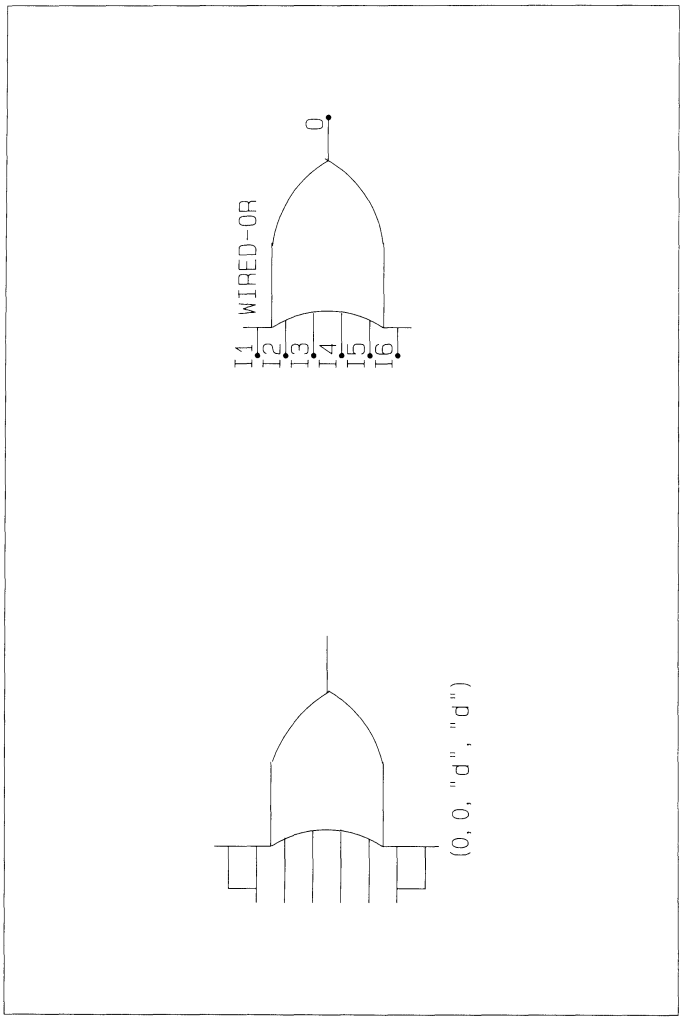
COMPONENT PLOTS

Plot 93



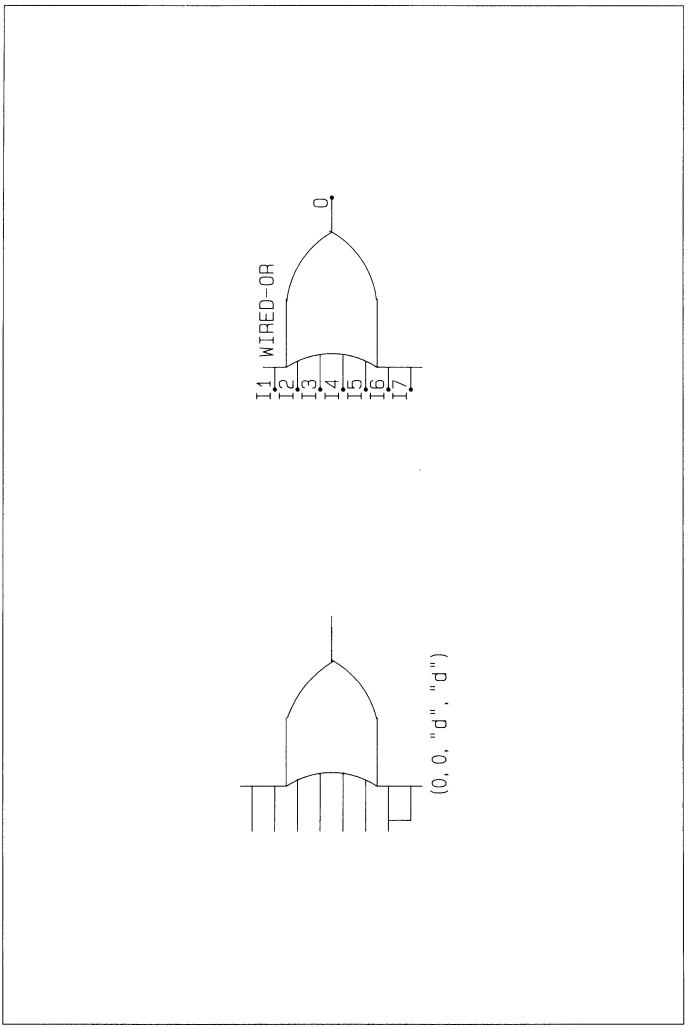
COMPONENT PLOTS

Plot 94



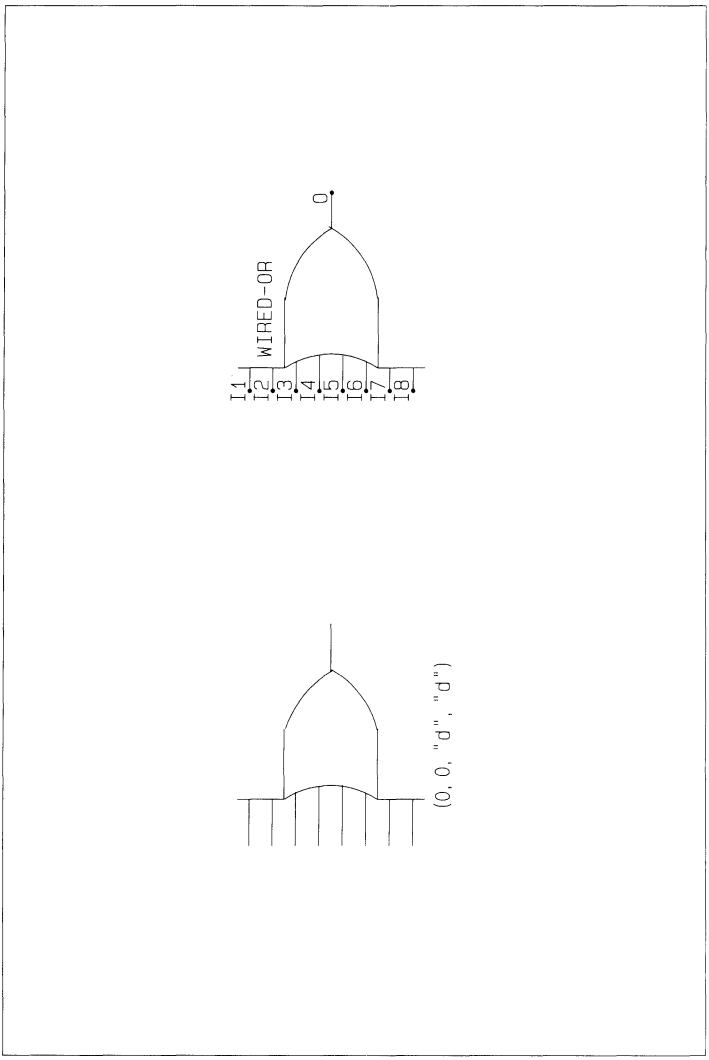
COMPONENT PLOTS

Plot 95

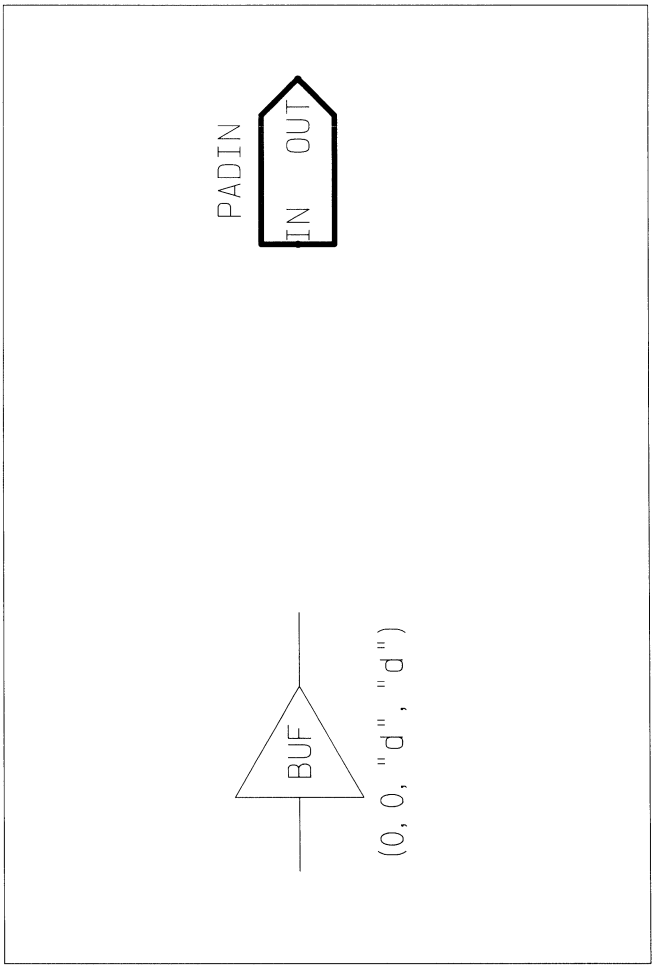


COMPONENT PLOTS

Plot 96



COMPONENT PLOTS Plot 97



COMPONENT PLOTS

Plot 98