TECHNICAL MANUAL
NS11E
MEMORY CARD ASSEMBLY

National Semiconductor
Memory Systems

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TABLE OF CONTENTS

FIGURES

TABLES

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual contains four sections which describe the NS11E Add-in Memory System. This information will include a general description, an installation and maintenence section, theory of operation, and a section containing assembly drawings, schematics, and bill of materials. Figure 1-1 is a photograph of the NS11E Add-In Memory System.

1.2 PURPOSE

The NS11E, P/N-980103839, is designed for use with DEC * PDP-11 CPU's. The NS11E is directly compatible with any DEC UNIBUS/Modified UNIBUS type backplane.

* DEC,UNIBUS, Modified UNIBUS, and PDP11 are registered trade marks of Digital Equipment Corp., Maynard Mass.

1.3 PHYSICAL DESCRIPTION

The NS11E memory is contained on one multilayer printed circuit card. See Table 1-1 for the physical dimensions of the NS11E.

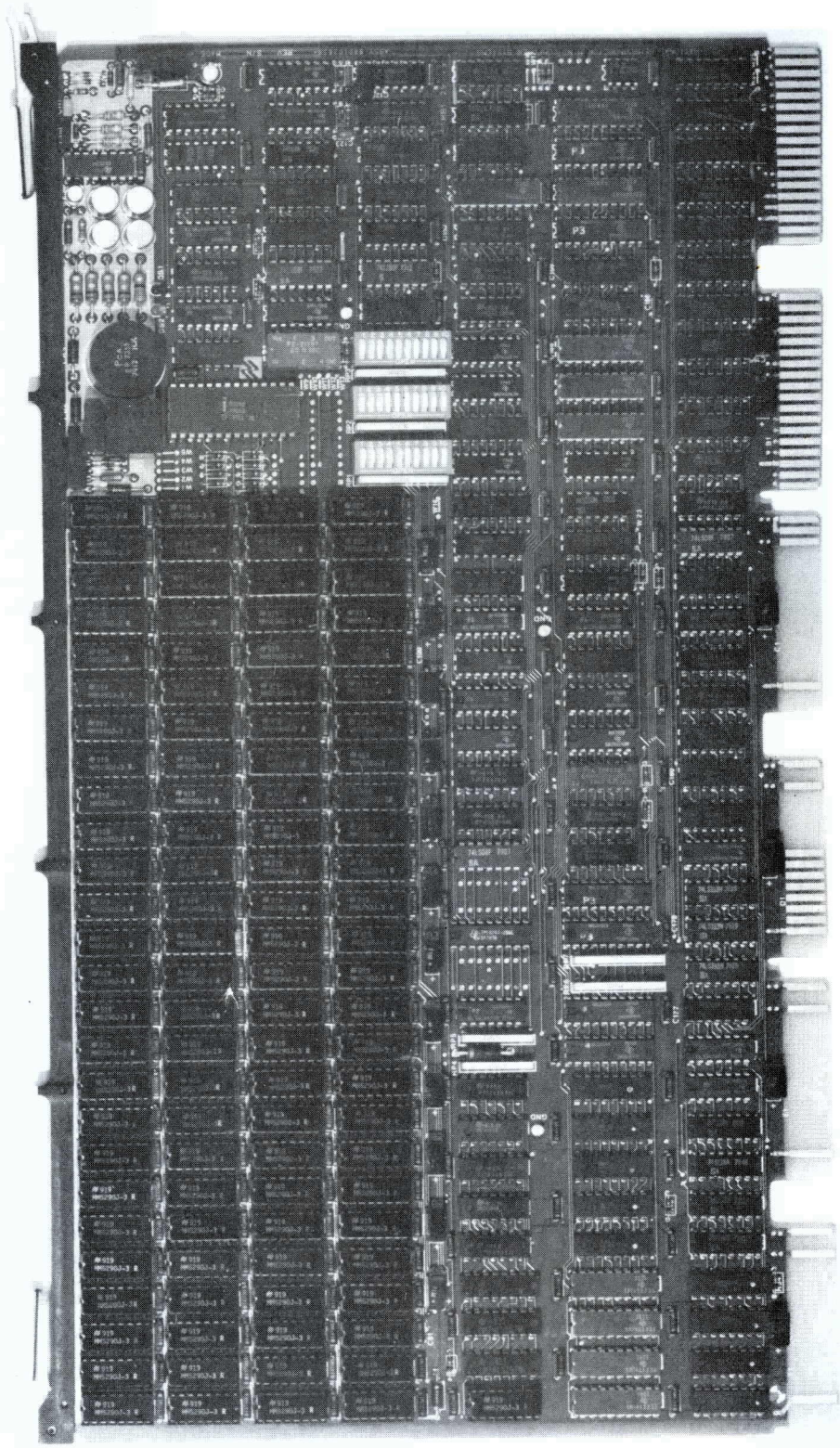


FIGURE 1-1

Table 1-1 NS11E Dimensions

Thickness	.480	inches
Height	8.680	inches
Length	15.687	inches

The NS11E memory is designed to mount on a minimum center-to-center board spacing of 0.50". Two card ejectors permit easy removal of the card.

Figure 1-2 is a connector locator diagram.

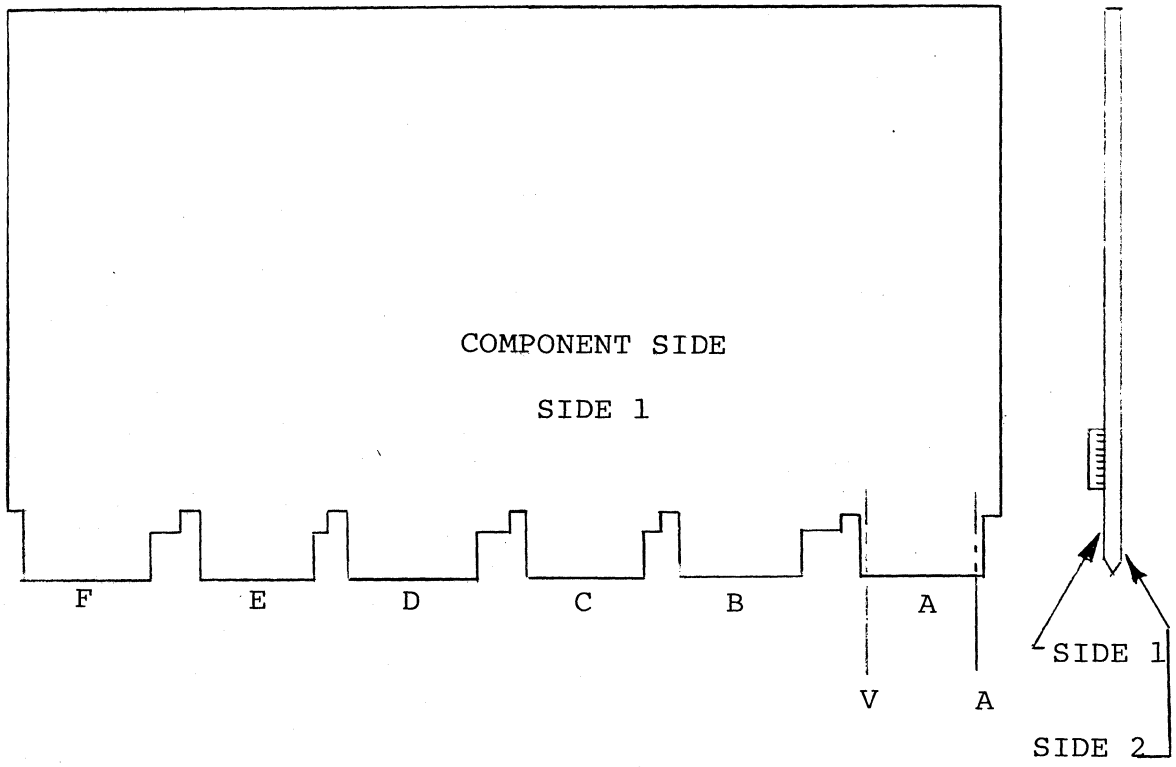


FIGURE 1-2

1.3.1 I/O Connectors

The NS11E Memory is designed to fit mechanically into the following PDP-11 backplanes:

1. DD11-DK slots 2-8
2. DD11-PK slots 3-8
3. DD11-CK slots 2-3

For installation in backplanes not listed above, the subject backplane connector pin assignments must be compatible with the NS11E pin assignments as listed in Table 3- 1.

1.4 FUNCTIONAL DESCRIPTION

The NS11E is 64K x 16* bit Add-In Memory for the DEC PDP-11 family of minicomputers. The NS11E board requires +5V only and generates the +12V and -5V with an on board DC to DC converter. The board is designed with byte ECC for maximum reliability and speed. Additionally, the board contains an on-board CSR register, eliminating the need for a DEC M-7850 parity controller. The NS11E is completely hardware and software compatible with all DEC systems as described in paragragh 1.2.

*26 bits internal, 16 bits on the Bus.

1.5 GENERAL SPECIFICATIONS

The following tables list the general specifications of the NS11E Add-In Memory. Table 1-2 lists the power requirements and Table 1-3 lists access and cycle times.

Table 1-2 NS11E Power Requirements

	Current-Amps					
Supply Voltage	Operational		Standby		Battery Back-up	
	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.
+5V	4.0	4.0	4.0	4.0	Ø	Ø
$+5V_{BB}$	2.0	3.5	1.5	1.5	1.5	1.8

Table 1-3 Access and Cycle Times

READ		
Cycle Time	450ns	MIN
Access Time	400ns	MAX
PARITY (CSR OPTION) ACCESS	100ns	MAX
Log Access	100ns	MAX
WRITE		
Cycle Time	450ns	MIN
Access Time (Add/Data Latch)	100ns	MAX
REFRESH		
Cycle Time	450ns	MIN

(Cycle requests made during a refresh will extend the cycle and access time an additional 450ns Max).

NOTE

1) Cycle time - The interval between memory reception of Bus MSYN L (at reciever input) and the availability of the memory to respond to the next Bus MSYN L.

2) Access Time - The interval between memory reception of Bus MSYN L and the assertion of Bus SSYN L.

1.5.1 Operating Modes

The operating mode of the memory is determined by the state of the C0 and C1 control lines and the A0 address line. These modes are defined in Table 1-4 shown below.

Table 1-4 Operating Modes

A0	C1	C0	COMMAND	OPERATION
X	0	0	DATI	Read
X	0	1	DATIP	Read
X	1	0	DATO	Write Word
0	1	1	DATOB 0	Write Byte 0
1	1	1	DATOB 1	Write Byte 1

NOTE: Logic 1=0 volts (LOW)
Logic 0=+ 3.4 volts (HIGH)

1.6 ENVIRONMENTAL SPECIFICATIONS

The NS11E is designed to operate over a variety of environmental conditions. Listed below are the environmental conditions and specifications.

1.6.1 Operating Specifications

- TEMPERATURE.....Ambient Air temperature range of $0^{o}C$ to $+50^{o}C$.
- THERMAL SHOCK.....The NS11E Memory can withstand a thermal shock with a maximum rate of change of $30^{o}C$ per hour during operation.

- HUMIDITY.....The Memory has been designed to operate in a relative humidity of up to 95% (without condensation).
- ALTITUDE.....This system is capable of operation at altitudes from -1,000 feet msl to +10,000 feet msl.
- COOLING.....Suggested minimum air flow for the NS11E Memory is 25 cfm.

1.6.1 Shipping and Storage Specifications

- TEMPERATURE.....The NS11E Memory can withstand a temperature range of -40^{o}C to +85^{o}C during shipment or storage.
- THERMAL SHOCK.....A thermal rate of change as high as 10^{o}C per minute can be tolerated by the Memory.
- ALTITUDE.....A Shipping Altitude of 40,000 feet can be withstood.
- MECHANICAL SHOCK....The NS11E Memory, housed in its shipping container, can tolerate mechanical shock resulting from drop tests performed in accordance with MIL-STD-810B, Method 516, procedure V, without exhibiting damage or degradation.

1.7 RELIABILITY

This card was designed to the best commercial standards of workmanship. Vigorous testing is conducted (including tests over operating temperature range) to ensure a reliable service of ten years at 24-hours per day usage (exclusive of routine maintenance time). The design is such that catastrophic

failure occurrence is minimized and minimal propagation of such failure will be experienced. Calculated MTBF using A+ logic and MIL Handbook 217B (where applicable) is 113,000 hours.

SECTION II

INSTALLATION AND MAINTENANCE

2.1 GENERAL

The NS11E Memory is ready for installation upon receipt; however, the memory size and address switches and the option jumper must be checked before the card is installed. Refer to paragraphs 2.4 thru 2.7. for switch and jumper information.

The NS11E is completely compatible with DEC's PDP 11-34 computers and all standard DEC peripheral devices. It can be used in both parity and non-parity systems.

For installation in backplanes not listed below, the subject backplane connector pin assignments must be compatible with the NS11E pin assignments listed in Table 3-1.

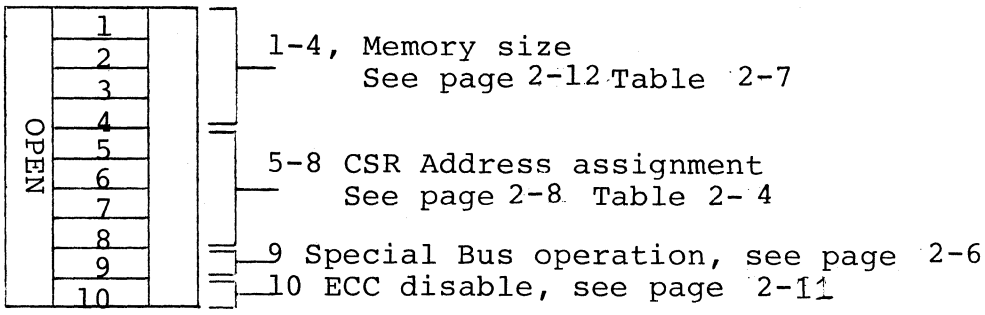
The Memory is directly plug-compatible into the following DEC backplanes:

- DD11-DK (slots 2-8)
- DD11-PK (slots 3-8)
- DD11-CK (slots 2-3)

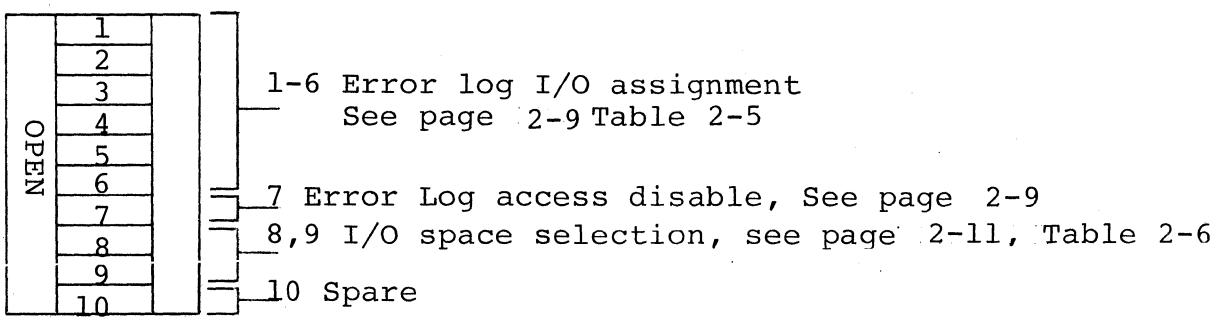
Table 2-3

SWITCH DESIGNATIONS AND LED INDICATORS

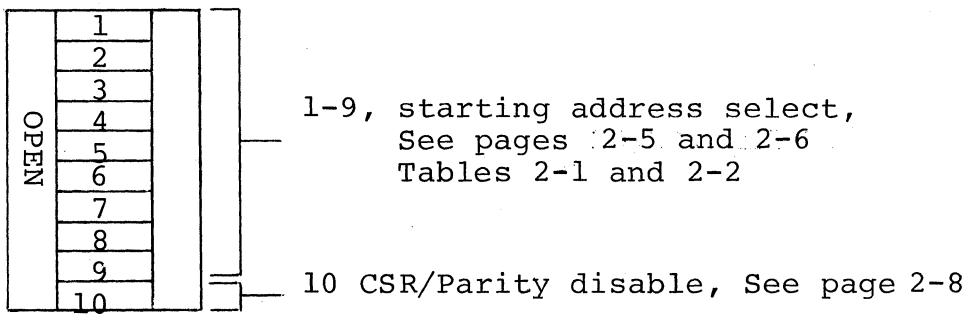
SWITCH 1



SWITCH 2



SWITCH 3



NOTE: (a) Red LED is for parity error. (CSR bit 15 set)

(b) Yellow LED is lighted for convertor failure and DC LO is asserted.

CAUTION

Do not attempt to install the NS11E Memory board into DEC backplanes listed below or damage to the equipment could result:

- MF11-U
- MF11-W

Maintenance of the NS11E is minimal, enhanced by the use of fixed timing sequences. Refer to paragraph 2. for maintenance information.

2.2 SAFETY

The following safety precautions should be observed during installation and maintenance:

WARNING

Proper concern for the safety of all personnel is vital when installing equipment. The following safety practices should always be observed, or injury could occur.

2.2.1 Power

1. Remove all power from the system before installation using the related facility and/or system circuit breakers. Remove the AC power plug from the AC receptacle. (This is particularly important when cards or components are to be removed).

2. Tag all system circuit breakers with WARNING tags to ensure that cirucit breakers will not be inadvertently turned on during installation.
3. When it is necessary to work on a system where power is present, never work alone. Two people must always be present when work is being done within a system, or on an interconnecting cable whenever system power is applied.

2.2.2 Fire

1. Good housekeeping is a significant factor in fire and accident prevention. Keep benches and working areas clear of unnecessary articles.
2. Ensure fire extinguishers of the CO_2 type (for electrical fires) are readily available.

2.3 UNPACKING AND INSPECTION

Follow the steps listed below to unpack and inspect the NS11E Memory board:

1. Remove all packing materials. (Failure to do so could result in damage to the equipment and present a fire hazard); store the reusable packing materials for future use.
2. Remove the Memory board from its container.
3. Inspect the board for visual damage, checking for bent stiffener, damaged IC's,broken wires or connectors,

dislocated or broken switches or indicators, etc. Certain damage may not be detected until power has been applied and diagnostics performed.

NOTE: Visually damaged or inoperative boards should be returned to: NATIONAL SEMICONDUCTOR
2900 Semiconductor Drive
Santa Clara, California 95051

2.4 ADDRESS AND I/O SWITCH CONFIGURATIONS

2.4.1 Address

The NS11E Memory will accept a full 22 bit address with the least significant bit being used for Byte selection. The address lines to the memory are single rail; the addressing mode may be random. The address lines are identified as A0 through A21.

The NS11E may be used for expansion to 2M words using the 22 bits of address. When this expansion is used, address I/O pin assignments are as follows:

BUS A18-BE2
BUS A19-BE1
BUS A20-AP1
BUS A21-AN1

A0 is used for Byte selection. A1 through A21 are decoded for one of 2,097,152 address locations.

A13 through A21 are 'strappable' on the memory module. These address lines may be strapped to set the initial address for a memory module. Nine switch positions located at S3 are provided to set the initial address. Four positions are used for initial address selection in the 0-64K address range. The remaining five positions can be used for expansion to 2M word See Table 2-1 for 0-64K Select. See Table 2-2 for expansion to 2M word. Address selection is in 64K blocks to 2M word. Addresses A17 thru A21 are switch settable via switches per Table 2-2. Address buffer for A18-A21 must be enabled by closing switch 1-9 (LO). For system expansion beyond 64K, Table 2-1 is used in conjunction with Table 2-2 to ascertain required switch settings.

Table 2-3 is a general guide to the address and I/O switch configurations, and lists the pages of this guide for switch selection. (See page 2-2)

Table 2-1 STARTING ADDRESS SELECT

UNIBUS STARTING ADD (OCTAL)	MEMORY STARTING ADDRESS	SWITCH 3 S3-4	S3-3	S3-2	S3-1
000000	0K	off	off	off	off
020000	4K	off	off	off	on
040000	8K	off	off	on	off
060000	12K	off	off	on	on
100000	16K	off	on	off	off
120000	20K	off	on	off	on
140000	24K	off	on	on	off
160000	28K	off	on	on	on
200000	32K	on	off	off	off
220000	36K	on	off	off	on
240000	40K	on	off	on	off
260000	44K	on	off	on	on
300000	48K	on	on	off	off
320000	52K	on	on	off	on
340000	56K	on	on	on	off
360000	60K	on	on	on	on

off = OPEN
on = CLOSED

Table 2-2 STARTING ADDRESS SELECT

SPECIAL BUS STARTING ADDR (OCTAL)	MEMORY STARTING ADDRESS	ADD A21 SW S3-9	A20 S3-8	A19 S3-7	A18 S3-6	A17 S3-5
00400000	64K	off	off	off	off	on
01000000	128K	off	off	off	on	off
01400000	192K	off	off	off	on	on
02000000	256K	off	off	on	off	off
02400000	320K	off	off	on	off	on
03000000	384K	off	off	on	on	off
03400000	448K	off	off	on	on	on
04000000	512K	off	on	off	off	off
04400000	576K	off	on	off	off	on
05000000	640K	off	on	off	on	off
05400000	704K	off	on	off	on	on
06000000	768K	off	on	on	off	off
06400000	832K	off	on	on	off	on
07000000	896K	off	on	on	on	off
07400000	960K	off	on	on	on	on
10000000	1024K	on	off	off	off	off
10400000	1088K	on	off	off	off	on
11000000	1152K	on	off	off	on	off
11400000	1216K	on	off	off	on	on
12000000	1280K	on	off	on	off	off
12400000	1344K	on	off	on	off	on
13000000	1408K	on	off	on	on	off
13400000	1472K	on	off	on	on	on
14000000	1536K	on	on	off	off	off
14400000	1600K	on	on	off	off	on
15000000	1664K	on	on	off	on	off
15400000	1728K	on	on	off	on	on
16000000	1792K	on	on	on	off	off
16400000	1856K	on	on	on	off	on
17000000	1920K	on	on	on	on	off
17400000	1984K	on	on	on	on	on

off = OPEN
on = CLOSED

2.5 CSR ADDRESS ASSIGNMENT

The NS11E contains an on board CSR, which contains error information in the event of a parity (double bit) error. There are 16 possible CSR addresses as listed in Table 2-4. When a NS11E is used in conjunction with DEC parity memory and a DEC M7850 parity controller, or multiple NS11E's, the CSR addresses of the M7850 and NS11E's must not be the same. The CSR can be disabled by closing switch 3-10.

Table 2-4

CSR ADDRESS (SWITCH 1)

SWITCH 1 CSR ADDRESS SELECTION

8765	UNIBUS ADDRESS	SPECIAL BUS ADDRESS
0000	772100	17772100
0001	772102	17772102
0010	772104	17772104
0011	772106	17772106
0100	772110	17772110
0101	772112	17772112
0110	772114	17772114
0111	772116	17772116
1000	772120	17772120
1001	772122	17772122
1010	772124	17772124
1011	772126	17772126
1100	772130	17772130
1101	772132	17772132
1110	772134	17772134
1111	772136	17772136

1=OPEN
0=CLOSED

NOTE: CSR address has no relevance to the memory starting address or storage capacity of the NS11E.

2.6 LOG I/O SPACE ASSIGNMENT

Since the error log is addressable via the bus there are 64 address locations assigned in the user address boundary as listed in Table 2-5. Switch 2-7 when closed inhibits log Reads or Writes via the bus.

Table 2-5

ERROR LOG ADDRESS ASSIGNMENT

	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1	BUS ADDR (OCTAL)
1	0	0	0	0	0	0	764000
2	0	0	0	0	0	1	764002
3	0	0	0	0	1	0	764004
4	0	0	0	0	1	1	764006
5	0	0	0	1	0	0	764010
6	0	0	0	1	0	1	764012
7	0	0	0	1	1	0	764014
8	0	0	0	1	1	1	764016
9	0	0	1	0	0	0	764020
10	0	0	1	0	0	1	764022
11	0	0	1	0	1	0	764024
12	0	0	1	0	1	1	764026
13	0	0	1	1	0	0	764030
14	0	0	1	1	0	1	764032
15	0	0	1	1	1	0	764034
16	0	0	1	1	1	1	764036
17	0	1	0	0	0	0	765000
18	0	1	0	0	0	1	765002
19	0	1	0	0	1	0	765004
20	0	1	0	0	1	1	765006
21	0	1	0	1	0	0	765010
22	0	1	0	1	0	1	765012
23	0	1	0	1	1	0	765014
24	0	1	0	1	1	1	765016
25	0	1	1	0	0	0	765020
26	0	1	1	0	0	1	765022
27	0	1	1	0	1	0	765024
28	0	1	1	0	1	1	765026
29	0	1	1	1	0	0	765030
30	0	1	1	1	0	1	765032
31	0	1	1	1	1	0	765034
32	0	1	1	1	1	1	765036
33	1	0	0	0	0	0	766000
34	1	0	0	0	0	1	766002
35	1	0	0	0	1	0	766004
36	1	0	0	0	1	1	766006
37	1	0	0	1	0	0	766010
38	1	0	0	1	0	1	766012
39	1	0	0	1	1	0	766014
40	1	0	0	1	1	1	766016
41	1	0	1	0	0	0	766020
42	1	0	1	0	0	1	766022
43	1	0	1	0	1	0	766024
44	1	0	1	0	1	1	766026
45	2	0	1	1	0	0	766030
46	2	0	1	1	0	1	766032
47	1	0	1	1	1	0	766034
48	1	0	1	1	1	1	766036
49	1	1	0	0	0	0	767000
50	1	1	0	0	0	1	767002
51	1	1	0	0	1	0	767004
52	1	1	0	0	1	1	767006
53	1	1	0	1	0	0	767010
54	1	1	0	1	0	1	767012
55	1	1	0	1	1	0	767014
56	1	1	0	1	1	1	767016
57	1	1	1	0	0	0	767020
58	1	1	1	0	0	1	767022
59	1	1	1	0	1	0	767024
60	1	1	1	0	1	1	767026
61	1	1	1	1	0	0	767030
62	1	1	1	1	0	1	767032
63	1	1	1	1	1	0	767034
64	1	1	1	1	1	1	767036

NOTE: 1=OPEN
0=CLOSED

2.7 I/O CONFIGURATIONS

A. Space Selection

The NS11E has a normal reserved I/O space of 4K but can be selectable to either 8K or 2K. The I/O space normally resides between 124K and 128K for Unibus operation. I/O space will reside at the top of the 2M words for 22-Bit address operation. See Table 2-6.

Table 2-6

I/O SPACE	SWITCH-2	
	9	8
8K	off	off
4K	off	on
2K	on	on

OFF=OPEN
ON=CLOSED

B. ECC Disable

ECC can be disabled by closing switch S1-10.

C. Memory Size Selection

The NS11E can be configured in 4K increments to 64K. Memory size must be set according to actual board capacity. See Table 2-7.

Table 2-7

Switch 1				Memory
S1-4	S1-3	S1-2	S1-1	Size
off	off	off	off	4K
off	off	off	on	8K
off	off	on	off	12K
off	off	on	on	16K
off	on	off	off	20K
off	on	off	on	24K
off	on	on	off	28K
off	on	on	on	32K
on	off	off	off	36K
on	off	off	on	40K
on	off	on	off	44K
on	off	on	on	48K
on	on	off	off	52K
on	on	off	on	56K
on	on	on	off	60K
on	on	on	on	64K

ON=CLOSED
OFF=OPEN

2.8 INSTALLATION

Perform the following steps in the order listed to install the NS11E Memory board:

1. Verify that the PDP11 system is performing properly by running the appropriate memory diagnostics before any changes to the CPU configuration are made.

2. Verify that jumper connections and switch settings are correct according to the memory starting address, memory size, CSR address, ECC operation, error log address, I/O space, and battery back-up. As per sections 2.4 thru 2.7.
3. Turn off CPU power.
4. Carefully slide the memory into the selected slot. Be sure that the component side faces the correct direction, that the board is aligned in the card guides. Insert and remove slowly so contact is not made with adjacent boards. When the memory has engaged the connectors, press firmly on the card and seat it by exerting equal pressure on the two ejectors.
5. Replace any cables, covers, panels, etc., which were moved during installation. Turn on CPU power.
6. Perform post-installation checks listed in paragraph 2.9.

2.9 POST INSTALLATION CHECKS

Post installation checks consist primarily of checking operation of the memory unit as an integral part of the data processing system in which it is installed. Since the functional checks depend upon the data processing system configuration and user application, the test routines to be used are left to the discretion of the user. Owing to the all-electronic nature of the memory unit, there are no mechanical checks or inspections to be performed once the unit is installed.

NOTE: Any unused modified bus backplane slot must have a bus grant card in location D, or CPU will show bus error.

Again verify that the system is performing properly by running the appropriate memory diagnostics.

2.10 MAINTENANCE

The maintainability of the NS11E Memory is enhanced by the use of fixed timing sequences. Since all timing is controlled by the user, and one card type is used, complete interchangeability is realized. A spare card can be used in place of a failing unit without the need for any timing adjustments.

The memory devices are all mounted in sockets, and the peripheral devices are in common use so that repairs can be effected on-site.

Paragraph 2.10.1 contains a listing of steps to follow prior to troubleshooting at the component level.

2.10.1 Preliminary Checks

If the memory fails, the following preliminary procedure should be followed before component-level troubleshooting:

1. Check the memory installation; it must be installed facing the correct direction. (Memory components are facing the same direction as the CPU board components.)

2. Remove memory and visually inspect; wipe edge-connector with clean cloth.
3. Recheck the jumper connections and switch settings. (Refer to paragraph s 2.4, thru 2.7.
4. Reinstall the Memory carefully seating module in the chassis connectors.
5. Using the peripheral equipment, interrogate various address areas of the memory. (This will assure the module is fully operational.)
6. When possible, switch with another module known to be operating properly. (Use the results to determine whether the problem is in the module or in the processor interface.)

2.10.2 Pretested Memory Replacement

One pretested memory device is plugged into an on-board socket for spare requirements. This spare memory device can be used to replace any failing memory devices in the field. The spare memory is at location ul31.

Figure 2-1 may be used for locating defective memory devices.

2.11 ERROR LOG UTILIZATION

The NS11E error log can be polled from either the CPU front panel, a remote terminal, or by software:

- Utilization of the error log software package, as supplied by NSC, is discussed in TN79-002.

- The error log automatically clears itself during a power-up sequence. However; due to some CPU operations during system initialization, the error log may have to be manually cleared to ensure log data integrity. Most operating systems, and some boot routines (to determine the size of available memory), will begin system initialization by READING blocks of memory. Since the NS11E storage medium is comprised of volatile RAM, which contains random data after power is applied, there is a high probability that any Memory Read will produce an error, which will be logged.
- After the power-up sequence, boot, and memory-sizing has been completed, the error log(s) may be reinitialized by depositing 000002_8 in the appropriate error log register. Table 2-5 gives a list of the possible Error Log address assignments.
- It should also be noted that the same problem exists when running a DEC memory diagnostic which contains a parity memory test. This diagnostics will check the functionality of the parity CSR register by writing wrong parity into memory and checking that the CSR registers the error on the subsequent READ. Because the diagnostic clears the "write wrong parity" bit (02) on the CSR prior to reading, the error log will also record the errors as double-bit errors. To utilize the error log capabilities while running DEC memory diagnostics, the following steps must be taken:

a) Power up system and load diagnostics.

b) Set CPU front panel switch registers (or software switch registers) to indicate that non-parity memory is present.

c) Start diagnostic run. Stop CPU after memory size has been printed.

d) Clear the appropriate error log registers (one each for each NS11E by depositing 000002_8 in each error log register.

e) Press CONTINUE on the CPU console. The diagnostic will now continue running with all error log registers reset.

NOTE: After several passes through the diagnostics, the contents of the error log registers should be examined. Paragraph 2.11.1, below, describes the error log register.

2.11.1 Error Log Operation and Testing

Each memory has an on-board error log for recording single and multiple Bit errors that occur in memory. The log functional operations; other than logging errors, are software controlled via bus protocol. Upon power-up, the error log executes a Clear/Write and bus DC LO is held LOW until this operation is complete. See to Figures 2- 1 and 2- 2 for log operation and Data interpretation.

Error log register Data Bit assignment is as follows:

a) Bits 0-4 (read) are syndrome Bits for Byte 0

b) Bits 8-12 (read) are syndrome Bits for Byte 1

c) Bits 6 & 7 are most significant Address (row indicator)

d) Bit 15 "ERROR IN LOG" indication

e) Bit 14 is "END OF LOG PASS" for scan or clear

f) Bit 0, when written, is a log scan command (Logic 1)

g) Bit 1, when written, is a log clear command (Logic 1)

h) Bit 13 is always read as a logical 0

i) Bit 5 "ERROR FOUND" indication

NOTES: 1) Bits 2-15 are Read only Bits

2) Bits 0, and 1 are the only Bits that can be written from the bus and are transparent to the bus (i.e. bus Data written in log Bits 0 and 1 cannot be read).

2.11.2 Error Log Operation Description

The following is an operational description of the error log: (see Figure 2-2).

1) Bit 14 is always set unless the log is in the process of scanning or clearing (i.e. Bit 0 or 1 has been set).

2) Processor reads log register to see if Bit 15 is set - ignores all other Data Bits; if Bit 15 is set there are one or more errors in the log.

3) Set log register Bit 0 to start log scanning for errors, Bit 14 will clear, log counter resets to 0 and log begins error search.

4) Log register may be read during scan but Data may be delayed by log cycle in progress by up to 500 ns.

5) If Bit 14 is not set, scan is not complete. If Bit 5 is not set, error has not been found.

6) Log scan in progress will stop if the log register is Read via the Unibus, but will continue when Read log register bus protocol is complete.

7) If error is found, Bit 5 will be set, log scan will stop and error Data is available in log register.

8) To continue scan, Bit 0 must again be asserted.

9) When log scan is complete, Bits 14 and 15 will be set.

10) If a Clear/Write of log is to be executed, Bit 1 is set. When CLR log is complete, Bits 5, 13 and 15 will be cleared; the remaining bits will be set.

11) Error logging is disabled during log scan or clear and when the parity CSR Bit 2 is set (for Write/Wrong parity diagnostic. NOTE: If diagnostic does not leave CSR Bit 2 set for both Read and Write, error log will fill with errors and must be cleared).

12) If the syndrome Bit Data combination is even, a multiple Bit error has occurred and only the most significant address information is valid (Log Bits 6 and 7).

13) If the error log stops on an error and a clear is required and bit 14 is not set, Bit 1 must be set twice to clear the complete log.

14) Error log access is disabled when switch 2-7 is closed.

2.11.3 Error Log Interrogation

This paragraph provides an example of an error log interrogation via the CPU front panel. The assumptions are that there is only one NS11E installed and the E.L. register address is 764000_8.

Step Number	Comments
1	Examine the contents of 764000.
2	Is Bit 15 set? If not, then there is no error information in the register and the interrogation is complete. If Bit 15 is set, then at least one error has occurred.
3	Deposit 000001_8 (set bit 0) @ 764000. This will start the error log scan. The scan will continue until the first error is found.
4	Examine 764000. Is Bit 5 set? If not, re-examine the location until Bit 5 is set. NOTE: Because Front Panel manual operations are so slow, Bit 5 should always be set since the log scan caused by step 3 can only take a maximum of 2 ms. If Bit 5 is set, the rest of the data can be interpreted per Figure 2-1. An example of data interpretation is:

Bit No.	15	14	13	12	11	12	9	8	7	6	5	4	3	2	1	0
Data	1	0	0	1	1	0	1	1	0	1	1	1	0	1	0	1

Bits 0-4 are the syndrome bits for byte 0. An odd number of bits has been set, so the error is a single bit error. Using bits 0-4 in conjunction with Bits 6 and 7 and

Step Number	Comments
	and Figure 2-1, shows the faulty RAM to be U28. See assembly for RAM location. Examination of bits 8-12 shows an even number of syndrome bits sets, therefore; a double-bit or uncorrectable error has occurred in ROW 01.
	NOTE: If the syndrome bits in a byte are all 0's, then no error occurred in that particular byte.
5	Is Bit 14 set? If not, the log has not reached the end of it's scan. Repeat steps 3 and 4, noting if Bit 14 does set, the scan is complete.
6	To clear the log, deposit 000002_8 (set bit 1) @ 764000. Since the log will only clear from its present scan address to the last scan address, it is suggested that bit 1 be set twice in succession to ensure that the log is completely clear. The log register should now contain 057737.

Figure 2-1

LOG REGISTER BIT TO MEMORY CHIP LOCATOR

(Reference Figure 1-1)

Spare RAM is at Loaction U131

LOG REG BIT														
BIT 0	1	1	0	1	0	1	1	0	1	0	0	0	0	
BIT 1	1	0	1	0	1	1	0	1	0	1	0	0	0	
BIT 2	0	1	1	0	0	0	1	1	0	0	1	0	0	
BIT 3	0	0	0	1	1	1	1	1	0	0	0	1	0	
BIT 4	1	1	1	1	1	0	0	0	0	0	0	0	1	
	0	1	2	3	4	5	6	7	C0	C1	C2	C3	C4	MEMORY BIT
0 0	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	
0 1	U27	U28	U29	U30	U31	U32	U33	U34	U35	U36	U37	U38	U39	
1 0	U53	U54	U55	U56	U57	U58	U59	U60	U61	U62	U63	U64	U65	ARRAY
1 1	U79	U80	U81	U82	U83	U84	U85	U86	U87	U88	U89	U90	U91	
BIT BIT 7 6 LOG REG							BYTE 0							

LOG REG BIT														
BIT 8	1	1	0	1	0	1	1	0	1	0	0	0	0	
BIT 9	1	0	1	0	1	1	0	1	0	1	0	0	0	
BIT 10	0	1	1	0	0	0	1	1	0	0	1	0	0	
BIT 11	0	0	0	1	1	1	1	1	0	0	0	1	0	
BIT 12	1	1	1	1	1	0	0	0	0	0	0	0	1	
	8	9	10	11	12	13	14	15	C5	C6	C7	C8	C9	MEMORY BIT
0 0	U14	U15	U16	U17	U18	U19	U20	U12	U22	U23	U24	U25	U26	
0 1	U40	U41	U42	U43	U44	U45	U46	U47	U48	U49	U50	U51	U52	
1 0	U66	U67	U68	U69	U70	U71	U12	U13	U74	U75	U76	U77	U78	ARRAY
1 1	U92	U93	U94	U95	U96	U97	U98	U99	U100	U101	U102	U103	U104	
BIT BIT 7 6 LOG REG							BYTE 1							

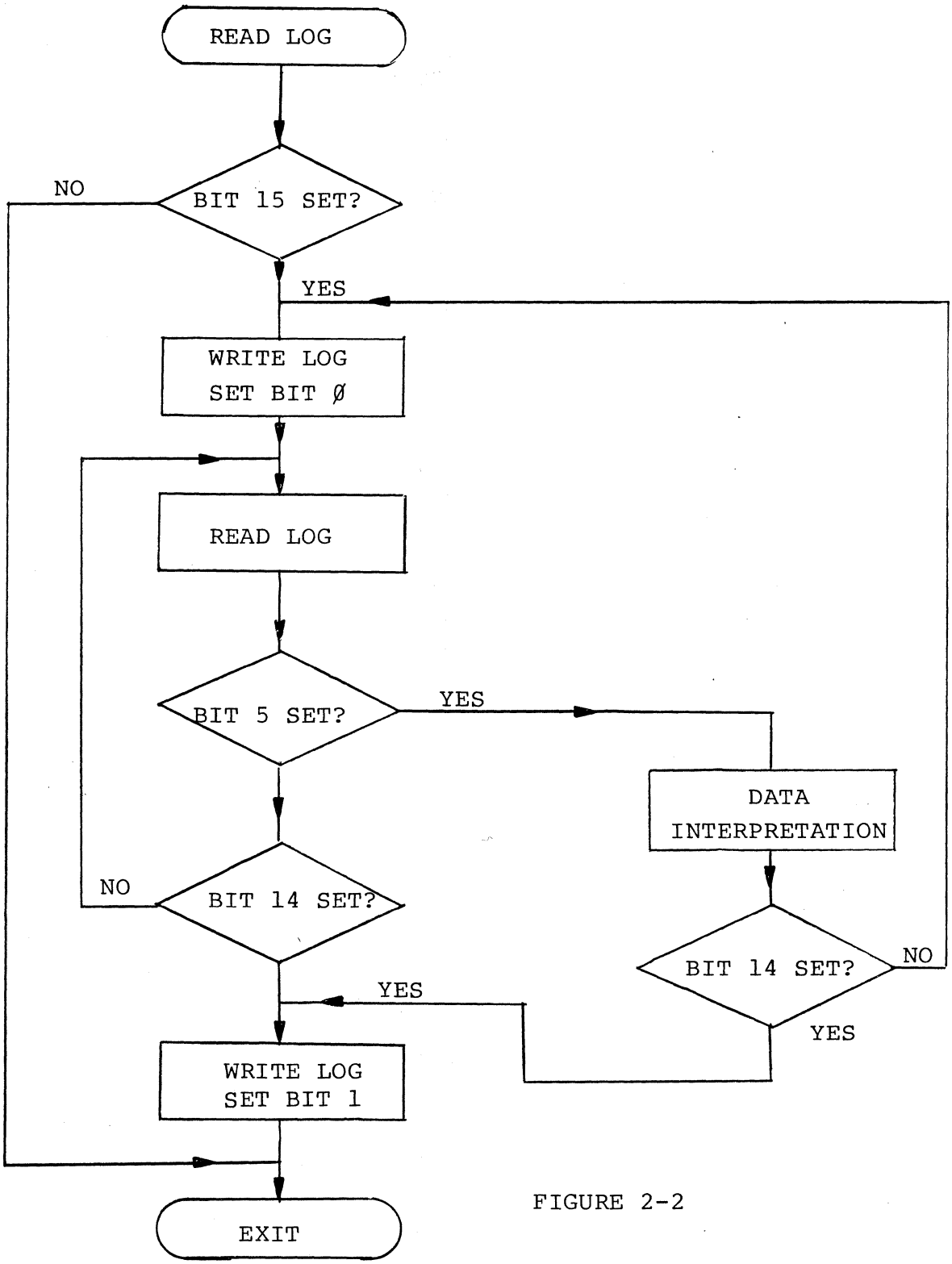

READ LOG
BIT 15 SET?
NO
YES
WRITE LOG
SET BIT Ø
READ LOG
BIT 5 SET?
YES
DATA
INTERPRETATION
BIT 14 SET?
NO
BIT 14 SET?
NO
YES
YES
WRITE LOG
SET BIT 1
EXIT

FIGURE 2-2

SECTION III

THEORY OF OPERATION

3-1 GENERAL

This section comprises a functional description of the memory card assembly. Description is divided into general discussion and detailed circuit description, each referring to appropriate block, simplified logic, logic, schematic, and timing diagrams. The schematic diagram is located in section IV.

3-2 INTERFACE

3.2.1 Unibus; Standard, Modified and Special Bus

The DEC PDP-11 Unibus has three configurations. The standard configuration differs slightly from the Modified and Special configuration in pin designation. The Unibus signals are delineated in Table 3-1.

TABLE 3-1 Bus Signals Viewed From The Connector End

PIN NUMBER	STANDARD	MODIFIED	SPECIAL
AA1	INIT L	INIT L	INIT L
AB1	INTR L*	INTR L*	INTR L*
AC1	DOO L	DOO L	DOO L
AD1	DO2 L	DO2 L	DO2 L
AE1	DO4 L	DO4 L	DO4 L
AF1	DO6 L	DO6 L	DO6 L
AH1	DO8 L	DO8 L	DO8 L
AJ1	D10 L	D10 L	D10 L
AK1	D12 L	D12 L	D12 L
AL1	D14 L	D14 L	D14 L
AM1	PA L*	PA L*	PA L*
AN1	GND*	PAR P1*	A21 L
AP1	GND*	PAR P0	A20 L
AR1	GND*	+15 BATT*	+15 BATT*
AS1	GND*	-15 BATT*	-15 BATT*
AT1	GND*	GND	GND
AU1	NPG H*	+20V (CORE)*	+20V (CORE)*
AV1	BG7 S0*	+20V (CORE)*	+20V (CORE)*
AA2	+5V	+5V	+5V
AB2	GND*	TP*	TP*
AC2	GND	GND	GND
AD2	D01 L	D01 L	D01 L
AE2	D03 L	D03 L	D03 L
AF2	D05 L	D05 L	D05 L
AH2	D07 L	D07 L	D07 L
AJ2	D09 L	D09 L	D09 L
AK2	D11 L	D11 L	D11 L
AL2	D13 L	D13 L	D13 L
AM2	D15 L	D15 L	D15 L
AN2	PB L	PB L	PB L
AP2	BBSY L*	BBSY L*	BBSY L*
AR2	SACK L*	SACK L*	SACK L*
AS2	NPR L*	NPR L*	NPR L*
AT2	BR7 L*	BR7 L*	BR7 L*
AU2	BR6 L*	BR6 L*	BR6 L*
AV2	GND	+20V (CORE)*	+20V (CORE)*

*Pins assigned in Unibus connector but not used by memory.

TABLE 3-1 Bus Signals Viewed From The Connector End (Cont'd)

PIN NUMBER	STANDARD	MODIFIED	SPECIAL
BA1	BG6 H*	RESV*	RESV*
BB1	BG5 H*	RESV*	RESV*
BC1	BR5 L*	BR5 L*	BR5 L*
BD1	GND*	+5 BATT	+5 Batt
BE1	GND*	SSYN INT L*	A19 L
BF1	ACLO L*	ACLO L*	ACLO L*
BH1	A01 L	A01 L	A01 L
BJ1	A03 L	A03 L	A03 L
BK1	A05 L	A05 L	A05 L
BL1	A07 L	A07 L	A07 L
BM1	A09 L	A09 L	A09 L
BN1	A11 L	A11 L	A11 L
BP1	A13 L	A13 L	A13 L
BR1	A15 L	A15 L	A15 L
BS1	A17 L	A17 L	A17 L
BT1	GND	GND	GND
BU1	SSYN L	SSYN L	SSYN L
BV1	MSYN L	MSYN L	MSYN L
BA2	+5V *	+5V *	+5V *
BB2	GND *	TP *	TP *
BC2	GND *	GND *	GND *
BD2	BR4 L*	BR4 L*	BR4 L*
BE2	BG4 L*	PAR DET L*	A18 L
BF2	DC LO L	DC LO L	DC LO L
BH2	A00 L	A00 L	A00 L
BJ2	A02 L	A02 L	A02 L
BK2	A04 L	A04 L	A04 L
BL2	A06 L	A06 L	A06 L
BM2	A08 L	A08 L	A08 L
BN2	A10 L	A10 L	A10 L
BP2	A12 L	A12 L	A12 L
BR2	A14 L	A14 L	A14 L
BS2	A16 L	A16 L	A16 L
BT2	C1 L	C1 L	C1 L
BU2	C0 L	C0 L	C0 L
BV2	GND *	-5V (CORE)*	-5V (CORE)*

*Pins assigned in Unibus connector but not used by memory.

3.2.2 SIGNALS

There are three types of signals; input, output and bi-directional. These signals are received, processed and passed back to the CPU in two logic levels. A high, or logic level one, and a low, or logic level zero. Specifications for these logic levels are as follows:

TYPE OF SIGNAL	LEVEL ONE	LEVEL ZERO
Bus Logic Levels	+0.8V or Less	+2.0V or More
Input Signal Logic Levels	1.3V Maximum 30 microamps typical at 0.8V	1.7V Minimum 80 microamps maximum at 2.5V
Output Signal Logic Levels	0.8V maximum at 70milliamps	2.4V mimimum 25 microamps maximum at 3.5V

Memory System Interface Timing is given in figure 3-1. All timing is measured at the card edge connectors and is referenced to the +1.5V level of signal transition.

3.2.3 Types of Signals

There are three types of signals. Input signals, output signals and Bi-directional signals.

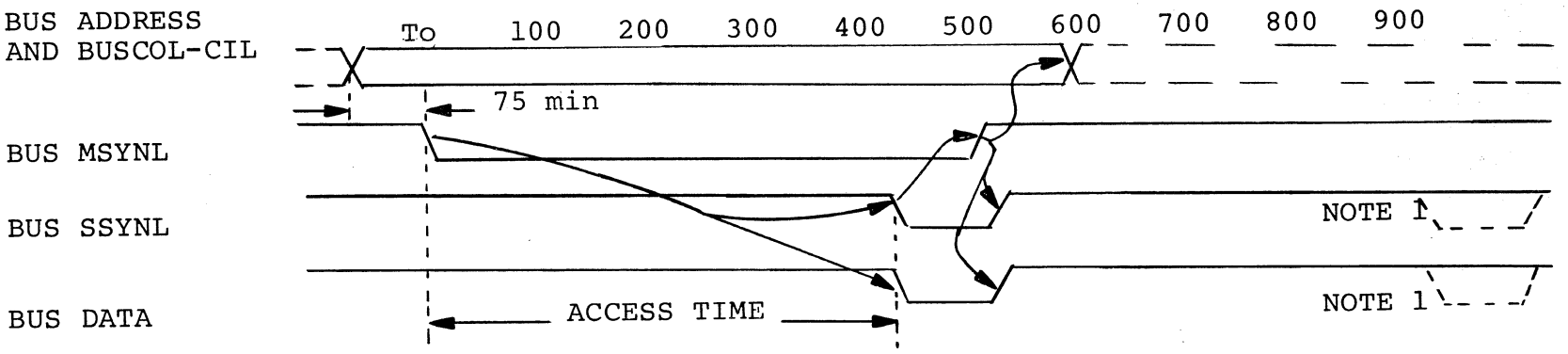
Input Signals

These signals are address and command signals. A00 through A21 are address lines which determine memory location. A0 determines which byte is written when Byte Write (DATOB) is executed (BH1 - BS1, BH2 - BS2). When addresses A18 - A21 are used the following pin assignments are used (Special Bus Operation). A18 - BE2

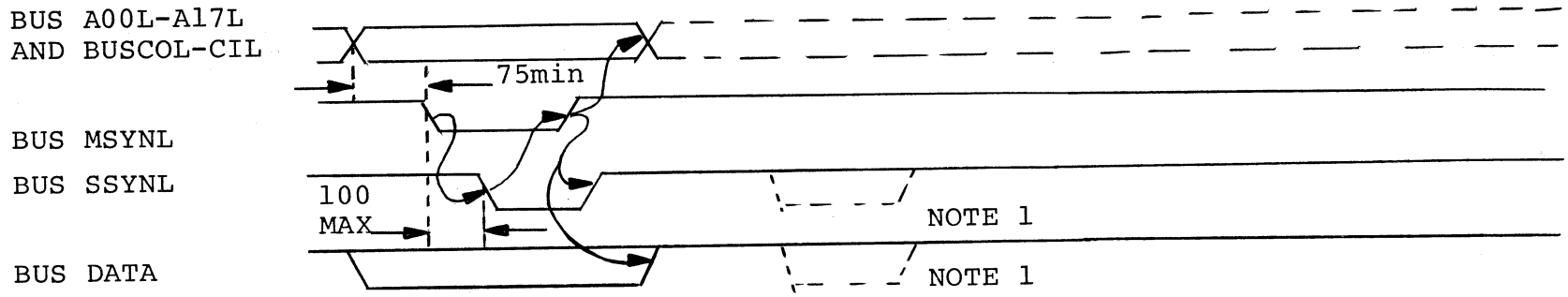
A19 - BE1

A20 - AP1

A21 - AN1



DATI AND DATIP



DATO

NOTE 1 DATA and SSYNL may be delayed up to 500ns due to simultaneous Refresh and Memory Request.

FIGURE 3-1

C0 and C1 are the signals which determine cycle and if the memory will be processing data in Byte Write mode or in Full Write mode. C1 selects Read or Write Cycle. C0 selects Byte Write or Full Write.

Master Sync, MSYN, is the Bus control signal which initiates memory cycle when memory is available (BVI).

Initialize, INIT, is used as a clear signal before MSYN occurs. It clears the Control Status Registers (CSR's) for bits 0, 2, 14, and 15 (AA1).

DC LO, when asserted, causes the memory to perform Refresh only. It also causes data to be retained should the battery back-up voltage be activated (BF2).

Output Signals

SSYN is the Slave Sync signal. It tells the host system that memory is on line and data is ready for the Read Cycle. During the Write cycle it indicates that address/data has been accepted by memory for processing (BU1).

PB is the signal which indicates that a parity error has been detected.

Bi-directional Signals

D0 through D15 data lines are bi-directional. These 16 lines are used to communicate data information with the Unibus I/0 (AC1 through AK1 and AD2 through AM2).

3.3 ADDRESS (FIGURE 3-2)

The NS11E Memory accepts a full 22 bit address with the least significant bit being used to control Byte Write. The address lines to the memory are single rail and the addressing mode is random. Address signals are identified as A0 through A21 (See Figure 3-2.

A0 is used in the Byte Write mode as the byte selection control bit. A1 through A21 can be decoded across a range of addresses from zero through 2,097,152 locations in memory. The extention of memory addressing through 2 Mega Words is achieved by the setting of Switch S1-9, that enables the buffer for bits A18 through A21 and allows them to be included in the address certification process.

Four Buffer chips receive the address from the bus. The address is stable on the Bus for 75 nSec prior to receipt of MSYNC, the Master Sync pulse. During this time it is processed through the address selection circuitry (see Figure 3-2). The address buffers receive and pass all inputs from the bus to the Address Latch which is transparent until the Selection process is completed.

A0 through A17 are passed through the Address Latch chips. A1 through A14 go directly to the RAS/CAS Address Multiplexer where they select the Row and Column RAM address. This is discussed in greater detail later in this section.

A13 through A21, (seen on the schematic as BA13 through BA21,) are presented at the Starting Address Select circuitry and compared with the initial address entered in the nine switch positions located on Switch S3. These nine switch positions represent the minimum bus address to which the card can respond.

When the Starting Address Selection process is complete one of two conditions have been recognized:

- The address is either less than the minimum number set in Switch 3, 1 through 9.

- Or it is equal to, or greater than, the minimum switch settings.

If the address is less than the switch settings it is rejected and no further action is taken. If, however, the address is found to be equal to or greater than the minimum switch setting the Starting Address Select function outputs a Normalized address. This address is the difference between the bus address and the address set in Switch 3, 1 through 9. When the number arrived at is less than the maximum switch selectable upper limit for this card (from 8 to 64K) the +addr Sel signal is generated. The +Addr Sel signal, when enabled by MSYNC, latches the address in the Address Latch beginning the memory cycle.

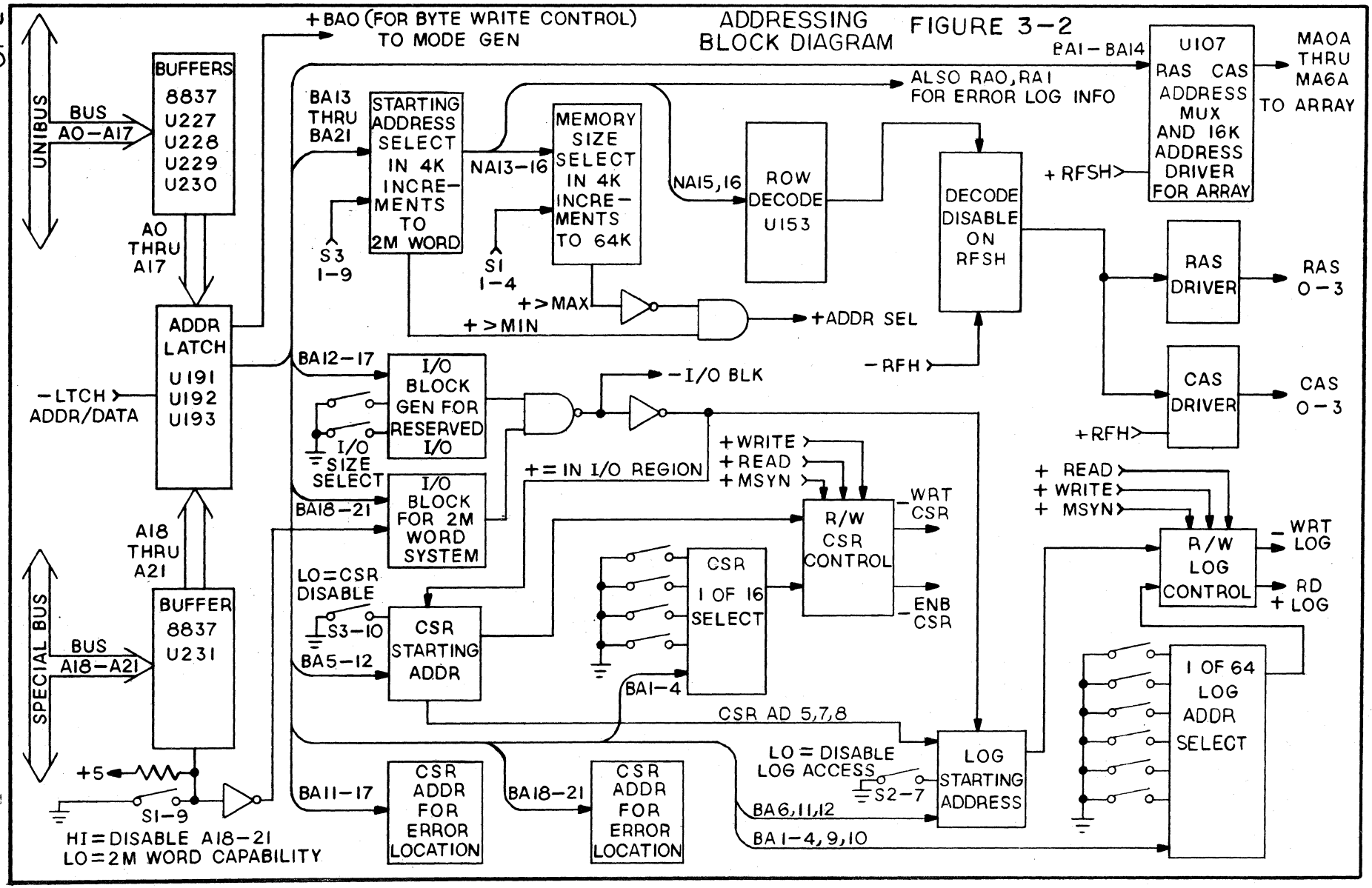
When the two criteria cited above are met, address bits NA15 and NA16 are presented to the Row Decode circuitry which selects a row of RAM on the card.

Signals BA1 through BA14 briefly mentioned above, select row and column position in each memory chip affected. They are multiplexed by the Address Multiplexer chip which transmits row address then column address during a normal cycle. During the Refresh Cycle the chip also provides refresh address.

The I/O Block is an area in Memory that is usually 4K words in size. It is normally located in the top 4K of Memory, i.e., from 124K words to 128K words, using a Unibus interface. It is located at the top of 2M words when interfacing with the Special Bus (from 1.996M to 2M). In the I/O address space, the Memory does not respond to Bus MSYN L unless the on-board CSR or Error Log have been addressed. The I/O Block has a Size Select Switch which permits selection of 2K, 4K, or 8K words of I/O space. This switch is set as a part of the installation procedure. (Section II)

CSR Address Selection is accomplished in the I/O region. The CSR, seen by the CPU as an I/O peripheral, has assigned addresses which can be accessed (one of sixteen) by a Bus Master via the Unibus or Special Bus. This address will contain diagnostic and error information (error address to the nearest 1K) if an error has occured. CSR operation can be disabled via S3-10.

The CSR starting address receives an enable from the I/O region (high) and BA1-12 . S3-10 enables the starting address circuitry. The output of the CSR starting address is fed to the Read/Write CSR Control which receives the CSR (1 of 16) select input. These inputs combined with +MSYN, +READ or +WRITE produce -WRT CSR or -ENB CSR.
CSR starting address also provides A05, A07, and A08 to the log Starting Address. The log also receives a high from the I/O Region, BA6, BA11, and BA12. S2-7 is set high enabling log access. There are four 16K increments of error log addresses. The Log Starting Address circuitry output, combined with the Log Select Signal are input to the R/W Log Control which produces -WRT LOG or +RD LOG. Log access can be disabled by closing S2-7.


ADDRESSING BLOCK DIAGRAM
FIGURE 3-2
UNIBUS
BUS A0-A17
BUFFERS 8837 U227 U228 U229 U230
A0 THRU A17
ADDR LATCH U191 U192 U193
-LTCH ADDR/DATA
+BA0 (FOR BYTE WRITE CONTROL) TO MODE GEN
BA13 THRU BA21
STARTING ADDRESS SELECT IN 4K INCREMENTS TO 2M WORD
S3 1-9
NA13-16
MEMORY SIZE SELECT IN 4K INCREMENTS TO 64K
S1 1-4
+>MAX
+>MIN
+ADDR SEL
NA15,16
ROW DECODE U153
ALSO RA0,RA1 FOR ERROR LOG INFO
BA1-BA14
U107 RAS CAS ADDRESS MUX AND 16K ADDRESS DRIVER FOR ARRAY
+RFSH
MA0A THRU MA6A TO ARRAY
DECODE DISABLE ON RFSH
-RFH
RAS DRIVER
RAS 0-3
CAS DRIVER
CAS 0-3
+RFH
BA12-17
I/O BLOCK GEN FOR RESERVED I/O
-I/O BLK
I/O SIZE SELECT
+=IN I/O REGION
+WRITE
+READ
+MSYN
BA18-21
I/O BLOCK FOR 2M WORD SYSTEM
A18 THRU A21
SPECIAL BUS
BUS A18-A21
BUFFER 8837 U231
LO=CSR DISABLE
S3-10
CSR STARTING ADDR
BA5-12
CSR 1 OF 16 SELECT
BA1-4
R/W CSR CONTROL
-WRT CSR
-ENB CSR
+READ
+WRITE
+MSYN
R/W LOG CONTROL
-WRT LOG
RD +LOG
1 OF 64 LOG ADDR SELECT
CSR AD 5,7,8
LO=DISABLE LOG ACCESS
S2-7
LOG STARTING ADDRESS
BA6,11,12
BA1-4,9,10
+5
S1-9
HI=DISABLE A18-21
LO=2M WORD CAPABILITY
BA11-17
CSR ADDR FOR ERROR LOCATION
BA18-21
CSR ADDR FOR ERROR LOCATION

3.4 TIMING AND CONTROL (FIGURE 3-3)

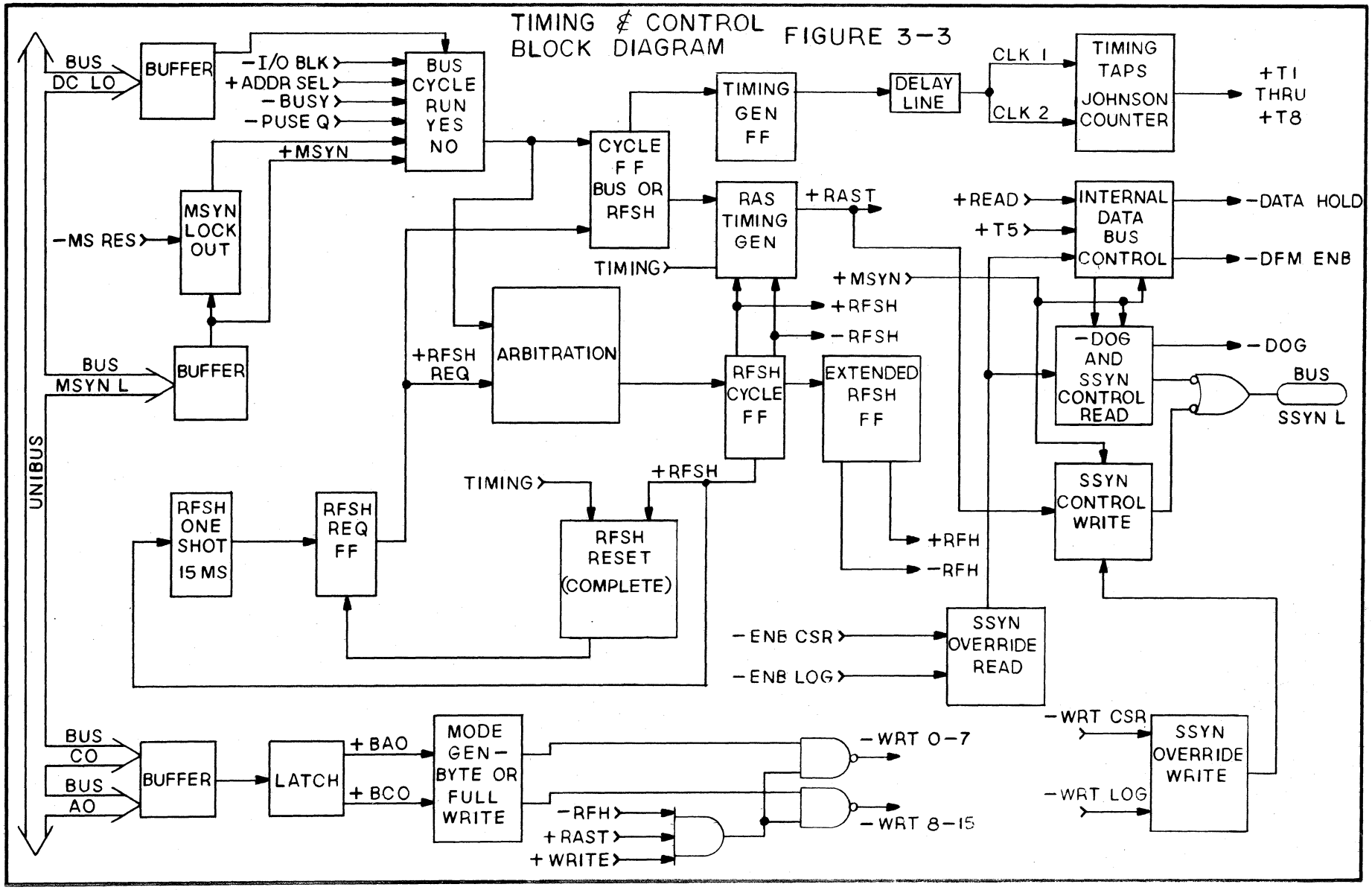
The Timing and Control circuitry determines if a Bus Cycle is to be executed or not. It tests the condition of the memory to find out if it is busy performing a read or write cycle, or if a refresh cycle is taking place. A Bus Cycle can be delayed as much as 500 nSec if it arrives after a refresh cycle has begun. A unique arbitration technique for testing the condition of the memory is employed each time a bus cycle is initiated.

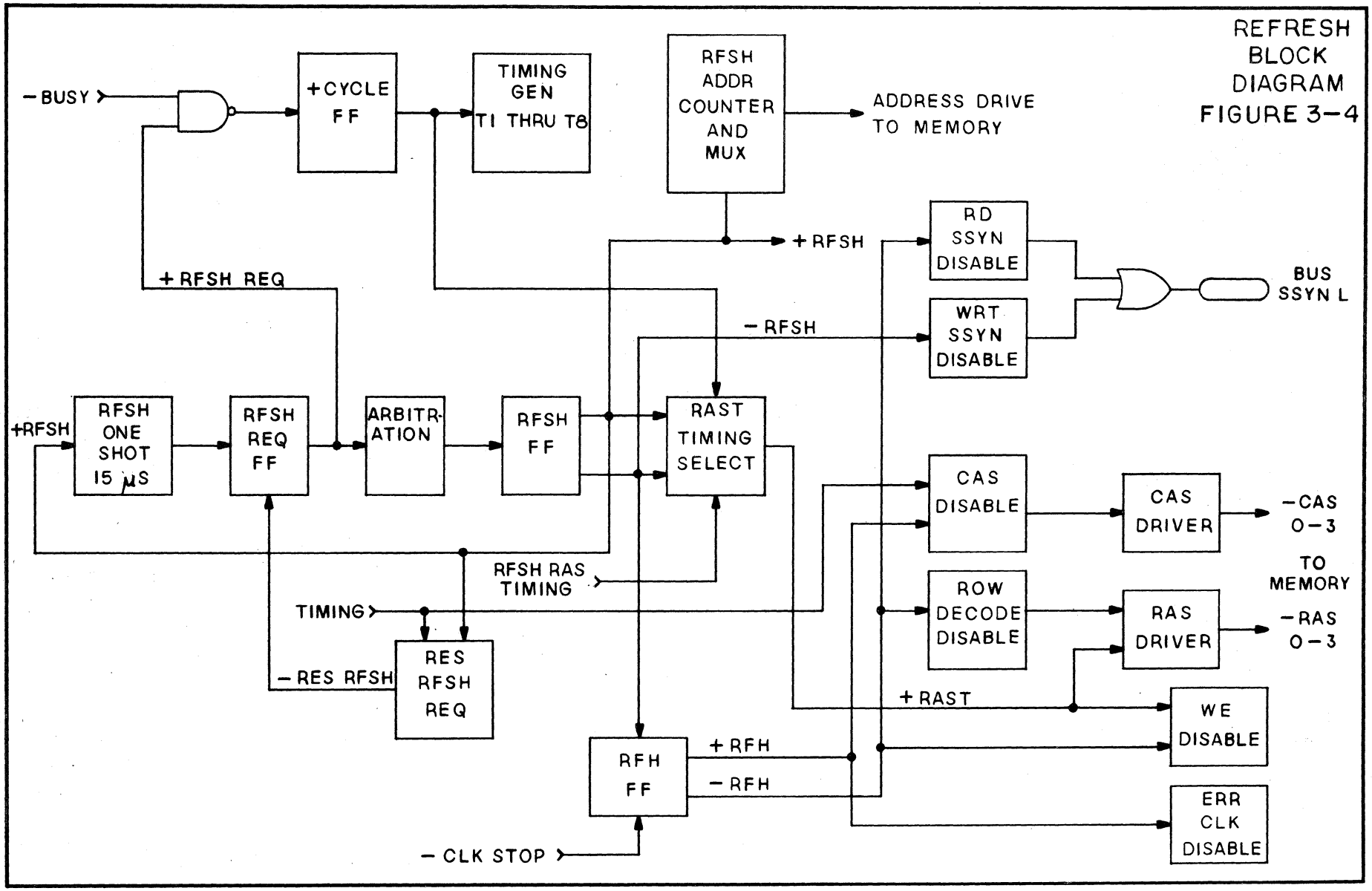
There are eight fixed timing sequences generated by the Johnson Counter that are used to control the memory system timing. The Timing Generator Flip-flop controls the Johnson counter.

The Cycle Flip-flop is set when the following conditions are true; there is no activity in the I/O Block, -Busy is not asserted, powerUp Sequence is not asserted, +Address Select is present, the MSYN Lock Out Flip-flop is set and MSYN is present.

With the above conditions true, a +Cycle Start pulse is presented to the Cycle Flip-flop and the Arbitration circuit simultaneously. If a Refresh Cycle is not in progress, or if the request for a Refresh Cycle arrives at the same time as the +Cycle Start (the request for a Normal Cycle) the memory will run a normal cycle. This causes the system to place any Refresh request in a hold status pending completion of the Normal Cycle. +Cycle start initiates normal cycle timing and inhibits the Refresh Reset, insuring that any existing request for Refresh will not be lost.

The Refresh One Shot is set by the output of the Refresh Reset Flip-flop, which also resets the Refresh Request Flip-flop. A refresh cycle is run one every 15 uSec when a normal cycle is not in progress. When Refresh Request is accepted by the Arbitration circuitry the Refresh Cycle Flip-flop is set and a Refresh Cycle begins.


TIMING & CONTROL BLOCK DIAGRAM
FIGURE 3-3
UNIBUS
BUS DC LO
BUFFER
-I/O BLK
+ADDR SEL
-BUSY
-PUSE Q
BUS CYCLE RUN YES NO
+MSYN
MSYN LOCK OUT
-MS RES
BUS MSYN L
BUFFER
CYCLE F F BUS OR RFSH
TIMING GEN FF
DELAY LINE
CLK 1
CLK 2
TIMING TAPS JOHNSON COUNTER
+T1 THRU +T8
RAS TIMING GEN
+RAST
TIMING
+RFSH REQ
ARBITRATION
+RFSH
-RFSH
RFSH CYCLE FF
EXTENDED RFSH FF
+READ
+T5
INTERNAL DATA BUS CONTROL
-DATA HOLD
-DFM ENB
+MSYN
-DOG AND SSYN CONTROL READ
-DOG
BUS SSYN L
SSYN CONTROL WRITE
TIMING
+RFSH
RFSH ONE SHOT 15 MS
RFSH REQ FF
RFSH RESET (COMPLETE)
+RFH
-RFH
-ENB CSR
-ENB LOG
SSYN OVERRIDE READ
BUS CO
BUS AO
BUFFER
LATCH
+BAO
+BCO
MODE GEN- BYTE OR FULL WRITE
-RFH
+RAST
+WRITE
-WRT 0-7
-WRT 8-15
-WRT CSR
-WRT LOG
SSYN OVERRIDE WRITE


REFRESH BLOCK DIAGRAM FIGURE 3-4
-BUSY
+CYCLE FF
TIMING GEN T1 THRU T8
RFSH ADDR COUNTER AND MUX
ADDRESS DRIVE TO MEMORY
+RFSH
+RFSH REQ
-RFSH
RD SSYN DISABLE
WRT SSYN DISABLE
BUS SSYN L
+RFSH
RFSH ONE SHOT 15 µS
RFSH REQ FF
ARBITR-ATION
RFSH FF
RAST TIMING SELECT
CAS DISABLE
CAS DRIVER
-CAS 0-3
TO MEMORY
RFSH RAS TIMING
TIMING
ROW DECODE DISABLE
RAS DRIVER
-RAS 0-3
-RES RFSH
RES RFSH REQ
+RAST
WE DISABLE
+RFH
RFH FF
-RFH
ERR CLK DISABLE
-CLK STOP

Refresh Cycle does not interfere with CSR or error log accesses.

3.5 REFRESH (FIGURE 3-4)

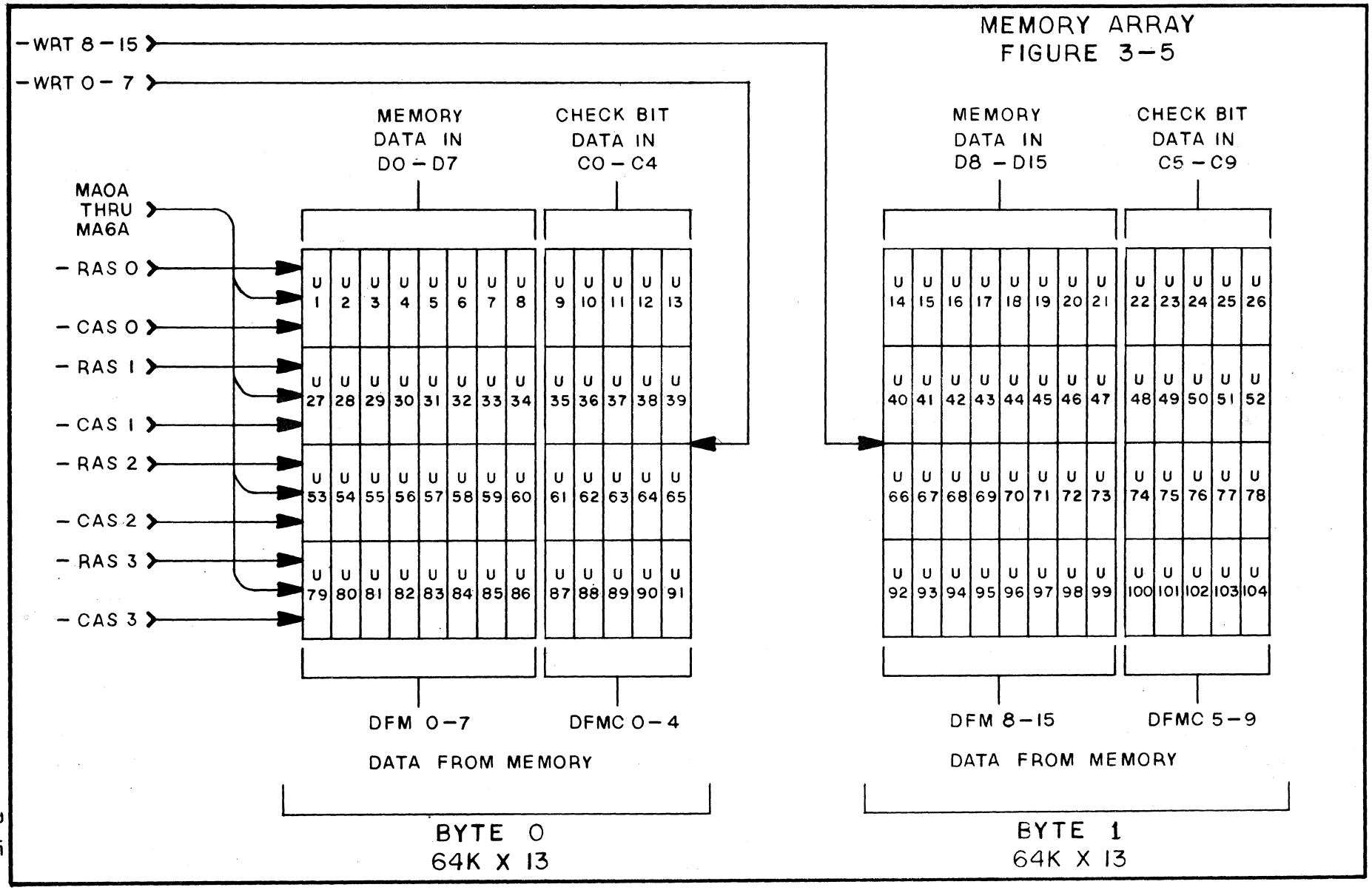
Refresh of the dynamic RAM's takes place every 15 uSec and lasts 450 nSec cycle. RAM is refreshed to prevent loss of existing DATA. Refresh is accomplished by the selection of a particular Refresh RAS Address, and inhibiting Row Decode so that all rows of RAM are selected. A counter in the Refresh Address Counter and Multiplexer increments once each time a Refresh Cycle is completed. This counter sets up the RAS address selection process for the next Refresh Cycle, thereby stepping the refresh activity completely through the memory every 2 milleconds. When the following conditions exist, Refresh Cycle can start:

- o Refresh Request is present.
- o -Busy is not asserted.
- o +Cycle Flip-flop is reset.
- o +Cycle Start is not asserted.

When +Cycle Start is not asserted at the arbitration circuitry and Refresh Request is present, the Refresh Flip-flop is set. When in the set condition, the Refresh Flip-flop enables the Refresh address onto the Memory Address lines and selects refresh RAST timing. At the conclusion of the Refresh cycle the Refresh Flip-flop updates the Refresh Address Counter, fires the one shot and resets the Refresh Request Flip-flop.

3.6 MEMORY ARRAY (FIGURE3-5)

The Memory Array is comprised of 104 16K Dynamic Rams in a 4x26 matrix. Each Byte contains 64kx13 bits of memory, eight data bits and 5 check bits. Addresses MA0A thru MA6A are common to all Rams. RAS and CAS signals (1 of 4) are common to each row. Basic Array organization is shown in Figure 3-5.


MEMORY ARRAY
FIGURE 3-5
-WRT 8-15
-WRT 0-7
MEMORY DATA IN D0-D7
CHECK BIT DATA IN C0-C4
MEMORY DATA IN D8-D15
CHECK BIT DATA IN C5-C9
MA0A THRU MA6A
-RAS 0
-CAS 0
-RAS 1
-CAS 1
-RAS 2
-CAS 2
-RAS 3
-CAS 3
U 1 U 2 U 3 U 4 U 5 U 6 U 7 U 8 U 9 U 10 U 11 U 12 U 13
U 14 U 15 U 16 U 17 U 18 U 19 U 20 U 21 U 22 U 23 U 24 U 25 U 26
U 27 U 28 U 29 U 30 U 31 U 32 U 33 U 34 U 35 U 36 U 37 U 38 U 39
U 40 U 41 U 42 U 43 U 44 U 45 U 46 U 47 U 48 U 49 U 50 U 51 U 52
U 53 U 54 U 55 U 56 U 57 U 58 U 59 U 60 U 61 U 62 U 63 U 64 U 65
U 66 U 67 U 68 U 69 U 70 U 71 U 72 U 73 U 74 U 75 U 76 U 77 U 78
U 79 U 80 U 81 U 82 U 83 U 84 U 85 U 86 U 87 U 88 U 89 U 90 U 91
U 92 U 93 U 94 U 95 U 96 U 97 U 98 U 99 U 100 U 101 U 102 U 103 U 104
DFM 0-7
DFMC 0-4
DFM 8-15
DFMC 5-9
DATA FROM MEMORY
DATA FROM MEMORY
BYTE 0
64K X 13
BYTE 1
64K X 13

3.7 ECC (FIGURE 3-6)

The NS11E has Error Correction and Check (ECC) circuitry which allows single bit error correction and double bit error detection for each byte. Figure 3-6 shows the ECC data path block diagram. Each byte contains it's own ECC check bit generation and compare circuitry.

3.7.1 ECC Write Data Path

During a write (DATO or DATOB) cycle the data to memory passes from the bus, through the 8641 tranceivers and is latched internally by S373 octal latches. The Data-in latch outputs are tied to the "internal data bus", which is labled as DØ-D15 on the schematic. The data from the latches is fed to the check bit generation circuit and also the memory array. The check bit generation circuit is comprised of several exclusive OR/NOR gates (S135's) and will generate a unique check bit pattern, based on the Hamming Code, for any combination of input data. To provide single bit correction and double bit detection, N+2 check bits must be provided for every 2^N data bits. Since there are 8 data bits per byte, an additional 5 check bits per byte are required, thus providing a total of 13 data bits per byte. Table 3-2 illustrates how each check bit is generated. As an example, check bit Ø will also be a zero. The check bit generator output (CØ-C9), along with the data on the internal bus, is written into the appropriate byte(s) in the memory array.

3.7.2 ECC Read Data Path

During a Read (DATI or DATIP) cycle, the sixteen data bits DFM Ø-15 are buffered by two S241 octal buffers and put on the internal data bus. The data appears at both the correction merge circuitry (comprised of S135 XNOR's) and the check bit generator. Another set of check bits is generated and compared with the check bit data that had been stored (DFM CØ-C9) at the syndrome bit generation circuit. Any difference between a newly generated check bit and the check bit that had been stored in memory will generate an error bit called a syndrome bit. The presence of any syndrome bit (SØ-S9) during a read cycle constitutes an error and an error clock will be enabled. SØ-S4 are associated with byte Ø and S5-S9 are for byte 1. An odd number of syndrome bits for any byte indicates a correctable or single bit error, while an even number (excluding zero) will indicate an uncorrectable or multiple bit error in that byte. If a single bit error has occured in either (or both) bytes, the correction bit generator will decode the syndrome bit pattern and, through the correction merge circuitry, complement the bit in error. In the case of an uncorrectable error in either byte, the correction bit generator is disabled and the partiy error flag, BUS PBL, will be enabled onto the bus.

After passing through the correction merge circuitry, the corrected data (if a single bit error occured) is latched by the Data Out latches (S373's). The 3 state outputs from the DFM buffers are disabled and the outputs from the DO latches are enabled. The data then passes through the 8641 transceivers and on to the Bus.

3.7.3 Diagnostics

When parity diagnostics are run, bit 2 in the CSR is set to write wrong parity in the memory. Since the NS11E is not a parity memory, the CSR bit 2 output is used to complement check bits CØ-C3 and C5-C8, which are being written into memory. During the subsequent Read of that data, syndrome bits SØ-S3 and S5-S8 will be generated (an even number for each byte). The error circuitry will detect an uncorrectable error in each byte and the parity error flag will be enabled.

The dip socket at location U131, which houses the spare RAM, is also used as the input connection for factory ECC test diagnostics.

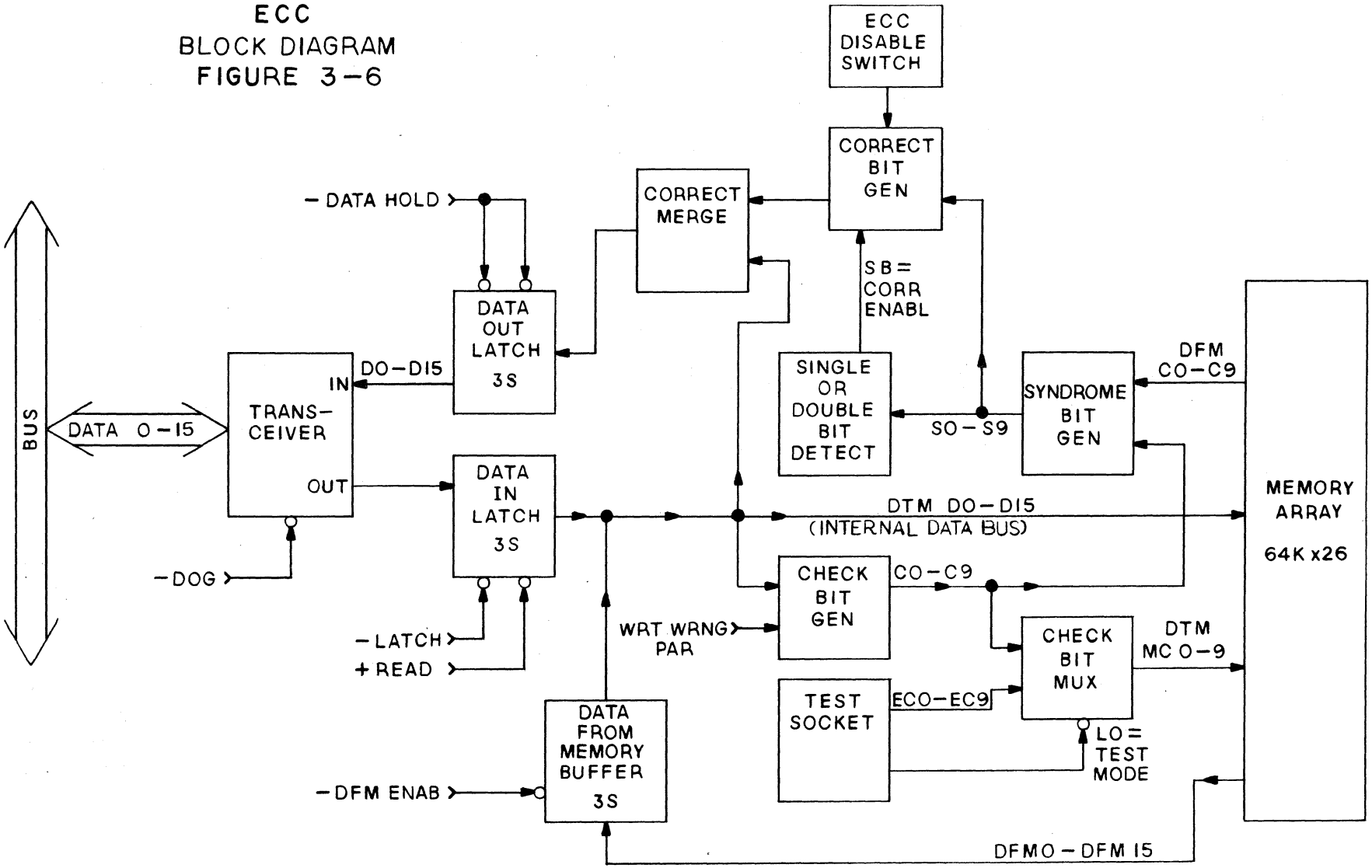
ECC can be disabled by turning switch 1-10 ON (CLOSED). For syndrome Bit to defective RAM location see section II.

CHECK BITS	DATA BITS															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C0	X	X		X		X	X									
C1	X		X		X	X		X								
C2		X	X				X	X								
C3				X	X	X	X	X								
C4	X	X	X	X	X											
C5									X	X		X		X	X	
C6									X		X		X	X		X
C7										X	X				X	X
C8												X	X	X	X	X
C9									X	X	X	X	X			

TABLE 3-2

CHECK BIT GENERATION CHART

ECC
BLOCK DIAGRAM
FIGURE 3-6



3.8 ERROR LOG (FIGURE 3-7)

The Error Logs main purpose is to store the error location, If a failure has occured. It is a sub-system of the main system in that it has it's own timing generator and control circuits. It is software addressable via the operators console or maintenance panel. The error log has three modes of operation:

1) Error Logging
2) Log Scan for Errors
3) Log Clear

3.8.1 Error Logging

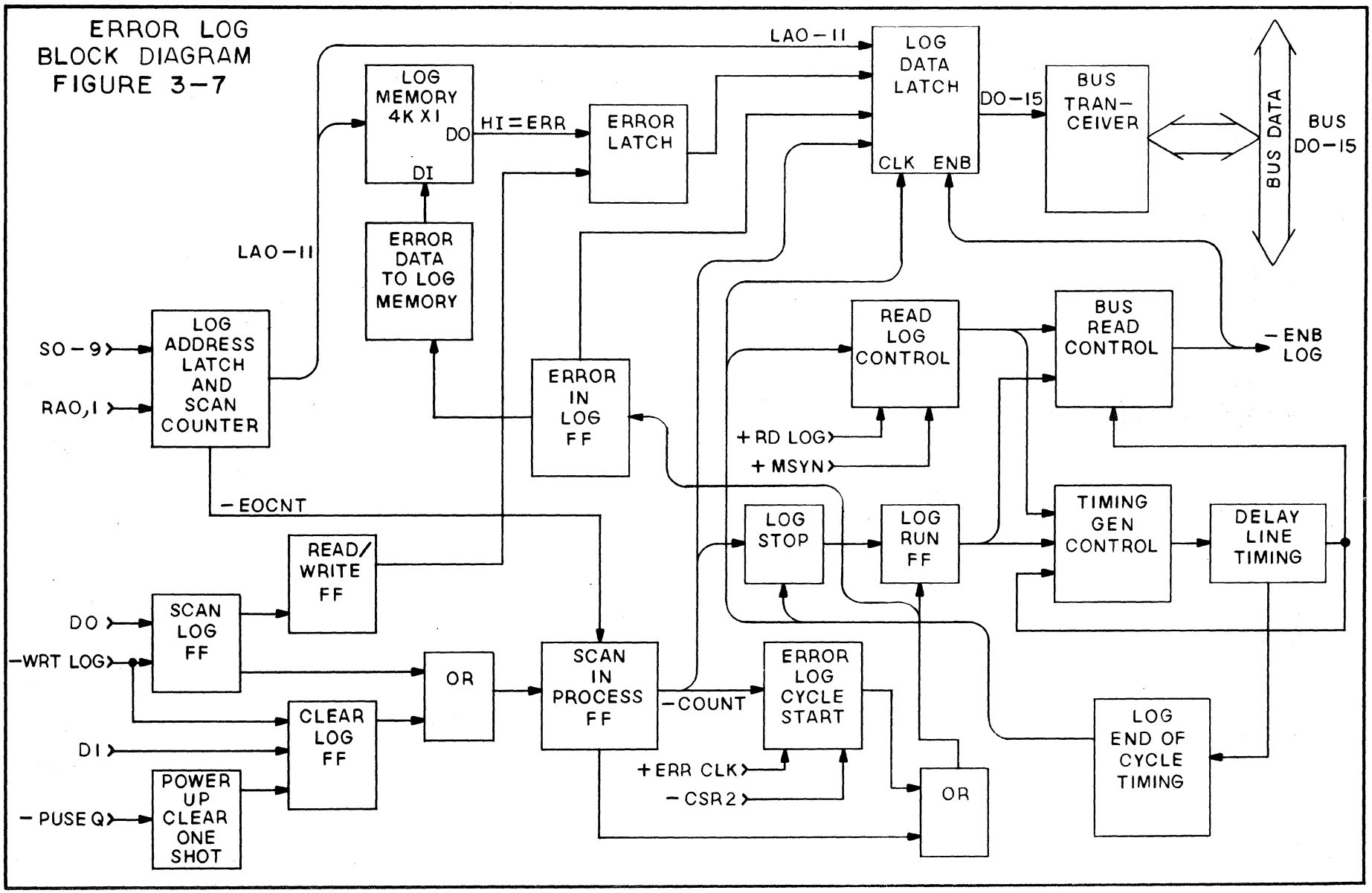
Memory System is in normal operation and error log is operational. On a read cycle if there has been an error detected in the ECC circuitry, the +ERR CLK signal is generated and sent to the error log. This signal serves as an intiate for the log. Syndrome data (SØ-9) and row address data (RA0 RA1) are latched and used as address for the 4Kx1 memory in the log. A "ONE" is written in Log Memory at this location.

3.8.2 Log Scan

When it is desired to find the bad Memory a Log Scan will be performed. The Log will be written via the Bus and Bit 0 will be set. The Log will scan until it finds a "ONE" In Memory. Scan then stops and that address of Log Memory provides the error location in main memory. To continue Log Scan Bit 0 must again be asserted. This process will be repeated until complete log has been searched.

3.8.3 Log Clear

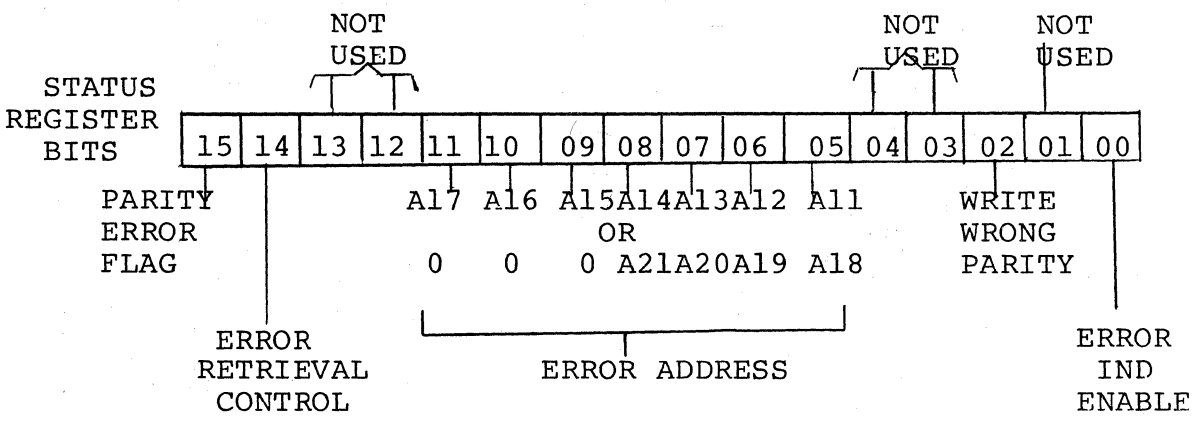
After all data has been read from the error log and a clear is required, Bit 1 is set and the log will be cleared to all 0's at all locations.


ERROR LOG
BLOCK DIAGRAM
FIGURE 3-7
LAO-11
LOG
DATA
LATCH
CLK ENB
DO-15
BUS
TRAN-
CEIVER
BUS DATA
BUS
DO-15
LOG
MEMORY
4K X1
DO
DI
HI=ERR
ERROR
LATCH
ERROR
DATA
TO LOG
MEMORY
LAO-11
SO-9
RAO,1
LOG
ADDRESS
LATCH
AND
SCAN
COUNTER
READ
LOG
CONTROL
BUS
READ
CONTROL
-ENB
LOG
ERROR
IN
LOG
FF
+RD LOG
+MSYN
-EOCNT
LOG
STOP
LOG
RUN
FF
TIMING
GEN
CONTROL
DELAY
LINE
TIMING
READ/
WRITE
FF
DO
-WRT LOG
SCAN
LOG
FF
OR
SCAN
IN
PROCESS
FF
-COUNT
ERROR
LOG
CYCLE
START
CLEAR
LOG
FF
DI
+ERR CLK
-CSR2
OR
LOG
END OF
CYCLE
TIMING
POWER
UP
CLEAR
ONE
SHOT
-PUSEQ

3.9 CSR (FIGURE 3-8)

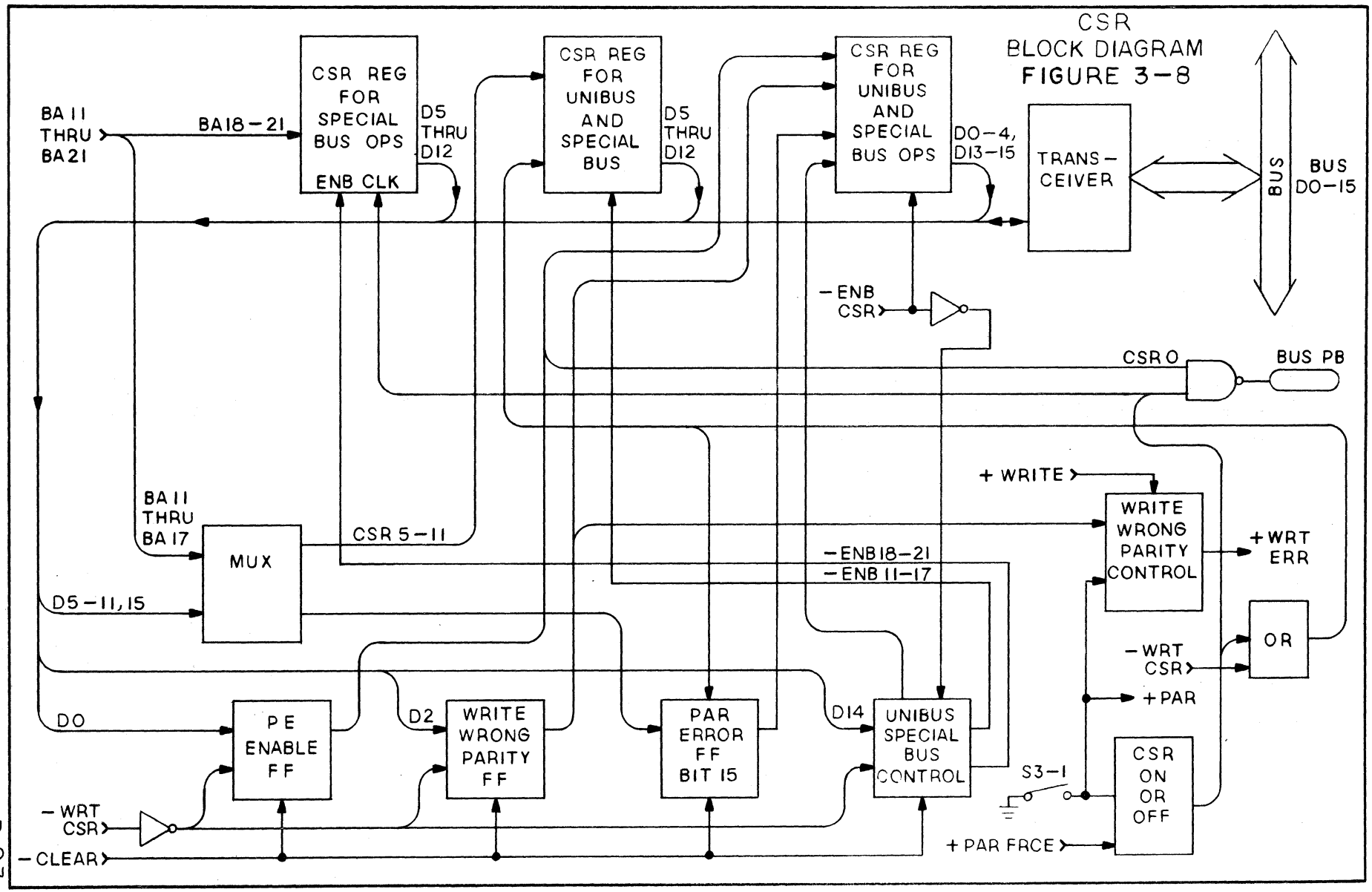
The Control and Status Register (CSR) in the NS11E allows program control of certain diagnostic information (error address to the nearest 1K) when an error occurs. The CSR is assigned an address and can be accessed by a bus master via the Unibus or the Special Bus. Each NS11E in a given backplane, must be assigned a different address. Some CSR Bits are cleared by the assertion of BUS INIT L as a part of the processor power-up sequence. The CSR Bit assignment and operational description is as follows:

The memory corrects single bit errors and detects multiple bit errors. The detection of an uncorrectable multiple bit error is used to generate the parity error flag BUS PB L and to latch the faulty address into CSR. The memory is compatible with all modified Unibus parity or non-parity memories.



Bits 1,3,4,12,13

These bits are not used and are always read as logical 0's. Writing these bits has no effect on the CSR.


CSR
BLOCK DIAGRAM
FIGURE 3-8
BA 11 THRU BA 21
BA18-21
CSR REG FOR SPECIAL BUS OPS
ENB CLK
D5 THRU D12
CSR REG FOR UNIBUS AND SPECIAL BUS
D5 THRU D12
CSR REG FOR UNIBUS AND SPECIAL BUS OPS
DO-4, D13-15
TRANS-CEIVER
BUS
BUS DO-15
-ENB CSR
CSR 0
BUS PB
+ WRITE
BA 11 THRU BA 17
MUX
CSR 5-11
-ENB18-21
-ENB 11-17
D5-11,15
WRITE WRONG PARITY CONTROL
+WRT ERR
OR
-WRT CSR
+PAR
DO
PE ENABLE FF
D2
WRITE WRONG PARITY FF
PAR ERROR FF BIT 15
D14
UNIBUS SPECIAL BUS CONTROL
S3-1
CSR ON OR OFF
-WRT CSR
-CLEAR
+PAR FRCE

DO-(Bit 0) is the Error Indication Enable Bit. When D0 is logical 1 it allows the memory to assert BUS PB L. This Bit is a Read/Write Bit and is cleared by BUS INIT L. D0 sets the PE Enable Flip-flop that enables (CSR 0) the Bus PB L Driver.

D2-(Bit 2) is the Write/Wrong Parity control. This Bit, when set, causes the NS11E to complement the ECC check Bits when Data is written during a Write cycle (DATO or DATOB). A multiple Bit error will then be detected when this Data is read during a Read (DATI or DATIP) cycle. The detection of the multiple Bit error causes the parity error flag to be asserted as if bad parity had been written. This Bit is set for diagnostic purposes and is cleared for normal operation. Bit 2 is a Read/Write Bit and is cleared by BUS INIT L.

D5-11 (Bits 5-11) are the Error Address Bits. Once a multiple Bit error has been detected, these bits contain a partial address of the faulty Data that caused the multiple Bit error. In Unibus operation address Bits A11-A17 are in CSR Bits 5-11 respectively, specifying the faulty Data location to a 1K segment of memory. In special Bus operation, the address placed in Bit 5-11 is determined by Bit 14. Bits 5-11 are Read/Write Bits and are not cleared by BUS INIT L.

D14-(Bit 14) is the Special Bus Error Retrieval Bit. This Bit, when set, causes the memory to place A18-A21 of the faulty Data location into CSR Bits 5-8; logical 0's are placed in Bits 9-11. Address Bits A11-A17 are placed in Bits 5-11 when Bit 14 is cleared. In Special Bus operation, Bit 14 is a Read/Write Bit and is cleared by BUS INIT L. In Unibus operation, Bit 14 is a Read only Bit and is always a logic 0 (clear).

NOTE: In normal Special Bus operation, Bit 14 is a logic 0. If a multiple Bit error has occurred, the partial address (A11-A21) of the faulty data is retrieved with the following sequence:

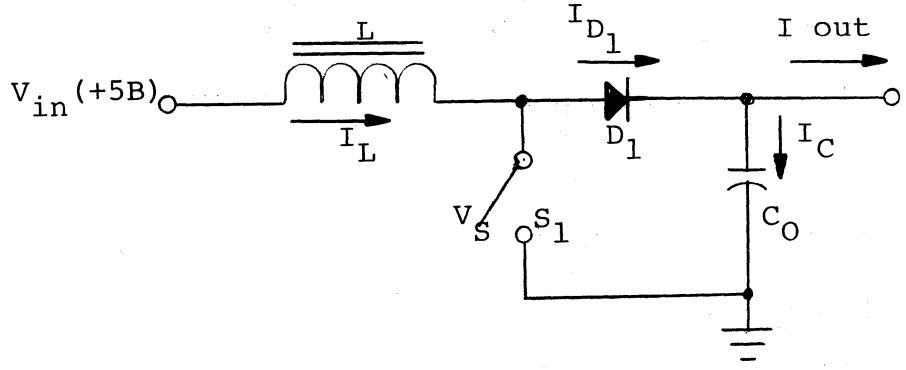
a) Read CSR to obtain A11-A17. Bit 14 should be read as a logical 0.
b) Write a logical 1 in Bit 14 of the CSR.
c) Read CSR to obtain A18-A21. Bit 14 should be read as a logical 1.

Bit 15 is the Parity Error Bit. When set it indicates that a parity error has occurred. Bit 15 is a Read/Write Bit and is cleared by BUS INIT L. A red LED is provided for CSR Bit 15 to indicate a parity error.

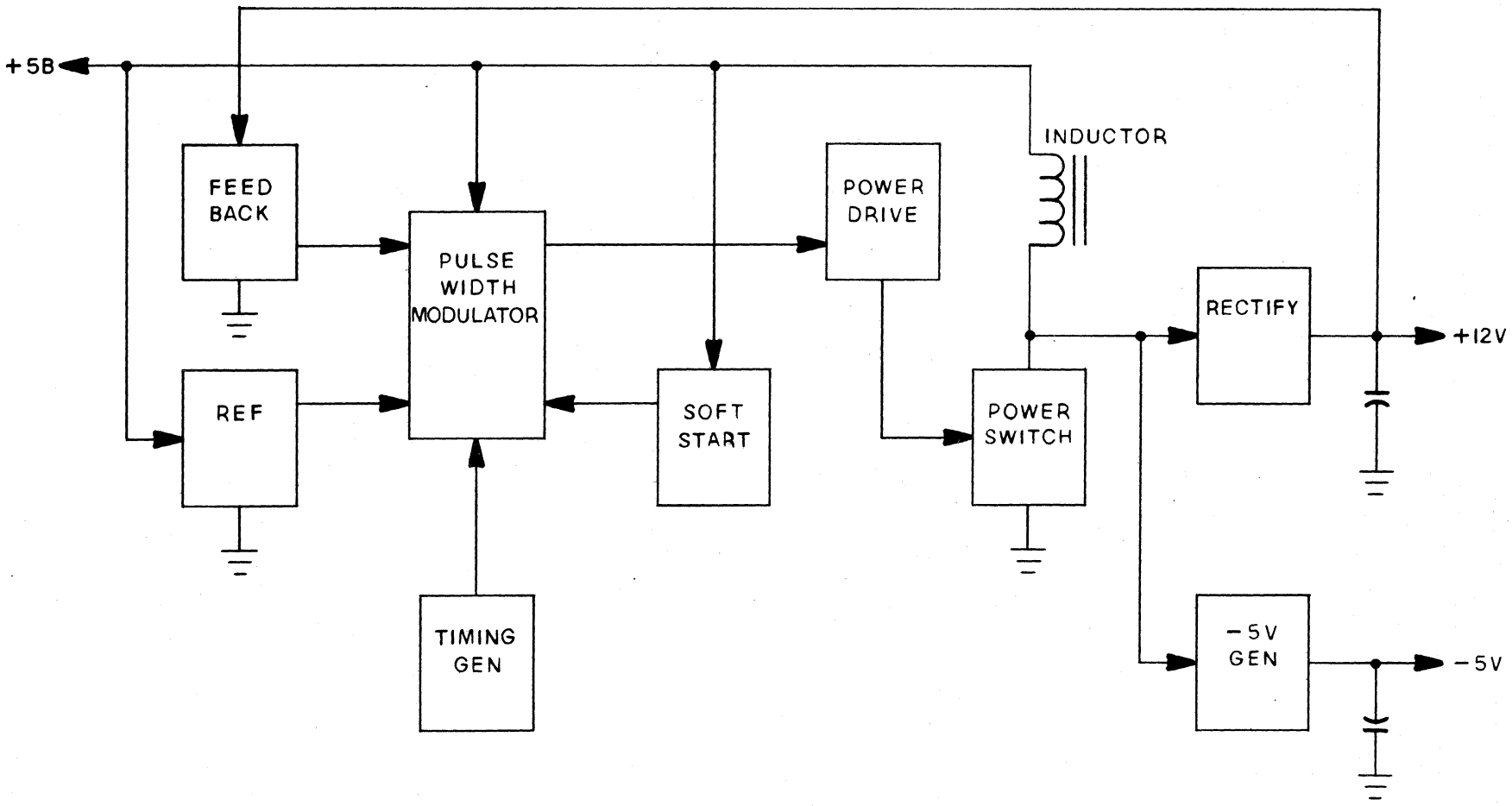
NOTE: The on-board CSR can be disabled by closing the (ON) Switch, 3-10.

3.10 DC TO DC CONVERTOR (FIGURE 3-9)

The NS11E employs a DC to DC convertor switching regulator that operates as flyback convertor in a step-up mode. The basic circuit is shown below:



DC TO DC CONVERTOR
BLOCK DIAGRAM
FIGURE 3-9

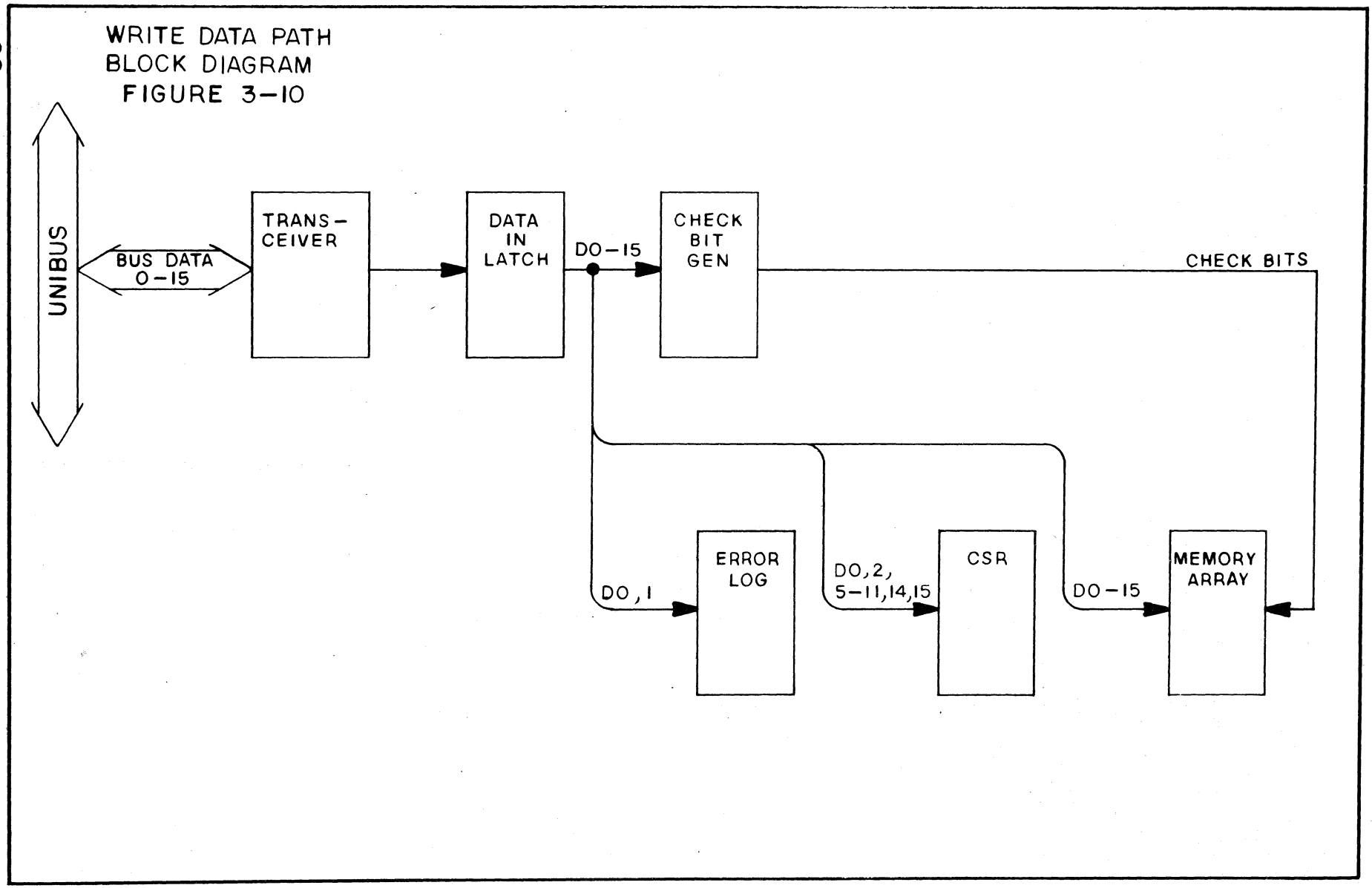


When the switch, S1, closes the applied voltage drops to almost zero (V_a=V_s), and the voltage Vin-Vs is applied accross the inductor, causing the inductor current to increase linearly. Because the applied voltage is less than the output voltage, the diode is reverse-biased and current cannot flow to the output. When the switch opens, the inductor current cannot change instantly and the applied voltage changes to the total of the output voltage plus the diode voltage. At this time current can flow through the diode to the load capacitance and the inductor current decreases at a linear rate, determined by Vout + V_D-Vin. Timing adjustments control the average diode current (I_{D1}) so it is equal to the load current. The diode current can only flow during off-time, so the maximum output current is (Ipk/2) ($T_{off}/T_{on}+T_{off}$). If the load current is less than the maximum output current, off-time is increased by a dead time with no current to the output. Input current can flow during both on and off times, so the average input current is always greater than the maximum output current.

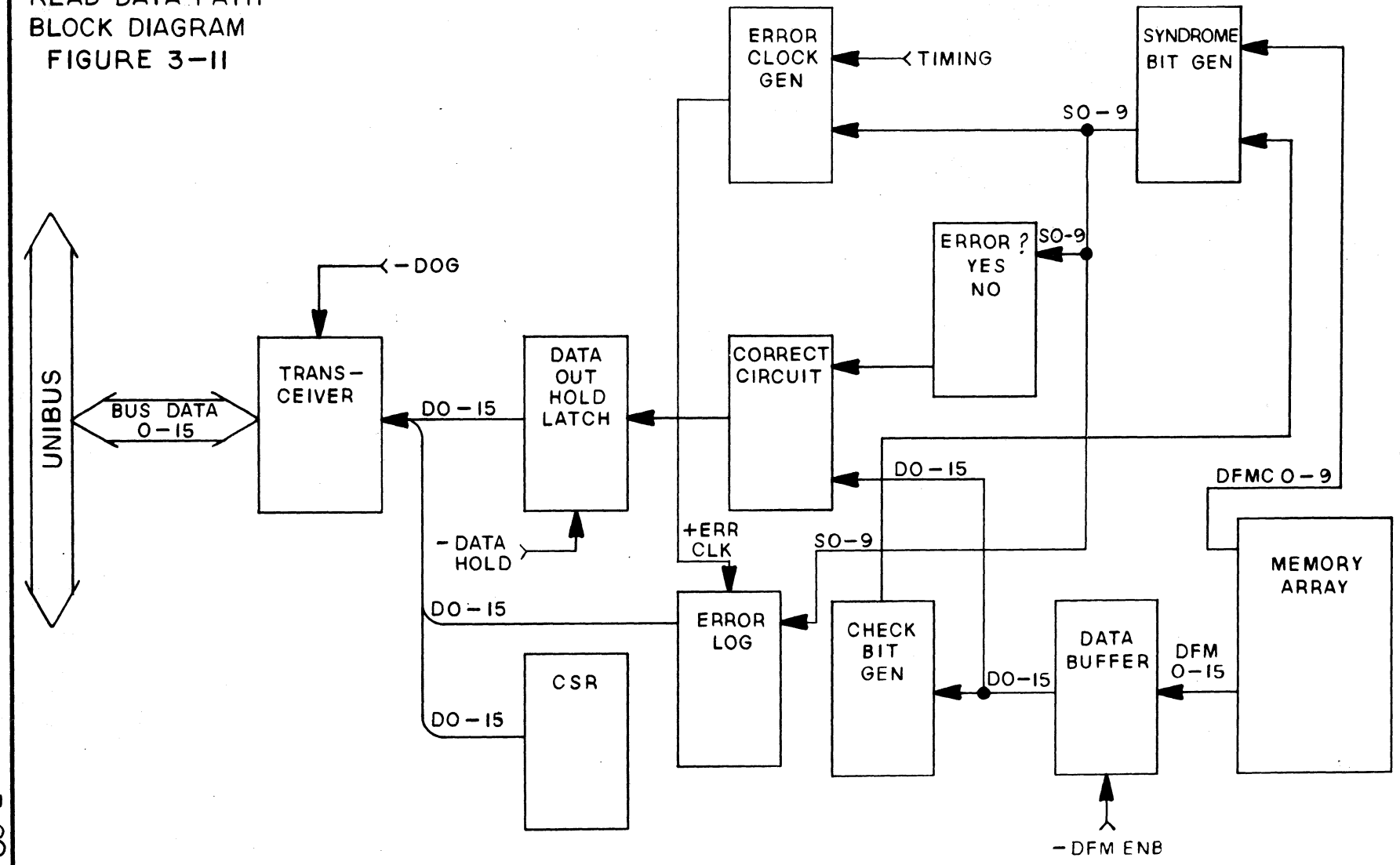
In the above figure the designations correspond to schematic reference designations as follows: L=L1, S_1=O2 thru 05, D1=CR5, CR6, Co=all capacitance on +12V line.

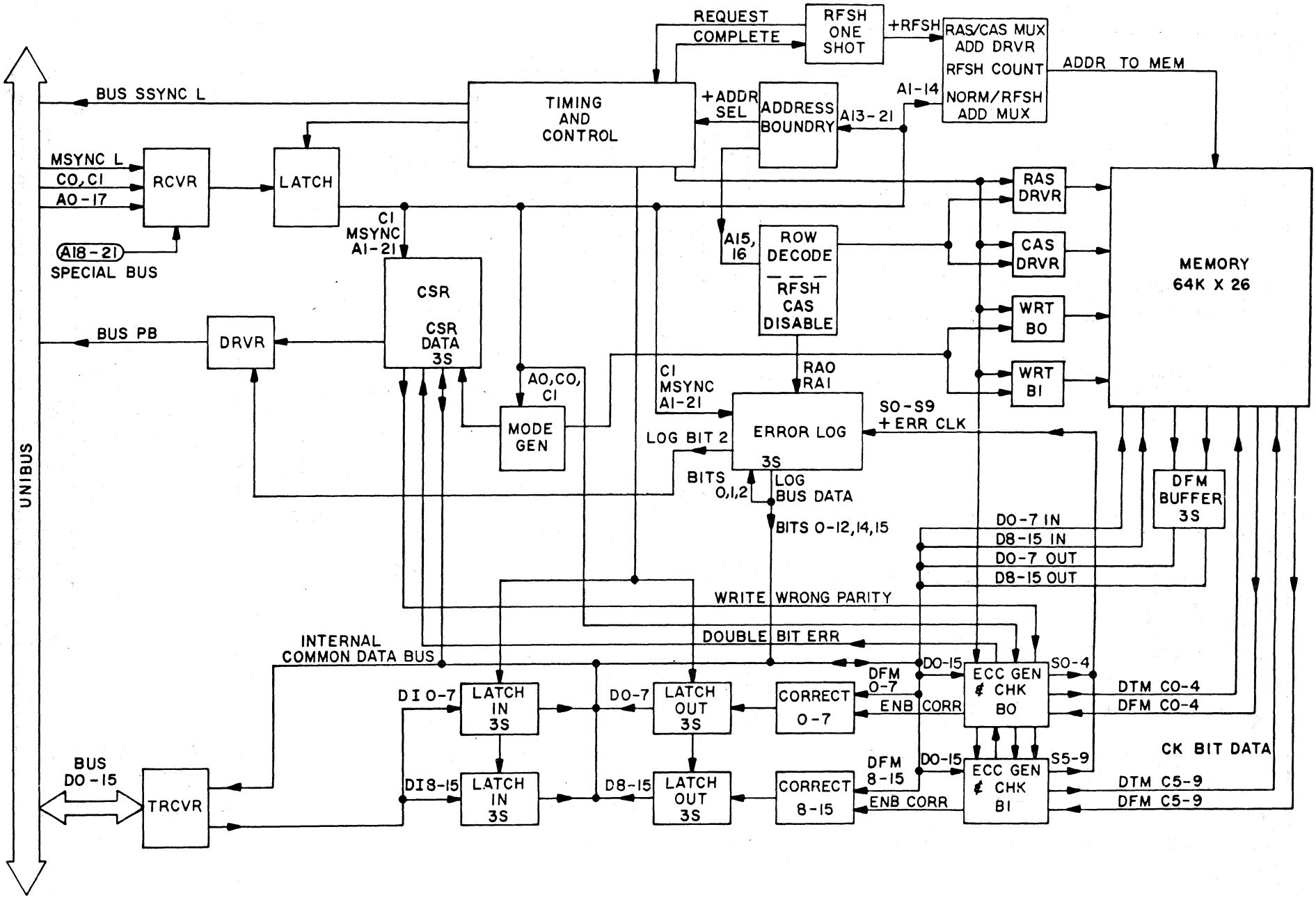
Main control for the convertor is handled by a pulse width modulator that controls on time, off time, dead time, voltage regulation and soft-start sequence.

WRITE DATA PATH
BLOCK DIAGRAM
FIGURE 3-10



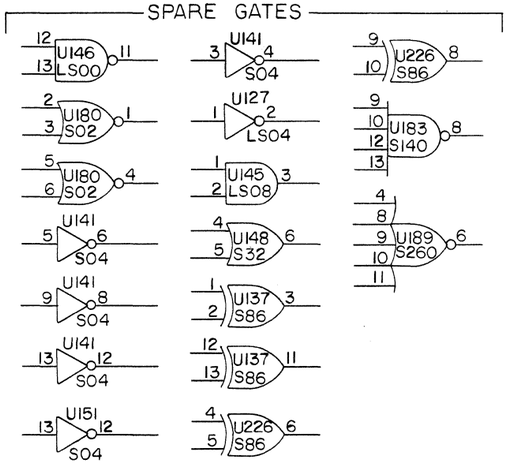
READ DATA PATH
BLOCK DIAGRAM
FIGURE 3-11



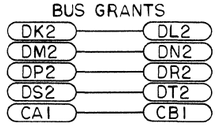

UNIBUS
BUS SSYNC L
MSYNC L
CO, CI
A0-17
RCVR
A18-21
SPECIAL BUS
LATCH
TIMING AND CONTROL
REQUEST COMPLETE
RFSH ONE SHOT
+RFSH
RAS/CAS MUX ADD DRVR
RFSH COUNT
NORM/RFSH ADD MUX
ADDR TO MEM
+ADDR SEL
ADDRESS BOUNDRY
A13-21
A1-14
CI MSYNC A1-21
CSR
CSR DATA 3S
BUS PB
DRVR
A15, 16
ROW DECODE
RFSH CAS DISABLE
RAS DRVR
CAS DRVR
WRT B0
WRT B1
MEMORY 64K X 26
A0, C0, C1
MODE GEN
CI MSYNC A1-21
RA0 RA1
ERROR LOG
3S
S0-S9 + ERR CLK
LOG BIT 2
BITS 0,1,2
LOG BUS DATA
BITS 0-12,14,15
DFM BUFFER 3S
D0-7 IN
D8-15 IN
D0-7 OUT
D8-15 OUT
WRITE WRONG PARITY
DOUBLE BIT ERR
INTERNAL COMMON DATA BUS
DI 0-7
LATCH IN 3S
DO-7
LATCH OUT 3S
CORRECT 0-7
DFM 0-7
ENB CORR
D0-15
ECC GEN & CHK B0
S0-4
DTM C0-4
DFM C0-4
BUS D0-15
TRCVR
DI8-15
LATCH IN 3S
D8-15
LATCH OUT 3S
CORRECT 8-15
DFM 8-15
ENB CORR
D0-15
ECC GEN & CHK B1
S5-9
CK BIT DATA
DTM C5-9
DFM C5-9

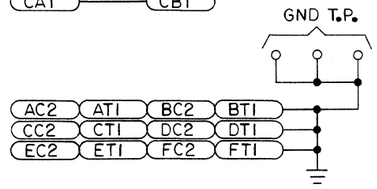
REVISIONS			
REV	DATE	ECO NO.	APPVD
B	7/16/79	PDD 3468	

SPARE GATES

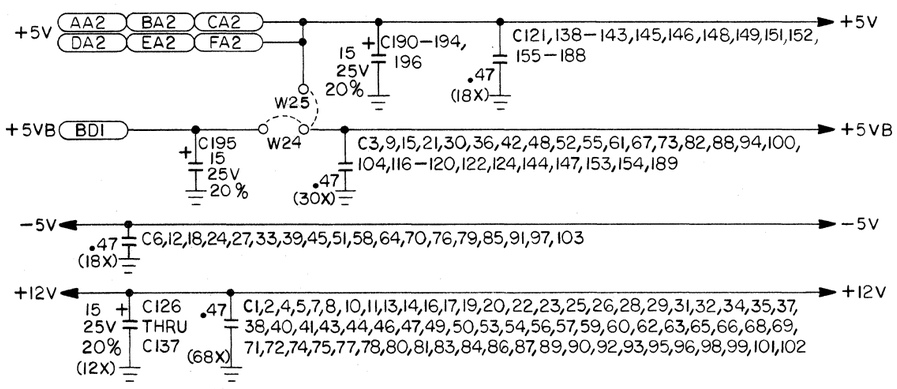


BUS GRANTS





REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C196	C150
CR9	
DS2	
F1	
L1	
Q6	
R54	R29 – R32
RP7	
S3	
U236	U140, 142, 144, 177, 200



VOLTAGE TABLE				
DEVICE TYPE	+5V	+5VB	GND	REFERENCE DESIGNATIONS
DELAY LINE 25NS		14	7	U116
DELAY LINE 100NS			8,14	U182
3524		16	8	U105
26S02		16	8	U130
3242		28	14	U107
4044		18	9	U143
8136	16		8	U156
8641	16		8	U232–235
8641		16	8	U236
8837	16		8	U227–231
74LS00		14	7	U110, 129
74LS00	14		7	U146, 159, 221, 225
74S00		14	7	U117, 123
74S00	14		7	U184
74S02		14	7	U128
74S02	14		7	U180
74LS04		14	7	U127
74LS04	14		7	U152, 181
74S04		14	7	U121
74S04	14		7	U141, 151, 186
74LS08		14	7	U118
74LS08	14		7	U145, 224
74S08		14	7	U126
74LS10		14	7	U149
74LS10	14		7	U222
74S10	14		7	U124
74S10		14	7	U163
74LS11		14	7	U112
74LS11	14		7	U223
74S20	14		7	U187
74S22		14	7	U164
74S30	14		7	U185, 188
74S32		14	7	U148
7437		14	7	U108
74S37		14	7	U109, 111
74LS74	14		7	U119, 216–219
74LS74		14	7	U120
74S74	14		7	U147, 160, 161, 220
74S74		14	7	U165
7485	16		8	U190
74S86	14		7	U135–139, 226
74S132		14	7	U122
74S133	16		8	U150
74S135	16		8	U170–174, 202–205
74S138	16		8	U153, 206–209
74S140	14		7	U183
74S157	16		8	U195
74LS157	16		8	U132–134, 154, 194
74S175		16	8	U113, 114
74LS193	16		8	U213–215
74S241		20	10	U115
74S241	20		10	U175, 176
74S260	14		7	U125, 189, 212
74S280	14		7	U210, 211
74S283	16		8	U155, 157, 158
74S373	20		10	U162, 166–169, 191–193, 197, 199
74S374	20		10	U178, 179, 196, 198
75452	8		4	U201

NOTES: UNLESS OTHERWISE SPECIFIED.

1. CAPACITANCE VALUES IN MICROFARADS, 50V, 10%.
2. RESISTANCE VALUES IN OHMS, 1/8W, 5%.
3. ALL DIODES ARE IN4531.
4. ALL TRANSISTORS ARE 2N3506.

NEXT ASSY	USED ON

MATERIAL

FINISH

TOLERANCE: ANG. —— 2 PL —— 3 PL ——

DR BY	JCJ	02-27-79
CHK		3-5-79
MFG		
EE		7/16/79
PE		7/16/79

UNLESS OTHER SPECIFIED

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.

REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SCHEMATIC DIAGRAM
NS-IIE
128K BYTE MEMORY

SIZE D | DR. NO. 870103839 | 001

SCALE NONE | SHEET 1 OF 10

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SH 1	

+5VB
R33 330
DS1 YELLOW
-5VA
Q6 2N5434
R34 47K
U126 S08
U118 LS08
U121 S04
SH 8 CH -STRT
AB2
U120 LS74
SH 8 A -EOCNT
R41 1K
U126 S08
U165 74S74
U236 8641
BUS DC LO BF2
BUS INIT L AA1
U128 S02
U117 S00
U116 25NS DELAY LINE
U121 S04
U122 S132
U112 LS11
SH 3 B -I/O BLOCK
SH 4 C +ADDR SEL
-BUSY
U118 LS08
U129 LS00
U164 S22
U163 S10
SH 3,6,8 D +MSYN
MS RES
U122 S132
U121 S04
U121 S04
-CLK STOP
+CYCLE
+5VB
R45 4.7K
U129 LS00
△-EOC
U163 S10
U111 S37
U111 S37
U126 S08
U126 S08
U118 LS08
SH 3,7 H -ENB CSR
SH 8 J -ENB LOG
SH 3,7 K -WRT CSR
SH 4,8 L -WRT LOG
SH 3,7 M +WRITE
SH 3,5,7 N +READ
SH 3 E +BCO
SH 3 F +BAO
U119 LS74
U119 LS74
U113 S175
U114 S175
+T1
+T2
+T3
+T4
+T5
+T6
+T7
+T8
-T1
-T3
-T7
-T8
C125 270PF 100V
R42 82K
R46 10K
R47 10K
W17
W16
U130 26S02
U165 74S74
-RES RFSH
U122 S132
U128 S02
U117 S00
+T6 P SH 4
-T6 R SH 6
+T4 S SH 6
+ PWR UP V SH 8
+T3 U SH 4
-T2 W SH 4
-CLK STOP AL SH 6
PUI AC SH 8
+RFSH X SH 4
-PUSEQ Y SH 8
-CLEAR Z SH 7
-DC LO AA SH 8
+RAST AB SH 4
+RFH BH SH4,6
U127 LS04
+5VB
R39 4.7K
R38 10
C123 33PF 100V
R37 5.6K
U164 S22
+RFSH REQ
U122 S132
U123 S00
U123 S00
U123 S00
U187 S20
-RFSH
U117 S00
U117 S00
-RFH AE SH4
+CYCLE CK SH6
-LTCH ADDR/DATA AD SH3,5
U159 LS00
U120 LS74
U124 S10
U124 S10
-DATA HOLD AF SH 5
-DFM ENB AH SH 5
U112 LS11
U111 S37
U111 S37
R26 15
R20 15
-WRT 8 THRU 15 AJ SH 10
-WRT 0 THRU 7 AK SH 9
U127 LS04
U201 452
BUS SSYN L BU1
U129 LS00
-DOG AM SH 5

NEXT ASSY	USED ON

MATERIAL
FINISH
TOLERANCE ANG. 2 PL 3 PL
UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX

DR. BY	J.C.J.	02-27-79
CHK. BY		3-5-79
MFG.		
E.E.		
P.E.		

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

NS-11E
128K BYTE MEMORY

SIZE D | DR. NO. 870103839 | 001
SCALE NONE | SHEET 2 OF 10

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SH 1	

BUS MSYNL, BUS COL, BUS CIL, BUS A00, BUS A01, BUS A02 → TYP U227 8837 DB DA → COA, CIA, A0, A1, A2

BUS A03, BUS A04, BUS A05, BUS A06, BUS A07, BUS A08 → TYP U229 8837 DB DA → A3, A4, A5, A6, A7, A8

BUS A09, BUS A10, BUS A11, BUS A12, BUS A13, BUS A14 → TYP U228 8837 DB DA → A9, A10, A11, A12, A13, A14

BUS A15, BUS A16, BUS A17 → TYP U230 8837 DB DA → A15, A16, A17

BUS A18, BUS A19, BUS A20, BUS A21 → TYP U231 8837 DB DA → A18, A19, A20, A21

U124 SIO

COA, CIA, A0, A1, A2, A3, A4, A5 → U191 S373 → BA1, BA2, BA3, BA4, BA5

A6, A7, A8, A9, A10, A11, A12, A13 → U192 S373 → BA6, BA7, BA8, BA9, BA10, BA11, BA12, BA13

A14, A15, A16, A17, A18, A19, A20, A21 → U193 S373 → BA14, BA15, BA16, BA17, BA18, BA19, BA20, BA21

U186 S04

R53 10K, +5V, S1-9

SH 2,5 AD −LTCH ADDR/DATA

SH 7 AN +PAR

BA17, BA18, BA19, BA20 → U158 S283

BA13, BA14, BA15, BA16 → U157 S283

S3-

RP3-9 1K, +5V

BA21, BA20, BA19, BA18 → U187 S20

BA17, BA16, BA15, BA14, BA13, BA12 → U188 S30

S2-8, S2-9

U225 LS00, U226 S86, U152 LS04

R52 10K, R51 10K, +5V

BA12, BA10, BA6, BA11, BA9, BA8, BA7, BA5 → U150 S133

U186 S04, U151 S04

NA17, NA18, NA19, NA20, NA21 → U189 S260

RP3-10 1K, RP3-2 1K, RP3-3 1K, RP3-4 1K, RP3-5 1K, RP3-6 1K, RP3-7 1K, RP3-8 1K

SI-1, SI-2, SI-3, SI-4, RP1-9 1K, RP1-2 1K, RP1-3 1K, RP1-4 1K

U155 S283 → +> MAX, NA14, NA15, NA16

U224 LS08, U222 LS10 → +> MIN, −WRT CSR, −ENB CSR

CIA	T SH 6
+MSYN	D SH2,6,8
+BCO	E SH 2
+WRITE	M SH2,7
+BAO	F SH 2
+READ	N SH2,5,7
BA1−BA21	AP SH 4,7
PU3	AR SH4,6,8
+> MAX	AS SH 4
NA14	AT SH 4
NA15	AU SH 4
NA16	AV SH 4
	AW SH 4
+> MIN	AX SH 4
	AY SH 4
	AZ SH 4
−WRT CSR	K SH2,7
−ENB CSR	H SH2,7
	BA SH 4
	BB SH 4
−I/O BLOCK	B SH 2
CSRAD5	BC SH 4
CSRAD7	BD SH 4
CSRAD8	BE SH 4

MATERIAL	DR BY JCJ	02-27-79
FINISH	CHK BY	3-5-79
	M.E.	
	E.E.	
	P.E.	

UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.
TOLERANCE: ANG | 2 PL | 3 PL

NEXT ASSY | USED ON

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NS − 11E
128K BYTE MEMORY

SIZE D | DR NO. 870103839 | 001
SCALE NONE | SHEET 3 OF 10

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SH 1	

SH 2 W −T2

+5V R35 10K

W9 W10 W11 W12 W13

BA6 BA14

+5V R36 10K

(−CAS ADDR)

U107 3242 ROW ENB

BA1 9 A0 · BA2 5 A1 · BA3 7 A2 · BA4 21 A3 · BA5 23 A4 · 25 A5 · BA7 27 A6 · BA8 10 A7 · BA9 6 A8 · BA10 8 A9 · BA11 20 A10 · BA12 22 A11 · 24 A12 · BA13 26 A13

COUNT 1 · RFSH ENB 2

Q0 11 +MA0A · Q1 13 +MA1A · Q2 12 +MA2A · Q3 18 +MA3A · Q4 17 +MA4A · Q5 16 +MA5A · Q6 19 +MA6A

+MA0A THRU +MA6A BF SH 9,10

SH 3,7 AP BA1 − BA13

SH 2 X +RFSH

SH 2 AB +RAST

SH 3 AY

SH 3 AZ

SH 3,6,8 AR PU3

SH 3 BA

SH 3 BB

SH 3 BE CSR AD 8

SH 3 BD CSR AD 7

SH 3 BC CSR AD 5

+5V RP2-7 1K RP2-6 1K RP2-5 1K RP2-4 1K RP2-3 1K RP2-2 1K RP2-9 1K

S2-1 S2-2 S2-3 S2-4 S2-5 S2-6 S2-7

U186 S04 · U185 S30 · U186 S04

BA12 BA11 BA6

+5V RP1-8 1K RP1-7 1K RP1-6 1K RP1-5 1K

SI-5 SI-6 SI-7 SI-8 CSR ADDR

U190 7485 A=B COMPARATOR

A0 10 · A1 12 · A2 13 · A3 15 · B0 9 · B1 11 · B2 14 · B3 1 · A=B OUT 6 · IN · A<B 2 · A>B 4 · A=B 3

BA1 BA2 BA3 BA4

+5V R27 10K

+5V RP1-10 1K W14

U156 DM8136 STRB

T1 2 · T2 4 · T3 6 · T4 10 · T5 12 · T6 14 · OUT 9 · STRB 7

BA1 1 B1 · BA2 3 B2 · BA3 5 B3 · BA4 11 B4 · BA9 13 B5 · BA10 15 B6

U154 LS157

2A 5 · 2B 6 · 1A 2 · 1B 3 · 3A 11 · 3B 10 · 4A 14 · 4B 13 · S 1 · G 15 · 2Y 7 · 1Y 4 · 3Y 9 · 4Y 12

U153 S138

A 1 · B 2 · C 3 · G2A 4 · G2B 5 · G1 6 · Y0 15 · Y1 14 · Y2 13 · Y3 12 · Y4 11 · Y5 10 · Y6 9 · Y7 7

U110 LS00 (12,13→11 · 4,5→6 · 1,2→3 · 9,10→8)

U152 LS04 (11→10 · 5→6)

U223 LS11 (4,5→6)

U128 S02 (11,12→13 · 3,2→1)

SH 3 AT NA14

SH 3 AU NA15

SH 3 AV NA16

SH 3 AW +>MIN

SH 3 AX

SH 3 AS +>MAX

SH 2 AE −RFH

SH 2 U +T3

SH 2 P +T6

SH 2,6 BH +RFH

U222 LS10 (2,1→12 · 13,1→12)

−WRT LOG L SH 2,8

+RD LOG BJ SH 8

RA1 BK SH 8

RA0 BL SH 8

U109 S37 · U108 7437

RI9 RI6 R22 R23 RI7 RI8 R25 R24 15

−RAS0 BM SH 9,10

−RAS1 BN SH 9,10

−RAS2 BP SH 9,10

−RAS3 BR SH 9,10

−CAS0 BS SH 9,10

−CAS1 BT SH 9,10

−CAS2 BU SH 9,10

−CAS3 BV SH 9,10

+ADDR SEL C SH 2

MATERIAL		DR. BY JCJ	02-27-79
FINISH		CHK.	3-5-79
		M.E.	
		E.E.	
		P.E.	

UNLESS OTHER SPECIFIED

TOLERANCE: ANG. — 2 PL — 3 PL

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.

REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.

NEXT ASSY | USED ON

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NS − IIE
128K BYTE MEMORY

SIZE D · DR. NO. 870103839 · 001

SCALE NONE · SHEET 4 OF 10

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SH 1	

SH 6 BW CORR 0 – CORR 7

SH 9 BX DFM 0 – DFM 7

SH 6 BW CORR 8 – CORR 15

DO – DI5 BZ SH6,7, 8,9,10

SH 2,3 AD –LTCH ADDR/DATA
SH 2,3,7 N +READ
SH 2 AH –DFM ENB
SH 10 BY DFM 8 – DFM 15
SH 2 AF –DATA HOLD

MATERIAL	DR. BY JCJ 02-27-79
FINISH	DES. M.E. 3-5-79
	E.E.
	P.E.
UNLESS OTHER SPECIFIED	
TOLERANCE: ANG. — 2 PL. — 3 PL. —	DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.
NEXT ASSY	USED ON

National Semiconductor Corporation
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NS-11E
128K BYTE MEMORY

SIZE D DR. NO. 870103839 001
SCALE NONE SHEET 5 OF 10

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SH 1	

+MOD WRITE

SH 2,4 BH +RFH
SH2 S +T4
SH2 R −T6

SH3 T CIA
SH2 CK +CYCLE
SH2 AL −CLK STOP

U147 S74 PR P/O

SH 3,4,8 AR PU3
2,3,8 D +MSYN
9,10 CA DFMC0 − DFMC9

U125 S260 · U148 S32 · U212 S260

ΣE0 · ΣE1 · U148 S32

+5V
RP4-3 10K DFMC0 · RP4-5 10K DFMC1 · RP4-2 10K DFMC2 · RP4-4 10K DFMC3 · RP5-4 10K DFMC4
DFMC5 RP4-7 10K · DFMC6 RP4-6 10K · DFMC7 RP5-2 10K · DFMC8 RP5-3 10K · DFMC9 RP4-8 10K

+PAR FRCE CD SH7
+ERR CLK CC SH8

SO−S9 CE SH8

7 CB +WRT ERR
5,7,8,9,10 BZ DO THRU D15

U174 S135 · U173 S135 · U138 S86 · U139 S86 · U211 S280 · U208 S138 · U206 S138

C0 C1 C2 C3 C4 C5 C6 C7 C8 C9
DFMC0 DFMC1 DFMC2 DFMC3 DFMC4 DFMC5 DFMC6 DFMC7 DFMC8 DFMC9
S0 S1 S2 S3 S4 S5 S6 S7 S8 S9

C9 ERR · C5 ERR · C6 ERR · CORR 8 · C7 ERR · CORR 9 · CORR 10
C4 ERR · C0 ERR · CORR 0 · C2 ERR · CORR 1 · CORR 2

+5V R48 10K
LO = ECC OFF
S1-10
U141 S04

U172 S135 · U171 S135 · U170 S135 · U135 S86 · U137 S86 · U136 S86 · U210 S280 · U209 S138 · U207 S138

C3 ERR · CORR 3 · CORR 4 · CORR 5 · CORR 6 · CORR 7
C8 ERR · CORR 11 · CORR 12 · CORR 13 · CORR 14 · CORR 15

CORR 0 − CORR 15 BW SH5

MC0 − MC9 CF SH 9,10

U133 LS 157 · U134 LS 157 · U132 LS 157 · U131

EC0 EC1 EC2 EC3 EC4 EC5 EC6 EC7 EC8 EC9
MC0 MC1 MC2 MC3 MC4 MC5 MC6 MC7 MC8 MC9

+5V R43 10K

MATERIAL		DR. BY JCJ	02-27-79
FINISH		M.E.	3-5-79
		E.E.	
		P.E.	

UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.
TOLERANCE: ANG. · 2 PL. · 3 PL.

NEXT ASSY · USED ON

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NS-IIE
128K BYTE MEMORY

SIZE D · DR. NO. 870103839 001
SCALE NONE · SHEET 6 OF 10

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SH 1	

AR1 +12V TEST

+5VB — C115 33 35V,20% — C113 .47 — F1 4.0 AMP

U105 SG3524: VREF, VIN, NI, INV, RT, CT, OV, OSC, COMP, −CL, +CL, C1, C2, E1, E2

R11 2.21K 1% — R12 2.21K 1% — R13 8.87K 1% — R10 2.21K 1% — C110 4700PF 100V — R9 10K — C112 .47 — R8 470 1/4W — R6 36 1/2W

Q1 2N4014 — Q2 — Q3 — Q4 — Q5

L1 150UH — R7 2.2K 1/4W — C109 33 35V,20%

CR5 IN5817 — CR6 IN5817 — CR7 — CR8 — CR3 — CR4 — CR9 MPTE 12 — CR1 IN5817 — CR2 IN5231B

C107 33 35V 20% — C108 33 35V 20% — C106 22 35V,20% — C105 33 35V 20% — C111 1000PF 100V — C114 4.7 10V,20% — R14 47K — R15 1M — R2 1 1/2W — R3 1 1/2W — R5 1 1/2W — R4 1 1/2W — R1 150 1/4W

W5 — W3 — W4 — W1 — W2

+12V — −5V$_A$ — −5V

AS1 −5V TEST

+5VB — R28 1K — S3-10

U112 LS11 — +WRT ERR CB SH6 — +PAR AN SH3

U118 LS08 — U121 S04 — U159 LS00

SH 2,3,6 M +WRITE
SH 6 CD +PAR FRCE
SH 2,3 K −WRT CSR
SH 3,4 AP BA11−BA21
SH 5,6,8 BZ D0−D15
9,10 SH 2,3,5 N +READ

U194 LS157 — U195 S157 — U196 S374 — U162 S373 — U198 S374

U201 452

AN2 BUS PB L
SH 2,3 H −ENB CSR

+PAR ERR

U121 S04 — −ENB 11−17

CSR 0
+CSR 2
CSR 15

D2 — D14 — D0

+5V — R44 10K

U161 74S74 — U160 74S74 — U159 LS00 — −ENB 18−21

SH 2 Z −CLEAR

U127 LS04

−CSR2 CJ SH8

+5V$_B$ — DS2 RED — R21 330

NEXT ASSY	USED ON

MATERIAL	DR. BY JCJ	02-27-79	National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH	CHK. BY	3-5-79	NS-IIE 128K BYTE MEMORY
	M.E.		
	E.E.		
	P.E.		

UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.
TOLERANCE: ANG ___ 2 PL ___ 3 PL ___

SIZE D | DR. NO. 870103839 | 001
SCALE NONE | SHEET 7 OF 10

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SH 1	

SH4 BL RA0
SH4 BK RA1
SH6 CE S0–S9
U213 LS193 U214 LS193 U215 LS193
+RES CNT
–LOAD
U143 4044
U178 S374 U179 S374
–STRT CH SH2
LTCH DATA
U184 S00
U180 S02
28 MIN 33TYP
U181 LS04 U221 LS00 +COUNT
–START
SH 2 Y –PUSE Q
SH 2 AC PU1
U130 26S02 P/O
+5VB R40 5.6K
U145 LS08
DO–D15 SH 5,6,7, 8,9,10 BZ
–EOCNT A SH 2
U221 LS00 U224 LS08
–ENB LOG J SH 2
U149 LS10
LD14
LD15
SH5,6,7, 8,9,10 BZ DO–DI
DO DI
U151 S04
SH 2,4 L –WRT LOG
U218 LS74 U216 LS74 U217 LS74 U220 74S74 U219 LS74
+Q1 +Q2 –Q1 –Q2 + L RUN
U152 LS04
SH 4 BJ +RD LOG
SH 2,3,6 D +MSYN
SH 2 V +PWR UP
SH 2 AA –DC LO
U148 S32
U145 LS08
+L READ
+L WRITE
U146 LS00
U224 LS08
+5V RP2-10 1K
SH 3,4,6 AR PU3
U149 LS10 –LEOC
U152 LS04
U181 LS04
U182 DELAY LINE 100 NS
+5V R50 220 R49 270
–LT6
U183 S140
–LT10
+LEOC
U184 S00
–COUNT
+ERR
U223 LS11
+LT10
SH 7 CJ –CSR2
SH 6 CC + ERR CLK
50

MATERIAL	
FINISH	
NEXT ASSY	USED ON

DR. BY	JCJ	02-27-79
CHK		3-5-79
M.E.		
E.E.		
P.E.		

UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.
TOLERANCE: ANG. — 2 PL — 3 PL —

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NS–11E
128K BYTE MEMORY

SIZE D | DR. NO. 870103839 | 001
SCALE NONE | SHEET 8 OF 10

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SH 1	

SH 6,10 CF — MC 0 – MC 4

SH 5, BZ — D0 – D7
6,7,8,10

+MA0A THRU +MA6A
SH 4,10 BF

SH 4,10 BM — –RAS 0
4,10 BS — –CAS 0

SH 4,10 BN — –RAS 1
4,10 BT — –CAS 1

SH 4,10 BP — –RAS 2
4,10 BU — –CAS 2

SH 4,10 BR — –RAS 3
4,10 BV — –CAS 3

SH 2 AK — –WRT 0 THRU 7

	D0	D1	D2	D3	D4	D5	D6	D7	MC 0	MC 1	MC 2	MC 3	MC 4
+MA0A 5	U 1	U 2	U 3	U 4	U 5	U 6	U 7	U 8	U 9	U 10	U 11	U 12	U 13
+MA1A 7	U 27	U 28	U 29	U 30	U 31	U 32	U 33	U 34	U 35	U 36	U 37	U 38	U 39
+MA2A 6	U 53	U 54	U 55	U 56	U 57	U 58	U 59	U 60	U 61	U 62	U 63	U 64	U 65
+MA3A 12	U 79	U 80	U 81	U 82	U 83	U 84	U 85	U 86	U 87	U 88	U 89	U 90	U 91
+MA4A 11													
+MA5A 10													
+MA6A 13													
4													
15													
2													
3													
14	DFM 0	DFM 1	DFM 2	DFM 3	DFM 4	DFM 5	DFM 6	DFM 7	DFM CO	DFM C1	DFM C2	DFM C3	DFM C4

DFM CO THRU DFM C4 — CA — SH 6,10
BX — SH 5
DFM 0 THRU DFM 7

(TYP X104)

(–5V) VBB	1	16	VSS (GND)
DI	2	15	–CAS
–WRT	3	14	DO
–RAS	4	13	A6
A0	5	12	A3
A2	6	11	A4
A1	7	10	A5
(+12V) VDD	8	9	VCC (+5B)

16K RAM

NEXT ASSY	USED ON

MATERIAL

FINISH

TOLERANCE: ANG. — 2 PL — 3 PL

UNLESS OTHER SPECIFIED

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.

REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.

	DR. BY	CHK.	M.E.	E.E.	P.E.
	JCJ 02-27-79	3-5-79			

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NS–IIE
128K BYTE MEMORY

SIZE D — DR. NO. 870103839 — 001

SCALE NONE — SHEET 9 OF 10

REVISIONS			
REV	DATE	ECO NO.	APPVD
B		SEE SH 1	

SH 6,9 CF — MC5 – MC9

SH 5,6,7,8,9 BZ — D8 – D15

+MA0A THRU +MA6A

SH 4,9 BF

SH 4,9 BM — −RAS 0

SH 4,9 BS — −CAS 0

SH 4,9 BN — −RAS 1

SH 4,9 BT — −CAS 1

SH 4,9 BP — −RAS 2

SH 4,9 BU — −CAS 2

SH 4,9 BR — −RAS 3

SH 4,9 BV — −CAS 3

SH 2 AJ — −WRT 8 THRU 15

D8	U 14	U 40	U 66	U 92	D9	U 15	U 41	U 67	U 93
D10	U 16	U 42	U 68	U 94	D11	U 17	U 43	U 69	U 95
D12	U 18	U 44	U 70	U 96	D13	U 19	U 45	U 71	U 97
D14	U 20	U 46	U 72	U 98	D15	U 21	U 47	U 73	U 99
MC5	U 22	U 48	U 74	U 100	MC6	U 23	U 49	U 75	U 101
MC7	U 24	U 50	U 76	U 102	MC8	U 25	U 51	U 77	U 103
MC9	U 26	U 52	U 78	U 104					

Each DFM 8 / DFM 9 / DFM 10 / DFM 11 / DFM 12 / DFM 13 / DFM 14 / DFM 15 / DFM C5 / DFM C6 / DFM C7 / DFM C8 / DFM C9 connects:

+MA0A	5	2	14
+MA1A	7		
+MA2A	6		
+MA3A	12		
+MA4A	11		
+MA5A	10		
+MA6A	13		
	4		
	15	3	

DFM C5 THRU DFM C9 — CA — SH 6,9

BY — SH 5

DFM 8 THRU DFM 15

(TYP X104)

(−5V) V_{BB}	1	16	V_{SS} (GND)
DI	2	15	−CAS
−WRT	3	14	DO
−RAS	4	13	A6
A0	5	12	A3
A2	6	11	A4
A1	7	10	A5
(+12V) V_{DD}	8	9	V_{CC} +5B

16K RAM

MATERIAL		DR. BY JCJ	02-27-79
		CHK. BY	3-5-79
FINISH		M.E.	
		E.E.	
		P.E.	

UNLESS OTHER SPECIFIED

TOLERANCE: ANG. — 2 PL. — 3 PL.

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.

REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.

NEXT ASSY	USED ON

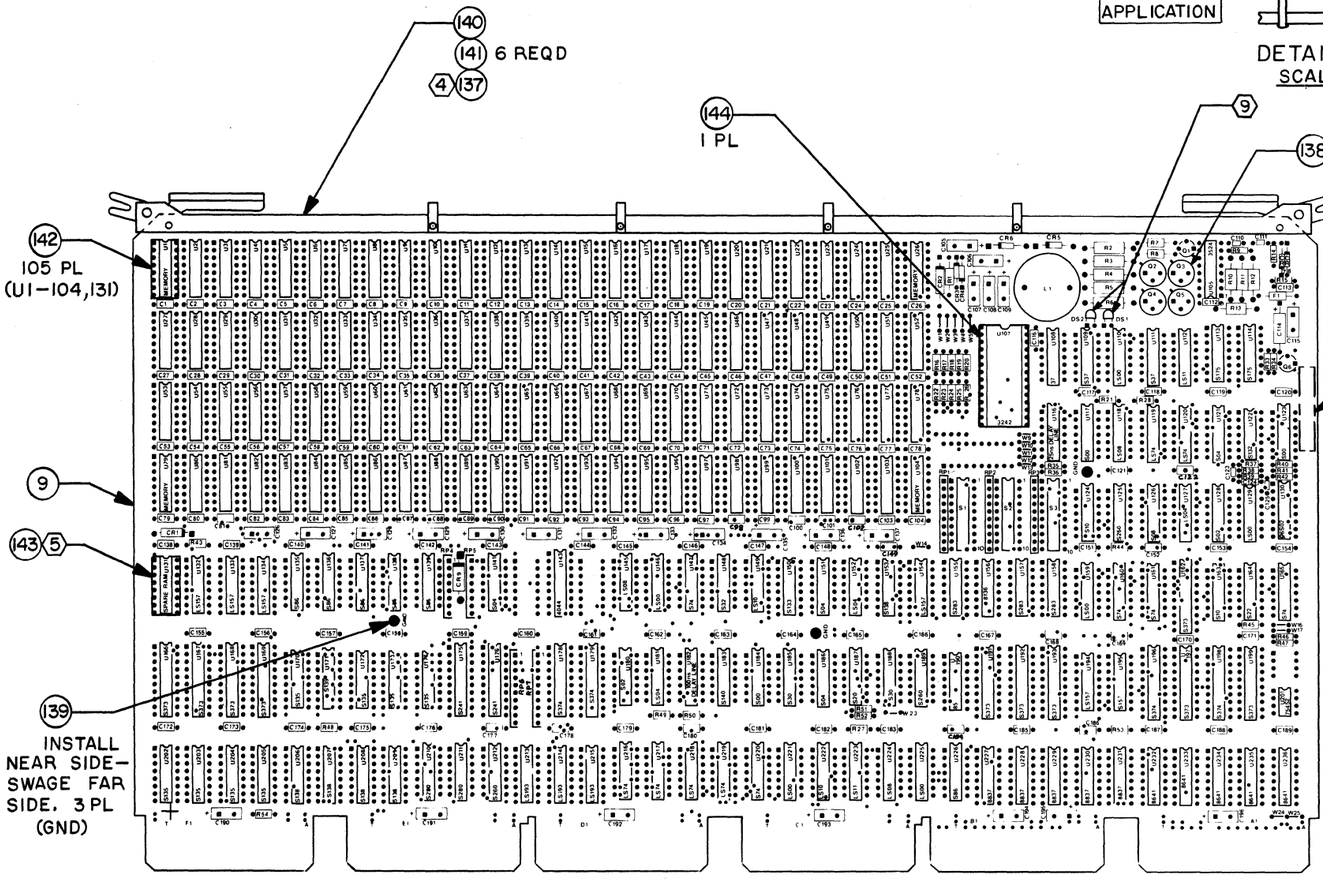
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

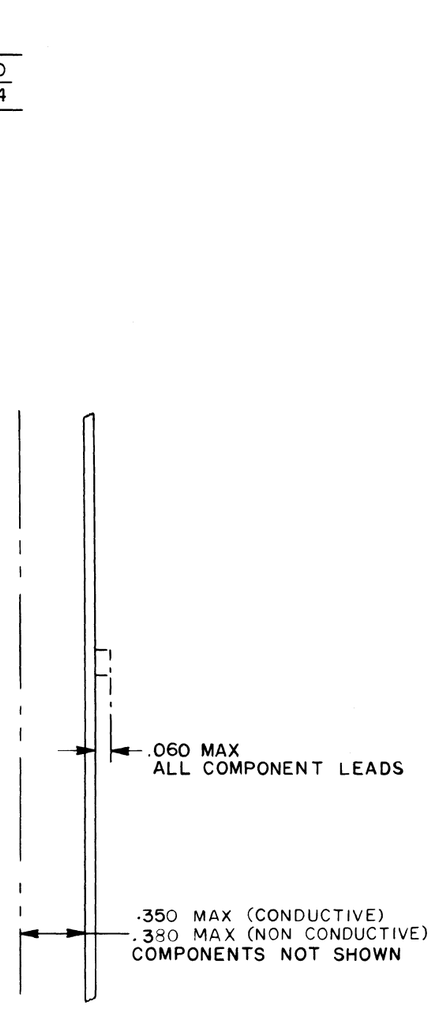
NS−11E
128K BYTE MEMORY

SIZE D — DR. NO. 870103839 — 001

SCALE NONE — SHEET 10 OF 10

REVISIONS			
REV	DATE	ECO NO.	APPVD
C	8-13-79	PDD 3468	Conaway
D	9-25-79	PCO 2-3618	Conaway
E	10-4-79	RELEASE ECO 43037	Conaway





1. ASSEMBLE AND SOLDER PER NSC SPEC. 429101895.

(2) MARK ASSY. DASH NO., S/N AND REV. LEVEL WITH .12–.18 HIGH CHARACTERS WHERE SHOWN.

3. ALL JUMPER OPTIONS SHOULD BE INSTALLED USING ITEM 135.

(4) APPLY ITEM 137 (LOCTITE) TO TAPPED HOLES IN ITEM 140 (STIFFENER) PRIOR TO INSERTING ITEM 141 (SCREWS).

(5) INSTALL ITEM 143 AFTER PRE-TESTING PER TEST SPEC. 425103839.

(6) INSTALL MEMORY I.C.'S AND JUMPERS ACCORDING TO THE TABULATED DATA CHART.

7. FACTORY INSTALLED JUMPERS FOR ALL VERSIONS ARE W1, W4 & W25.

(8) AFTER FINAL TEST INSTALL/REMOVE JUMPERS AS DEFINED BY THE MARKETING CONFIGURATION CODE TABLE.

(9) 1. SHORT LEG IS CATHODE.
2. CATHODE TO SQUARE PAD.
3. BEND PER DETAIL A–A BEFORE INSTALLATION.

(6) TABULATED DATA CHART

VERSION	RAM QTY	POPULATED MEMORY ELEMENT LOCATIONS	BILL OF MATL ITEM NO			JUMPERS INSTALLED	SYSTEM CAPACITY
			16K	8K RH	8K LH		
–001	104	U1 THRU U104	ITEM 145			W10, W13	64K
–002	52	U1 THRU U52	ITEM 145			W10, W13	32K
–003	104	U1 THRU U104		ITEM 146		W9, W11, W14	32K
–004	104	U1 THRU U104			ITEM 147	W11, W14	32K

(8) MARKETING CONFIGURATION CODE TABLE
USER SELECTABLE OPTION JUMPERS

MKTG CONFIG. CODE	JUMPERS		REMARKS
	INSTALLED	REMOVED	
NONE	—	—	NO OPTIONS
01	W24	W25	BATTERY BACKUP

MATERIAL	
FINISH	
TOLERANCE	ANG / 2 PL / 3 PL
NEXT ASSY	USED ON

DR BY	A.C. Jacobs	7-5-79
CHK	Conaway	9-25-79
ME	Conaway	9-25-79
FE	Conaway	10-16-79
PE	Conaway	10-16-79

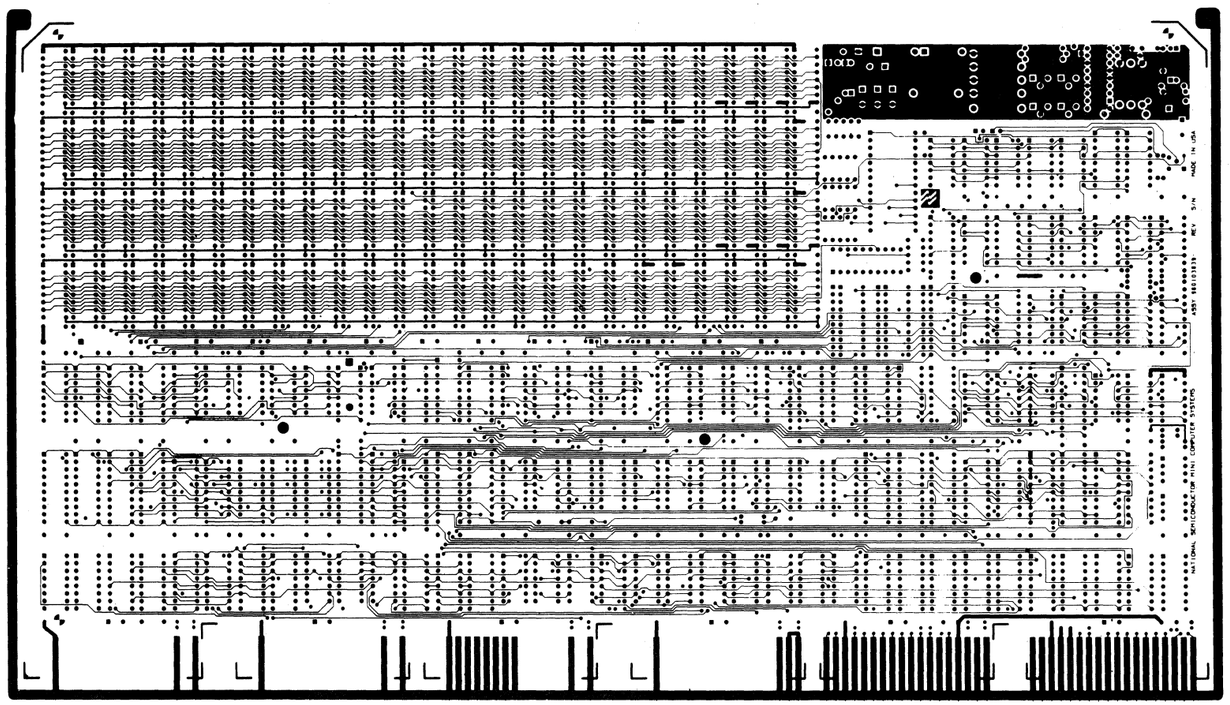
UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS
.015 MAX

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

PCB ASSEMBLY DRAWING
NSIIE
128K BYTE MEMORY

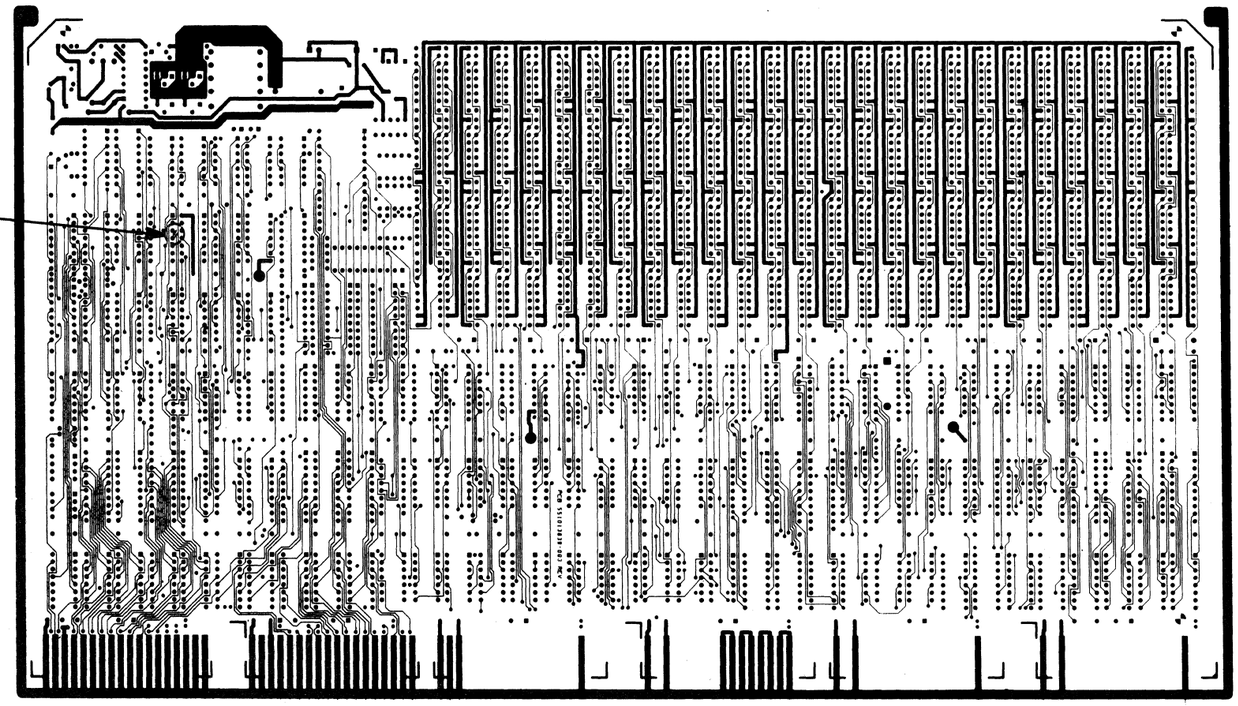
SIZE D | DR NO 980103839 | 000
SCALE 1/1 | SHEET 1 OF 2

REVISIONS			
REV	DATE	ECO NO.	APPVD
D	9-25-79	PCO 2-3618	
E	10-4-79	RELEASE ECO 43037	



COMPONENT SIDE

REWORK INSTRUCTIONS



CIRCUIT SIDE

1. CUT TRACE BETWEEN U120-3 AND U127-2.

MATERIAL	DR BY J.C. Jacobs 9-25-79	National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051	
FINISH	CH BY		
	APP'D	SEE SHT 1	ASSEMBLY DRAWING NS II E 128 K BYTE MEMORY
	UNLESS OTHER SPECIFIED		
	DIMENSIONS ARE IN INCHES AND ALL DIE CHEMICALLY APPLIED FINISHES	SIZE D	DR NO 980103839 000
	TOLERANCE ANG. 2 PL 3 PL	REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS .015 MAX	SCALE NONE SHEET 2 OF 2
NEXT ASSY	USED ON		

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
KEY (1): A = WITH B/M, D = WITHOUT B/M, R = REFERENCE, S = SPECIFICATION
KEY (2):
RELEASED FOR ASSEMBLY:
BILL OF MATERIAL NO: 980103839-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
1								
2								
3	0	04	R		870103839-001	SCHEMATIC DIAGRAM		
4	0	04	R		427103839-001	TEST PROCEDURE		
5	0	04	S		425103839-001	TEST SPEC		
6	0	04	S		426103839-001	PRODUCT SPEC		
7								
8								
9	1	04	D		551103839-003	PC BOARD		
10								
11	6	04			482000354-001	I.C. 74LS00		U110,129,146
12								159,221,225
13	3	04			482000079-001	74S00		U117,123,184
14	2	04			482000334-001	74S02		U128,180
15	3	04			482100785-001	I.C 74LS04		U127,152,181
16								

ASSY USAGE REF:
NOTES:

ENG CHG	REV	C	D	E
	CHG NO.	PDD 3428	PCO 2-3619	ECO 4-3037
	DATE	8-13-79	9-25-79	10-4-79
	APPR	[illegible]	[illegible]	[illegible]

TITLE: NS11E 128 K BYTE MEMORY

WRITTEN BY: D Taylor 3-5-79 | DATE | DESIGN | DATE
CHECKED BY | DATE | APPROVED | DATE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE | BILL OF MATERIAL NO 980103839-000 | SH 1 OF 10

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
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BILL OF MATERIAL NO: 980103839-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
17	4	04			482000180-001	I.C. 74S04		U121, 141,
18								151, 186
19	3	04			482102770-001	74LS08		U118,145,224
20	1	04			482100672-001	74S08		U126
21	2	04			482105000-001	74LS10		U149, 222
22	2	04			482001344-001	74S10		U124, 163
23	2	04			482101178-001	74LS11		U112, 223
24	1	04			482001345-001	74S20		U187
25	1	04			482000438-001	74S22		U164
26	2	04			482000335-001	74S30		U185, 188
27	1	04			482101026-001	74S32		U148
28	1	04			482001341-001	7437		U108
29	2	04			482100777-001	74S37		U109, 111
30	6	04			482100365-001	I.C. 74LS74		U119, 120,
31								216-219
32								

ASSY USAGE REF:
NOTES:

ENG CHG	REV	C	D	E
	CHG NO.	PDD 3428	PCO 2-3619	
	DATE	SEE SHT 1	SEE SHT 1	SEE SHT 1
	APPR	—	—	

TITLE: NS11E 128 K BYTE MEMORY

WRITTEN BY: D Taylor 3-5-79 | DATE | DESIGN | DATE
CHECKED BY | DATE | APPROVED | DATE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE | BILL OF MATERIAL NO 980103839-000 | SH 2 OF 10

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
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BILL OF MATERIAL NO: 980103839-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
33	3	04			482000179-001	I.C. 74S74		U147,160,161,
34								165,220
35	1	04			482103946-001	7485		U190
36	6	04			482000300-001	74S86		U135-139,226
37	1	04			482100840-001	74S132		U122
38	1	04			482000310-001	74S133		U150
39	9	04			482001174-001	74S135		U170-174
40								202-205
41	5	04			482000314-001	74S138		U153,
42								206-209
43	1	04			482000355-001	74S140		U183
44	5	04			482100784-001	74LS157		U132-134,
45								154,194
46	2	04			482000437-001	74S175		U113,114
47	3	04			482102001-001	74LS193		U213-215
48	1	04			482000302-001	I.C. 74S157		U195

ASSY USAGE REF:
NOTES:

ENG CHG	REV	C	D	E
	CHG NO.	PDD 3428	PCO 2-3619	
	DATE	SEE SHT 1	SEE SHT 1	SEE SHT 1
	APPR	—	—	

TITLE: NS11E 128 K BYTE MEMORY

WRITTEN BY: D Taylor 3-5-79 | DATE | DESIGN | DATE
CHECKED BY | DATE | APPROVED | DATE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE | BILL OF MATERIAL NO 980103839-000 | SH 3 OF 10

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
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BILL OF MATERIAL NO: 980103839-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
49	2	04			482104624-001	I.C. 74S241		U175,176
50	3	04			482101177-001	74S260		U125,189,212
51	2	04			482000342-001	74S280		U210, 211
52	3	04			482102505-001	74S283		U155,157,158
53	10	04			482102641-001	74S373		U162,
54								166-169,
55								191-193,
56								197,199
57	4	04			482101837-001	74S374		U178,179
58								196,198
59	1	04			482103971-001	75452		U201
60	1	04			482102062-001	26S02		U130
61	1	04			482104781-001	3242		U107
62	1	04			482104950-001	4044		U143
63	1	04			482000376-001	I.C. 8136		U156
64								

ASSY USAGE REF:
NOTES:

ENG CHG	REV	C	D	E
	CHG NO.	PDD 3428	PCO 2-3619	—
	DATE	SEE SHT 1	SEE SHT 1	SEE SHT 1
	APPR	—	—	—

TITLE: NS11E 128 K BYTE MEMORY

WRITTEN BY: D Taylor 3-5-79 | DATE | DESIGN | DATE
CHECKED BY | DATE | APPROVED | DATE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE | BILL OF MATERIAL NO 980103839-000 | SH 4 OF 10

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
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BILL OF MATERIAL NO: 980103839-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
65	5	04			482103697-001	I.C. 8641		U232-236
66	5	04			482000248-001	8837		U227-231
67	1	04			482104567-001	I.C. 3524		U105
68								
69								
70								
71	1	04			611100900-100	DELAY LINE 100 NS		U182
72	1	04			611104536-001	DELAY DIGITAL 25NS		U116
73	1	04			394105352-002	LED (YELLOW)		DS1
74	1	04			394105352-001	LED (RED)		DS2
75	3	04			513100986-010	SWITCH, DIP 10 POS		S1-3
76	1	04			518102113-011	FUSE 4.0 AMP		F1
77	1	04			180105031-001	INDUCTOR 150 UH		L1
78								
79								
80								

ASSY USAGE REF:
NOTES:

ENG CHG	REV	C	D	E
	CHG NO.	PDD 3428	PCO 2-3619	—
	DATE	SEE SHT 1	SEE SHT 1	SEE SHT 1
	APPR	—	—	—

TITLE: NS11E 128 K BYTE MEMORY

WRITTEN BY: D Taylor 3-5-79 | DATE | DESIGN | DATE
CHECKED BY | DATE | APPROVED | DATE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE | BILL OF MATERIAL NO 980103839-000 | SH 5 OF 10

FORM NO. 0011A

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BILL OF MATERIAL NO: 980103839-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
81	3	04			481100853-001	DIODE IN5817		CR1,5,6
82	4	04			481101049-001	DIODE IN4531		CR3,4,7,8
83	1	04			481100775-001	DIODE,ZENER IN5231B		CR2
84	1	04			480105601-001	TRANSZORBS BV 12.0V		CR9
85	1	04			480103970-001	TRANSISTOR,FET 2N5484		Q6
86	4	04			480105342-001	TRANSISTOR 2N3506		Q2-5
87	1	04			480104767-001	TRANSISTOR 2N4014		Q1
88								
89								
90	3	04			474101854-001	RES.MOD 10PIN SIP 1K		RP1-3
91	2	04			474100807-066	RES. MOD 8 PIN SIP 10K		RP4,5
92	2	04			474101954-002	RES. MOD 10 PIN SIP 10K		RP6,7
93	1	04			470100611-043	RES.CC 150Ω, 1/4W, 5%		R1
94	4	04			470101135-001	RES CC 1Ω, 1/2W, 5%		R2-5
95	1	04			470101135-038	RES CC 36Ω, 1/2W, 5%		R6
96	1	04			470100611-071	RES CC 2.2K, 1/4W, 5%		R7

ASSY USAGE REF:
NOTES:

ENG CHG	REV	C	D	E
	CHG NO.	PDD 3468	PCO 2-3618	-
	DATE	SEE SHT 1	SEE SHT 1	SEE SHT 1
	APPR	—	—	—

TITLE: NS11 E 128K BYTE MEMORY

WRITTEN BY: D Hayton 3-5-79 DATE DESIGN DATE
CHECKED BY DATE APPROVED DATE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE | BILL OF MATERIAL NO 980103839-000 | SH 6 OF 10

FORM NO. 0011A

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BILL OF MATERIAL NO: 980103839-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
97	1	04			470100611-055	RES CC 470Ω, 1/4W, 5%		R8
98								
99	3	04			474102565-038	RES,FILM 2.21K, 1/8W, 1%		R10-12
100	1	04			474102565-096	RES,FILM 8.87K, 1/8W, 1%		R13
101								
102	1	04			470101134-135	RES.CC 1MΩ, 1/8W, 5%		R15
103	10	04			470101134-019	RES.CC 15Ω, 1/8W, 5%		R16-20,22-26
104	2	04			470101134-051	RES.CC 330Ω, 1/8W, 5%		R21,33
105	2	04			470101134-103	RES.CC 47K, 1/8W, 5%		R14,34
106	13	04			470101134-087	RES.CC 10K, 1/8W, 5%		R9,27,35,36
107								43,44,46-48
108								51-54
109	7	04			470101134-081	RES,CC 5.6K, 1/8W, 5%		R37,40
110	1	04			470101134-015	RES.CC 10Ω, 1/8W, 5%		R38
111	2	04			470101134-079	RES.CC 4.7K, 1/8W, 5%		R39,45
112								

ASSY USAGE REF:
NOTES

ENG CHG	REV	C	D	E
	CHG NO.	PDD 3468	PCO 2-3618	-
	DATE	SEE SHT 1	SEE SHT 1	SEE SHT 1
	APPR	—	—	—

TITLE: NS11 E 128K BYTE MEMORY

WRITTEN BY: D Hayton 3-5-79 DATE DESIGN DATE
CHECKED BY DATE APPROVED DATE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE | BILL OF MATERIAL NO 980103839-000 | SH 7 OF 10

FORM NO. 0011A

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BILL OF MATERIAL NO: 980103839-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
113	2	04			470101134-063	RES.CC,1K, 1/8W, 5%		R28,41
114	1	04			470101134-109	RES.CC,82K, 1/8W, 5%		R42
115	1	04			470101134-049	RES.CC 270Ω, 1/8W, 5%		R49
116	1	04			470101134-047	RES.CC 220Ω, 1/8W, 5%		R50
117								
118								
119								
120								
121	164	04			151104975-012	CAP,CER,.47UF,50V,10%		C1-104,112,
122								113,116-122,
123								124,128-147, 151-189
124	19	04			155105442-005	CAP.TANT, 15UF,25V,20%		C126-137,
125								190-196
126								
127	1	04			155104570-003	CAP.TANT, 22UF,35V,20%		C106
128	1	04			151101308-033	CAP,CER,.9700PF,100V,10%		C110

ASSY USAGE REF:
NOTES:

ENG CHG	REV	C	D	E
	CHG NO.	PDD 3468	PCO 2-3618	-
	DATE	SEE SHT 1	SEE SHT 1	SEE SHT 1
	APPR	—	—	—

TITLE: NS11 E 128K BYTE MEMORY

WRITTEN BY: D Hayton 3-5-79 DATE DESIGN DATE
CHECKED BY DATE APPROVED DATE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE | BILL OF MATERIAL NO 980103839-000 | SH 8 OF 10

FORM NO. 0011A

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BILL OF MATERIAL NO: 980103839-000

ITEM/FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
129	1	04			151101308-025	CAP,CER.1000 PF,100V,10%		C111
130	1	04			155100628-017	CAP.TANT 4.7UF,10V,20%		C114
131	1	04			151101308-007	CAP,CER. 33PF, 100V, 10%		C123
132	1	04			151101308-018	CAP,CER. 270PF, 100V, 10%		C125
133	5	04			155104570-004	CAP,TANT, 33 UF, 35V, 20 %		C105,107-109,
134								115
135	0	04			600100155-005	WIRE,PVC 24AWG,SOLID,GRN		
136	0	04			600100158-005	WIRE,PVC 30 AWG,SOLID,GRN		
137	0	04			160101790-001	LOCTITE		
138	4	04			790002971-001	TRANSISTOR PAD		Q2-5
139	3	04			215100496-003	TERMINAL		
140	1	04			980103715-001	STIFFENER-EJECTOR		
141	6	04			230100065-006	SCREW,4-40 x 3/8LG PH		
142	105	04			214102685-003	I.C.SOCKET, 16 PIN		U1-104, 131
143	1	04			482102598-012	16K RAM 200 NS		U131
144	1	04			214103006-006	I.C. SOCKET, 28 PIN		U107

ASSY USAGE REF:
NOTES:

ENG CHG	REV	C	D	E
	CHG NO.	PDD 3468	PCO 2-3618	-
	DATE	SEE SHT 1	SEE SHT 1	SEE SHT 1
	APPR	—	—	—

TITLE: NS11 E 128K BYTE MEMORY

WRITTEN BY: D Hayton 3-5-79 DATE DESIGN DATE
CHECKED BY DATE APPROVED DATE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE | BILL OF MATERIAL NO 980103839-000 | SH 9 OF 10

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
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ITEM/FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
145	0	04			482102598-012	16K RAM, 200NS		(6)
146	0	04			482102989-112	8K PARTIAL RAM-R.HALF 200NS		(6)
147	0	04			482103060-112	8K PARTIAL RAM-L.HALF 200NS		(6)
148								
149								
150								
151								
152								
153								
154								
155								
156								
157								
158								
159								
160								

ASSY USAGE REF:
NOTES

ENG CHG	REV	C	D	E
	CHG NO.	PDD 3468	PCO 2-3618	-
	DATE	SEE SHT 1	SEE SHT 1	SEE SHT 1
	APPR	—	—	—

TITLE: NS11 E 128K BYTE MEMORY

WRITTEN BY: D Hayton 3-5-79 DATE DESIGN DATE
CHECKED BY DATE APPROVED DATE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE | BILL OF MATERIAL NO 980103839-000 | SH 10 OF 10

FORM NO. 0011A