Hardware Reference Manual

ATRON

ATRON 601 CONTROLLERS

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Controllers designed from these assemblies are:

- LOW COST because they are constructed from standard assemblies produced in large volume, require low system development cost, and eliminate wasted capability.

- PROGRAMMABLE with a comprehensive instruction repertoire. To change the function performed by the Controller, it is only necessary to change the microprogram stored in Program Memory.

- HIGH PERFORMANCE with a 260 nanosecond Micro-Processor, 260 nanosecond Program Memories, and 1 microsecond Main Memories.

- FIELD MODIFIABLE and FIELD EXPANDABLE. Standard bus interfaces allow easy field-substitution or addition of assemblies.

A typical ATRON 601 Controller consists of a Micro-Processor Assembly, one or more Read-Only Program Memory Assemblies, an appropriate Interface Adaptor Assembly, and may include a Core\or Semiconductor Main Memory as needed. Each assembly (with the exception of Core Memory) is on a single 9.65 inch by 11 inch printed-circuit board. An Interconnect Unit houses and interconnects the assemblies.

The Micro-Processor can execute an instruction in 260 nanoseconds, contains a 16-byte internal scratch pad memory, and directly addresses external units on a bus interface. The instruction repertoire shown below is both single and two address and has complete arithmetic, logical, and shifting capability as well as extensive literal facility for program storage efficiency. The following paragraphs summarize these instructions.
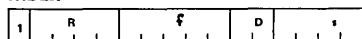
- Indexing Instructions - These instructions add or substract one from the addressed R- or S-Register. A carry link (LK) allows multi-byte indexing.

- Literal/Logical Instructions - These instructions perform logical operations on addressed R-Registers. These operations are OR (U), EXCLUSIVE OR (⊕), and AND (∩). Included in this category are two direct transfers (L→R and L→S) and two test instructions (L ⊕ R and L∩R). The test instructions set a condition register (C) and have no destination.

- Conditional Jump Instructions - These instructions execute a program jump to the address designated by L if a specified bit of the C-Register is 0 or 1. The C-Register bit is addressed by the n-field.

  Other jumps (unconditional) are done in the Index Instructions (L→R where R is P) and in the Arithmetic/Logical Instructions where D=0 specifies P.

- Arithmetic/Logical Instructions - These instructions are double-operand instructions where S- and R-Registers are added, subtracted, or logically combined. The results of the operation go to a register specified by the instruction D-field.

- Shift Instructions - These instructions perform a single-bit shift of the addressed R- or S-Register. In this group, 0,1, and Sign Fill are allowed. The Sign Fill permits multi-byte shifts by filling with the most recently "lost" shift bit.
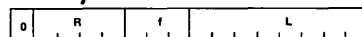
INDEX

| 1 | R | f | D | s |

(s) ──► Destination, Set C
(R) ──► Destination, Set C
(s) - 1 ──► Destination, Set C
(R) - 1 ──► Destination, Set C
(s) + 1 ──► Destination, Set C
(R) + 1 ──► Destination, Set C
(s) + SIGN + LK ──► Destination, Set C
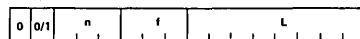(R) + SIGN + LK ──► Destination, Set C

See Note 1 to determine Destination.

LITERAL/LOGICAL
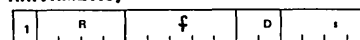
| 0 | R | f | L |

L ∪ (R) ──► R
L ──► R
L ⊕ (R) ──► R
L ∩ (R) ──► R
L ⊕ (R), SET C
L ∩ (R), SET C
L ──► s

CONDITIONAL JUMP

| 0 | 0/1 | n | f | L |

If BIT n of C = 0/1, L ──► P_L

ARITHMETIC/LOGICAL

| 1 | R | f | D | s |

(s) + (R) ──► Destination
(s) + (R) + LK ──► Destination
(s) + ($\overline{R}$) + 1 ──► Destination
(s) + ($\overline{R}$) + LK ──► Destination
(s) ∪ (R) ──► Destination
(s) ⊕ (R) ──► Destination
(s) ∩ (R) ──► Destination
($\overline{R}$) ──► Destination

SHIFT
⎡ Right Shift (R), Fill 1 ──► Destination, Set C
  Right Shift (R), Fill Sign ──► Destination, Set C
  Left Shift (R), Fill 0 ──► Destination, Set C
  Left Shift (R), Fill Sign ──► Destination, Set C
  Right Shift (s), Fill 1 ──► Destination, Set C
  Right Shift (s), Fill Sign ──► Destination, Set C
  Left Shift (s), Fill 0 ──► Destination, Set C
⎣ Left Shift (s), Fill Sign ──► Destination, Set C

See Note 1 to determine Destination.

Note 1: Determining Destination

If D = 0, Result ──► Pu, (A) ──► P_L
   = 1, s
   = 2, R
   = 3, s and R

Atron's 601 Support Engineering Staff offers design, manufacturing, programming, and maintenance assistance for systems using 601 Controller assemblies. Also available is the 601 Program Development Support System (PDSS) to aid the customer in initial program development.

The PDSS (Figure 1-1), a programming and support tool, is especially useful for program debugging in the actual Controller configuration and also functions as a hardware instruction assembler. It provides alterable, high-speed program memory for the ATRON 601, an inspect-and-change feature, an
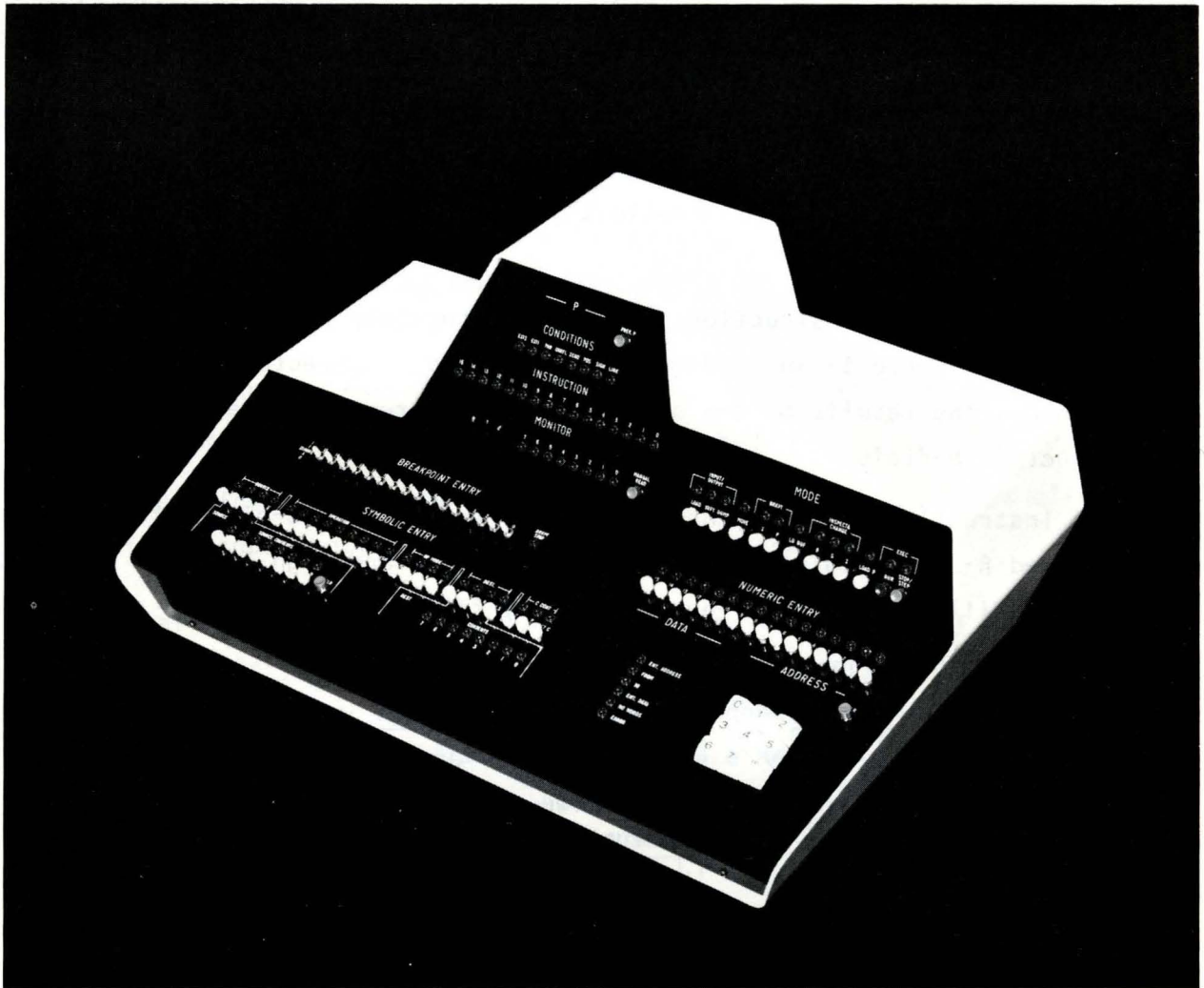
Figure 1-1. Program Development Support System (PDSS)

external peripheral interface for loading and dumping program memory, and instruction-step and break-point features with display of all program-addressable registers.

PHYSICAL DESCRIPTION

The following paragraphs briefly describe the basic components of the ATRON 601 Controller and their integration into a complete unit.

Printed-Circuit Board Assemblies

The standard ATRON 601 printed-circuit board measures 9.65 inches wide by 11 inches long by .062 inches thick. Shown in Figure 1-2, the conventional logic board for the 601 is designed for 64 dual-in-line packages of either 14 or 16 pins each. Voltage (+5 VDC) and ground are routed around the board via bus bars. As indicated in Figure 1-2, a total of 88 input/output pins are available -- 44 on the A connector and 44 on the B connector. All even numbered pins are on the solder side of the board and all odd numbered pins are on the component side of the board.

Back Panel Assembly

ATRON 601 Controllers are constructed using the "motherboard" technique on the back-panel or wire-wrap plate. In other words, the back panel is a printed-circuit board which, in addition to providing the necessary edge connectors for the 601 assemblies, also incorporates some printed-circuit connections. These eliminate a large percentage of the wire-wrapping normally required on a system composed of multiple printed-circuit boards.

The standard 12-card back panel is shown in Figure 1-3. Optional back panels are available which accept 6 or 18 standard printed-circuit boards. The Micro-Processor Assembly always occupies Position 100. Further expansion of either Program Memory or auxiliary modules can then be accomplished with the Micro-Processor still in Position 100, as in the 6- and 18-card version.

Connectors A and B of the back-panel assembly provide direct access to the Micro-Processor Assembly via the pre-routed back panel. These connectors, used by the Maintenance Console or the PDSS, are pin-for-pin identical with
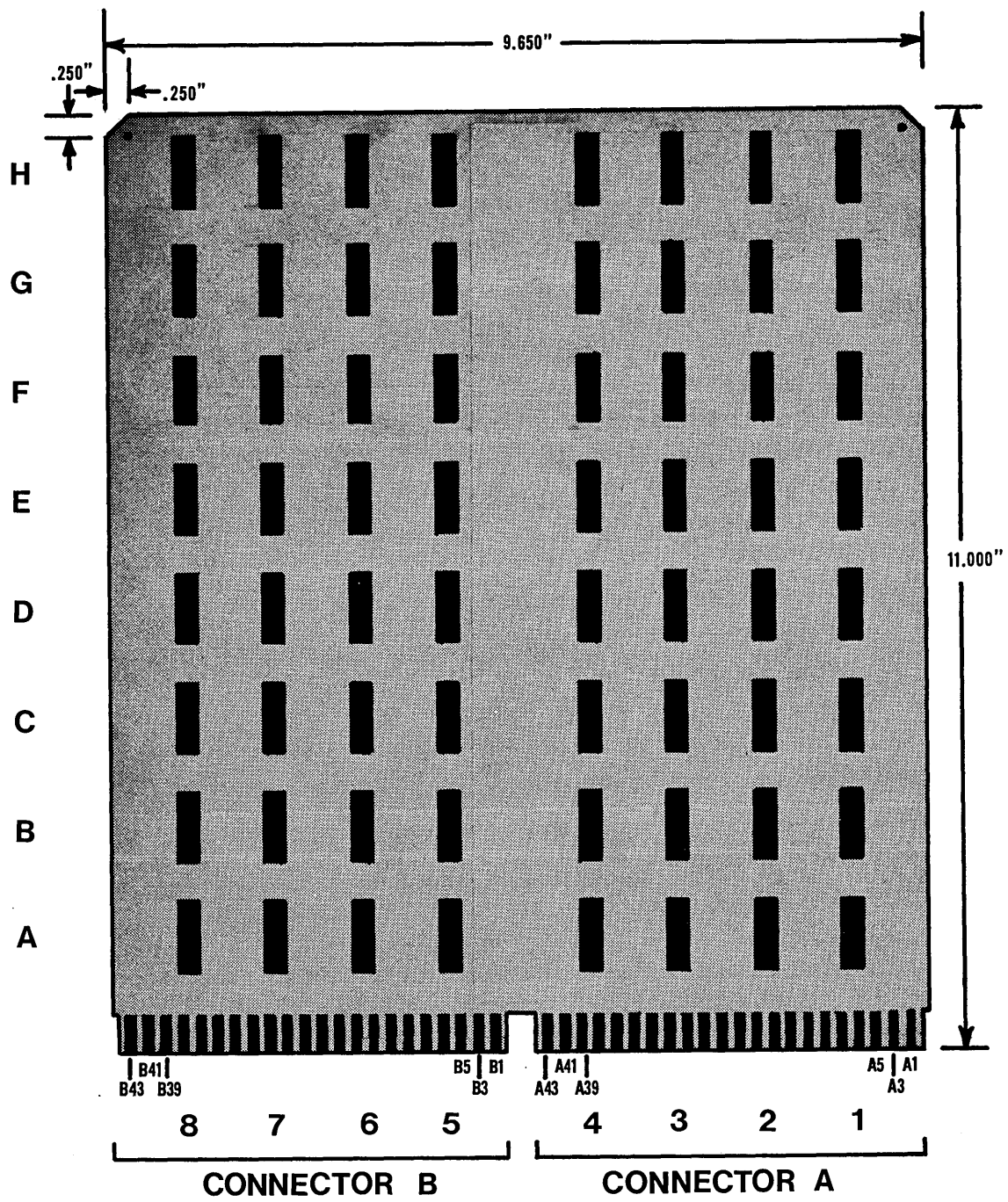
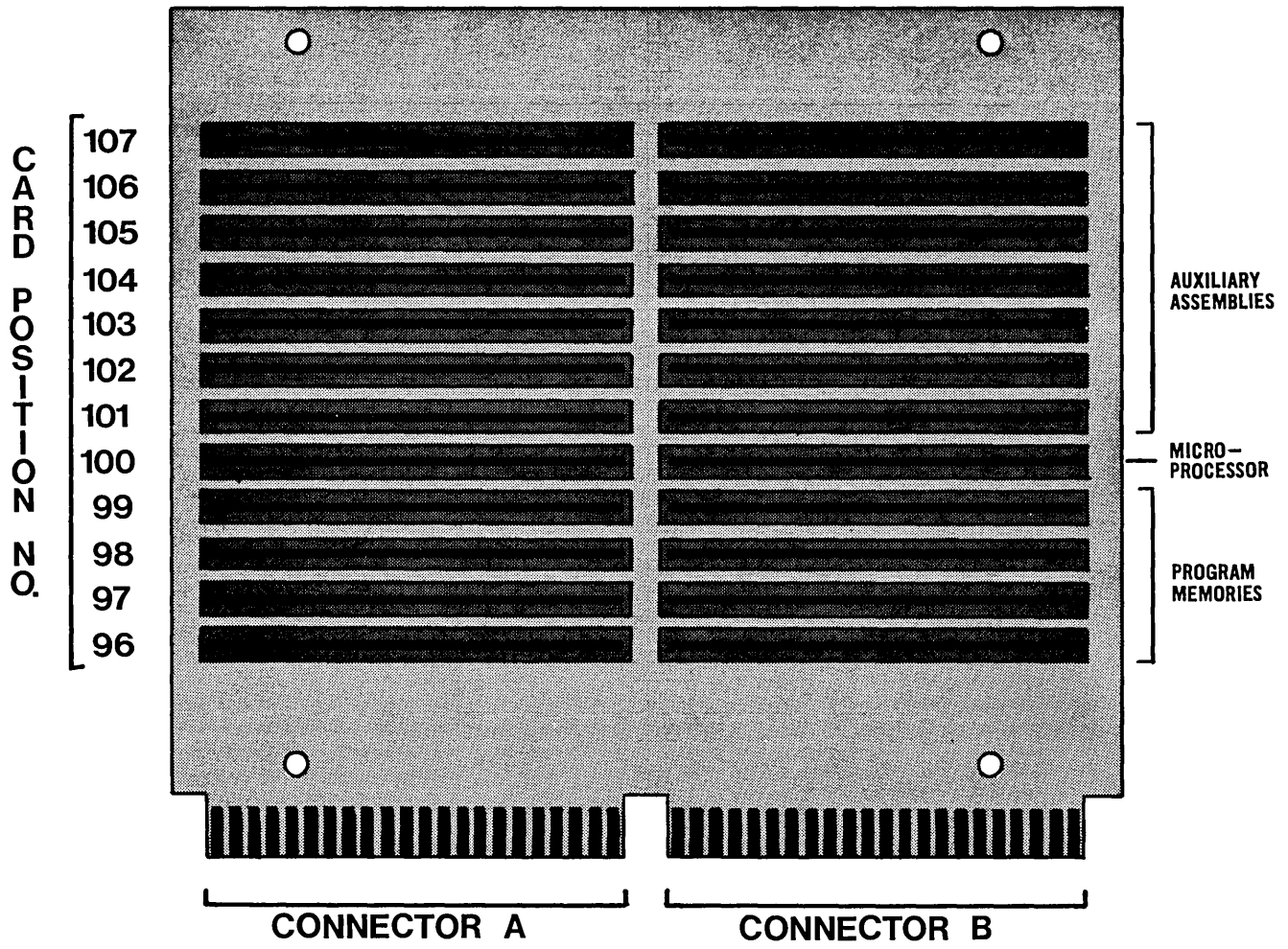Figure 1-2. Standard 601 Printed-Circuit Board

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Figure 1-3. ATRON 601 Back Panel Assembly

the Micro-Processor except that +5 VDC is not connected to pins B43 and B44.
This prevents overloading of the 601 power supply and requires that any
maintenance or programming device supply its own power. Since the back panel
is pre-routed, certain input/output pins are pre-assigned depending upon the
card slot to be used. Auxiliary assemblies utilizing unassigned input/output
pins receive the additional lines through conventionally wire-wrapped wires.

Interconnect Unit

The Interconnect Unit integrates and houses the printed-circuit board
assemblies and the back panel. The standard 12-card Interconnect Unit shown
in Figure 4 measures 12 inches high, $10\frac{1}{2}$ inches wide, and $6\frac{1}{2}$ inches deep.
Weighing 5 pounds, the framework of the Unit is constructed of aluminum and
the card guides of injected molded plastic. Optional Interconnect Units are
available which accept 6 or 18 standard printed-circuit boards.

Maintenance Panel

The Maintenance Panel allows the Maintenance Engineer to manually
execute 601 micro-instructions and monitor the results. Instruction step
and clock step functions are provided as well as a means for exercising
the Program Memory.

The 601 Maintenance Panel measures approximately 12-1/4" H X 10-1/2" W
X 10" D. It contains its own power supply and plugs directly into the 601
Interconnect Unit. See Figure 1-4.

Environmental Conditions

ATRON 601 Controllers operate in an ambient temperature of from 0° to
25°C and within a relative humidity range of 10% to 95% without condensation.
They can be stored at temperatures ranging from -65°C to $+150^{\circ}$C.

Power Requirements

The ATRON 601 requires 115 VAC (±10%) or optionally 230 VAC (±10%),
50 to 60 Hz., single-phase. The following chart indicates the current
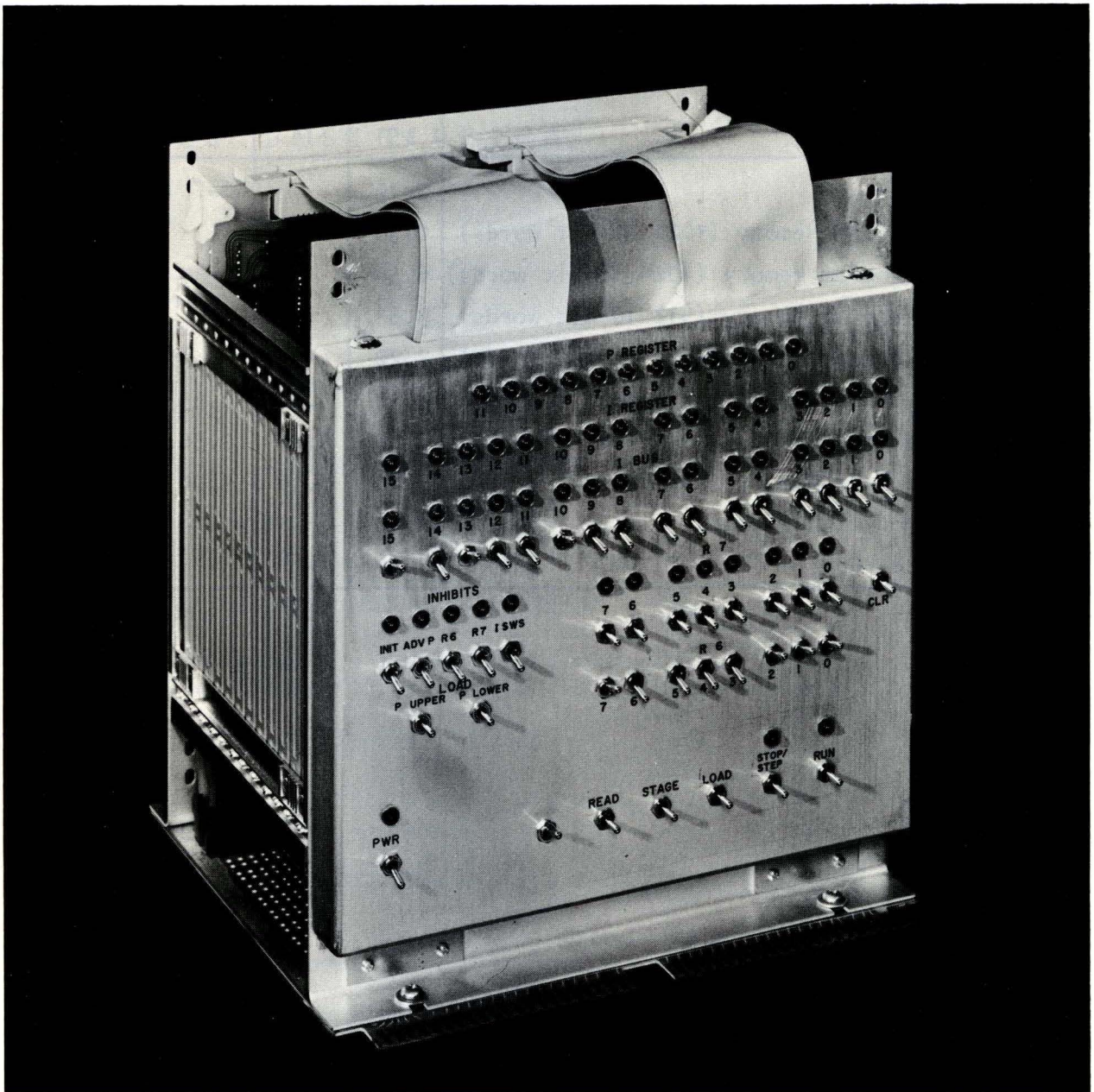requirements of the various assemblies.

Figure 1-4.   ATRON 601 Maintenance Panel

Current Requirements of 601 Assemblies

Assembly	Voltage				
	+5	+14	-5	-7	-10
Micro-Processor	2.10	-	-	-	-
Read-Only Program Memory (1024 16-bit words)	0.30	-	-	-	-
Read/Write Program Memory (1024 16-bit words)	6.50	-	-	-	-
Read/Write Program Memory (512 16-bit words)	3.63	-	-	-	-
Read/Write Program Memory (256 16-bit words)	2.20	-	-	-	-
Ferrite Core Main Memory (4K bytes)	3.30	3.70	0.25	-	-
Ferrite Core Main Memory (8K bytes)	5.60	5.60	0.50	-	-
Ferrite Core Main Memory (16K bytes)	7.00	8.40	1.00	-	-
MOS Main Memory (1024 bytes)	1.40	-	-	.480	.440
Priority Interrupt	1.50	-	-	-	-

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ATRON 601 CONTROLLERS

ASSEMBLY DESCRIPTION

INTRODUCTION

A typical ATRON 601 Controller consists of a Micro-Processor Assembly, one or more Read-Only Program Memories, an appropriate Interface Adaptor Assembly, and may include a Core or Semiconductor Main Memory as needed. These, however, do not limit system configurations. A Priority Interrupt Assembly, additional I/O interface assemblies, or special arithmetic modules may be attached to match the Controller to the application. These are directly addressed by the Micro-Processor on a bus interface as shown below.
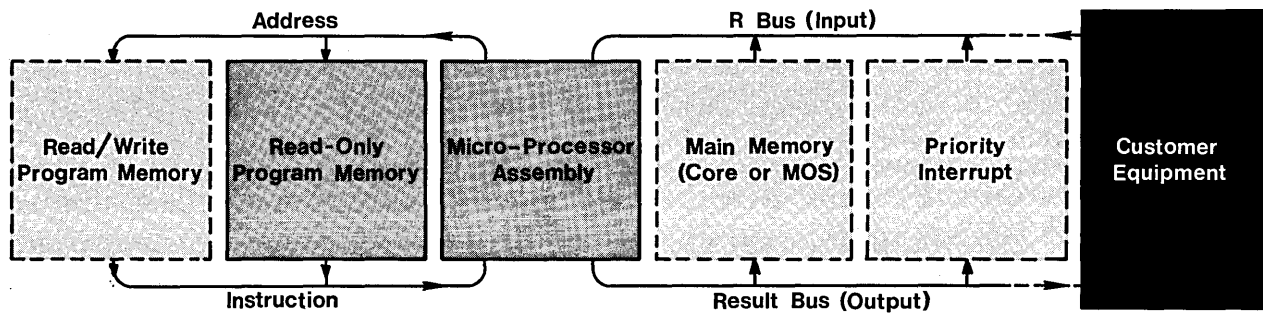
711HM101-2

Address | R Bus (Input)

| Read/Write Program Memory | Read-Only Program Memory | Micro-Processor Assembly | Main Memory (Core or MOS) | Priority Interrupt | Customer Equipment |

Instruction | Result Bus (Output)

Each assembly (with the exception of Core Memory) is on a single 9.65 inch by 11 inch printed-circuit board. These are integrated and housed by the Interconnect Unit described in the General Description. The purpose of this section is to summarize the characteristics of these assemblies.

MICRO-PROCESSOR ASSEMBLY (0601-00)

Highlights

The Micro-Processor Assembly, shown in Figure 2-1, can execute an instruction in 260 nanoseconds (Jumps: 520 nanoseconds), contains a 16-byte internal scratch pad memory, a variable clock, and directly addresses external units on a bus interface. It is capable of addressing 4096 words of Program Memory. The block diagram of the Micro-Processor shown below is described in the following paragraphs.

Instruction Section

Instruction (I) Register   The I-Register holds each micro-instruction during execution. The least significant bits supply literal (immediate) operands for literal-class instructions.

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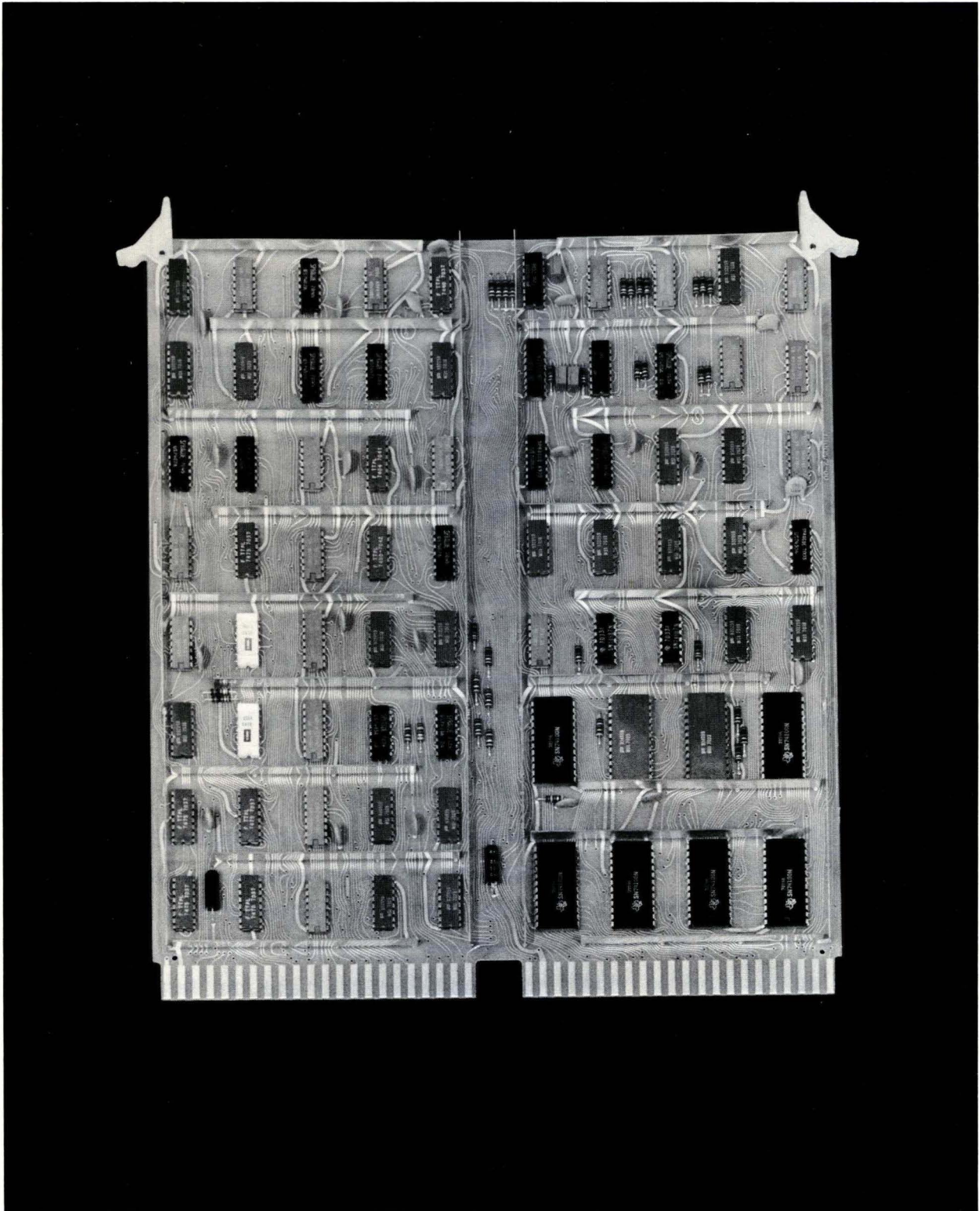
Figure 2-1.   ATRON 601 Micro-Processor Assembly

711HM101-2
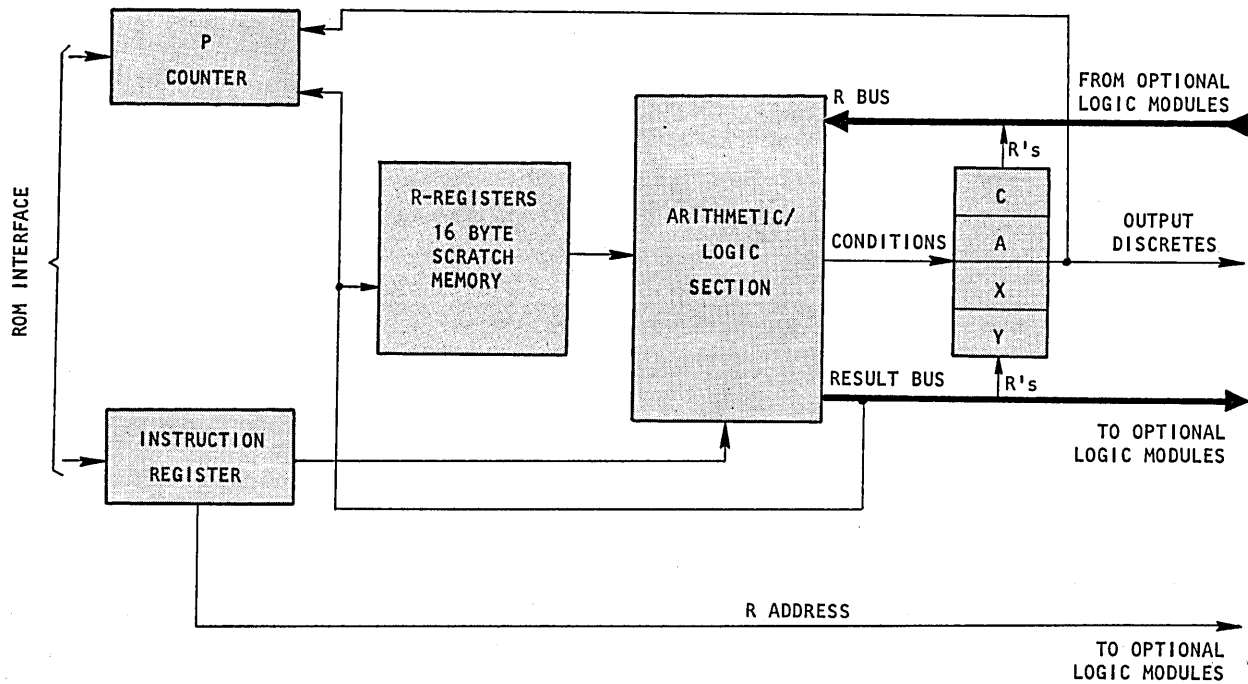
P-Counter

The P-Counter holds the address of a micro-instruction during instruction access. Before each instruction access, the P-Counter is incremented by one. It receives inputs from the A-Register and the Result Bus when P is specified as a destination. In that case, instruction execution time is extended to 520 nanoseconds.

Arithmetic/Logic Section

This section contains the circuitry for implementing logical and arithmetic operations on operands secured from the Scratch Memory (S-Registers), I-Register (literals), and/or R-Bus. Registers for staging the operands and

condition bits from the C-Register are provided. The results of the arithmetic/logical operations appear on the Result Bus.

R-Registers

These registers are the semi-dedicated storage elements of a 601 Controller. Four are included on the Micro-Processor Assembly (A, C, X, and Y) and have specific functions in the Processor. R-Registers are addressed by the R-field of micro-instructions. The following table specifies the binary names of the R-Registers:

R-Register	Binary Name
A	0000
C	0001
X	0010
Y	0011
P_U	0100
P_L	0101
External R's	0110-1111

The functions of the R-Registers on the Micro-Processor Assembly are described in the following paragraphs.

A-Register (R=0)   This is a general-purpose register which can be referenced both as a source and as a destination. As a secondary function, it provides the lower 8 bits during a jump where D equals 0. (Refer to Instruction Repertoire.)

C-Register (R=1)   The C-Register is the condition register and is used to detect conditions arising within the processor during the execution of certain instructions. In addition, it contains bits which indicate the occurrence of certain external events. Table 2-1 defines the location and meaning of the C-Register bits.

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Table 2-1. Definitions of C-Register Bits

C-Register Bit	Name and Meaning
0	*LINK (LK)* - This bit is set by a carry-out of the adder from a previous arithmetic operation.
1	*SIGN* - The SIGN bit remembers the sign of one of the operands of a previous arithmetic operation.
2	*POSITIVE (POS)* - The POSITIVE bit is set when the result of an arithmetic or logical operation is positive.
3	*ZERO* - The ZERO bit is set when a result appearing on the Result Bus is zero.
4	*OVERFLOW (OVRFLW)* - The OVERFLOW bit is set when an arithmetic operation is performed which may have generated an arithmetic overflow condition.
5	*PARITY ERROR (PAR)* - This bit is set if the R-Register selected to the R-Bus appears to have erroneous parity.
6,7	*EXTERNAL CONDITION (EXT 1, EXT 2)* - The EXTERNAL CONDITION bits are generated by logic outside of the Micro-Processor Assembly. Their meaning is determined by the nature of their source.

X-Register (R=2)	This is a general-purpose register which can be referenced both as a Source and as a Destination. The bits of this register may be used as Output Discrete Bits controlling other 601 Controller assemblies.
Y-Register (R=3)	This is a general-purpose register which may also be referenced both as a Source and as a Destination. As a secondary function, it may be used as a Output Discrete Register controlling other 601 Controller assemblies.
P_U-Register (R=4)	These are the most significant 4 bits of the P-Counter. This register can only be referenced as a destination.
P_L-Register (R=5)	These are the least significant 8 bits of the P-Counter and can only be referenced as a destination.
External R-Registers (R=6 to 15)	These R-Registers are external to the Micro-Processor Assembly. Located in the various assemblies attached to the 601 Controller, these registers comprise the remainder of the processing system. As such, they are referenced as sources and/or destinations depending on function.

External Interfaces

Communication with auxiliary assemblies is accomplished by the transfer of information between the Micro-Processor and the R-Registers located in the auxiliary assemblies. Processor instructions include R-Register identification (R-Address) and may request them to source and/or sink data. Communication with R-Registers is under Micro-Processor control and transfers are timed with the Processor clock. The number of R-Registers located in an auxiliary assembly is dependent on the function of the particular module.

The following paragraphs describe the input/output signals transferred between the Micro-Processor and the auxiliary assemblies.

Result Bus (output)	The Result Bus is the primary path by which the Processor transmits information to auxiliary assemblies. These lines carry the information which is to be loaded into auxiliary assembly R-Registers.
R-Bus (input)	The R-Bus is the primary path by which information is transmitted from auxiliary assemblies to the Processor. The contents of a given R-Register is held on the R-Bus as soon and as long as the R-Address Bus identifies that register. A line for a parity bit is included in the R-Bus. Parity may be tested at the option of the programmer.
Sink Line (output)	The Processor raises the sink line to a high level during instructions which require any R-Register to sink data.
Phase D (output)	Phase D is a timing pulse used to clock data into an R-Register.
Phase B (output)	This signal has no assigned function in auxiliary assemblies, but is available under- lapping Phase D.
R-Address Bus	The Processor transmits R-Register identi- fication via the R-Address Bus. The R- Register identified may act as a data source and/or sink during the execution of a given Processor instruction. A given R-Register is gated onto the R-Bus continuously while its address is present on the R-Address Bus.

X-Bus and Y-Bus (output)	The X-Bus and Y-Bus transmit the data contained in the Micro-Processor X- and Y-Registers to auxiliary assemblies. There is no pre-assigned function for the X and Y bits.
C-Lines (input)	The C-Lines transmit two bits of data from auxiliary assemblies to Bits 6 and 7 (EXTERNAL CONDITION) of the Micro-Processor C-Register. There is no pre-assigned function for these two bits.

Timing

The timing of the primary auxiliary interface signals is shown in Figure 2-2. The minimum cycle time is 260 nanoseconds, but can be adjusted to accommodate slower assemblies. X denotes the amount of time which is added to the cycle time to achieve Result Bus stability earlier with respect to Phase D. Y denotes the amount of time which is added to the cycle time to allow for additional delay in achieving R-Bus stability.

TRANSFORMER READ-ONLY PROGRAM MEMORY (0602-20)

Highlights

The Micro-Processor Assembly receives its instruction from the program memory module(s). The Micro-Processor specifies an instruction location (address) and assembly number and requests an instruction from the program memory. The appropriate Program Memory Assembly responds by transmitting the instruction located at the specified address to the Micro-Processor. Read-Only Program Memories are ideally suited to Controllers since the microprogram normally remains the same over a period of time.

The ATRON 0602-20 Read-Only Memory (ROM) as shown in Figure 2-3 is a totally self-contained random access, non-destructive read-out memory. Each ROM Assembly can contain up to 1024 16-bit words. However, since the memory is of the braid (rope) type, any smaller number of words may be strung and additional words added at a later date. The memory operates with an access time of 130 nanoseconds and a minimum cycle time of 260 nanoseconds.
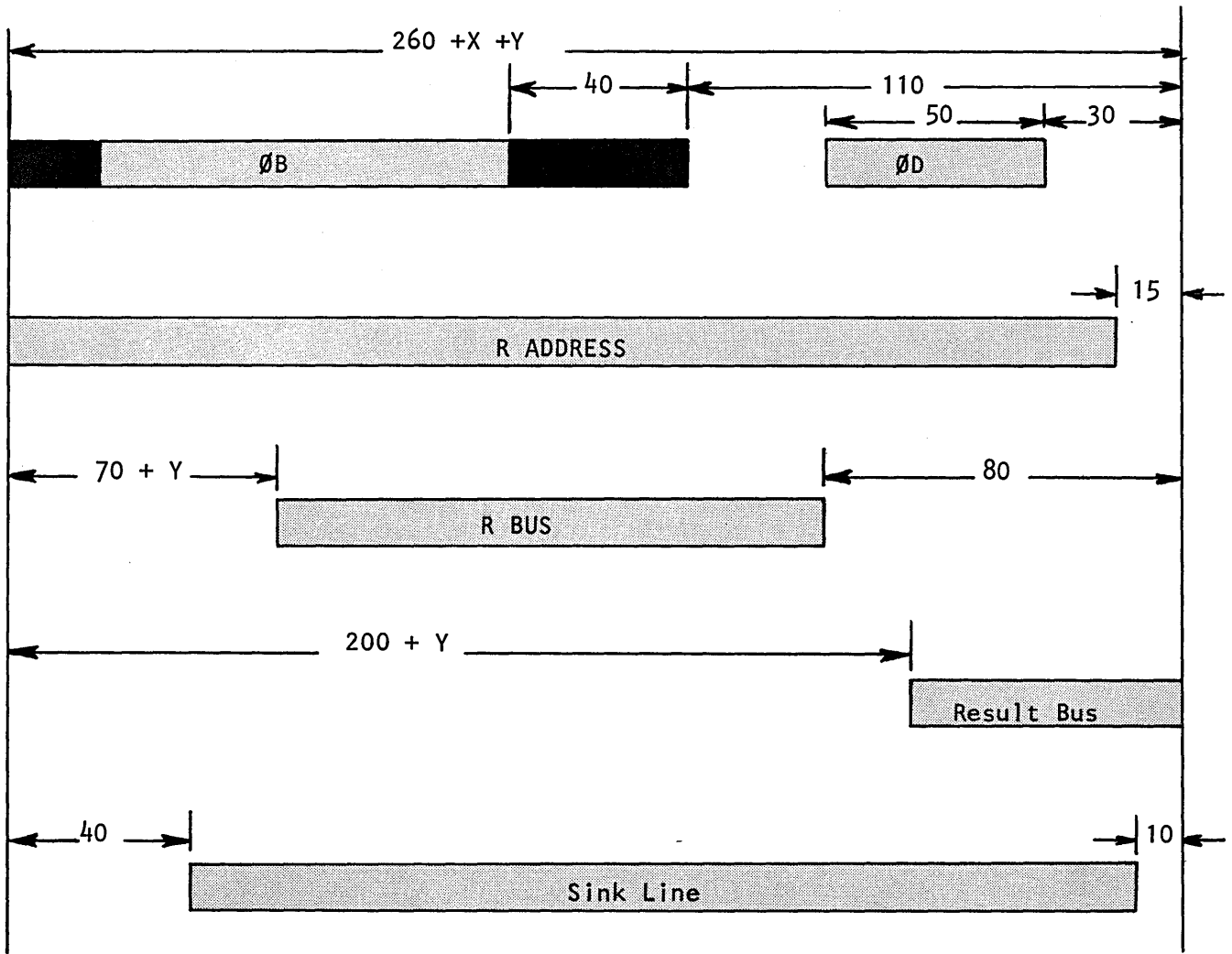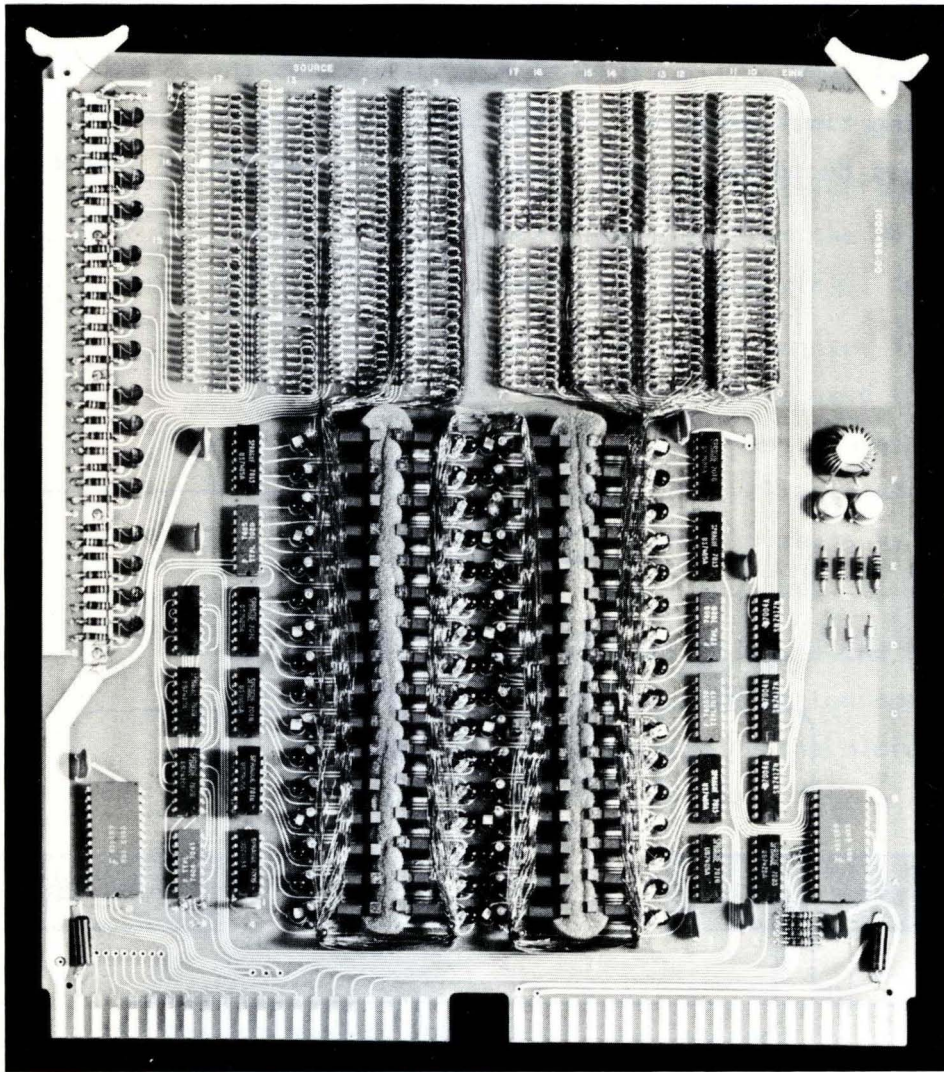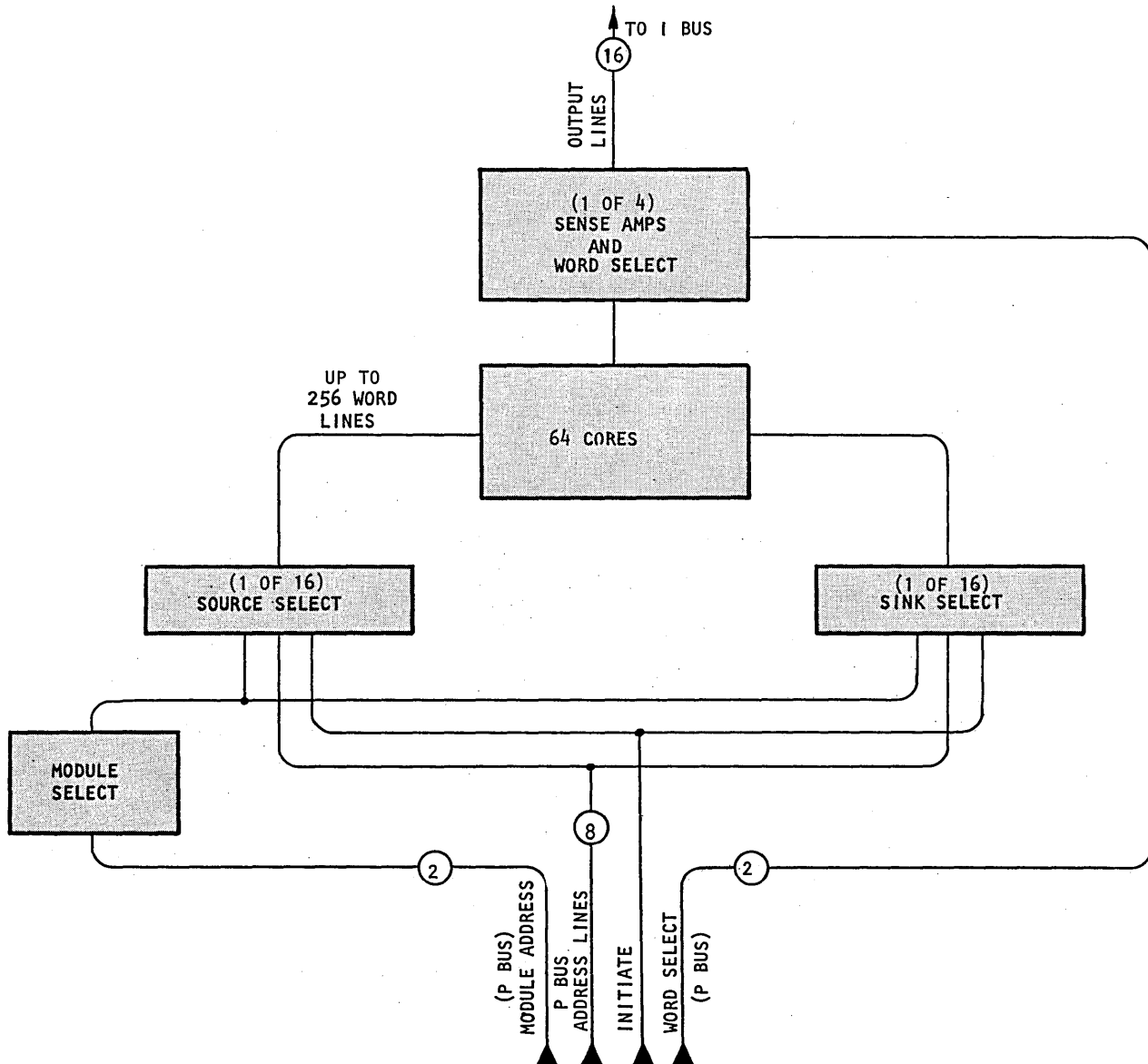
711HM101-2

Figure 2-2. Interface Timing

Figure 2-3.   601 Read-Only Program Memory

Ten address lines, 2 module enable lines, and one instruction (Program Memory Initiate) line are required to randomly access the assembly as shown in the following block diagram. Up to four assemblies may be stacked. Complete address decoding is performed in the Program Memory Assembly.

Block Diagram

Each ROM Assembly contains a Program Memory Interface. Ten Address lines, two Module Enable lines, and one Initiate line are required to randomly access a ROM Assembly. Four Module Enable inputs are provided to the ROM, however, to allow use of more than one module. The Input/Output lines are described in the following paragraphs.

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I Bus	The I Bus is the path by which instructions are transmitted from the Program Memory Assembly(s) to the Micro-Processor. (input)
P Bus	The P Bus is the path by which address information is transmitted from the Micro-Processor to Program Memory Assembly(s). (output)
P_{10}, P_{11}	Bits 10 and 11 of the P Counter (see Micro-Processor description) are used to enable Program Memory Assemblies. Both true and complement lines are available enabling assignment of assembly numbers by appropriate back panel wiring. (output)
Initiate	The Initiate signal requests the Program Memory to gate the information located at the address specified by the Micro-Processor onto the I Bus. (output)

READ/WRITE PROGRAM MEMORY (0604-XX)

Highlights

The Read/Write Program Memory (Figure 2-4) is intended for use primarily in ATRON 601 program development. It includes features which allow loading and dumping of programs. Operating at ROM speed, programs in the Read/Write Memory can be checked on-line on a real-time basis. It is available in the following capacities:

- 256 16-bit words (0604-00)
- 512 16-bit words (0604-10)
- 1024 16-bit words (0604-20)

Block Diagram

The Read/Write Program Memory contains two interfaces -- a Program Memory Interface identical to the ROM interface and an Auxiliary Interface.
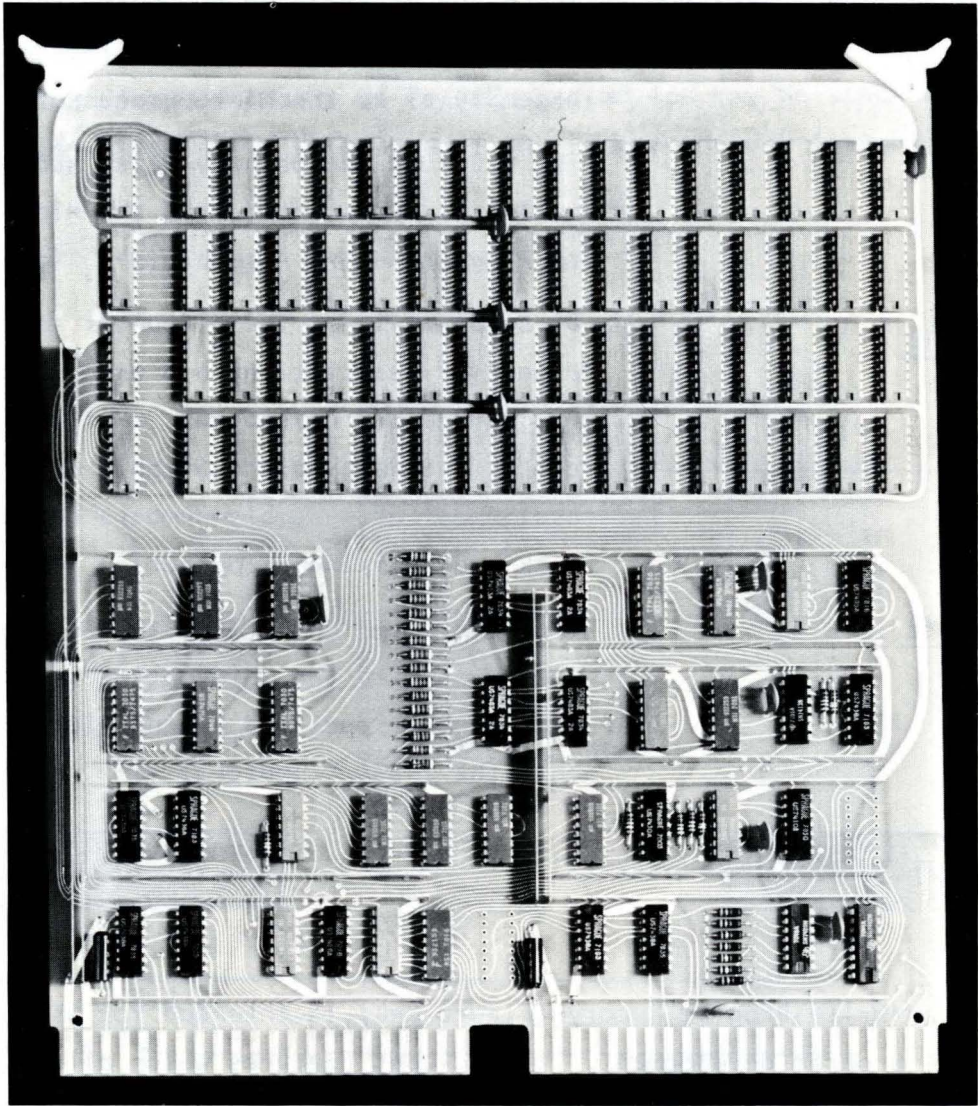
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Figure 2-4. Read/Write Program Memory
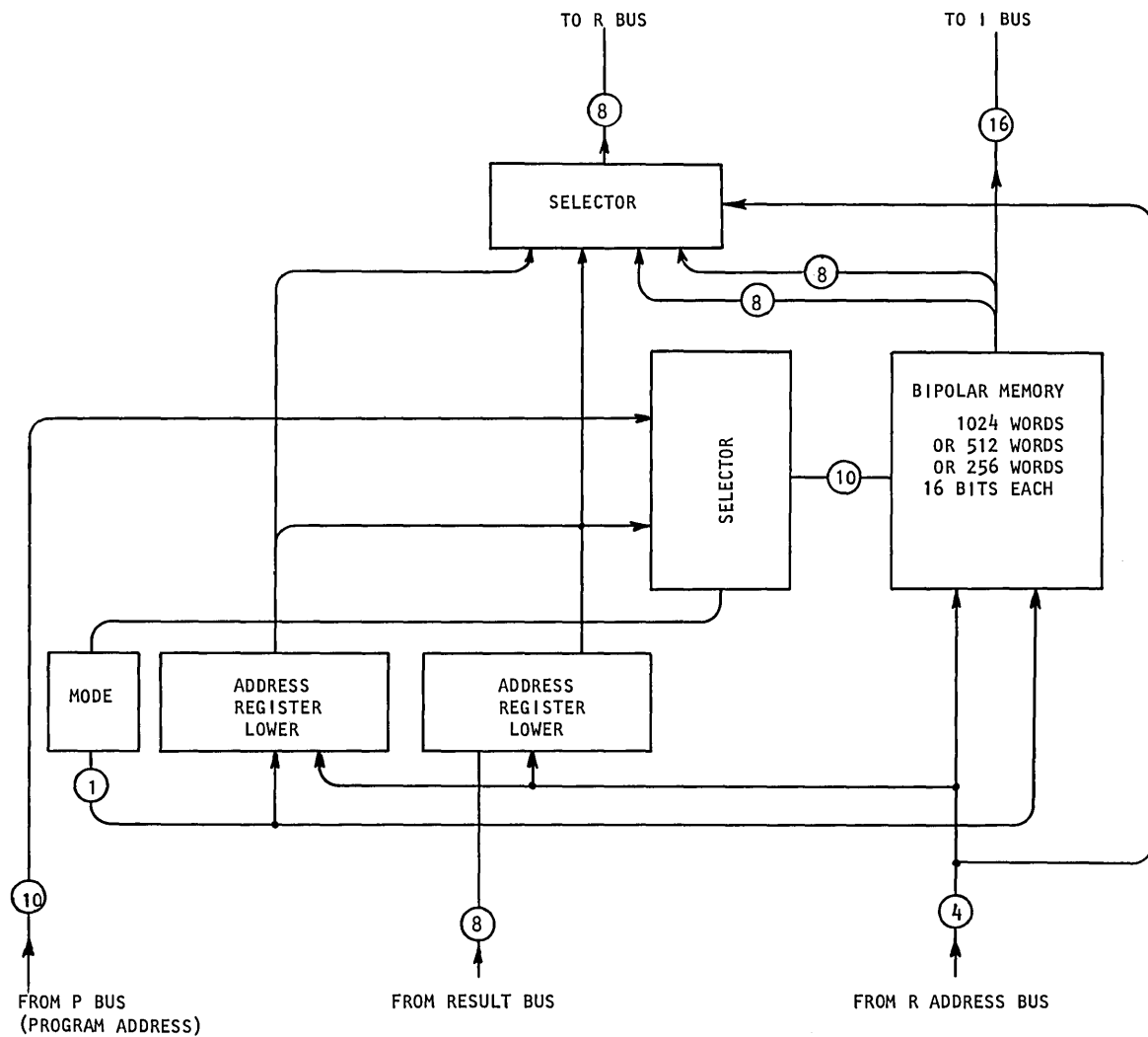
The Program Memory Interface allows the assembly to be used in place of a Read-Only Memory for the following purposes.

- Alterable memory for program development. As such, it would normally be associated with the Program Development Support System (PDSS).

- To gain economy when a user has many independent programs to run. The user may load each program from a peripheral device such as a card reader into one Read/Write Memory instead of purchasing a ROM for each program.

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The Auxiliary Interface is used to load and dump programs. Loading and dumping of programs requires a Read-Only Memory programmed to load and dump the Read/Write Program Memory using the appropriate peripheral devices. When developing programs, the PDSS will contain the appropriate programs as well as the peripheral device.

The Auxiliary Interface also allows the memory to be used as an auxiliary memory for data storage. However, the MOS and Core Main Memory Assemblies are advantageous when large capacities are required.

FERRITE CORE MAIN MEMORY (0603-00)

Highlights

The Read/Write Core Memory available with ATRON 601 Controllers is expandable from 4K bytes to 16K bytes (see Figure 2-5). This is the only assembly requiring more than one printed-circuit board and they are as follows:
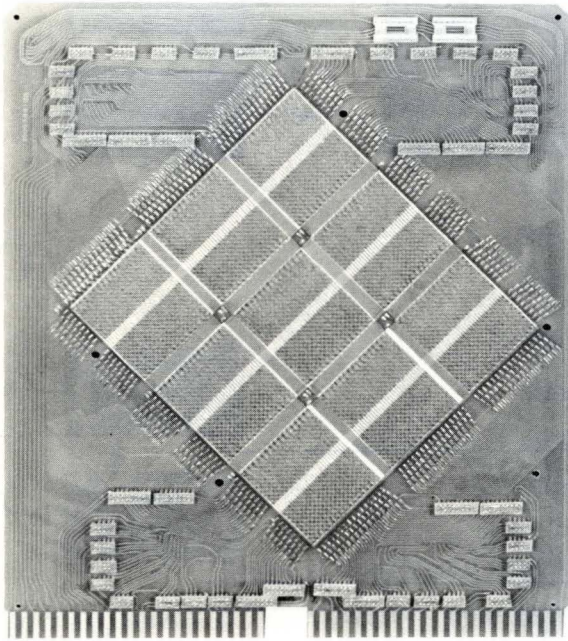
- Ferrite Core Plane
- Sense Inhibit
- X-Y Driver
- Interface

Core Memory operates with an access time of 600 nanoseconds and a cycle time of 1 microsecond. Parity is optional.

Block Diagram

Communication with the auxiliary Core Memory is accomplished by the transfer of information between the Micro-Processor and four registers located in the Core Memory Interface Assembly. Processor instructions include register address identification and specify whether the register will be a source or a destination. Communication with the registers is under Micro-Processor control, and transfer of address and data are timed by the Processor clock.

The following paragraphs describe the input/output lines between the Micro-Processor and Core Memory Interface.

Ferrite Core Plane
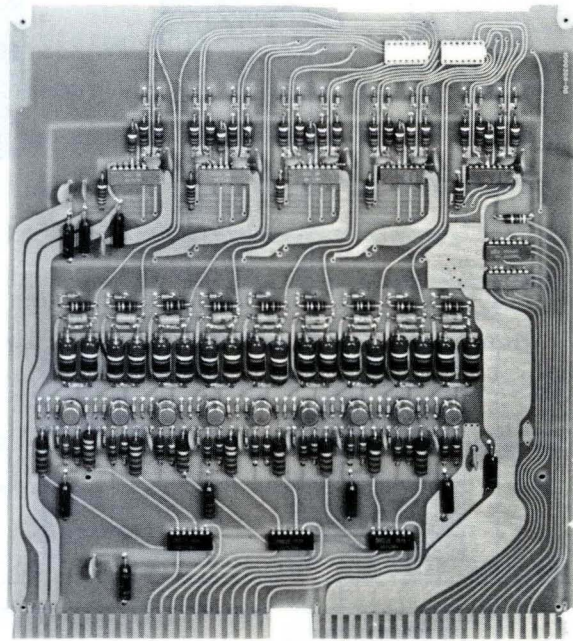
Sense Inhibit

X-Y Driver

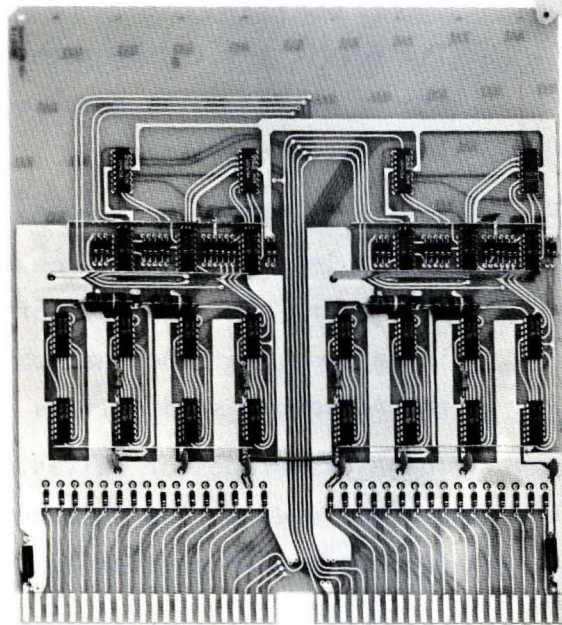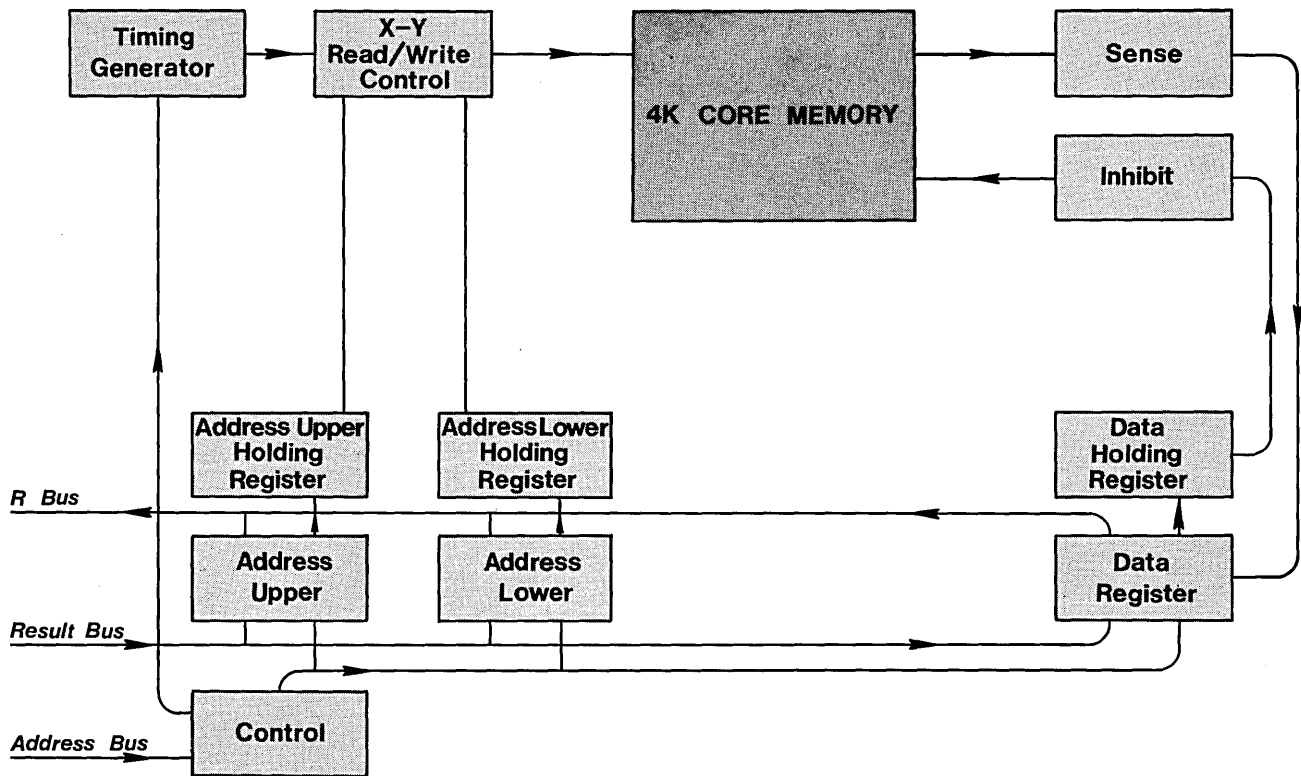Figure 2-5. Core Memory Assemblies

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Timing Generator → **X-Y Read/Write Control** → **4K CORE MEMORY** → **Sense**

Inhibit

Address Upper Holding Register   **Address Lower Holding Register**   **Data Holding Register**

R Bus

Address Upper   **Address Lower**   **Data Register**

Result Bus

Address Bus → **Control**

Result Bus (output)

The Result Bus is the path by which the Processor transmits data to the Core Memory Interface R-Registers.

R-Bus (input)

The R-Bus is the primary path by which information is transferred from Core Memory to the Processor. The contents of a given R-Register is held on the R-Bus as soon and as long as the Address Bus identifies that register.

Sink Line (output)

The Micro-Processor raises the sink line to a high level during instructions that reference any R-Register as a destination.

Phase D (output)

Phase D is a timing pulse used to clock data into an R-Register.

<u>Register Address Bus</u> <u>(output)</u>	The Processor sends R-Register Address identification to the Core Memory Interface via the Register Address Bus. The R-Register identified may act as a data source and/or destination during the execution of a given Processor instruction. A given R-Register is gated onto the R-Bus continuously while its address is present on the Register Address Bus.
<u>X- and Y-Bus</u>	The X- and Y-Bus from the Micro-Processor are available to the Core Memory Interface by backpanel wire-wrapping and can be used in the extension of the R-Address.

The Core Memory Interface contains four registers which sink or source data by means of the Result Bus (sink data) and the R-Bus (source data). Those four registers are described in the following paragraphs.

<u>MEMORY ADDRESS REGISTER</u> <u>LOWER (MARL)</u>	The MARL contains the lower eight bits of the memory address.
<u>MEMORY ADDRESS REGISTER</u> <u>UPPER (MARU)</u>	The MARU contains the upper six bits of the Core Memory address. Both the MARL and the MARU are double-rank type registers with the lower rank handled as an R-Register. The upper rank is loaded upon memory cycle initiation. Both are referenced by the Processor from the lower rank only.
<u>MEMORY DATA REGISTER (MDR)</u>	The MDR contains the core data plus parity. The MDR is a double-rank type register with data coming into and out of the lower rank. Data coming in is double-ranked and the data clocked into the second rank by the memory cycle initiation. Data coming out is clocked into the lower rank at the access time of the memory.

<u>MEMORY CONTROL REGISTER</u>
<u>(MCR)</u>

The MCR contains information determining the mode in which the memory will operate.

- Memory Initiate
- Read/Write
- Auto Initiate on loading MDR
- Auto Initiate on loading MARU
- Auto Initiate on loading MARL
- Split
- Clear

A single-rank type register, the MCR cannot be changed during a memory cycle, but can be read.

MOS MAIN MEMORY (0603-60)

Highlights

Contained on a single board, the Read/Write MOS Main Memory provides up to 1024 bytes. The assembly operates with an access time of 1.5 microseconds and a cycle time of 1.5 microseconds. See Figure 2-6.

Block Diagram

Communication with the auxiliary MOS Memory is accomplished by the transfer of information between the Micro-Processor and four registers located in the MOS Memory Interface Assembly. Processor instructions include register address identification and specify whether the register will be a source or a destination. Communication with the registers is under Micro-Processor control, and transfer of address and data are timed by the Processor clock.

The following paragraphs describe the input/output lines between the Micro-Processor and MOS Memory Interface.

<u>Result Bus (output)</u>

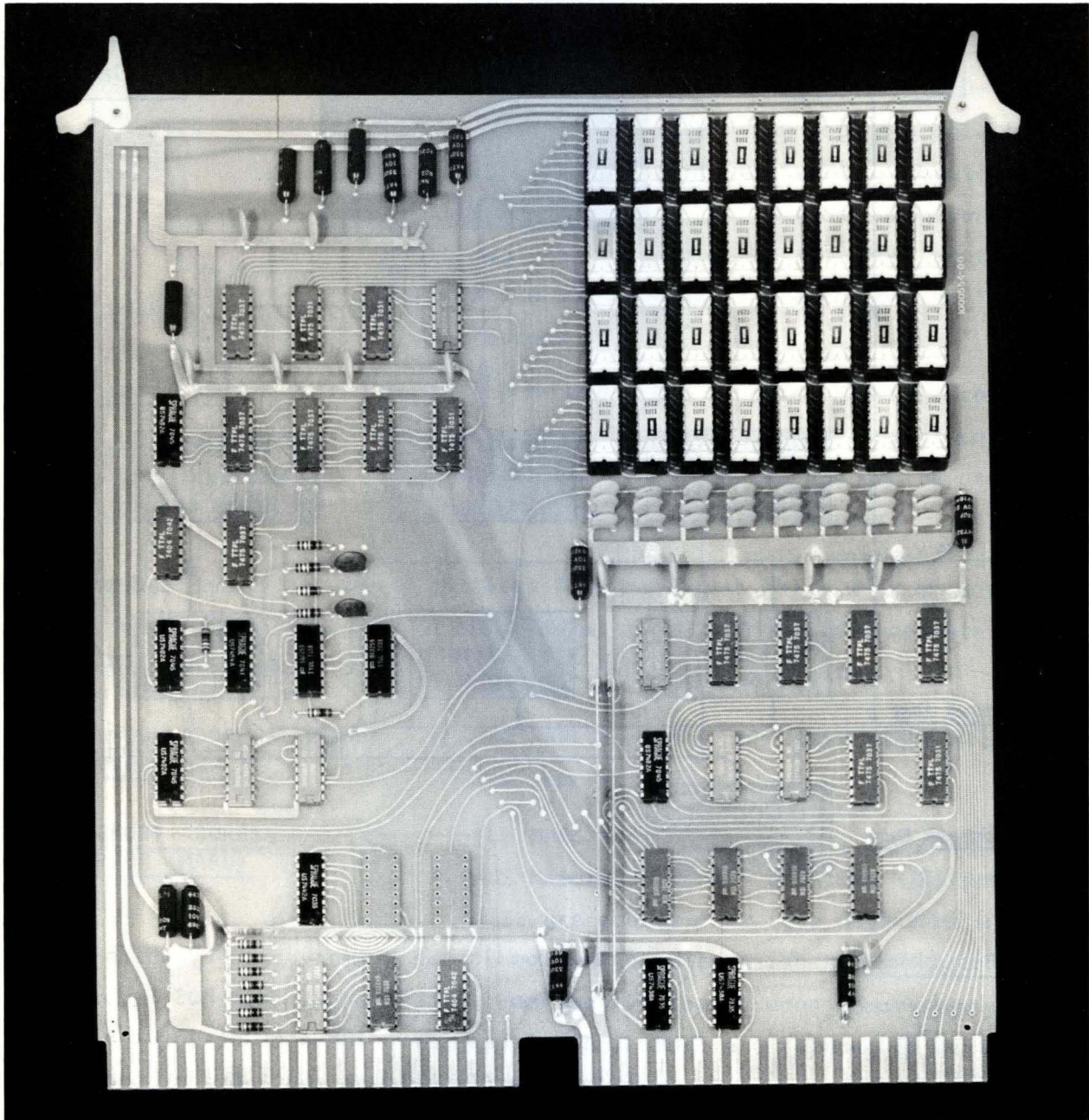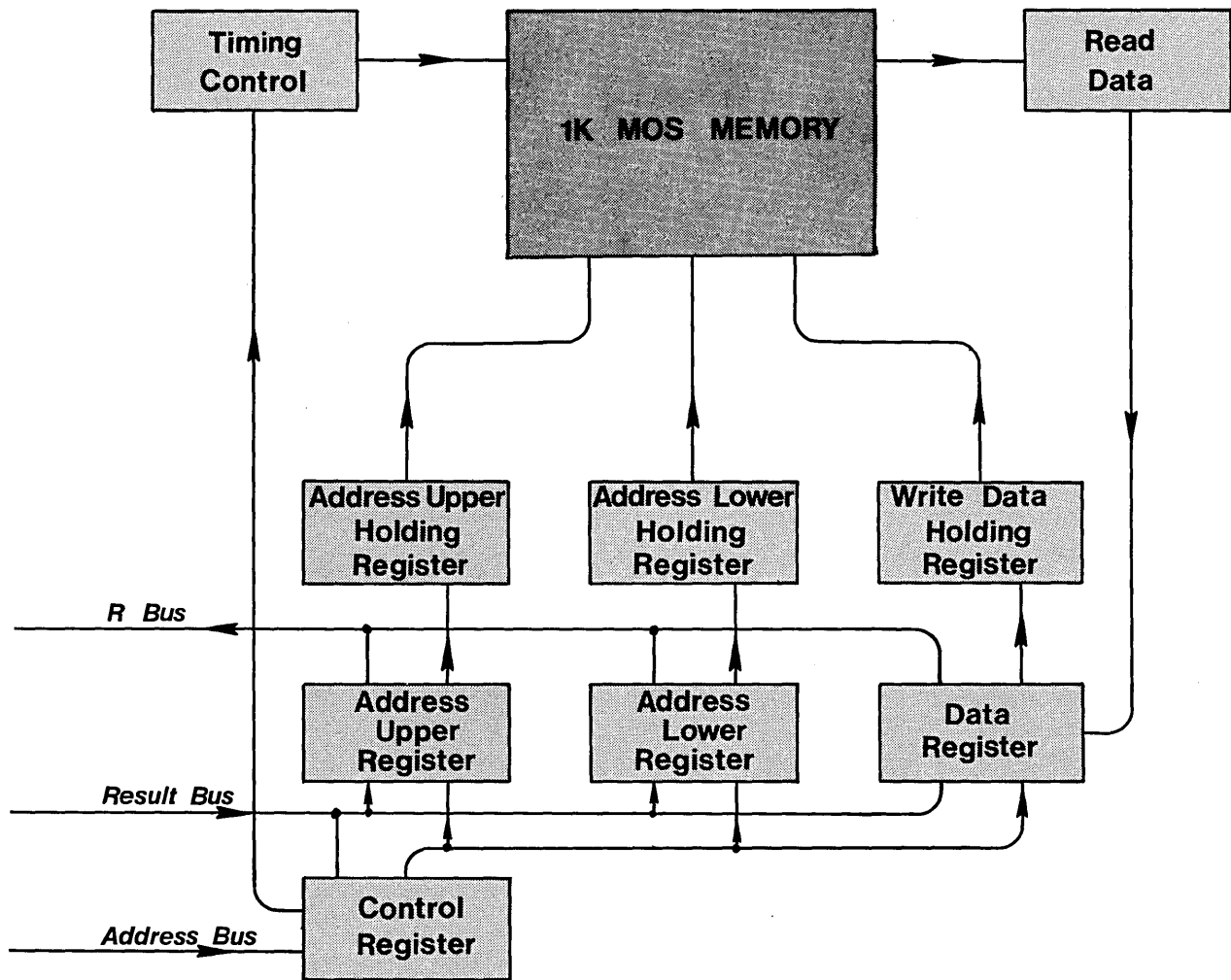The Result Bus is the path by which the Processor transmits data to the MOS Memory Interface R-Registers.

Figure 2-6. MOS Main Memory

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R-Bus (input)

The R-Bus is the primary path by which in-
formation is transferred from MOS Memory
to the Processor. The contents of a given
R-Register is held on the R-Bus as soon and
as long as the Address Bus identifies that
register.

Sink Line (output)

The Micro-Processor raises the sink line to
a high level during instructions that
reference any R-Register as a destination.

Phase D (output)

Phase D is a timing pulse used to clock
data into an R-Register.

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Register Address Bus (output)	The Processor sends R-Register Address identification to the MOS Memory Interface via the Register Address Bus. The R-Register identified may act as a data source and/or destination during the execution of a given Processor instruction. A given R-Register is gated onto the R-Bus continuously while its address is present on the Register Address Bus.
X- and Y-Bus	The X- and Y-Bus from the Micro-Processor are available to the MOS Memory Interface by backpanel wire-wrapping and can be used in the extension of the R-Address.

The MOS Memory Interface contains four registers which sink or source data by means of the Result Bus (sink data) and the R-Bus (source data). Those four registers are described in the following paragraphs.

MEMORY ADDRESS REGISTER LOWER (MARL)	The MARL contains the lower eight bits of the memory address.
MEMORY ADDRESS REGISTER UPPER (MARU)	The MARU contains the upper six bits of the − MOS Memory address. Both the MARL and the MARU are double-rank type registers with the lower rank handled as an R-Register. The upper rank is loaded upon memory cycle initiation. Both are referenced by the Processor from the lower rank only.
MEMORY DATA REGISTER (MDR)	The MDR contains the MOS data plus parity. The MDR is a double-rank type register with data coming into and out of the lower rank. Data coming in is double-ranked and the data clocked into the second rank by the memory cycle initiation. Data coming out is clocked into the lower rank at the access time of the memory.

MEMORY CONTROL REGISTER
(MCR)

The MCR contains information determining the mode in which the memory will operate.

- Memory Initiate
- Read/Write
- Auto Initiate on loading MDR
- Auto Initiate on loading MARU
- Auto Initiate on loading MARL

A single-rank type register, the MCR cannot be changed during a memory cycle, but can be read.

PRIORITY INTERRUPT ASSEMBLY (0608-00)

Highlights

Mounted on a single printed-circuit board, the Priority Interrupt Assembly provides the following functions:

- Provides an interface to the 601 Micro-Processor from up to 31 interrupt lines from external assemblies. Since there is no storage for interrupt requests on the Interrupt Assembly, these lines are stored within the source modules.

- Selects the interrupt request of highest priority of the 31. Priority is on a position-encoded basis.

- Provides flip-flops for the selective enabling or disabling of each line.

- Provides a Master Enable/Disable flip-flop by which all 31 interrupt requests may be enabled or disabled.

- Provides a Lockout flip-flop independent of the Master Enable or Disable line. This is set when an interrupt occurs and remains set until receiving a clear command from the Micro-Processor.

- Captures the value of the Program Address Counter from the Micro-Processor when an interrupt occurs. This value is the address of the interrupt and consequently is the normal return address upon exit from the interrupt routine.

Highlights

The PDSS is a programming and maintenance tool (Figure 2-7) which can be attached to the 601 Controller. When connected, it provides

- alterable, high-speed program memory for the ATRON 601

- an inspect-and-change feature for altering this program memory

- an external peripheral interface to facilitate loading and dumping the program memory before and/or after alteration

- instruction-step and break-point features with display of all program-addressable registers

- and a maintenance facility for locating hardware faults.

The PDSS is especially useful for full-speed program debugging before the Read Only Memory is programmed. The PDSS also functions as a hardware instruction assembler. The PDSS consists of six subsystems configured as shown below. The following paragraphs describe those subsystems.

PDSS Controller

The PDSS Controller subsystem is actually an ATRON 601 and interfaces with other subsystems through a network of addressed R-Registers (to be distinguished from those R-Registers of the monitored Controller). These R-Registers are located in the various subsystems and their assignments are therefore fixed. The PDSS Controller controls all activity in the PDSS with the exception of the Maintenance Panel.

Manual switch inputs are received from the PDSS Operator Panel via the Controller R-Bus. Commands are then sent to other subsystems via the Controller Result Bus. The manner in which the PDSS responds to these manual switch inputs is determined by the PDSS program residing in the Controller ROM.
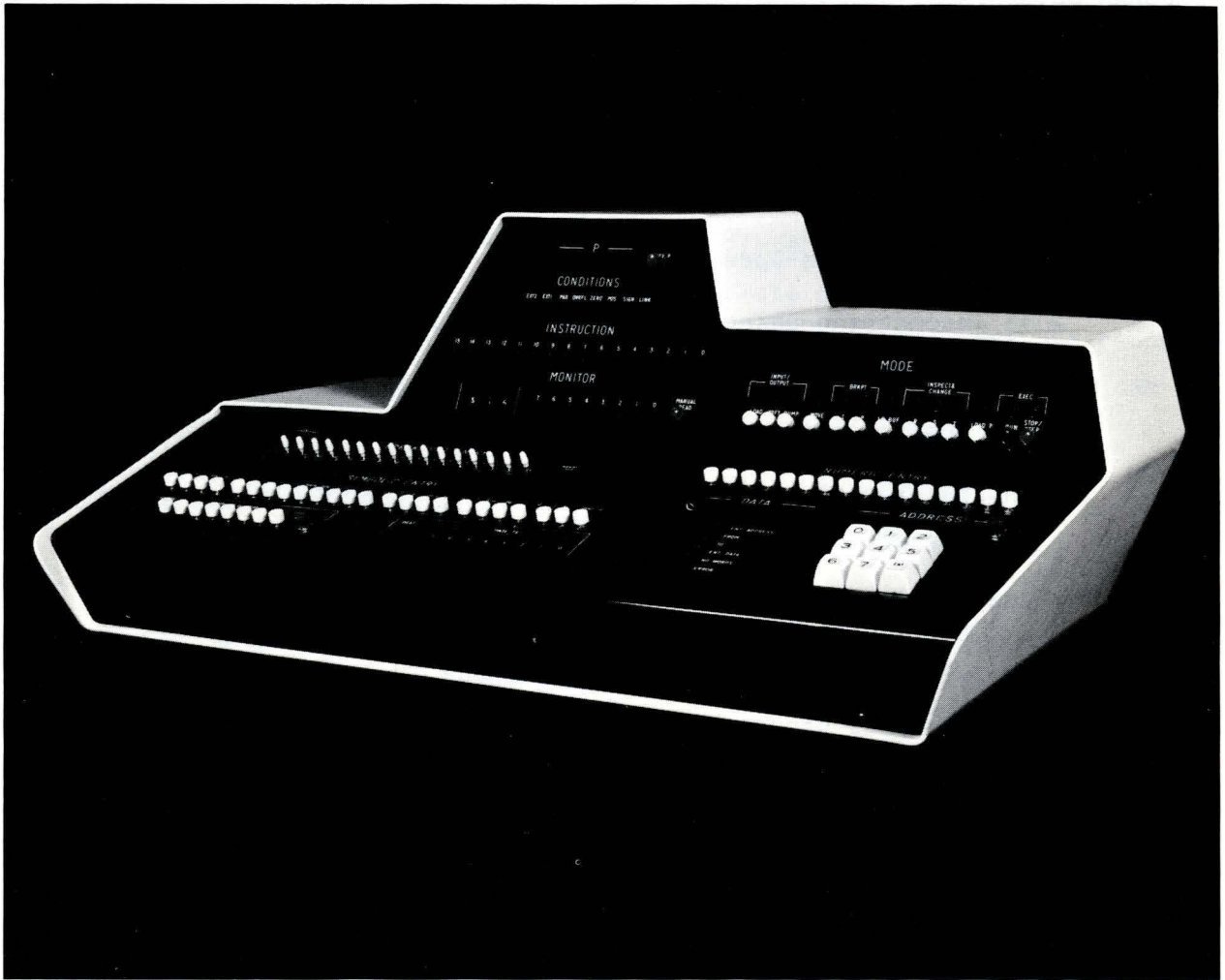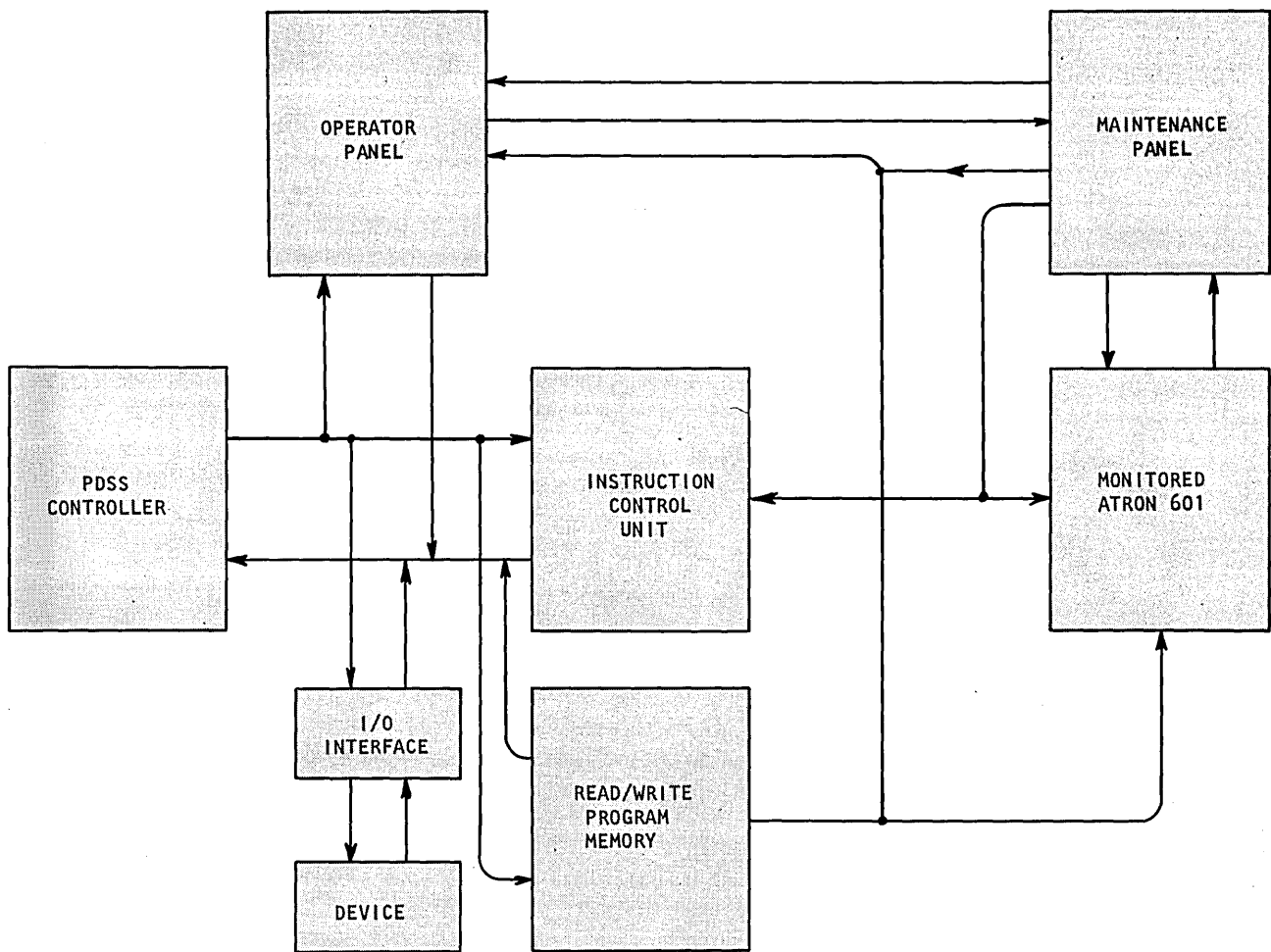
Figure 2-7. Program Development Support System (PDSS)

Operator Panel

The Operator Panel permits the operator to select any of the following operating modes:

- Load
- Verify
- Dump
- Move
- Breakpoint I or P
- Load Buffer
- Inspect-and-Change R, S, or I
- Load P
- Run
- Stop/Step

Instruction Control Unit

The PDSS provides for monitoring of all program addressable S- and R-
Registers. In order to accomplish this, the Controller being monitored is
forced to accept a packet of instructions generated by the PDSS Controller
and assembled by the Instruction Control Unit. These instructions gate
selected registers sequentially onto the 601 Controller R-Bus. Once on the
Bus, they are captured and displayed on the Operator Panel.

Read/Write Program Memory

The R/W Program Memory is a high speed bipolar semiconductor memory of
256, 512, or 1024 16-bit words designed to be used by 601 Controllers. A
memory has both a 16-bit instruction interface and an 8-bit data interface.
In a PDSS hookup, one memory is shared between the monitored 601 and the PDSS
Controller. The monitored 601 uses the instruction interface, executing
instructions placed there by the PDSS Controller via the data interface.

I/O Interface

The I/O Interface is a device-tailored interface and connects to input and
output registers via appropriate drivers and receivers. Control lines and data
are read (input) and written (output) by the PDSS Controller.

Maintenance Panel

The Maintenance Panel allows the Maintenance Engineer to manually
execute 601 micro-instructions and monitor the results. Instruction step and
clock step functions are provided as well as a means for exercising the
Program Memory.

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°Arithmetic/Logical Instructions - These instructions are double-operand instructions where S- and R-Registers are added, subtracted, or logically combined. The results of the operation go to a register specified by the instruction D-field. Conditions generated during execution of this class of instructions will be trapped in the C registers if the instruction so specifies.
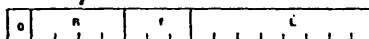
INDEX
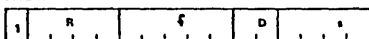
1	R	f	D	s

(s) ⟶ Destination, Set C
(R) ⟶ Destination, Set C
(s) - 1 ⟶ Destination, Set C
(R) - 1 ⟶ Destination, Set C
(s) + 1 ⟶ Destination, Set C
(R) + 1 ⟶ Destination, Set C
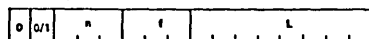(s) + SIGN + LK ⟶ Destination, Set C
(R) + SIGN + LK ⟶ Destination, Set C

See Note 1 to determine Destination.

LITERAL/LOGICAL

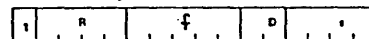| 0	R	f	L

L U (R) ⟶ R
L ⟶ R
L ⊙ (R) ⟶ R
L ∩ (R) ⟶ R
L ⊙ (R), SET C
L ∩ (R), SET C
L ⟶ s

CONDITIONAL JUMP

0	0/1	n	f	L

If BIT n of C = 0/1, L ⟶ P_L

ARITHMETIC/LOGICAL

1	R	f	D	s

(s) + (R) ⟶ Destination
(s) + (R) + LK ⟶ Destination
(s) + (R̄) + 1 ⟶ Destination
(s) + (R̄) + LK ⟶ Destination
(s) U (R) ⟶ Destination
(s) ⊙ (R) ⟶ Destination
(s) ∩ (R) ⟶ Destination
(R̄) ⟶ Destination

SHIFT
Right Shift (R), Fill 1 ⟶ Destination, Set C
Right Shift (R), Fill Sign ⟶ Destination, Set C
Left Shift (R), Fill 0 ⟶ Destination, Set C
Left Shift (R), Fill Sign ⟶ Destination, Set C
Right Shift (s), Fill 1 ⟶ Destination, Set C
Right Shift (s), Fill Sign ⟶ Destination, Set C
Left Shift (s), Fill 0 ⟶ Destination, Set C
Left Shift (s), Fill Sign ⟶ Destination, Set C

See Note 1 to determine Destination.

Note 1: Determining Destination

If D = 0, Result ⟶ Pu, (A) ⟶ P_L
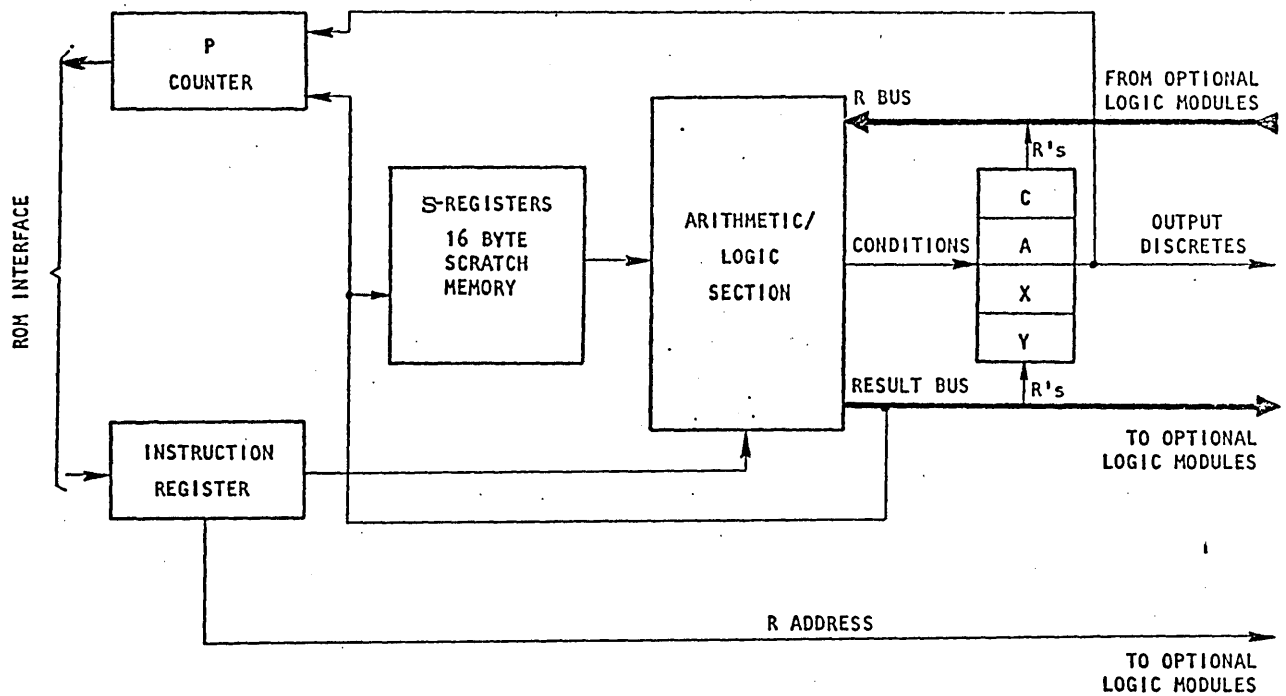   = 1, s
    = 2, R
    = 3, s and R

Set C if c bit of f field.

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Environmental conditions

ATRON 601 Controllers operate in an ambient temperature of from 0° to 50°C and within a relative humidity range of 10% to 95% without condensation. They can be stored at temperatures ranging from -65°C to +150°C.

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ATRON CORPORATION

1256 TRAPP ROAD·ST. PAUL, MINNESOTA 55118