PDP-1 COMPUTER
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PDP-38

MODES, REGISTERS, NEW INSTRUCTIONS, and TRAPS and INTERRUPTS in the PDP-1-X

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Modes

The PDP-1-X will have four general modes of operation, namely TS OFF, TS DEBUG, EXEC, and USER. (These modes are independent of the machine's addressing and extend modes.) The current mode is determined by TS SW, a toggle switch, and the two flip-flops TS and EXEC, as follows:

MODES	TS OFF	TS DEBUG	EXEC	USER
TS SW	0	1	1	1
TS	x	0	1	1
EXEC	x	x	1	0

The modes TS DEBUG and EXEC are called superior modes.

While in mode TS OFF, the only legal instructions are "normal" PDP instructions, the iof and rfn instructions (for i/o), and class I new instructions (see below). Programs running in mode TS DEBUG may execute the same instructions, and class III new instructions in addition. Programs running in EXEC mode may execute all the instructions mentioned above and the class IV instruction ubf as well. Programs running in USER mode may execute "normal" PDP instructions, the ivk instruction (for i/o and supervisor calls), and class I and II new instructions.

Instructions with operation codes 0, 12, and 72 are illegal in all modes.

Mode Switching

Turning off the switch TS SW places the machine in TS OFF mode. Turning on the switch TS SW places the machine in TS DEBUG mode (the flip-flop TS is automatically set to zero when TS SW is turned on).

A program running in TS DEBUG mode may cause the machine to enter EXEC mode by executing the unbreak instruction ubn. When this happens, the executive stateword is loaded into the machine's live registers from core locations 70000 ff. and execution continues at the address specified by the executive program counter, in EXEC mode. If a program running in EXEC mode runs into trouble (e.g., executes an illegal instruction), the executive stateword will be deposited in core locations 70000 ff. and execution will continue at 70006, in TS DEBUG mode.

A program running in EXEC mode may cause the machine to enter USER mode by executing either of the unbreak instructions ubn and ubf. In either case, the stateword addressed by the process pointer is loaded into the machine's live registers (with some special modifications in case of ubf) and execution continues at the address specified by the process' program counter, in USER mode. If a program running in USER mode runs into trouble, or calls the executive with an enter, or executes any of the instructions frk, qit, bpt, or executes a pause mode ivk instruction, or if the machine is in USER mode and an i/o function completes; then the process' stateword will be deposited at the location addressed by the process pointer and execution will continue in EXEC mode at the location peculiar to the trap or interrupt.

If a program running in TS DEBUG or TS OFF mode runs into trouble, the machine stops.

The core translation and protection hardware is active only in USER mode, and in EXEC mode while in EXTEND mode.

The machine operator can force the machine into TS DEBUG mode (if TS SW is on) by pressing the SYSTEM INTERRUPT button on the central indication panel's goose box.

Registers

The PDP-1-X will have several live registers not found in the normal PDP-1. (These registers are required to help cut the overhead of time-shared operation.)

The PDP-1-X will have an 18-bit instruction register, which replaces the standard 5-bit instruction register. This is needed to execute the microprogram instruction, since almost the entire instruction must be saved for the duration of the execution of the instruction, and a cleaner encoding is obtained with a full 18 bits.

There will be a 12-bit (or 15-bit) index register, which is described in a separate memorandum. There is a 2-bit addressing mode register, which holds the nominal addressing mode, coded as follows:

0	normal
1	base
2	index
3	defer

And there is a 1-bit alternation indicator and a 1-bit alternation history indicator, which, from the nominal mode in the addressing mode register, determine the current addressing mode.

There are five registers associated with the process scheduling hardware, which is described in a separate memorandum. The registers are the process pointer (12 bits, always taken to be a core 7 address), the current priority (4 bits) the queue priority (4 bits), the quantum counter (5 bits, and part of processes' statewords), and the quantum timer (8 bits).

There is a fault address register (15 bits) which is reset to the untranslated address of every memory reference made in USER mode. This information is essential to efficient handling of address snags, enter meta-instructions, and "proceed"s away from breakpoints.

The function number register (6 bits) is part of the PDP-1-X i/o controller and holds the function number of the completed function on a FCN SERVICE interrupt. The wait number register (6 bits) holds the function number of the i/o function involved on a FCN BUSY or FCN TARDY trap.

New Instructions

These instructions are the only special time-sharing instructions in the PDP-1-X. They are all of the form 770xxx (particular opcodes have not been assigned as of this writing). They are organized into four legality classes (see the section on modes above).

Class I

eem — enter extend mode

lem — leave extend mode

nam — normal addressing mode

bam — base addressing mode

iam — index addressing mode

dam — defer addressing mode

aam — alternate addressing mode

rpf — read program flags - sets IO_{0-1} to the nominal addressing mode, IO_{2-11} to zeroes, and IO_{12-17} to the contents of the program flags

lpf — load program flags - sets the nominal addressing mode from IO_{0-1} and the program flags from IO_{12-17}

Class II

lck — lock - sets the lock indicator

ulk — unlock - clears the lock indicator

When the lock indicator is set, the process will not be interrupted by the executive; unless it uses more than 64 memory cycles or executes more than one multiply or divide instruction, in which case the LOCK FAULT trap occurs to the executive.

frk — fork - accomplishes a fork

The word after the frk should contain the extended address of where the forked process starts execution. When frk is executed, the program counter is indexed an extra time and the FORK trap occurs to the executive.

qit — quit - accomplishes a quit

The QUIT trap occurs to the executive.

bpt — breakpoint - the BREAKPOINT trap occurs to the executive

Class III

rfa — read fault address - sets IO_{3-17} to the fault address, and clears IO_{0-2}

rbn — read break number - places the number which indicates which trap or interrupt occurred in IO_{1-5}, and clears IO_0 and IO_{6-17}

rfn — read function number - clears IO_{0-5}, sets IO_{6-11} to the contents of the function number register, and sets IO_{12-17} to the contents of the wait number register

lpp — load process pointer - sets the process pointer from IO_{6-17}

rpp — read process pointer - sets IO_{6-17} from the process pointer

sqp — set queue priority - sets the queue priority from IO_{14-17}

rqp — read queue priority - sets IO_{14-17} from the queue priority

scp — set current priority - similarly

rcp — read current priority - similarly

cqt — clear quantum timer - clears the quantum timer register

ubn — unbreak normal - pick up a new stateword and change mode

Class IV

ubf unbreak fork - start the forked process

This instruction is used to help accomplish a fork. The new stateword is picked up from the locations addressed by the process pointer, and the process pointer is replaced by the contents of the AC (not quite in any order). (The process pointer should then point to the new process entity.) The program counter is undexed and then replaced by the word it addresses. The machine switches to USER mode and continues.

Traps and Interrupts

When a trap or an interrupt occurs to the executive, the process' stateword is deposited in the locations addressed by the process pointer, the process pointer is jammed into the index register, and execution continues in EXEC mode at the location peculiar to the trap or interrupt. (These locations will start at 70040 but the exact location peculiar to each trap has not been assigned as of this writing.) The traps and interrupts are as follows:

FCN SERVICE - completion of an i/o function
FCN BUSY - error on the part of the running process
FCN TARDY - error on the part of the running process
FCN STARTED - the running process has executed a pause mode ivk instruction

META

ENTER - the running process has invoked an entry capability

FORK

QUIT

BREAKPOINT

HALT - the running process has attempted to stop the clock

ADDRESS SNAG - the running process has attempted to refer to a program image section not in core

ILLEGAL OPCODE

LOCK FAULT - this is handled by the exec as an error condition

SINGLE INSTRUCTION DONE

PREEMPT - leave this process on this queue level and run most deserving process

RND RBN - demote this process and run most deserving process

SYSTEM INTERRUPT