LISP Machine TV Board CADRTV;LMTV4B UML 07-DEC-80 2352
******* DIP MAP *******

26S10 XBDATA x F30	74LS299 RAMSHF x E30	2118 RAMD x D30	2118 RAMC x C30	2118 RAMB x B30	2118 RAMA x A30
26S10 XBDATA x F29	74LS374 RAMREG x E29	2118 RAMD x D29	2118 RAMC x C29	2118 RAMB x B29	2118 RAMA x A29
26S10 XBDATA x F28	74LS299 RAMSHF x E28	2118 RAMD x D28	2118 RAMC x C28	2118 RAMB x B28	2118 RAMA x A28
26S10 XBDATA x F27	74LS374 RAMREG x E27	2118 RAMD x D27	2118 RAMC x C27	2118 RAMB x B27	2118 RAMA x A27
26S10 XBDATA x F26	74LS299 RAMSHF x E26	2118 RAMD x D26	2118 RAMC x C26	2118 RAMB x B26	2118 RAMA x A26
26S10 XBDATA x F25	74LS374 RAMREG x E25	2118 RAMD x D25	2118 RAMC x C25	2118 RAMB x B25	2118 RAMA x A25
26S10 XBDATA x F24	74LS299 RAMSHF x E24	2118 RAMD x D24	2118 RAMC x C24	2118 RAMB x B24	2118 RAMA x A24
26S10 XBDATA x F23	74LS374 RAMREG x E23	2118 RAMD x D23	2118 RAMC x C23	2118 RAMB x B23	2118 RAMA x A23
25LS2521 XBADR x F22	74LS299 RAMSHF x E22	2118 RAMD x D22	2118 RAMC x C22	2118 RAMB x B22	2118 RAMA x A22
25LS2521 XBADR x F21	74LS374 RAMREG x E21	2118 RAMD x D21	2118 RAMC x C21	2118 RAMB x B21	2118 RAMA x A21
25LS2521 XBADR x F20	74LS299 RAMSHF x E20	2118 RAMD x D20	2118 RAMC x C20	2118 RAMB x B20	2118 RAMA x A20

LISP Machine TV Board CADRTV;LMTV4B UML 07-DEC-80 2353
******* DIP MAP *******

25LS2521 XBADR x F19	74LS374 RAMREG x E19	2118 RAMD x D19	2118 RAMC x C19	2118 RAMB x B19	2118 RAMA x A19
74LS240 XBADR x F18	74LS299 RAMSHF x E18	2118 RAMD x D18	2118 RAMC x C18	2118 RAMB x B18	2118 RAMA x A18
74LS240 XBADR x F17	74LS374 RAMREG x E17	2118 RAMD x D17	2118 RAMC x C17	2118 RAMB x B17	2118 RAMA x A17
74LS240 XBADR x F16	74LS299 RAMSHF x E16	2118 RAMD x D16	2118 RAMC x C16	2118 RAMB x B16	2118 RAMA x A16
26S10 XBDATA x F15	74LS374 RAMREG x E15	2118 RAMD x D15	2118 RAMC x C15	2118 RAMB x B15	2118 RAMA x A15
26S10 XBDATA x F14	74LS74 XBCTL xx E14	898-3-R2 RAMBUF x D14	898-3-R2 RAMBUF x C14	898-3-R2 RAMBUF x B14	898-3-R2 RAMBUF x A14
74S138 XBCTL x F13	74S00 XBCTL xxxx E13	74LS244 COLOR x D13	74S37 RAMCAS xxxx C13	898-3-R2 RAMCAS x B13	74S241 RAMBUF x A13
25LS2519 XBCTL x F12	74S374 XBCTL x E12	74S00 SYNCLK xxxx D12	25LS2539 RAMCAS xx C12	74S253 RAMADR x B12	74S253 RAMADR x A12
74LS244 COLOR x F11	74S32 COLOR xxxo E11	TD100 RAMCAS x D11	74S37 SYNCLK xxxx C11	74S253 RAMADR x B11	74S253 RAMADR x A11
74S04 XBDATA xxxxxx F10	74S139 XBCTL xx E10	74S08 SYNCLK xxxx D10	74LS163 TVMA x C10	74LS569 RAMADR x B10	74LS569 RAMADR x A10
74S257 COLOR x F09	74S241 COLOR x E09	74S37 SYNCLK xxxx D09	74LS163 TVMA x C09	74LS163 TVMA x B09	74LS163 TVMA x A09

LISP Machine TV Board CADRTV;LMTV4B UML 07-DEC-80 2353
******* DIP MAP *******

10105 ECLCLK oox F08	74128 ECLVID xxoo E08	74S04 RAMADR xxxxxx D08	EXAR-CL ECLCLK x C08	74S283 TVINC x B08	74S283 TVINC x A08
10124 ECLCLK x F07	10124 ECLVID x E07	74S374 SYNCLK x D07	74LS377 SYNADR x C07	74LS377 SYNADR x B07	74LS273 TVINC x A07
10124 ECLVID x F06	10124 ECLVID x E06	74S288 SYNCLK x D06	74LS569 SYNADR x C06	74LS569 SYNADR x B06	74LS569 SYNADR x A06
DUAL-SIP ECLSIP x F05	DUAL-SIP ECLSIP x E05	74LS244 SYNRAM x D05	74S472 SYNRAM x C05	74LS374 SYNADR x B05	74LS374 SYNADR x A05
10102 ECLVID xxxx F04	10141 ECLVID x E04	74S51 TVMA xx D04	25LS2539 SYNREG xx C04	2147 SYNRAM x B04	2147 SYNRAM x A04
10212 ECLVID xo F03	10141 ECLVID x E03	74S04 TVMA xxxxxx D03	74S374 SYNREG x C03	2147 SYNRAM x B03	2147 SYNRAM x A03
10136 ECLCLK x F02	10125 ECLCLK x E02	74LS175 SYNREG x D02	74LS669 SYNREG x C02	2147 SYNRAM x B02	2147 SYNRAM x A02
10121 ECLVID x F01	DUAL-SIP ECLSIP x E01	74S10 SYNREG xxx D01	74LS669 SYNREG x C01	2147 SYNRAM x B01	2147 SYNRAM x A01

LISP Machine TV Board CADRTV;LMTV4B UML 07-DEC-80 2353
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

-A-	-B-	-C-	-D-
A1 -XBUS35 A2 +5.0V++++++++++++++++++	A1 -XBUS5 A2 +5.0V++++++++++++++++++ #	A1 A2 +5.0V++++++++++++++++++	A1 A2 +5.0V++++++++++++++++++
B1 -XBUS34 B2	B1 -XBUS4 B2 #	B1 B2	B1 B2
C1 -XBUS33 C2 DEVADR 17----------	C1 -XBUS3 C2 DEVADR 17---------- #	C1 C2 DEVADR 17----------	C1 C2 DEVADR 17----------
D1 -XBUS32 D2 -XBUS31	D1 -XBUS2 # D2 -XBUS1	D1 # D2 -XBUS.RQ H	D1 D2
E1 -XBUS30 E2 -XBUS29	# E1 -XBUS0 # E2 -XBUS.PAR	# E1 E2 -XBUS.ACK H	E1 -COLOR CLK H # E2
F1 DEVADR 17 F2 -XBUS28	F1 DEVADR 17 # F2 -XADDR.PAR	F1 DEVADR 17 F2 -XBUS.WR H	F1 DEVADR 17 # F2
H1 -XBUS27 H2 -XBUS26	# H1 -XADDR 21 H # H2 -XADDR 20 H	H1 -XBUS.EXTGRANT.IN H2 -XBUS.IGNPAR H	H1 -LOAD COLOR 0 H # H2
J1 -XBUS25 J2 -XBUS24	# J1 -XADDR 19 H # J2 -XADDR 18 H	J1 -XBUS.EXTGRANT.OUT J2 -XBUS.INIT H	J1 -LOAD COLOR 1 H # # J2
K1 -XBUS23 K2 -XBUS22	# K1 -XADDR 17 H # K2 -XADDR 16 H	K1 XBUS.POWER.OK K2 -XBUS.EXTRQ	K1 -LOAD COLOR 2 H # K2
L1 -XBUS21 L2 -XBUS20	# L1 -XADDR 15 H # L2 -XADDR 14 H	L1 L2 -XBUS.BUSY	L1 L2
M1 -XBUS19 M2 -XBUS18	# M1 -XADDR 13 H # M2 -XADDR 12 H	M1 M2 -XBUS.SYNC	M1 M2
N1 DEVADR 17 N2 -XBUS17	N1 DEVADR 17 # N2 -XADDR 11 H	N1 DEVADR 17 N2	N1 DEVADR 17 N2
P1 -XBUS16 P2 -XBUS15	# P1 -XADDR 10 H # P2 -XADDR 9 H	P1 P2 -XBUS.INTR H	# P1 P2
R1 -XBUS14 R2 -XBUS13	# R1 -XADDR 8 H # R2 -XADDR 7 H	R1 R2	R1 R2
S1 -XBUS12 S2 -XBUS11	# S1 -XADDR 6 H # S2 -XADDR 5 H	S1 S2	S1 S2
T1 DEVADR 17---------- T2 -XBUS10	T1 DEVADR 17---------- # T2 -XADDR 4 H	T1 DEVADR 17---------- T2	T1 DEVADR 17---------- T2
U1 -XBUS9 U2 -XBUS8	# U1 -XADDR 3 H # U2 -XADDR 2 H	U1 -XBUS POWER RESET H # U2	U1 U2
V1 -XBUS7 V2 -XBUS6	# V1 -XADDR 1 H # V2 -XADDR 0 H	V1 V2	V1 V2

LISP Machine TV Board CADRTV;LMTV4B UML 07-DEC-80 2353
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

-E-		-F-		-J01-	-J02-
A1		A1		01	01
A2 +5.0V++++++++++++++++++		A2 +5.0V++++++++++++++++++		02	02
B1		B1		03	03
B2		B2		04	04
C1		C1		05	05
C2 DEVADR 17----------		C2 DEVADR 17----------		06	06
D1		D1 COMP VIDEO OUT		07	07
D2		D2		08	08
E1		E1 -BLANKING (FUDGED) H	#	09	09
E2		E2 TTL VIDEO DRIVE	#	10	10
F1 DEVADR 17		F1 DEVADR 17		11	11
F2		F2		12	12
H1 COLOR VALUE 0	#	H1 MECL VIDEO OUT	#	13	13
H2		H2		14	14
J1 COLOR VALUE 1	#	J1 -MECL VIDEO OUT H	#	16	15
J2		J2		16	16
K1 COLOR VALUE 2	#	K1 COLOR 0	#	17	17
K2		K2		18	18
L1 COLOR VALUE 3	#	L1 COLOR 1	#	19	19
L2		L2		20	20
M1 COLOR VALUE 4	#	M1 COLOR 2	#	21	21
M2		M2		22	22
N1 DEVADR 17		N1 DEVADR 17		23	23
N2		N2		24	24
P1 COLOR VALUE 5	#	P1 COLOR 3	#	25	25
P2		P2		26 ----------	26 ----------
R1 COLOR VALUE 6	#	R1 COLOR 4	#	27 ----------	27 ----------
R2		R2		28 ----------	28 ----------
S1 COLOR VALUE 7	#	S1 COLOR 5	#	29 ----------	29 ----------
S2		S2		30 ----------	30 ----------
T1 DEVADR 17----------		T1 DEVADR 17----------		31 ----------	31 ----------
T2		T2		32 ----------	32 ----------
U1 HSYNC OUT	#	U1 COLOR 6	#	33 ----------	33 ----------
U2		U2		34 ----------	34 ----------
V1 VSYNC OUT	#	V1 COLOR 7	#	35 ----------	35 ----------
V2		V2		36 ----------	36 ----------
				37 ----------	37 ----------
				38 ----------	38 ----------
				39 ----------	39 ----------
				40 ----------	40 ----------
				41 ----------	41 ----------
				42 ----------	42 ----------
				43 ----------	43 ----------
				44 ----------	44 ----------
				45 ----------	45 ----------
				46 ----------	46 ----------
				47 ----------	47 ----------
				48 ----------	48 ----------
				49 ----------	49 ----------
				50 ----------	50 ----------

LISP Machine TV Board CADRTV;LMTV4B UML 07-DEC-80 2354
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ----,Dedicated ground, ++++ Dedicated power) *******

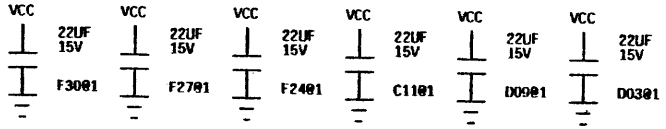
-J03-	-J04-	-J05-	-J06-
01 02	01 02	01 02	01 02
03 04	03 04	03 04	03 04
05 06	05 06	05 06	05 06
07 08	07 08	07 08	07 08
09 10	09 10	09 10	09 10
11 12	11 12	11 12	11 12
13 14	13 14	13 14	13 14
15 16	15 16	15 16	15 16
17 18	17 18	17 18	17 18
19 20	19 20	19 20	19 20
21 ---------- 22 ----------	21 ---------- 22 ----------	21 22	21 22
23 ---------- 24 ----------	23 ---------- 24 ----------	23 24	23 24
25 ---------- 26 ----------	25 ---------- 26 ----------	25 26 ----------	25 26 ----------
27 ---------- 28 ----------	27 ---------- 28 ----------	27 ---------- 28 ----------	27 ---------- 28 ----------
29 ---------- 30 ----------	29 ---------- 30 ----------	29 ---------- 30 ----------	29 ---------- 30 ----------
31 ---------- 32 ----------	31 ---------- 32 ----------	31 ---------- 32 ----------	31 ---------- 32 ----------
33 ---------- 34 ----------	33 ---------- 34 ----------	33 ---------- 34 ----------	33 ---------- 34 ----------
35 ---------- 36 ----------	35 ---------- 36 ----------	35 ---------- 36 ----------	35 ---------- 36 ----------
37 ---------- 38 ----------	37 ---------- 38 ----------	37 ---------- 38 ----------	37 ---------- 38 ----------
39 ---------- 40 ----------	39 ---------- 40 ----------	39 ---------- 40 ----------	39 ---------- 40 ----------
		41 ---------- 42 ----------	41 ---------- 42 ----------
		43 ---------- 44 ----------	43 ---------- 44 ----------
		45 ---------- 46 ----------	45 ---------- 46 ----------
		47 ---------- 48 ----------	47 ---------- 48 ----------
		49 ---------- 50 ----------	49 ---------- 50 ----------

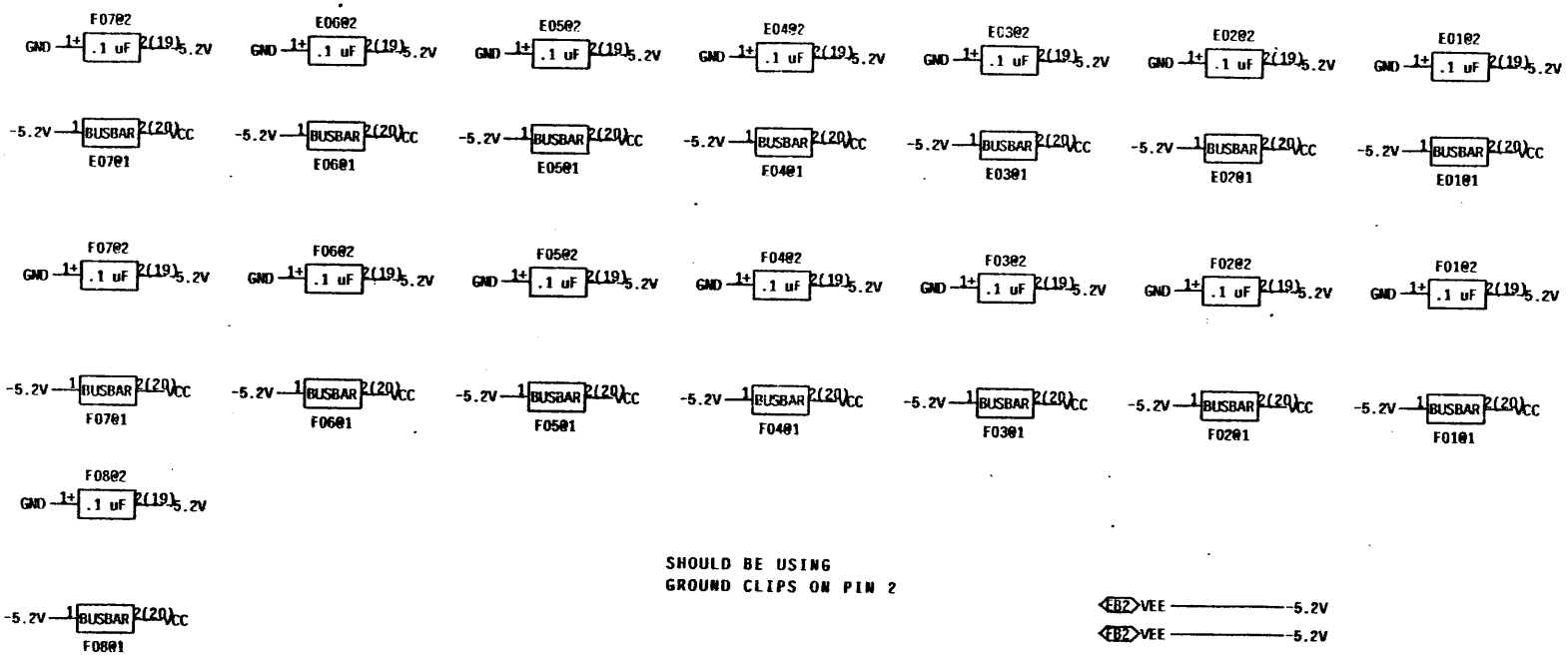
LISP Machine TV Board CADRTV;LMTV4B UML 07-DEC-80 2354
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

-J07-	-J08-	-J09-	-J10-
01 02	01 02	01 02	01 02
03 04	03 04	03 04	03 04
05 06	05 06	05 06	05 06
07 08	07 08	07 08	07 08
09 10	09 10	09 10	09 10
11 12	11 12	11 12	11 12
13 14	13 14	13 14	13 14
15 16	15 16	15 16	15 16
17 18	17 18	17 18	17 18
19 20	19 20	19 20	19 20
21 ---------- 22 ----------	21 ---------- 22 ----------	21 22	21 22
23 ---------- 24 ----------	23 ---------- 24 ----------	23 24	23 24
25 ---------- 26 ----------	25 ---------- 26 ----------	25 26 ----------	25 26 ----------
27 ---------- 28 ----------	27 ---------- 28 ----------	27 ---------- 28 ----------	27 ---------- 28 ----------
29 ---------- 30 ----------	29 ---------- 30 ----------	29 ---------- 30 ----------	29 ---------- 30 ----------
31 ---------- 32 ----------	31 ---------- 32 ----------	31 ---------- 32 ----------	31 ---------- 32 ----------
33 ---------- 34 ----------	33 ---------- 34 ----------	33 ---------- 34 ----------	33 ---------- 34 ----------
35 ---------- 36 ----------	35 ---------- 36 ----------	35 ---------- 36 ----------	35 ---------- 36 ----------
37 ---------- 38 ----------	37 ---------- 38 ----------	37 ---------- 38 ----------	37 ---------- 38 ----------
39 ---------- 40 ----------	39 ---------- 40 ----------	39 ---------- 40 ----------	39 ---------- 40 ----------
		41 ---------- 42 ----------	41 ---------- 42 ----------
		43 ---------- 44 ----------	43 ---------- 44 ----------
		45 ---------- 46 ----------	45 ---------- 46 ----------
		47 ---------- 48 ----------	47 ---------- 48 ----------
		49 ---------- 50 ----------	49 ---------- 50 ----------

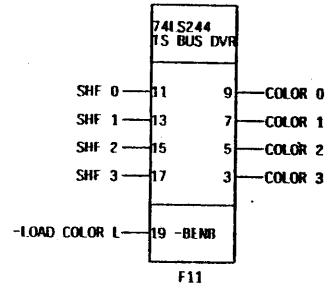
LISP Machine TV Board CADRTV;LMTV4B UML 07-DEC-80 2354
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

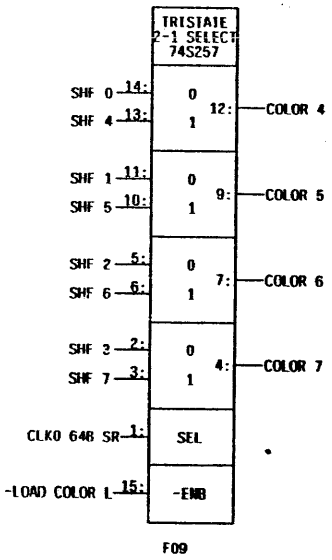
-J11-	-J12-
01 02	01 02
03 04	03 04
05 06	05 06
07 08	07 08
09 10	09 10
11 12	11 12
13 14	13 14
15 16	15 16
17 18	17 18
19 20	19 20
21 ---------- 22 ----------	21 ---------- 22 ----------
23 ---------- 24 ----------	23 ---------- 24 ----------
25 ---------- 26 ----------	25 ---------- 26 ----------
27 ---------- 28 ----------	27 ---------- 28 ----------
29 ---------- 30 ----------	29 ---------- 30 ----------
31 ---------- 32 ----------	31 ---------- 32 ----------
33 ---------- 34 ----------	33 ---------- 34 ----------
35 ---------- 36 ----------	35 ---------- 36 ----------
37 ---------- 38 ----------	37 ---------- 38 ----------
39 ---------- 40 ----------	39 ---------- 40 ----------

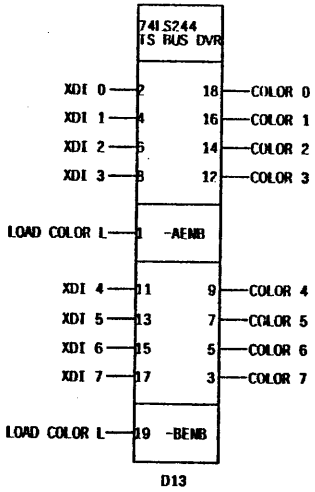


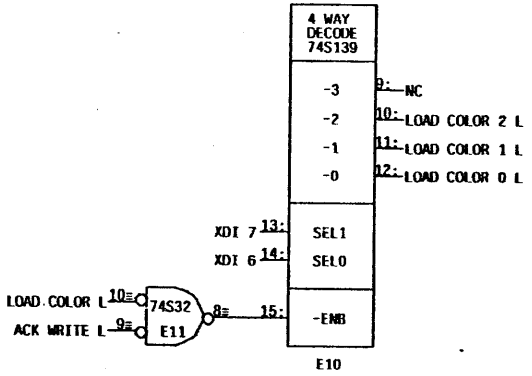


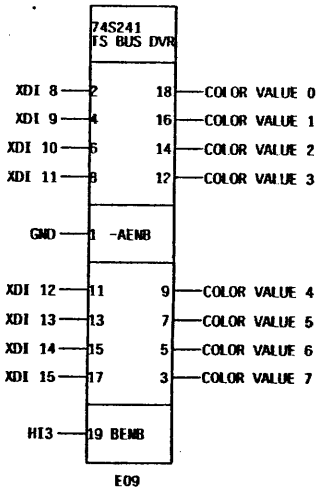
LISPM TV	Bypass Caps	7-FEB-1981 12:34	AI: CADRTV; CAPS



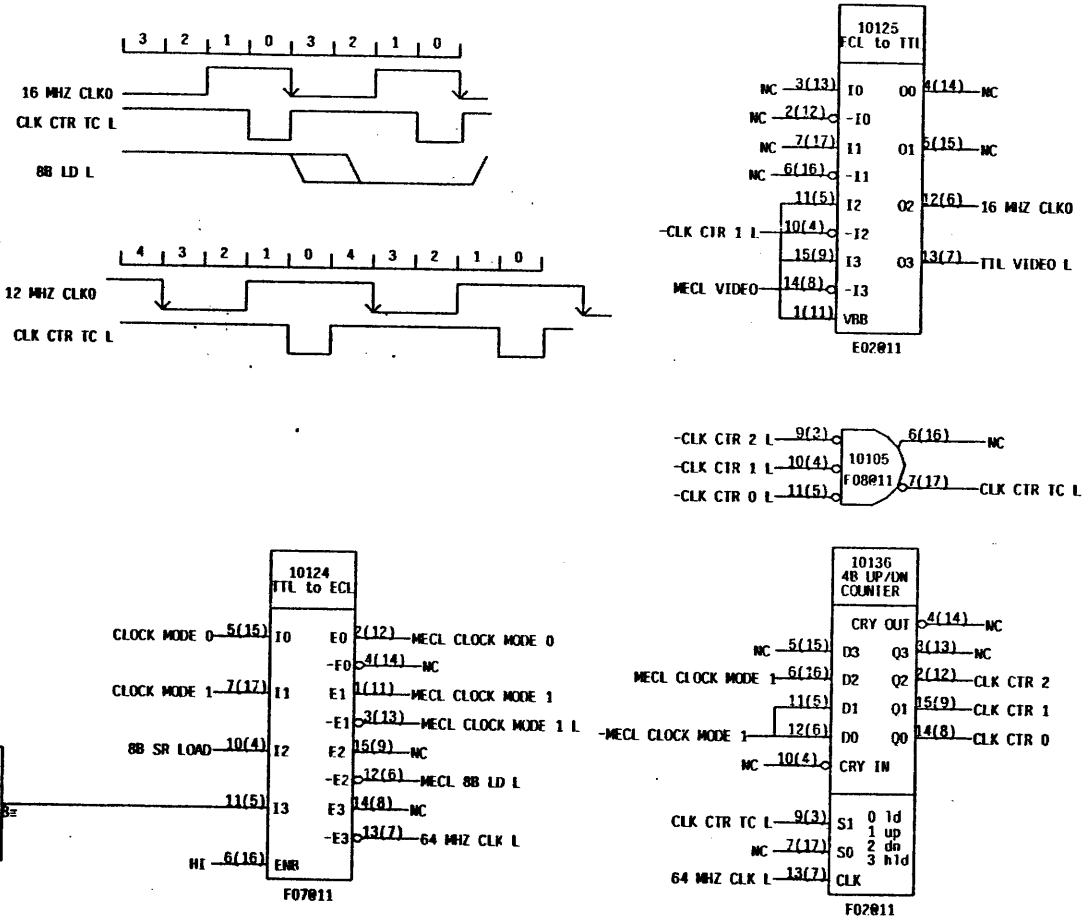






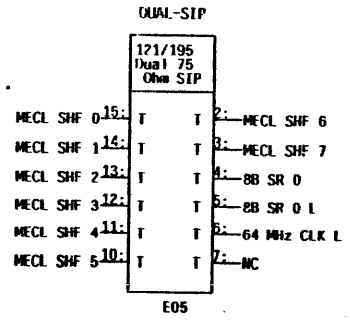


LISPM TV	Color Map Interface	7-DEC-1980 22:51	AI: CADRTV; COLOR

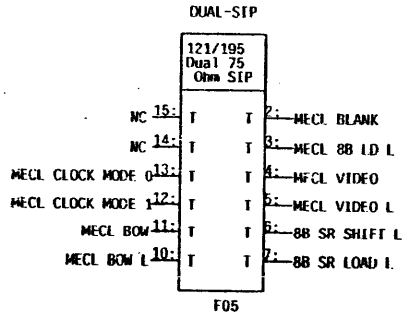


LISPM TV	MECL Clock	7-DEC-1980 22:49	AI: CADRTV; ECLCLK

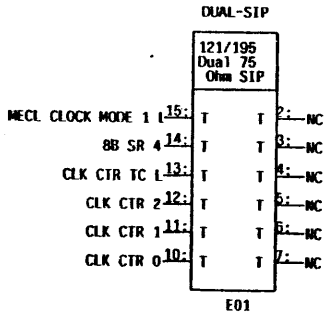
NOTE: Install with pin 1 down



NOTE: Install with pin 1 down

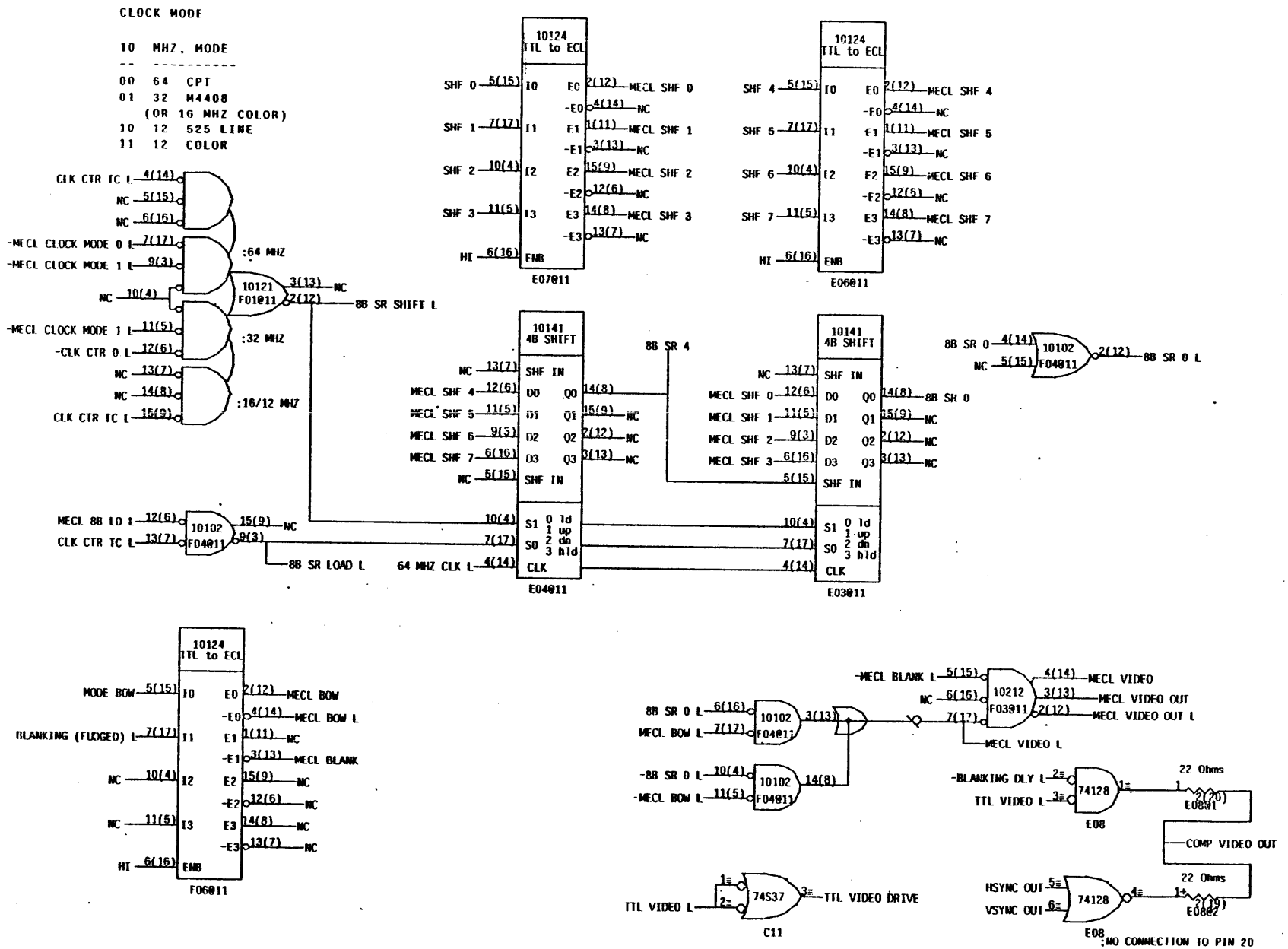


NOTE: Install with pin 1 down

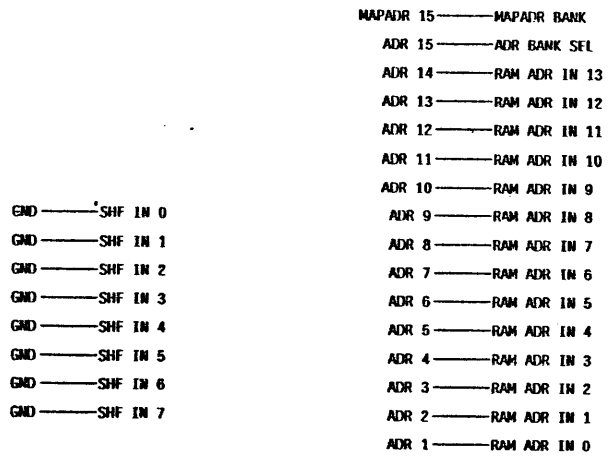


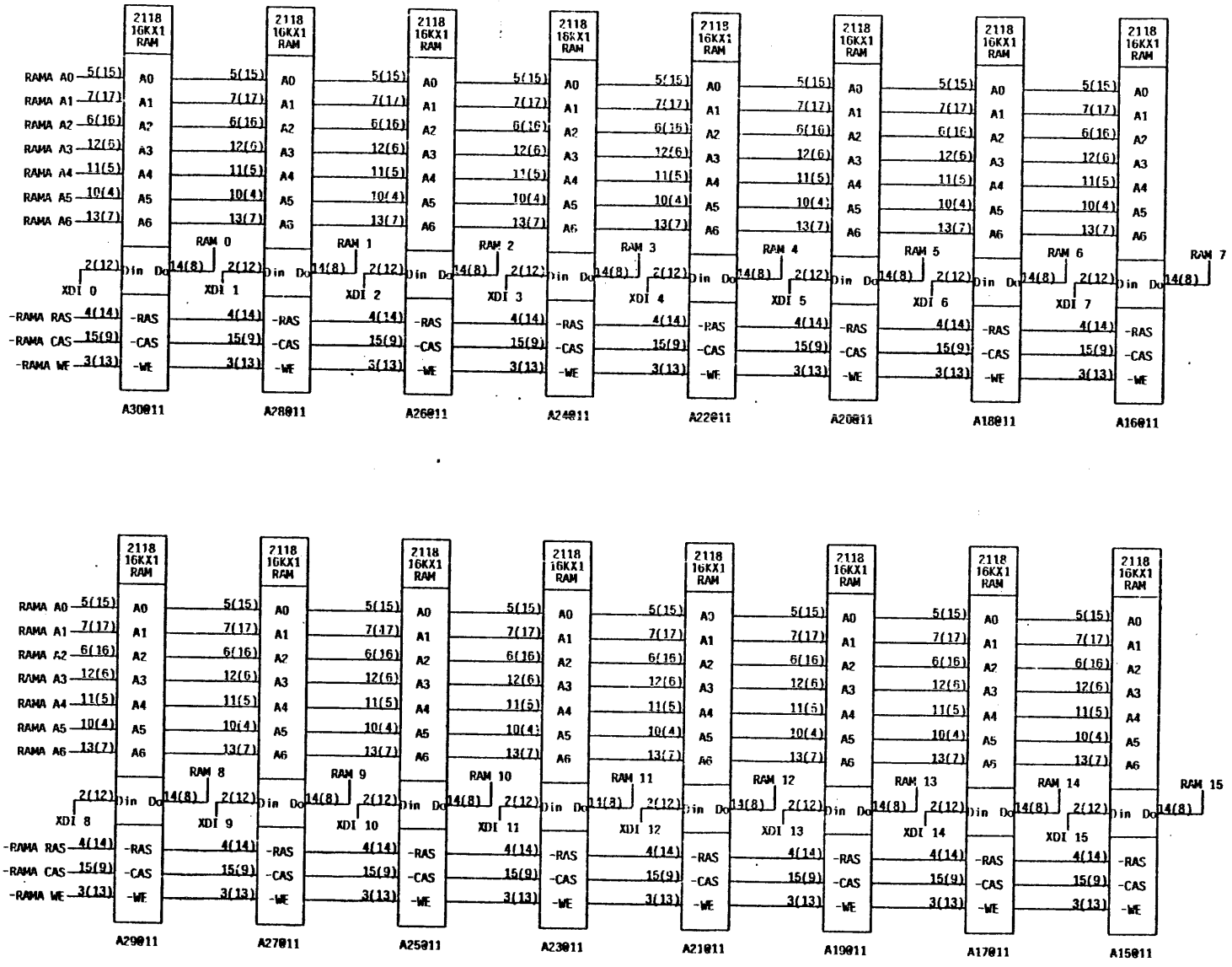
INSTALL 121 OHM SIDE OF SIP CONNECTED TO PIN 10

THE "NC" SIP PINS SHOULD MEASURE -2 VOLTS



LISPM TV	MECL Video	7-DEC-1980 22:44	AI: CADRTV; ECLVID


GND SHF IN 0
GND SHF IN 1
GND SHF IN 2
GND SHF IN 3
GND SHF IN 4
GND SHF IN 5
GND SHF IN 6
GND SHF IN 7
MAPADR 15 MAPADR BANK
ADR 15 ADR BANK SEL
ADR 14 RAM ADR IN 13
ADR 13 RAM ADR IN 12
ADR 12 RAM ADR IN 11
ADR 11 RAM ADR IN 10
ADR 10 RAM ADR IN 9
ADR 9 RAM ADR IN 8
ADR 8 RAM ADR IN 7
ADR 7 RAM ADR IN 6
ADR 6 RAM ADR IN 5
ADR 5 RAM ADR IN 4
ADR 4 RAM ADR IN 3
ADR 3 RAM ADR IN 2
ADR 2 RAM ADR IN 1
ADR 1 RAM ADR IN 0


2118 16KX1 RAM
RAMA A0
RAMA A1
RAMA A2
RAMA A3
RAMA A4
RAMA A5
RAMA A6
-RAMA RAS
-RAMA CAS
-RAMA WE
A0
A1
A2
A3
A4
A5
A6
-RAS
-CAS
-WE
Din
Dout
RAM 0
RAM 1
RAM 2
RAM 3
RAM 4
RAM 5
RAM 6
RAM 7
RAM 8
RAM 9
RAM 10
RAM 11
RAM 12
RAM 13
RAM 14
RAM 15
XDI 0
XDI 1
XDI 2
XDI 3
XDI 4
XDI 5
XDI 6
XDI 7
XDI 8
XDI 9
XDI 10
XDI 11
XDI 12
XDI 13
XDI 14
XDI 15
A30011
A28011
A26011
A24011
A22011
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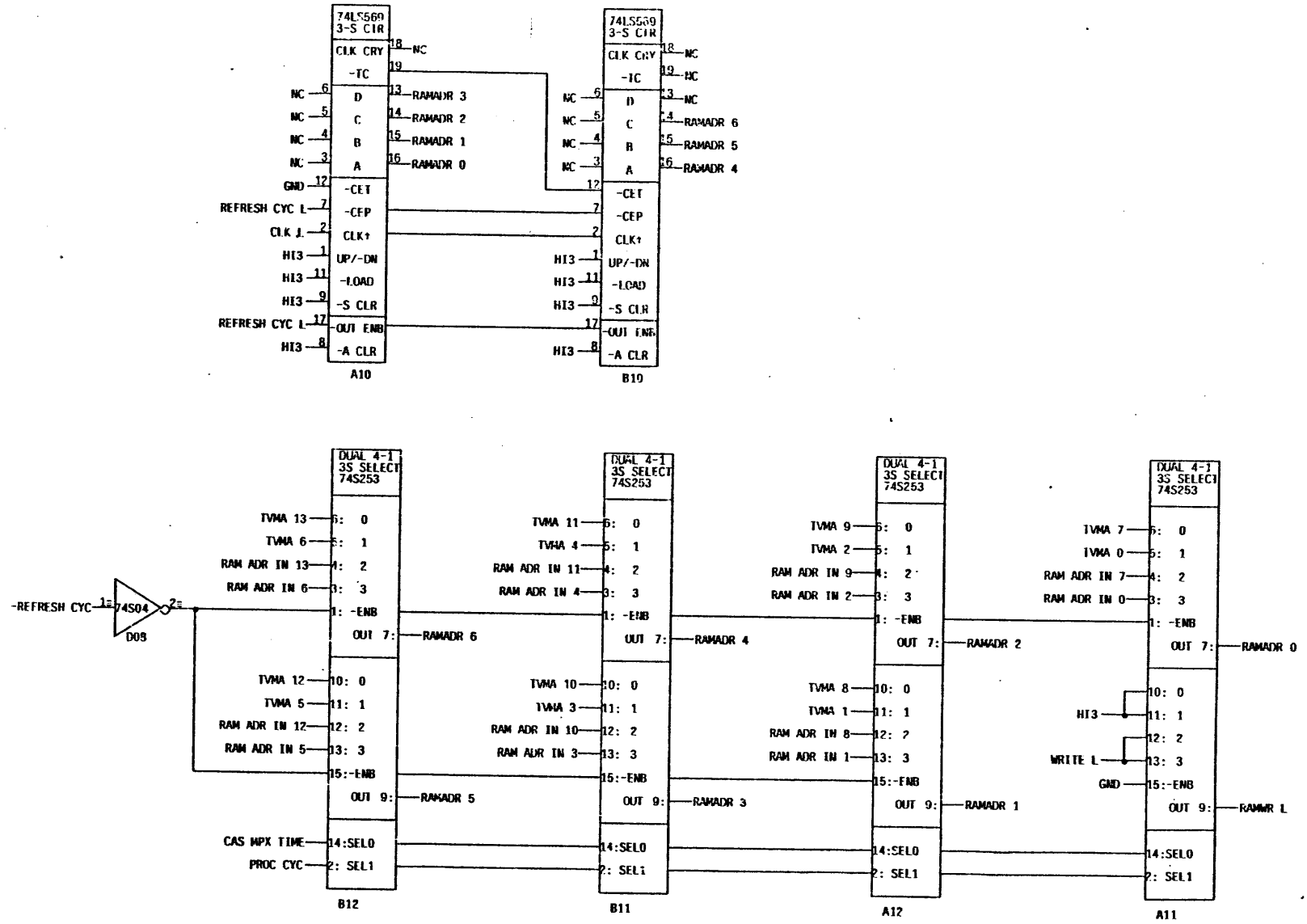
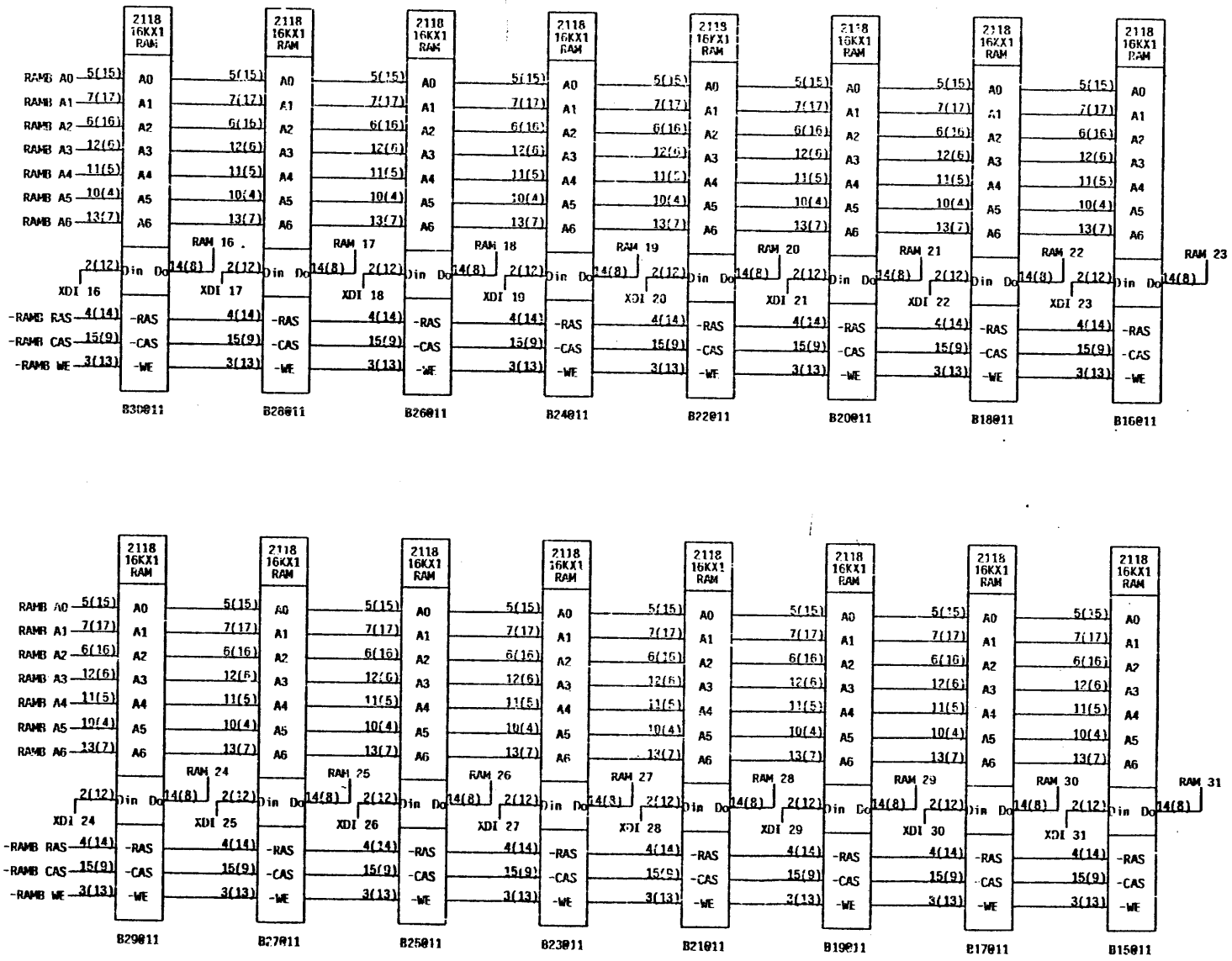
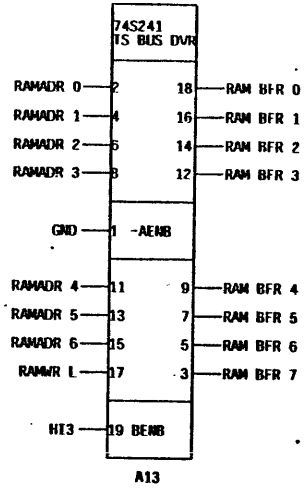
A25011
A23011
A21011
A19011
A17011
A15011

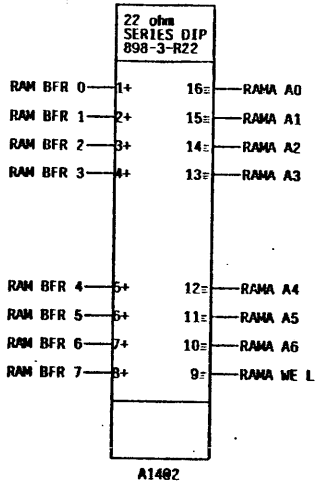


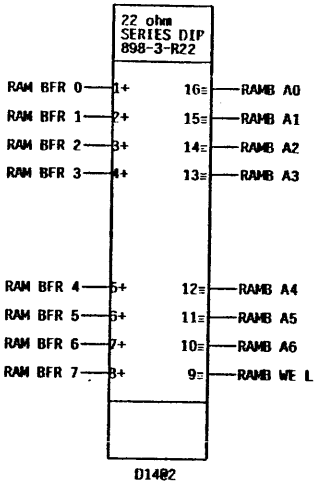
LISPM TV	Ram Address Logic	7-DEC-1980 22:50	AI: CADRTV; RAMADR

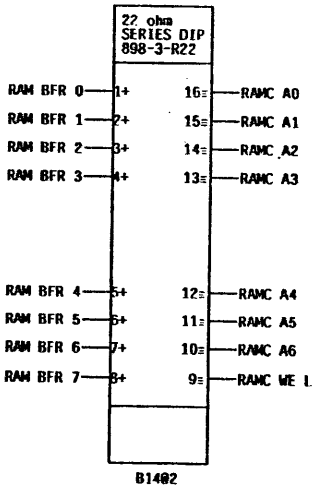


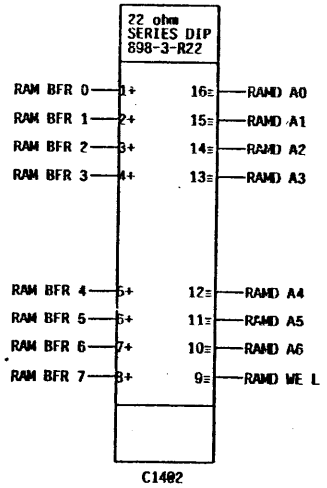
LISPM TV	Video Memory: Row B	7-DEC-1980 19:50	AI: CADRTV; RAMB

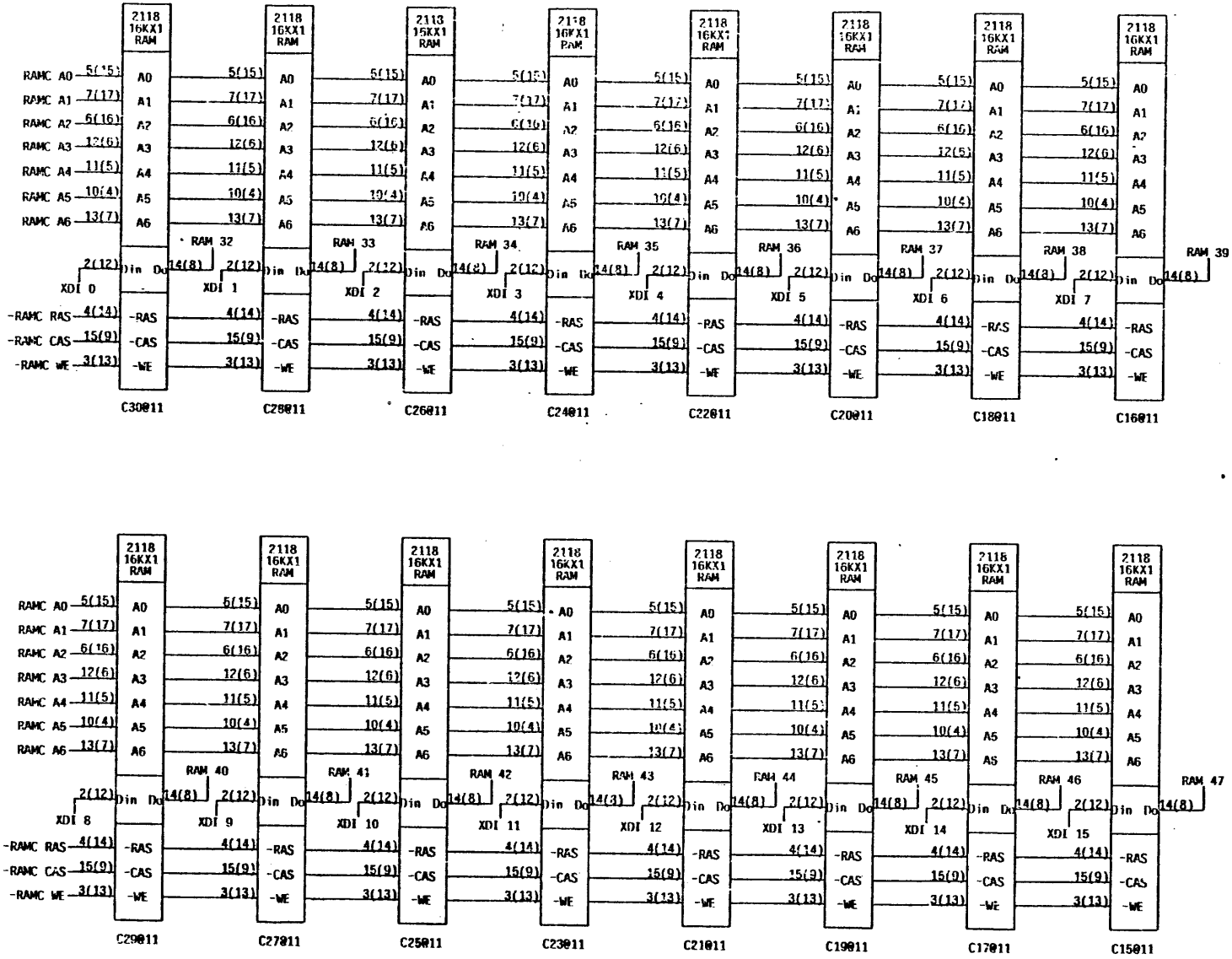

74S241
TS BUS DVR
RAMADR 0
RAMADR 1
RAMADR 2
RAMADR 3
GND
-AENB
RAMADR 4
RAMADR 5
RAMADR 6
RAMWR L
HI3
BENB
RAM BFR 0
RAM BFR 1
RAM BFR 2
RAM BFR 3
RAM BFR 4
RAM BFR 5
RAM BFR 6
RAM BFR 7
A13

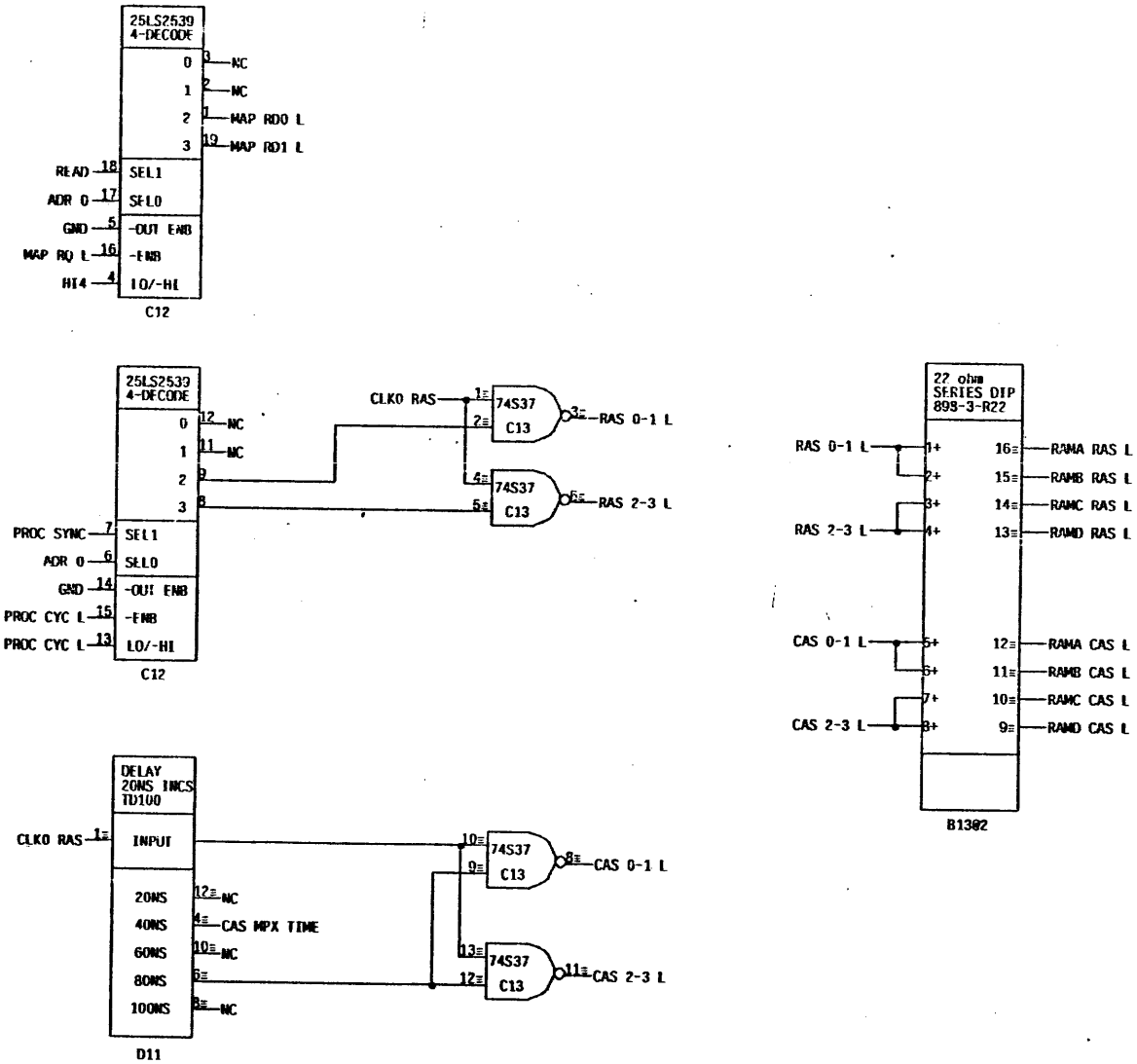

22 ohm
SERIES DIP
898-3-R22
RAM BFR 0
RAM BFR 1
RAM BFR 2
RAM BFR 3
RAM BFR 4
RAM BFR 5
RAM BFR 6
RAM BFR 7
RAMA A0
RAMA A1
RAMA A2
RAMA A3
RAMA A4
RAMA A5
RAMA A6
RAMA WE L
A1402

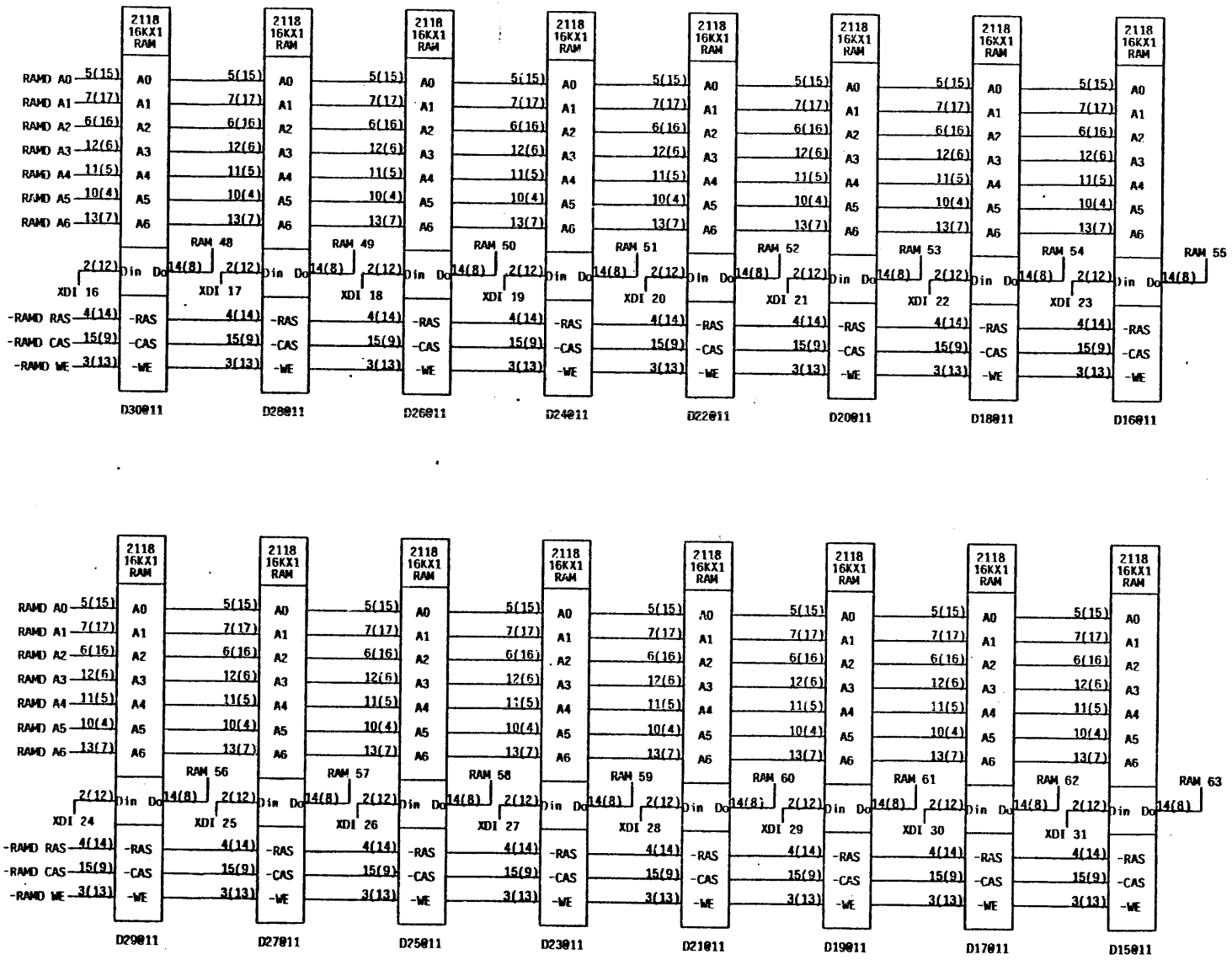

22 ohm
SERIES DIP
898-3-R22
RAM BFR 0
RAM BFR 1
RAM BFR 2
RAM BFR 3
RAM BFR 4
RAM BFR 5
RAM BFR 6
RAM BFR 7
RAMB A0
RAMB A1
RAMB A2
RAMB A3
RAMB A4
RAMB A5
RAMB A6
RAMB WE L
D1402


22 ohm
SERIES DIP
898-3-R22
RAM BFR 0
RAM BFR 1
RAM BFR 2
RAM BFR 3
RAM BFR 4
RAM BFR 5
RAM BFR 6
RAM BFR 7
RAMC A0
RAMC A1
RAMC A2
RAMC A3
RAMC A4
RAMC A5
RAMC A6
RAMC WE L
B1402

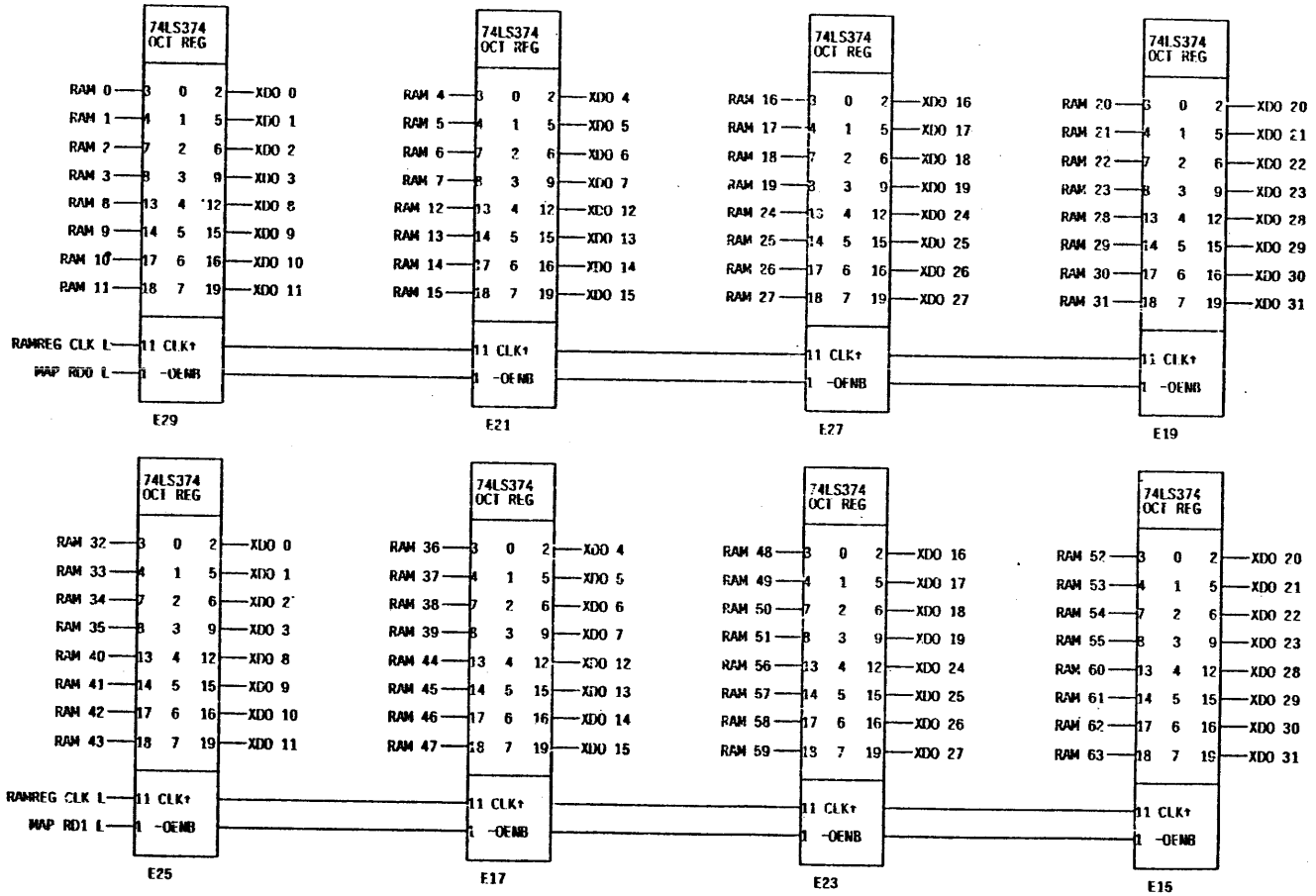

22 ohm
SERIES DIP
898-3-R22
RAM BFR 0
RAM BFR 1
RAM BFR 2
RAM BFR 3
RAM BFR 4
RAM BFR 5
RAM BFR 6
RAM BFR 7
RAMD A0
RAMD A1
RAMD A2
RAMD A3
RAMD A4
RAMD A5
RAMD A6
RAMD WE L
C1402


2118 16KX1 RAM
RAMC A0
RAMC A1
RAMC A2
RAMC A3
RAMC A4
RAMC A5
RAMC A6
-RAMC RAS
-RAMC CAS
-RAMC WE
A0
A1
A2
A3
A4
A5
A6
Din
Dout
-RAS
-CAS
-WE
RAM 32
RAM 33
RAM 34
RAM 35
RAM 36
RAM 37
RAM 38
RAM 39
RAM 40
RAM 41
RAM 42
RAM 43
RAM 44
RAM 45
RAM 46
RAM 47
XDI 0
XDI 1
XDI 2
XDI 3
XDI 4
XDI 5
XDI 6
XDI 7
XDI 8
XDI 9
XDI 10
XDI 11
XDI 12
XDI 13
XDI 14
XDI 15
C30011
C28011
C26011
C24011
C22011
C20011
C18011
C16011
C29011
C27011
C25011
C23011
C21011
C19011
C17011
C15011

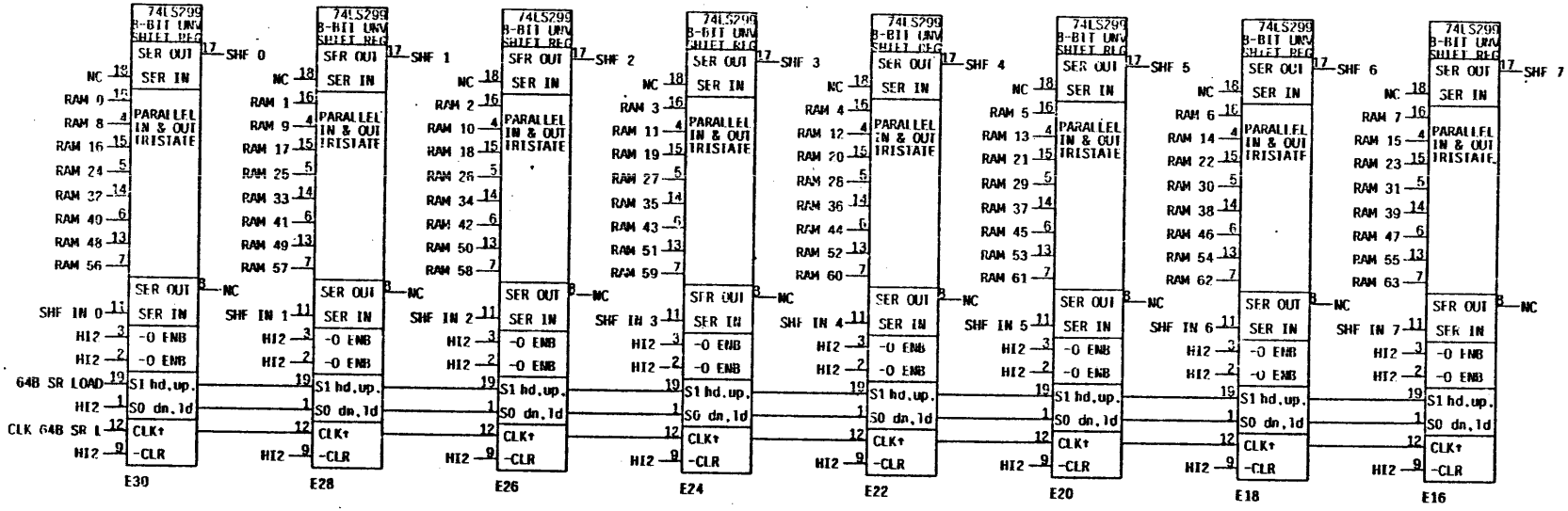

25LS2539
4-DECODE
0
1
2
3
NC
NC
MAP RD0 L
MAP RD1 L
READ
ADR 0
GND
MAP RQ L
HI4
SEL1
SEL0
-OUT ENB
-ENB
LO/-HI
C12
CLKO RAS
74S37
C13
RAS 0-1 L
RAS 2-3 L
PROC SYNC
PROC CYC L
22 ohm
SERIES DIP
899-3-R22
RAMA RAS L
RAMB RAS L
RAMC RAS L
RAMD RAS L
CAS 0-1 L
CAS 2-3 L
RAMA CAS L
RAMB CAS L
RAMC CAS L
RAMD CAS L
B1302
DELAY
20NS TMCS
TD100
INPUT
20NS
40NS
60NS
80NS
100NS
CAS MPX TIME
D11



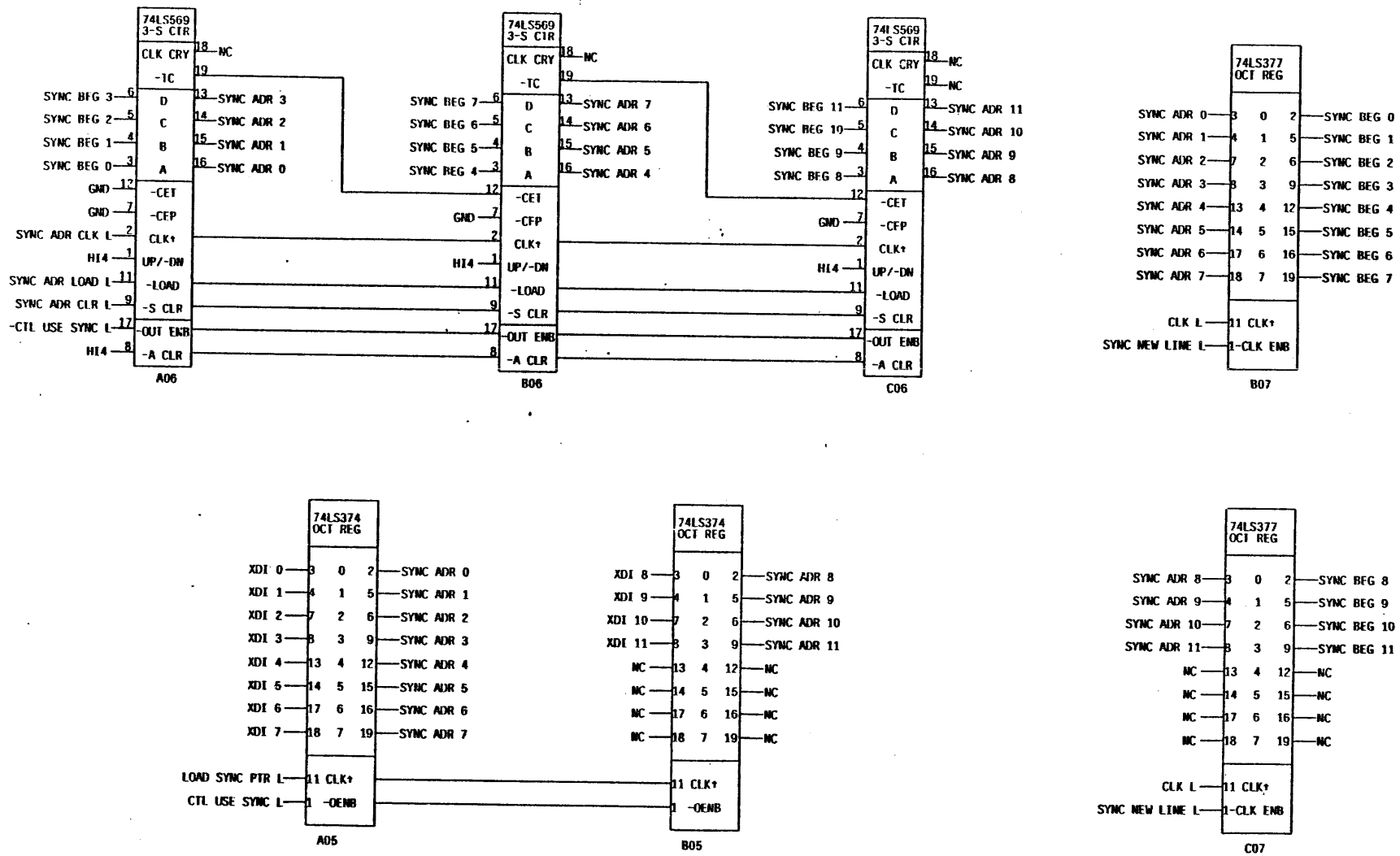
LISPM TV	Video Memory: Row D	7-DEC-1980 19:53	AI: CADRTV; RAMD



LISPM TV	Ram Output Registers	7-DEC-1980 23:02	AI: CADRTV; RAMREG



LISPM TV	64-bit Video Shift Register	7-DEC-1980 22:52	AI: CADRTV; RAMSHF

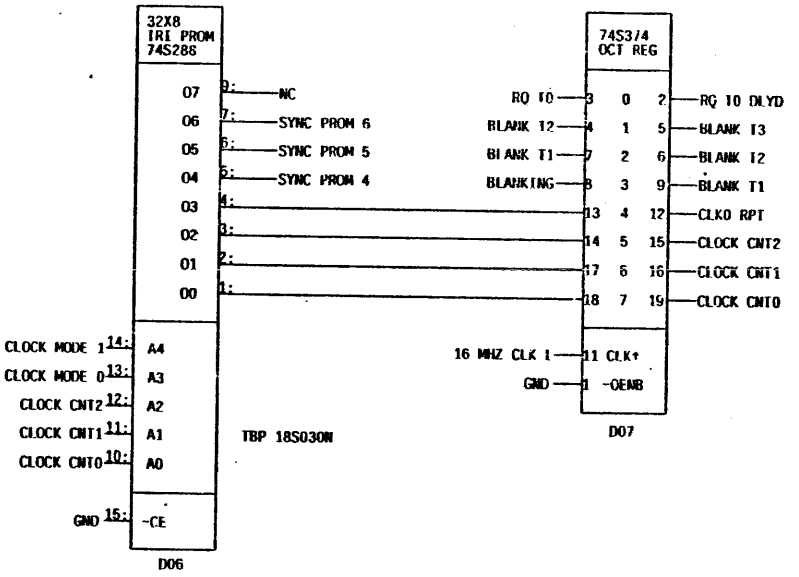


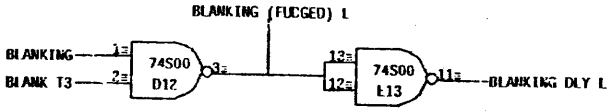
LISPM TV	Sync Program Address	7-DEC-1980 22:53	AI: CADRTV; SYNADR

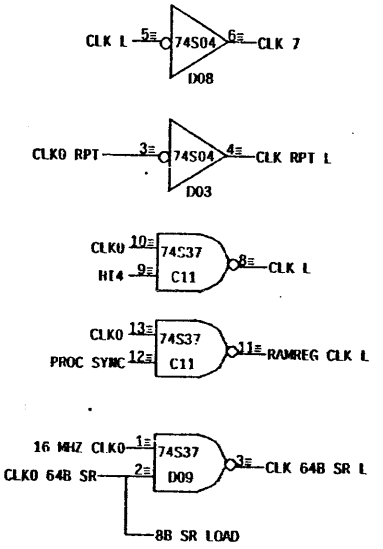
ON CADRTV;NXBCTL

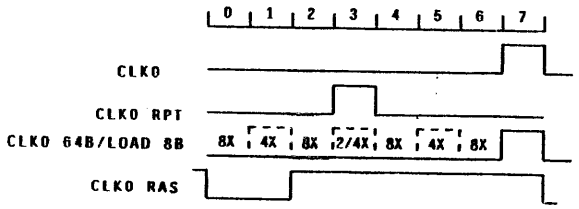
SYNC PROM

4 CLKO
5 CLKO 65B SR
7 CLKO RAS
7 ---





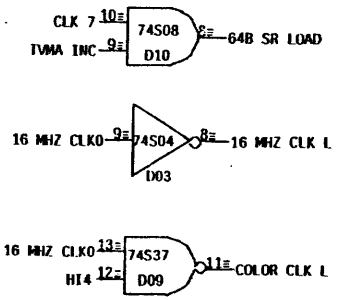




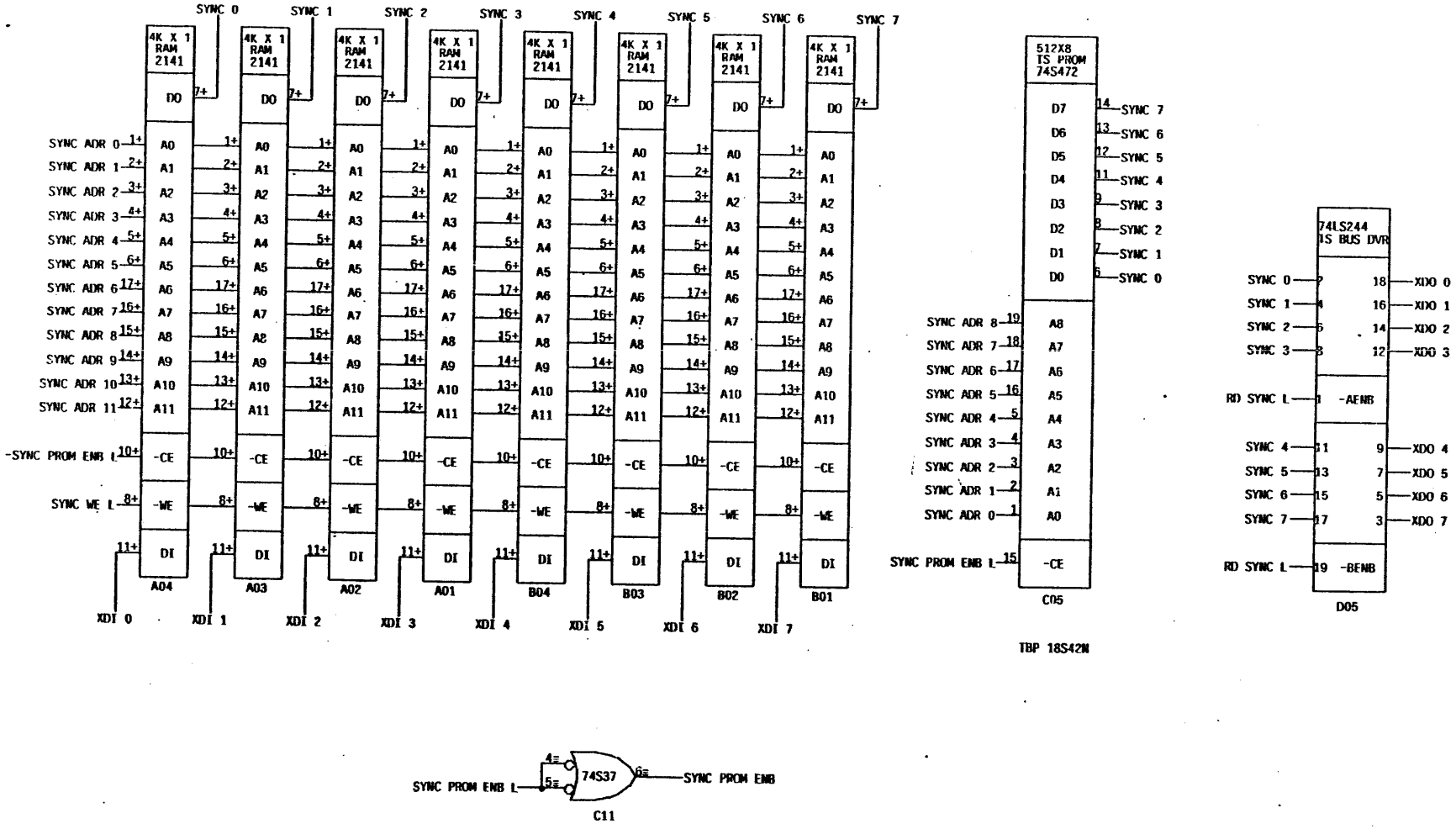
CLOCK MODE

10	MHZ.	MODE
--	----------	
00	64	CPI
01	32	M4408
	(OR 16 MHZ COLOR)	
10	12	525 LINE
11	12	COLOR

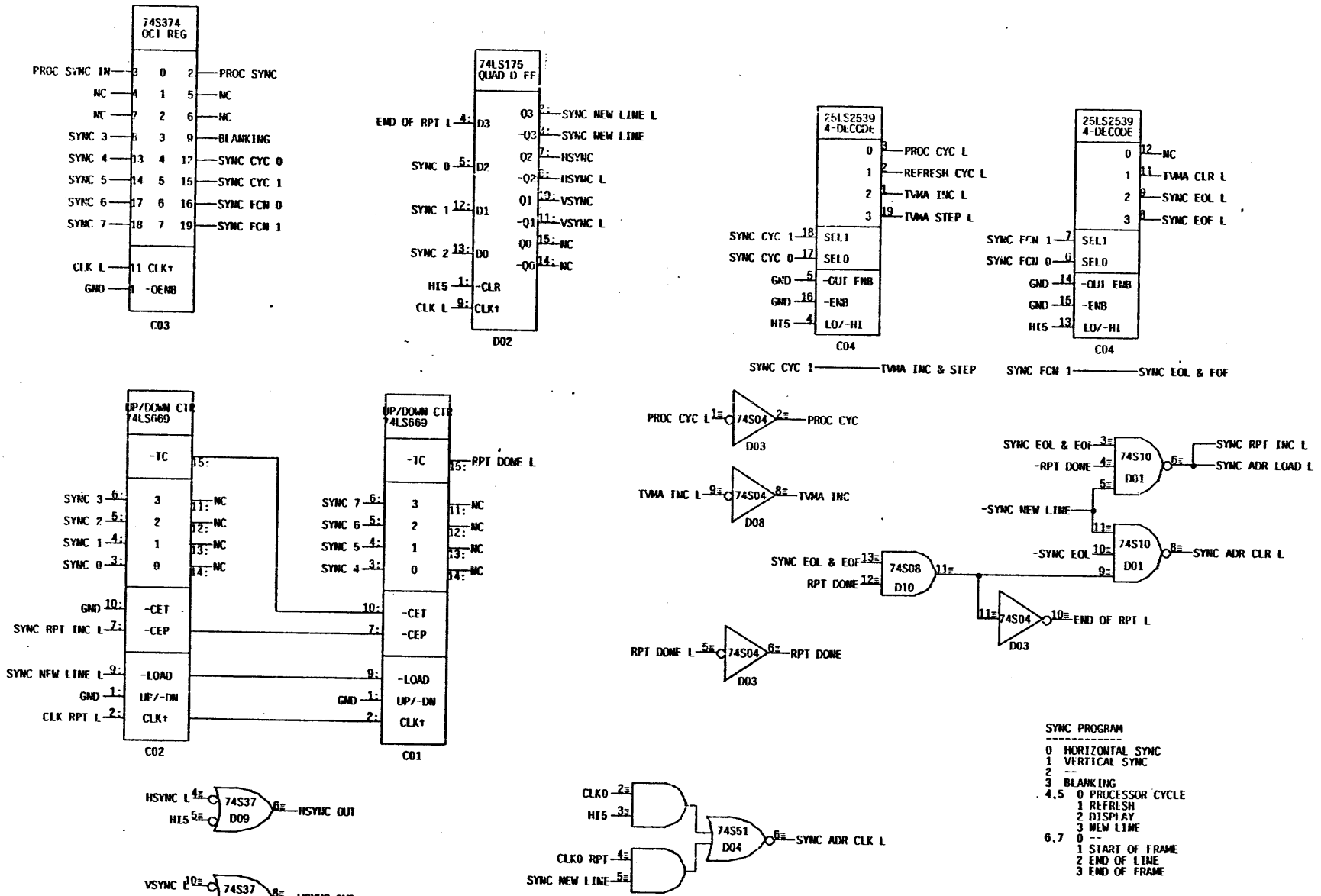
CLK 7 DELAYED FROM CLKO
ALLOW FOR HOLD TIME OF 74S299



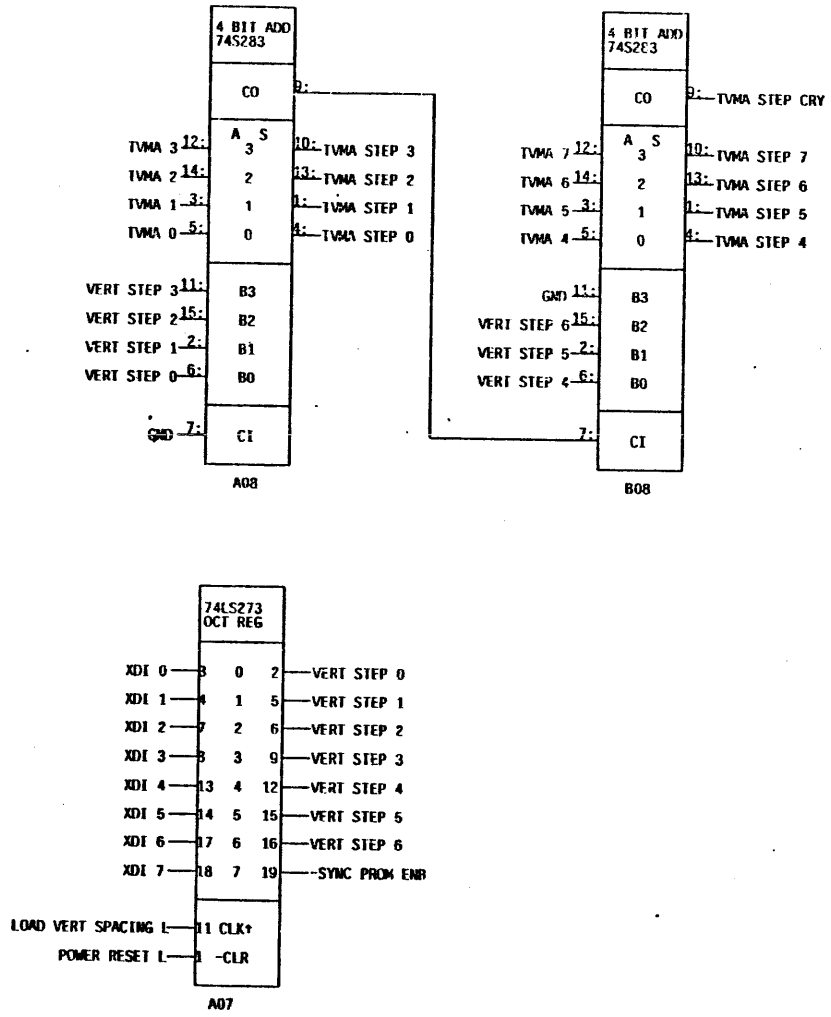
LISPM TV	Sync Clocking	7-DEC-1980 23:27	AI: CADRTV; SYNCLK



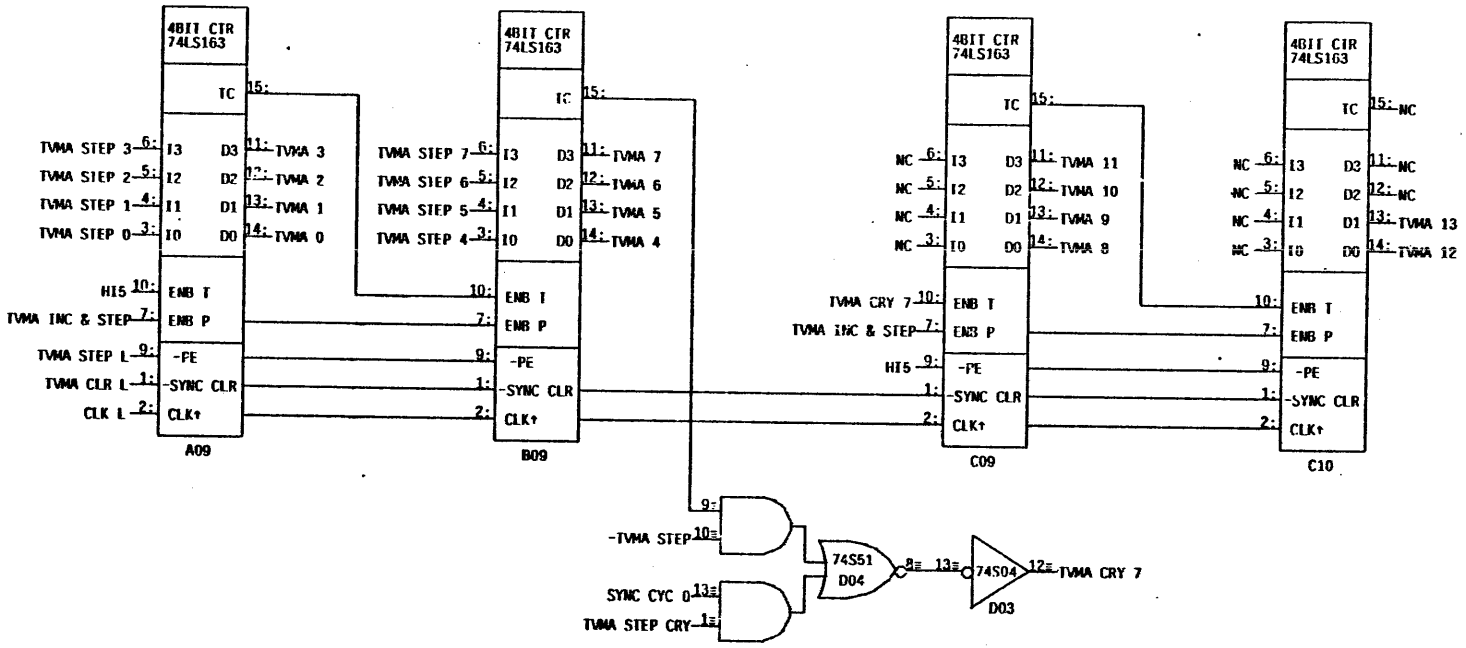
LISPM TV	Sync Program Memory	7-DEC-1980 23:31	AI: CADRTV; SYNRAM



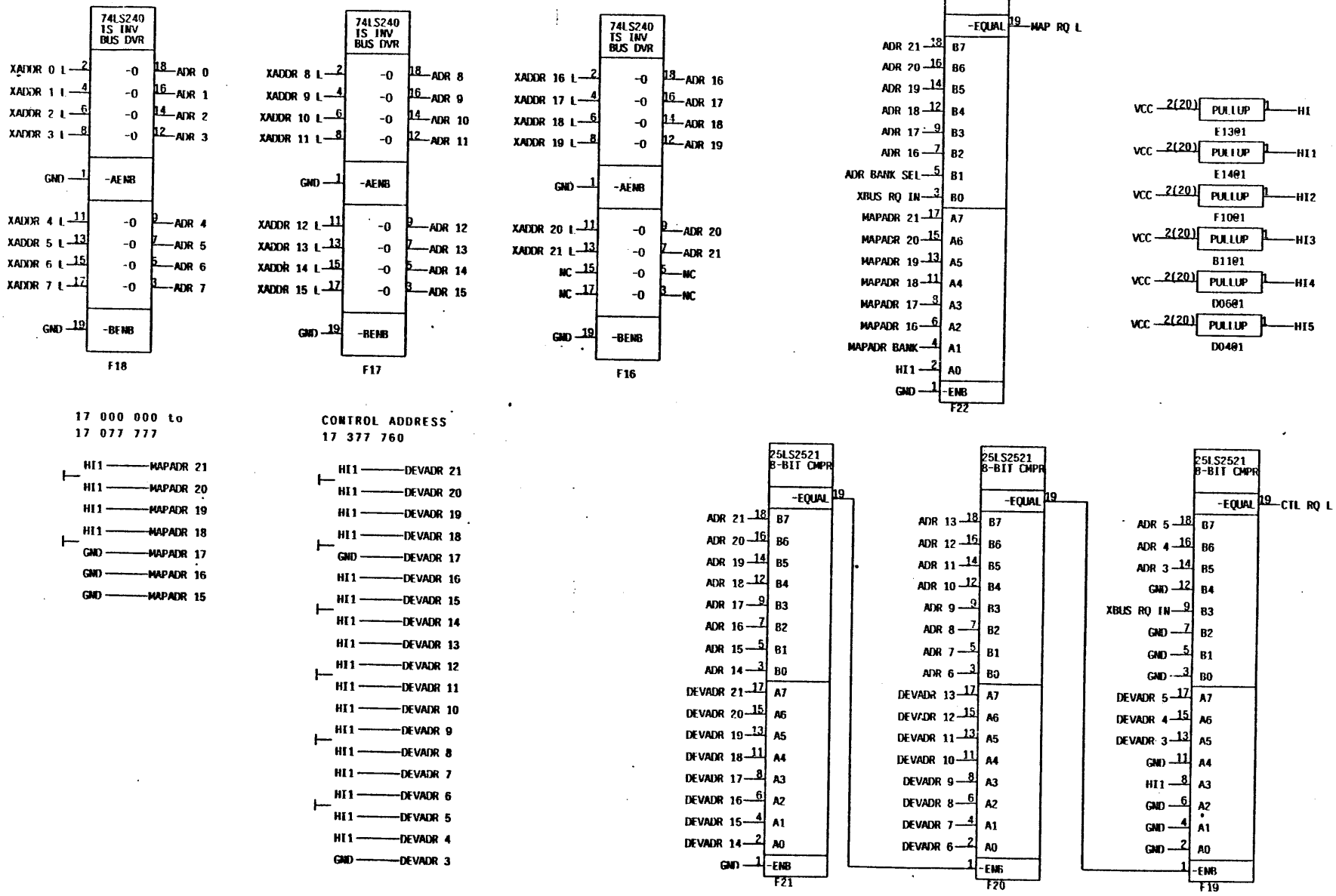
LISPM TV	Sync Program Reg & Repeat	7-DEC-1980 22:57	AI: CADRTV; SYNREG



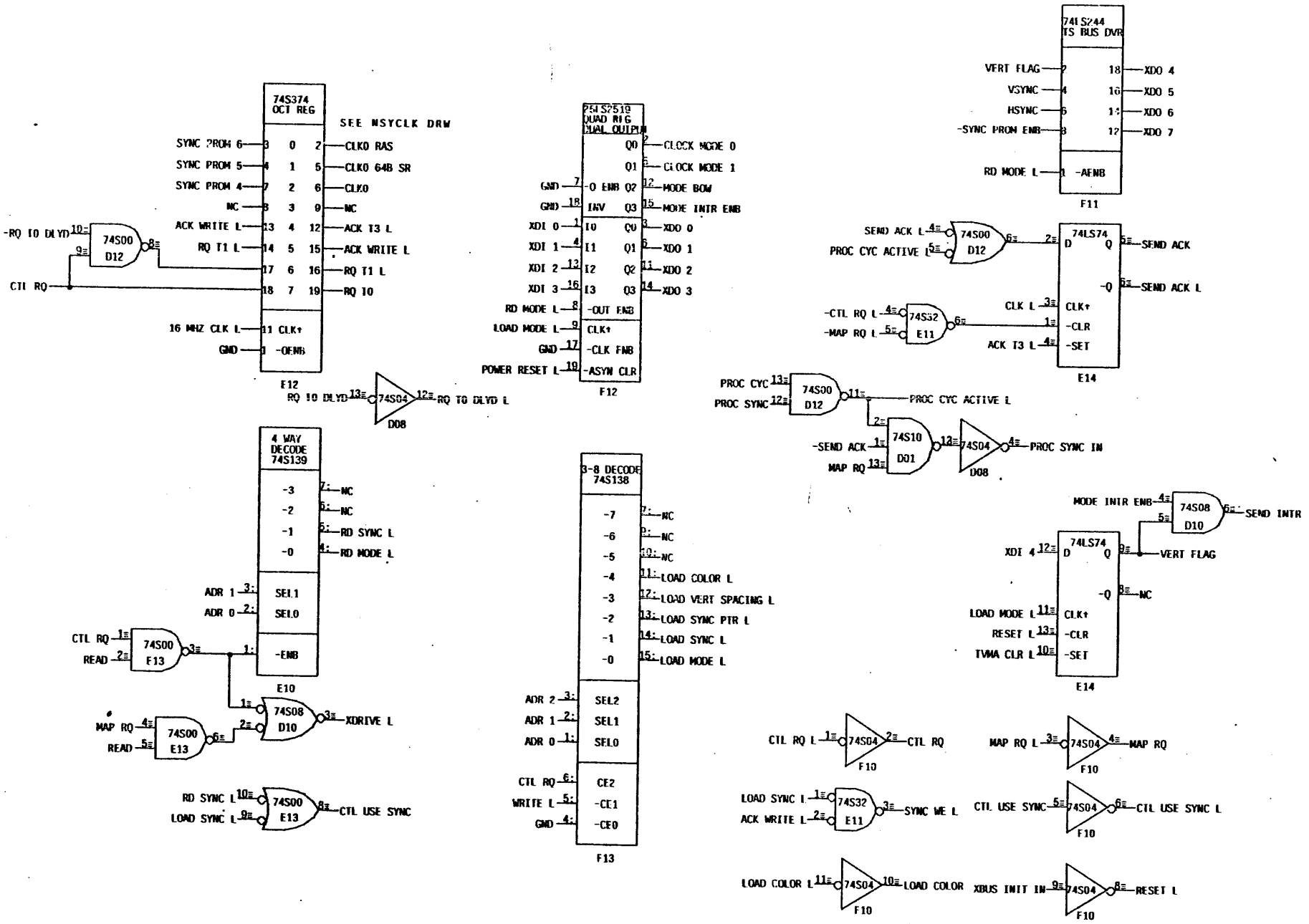
LISPM TV	TV Mem Address Adder	7-DEC-1980 22:58	AI: CADRTV; TVINC



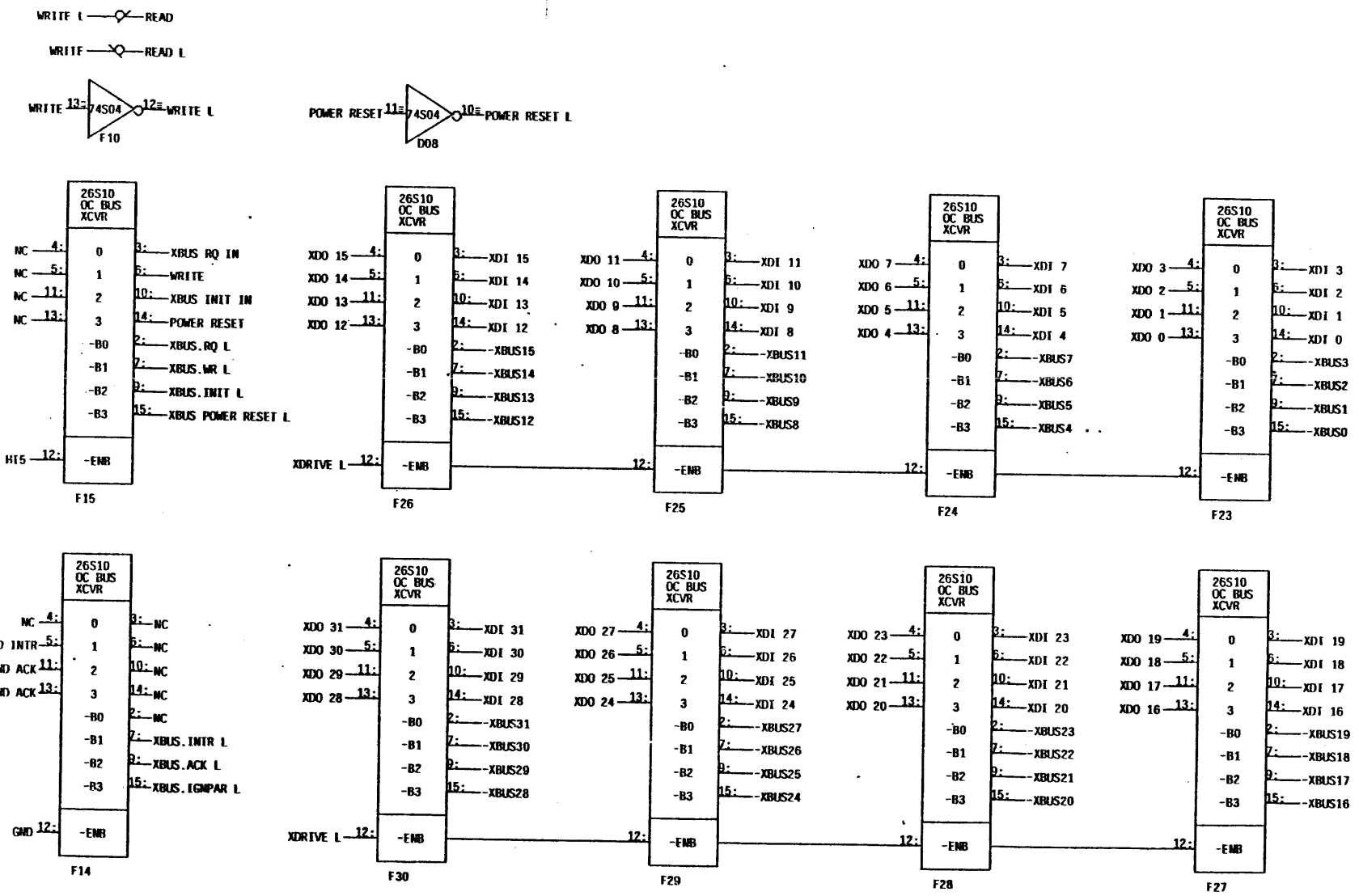
LISPM TV	TV Mem Address Counter	7-DEC-1980 23:02	AI: CADRTV; TVMA



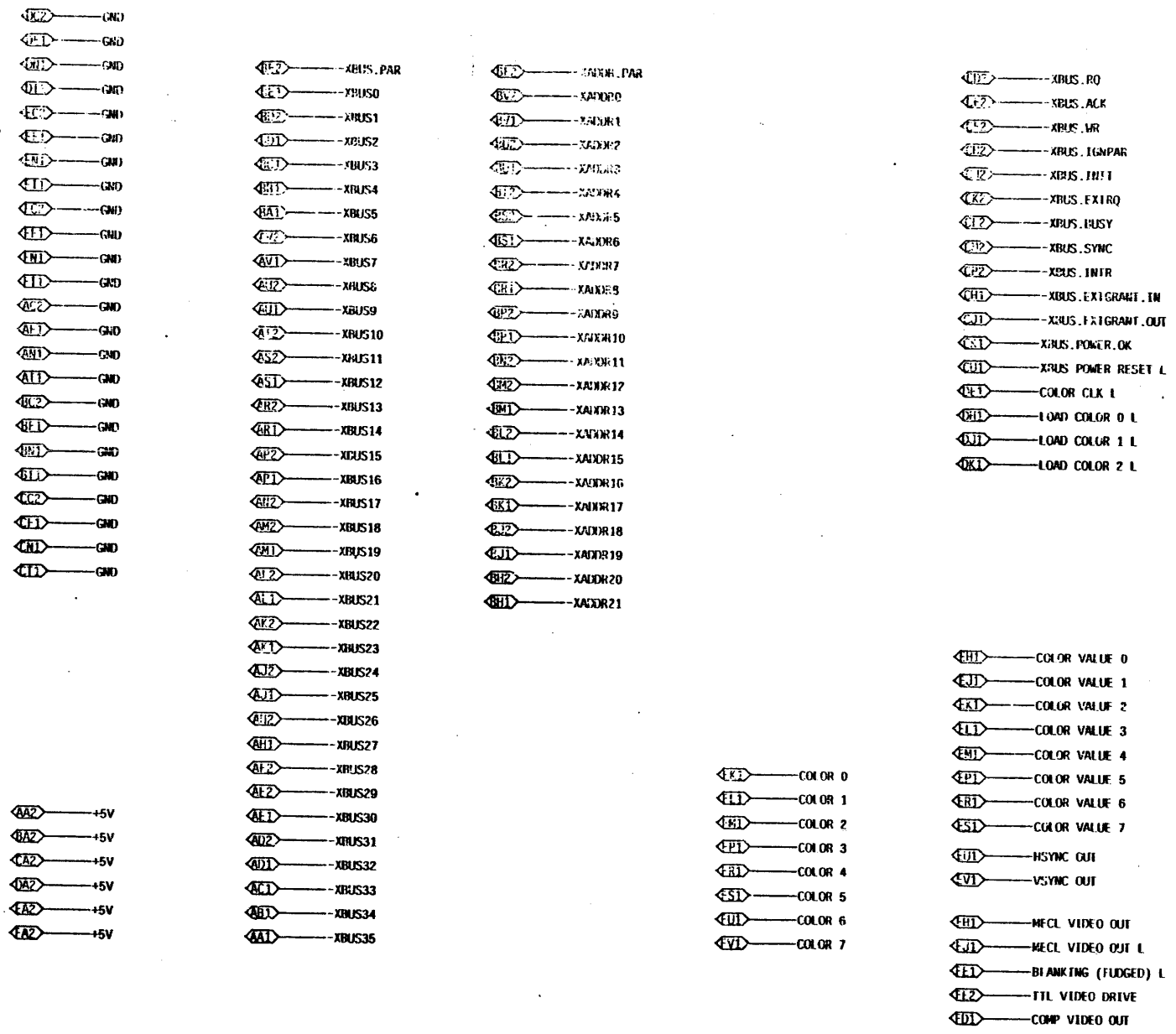
LISPM TV	XBus Address Selector	10-DEC-1980 10:51	AI: CADRTV; XBADR



LISPM TV	Mode Reg and Xbus Control	7-DEC-1980 23:05	AI: CADRTV; XBCTL



LISPM TV	Xbus Data Transceiver	7-DEC-1980 23:04	AI: CADRTV; XBDATA



LISPM TV	Backplane Connections	7-DEC-1980 23:01	AI: CADRTV; XBUS