HD/CTC

Preliminary Manual

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INTRODUCTION

The HD/CTC is an IEEE 696/S-100 compatible intelligent slave combining a hard disk and cartridge tape controller on one board. With a Z80A CPU (Z80B optional) and up to 48K-bytes of mixed EPROM/RAM the HD/CTC is capable of providing the high performance mass storage management required in "state of the art" system designs. Additionally this intelligence allows easy integration of the HD/CTC into any system since all host level communications take place using high level commands. This feature simplifies the software requirements and removes any unnecessary overhead from the host CPU, permitting the system to operate in a more efficient manner.

The HD/CTC provides a unique FIFO buffer interface to the host system. This buffer appears as an I/O port to the host and therefore will not cause memory conflicts with existing boards or require any cumbersome "memory mapping" techniques to interface. The host can initiate a read, write, or backup operation and place the appropriate data in the FIFO. While the HD/CTC is performing the operation the host system is free to execute other system functions such as responding to user requests or setting up the next required hard disk access. Once the HD/CTC has completed the current operation and placed the appropriate data in the FIFO the host system is notified by either a system interrupt or the setting of a status flag. At this time the host can retrieve the result data at full speed in a "burst" or block mode (limited only by the access time of the static RAM buffer) and initiate the next operation.

Note that during the time that data is being transferred between the FIFO and one "side" (the host or HD/CTC) of the system, the other side is free to perform normal operations. This architecture minimizes the time required to execute data transfers and allows the host and slave to operate independently of each other. Quite different host and slave designs can be combined using this method, permitting the use of varied clock speeds and 8/16 bit processors.

Combine the performance capability of the HD/CTC with the cost effectiveness of an integrated tape cartridge controller on the same board and you have a truly state of the art S-100 board. The standard version being able to manage two hard disk drives and one stop-start cartridge tape drive makes the HD/CTC ideal for a wide range of applications requiring both high speed disk storage and tape backup support.

Add to these features the availability of operating system level software from Teletek to support CP/M, TurboDOS, and Micro Mikes MDZ/OS, and you get the solution for your system's mass storage management problems.

SPECIFICATIONS

CPU

Z80A (4MHz) standard, optionally Z80B (6MHz) available.

MEMORY

6Kbytes **EPROM** standard: 2Kbytes (2716) Monitor, 4Kbytes (2732) Formatter.   Optionally, 16Kbyte devices (27128) allowed.

4Kbytes static RAM standard: 2Kbytes (2016) FIFO, 2Kbytes (2016) scratchpad. Expansion allowed for future 8Kbyte devices.

HOST INTERFACE

HD/CTC occupies four I/O ports with the following addressing options: 30-33H (standard), 80-83H, B0-B3H, F0-F3H.

Uses the following S-100 signals:

Pin#	Signal
44	sM1
45	sOUT
46	sINP
96	sINTA
78	pDBIN
77	pWR*
73	INT*
75	RESET*
54	SLAVE CLR*
49	CLOCK
	A0-A7
	DO0-DO7
	DI0-DI7
	+8 Volts @ 2.7A Max.
	+16 Volts @ 30mA Max.
	-16 Volts @ 50mA Max.
	GND

PERIPHERAL INTERFACE

Hard Disk: Two 5Mbits/sec, soft sector, ST506 compatible standard.   Other drives supported (including hard sector) up to 15Mbits/sec.

Tape Drive: One 1/4" DEI FUNNEL drive standard.   Other tape drives supported.

Forced air cooling required.

INSTALLATION

Upon receipt of HD/CTC, check the shipping package for any signs of abuse which may indicate possible damage. Check the board physically to look for any components which may have been damaged during shipping. If any diskettes were shipped with HD/CTC, check them for damage such as bending or signs of a sharp object being placed against the disk. Diskettes are quite fragile and any warping of the media surface will render the disk inoperative. Notify the shipper of any damage.

HD/CTC is ready for immediate use upon receipt. The only requirements are to establish the peripheral connections, plug the board into the S-100 bus, and install the operating system. The HD/CTC needs to be in a well ventilated area due to the high density of IC's on-board. Ideally, the board should be mounted vertically in a stream of air which will be moving across the face of the board. Whatever the mounting position, forced-air cooling is mandatory.

Peripheral Connections

For the standard ST-506 compatible drives supported the peripheral connections need only be flat ribbon cable with the appropriate crimp style connectors attached. One 34-pin daisy chain cable (for both drives) and one 20 pin data cable (for each drive) is needed for the 5 1/4" hard disks. One 50-pin cable will be needed for the cartridge tape drive. When constructing the cables make sure that pin 1 of each connector on the cable is aligned correctly. Bring peripheral cables neatly away from the HD/CTC with enough slack to prevent any tension from being applied to the board-cable connection.

The pin assignments for the hard disk connectors are shown on the next page. The 20-pin J3 connector on the extreme right side of the board is used for the drive A data cable, while J4 (to the left of J3) is used for drive B. The 34-pin J2 connector to the left of J4 is the daisy chain control cable that links to both drives A and B. These male connectors are keyed to allow use of similarly keyed female connectors. If keyed female connectors are not used, make sure that pin 1 of the cable is pointing to the left side of the board (the side with the voltage regulator) when it is installed.

It is possible to order pre-assembled cables meeting your specifications directly from Teletek. Contact Teletek for pricing and shipping information.

J-2 CONNECTOR PIN ASSIGNMENT

GND PIN	SIGNAL PIN	SIGNAL NAME
1	2	-Reduced Write Current
3	4	RESERVED
5	6	-Write Gate
7	8	-Seek Complete
9	10	-Track 0
11	12	-Write Fault
13	14	-Head Select 0
15	16	RESERVED
17	18	-Head Select 1
19	20	-Index
21	22	-Ready
23	24	-Step
25	26	-Drive Select 1
27	28	-Drive Select 2
29	30	-Drive Select 3
31	32	-Drive Select 4
33	34	-Direction In

J-3,J-4 CONNECTOR PIN ASSIGNMENT

GND PIN	SIGNAL PIN	SIGNAL NAME
2	1	-Drive Selected
4	3	RESERVED
6	5	RESERVED
8	7	RESERVED
	9,10	RESERVED
12	11	GND
	13	+MFM Write Data
	14	-MFM Write Data
16	15	GND
	17	+MFM Read Data
	18	-MFM Read Data
20	19	GND

I/O Addressing

Teletek's HD/CTC occupies a cluster of four I/O ports, the starting address of the cluster being a jumper selectable option. The standard HD/CTC provides the ability to address the I/O cluster starting at either 30, 80, B0, or F0 hex. The option jumpers A0 and A1 determine this address as follows:

A0	A1	Location
0	0	30-33H
1	0	80-83H
0	1	B0-B3H
1	1	F0-F3H

Note: A1 means the jumper is in place, A0 means the option is left open.

The following options are set according to the operating system being used. Check the operating system documentation for information pertaining to these options.

Interrupt Daisy Chain

The HD/CTC is capable of providing a Zilog mode 2 interrupt vector on the data bus during the interrupt acknowledge cycle of the host system. The HD/CTC can also incorporate itself into the Zilog interrupt daisy chain. There are two pins on the board corresponding to the interrupt enable in (IEI) and the interrupt enable out (IEO) functions. These pins are compatible with those provided on other Teletek products. The system board having the next higher priority than HD/CTC should have its IEO pin connected to the HD/CTC's IEI pin, and in the same manner the HD/CTC should have its IEO pin connected to the IEI pin of the next lower priority board in the system.

Option A

This option determines whether the HD/CTC is to be used in an interrupt mode or a polled mode of operation with respect to the host system. If jumper option A is in place, the HD/CTC will interrupt the system host when a task has been completed.

If jumper option A is removed, the controller operates in a polled mode.

Option B

Option B determines whether the bus signal pDBIN (pin 78) is used to qualify the return of the Zilog mode 2 interrupt vector to the host system. If jumper option B is in place, the interrupt vector is returned to the host system only when sINTA (pin 96) has been received, pDBIN is active high, and IEI from the interrupt daisy chain is high.

If jumper option B is removed, pDBIN is no longer used to qualify the interrupt vector return. The vector will be placed on the system data bus when both sINTA and IEI are high.

Operating System Software

At this point the cables have been connected between the peripherals and the HD/CTC, the HD/CTC configured for the proper I/O addressing, and any options required by the operating system enabled. An operating system disk incorporating the HD/CTC that is capable of booting on a floppy drive is normally provided. The general procedure will be to boot the floppy disk system and initialize the hard disk parameters using a utility program provided. Once this has been completed the hard disk drive(s) being used may be initialized. The system can now be configured as desired, booting from either floppy, hard disk, or cartridge tape. Depending upon the requirements, the standard boot EPROMs provided may need to be exchanged for custom versions. Consult the operating system documentation for further information.

THEORY OF OPERATION

The Hard-Disk, Cartridge-Tape Controller can control both a hard disk such as the Seagate ST-506, and a cartridge tape drive such as the DEI Funnel. With on-board intelligence, the controller relieves the host CPU of most of the overhead involved in transferring data to either drive. The host CPU passes commands and data via a FIFO buffer and the on-board CPU then performs the necessary operations on the appropriate drive.

Data are stored utilizing MFM encoding on both tape and hard-disk in a format that embeds an identification in the data sector. This method provides the maximum data storage on the drive consistent with reliable operation. A 16-bit CRC character is appended to each sector to detect errors.

System I/O Ports

The four port cluster that the HD/CTC occupies in the system I/O space is used for communications between the HD/CTC and the host system. Each of the four port locations performs a different function, which is determined by either a read or a write operation to a particular port. These functions are summarized in the following tables:

READ OPERATION

H0	Status port
H1	FIFO data
H2	No response
H3	No response

WRITE OPERATION

H0	Reset controller
H1	FIFO data
H2	Generate controller interrupt
H3	Reset S-100 interrupt request

Note: H0 refers to the I/O address assignment + 0, H1 refers to address + 1, etc.

Status Register

The status byte returned by the controller has the following bit assignments:

Bit	Function
7	Controller REQUESTs service from Bus Master
6	Controller is BUSY, do not disturb
5	Flag, set by the on-board CPU to aid in handshaking with the host. Indicates controller is READY to serve master. This is bit 1 of the HD/CTC Control Register.
4	Flag, set by the on-board CPU to indicate that ERRORs have occurred.
3-0	Not used, no meaning

Note: all status signals are active-high.

HD/CTC Memory Addressing

The Z-80 CPU on-board the controller accesses four devices within its 64k-byte address space:

Address	Device
0000-3FFFH	EPROM, either a 2716, 2732, 2764, or 27128
4000-7FFFH	RAM, a 2k-byte device for the standard board
8000H	Load FIFO low-order address register
8001H	Load FIFO high-order address register
8002H	Read or Write FIFO data
C000H	Write to on-board control register

If an EPROM less than 16k-bytes is used, it will appear multiple times within the address space of 0-3FFFH. Similarly, the 2k RAM appears 8 times within its 16k-byte address space. To function correctly, the on-board monitor must be addressed to function starting at 0000H. Assume the RAM starts at 7800H and ends at 7FFFH. This allows future use of a larger RAM without extensive software modification.

Similarly, the control functions which are memory-mapped will appear numerous times within the 16k-byte memory block. To avoid problems, only address these functions at 8000H to 8002H.

Note: The Non-Maskable Interrupt (NMI) is used by the host system to get the attention of the HD/CTC Z-80 CPU. Thus a NMI service routine starting at address 66H must be provided which responds to a host system request.

HD/CTC ROM

The on-board ROM (or EPROM) can be a 2716, 2732, or 2764 for a size from 2K to 8K bytes. Depending on the ROM used, jumpers E-1, 2, and 3 may need to be changed. The following table lists the requirements:

EPROM	JUMPER
2716	E-2 to E-1
2732	E-2 to E-3
2764	E-2 to E-3

HD/CTC RAM

The on-board scratch-pad memory for the CPU can be either 1K or 2K bytes in size. Jumpers E-4, 5, and 6 must be set accordingly.

RAM	JUMPER	
1k	E-5 to E-4	(4118)
2k	E-5 to E-6	(6116, 2016)

FIFO RAM

The RAM buffer for the FIFO can be either a 2k or 4k-byte device. Jumpers E-7, 8, and 9 must be set, and a suitable socket used depending on the RAM.

RAM	JUMPER	SOCKET
2k	E-8 to E-7	24-pin
4k	E-8 to E-9	28-pin

FIFO Access

The Z-80 CPU accesses the FIFO via memory addresses 8000, 8001, and 8002 when the FIFO function select lines are set high (these lines are bits 0 and 1 of the cartridge-tape control register). When reading or writing the FIFO, the FIFO address counter will automatically increment to the next FIFO data location after the completion of the present read or write operation. To provide random access capability, the address counters can be preset to a desired starting address and the FIFO data at that address accessed.

The FIFO uses an 11 or 12-bit address, depending on the size of the associated RAM. The CPU must perform two write operations to load the desired FIFO address: a low-order byte, and a high-order nibble. Together, these will become the FIFO address.

Load the desired FIFO address low byte first, then the high nibble. The low-order byte will increment once when the high-order nibble is loaded. Therefore, the value loaded into the low-order byte must be one less than the desired value to accommodate the increment.

To load the FIFO address counters, output the desired low-order byte less one, to memory address 8000H. Then output the high-order nibble (in bits 0-3) to memory address 8001H. The FIFO data at that address is now available. The low-order byte must be one less than desired because it will be incremented once when the high-order nibble is output. Note that for a 2k byte FIFO RAM, only 11 bits of address are meaningful, and the twelfth bit will be ignored.

Note that a load register pair to location 8000H will automatically load the address counters in one instruction. Remember that the final low-order counter value will be one more than that loaded by the register pair. Using this method, a register pointer can be used to keep track of FIFO data as needed.

The on-board CPU can access FIFO sequentially by reading or writing to location 8002H. The FIFO address counters will automatically increment after each operation, providing sequential access to the FIFO data.

HD/CTC Control Register

This register (located at memory address C000H) controls the data transfer controller (formatter), and other on-board functions. **These** are defined below.

Bit	Active State	Function
0	HIGH	Enables the cartridge-tape and hard-disk write and certain other control lines. This bit is reset on power-up and any slave-clear or software reset. After reset, this bit must only be set after the cartridge-tape and HD/CTC control registers have been initialized.
1	HIGH	BUSY. This bit is set by the CPU to indicate to the S-100 bus master that the CPU is busy and can not be accessed.
2	HIGH	HARD-DISK data transfer select. When LOW, the cartridge-tape drive data transfer is selected. This bit is set prior to any read or write to a drive.
3	LOW	Drive to FIFO data enable. When active, the formatter can transfer data from the drive to the FIFO.
4	-	Sequencer option 0, see below
5	-	Sequencer option 1, see below
6	HIGH	WRITE GATE. Enables the formatter to write data from the drive.
7	HIGH	READ GATE. Enables the formatter to read data from the drive.

Options 0 and 1 are defined by software stored in the sequencer EPROM. Option 0 and 1 select a 1k byte segment of the formatter EPROM. Because address A-7 from the FIFO address counter is skipped, the actual length of sector data can be up to 2k bytes including the sync field, header and trailing fill characters.

HD/CTC SEQUENCER EPROM

The following functions are stored in this EPROM:

Option 0	Option 1	Function
0	0	Read a sector
1	0	Write a sector
0	1	Read an ID
1	1	Format

Option (0,0) reads a sector into the FIFO RAM. Option (1,0) writes a sector from the FIFO RAM. Option (0,1) reads the ID of a sector and sets the ID-FOUND flag. The sector ID is stored in a different location in the FIFO than the normal sector, allowing the CPU to set up a sector and then finding the sector just before the desired one.

The remaining option, (1,1), formats the sector. It must be different than a normal write operation because the sync and trailing fill gaps must be longer to prevent over-writing the sector following during normal operation.

HD/CTC I/O Port Assignments

The following devices are addressed by the HD/CTC Z80 CPU independent of the S-100 bus:

Address	Function
00H	Write-only hard-disk control register
04H	Read-only hard-disk drive status
08H	Read-only cartridge-tape status
0CH	Write-only, cartridge-tape control

Address	Function
10H	Z-80 CTC
14H	Reset Bus Master request to CPU, read or write
18H	Initiate S-100 bus interrupt, read or write
1CH	Write-only CT-HD control register

Hard-Disk Control Register (port 00H)

This register controls the select and direction functions of the hard disk. Only one drive select line should be active at any one time. Thus immediately after a reset, the on-board CPU must set all select lines to their inactive high state. The following table identifies the function of each bit of this register.

Hard-Disk Control Register Bit Assignment

Bit	Active State	Function
0	LOW	Drive Select 1
1	LOW	Drive Select 2
2	LOW	Drive Select 3
3	LOW	Drive Select 4
4	LOW	Head Select 0
5	LOW	Head Select 1
6	LOW	Head Select 2
7	LOW	Seek direction*

Note: When LOW, head moves in to center of disk surface after seek pulse. When HIGH, head moves out.

Hard-Disk Status (port 04H)

The status of the hard-disk drive is made available on this read-only port.

Bit	Active State	Function
0	LOW	Drive 1 select acknowledge
1	LOW	Drive 2 select acknowledge
2	HIGH	ID field has been read and is in FIFO
3	LOW	Drive READY
4	LOW	INDEX pulse (about 200 uSec duration)
5	LOW	Write Fault
6	LOW	Head over TRACK 0 (Outer-most track)
7	LOW	SEEK COMPLETE

Cartridge-Tape Status (port 08H)

The status of the cartridge-tape drive, and the on-board formatter CRC check are available on this read-only port.

Bit	Active State	Function
0	HIGH	Formatter operation completed
1	HIGH	CRC error detected
2	-	External error-correction detector
3	LOW	Cartridge installed
4	LOW	Tachometer pulse (11.25 deg. of rotation)
5	LOW	Lower tape hole sensed
6	LOW	Upper tape hole sensed
7	LOW	SAFE plug installed, write disabled

Cartridge-Tape Control Register (port 0CH)

This register provides both cartridge-tape drive and FIFO control signals.

Bit	Active State	Function
0	-	FIFO select 0 (see below)
1	-	FIFO select 1 (see below)
2	LOW	Track-select 0-select desired tape track
3	LOW	Track-select 1-select desired tape track
4	LOW	Read threshold-select 0
5	LOW	Read threshold-select 1
6	LOW	Read threshold-select 2
7	LOW	GO. Tape motion control enabled

FIFO Function Select

Bits 0 and 1 of the Cartridge-Tape Control Register control the function and access of the on-board FIFO buffer. The following table outlines the four available functions.

Bit 0	Bit 1	Function
LOW	LOW	The S-100 Bus Master can read or write the FIFO buffer.
HIGH	LOW	Data can be transferred between a drive and the FIFO under the control of the formatter.
LOW	HIGH	The interrupt vector to the Bus Master can be read during interrupt acknowledge or an S-100 FIFO read operation without incrementing the FIFO address counters.
HIGH	HIGH	The on-board CPU can load the FIFO address counters to provide random as opposed to sequential access of the FIFO, and access the FIFO data.

Z-80 CTC (port 10H)

The CTC is used to generate the cartridge-tape write signal, hole-sensor reference frequency, and servo reference frequency. The remaining channel can be used as an interrupt-driven real-time clock for error time-out or other uses. The following paragraphs describe the set-up and function of each channel.

CTC Channel 0

Channel 0 of the CTC is used to generate the hole-sensor reference frequency of 20 kHz. Because the CTC does not generate a square wave which is required by the drive, a 74LS74 divides the channel output by two. Thus this channel provides an output frequency of 40 kHz. Set up the channel in the counter mode, with a time constant of 48.

CTC Channel 1

Channel 1 of the CTC generates a clock whose frequency is two times the data rate of the cartridge-tape system. Nominally this frequency is 480 kHz. The input to channel 1 is 1/2 the CPU clock frequency, 1.92 MHz. Set up this channel in the counter mode, time constant of 4.

CTC Channel 2

This channel generates the servo reference frequency of 1 kHz. Again, a counter divides the channel output to create a square wave. Thus the channel output is 2 kHz. Set up channel 2 in the timer mode, with a pre-scaler of 16, and a time constant of 120. The output will then be 2 kHz.

CTC Channel 3

The input of channel 3 connects to a counter whose input is the output of channel 2. The frequency available to channel 3 is one-eighth that from the output of channel 2. In the standard product, the output of channel 2 is 2 kHz, and the 1/8 count output is 250 Hz. Thus for a one-second interrupt, channel 3 can be set to the counter mode, with a time constant of 250. For a 100 mSec output, the time constant would be 25.

HD/CTC CPU NMI Reset (port 14H)

Any read or write of port 05H will reset the host system Non Maskable Interrupt request to the on-board CPU. This should be performed on entry to the NMI service routine at 66H. Simply do an output to port 05H. The output data are inconsequential.

HD/CTC CPU to Host System Interrupt (port 18H)

Any read or write of port 06H will initiate an interrupt to the S-100 bus master if option A is jumpered. The FIFO function should be set to Interrupt response, and the FIFO address counter set to the interrupt vector data. If option A is not jumpered, the on-board CPU waits for the bus master to acknowledge the polled request.

CT-HD Control Register (port 1CH)

This register controls functions on both the cartridge-tape and hard-disk drives.

Bit	Active State	Function
0	HIGH	Select read data from second hard-disk drive.
1	-	Flag, set by on-board CPU as needed to handshake with the host CPU.
2	LOW	LOW CURRENT, reset on cylinders equal to and greater than initialized parameter.
3	LOW	WRITE ENABLE. Enables writing on the hard disk.
4	LOW	STEP. The heads of the hard-disk move one cylinder for each pulse on this line, in the direction specified by bit 7 of the hard-disk control register. This pulse must be low for at least 10 uSec.
5	LOW	ERASE ENABLE, cartridge-tape drive. The tape will be erased when this is active.
6	LOW	REVERSE. The tape runs in reverse when this bit and the GO bit (Cartridge-Tape Control Register) are active.
7	LOW	WRITE ENABLE, cartridge-tape drive. Writing will commence on the tape.

Command and Message Protocol

The Bus Master and controller CPU transfer messages with a protocol based on interrupts to and from each device and the use of the BUSY and FLAG status bits. The following is a suggested implementation.

Idle State

When no operation is in effect on-board, the FIFO address counters are set to an unused FIFO area, and the HD/CTC CPU awaits an interrupt from the S-100 Bus Master. The Bus Master first checks the status port to determine if the controller is busy (bit 6 of the status, port H0). If not busy, the Bus Master sends a command and any operands to the FIFO address. When finished, the Bus Master then outputs any data to port H2 which interrupts the CPU. The Non-Maskable interrupt of the CPU is activated and the CPU enters the NMI service routine. In the service routine, the CPU resets the interrupt flip-flop by performing an output to port 05, sets the busy flag (bit 1 of the control register at C000H), then resets the FIFO address counter to the beginning of the unused FIFO area which now has a command from the Bus Master.

Depending on the command, appropriate action is taken and a result placed in the FIFO. The HD/CTC CPU sets the FIFO address to point to the interrupt vector, then sets the FIFO function select bits to the interrupt mode. An interrupt request is then made by performing an output to port 06. The BUSY flag remains set at this time. The S-100 Bus Master responds to the interrupt by interrupting the HD/CTC CPU again. This time the NMI service routine sets the FIFO address counter to point to the appropriate result data, and resets the BUSY flag. The Bus Master sees that BUSY is now reset and reads the data from the FIFO. The transaction is completed by the Bus Master writing a terminating command into the FIFO, and issuing one further interrupt request. This provides the final handshaking and the controller CPU again enters the idle state.

Controller Initialization

The first action of the Bus Master on power-up or reset is to initialize the controller. The Bus Master checks the status port to determine if BUSY is reset. If so, the Master outputs the initialization parameters. The CPU stores this data in its scratch pad memory, and then uses it whenever necessary.

Disk Format

The format on the disk consists of a synchronization field, an address mark, sector identification information, data, CRC, and fill bytes. The length and description are:

Synchronization field–	8 bytes of 00
Address Mark–	A1H (with missing clock)
Sync byte–	F8H
Sector status–	1 byte
Extra byte–	1 byte
Sector length–	1 byte
Cylinder low–	1 byte
'' high–	1 byte
Head–	1 byte
Sector #–	1 byte
Checksum of ID–	1 byte
Sector data–	512 bytes
CRC data–	2 bytes
Fill data–	50 bytes of B6H

During the format operation, a fill gap of 40 bytes is placed immediately after the index pulse prior to the first sector synchronization field. After the last sector (#16 on a Seagate-type drive), the fill character is written until the index pulse occurs.

SYSTEM SOFTWARE INTERFACE

The HD/CTC will occupy a block of four consecutive I/O ports, with the standard port addresses being 30h-33h. The functions of each port are as follows:

```
port0       input  = get controller status byte
            output = reset the controller
port1       input  = read data from controller FIFO
            output = write data to controller FIFO
port2       input  = not used
            output = interrupt the controller
port3       input  = not used
            output = clear 'Request' signal from controller
                          (see special note)
```

The status byte returned by the controller has the following bit assignments (all signals active high):

Bit	Name	Meaning
0-3		Not used
4	Error	Errors have occurred on the controller
5	Ready	Controller is ready to serve bus master
6	Busy	A command is in progress on the controller
7	Request	Controller requests service from bus master

NOTE: The form of the 'Request' signal depends on the option A jumper on the controller board. If option A is jumpered, Request will cause an S-100 interrupt when it goes high. If option A is open, the controller is in a polled mode of operation only. Thus 'wait for REQUEST from controller' means either waiting for an interrupt or polling the 'Request' status bit, depending on the option A jumper plug.

'Poll-wait' always means simple polling. Some portions of the controller protocol cannot be handled with interrupts.

INITIALIZATION SEQUENCE

```
hardware or software reset
reset REQUEST
pre-read status port (ignore contents)
delay 40 microseconds
poll-wait for controller BUSY
poll-wait for controller READY (will still be BUSY)

if ERROR
    then
            abort ... bad chips on controller
                    (most likely RAM, FIFO, or CPU)
    endif

output 16 bytes initialization data to controller FIFO
    (see definition under "Operating Parameters" below)

interrupt controller
wait for REQUEST from controller
reset REQUEST

if ERROR
    then
            interrupt controller
            poll-wait for READY from controller
            input error bytes from controller FIFO
                    (see definition under "Error Bytes")
            abort
    endif

interrupt controller
```

OPERATING PARAMETERS

These sixteen bytes of information are sent from the bus master to the **hard** disk controller during the initialization sequence. The **values** sent will remain in effect until (and only until) a hardware **or** software reset is received by the hard disk controller.

```
6 -—  byte 0     interrupt vector
7 —'  byte 1     option bit flags  (see below)
2 ——  byte 2     number drives currently on-line   (1 or 2)
      byte 3     number cylinders per drive          (low)
      byte 4       "        "       "      "          (high)
      byte 5     number heads (tracks per cylinder)
      byte 6     number bytes per logical block      (low)
      byte 7       "       "       "       "     "   (high)
      byte 8     step delay constant           (always F8 hex)
      byte 9     step rate                     (milliseconds)
      byte 10    cylinder settling delay constant (always F8 hex)
      byte 11    cylinder settling time        (milliseconds)
      byte 12    head settling time            (see note below)
      byte 13    head settling delay constant  (always 01)
      byte 14    low current boundry cylinder  (low)
      byte 15      "        "       "       "  (high)
```

Definition of **Option Bit Flags**

bit 0	blocking mode	0 = block is physical sector
		1 = blocking/deblocking
bit 1	track addressing mode	0 = physical track address
		1 = logical track address
bit 2	drive addressing mode	IF logical track addressing mode
		0 = 4-bit LUN, 20-bit block #
		1 = 24 bit block #
bit 3	write verification mode	0 = no verification
		1 = automatic read-back & verify
bits 4-7	reserved	MUST be zero

Computation of **Byte 12**:

byte 12 = ((head settling time in microseconds - 18 us) / 4 us) + 1

Example: suppose head settling time is 50 microseconds
```
byte 12 = ((50 us - 18 us) / 4 us) + 1
        = (32 us / 4 us) + 1
        = 8 + 1
        = 9          (if not integer, round UP)
```

GENERAL COMMAND STRUCTURE

ARBITRATION PHASE
        poll-wait for controller not BUSY and READY

COMMAND PHASE
        output command to controller FIFO
        interrupt controller
        wait for REQUEST from controller
        reset REQUEST

DATA PHASE   (optional depending on command)
        if NOT ERROR
            then
                        interrupt controller
                        poll-wait for READY from controller
                        transfer data to or from controller FIFO
                        interrupt controller
                        wait for REQUEST from controller
                        reset REQUEST
            endif

STATUS PHASE
        if ERROR
            then
                        interrupt controller
                        poll-wait for READY from controller
                        input error bytes from controller FIFO
                                (see definition under "Error Bytes")
            endif
        interrupt controller

AVAILABLE COMMANDS

Note: Write general code.   New commands will be added,
            commands may be re-numbered and command formats may
            change before the official release of this software.

    00 = **Prepare for Power Off**
            Clear dirty buffers
            Step heads to spindle (<u>beyond</u> last valid cylinder)

        do ARBITRATION
        do COMMAND with 1 byte:
            00   power off command
        do STATUS

    01 = **Rezero Unit**
            Clear dirty buffers
            Step heads to cylinder zero

        do ARBITRATION
        do COMMAND with 1 byte:
            01   rezero command
        do STATUS

    02 = **Clear Controller Buffers**
            Clear dirty buffers

            OPTIONS:
                bit 0   1 = flush buffers if possible
                bit 1   1 = forget buffers even if fatal
                             errors occur

        do ARBITRATION
        do COMMAND with 2 bytes:
            02   clear buffer command
            xx   option bits
        do STATUS

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04 = Operate on All Tracks of the Drive
        Step through every cylinder and head on the drive,
        doing the given function on every track selected.

        FUNCTIONS:
            00 = nop (just step through all tracks)
            01 = format each track

    do ARBITRATION
    do COMMAND with 3 bytes:
        04   all tracks command
        xx   function number
        xx   drive number
    do DATA
        output 'YES'
    do STATUS

08 = Read a Block

        OPTIONS:
            bit 0   1 = flush buffers if possible
            bit 1   1 = forget buffers even if fatal
                           errors occur

    do ARBITRATION
    do COMMAND with 7 bytes:
        08   get-block command
        xx   option bits
        xx
        xx
        xx   address   (addressing mode determines format)
        xx
        xx
    do DATA
        input bytes of block
    do STATUS

```
0A = Write a Block

        OPTIONS:
            bit 0       1 = flush buffers if possible
            bit 1       1 = forget buffers even if fatal
                            errors occur

    do ARBITRATION
    do COMMAND with 7 bytes:
        0a      put-block command
        xx      option bits
        xx
        xx
        xx      address   (addressing mode determines format)
        xx
        xx
    do DATA
        output bytes of block
    do STATUS      .
```

COMMAND ADDRESS FORMATS

If using physical track addressing mode, the command format for READ and WRITE commands is defined as:

```
byte 0      command byte
byte 1      options
byte 2      drive number
byte 3      cylinder (low)
byte 4      cylinder (high)
byte 5      head number
byte 6   ·  block number
```

If using logical track addressing mode, the command format for READ and WRITE commands is instead defined as:

```
byte 0      command byte
byte 1      options
byte 2      bits 7-4  logical drive number
            bits 3-0  block number (msb)
byte 3      block number
byte 4      block number (lsb)
byte 5      -
byte 6      -
```

If also using logical drive addressing, the drive number is included in the logical block number, and the logical block number is four bits longer (three full bytes):

```
byte 0      command byte
byte 1      options
byte 2      block number (msb)
byte 3      block number
byte 4      block number (lsb)
byte 5      -
byte 6      -
```

NOTE: Blocks are always numbered from zero, regardless of whether a block corresponds to a physical sector or to a portion of a sector (that is, regardless of whether the deblocking option is chosen).

ERROR BYTES

If there are errors associated with the current command,
these thirteen bytes will be returned to the bus master by the
hard-disk controller during the status phase.

NOTE: The definition of these bytes and bits WILL CHANGE
            before this software is officially released. Teletek
            invites comments and suggestions regarding information
            provided and format of that information.

        byte 0,1,2,3   error code bytes
                        number of bad:
        byte 4   seek attempts
        byte 5   read attempts since last seek
        byte 6   write attempts since last seek
        byte 7   rotate attempts before last read
        byte 8   rotate attempts before last write
        byte 9   rotate attempts before last verify
                        ID read attempts on last rotate:
    S - byte 10   good
    O - byte 11   bad
    S - byte 12   total

Definition of Bits of Error Code Bytes

        byte 0
            bit 0   one of the 22 different errors was fatal
            bit 1   one of the errors of byte 1 was not recoverable
            bit 2   error in bus master software (bits 3-7, this byte)
            bit 3   error in initialization parameters
            bit 4   option error   (not defined or not implemented)
            bit 5   command error   (command not defined)
            bit 6   command not confirmed
            bit 7   address error   (address out of range)

        byte 1
            bit 0   read id error   (never found valid id)
            bit 1   rotate error   (missed 'previous' sector)
            bit 2   CRC error on read   (sector was garbage)
            bit 3   checksum error   (CRC was OK, but ID bad)
            bit 4   sector read error   (got wrong sector)
            bit 5   cylinder seek error   (on wrong cylinder)
            bit 6   write CRC error (can't read sector just written)
            bit 7   write compare error   (sector failed verify)

ERROR BYTES (continued)

byte 2
        bit 0   drive select error   (does not acknowledge)
        bit 1   drive not ready
        bit 2   no seek complete
        bit 3   head select error   (using wrong head)
        bit 4   write fault never cleared
        bit 5   -
        bit 6   -
        bit 7   tape write protected

byte 3 not currently used

HARD DISK CONTROLLER CONSTANTS

        512   bytes per physical sector
        16   physical sectors per track

(In addition, the firmware assumes the drives are ST506
compatible.)

        E5 hex   byte used for CP/M sector initialization
        B6 hex   byte used for gap fill data

        7   number of bytes in a command
        12   number of error bytes returned

        10   maximum number of read or write retrys before abort