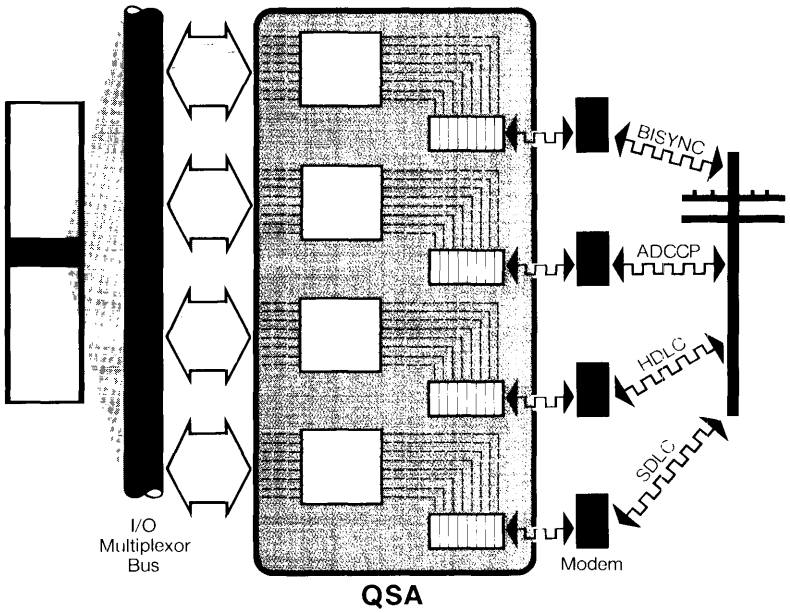
INTERDATA

PERIPHERALS



Quad Synchronous Adapter

The Quad Synchronous Adapter (QSA) is an economical and highly flexible communications interface for Interdata's computer systems and standard synchronous communication lines. QSA, constructed on one 15-inch board, contains all of the serializing, deserializing, and character buffering necessary to accommodate four synchronous lines.

QSA is available in two versions:

- M47-002 accommodates traditional binary synchronous protocol, or other similar character oriented protocols.
- M47-003 accommodates both the new bit-stuffing features required by SDLC, ADCCP, or HDLC and the widely used binary synchronous or other character oriented protocols.

Each line can operate individually in either half duplex or full duplex mode.

QSA achieves important design objectives for the systems builder:

- Line-Cost Economy – QSA cuts previous interfacing costs more than half.
- Installation and Modification Convenience – Line connections are much easier and communication expansion is inexpensive.
- System Design Flexibility – Easy conversion of QSA signals to a variety of signal standards is accomplished by implementation of a Line Conditioning Module (LCM).
- High Data Throughput – QSA handles data rates to 200,000 characters per second to match today's high data-rate facilities. Higher data rates mean less line connection time and lower costs.

Interdata's QSA provides enhanced flexibility and more control of communication parameters.

FEATURES

- Four half-duplex or full-duplex line interfaces, strap selectable on a per line basis.
- Full modem control on each line.
- TTL output levels, which utilize the Line Conditioning Module to interface various data sets.
- Half duplex Address Interleaving for configurations of multiple QSA's, all of which are strapped for half duplex. Allows conservation of device addresses.
- Local Loopback Mode for On-Line testing, selectable on a line pair basis.
- Program Control of character parameters such as character size, sync character, and odd/even or no parity.
- Split speed of each send/receive line pair.

Model M47-003

- Enable or disable under program control of Automatic Zero Bit Insertion/Deletion and Automatic Flag Insertion/Deletion as required by SDLC protocol, on a line basis.

FUNCTIONAL CHARACTERISTICS

When strapped for full-duplex operation, a QSA has eight consecutive device addresses. Each consecutive pair is the receive and transmit line address for a total of four lines.

The receive line is always assigned the even addresse and the transmit line the odd addresse. For half duplex operation, each line responds to the receive line addresses, unless half duplex interleaving is installed. The address interleaving scheme enables the consecutive addressing of eight half duplex lines, on two QSA's.

The transmission rate of the QSA is established by the particular modem, which must supply the clock signals. QSA is unaffected by the transmission rate as long as the rate does not exceed the upper limit of the unit 1.6M baud or 200,000 characters per second.

During binary synchronous transmission, data are transmitted bit serial and synchronization or character framing is achieved when the QSA detects a character match between the incoming characters and one previously established by the program. This match character called a sync character, is any 5, 6, 7, or 8-bit character in the range of X'03:X'FE' (with or without parity), it is program selectable for each line in non-bit stuffing mode.

FEATURE	PROGRAM CONTROL	STRAP CONTROL
Sync Character Selection	Each Line	
Character Bits Selection	Each Line	
Enable Zero Bit Insertion/ Deletion, Flag Insertion/ Deletion	Each Line	
Loop Back Capability	On Pair of Lines	
Automatic Parity Checking/Insertion		
Full/Half Duplex		Each Line
Deletion of All Leading Sync Characters		Per QSA Board
Automatic Resynchronization of SDLC Frame		Per QSA Board
Automatic Answer/ Full Modem Control	For Each Line	For Each Line

The table shows the various controls available to the user and system designer.

The new "bit-stuffing" or zero bit insertion/deletion (ZBID) mode is required to support the recently implemented bit oriented protocols. When the QSA with ZBID capability is selected this function may be enabled/disabled under program control on a line basis. When enabled the flag character is fixed as to pattern and size. The flag character is automatically sent by QSA at the beginning and end of each transmission. QSA also automatically provides zero-bit insertion and deletion as the particular bit stream is transmitted or received.

INSTRUCTIONS

The processor I/O Instructions used to communicate with the QSA are:

- Sense Status (SSR) - Used to determine if character transfers are complete and correct and to interrogate the data set status.
- Output Command (OCR) - Used to answer or disconnect calls and to set the QSA in the Receive or Send mode.
- Write Data (WDR) – Used to load the output character into the data register and also load the Sync Character Register.
- Read Data (RDR) – Used to read an assembled character into the processor.
- Acknowledge Interrupt (AIR) - Used to service interrupts. Execution of this instruction returns the address and status of an interrupting line (16 bit processors only).

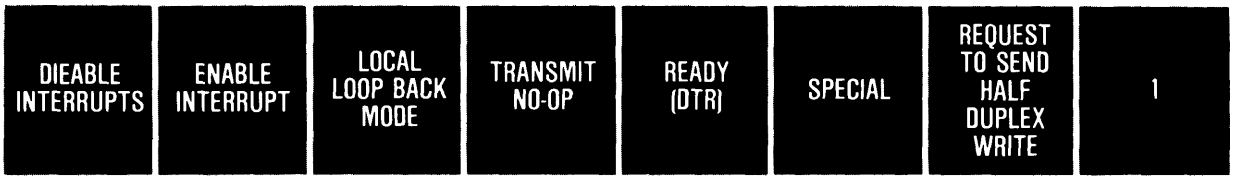
In addition to the QSA data registers, the processor also can load and examine the various QSA command and status registers. Each Transmit and each Receive Line has a Command Byte Register with the indicated functional characteristics.

QUAD SYNCHRONOUS ADAPTER COMMAND BYTE DESCRIPTION

RECEIVE

When set, caused the Receive line to go into the Sync/Flag Search mode, reset causes no change.

TRANSMIT



When set, outgoing data is diverted from the Data Set to the Receive side of another line pair.*

When set, continuous mark characters are delivered to the line, when reset, no change of line condition is affected.

Control signal to Data Set to accommodate new signals such as NEW SYNC or Speed Select.

When set, causes Ready Control line to Data Set to go to On level.

In two-wire mode, this bit set readies the line for transmitting. When reset, the line goes to Read mode. In both two-wire and four-wire, this bit set causes the Request to send Control Line to the Data Set to go active, and deactive when reset.

Steering Bit Indicating Command instructions go to the I/O Mode command registers.

*This feature not possible when adapter is interfaced to a Selector Channel.

In addition to the Command Register associated with each line, each pair (Receive/Transmit) also has a Common Register where information common to both is maintained.

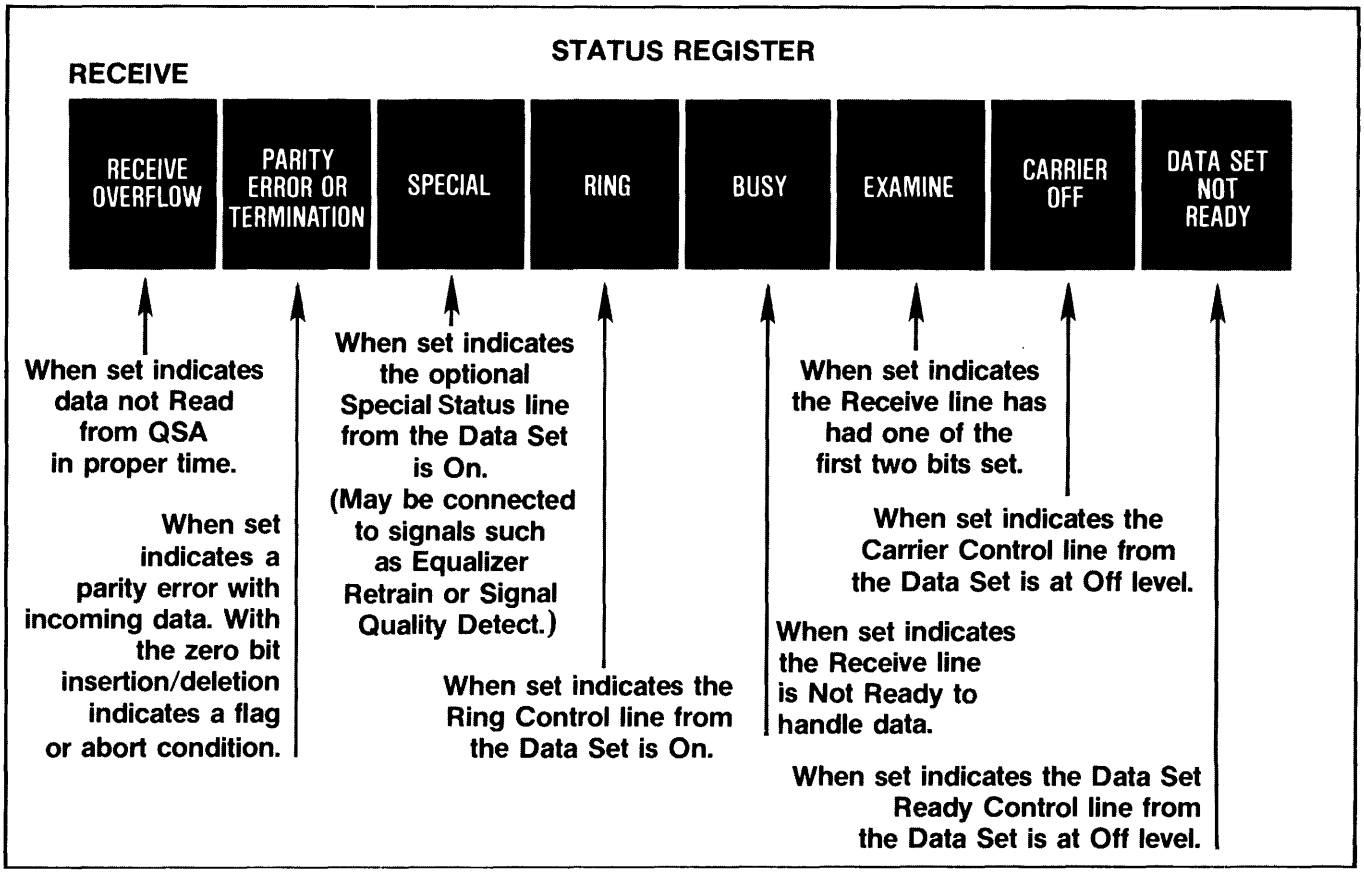
CONTROL MODE COMMAND REGISTER

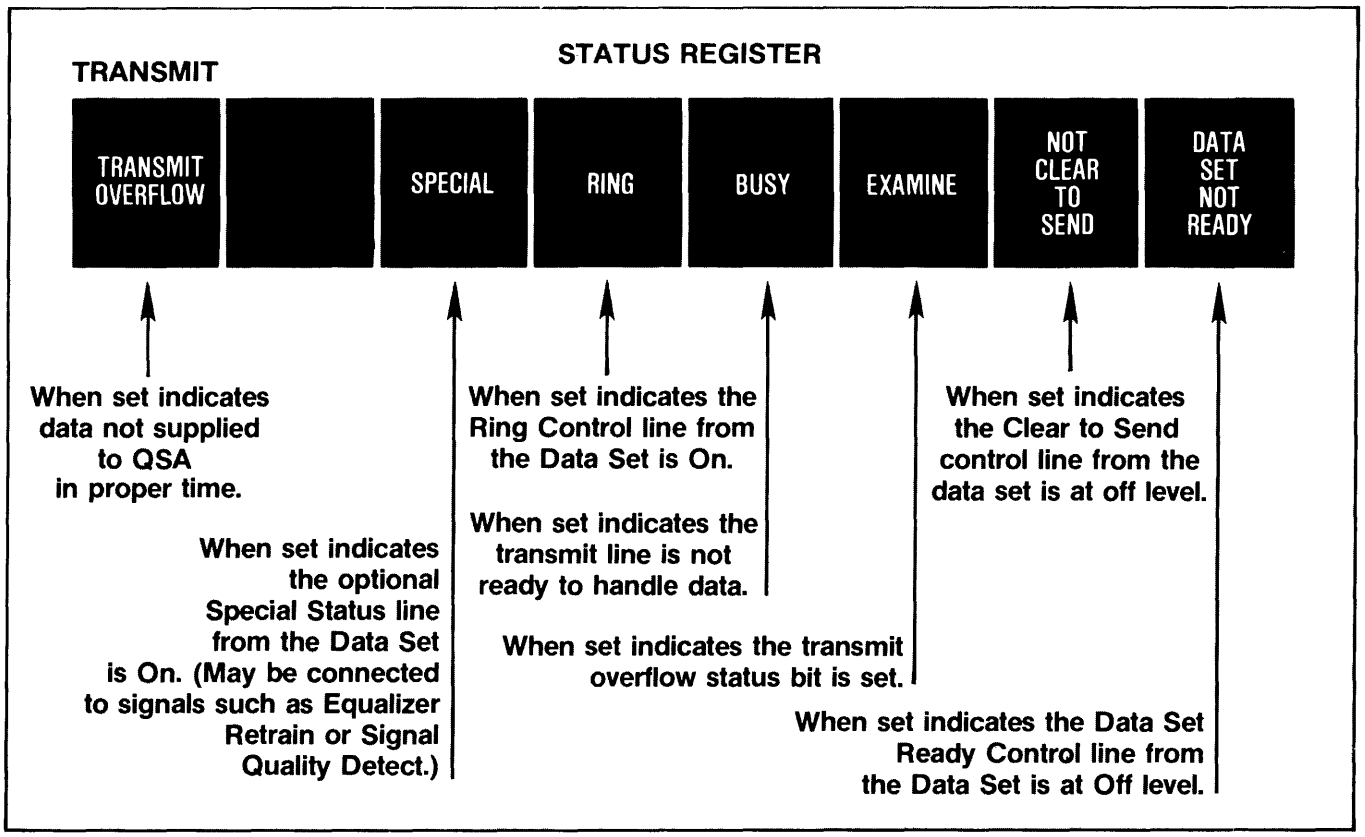
These two bits control parity selection and zero bit insertion/deletion.*

Steering bit when reset indicates command data is to be stored in the control mode command register.

*Program control of zero bit insertion/detection is only available on QSA Model 47-003.

Status Information is maintained for each Received and Transmitter line in a Status Register. Reading of this information is accomplished by the appropriate instruction to the line address.





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