MULTIPERIPHERAL CONTROLLER (MULTI-LAYER MPC)

Theory of Operation Manual

63-022 R00

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PREFACE

This manual provides the information necessary for the technician to maintain the multiperipheral controller (MPC) board.

The MPC contains the clocks, hardware communication assist, line printer interface, loader storage unit (LSU), and eight RS-232C synchronous/asynchronous communications channels.

Chapter 1 contains a general description of the MPC board, including purpose, function, and capabilities. Chapter 2 describes the multiplexor bus signals and timing. Chapter 3 provides the theory of operation of the loader storage unit (LSU). Chapter 4 describes the 8-line communications multiplexor (COMM MUX) and the microprocessor control of registers and data flow. Chapter 5 provides information on the precision interval clock (PIC) and the line frequency clock (LFC). Chapter 6 describes the line printer interface, and Chapter 7 analyzes the hardware communication assist section of the MPC. Appendix A contains the signal mnemonics listing. Appendix B contains a flowchart of the steps to follow when the error LED indicator is on.

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The multiperipheral controller (MPC) uses state-of-the-art microprocessor technology to implement input/output (I/O) functions, precision interval clocks (PICs)/line frequency clocks (LFCs), line printer interface, bootloader, and data communication handling assist on one printed circuit (PC) board.

This chapter describes the purpose, functions, and capabilities of an MPC in a Concurrent Computer Corporation data processing system.

1.2 PURPOSE AND FUNCTIONS

The MPC provides a means of interfacing user devices or terminals to a system using eight programmable, full-duplex data communications channels. The 8-channel data communications multiplexor (COMM MUX) can be increased in increments of eight channels when additional MPCs are added. The MPC also contains the PIC/LFC, hardware communication assist, line printer interface, and loader storage unit (LSU). See Figure 1-1 for a simplified block diagram of the MPC.

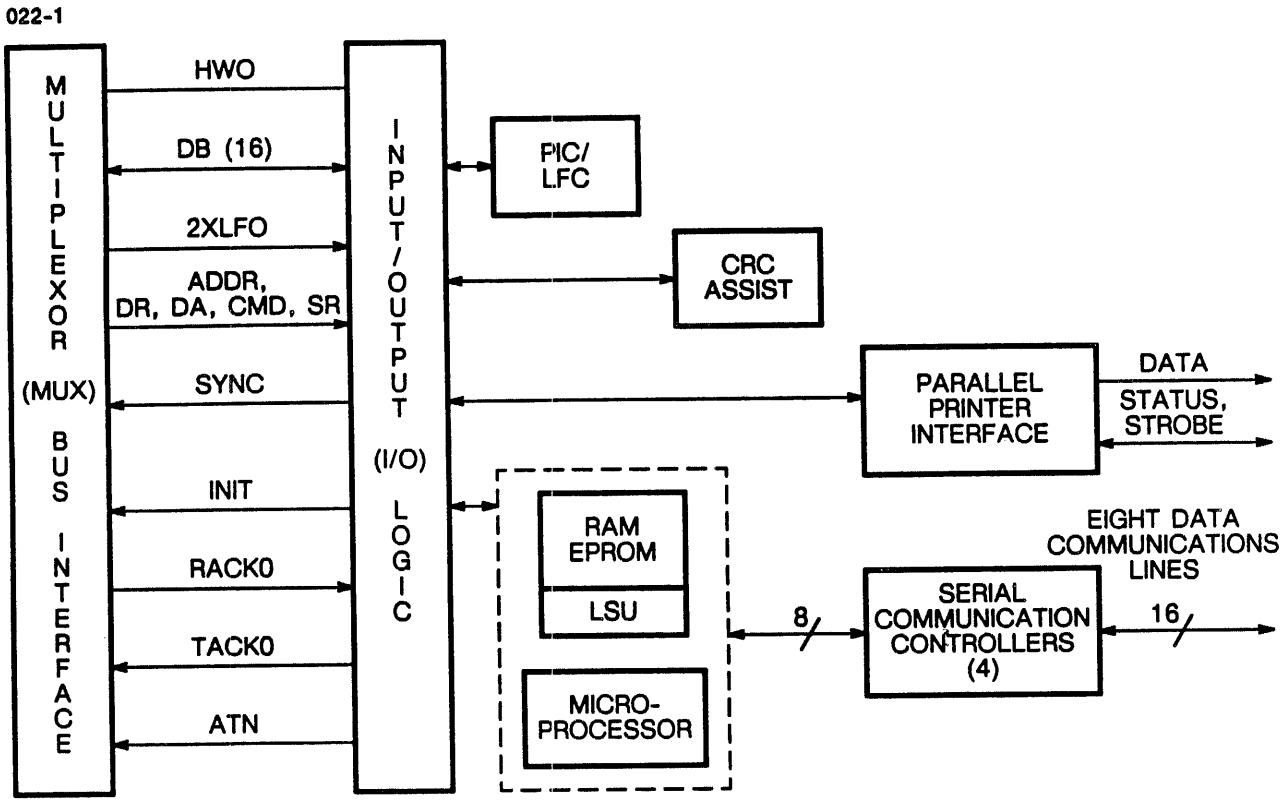

Figure 1-1 MPC Basic Block Diagram

1.3 CAPABILITIES

The MPC contains six major components:

- Multiplexor (MUX) bus interface
- Communications section
- LSU
- PIC/LFC
- Parallel line printer interface
- Hardware communication assist

More than one MPC may be configured in a system. Each MPC provides eight additional full-duplex communications channels. In systems with multiple MPCs, the LSU and PIC/LFC are activated only on the MPC in the highest priority slot, and the line printer interface is activated only on the MPC in the lowest priority slot. All other LSUs, PICs/LFCs, and line printer interfaces are deactivated.

The following sections describe the six major components of the MPC.

1.3.1 Multiplexor (MUX) Bus Interface

The MUX bus interface provides all the command and control request/response signals and address and data lines required to provide communications between the MPC board and the processor. The MPC interfaces to the backpanel via connector 0 (CONN0).

1.3.2 Communications Section

The communications section consists of a microprocessor, random access memory (RAM), and the 8-channel data COMM MUX.

1.3.2.1 Microprocessor

The microprocessor controls the request/response signals and data lines between the MUX bus and the 8-channel data COMM MUX.

1.3.2.2 Erasable Programmable Read-Only Memory (EPROM) and Random Access Memory (RAM)

The microprocessor has access to 16kB of 200ns EPROM and 8kB of 70ns static RAM. On power-up, portions of the EPROM are downloaded into the faster static RAM for program execution.

1.3.2.3 8-Channel Data Communications Multiplexor (COMM MUX) (Synchronous/Asynchronous)

The 8-channel data COMM MUX consists of four serial communication controllers. Each controller contains two independent full-duplex channels and provides the following features:

- A crystal oscillator
- A first-in/first-out (FIFO) buffer with quad receive/dual transmit capabilities

Any one of the eight channels can be asynchronous, synchronous data logic control (SDLC), bisynchronous (BISYNC), or monosynchronous. Any mixture of protocols is allowed to exist on the MPC board.

1.3.3 Loader Storage Unit (LSU)

There is an internal and an external LSU on the MPC board. The internal 6.6kB LSU is located in the microprocessor control store (CS). The external LSU is located in a separate 32kB chip. During initialization, the program stored in the activated LSU section can be automatically loaded into the computer's memory. If the system is configured with multiple MPC boards, only the LSU on the highest priority MPC board is activated.

A watchdog timer is included in the LSU. If the watchdog timer is enabled and the user program fails, the timer times out and the restart sequence is initiated. The timer can also be used to restart the user program upon restoration of power after a power failure.

1.3.4 Precision Interval Clock (PIC) and Line Frequency Clock (LFC)

The MPC contains both the PIC and LFC. These clocks generate interrupts to the processor at different rates. If more than one MPC is configured in a system, the PIC and LFC are deactivated on all but the highest priority MPC board for a standard installation.

1.3.5 Line Printer Interface

The line printer interface is compatible to the Centronics I/O parallel printer series and supports both lower- and upper-case characters. If the system is configured with multiple MPC boards and a single line printer, the line printer interface on the lowest priority MPC board is activated.

1.3.6 Hardware Communication Assist

The hardware communication assist contains CRC-BISYNC, CRC-SDLC, and longitudinal redundancy check (LRC) accumulation.

In the XF400 and Models 3203 and 3205, the hardware communication assist functions with the processor microcode. Therefore, on these systems, the hardware communication assist logic circuitry on the MPC board must be deactivated. On other Series 3200 and XF Series Systems, the hardware communication assist must be activated.

1.4 FUNCTIONAL VARIATIONS

This section describes the four functional variations of the multi-layer MPC board. See the functional variation table on assembly drawing 35-910 E03. Strapping information is described in the Multiperipheral Controller (Multi-Layer MPC) Installation and Programming Manual.

1.4.1 Functional Variation F00

This version of the multi-layer MPC provides an internal LSU, a universal clock (UCLOCK), a hardware communication assist, a line printer interface, and an 8-line COMM MUX to any Series 3200 Processor and XF Series larger than XF400.

1.4.2 Functional Variation F01

This version of the multi-layer MPC board is used as the primary MPC in the Model 3203 and XF400. This board has an automatic loading feature and a 32kB external LSU that provides support for boot devices under an IPC. This board also contains an internal LSU, a UCLOCK, a hardware communication assist, a line printer interface, and an 8-line COMM MUX.

1.4.3 Functional Variation F02

This depopulated version of the multi-layer MPC board provides a line printer interface and an 8-line COMM MUX only. It is used in multiple MPC installations where more communications lines or another line printer are required.

1.4.4 Functional Variation F03

This version of the MPC board has a 32kB external LSU which provides Series 3200 Processors and XF Systems larger than the XF400 with the capability of booting from a variety of peripheral devices. This board also contains an internal LSU, a UCLOCK, a hardware communication assist, a line printer interface, and an 8-line COMM MUX.

1.5 ANALYSIS

The block and functional diagrams of the MPC show the six major sections and their relationship to each other. See Figures 1-2 and 1-3. The sections are structured so they function as individual and integral parts of the MPC.

The following chapters describe in detail each section of the MPC. Also refer to the schematic diagram 35-910 D08 included at the end of this manual.

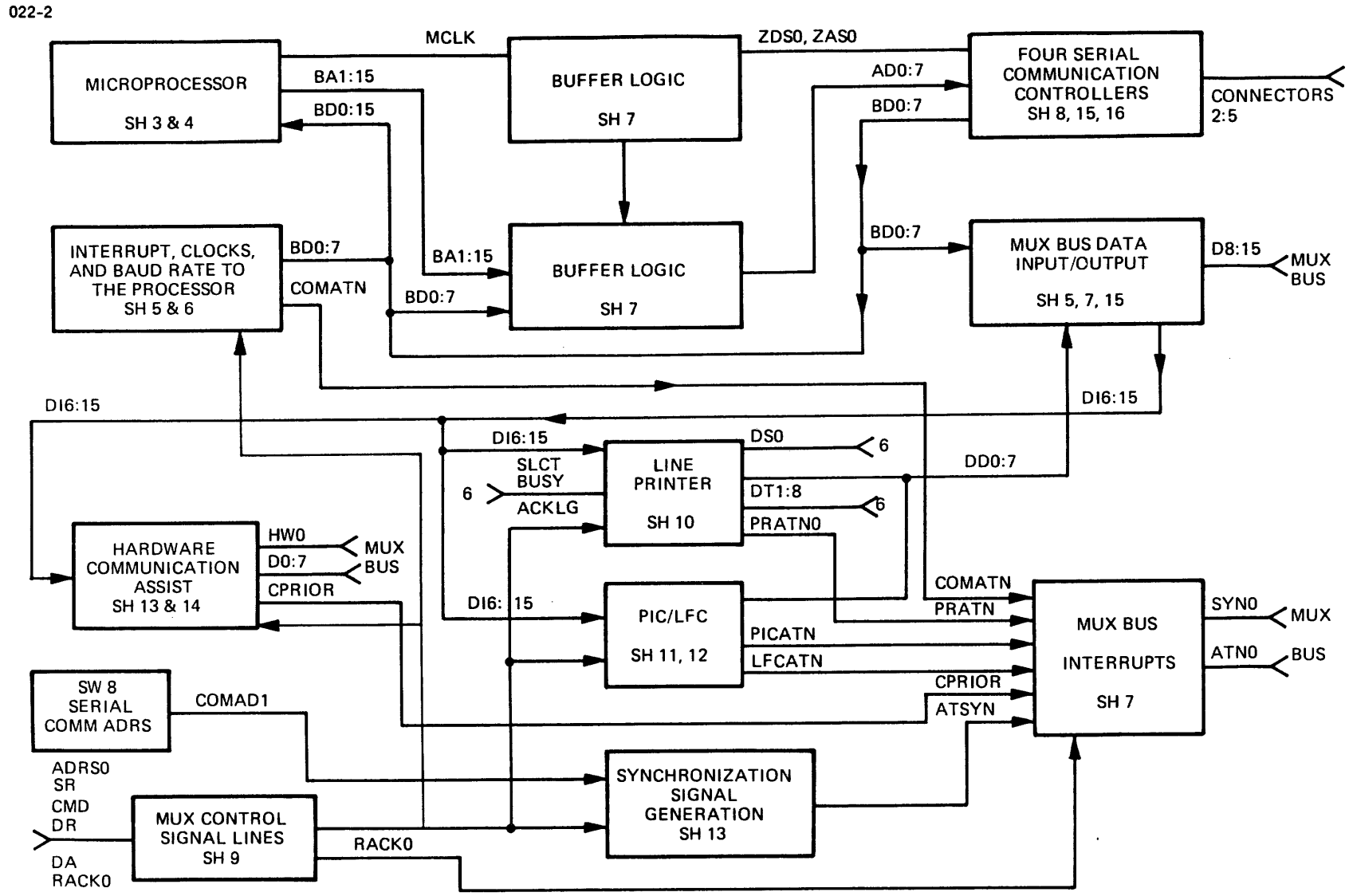

Figure 1-2 MPC Block Diagram

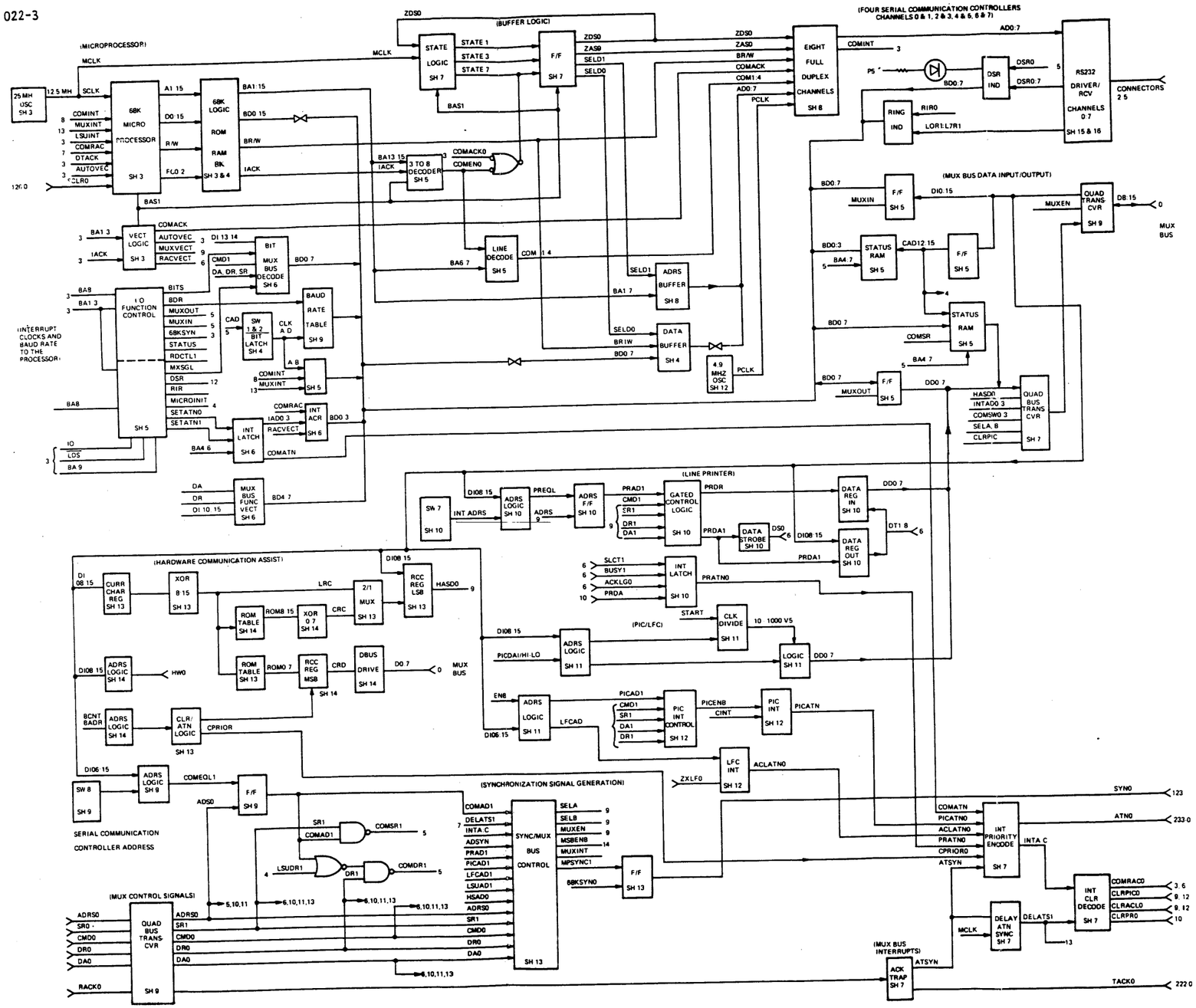

Figure 1-3 MPC Functional Diagram

CHAPTER 2
MULTIPLEXOR (MUX) BUS INTERFACE THEORY

2.1 INTRODUCTION

The MUX bus interface enables the MPC to interact with the processor in the form of request/response signals. See Table 2-1 for a list of the MUX bus signal lines.

TABLE 2-1 MUX BUS SIGNAL LINES

TYPE	MNEMONIC	DIRECTION ---> PROCESSOR MPC <---	NUMBER
Data lines	D000:150	<---------->	16 lines
Control lines	ADRS0	---------->	1 line
	SR0	---------->	1 line
	DR0	---------->	1 line
	DA0	---------->	1 line
	CMD0	---------->	1 line
	RACK0/TACK0	-(daisy-chain)->	1 line
Test lines	SYN0	<----------	1 line
	ATN0	<----------	1 line
	HW0	<----------	1 line
Initialize line	SCLR0	---------->	1 line

2.2 SIGNAL LINE DEFINITIONS

The following sections describe the MUX bus signal lines. With the exception of the serial receive acknowledge/transmit acknowledge (RACK0/TACK0) line, all MUX bus signal lines are connected, in parallel, to all devices on the MUX bus. The MSB is 0 for data transfer over the MUX bus. However, this is reversed so 0 is LSB on internal busses.

Data lines:

- D000:150

  The 16 low-active data lines (Sheets 9 and 14 of schematic diagram 35-910 B08) are used to transfer, in parallel, an 8-bit byte or a 16-bit halfword of data between the MUX bus and the MPC via the microprocessor. In the halfword mode, the data is transferred on data lines D000:150 (Sheets 9 and 14), backpanel pins 111 through 218. In the byte mode, the data is transferred on the least significant data lines (D080:150) (Sheet 9) using backpanel pins 115 through 218. Only the hardware communication assist portion of the MPC uses the halfword mode; the remaining sections of the board are byte-oriented.

Control lines (9A8):

- Address (ADRS0)

  This low-active control line is activated by the processor to the MPC. It is accompanied by a 10-bit device address on the data lines to select one device controller for subsequent I/O transfers. This line uses backpanel pin 219.

- Status request (SR0)

  This low-active control line is activated by the processor to the MPC. The selected device gates its status byte onto the data lines of the MUX bus. This line uses backpanel pin 119.

- Data request (DR0)

  This low-active control line is activated by the processor to the MPC. The selected device gates a byte or halfword of data onto the data lines of the MUX bus. This line uses backpanel pin 120.

- Data available (DA0)

  This low-active control line is activated by the processor to the MPC, accompanied by a byte or halfword of data on the data lines for a selected device. This line uses backpanel pin 221.

- Command (CMD0)

  This low-active control line is activated by the processor to the MPC, accompanied by a command byte on the data lines for a selected device. This line uses backpanel pin 220.

- Interrupt acknowledge (ACK0)

  This low-active control line is activated by the processor to the MPC. The highest priority device having an interrupt pending inhibits propagation of TACK0 to lower priority devices and gates its device address onto the data lines for the MUX bus. This line uses backpanel pin 122 for RACK0 and pin 222 for TACK0.

Test lines:

- Synchronize (SYN0) (13G2)

  This low-active test line is activated by the MPC to the processor via the MUX bus. SYN0 informs the processor that the selected I/O channel has properly recognized and responded to a control line signal.

- Attention (ATN0) (7H2)

  This low-active test line is activated by any enabled device that has an interrupt pending. The device holds this test line active until it has received an interrupt acknowledge (RACK0) control line signal. Several device controllers may activate ATN0 concurrently, but only the highest priority device responds to RACK0. This line uses backpanel pin 223.

- Halfword (HW0) (13G3)

  This low-active test line, which is activated by the hardware communication assist, indicates to the processor that the I/O device is capable of transferring 16 bits of data at a time. This line uses backpanel pin 226.

Initialize line:

- System clear (SCLR0) (3B1)

  This low-active line is activated during system power-up, system power-down, or initialization. This line uses backpanel pin 126.

2.3 MULTIPLEXOR (MUX) BUS INPUT/OUTPUT (I/O) TIMING

The request/response signals are used for MUX bus I/O operations. This allows the MUX bus to run at its maximum speed whenever possible, but permits a graceful slowdown if the characteristics of a particular device require signals of a longer duration. Any delays in the MUX bus timing over the specified minimum timing result in increased I/O instruction execution time and degraded system throughput.

2.3.1 Output Operation Timing (Processor/MPC)

Figure 2-1 shows the timing for the three types of output operations: address (ADRS0), command (CMD0), and data available (DA0). To start an output operation, the processor activates the data lines with the desired data, then activates the appropriate control line (ADRS0, CMD0, or DA0). When the MPC accepts the command or data or recognizes an address match, it activates the synchronize (SYN0) test line to the processor.

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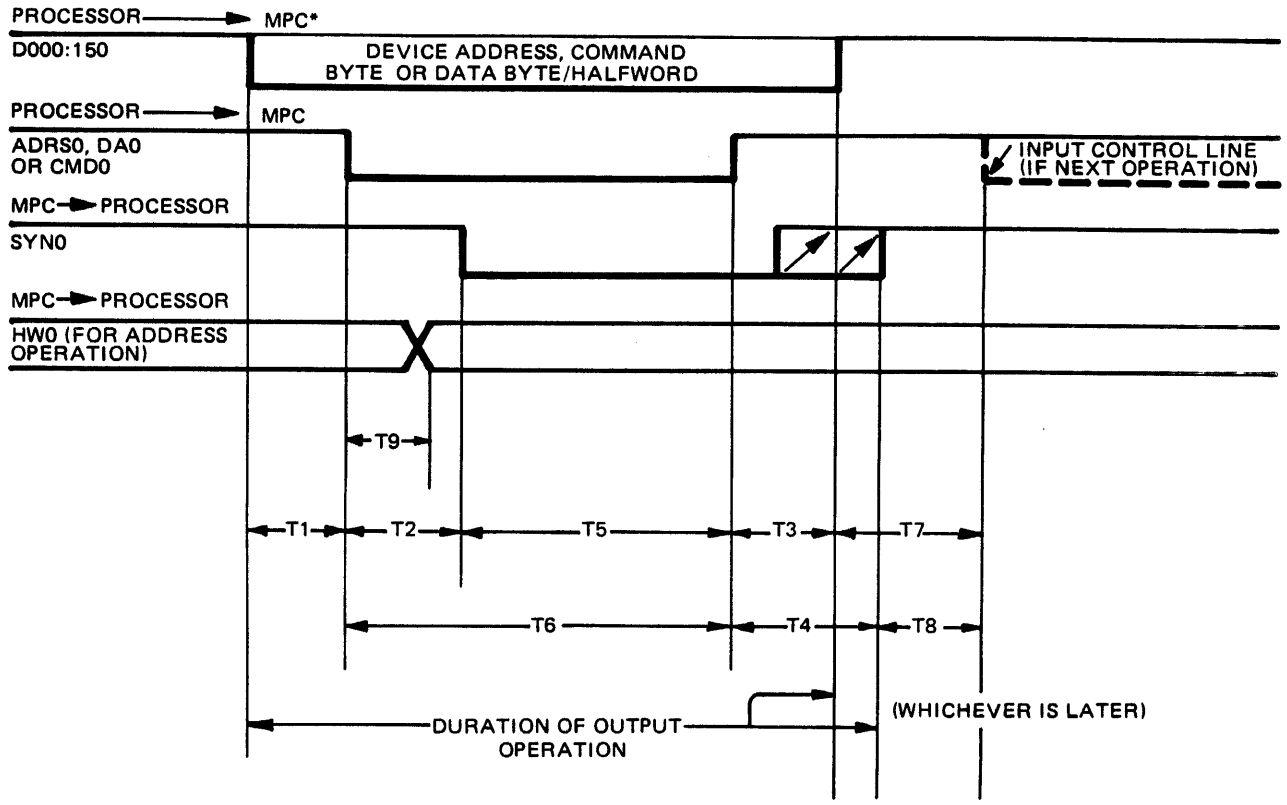


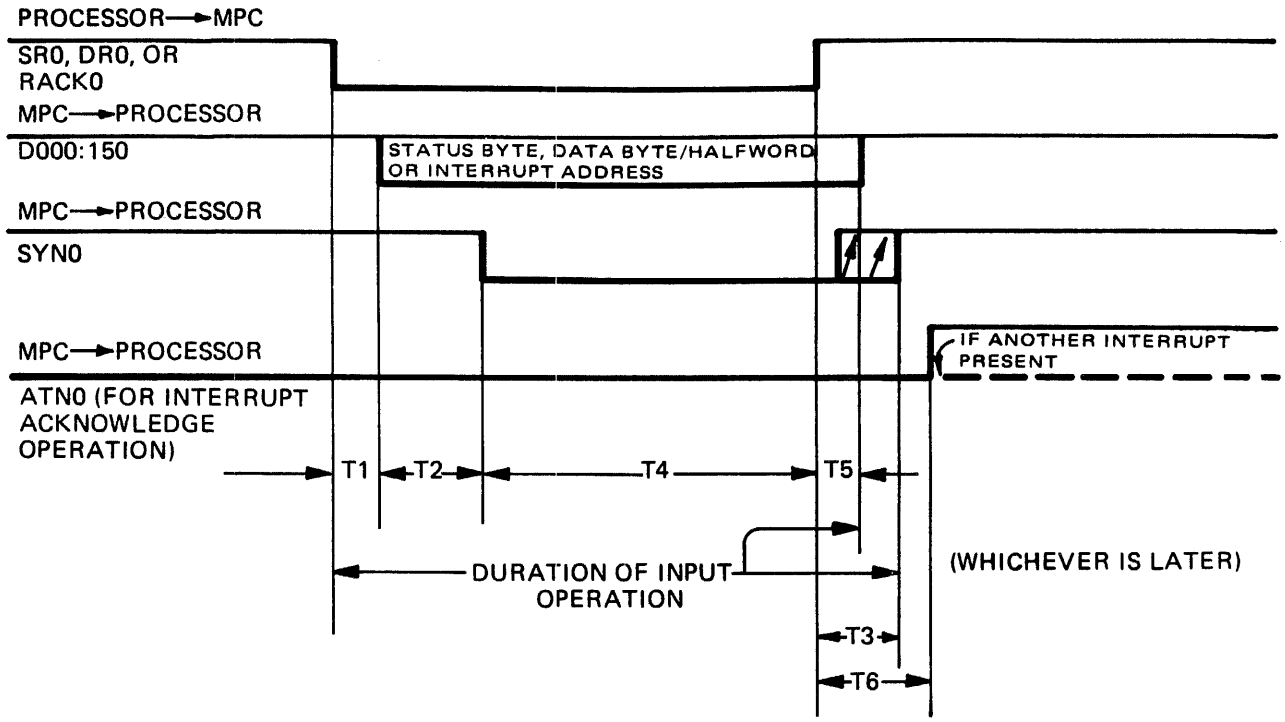
NOTE: TIMING SHOWN AT DEVICE CONTROLLER INPUTS

T1, T3 } 75 NS. GUARANTEED MINIMUM AT CONTROLLER INPUTS
T2 – AS SHORT AS POSSIBLE AFTER DEVICE RECOGNIZES ADDRESS OR ACCEPTS DATA OR COMMAND
T4 – AS SHORT AS POSSIBLE
T5 – 100 NS. MINIMUM
T6 – 350 NS. MINIMUM FOR ADRS0. DA0 AND CMD0 HAVE NO MINIMUM BUT DEACTIVATE AFTER SYN0 ACTIVATES
T7 – 100 NS. MINIMUM
T8 – MUST BE GREATER THAN ZERO
T9 – MUST BE LESS THAN T2
* THE PROCESSOR MUST DEACTIVATE THE DATA LINES MINIMUM 100 NS BEFORE ACTIVATING ANY CONTROL LINE FOR THE NEXT I/O OPERATION.

Figure 2-1 Output Operation Timing

2.3.2 Input Operation Timing (MPC/Processor)

Figure 2-2 shows the timing for the three types of processor input operations: status request (SR0), data request (DR0), and interrupt acknowledge (ACK0). The input operation starts as the processor activates one of the applicable control lines: SR0, DR0, or RACK0. The MPC then gates the appropriate data onto the MUX bus data lines and activates the SYN0 test line.



NOTE: TIMING SHOWN AT DEVICE CONTROLLER INPUTS

T1 – AS SHORT AS POSSIBLE
T2 – MUST BE GREATER THAN ZERO
T3 – AS SHORT AS POSSIBLE
T4 – 100 NS. MINIMUM
T5 – AS SHORT AS POSSIBLE
T6 – MUST BE GREATER THAN ZERO – I.E. DEVICE MUST NOT DEACTIVATE ATN0 BEFORE RACK0 (AT DEVICE INPUT) DEACTIVATES.

Figure 2-2 Input Operation Timing

2.4 MULTIPLEXOR (MUX) BUS INTERRUPTS

The MPC board generates an interrupt (ATN0) to the processor when any of its sections are ready for a data transfer. If more than one section of the MPC is ready for a data transfer at the same time, the MPC prioritizes the interrupts as described in the following sections. See Functional Schematic 35-910 D08 and Figure 2-3.

The MUX bus interrupts, from the eight data communications channels via the microprocessor, the PIC/LFC, the line printer interface, and the hardware communication assist on the MPC, are input to an octal latch (IC A74) (7C3) which is normally in a transparent mode. Any activity at the input pins is immediately reflected at the output pins and is prioritized by the 8-3 line encoder (IC A75) (7E2). IC A75 produces ATN0 (7H2) to the processor via the MUX bus for all interrupts except the hardware communication assist. The hardware communication assist only generates the internal code to the 3 to 8 decoder (IC A83) (7K2) and does not enable ATN0 to the MUX bus. When ATN0 is active, the processor replies to the interrupt with a RACK0 on the MUX bus. If the interrupt is pending on the MPC, RACK0 is trapped and TACK0 (7M4) is not propagated through the backpanel to any other system board. When RACK0 is active, it inputs ATSYN1 to IC A130 (7A4) and freezes the current condition of the interrupts to the highest priority interrupt. Attention synchronize (ATSYN1) (7J4) is clocked twice by the MCLK to eliminate any meta-stable states. The delay attention synchronize signal (DELATS1) (7L5) is input to the 3 to 8 decoder (IC A83) (7K2) and enables the appropriate code for the type of interrupt currently being acknowledged.

For example, if one of the eight data communications channels requests attention, communication attention (COMATN0) (7A3) is activated and becomes the pending interrupt to the 8-3 line encoder (IC A75). COMATN0 produces a low at input 6 (pin 3) of IC A75, which enables attention ATN0 (7H2) to the processor and produces an output code of A2 and A1 low and A0 high. When RACK0 is received, the interrupt output code from IC A75 (7E2), as shown in Table 2-2, is input to the 3 to 8 decoder (IC A83) (7K2) by DELATS1. This logic is decoded to produce communication receive acknowledge (COMRAC0) at Y1 (7L1) (see Table 2-3). COMRAC0 is input to the microprocessor as an interrupt in response to the interrupt generated by one of the eight data communications channels. The same procedure is used for the remaining interrupts except that the output of A83 is not sent to the microprocessor; the output signals are sent to clear the logic that generated the interrupt.

The interrupt priorities in descending order are as follows:

- Hardware communication assist (CPRIOR0)
- Eight data communications channels (COMATN0)
- PIC clock (PICATN0)
- LFC clock (ACLATN0)
- Line printer (PRATN0)

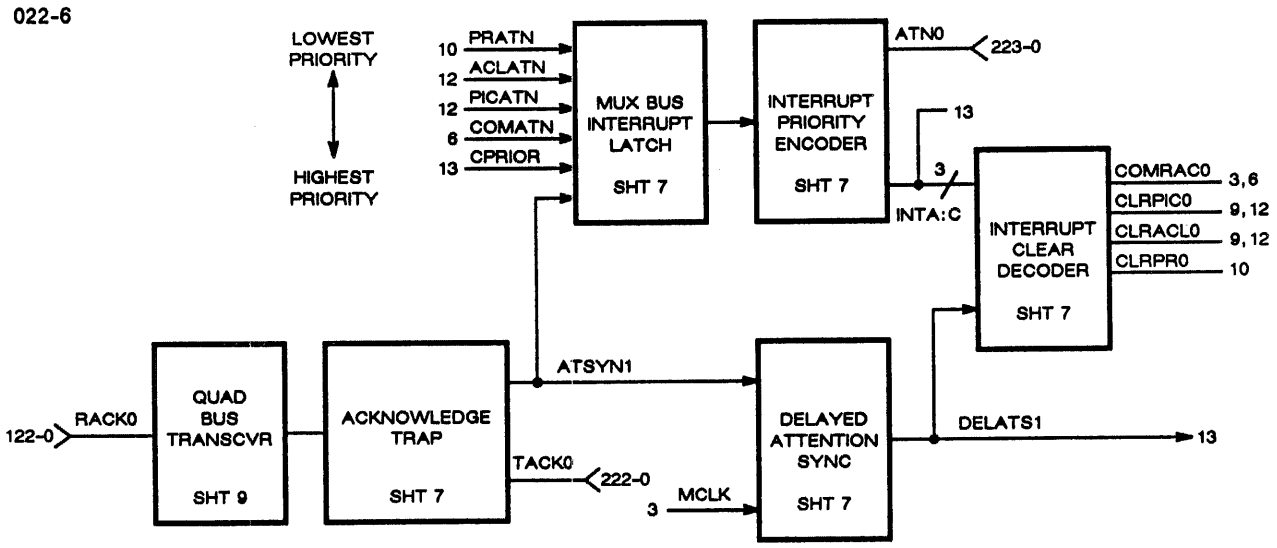


Figure 2-3 MUX Bus Interrupts

TABLE 2-2 8-3 LINE ENCODER (IC A75)

INPUTS								OUTPUTS				FUNCTION
0	1	2	3	4	5	6	7	A2	A1	A0	E0	
-	-	-	-	-	-	-	L	L	L	L	H	HCA Interrupt
-	-	-	-	-	-	L	H	L	L	H	H	COM Interrupt
-	-	-	-	-	L	H	H	L	H	L	H	PIC Interrupt
-	-	-	-	L	H	H	H	L	H	H	H	LFC Interrupt
-	-	-	L	H	H	H	H	H	L	L	H	PTR Interrupt
-	-	L	H	H	H	H	H	H	L	H	H	---
-	L	H	H	H	H	H	H	H	H	L	H	---
L	H	H	H	H	H	H	H	H	H	H	H	---
H	H	H	H	H	H	H	H	H	H	H	L	OFF

TABLE 2-3 3 TO 8 DECODER (IC A83)

INPUTS				OUTPUTS				FUNCTION
ENABLE	SELECT							
G1	C	B	A	Y1	Y2	Y3	Y4	
H	L	L	L	H	H	H	H	---
H	L	L	H	L	H	H	H	Clear DCOM Int
H	L	H	L	H	L	H	H	Clear PIC Int
H	L	H	H	H	H	L	H	Clear LFC Int
H	H	L	L	H	H	H	L	Clear PTR Int
H	H	L	H	H	H	H	H	---
H	H	H	L	H	H	H	H	---
H	H	H	H	H	H	H	H	---
L	-	-	-	H	H	H	H	---

2.5 SYNCHRONIZATION SIGNAL

The field programmable logic array (FPLA) IC A115 (13B3) determines when SYN0 is returned to the processor by monitoring SR0, CMD0, DR0, DA0, or DELATS1 in response to a RACK0. Interrupts A through C (INTA:INTC) (13A2) are the prioritizations of the different interrupts that the MPC can generate. The FPLA monitors the printer address (PRAD1), precision interval clock address (PICAD0), AC line frequency clock address (LFCAD0), loader storage unit address (LSUAD0), data communications address (COMAD0), hardware communication assist address (HASDO), and the address (ADRSO) pulse. The FPLA IC A115 is preprogrammed and the contents are shown in Table 2-4. The FPLA determines which part of the MPC is addressed and determines when a control pulse becomes available.

SYN0 is returned to the processor by activating the MPC synchronization pulse (MPSYNC1) (13C3), which is dual ranked by IC A166 (13E2) and generates the synchronization signal (SYN0) (13G3). For example, if ADSYN0 is low and ADRS1 is high on FPLA incoming pins 27 and 20, respectively (state 1), MPSYNC1 becomes active on pin 13 which sends SYN0 back to the processor (see Column 1 of Table 2-4).

TABLE 2-4 SYNCHRONIZATION SIGNAL GENERATION

PIN NUMBER	SIGNAL	1 STATE 32	
01	NC	----------	INPUT
02	INTC	--L----------LLLH-	
03	INTB	--L----------LHHL-	
04	INTA	--L----------HLHL-	
05	DELATS1	--H----------HHHH-	
06	DA1	-H----H---H---H---H---H---H---------	
07	DR1	-----H-H---H---H---H---H---H-------H	
08	CDM1	---H----H---H---H---H---H---H-------	
09	SR1	----H----H---H---H---H---H---H------	
10	NC	LLLLLLLLLLLLLLLLLLLLLLLLLLLLLL	OUTPUT
11	MUXINT0	HHHHHHLLLHHHHHHHHHHHHHHHHHHHHH	
12	MSBENB0	HHLHHHHHHHHHHHHHHHHHHHHHHHHHHL	
13	MPSYNC1	HHHHHHLLLHLLLHHHHHHHHHHHHHLHHHH	
14	GND		
15	MUXEN0	HHLHHLHLHLHLHHHHHHHLHHHHHHLLLLL	
16	68KSYNRST	LLLLLLHHHLHHHLLLLLLLLLLLLLLLLL	
17	SELB	LLLLLLLLLLLLLLLLLLLLLLLLLLHHHLL	
18	SELA	LLHLLLLLLLLLLLLLLLLLLLLLLLLHHLH	
19	CE	LLLLLLLLLLLLLLLLLLLLLLLLLLLLLL	INPUT
20	ADRS1	H----------	
21	HSAD0	-L-LLL----------L	
22	COMAD1	------HHHH----------	
23	LSUAD0	----------LLLL----------	
24	LFCAD0	----------LLLL----------	
25	PICAD0	----------LLLL----------	
26	PRAD1	----------HHHH-----	
27	ADSYN0	L----------	
28	P5		

H or L = active state
- = don't care

Another method of returning SYN0 is in response to a control function requiring a 68K operation. In this case, the processor generates an interrupt to the microprocessor by enabling the MUX interrupt (MUXINT0) (13C2) (states 7, 8, and 9). The microprocessor performs its function and, when it completes the operation, it activates flip-flop A135 (13B5) to generate SYN0 to the processor through IC A166. When the control line is deactivated by the processor, SYN0 is reset by the signal 68KSYNRST.

Other functions of the FPLA are as follows:

- Enabling the output of the least significant byte to the MUX bus with MUX bus enable (MUXEN0) (13C2).
- Enabling the most significant byte output of the communication assist data path with most significant byte enable (MSBENB0) (13C2).
- Generating select A (SELA) and select B (SELB) (13C1), which are used in conjunction with the 4-to-1 MUXs (9H2-8) for the different data paths that are loaded onto the MUX bus (see Figure 2-4).

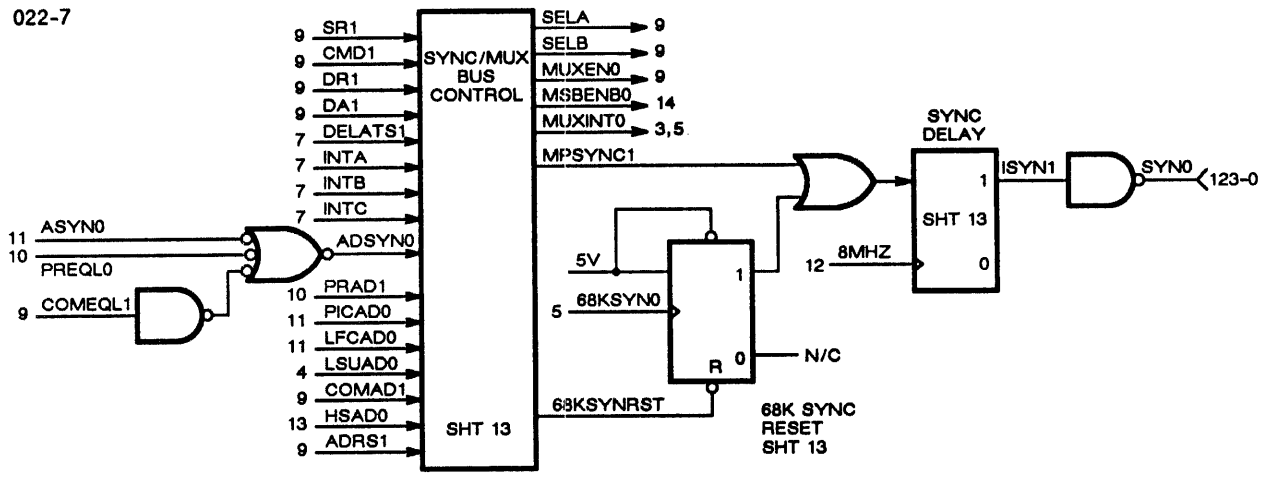


Figure 2-4 Synchronization Signal Generation

2.6 CONTROL SIGNALS

The quad bus transceivers A156 and A164 (9B9 and 9B7) receive the following six control signals from the MUX bus: ADRS0, SR0, CMD0, DR0, DA0, and RACK0. These signals are buffered and distributed throughout the MPC.

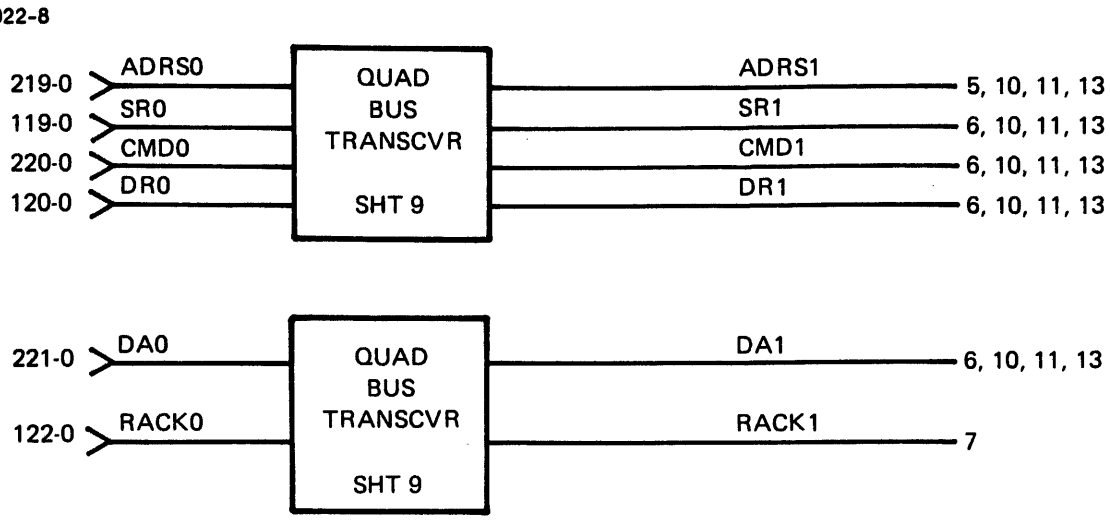


Figure 2-5 MUX Bus Control Signals

2.7 DATA INPUT/OUTPUT (I/O)

Data input to the MPC is through quad bus transceivers A171 and A193 (Sheet 9) creating the data input bus (DI08:15). Output to the MUX bus via A171 and A193 is through 4 to 1 MUXs A84, A85, A95, and A105 (Sheet 9), which multiplex the internal busses of the MPC for transmission to the processor. The internal data lines (DD0:7) (9E8) at the input of the 4 to 1 MUXs provide outputs at pins 1Y and 2Y when SELA and SELB (9F9) are low. These outputs are input to A171 and A193 and become available on the MUX bus by MUXEN0 (9K1).

When SELA is high and SELB is low, the hardware communication assist data lines HASD0:7 (9E9) become selected and propagate onto the MUX bus. Data input bus bits DI00:07 used by the hardware communication assist are gated through quad bus transceivers A181 (14F2) and A182 (14F4). The data is gated to the MUX bus by MSBENBO.

When SELA is low and SELB is high, the data communications interrupt device address bits (INTAD0:3) (9E1) and the data communications address bits (COMSW0:3) become selected. The data communications interrupt address bits (INTAD0:3) (9E1) make up the least significant nibble of the address line. The most significant nibble (COMSW0:3) is obtained from SW8 (IC A106) (9L7). In response to a RACK0 from the processor, the least significant nibble that was latched in the dual function chip A72, (6G6) together with the most significant nibble from SW8, propagate onto the MUX bus to form the address of the interrupting line to the processor.

When both SELA and SELB are high, the PIC/LFC interrupting address becomes selected. The input is either X'6C', the PIC address, or X'6D', the LFC address. When the PIC is the higher priority, clear PIC (CLRPIC0) at pin 3 of IC A83 is zero and the address available to the processor, in response to RACK0, is X'6C'. When the LFC is the higher priority, CLRPIC0 is high and the address to the processor is X'6D'. The two most significant address bits for the PIC/LFC in response to a RACKO are returned through quad bus transceiver A156 (9B9). Bits DI06:07 are also used throughout as the two most significant bits (MSBs) of a device address on the MPC (see Figure 2-6).

When the microprocessor is requested to handle a data available or command from the processor, the data byte DI8:15 is gated or read into the octal flip-flop A23 (5C8) by multiplexor in (MUXIN0) (5A9) to form buffered data byte (BD0:7) (5C9) to the microprocessor bus.

When the microprocessor is required to write a byte of data in response to a data request, it enables octal flip-flop A35 (5E2) by multiplexor out (MUXOUT0) (5A9) and transfers a byte of data from BD0:7 to DD0:7, which is a tristate internal bus available to the MUX bus.

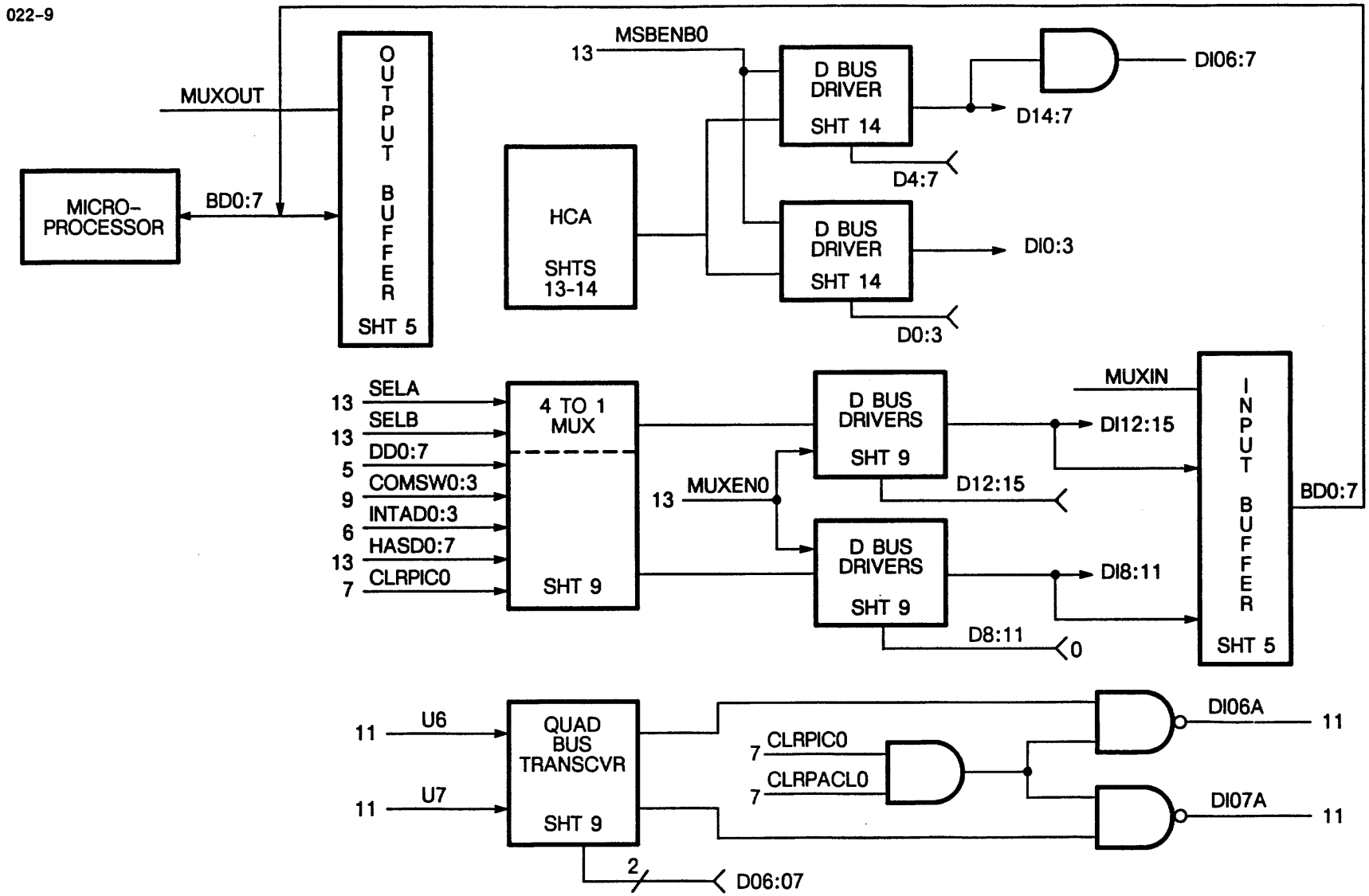


Figure 2-6 MUX Bus Data I/O

CHAPTER 3
LOADER STORAGE UNIT (LSU) OPERATION

3.1 INTRODUCTION

The LSU portion of the MPC is a microprocessor-controlled section that contains the initial program load (IPL) in ROM for common peripheral devices. This section also contains a timer (watchdog) which automatically restarts the LSU after a preprogrammed time if the load was unsuccessful.

3.2 LSU OPERATION

In systems containing an MPC board with the LSU enabled, the processor's microcode addresses the LSU (dedicated address X'05') during the power-up routine.

3.2.1 LSU Addressing

The LSU address is applied to A49 (see Figure 3-1) at an eight-input AND gate with the proper polarity to cause the output to a D-type flip-flop to be high. ADRS1 clocks the flip-flop which generates LSUAD0 at pin 15 of A49. This signal remains active until another device is addressed.

After the LSU is addressed and returns SYN0 to the processor, the processor sends data requests to the LSU causing IDR0 to go active and, in turn, LSUDR1. LSUDR1 active input to A108 activates LSUINT0.

The other inputs which cause LSUINT0 to go active are ICMD0 and IDA0. These signals are generated by the processor sending output commands or data to the MPC. These signals, in conjunction with LSUAD0, are a result of a software program sending data to the watchdog timer and enabling or disabling the timer (refer to Multiperipheral Controller (Multi-Layer MPC) Installation and Programming Manual for details).

The LSU section may be disabled by strapping 200-7 to 100-7 at E20 on the board. This grounds an input to A176, placing a low at the D-type input to the address flip-flop on A49. The other input to disable the LSU at A176 is from the processor IPL enable/disable logic.

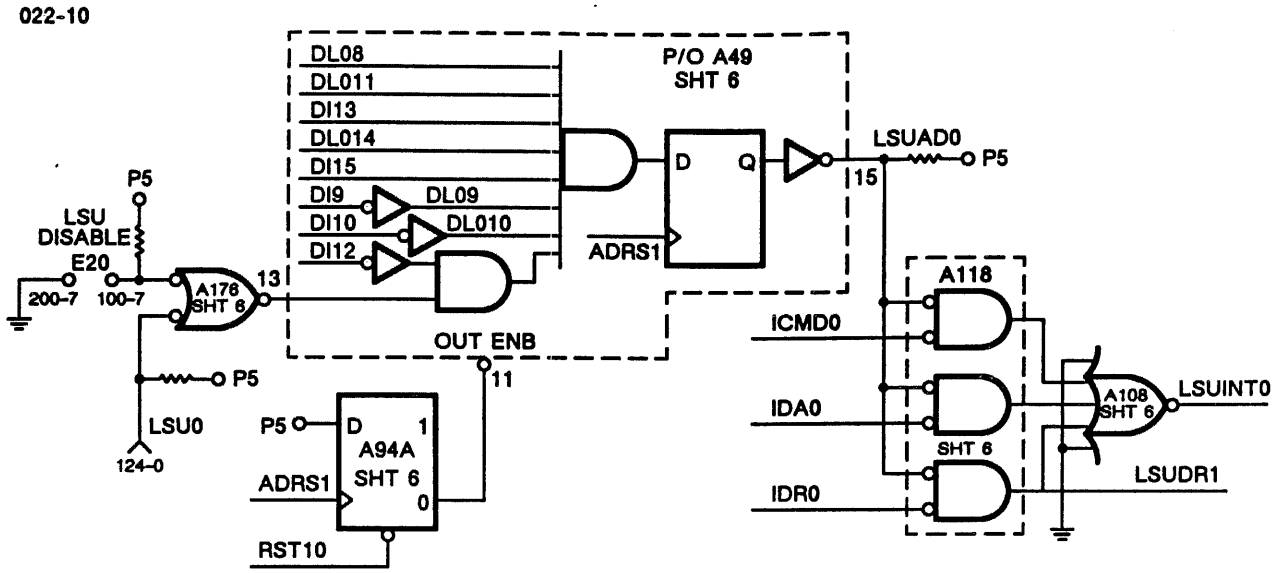


Figure 3-1 LSU Addressing

3.2.2 LSU Interrupt Control

When LSUAD0 is active and a data request or data available control line is activated, LSUINT0 is generated at A108. This signal is a level 2 input to the 8-3 line priority encoder A7 (see Figure 3-2). The binary code 2 is input to interrupt latch A15 where it is clocked and stored. The latched interrupt level 2 is input to the microprocessor interrupt priority level pins. The microprocessor responds by placing the interrupt level on pins A1:A3. All interrupts also cause microprocessor pins FC0:FC2 to go active high producing IACK1, enabling the 3-8 line decoder A153. The LSU interrupt generates AUTOVEC0 at A160 which is applied to the microprocessor input $\overline{\text{VPA}}$. When this signal is active, the microprocessor expects to receive an 8-bit value on the least significant byte (D0:7) of D0:15. This value is used to form the vector address used to branch to a routine to service the LSU interrupt.

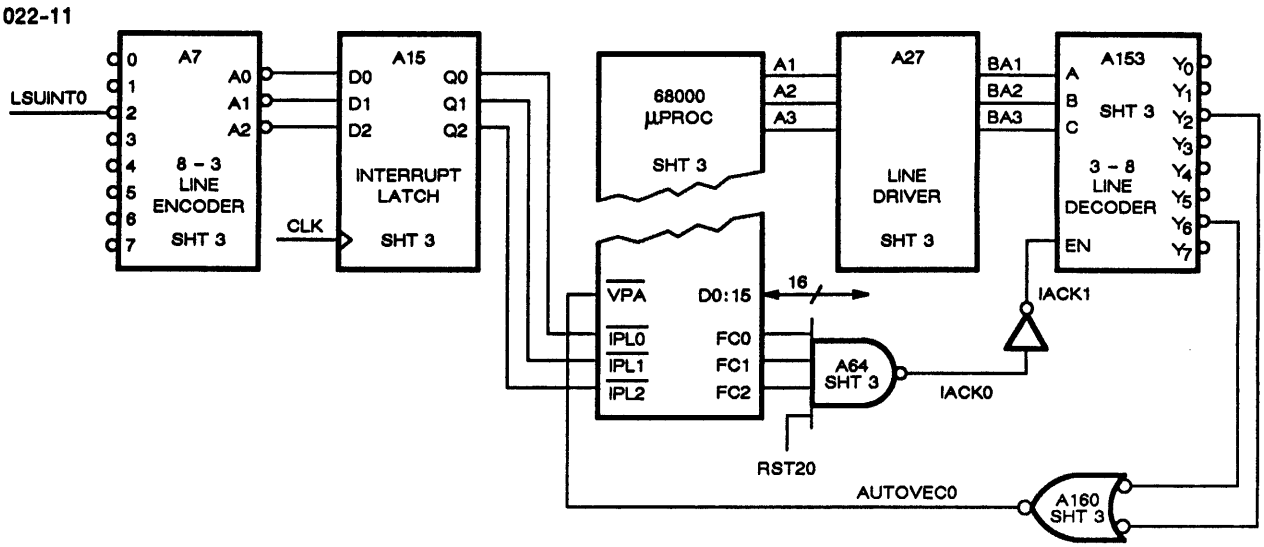


Figure 3-2 LSU Interrupt Control

3.2.3 LSU Data to Processor

Data requests from the processor, when the LSU is enabled and addressed, generate an output enable from A119 (see Figure 3-3) to A35. Data from the LSU ROM, placed on the inputs of A35 by the microprocessor LSU support program, is enabled to a 4 to 1 MUX bus output selector. The select pins SELA and SELB are low, which selects the data bus inputs. The select pins are controlled by programmable logic array (PLA) chip A115 (13B3) which has LSUAD0 active on pin 23. The output data from the 4 to 1 MUX is enabled to the MUX bus by the enable pin active on the transcievers. The enable signal (MUXEN0) is generated by PLA chip A115 (13B3). The data byte to the processor is accompanied by a SYN0 signal generated by PLA chip A115, delayed through flip-flop A166 and gated out of A137 (13F2) to the MUX bus.

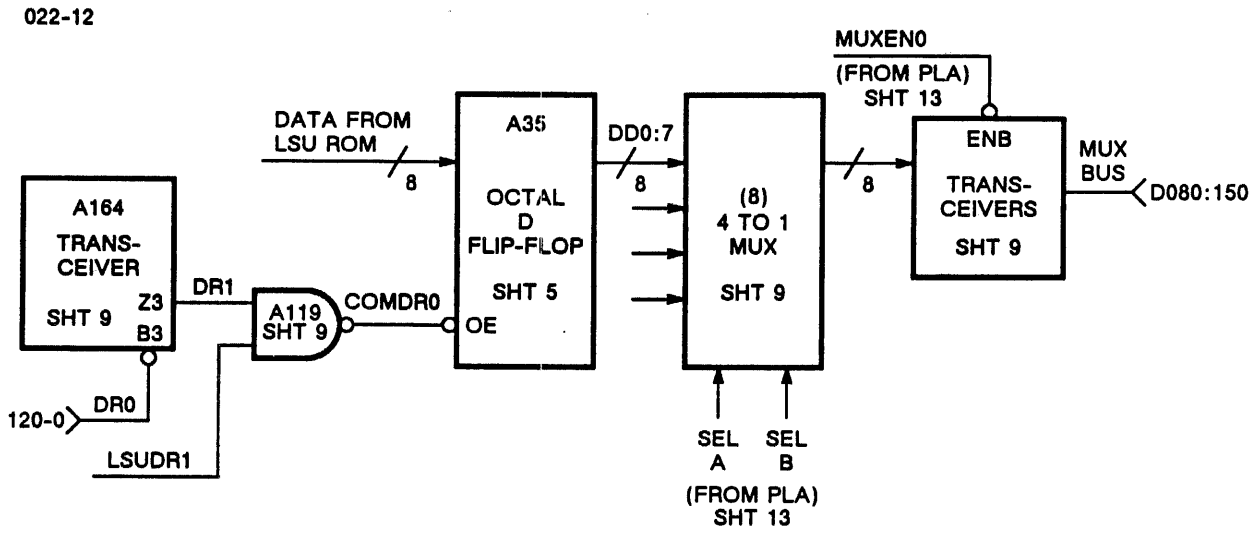


Figure 3-3 LSU Data Flow

CHAPTER 4
MICROPROCESSOR-CONTROLLED 8-LINE COMMUNICATIONS MULTIPLEXOR (COMM MUX)

4.1 INTRODUCTION

The following sections describe the communications section consisting of the microprocessor signals, memory decoder, erasable programmable read-only memory (EPROM) and random access memory (RAM), I/O register decoder, and 8-channel data COMM MUX.

4.2 MICROPROCESSOR

The microprocessor (IC A16) (Sheet 3) uses 15 address lines (A1:15) (3J3) and 16 data lines (D0:15) (3J6). Through these lines, the microprocessor reads from EPROM and reads/writes to RAM, controls the eight data COMM MUXs contained in four serial communications controllers, and sets or resets I/O associated control logic. Most of the operations are interrupt-driven using the interrupt priority level inputs (IPL0:2) (3G7) and the function code outputs (FC0:2) (3H7). See Figure 4-1.

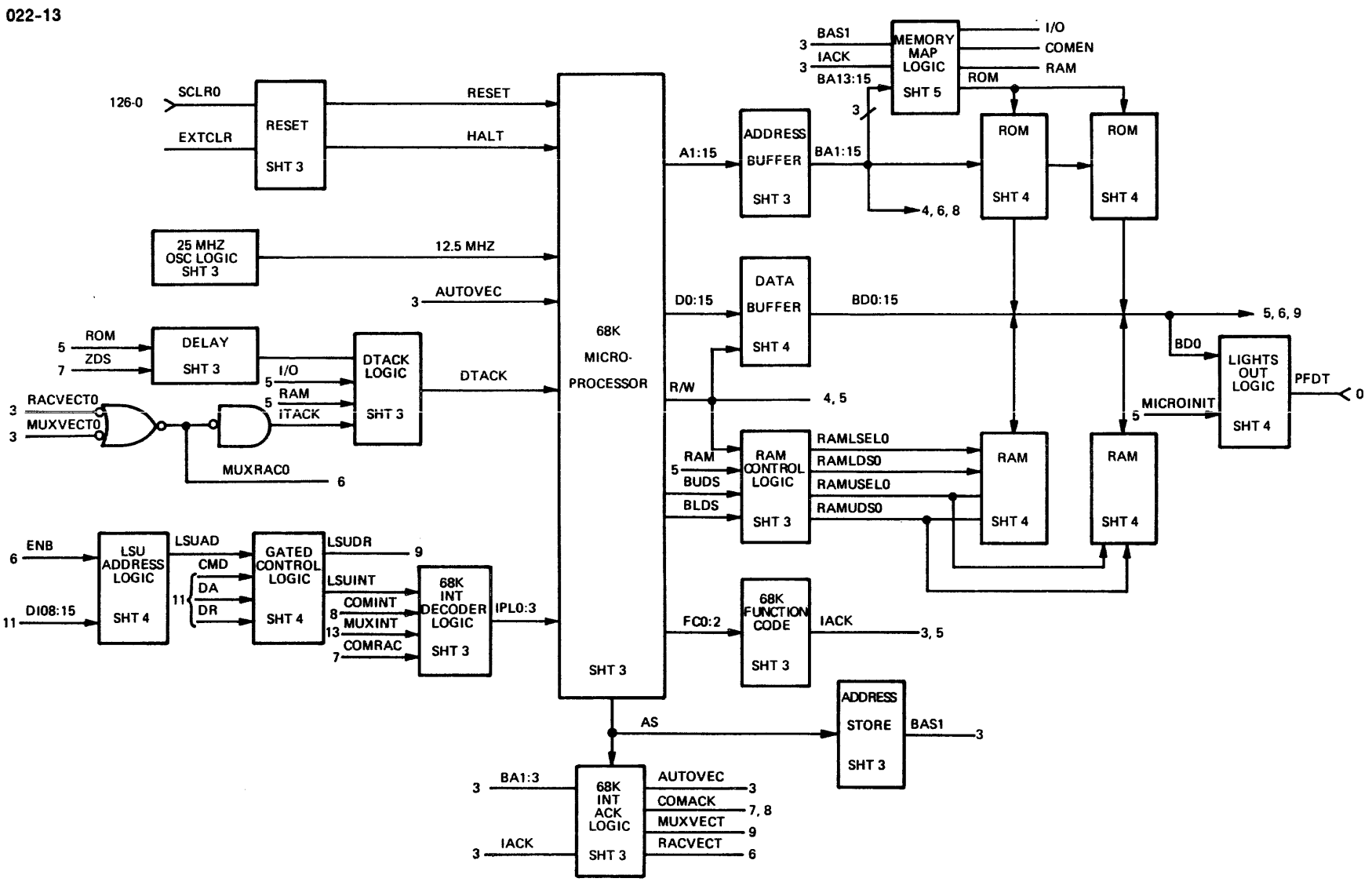


Figure 4-1 Microprocessor Functional Logic

The microprocessor operates on 12.5MHz, which is obtained from a 25MHz oscillator A120 (3A3). The oscillator is divided by two (A111) (3A3). The 12.5MHz is buffered by a driver/receiver (A101) (3E3) to produce MCLK and SCLK used for buffering and loading.

- Reset/halt (pins 18, 17)

  When the system is powered up or initialized, the system clear (SCLR0) signal (3B1) is activated to clear the system. SCLR0 also holds the microprocessor RESET pin (pin 18) and HALT pin (pin 17) (3G2) low for more than 100ms. The initialization sequence forces the microprocessor to vector the initial power-up, starting parameter location in the EPROM. The EPROM then starts execution of the MPC firmware. The external clear test point (3A2) enables the user to provide an internal systems clear without initializing the system.

- Address bus (A1:15) (pins 29:43)

  The MPC uses 15 bits of the 23-bit, tristate, unidirectional address bus (3J3). The 15 address bits (A1:15) are buffered at A27 (3K3) and A26 (3K6) and provide the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide information to a 3 to 8 decoder (A153) (3G9), indicating what level interrupt is being serviced while address lines A4:15 are all set to a logic high.

- Data bus (D0:15) (pins 5:1, 64:54)

  This 16-bit, tristate, bidirectional data bus is the general-purpose data path. It can transfer and accept data halfwords or bytes. During an interrupt acknowledge cycle, the internal interrupting device supplies the vector address on data lines D0:7 (3L7). IC A25 (LSB) (4E8) and IC A43 (MSB) (4E7) provide buffering for all the data signals.

- Address strobe (AS) (pin 6)

  This low-active signal indicates that there is a valid address on the address bus.

- Read/write (R/W) (pin 9)

  This signal defines the data bus transfer as a read or a write cycle. When the R/W is high, the microprocessor reads from the data bus. When R/W is low, data is written to the data bus (see Figures 4-2 and 4-3).

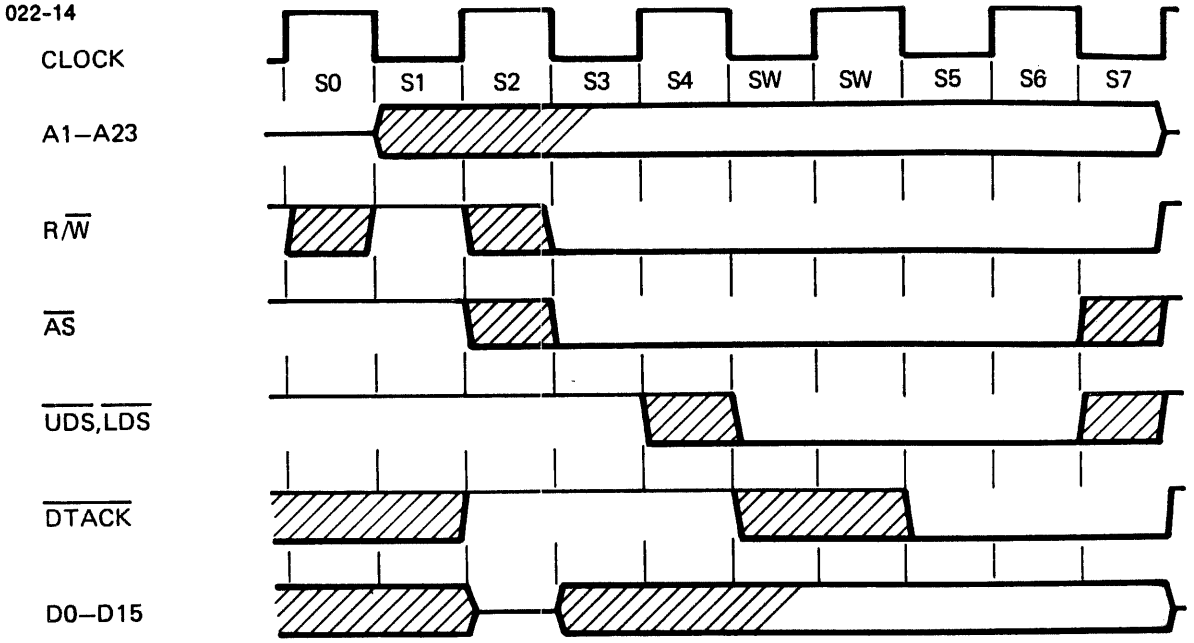


Figure 4-2 Microprocessor Write

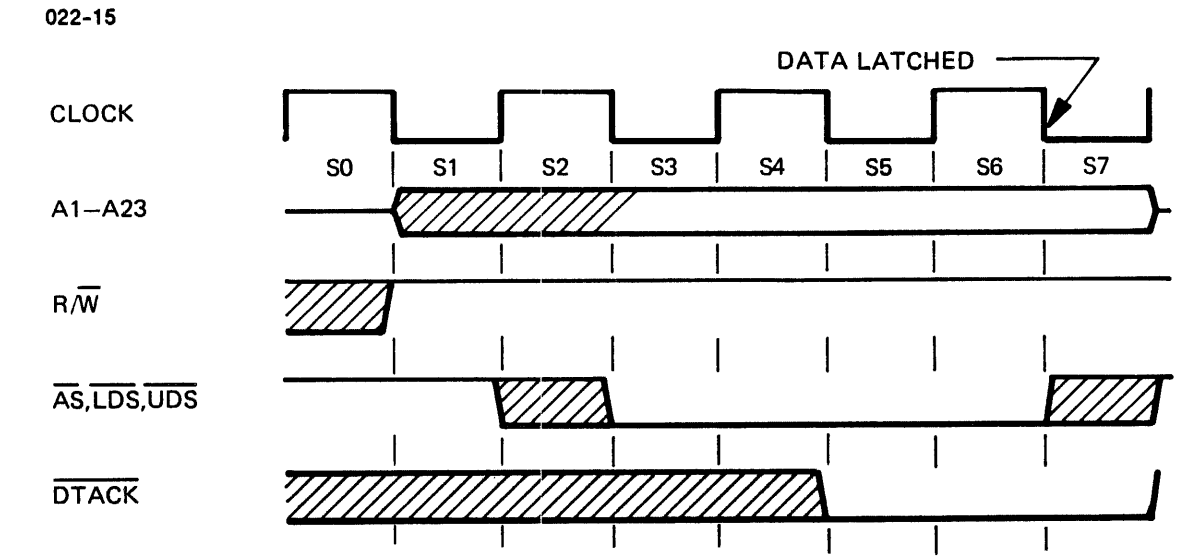


Figure 4-3 Microprocessor Read

- Upper data strobe/lower data strobe (UDS/LDS) (pin 7, 8)

  When LDS goes low (pin 8) (3J5), the microprocessor expects a byte of valid data on the LSB (D0:7). When UDS goes low (pin 7) (3J5), the microprocessor expects a byte of valid data on the MSB (D8:15). When they both go low, the microprocessor expects one halfword of valid data. All the on-board accesses for the processor, with the exception of EPROM and RAM accesses, are 1-byte references and require LDS only. The RAM can be a byte or halfword access but the EPROM accesses require both LDS and UDS.

- Data transfer acknowledge (DTACK) (pin 10)

  DTACK is the handshake signal the microprocessor receives to complete any cycle: read/write or interrupt acknowledge. Therefore, any operation the microprocessor performs requires the return of this signal. Failure to return DTACK causes the microprocessor to hang and the MPC to malfunction. Address cycles may require delays or wait states to allow slower devices to operate correctly. There are no wait states for the RAM or I/O but the EPROM and serial communications controllers require two wait states. These two wait states are generated through IC A99 (3B5). The 4-bit counter (IC A99) is preset by ROM0 and ZDS0 with X'D'. When the counter increments to X'F', a carry becomes available on pin 15 and ROMCK1 (3D5) is generated, producing DTACK to the microprocessor. Other signals that satisfy and generate DTACK are OR-tied: (IC A109) (3F6) I/O mapping enable (IO0), MUX bus interrupt acknowledge for the microprocessor (ITACK1), and RAM selected (RAM0).

- Interrupt priority level/function codes (IPL/FCO) (pins 23:25, 26:28)

  The IPL0:2 inputs from IC A15 (3B7) respond to interrupt priority level codes 0 through 7. Codes 1 through 7 are valid with 7 being the highest and 0 the lowest, indicating no interrupt. The codes are negative logic, meaning a zero is all ones on pins 23:25 (3G7). The interrupts available to the microprocessor are communication receive acknowledge (COMRAC), MUX bus interrupt (MUXINT0), serial communications controller interrupt (COMINT0) (3A7), and LSU interrupt (LSUINT0) (3C9).

  The highest interrupt, level 5, is the communication receive acknowledge (COMRAC0), indicating that an interrupt acknowledge (RACK0) from the processor is pending for one of the sixteen addresses of the data communications channels. This interrupt preempts all other interrupts.

  The level 4 interrupt is the MUX bus interrupt (MUXINT0), indicating that the processor wants the microprocessor to perform an I/O function (CMD, DA, or DR). This interrupt preempts any level 3 interrupts.

The level 3 interrupt is the communications interrupt (COMINT0) from one of the eight data communications channels indicating to the microprocessor that a channel operation must be serviced.

The LSU interrupt (LSUINT0) is level 2. It indicates that the processor is requesting the LSU bootstrap program or that a request is being made to the watchdog timer.

These interrupt signals at the output of IC A15 are inputs to the priority encoder A07 (3E9), which feeds back to A15 and produces the interrupt level requests to the microprocessor on pins 23:25.

IC A153 (3G9) is a 3 to 8 decoder that the microprocessor uses to acknowledge an interruption at the IPL pins. The microprocessor reacts to an interrupt as follows: it places the level of the interrupt on pins A1:3 (3K3) and generates a function code through FC0:2 of all ones to produce interrupt acknowledge (IACK1) (3K7). IACK1 enables the 3 to 8 decoder to decode the interrupt level present at BA1:3 (3F8), generating the LSU automatic vector (AUTOVEC0) (3J8), data communications acknowledge (COMACK0), MUX vector (MUXVECT0), or data communications channel vector (RACVECT0). These are the respective interrupt acknowledge signals to LSUINT0, COMINT0, MUXINT0, and COMRAC0. When these signals go active, the microprocessor expects to receive an 8-bit value on the least significant byte (D0:7) of D0:15. This value is used to form the vector address which is used to branch to a routine to service the interrupts.

Nesting of two interrupts is possible. For example, during normal operation, if COMINT0 goes low to the microprocessor, the microprocessor goes into an interrupt service routine (ISR) to service the interrupt. At that time, if MUXINT0 or COMRAC0 asynchronously goes low, an interrupt is generated at a higher priority. This pulls the microprocessor out of the current ISR (COMINT0) and services the higher priority interrupt, returning to the lower one upon completion.

4.3 MEMORY MAPPING

IC A144 (5H6) is a 3 to 8 line decoder that segments the addressing range of the microprocessor into different areas and functions. IC A144 decodes bits BA13:15 and determines whether it is an EPROM access, RAM access, 8K, on-board I/O access, or a serial communications controller access signal (see Table 4-1). If the first two outputs from IC A144 (Y0,Y1) (ROM0) are low, the microprocessor wishes to fetch instruction data from the EPROM. The Y2 output (RAM0) is a RAM access, Y3 is an 8K access, the Y4 output (COMEN0) is for data channel MUXs, and the Y6 output (IO0) is for I/O. When I/O is decoded by the microprocessor, the microprocessor wants to access an on-board register.

TABLE 4-1 MICROPROCESSOR MEMORY MAP

ACCESS SIGNALS	BUFFERED ADDRESS BITS																	
	23-16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPROM	'00'	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X
RAM	'00'	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X
8K	'00'	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
SERIAL COMMUNICATIONS CONTROLLER	'FF'	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X
I/O REGISTER	'FF'	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X

4.4 EPROM AND RAM

The MPC includes 56kB of control store (16kB of EPROM, 8kB of RAM and 32kB of optional EPROM). See Sheet 4 of schematic diagram 35-910 D08.

ICs A44 and A53 are the two 8kB x 8 EPROMs that contain the control store and internal LSU code. On power-up, the diagnostics that are contained in the EPROMs are run. When the diagnostics have successfully completed, the microprocessor transfers the microcode that controls the 8-channel data COMM MUX ICs to the RAMs (A73, A79, A66, and A67). Subsequently, all operations to service the lines are from the RAM. The optional EPROM A26A contain the external LSU code.

4.5 INPUT/OUTPUT (I/O) REGISTER CONTROL

The 3 to 8 line decoders, A125 (5H2) and A134 (5L2), are the I/O register control signal drivers. Whenever the microprocessor has to perform a function that requires moving data in or out, the data control is accomplished by the microcode sending a code (shown in Table 4-2) to either A125 or A134. For example, if the microprocessor wants to read the current RING condition of all eight lines through A63 (5B2), the following occurs. First, the I/O access from IC A144 (5H6) is selected by placing a code 6, using BA13:15, into pins 1, 2, and 3 (1 low, 2 and 3 high). When this occurs and the address strobe (BASIA) input to pin 6 goes high and IACK1 is low, IO0 becomes active and enables A125 or A134. Next, A134 (5H4) selects which register to use. As a result, BA8 is a 1 and BA9 is a 0; the output selected is Y1 which enables A134. When all these conditions are met and code 2 is presented by BA1:3 to pins 1, 2, and 3 (1 and 3 low, 2 high) of IC A134, RIR0 (5M2) becomes active and is input to A63 which enables this gate to transfer data to the BD0:7 bus, allowing the microprocessor to interrogate it. Format of the register contents is shown in Table 4-3.

TABLE 4-2 I/O REGISTER ASSIGNMENTS

	BUFFERED ADDRESS BITS																			
	23-16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Decoded Bits									Decoded Bits							
RCTL1	'FF'	1	1	0	0	0	0	0	0	line			r/t	0	0	0	1
MUXOUT	'FF'	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
MUXIN	'FF'	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1
68K SYNC	'FF'	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1
STATUS	'FF'	1	1	0	0	0	0	0	0	line			r/t	1	0	0	1
BITS	'FF'	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1
BDR	'FF'	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1
SPARE	'FF'	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1
MXSGL	'FF'	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1
DSR	'FF'	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1
RIR	'FF'	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1
SETATN0	'FF'	1	1	0	0	0	0	0	1	0	L0-3		r/t	0	1	1	1
SETATN1	'FF'	1	1	0	0	0	0	0	0	0	L4-7		r/t	1	0	0	1
SPARE	'FF'	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1
M-INIT	'FF'	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1
SPARE	'FF'	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1

r/t 0 = Receive
1 = Transmit

line = serial communication controller line address 0:7

TABLE 4-3 I/O REGISTER FORMATS

	7	6	5	4	3	2	1	0
RCTL1	DIS	EN	MUX INTPT	TPE	TPB	COM	0	0
MXSGL	SR	DR	DA	CMD	DI12	DI13	DI14	DI15
MUXIN/MUXOUT	DI08	DI09	DI10	DI11	DI12	DI13	DI14	DI15
DSR	L7	L6	L5	L4	L3	L2	L1	L0
RIR	L7	L6	L5	L4	L3	L2	L1	L0
BITS	0	1	0	0	DI12	1	DI14	DI13
BDR (Constant)	X	X	X	X	X	X	X	X

4.6 STATUS RANDOM ACCESS MEMORY (RAM)

ICs A71 (5H7) and A59 (5M7) are the status RAMs for the eight lines. These are dual-ported RAMs and have 16 locations. The microprocessor writes the status information for each line as it becomes available and the processor reads the status from the status RAM asynchronously. The microprocessor can read this information from the second port for verification from the outputs YB0:3 to the BD0:7 bus. The YA0:3 outputs from each status RAM are latched before going to DD0:7 which becomes available to the processor. The addressing of the status RAM is accomplished in two ways; on the left side BA4:7 (B0:3) represent the addressing from the microprocessor and, on the right side, CAD12:15 (A0:3) represent the addressing from the processor. See Table 4-4 for the addresses of the dual-ported RAMs for the particular lines. For example, when the microprocessor writes to the transmit side of line 4, it places the address code 9 on pins 4, 5, 6, and 7 of A71 and A59. At the same time that STATUS0 is presented to the write enable pin 3 (decoded by A125), valid data from the BD0:7 bus is placed on pins 1, 2, 26, and 27 on both chips together with BR/W (pin 25) going low-active, latches

the data into the status RAM. Reading to the microprocessor is the same except BR/W is high-active on pin 25 and is used to enable the output on pin 19, presenting the data to the BD0:7 bus through pins 10, 12, 15, and 17 on both chips. The processor reads data by placing the address code from CAD12:15 onto pins 21, 22, 23, and 24 on both chips. The YB bus output from the RAM to the processor is always enabled to A71A and latched by FSR1. COMSR0 enables the status to the DD0:7 bus where it is multiplexed to the MUX bus (Sheet 9). Verification of the status RAM is performed when the power-up diagnostics are run.

TABLE 4-4 STATUS RAM ADDRESSES

	BA15:13	BA12:8	BA7:4	BA3:0
LINE	I/O OPERATION	ZERO	LINE	MUX STATUS OPERATION
0RCV	C	0	0	9
0XMIT	C	0	1	9
1RCV	C	0	2	9
1XMIT	C	0	3	9
2RCV	C	0	4	9
2XMIT	C	0	5	9
3RCV	C	0	6	9
3XMIT	C	0	7	9
4RCV	C	0	8	9
4XMIT	C	0	9	9
5RCV	C	0	A	9
5XMIT	C	0	B	9
6RCV	C	0	C	9
6XMIT	C	0	D	9
7RCV	C	0	E	9
7XMIT	C	0	F	9

4.7 ERROR LED INDICATOR

The LED connected to IC A150 (12L8) is normally blinking. If the microprocessor malfunctions, the LED remains lit. If the PIC oscillator fails, the LED remains off. This is controlled by setting the flip-flop once every time the microprocessor goes through its idle loop and resetting it once every .5ms by the PIC oscillator. For more information on the LED, see the flowchart in Appendix B.

4.8 RECOGNITION OF MUX BUS REQUESTS

Table 4-5 shows how a vector address is created and presented to the microprocessor for an output command, data request, data available, or sending RACK0 to a particular line.

When the microprocessor is interrupted, it finishes the current instruction it is executing and goes into an ISR sequence where it fetches a vector value. This vector byte value is formed in the following manner. MUX bus bits 12 through 15 contain the address of the COMM MUX channel sent by the processor. These MUX bus bits become BD bus bits 0 through 3. BD bus bits 4 through 7 are formed as follows. Bit 7 is forced to a binary 1. Bit 6 is set when the interrupt is due to a data request (DR) by the processor. Bit 5 is set when the interrupt is due to a data available (DA) sent by the processor. Bit 4 is set when the processor issues an output command (OC). If the OC is sent, MUX A117 (6H3) switches BD bus bits 6 and 5 to reflect MUX bus bits 10 and 15, respectively. Bit 10 is set when data terminal ready (DTR) is set in the OC and bit 15 is set for a Command 1 and reset for a Command 2.

The byte that is formed on BD bus lines 0 through 7 have two additional bits appended by the microprocessor, and the resulting ten bits form the vector address to the microprocessor program to process the interrupt.

TABLE 4-5 VECTOR ADDRESS DECODER

BD BUS BITS							
7	6	5	4	3	2	1	0
FUNCTION				MUX Bus bits			
1	x	y	z	12	13	14	15
				CHANNEL ADDRESS			

Vector locations in EPROM after calculation

1xyz	0000	AA	MUX	BUS	CONTROL RCV	LINE 0
1xyz	0001	AA	MUX	BUS	CONTROL XMIT	LINE 0
1xyz	0010	AA	MUX	BUS	CONTROL RCV	LINE 1
1xyz	0011	AA	MUX	BUS	CONTROL XMIT	LINE 1
1xyz	0100	AA	MUX	BUS	CONTROL RCV	LINE 2
1xyz	0101	AA	MUX	BUS	CONTROL XMIT	LINE 2
1xyz	0110	AA	MUX	BUS	CONTROL RCV	LINE 3
1xyz	0111	AA	MUX	BUS	CONTROL XMIT	LINE 3
1xyz	1000	AA	MUX	BUS	CONTROL RCV	LINE 4
1xyz	1001	AA	MUX	BUS	CONTROL XMIT	LINE 4
1xyz	1010	AA	MUX	BUS	CONTROL RCV	LINE 5
1xyz	1011	AA	MUX	BUS	CONTROL XMIT	LINE 5
1xyz	1100	AA	MUX	BUS	CONTROL RCV	LINE 6
1xyz	1101	AA	MUX	BUS	CONTROL XMIT	LINE 6
1xyz	1110	AA	MUX	BUS	CONTROL RCV	LINE 7
1xyz	1111	AA	MUX	BUS	CONTROL XMIT	LINE 7

x = DR if z = 0, x = DTR if z = 1
y = DA if z = 0, y = CMD if z = 1
z = 1 if OC, otherwise z = 0
AA = Appended by microprocessor

4.9 SERIAL COMMUNICATIONS CONTROLLER ADDRESSES

IC A96 (9L5) decodes the six most significant bits (MSBs) (D06:11) of the address recognition circuit for the serial communications controllers. SW8 (IC A106) (9L7) is the only line address selection switch on the MPC. The setting of this switch generates four outputs (COMSW0:3). When the setting coincides with data on the MUX bus, it produces COMEQL1, which is input to flip-flop A133 (9L9). The leading edge of the address pulse (ADRS1) sets the flip-flop producing a COMAD1 output. The four least significant bits (LSBs) (DI12:15) are latched into A52 (5M4) with ADRS1 and distinguish the individual line addresses by generating CAD12:15 (see Figure 4-4).

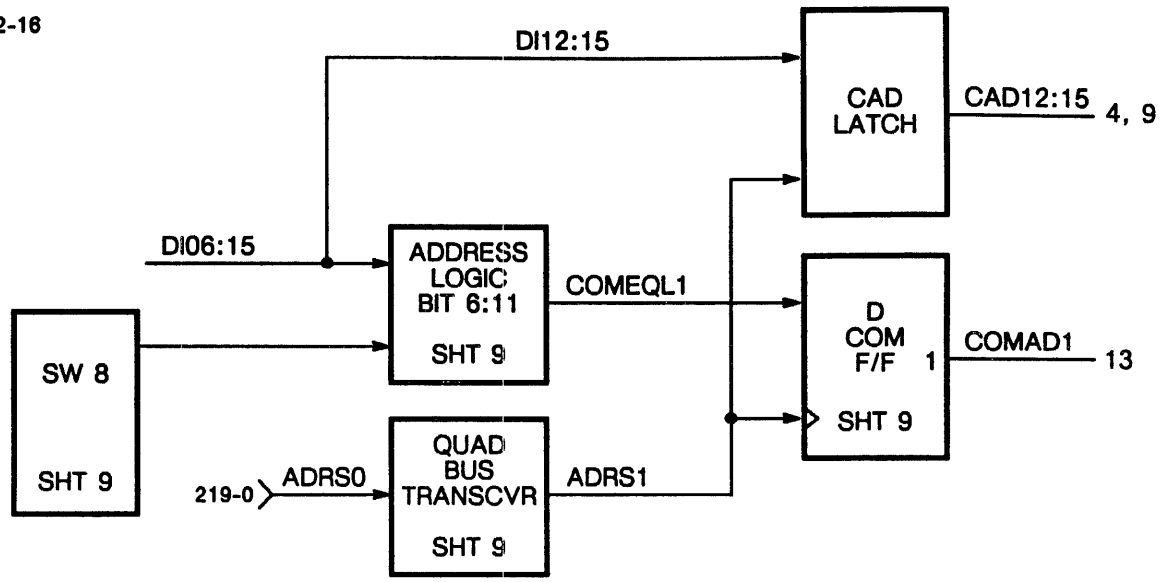


Figure 4-4 Serial Communications Controller Addresses

- Address

  Table 4-6 shows the address assignments used by the microprocessor microcode for the serial communications controllers internal register selection.

TABLE 4-6 SERIAL COMMUNICATIONS CONTROLLER ADDRESS ASSIGNMENTS

HEX ADDRESS			
BA23:08	BA07:00		REGISTER
CHANNEL B			
X'FF80'	aa00	1	WR0B OR RR0B
X'FF80'	aa00	3	WR1B OR RR1B
X'FF80'	aa00	5	WR2 OR RR2B
X'FF80'	aa00	7	WR3B OR RR3B
X'FF80'	aa00	9	WR4B --
X'FF80'	aa00	B	WR5B --
X'FF80'	aa00	D	WR6B --
X'FF80'	aa00	F	WR7B --
X'FF80'	aa01	1	WR8B OR RR8B
X'FF80'	aa01	3	WR9 --
X'FF80'	aa01	5	WR10B OR RR10B
X'FF80'	aa01	7	WR11B --
X'FF80'	aa01	9	WR12B OR RR12B
X'FF80'	aa01	B	WR13B OR RR13B
X'FF80'	aa01	D	WR14B --
X'FF80'	aa01	F	WR15B OR RR15B
CHANNEL A			
X'FF80'	aa10	1	WR0A OR RR0A
X'FF80'	aa10	3	WR1A OR RR1A
X'FF80'	aa10	5	WR2 OR RR2A
X'FF80'	aa10	7	WR3A OR RR3A
X'FF80'	aa10	9	WR4A --
X'FF80'	aa10	B	WR5A --
X'FF80'	aa10	D	WR6A --
X'FF80'	aa10	F	WR7A --
X'FF80'	aa11	1	WR8A OR RR8A
X'FF80'	aa11	3	WR9 --
X'FF80'	aa11	5	WR10A OR RR10A
X'FF80'	aa11	7	WR11A --
X'FF80'	aa11	9	WR12A OR RR12A
X'FF80'	aa11	B	WR13A OR RR13A
X'FF80'	aa11	D	WR14A --
X'FF80'	aa11	F	WR15A OR RR15A

aa (BA6:7) selects one of four serial communications controllers

4.10 BUS TRANSLATOR

A state machine that converts the microprocessor bus protocol into the serial communications controller bus protocol is shown at the bottom of Sheet 7 of schematic diagram 35-910 D08.

ZAS0 (7L6) is the address strobe to the serial communications controllers and ZDS0 (7L7) is the data strobe to the serial communications controllers. SELD0 (7L8) serves as the control signal that multiplexes the address or data to/from the serial communications controller bus.

SELD0 serves as a gating switch for the data buffer (IC A625) (4B5) while SELD1 serves as the gating switch for the address buffer (IC A51) (8N5).

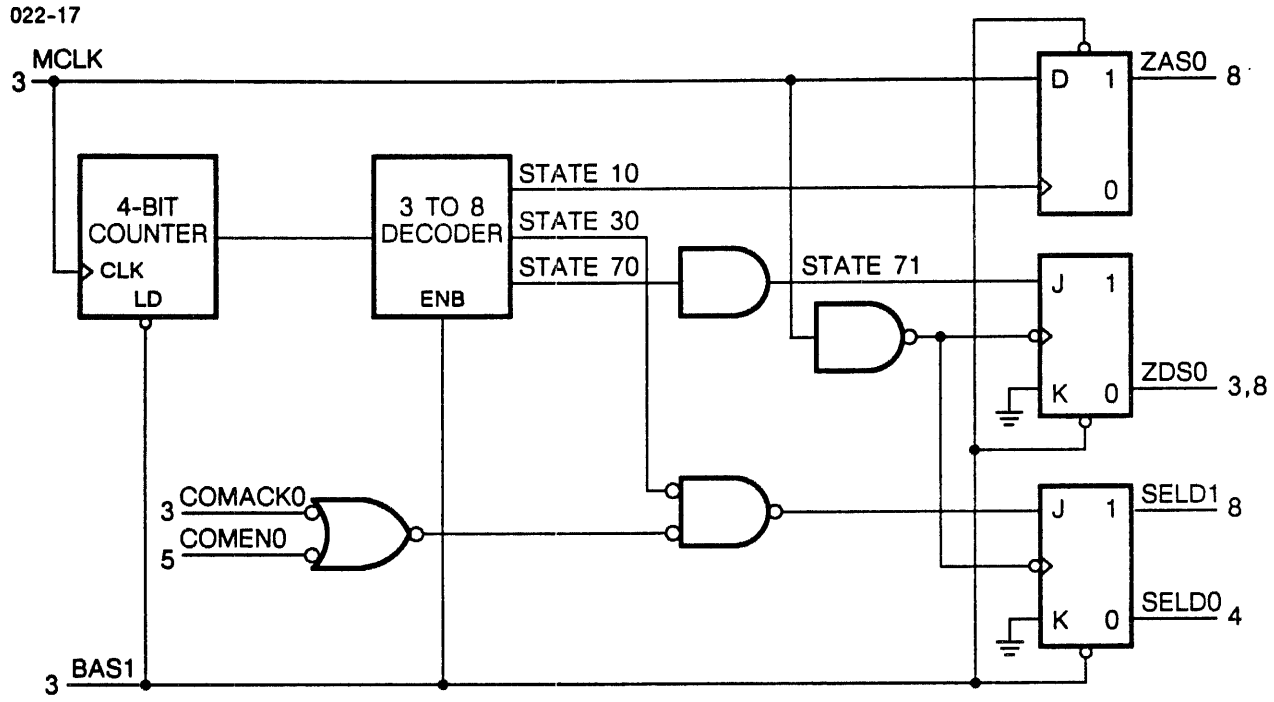


Figure 4-5 Bus Translator Logic

- Serial communications controller select logic

  The serial communications controllers are selected through IC A134 (5H4) depending on BA6 or BA7. When IC A144 output (COMEN0) (5J6) is active, the bit states of BA6:7 select one of four controller enable signals (COM1:4).

- Serial communications controller buffer logic

  The address and data directed to the serial communications controller are multiplexed to AD0:7 by IC A62 (4B7) and IC A51 (8N5). IC A62 receives the LSB of the microprocessor data bus and IC A51 receives the microprocessor address bus BA1:7. The state of SELD1 (7L9) selects whether the address or the data is present to the serial communications controller. When ZAS0 (7M7) goes low, whatever is present on the AD lines is the address. When ZDS0 (7M8) goes low, data is written to or read from the serial communications controller. See Figure 4-6.

When reading from the serial communications controller, either data or an interrupt vector is present at ZDS0 time.

- Serial communications controller logic

  The four serial communications controllers, A70, A104, A174, and A196 (Sheet 8), make up the 8-channel data COMM MUXs. The serial communications controllers supply all the data communications facilities on the MPC, including all modem control signals, recognition, and generation with the exception of RING, and data set ready (DSR), which the microprocessor samples in its idle loop. The modem cable ring conditions (L0RI:L7RI), which detect if the phone is ringing on a dial-up line, are fed to A63 (5B2). The DSR conditions (DSR00:DSR70), indicating the presence of a modem or terminal, are fed to A50 (5B6). See Figure 4-6.

- Serial communications controller drivers logic

  The RS-232C drivers/receivers are on Sheets 15 and 16 of schematic diagram 35-910 D08. These ICs interface the data/control signals to and from the modem or terminal. The control signals DSR, DCD, CL2S, and RING can be disabled through switches SW3, SW4, SW5, or SW6.

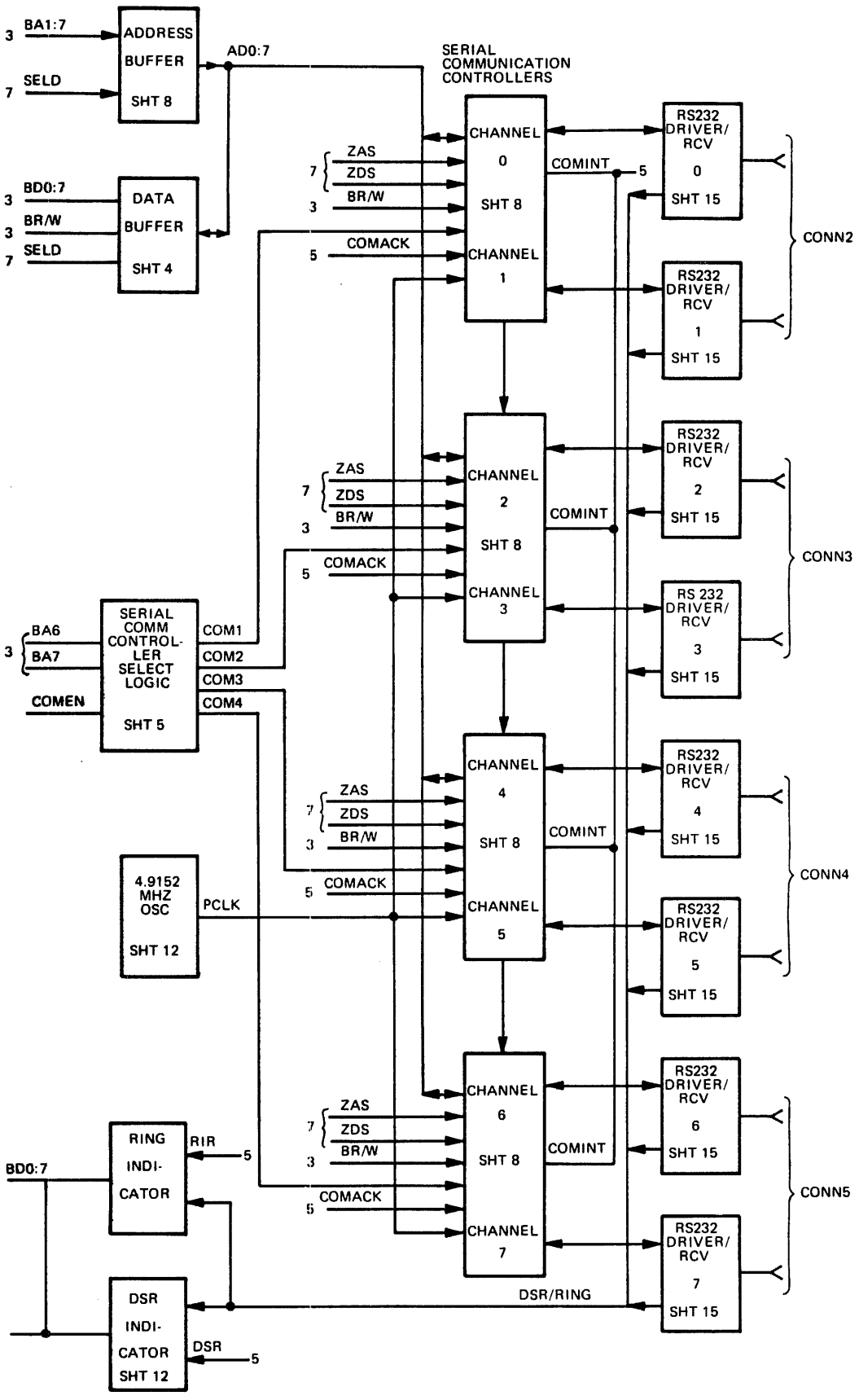


Figure 4-6 Serial Communications Controller I/O Logic

- Interrupts to microprocessor

  The serial communications controller ICs generate interrupts to the microprocessor on level 3. Each serial communications controller is assigned an interrupt vector in WR2 for each channel, shown in Table 4-7, which is used by the microcode.

TABLE 4-7 8-DATA CHANNEL INTERRUPTS TO MICROPROCESSOR

SERIAL COMMUNICATIONS CONTROLLER	FRONT EDGE CONNECTOR	DATA CHANNELS	VECTOR
1	2	0 - 1	40
2	3	2 - 3	50
3	4	4 - 5	60
4	5	6 - 7	70

The serial communications controller data channels interrupt the microprocessor on the following conditions:

- Character received, no error
- Character received, parity or framing error
- First-in/first-out (FIFO) overflow
- Modem signal change, clear to send or data carrier detect
- Break or abort in synchronous mode
- Transmitter buffer empty

Each serial communications controller modifies the least significant nibble of the interrupt vector to identify the data channel and the cause of the interrupt. The ICs are daisy-chained in priority. This is done by the signals IE0/IE1 between pins 6 and 7 of the serial communications controllers. Channel 0 has the highest priority and it toggles IE0 pin 6 low to disable all other serial communications controller ICs from generating any interrupts to the microprocessor. All channels could have an interrupt pending to the microprocessor via COMINT0 (pin 5). However, only the one with the highest priority, as determined by the serial communications controllers, responds to the microprocessor acknowledging the interrupt via the COMACK0 (8A4) signal.

- Interrupts to the processor

  When the microprocessor wishes to interrupt the processor on behalf of any of the eight channels, it generates that interrupt by writing a bit into one of the two 8-bit addressable latches by using one of the addresses shown in Table 4-8. For example, if the microprocessor wants to interrupt on line 0, the transmit side, the microprocessor sets Q1 of the 8-bit latch (A90) (6C6). This is accomplished by placing the line address code on BA4:6. In this case, BA4 is high, BA5 and BA6 are low, and BD0 is set to a 1, which generates the strobe SETATN00. This sets a 1 into the 8-bit latch at 6C6. The output is an input to FPLA A91, which prioritizes the interrupt, and, if there are no higher pending interrupts it generates the code 001 at its output pins 15:18. Pin 13 (COMATN0) also becomes active, which generates an interrupt on the MUX bus (Sheet 7). Priority at A91 is descending from top to bottom with the highest priority being pin 09, which is the receive side of line 0, and the lowest priority at pin 20, which is the transmit side of line 7. If any of the lines are active simultaneously, they are serviced from the processor one at a time (see Figure 4-7).

TABLE 4-8 ATTENTION LINE ADDRESSES

(A90)

	BA15:12	BA11:8	BA7:4	BA3:0
LINE	I/O OPERATION	I/O REGISTER 2	LINE 0:3	SET ATN0 OPERATION
0REC	C	1	0	7
0XMIT	C	1	1	7
1REC	C	1	2	7
1XMIT	C	1	3	7
2REC	C	1	4	7
2XMIT	C	1	5	7
3REC	C	1	6	7
3XMIT	C	1	7	7

(A78)

	BA15:12	BA11:8	BA7:4	BA3:0
LINE	I/O OPERATION	I/O REGISTER 2	LINE 4:7	SET ATN0 OPERATION
4REC	C	1	0	9
4XMIT	C	1	1	9
5REC	C	1	2	9
5XMIT	C	1	3	9
6REC	C	1	4	9
6XMIT	C	1	5	9
7REC	C	1	6	9
7XMIT	C	1	7	9

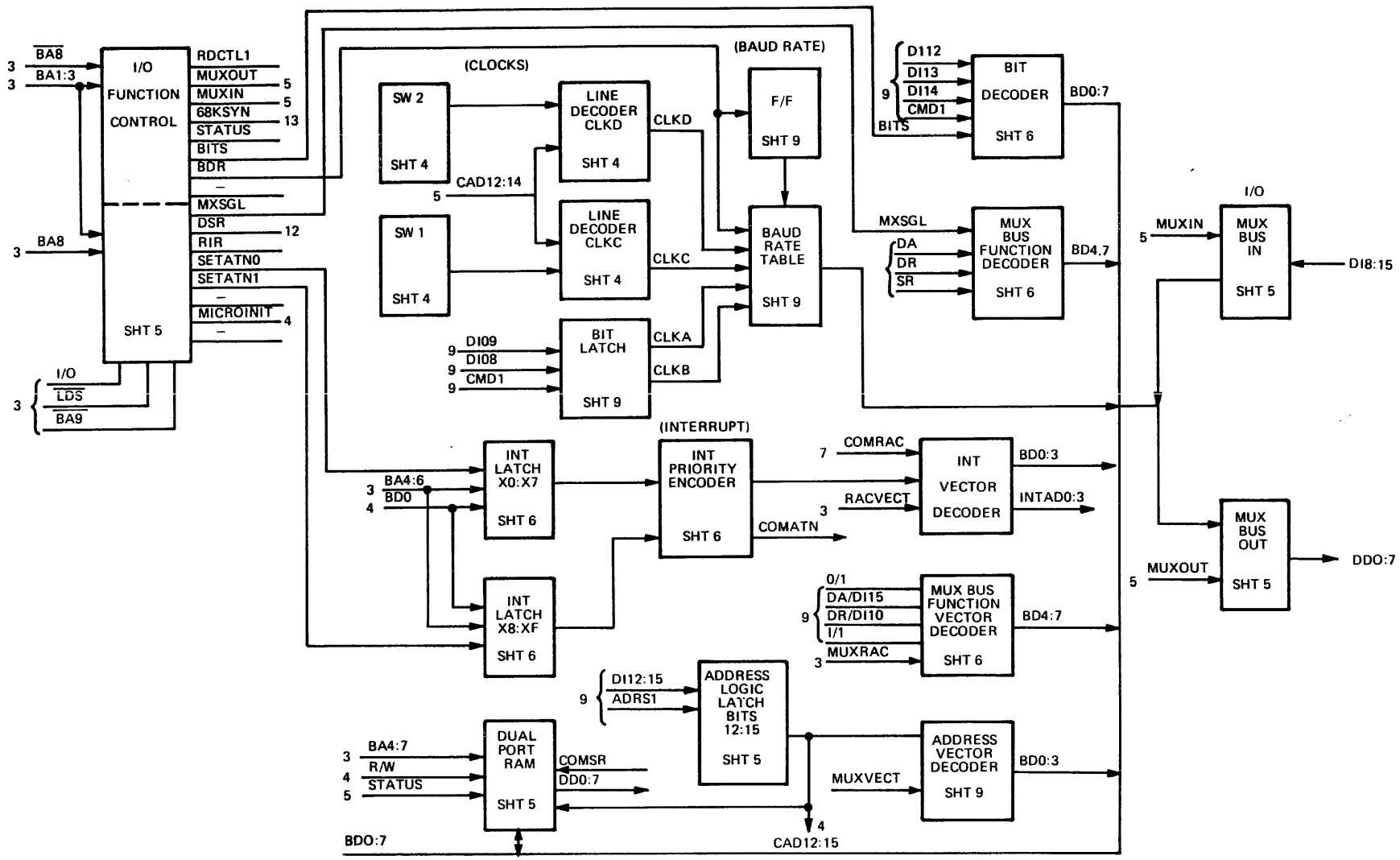


Figure 4-7 Microprocessor Controlled Logic

- Interrupt acknowledge from the processor

  The clock for IC A72 (COMRAC1) is activated when the processor responds with RACK0 to an interrupt. This latches the current state of IAD0:3 output from FPLA A91 and freezes that state into IC A72 (6G6). IC A72 has two roles. One is to generate the INTAD0:3 signals, which provide the least significant device address nibble back to the processor; the other is to complete the vector address by providing bits BD0:3, along with the decoded function RACKO for bits BD4:7 to the microprocessor. The resulting byte forms a direct vector to the correct microcode routine associated with this interrupt acknowledge. The contents of FPLA A91 are shown in Table 4-9. State 1 has the highest priority and state 16 has the lowest priority.

TABLE 4-9 INTERRUPT PRIORITY DECODER

PIN NUMBER	SIGNAL	1 STATE 16	
01	FE	----------	
02	L3T.INT	-------HLLLLLLLL	INPUT
03	L3R.INT	------HLLLLLLLLL	
04	L2T.INT	-----HLLLLLLLLLL	
05	L2R.INT	----HLLLLLLLLLLL	
06	L1T.INT	---HLLLLLLLLLLL	
07	L1R.INT	--HLLLLLLLLLLLL	
08	L0T.INT	-HLLLLLLLLLLLLL	
09	L0R.INT	HLLLLLLLLLLLLLL	
10	NC	.....	
11	NC	.....	
12	NC	.....	
13	COMATIN0	LLLLLLLLLLLLLLLL	OUTPUT
14	GND	LLLLLLLLLLLLLLLL	
15	IDA3	LLLLLLLLHHHHHHHH	
16	IDA2	LLLLHHHHLLLLHHHH	
17	IDA1	LLHHLLHHLLHHLLHH	
18	IDA0	LHLHLHLHLHLHLHLH	
19	CE	LLLLLLLLLLLLLLLL	
20	L7T.INT	---------------H	INPUT
21	L7R.INT	--------------HL	
22	L6T.INT	-------------HLL	
23	L6R.INT	------------HLLL	
24	L5T.INT	-----------HLLLL	
25	L5R.INT	----------HLLLLL	
26	L4T.INT	---------HLLLLLL	
27	L4R.INT	--------HLLLLLLL	
28	P5	HHHHHHHHHHHHHHHH	

H or L = active state
- = don't care
. = don't care

- Baud rate crystal

  The 4.9MHz crystal A175 (12A7) generates the basic frequency for the signal PCLK that is input to pin 20 of the serial communications controllers (Sheet 8). This is used both as the clock for the serial communications controllers and for the baud rate frequency, which is divided by the baud rate constant. The serial communications controller baud rate generators are programmed from the microprocessor using the frequency supplied on pin 20 and the constants read from A24 (9B3).

- Baud rate

  The group baud rate is recognized by the switching of two 8-to-1 line MUXs that output CLKC (4K5) and CLKD (4N6). These MUXs are operated by switches SW1 (4G6) and SW2 (4L6), which provide recognition of one of the four different group baud rate codes (0, 1, 2, and 3). See Table 4-10.

TABLE 4-10 GROUP BAUD RATE SELECTION

GROUP	SW2 CLKD	SW1 CLKC	DATA 8 CLKB	DATA 9 CLKA	RATE *
0	ON	ON	0	0	50
	ON	ON	0	1	110
	ON	ON	1	0	300
	ON	ON	1	1	1,200
1	ON	OFF	0	0	75
	ON	OFF	0	1	134.5
	ON	OFF	1	0	2,000
	ON	OFF	1	1	3,600
2	OFF	ON	0	0	150
	OFF	ON	0	1	600
	OFF	ON	1	0	4,800
	OFF	ON	1	1	9,600
3	OFF	OFF	0	0	1,800
	OFF	OFF	0	1	2,400
	OFF	OFF	1	0	7,200
	OFF	OFF	1	1	19,200

* Regrouping of baud rates can be accomplished by replacing A24 (9B3).
ON=0
OFF=1

There are four different baud rates within each group. The baud rates are selected from the two MSBs of the output command byte (DI8:9). These bits (DI8:9) become CLKA and CLKB (9A3). The four clock signals (CLKA:D) are input to A1:4 (9A3) of PROM A24. The PROM contains two halfword constants, which are read and sent to the serial communication controllers registers 12 and 13.

When the microprocessor is requested by a Command 2 instruction, the microcode activates two BDRO pulses. The first BDRO pulse enables the first halfword constant from PROM A24 to register 12 of the serial communications controller. This BDRO pulse is also sent to a D-type flip-flop A133 which controls the A0 input to the PROM A24. Input A0 is the steering input for the PROM A24 and directs access to the second halfword constant. When the second BDRO pulse is sent to the PROM, the next halfword constant is read and sent to register 13 of the serial communications controller. These constants are only used for asynchronous communication.

CHAPTER 5
PRECISION INTERVAL CLOCK (PIC) AND LINE FREQUENCY CLOCK (LFC)

5.1 INTRODUCTION

The MPC contains two independent clock devices. Both clocks provide timer-controlled processor interrupts but have different timing mechanisms (see Figure 5-1).

- Precision interval clock (PIC)

  The PIC produces or queues a processor interrupt. A specified time interval determines the point at which the interrupt occurs. The duration of the interval, as selected by the user, is measured in increments of time called the resolution rates. Four resolution rates are derived from a master time base, which is supplied by an 8MHz internal crystal oscillator. The four rates are: 1ms, 100μs, 10μs or 1μs. The number of times a specified resolution rate is to occur in an interval is called the interval count. The interval count is specified by the user and is variable through program control. The count constant can be a maximum of 12 bits long (X'FFF'); thus, the largest constant is a 4,095ms interval that can be timed by the PIC. The user can select an increment of time (resolution rate) and a count (interval count) where:

  resolution rate x interval count = interval

- Line frequency clock (LFC)

  The LFC generates or queues a processor interrupt. The point at which the interrupt occurs is determined by a fixed clock rate that is derived from the frequency of the AC power line. The user has no control over the LFC other than to enable, disable, or disarm interrupts. The power line frequency is either 60Hz or 50Hz, and the clock rate is always twice the line frequency. The durations of the intervals are shown in Table 5-1.

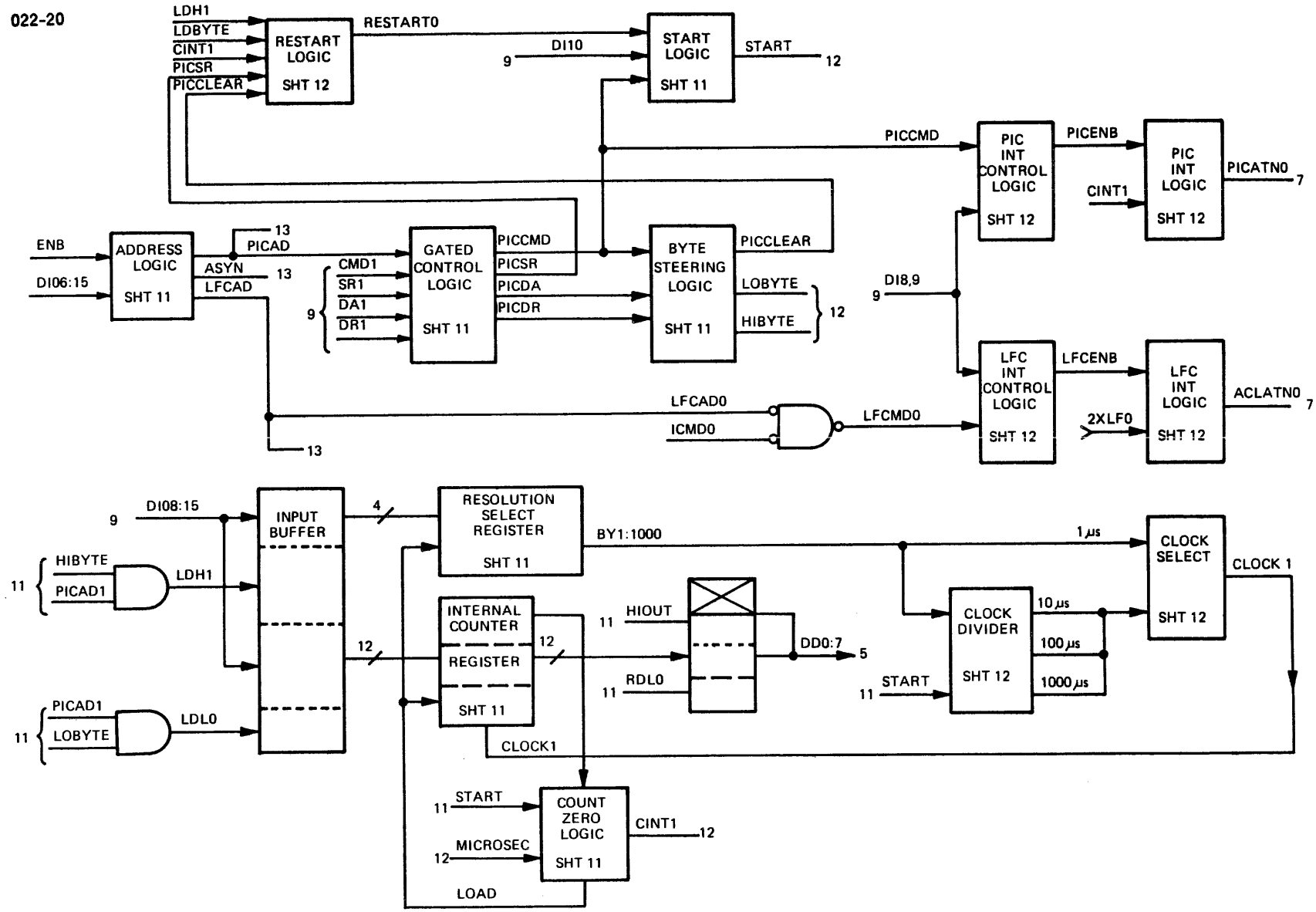


Figure 5-1 PIC/LFC Block Diagram

TABLE 5-1 INTERVAL DURATION IN RELATION TO LINE FREQUENCY

POWER LINE FREQUENCY	DURATION OF INTERVAL
60Hz	8.33ms
50Hz	10.00ms

5.2 CLOCK ADDRESSES

Both the PIC and LFC have a specific 10-bit address range with only the two most significant bits (MSBs) selectable. The address range for the PIC is X'06C' to '36C', and for the LFC, the address range is X'06D' to '36D'. The address for the LFC is always the address of the PIC plus one. See Table 5-2.

TABLE 5-2 PIC/LFC ADDRESSES

PIC		LFC	
BINARY	HEX	BINARY	HEX
00-11	0:3	00-11	0:3
0110	6	0110	6
1100	C	1101	D

5.3 PIC AND LFC ANALYSIS

IC A49 (11E2) contains two D-type flip-flops that determine if the PIC or the LFC were addressed. Logic at 11A2 allows addressing for one of four PIC/LFC addresses. This logic, plus the common I/O bus buffering, gates the control lines to their respective logic. Initialization ensures that the PIC and LFC are placed in the disarm mode. The resolution and counter input buffers, start, and byte steering logic are also reset.

The resolution and interval data is initially loaded into the PIC's input buffers A34 (11D7) and A41 (11D4) by a write halfword instruction. LDHI is used on the first DA and LDLO on the second. The LDHI and LDLO control signals are derived from the byte steering logic (11M2). This logic is initially set to load or read the HIBYTE first, then the trailing edge of DA or DR toggles IC A167 and primes the logic to load or read the second byte of data with LOBYTE. When the second DA or DR is removed, the logic is reset. A START command is required to load the values into the interval counter (A22, A33, and A40) and resolution select register (A48). The START command (PICCMD + DI10) (11J1) momentarily sets the START flip-flop (A167) (11L1) and the next MICROSEC pulse resets A167. This action resets the CINT1 flip-flop (A177) (11H6) and loads the resolution select register and interval counter from the input buffers. If the PIC is enabled, CINT1 generates an interrupt (PICATN0) (12J1) to the processor.

The clock divider logic receives its basic clock frequency MICROSEC from an 8MHz crystal (A197) via A165 (12D6) that feeds 4-bit counters A151, A142, and A132. The signals produced from the divider are: TUS0 (10 s from A151 pin 15), HUS1 (100μs from A19 pin 15), and MS1 (1ms from A132 pin 15). Together with the resolution select register outputs BY1, BY10, BY100, and BY1000 (A48) (11H4), they enable the clock divider outputs to produce CLOCK1 (A161) (12N5). CLOCK1 starts to decrement the interval counter. When the counter reaches zero, the next count pulse activates the borrow output from A40 (11G6) and the CINT1 flip-flop momentarily sets. It is reset by the next MICROSEC pulse. This causes an interrupt to be queued in the PIC attention flip-flop (A177) (12G2), if not in the disarm mode. PICATN0 goes active if enabled. The CINT1 (A177) (11J6) pulse also reloads the resolution select register and interval count register from the input buffer. The operation then recycles.

During the interval (counter not at zero), the input buffers may be altered. When the current interval concludes, the new data is loaded replacing the old data. However, if the interval times out between the start of the first DA and second DA, the restart flip-flop (A169) (12K2) stops the clock by holding A167 set and also prevents the interrupt from becoming queued. The clock restarts after the completion of the second DA or on receipt of a START command.

The PIC is provided with an output buffer (A39 and A32) (Sheet 11) so that the interval count can be interrogated without disturbing its operation. When the processor wants to read the counter value, it performs a read halfword instruction. The first DR reads the most significant byte (A32) and the second reads the least significant byte (A39), transferring the value onto the DD0:7 bus.

The LFC receives two times the AC line frequency (2XLF0) signal from the backpanel (102-0). If the LFC is activated, this signal sets the LFC interrupt flip-flop A188 (12K4) and generates an interrupt (ACLATN0) to the processor.

ICs A135, A168, and A145 (Sheet 12) determine whether the interrupts were enabled, disabled, or disarmed for both the PIC and LFC. The interrupt logic is arranged so that the PIC has the highest interrupt priority of the two.

CHAPTER 6
LINE PRINTER INTERFACE

6.1 INTRODUCTION

The line printer interface is compatible to the Centronics I/O parallel printer series and supports both lower- and upper-case characters. If the system is configured with more than one MPC board, only the line printer interface on the lowest priority MPC is enabled.

6.2 LINE PRINTER INTERFACE ANALYSIS

The line printer logic on Sheet 10 provides the necessary logic for interfacing the MUX bus to a line printer. The interface communicates with the printer over eight data lines, one strobe line, one acknowledgement line, one busy line, and three status lines (paper empty, fault, and selected). The printer accepts the standard 7-bit ASCII code with the capability of converting lower-case characters to upper-case if required (see Figure 6-1).

The line printer address switch (SW7) is located at 10A3. When the address switch matches DI08:15 from the MUX bus and the line printer interface is activated, the output of A14 (PREQL0) (10D2) becomes active. The signal PREQL0, along with ADRS1, sets the flip-flop A38 (10D5). A38 outputs PRAD1, which indicates that the line printer was addressed and gates the MUX bus control signals to the printer logic.

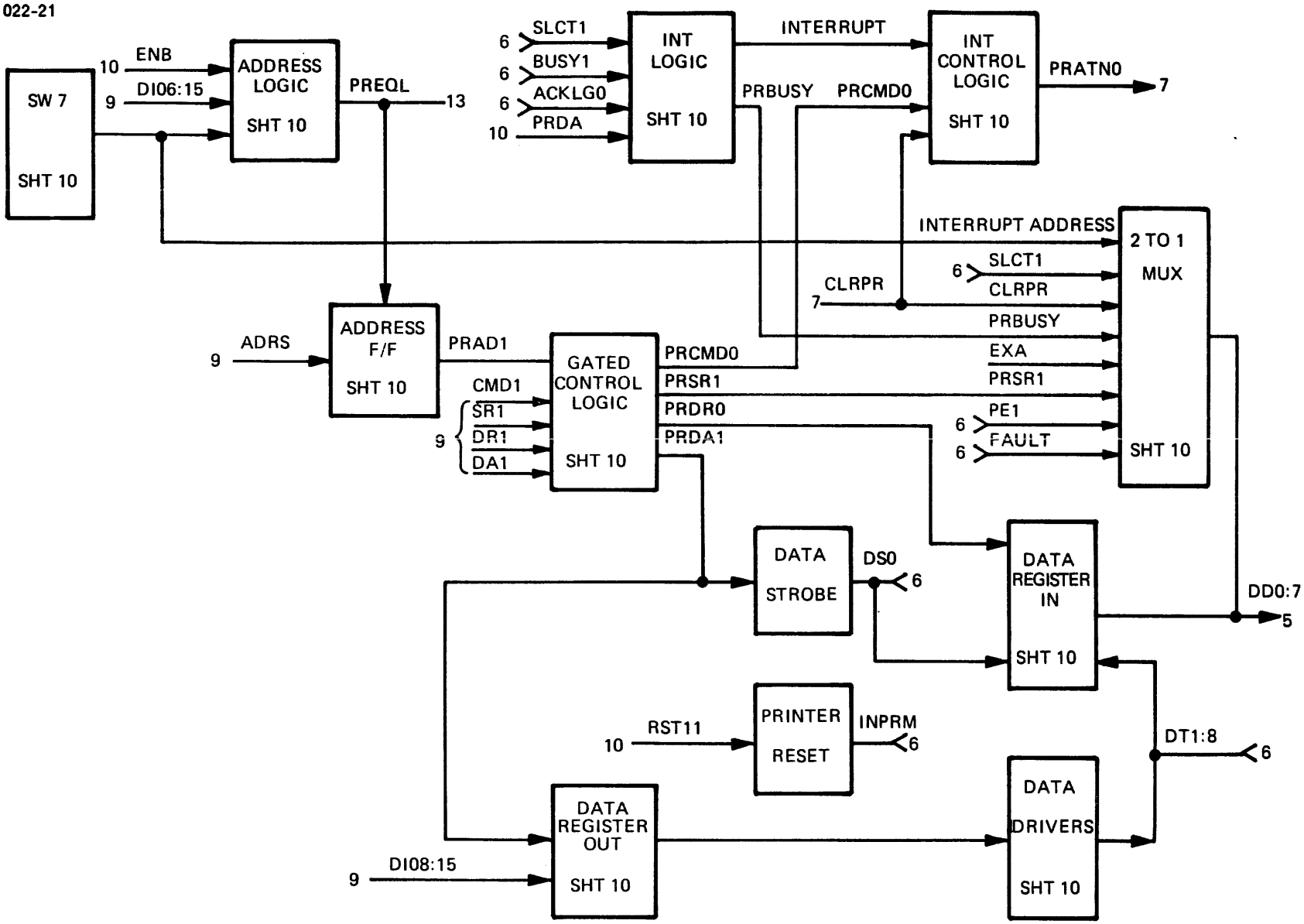


Figure 6-1 Line Printer Block Diagram

PRDA1 latches a byte of data from the MUX bus into the output data buffers A18 and A09 (10B6 and 10B8). Two microseconds later, it activates the data strobe (DS0) (10K8) to the printer indicating data is valid on DT1:8. The data presented to the printer at connector 6 (CONN6) is positive logic. Data is also latched from the output buffer by DS0 into the input data buffer. This allows the data presented to the printer on CONN6 to be verified by a data request instruction to the printer. The data is read from A29 (10L8) and presented to the DD0:7 bus by PRDR0.

When the processor requests the current status from the printer, the signal PRSR1 (10H4) goes high and selects the B side of A05 and A13 (10L3 and 10L4), which presents the following status: paper empty, fault, busy, examine, or selected onto DD0:7.

Interrupts can be queued, if not disarmed, by busy going inactive, by selecting or deselecting the printer, and, it the line printer interface is activated, interrupt the processor. When the processor acknowledges the interrupt by sending RACK0, the interrupt decoder (Sheet 7) on the MPC activates CLRPR0. This signal clears the pending interrupt and selects the A side of A05 and A13, which is the switch setting of SW7 (10A3) and returns the address of the line printer. ICs A05 and A13 are enabled either by doing a sense status or when CLRPR0 becomes available in response to RACK0.

Initialization (RST1) ensures that the address, busy, and interrupt flip-flops are reset. RST1 (10E4) also goes to the printer as a clear pulse to reset the printer.

CHAPTER 7
HARDWARE COMMUNICATION ASSIST

7.1 INTRODUCTION

The communication assist upgrades the auto driver channel of the processor and adds three instructions to the instruction repertoire. The auto driver channel time for CRC-BISYNC is reduced, and error checking capability is increased to include CRC-SDLC format. Three additional processor instructions are used: process byte (PB), process byte register (PBR), and move and process byte string register (MPBSR). These provide the capability to perform error checking of characters one byte at a time or as a string of data bytes. An error check can be calculated in any one of three formats: CRC-SDLC, CRC-BISYNC (also called CRC-16), or LRC. The MPBSR instruction allows buffer translation and movement in addition to the error check capability (see Figure 7-1).

7.2 HARDWARE COMMUNICATION ASSIST ANALYSIS

The steering logic (14L3) directs the type of data being sent to the board and enables the appropriate registers for loading. Three types of data can be sent to the board: format data, residual check character data, or the current data character to be included in the residual check character.

The box active logic (13F4) is part of the steering control logic that allows the board to produce an error check character. BCNT0 (14L7) causes BOXDT (14J7) to generate an internal clock (14J1) in the steering control logic. This clock toggles a counter (A88) (14K2) that steers (14M5) a delayed clock (A76) to the appropriate designation register. There are three valid states: format register (A98) (14K4) to be loaded, RCCR (A179, A180) (14C3), and (A199, A203) (13M3) to be loaded from the MUX bus, and the CCR (A204) (13D8) to be loaded with the RCCR updated. Data is gated from the RCCR back to the processor by RACK0. The counter remains in the last state until the MSBENB0 signal becomes active. At this time the counter is cleared and the board returns to the initialized state.

The format select register (A98) is set up by the format data from the processor. One of three formats can be selected: LRC, CRC-BISYNC, or CRC-SDLC.

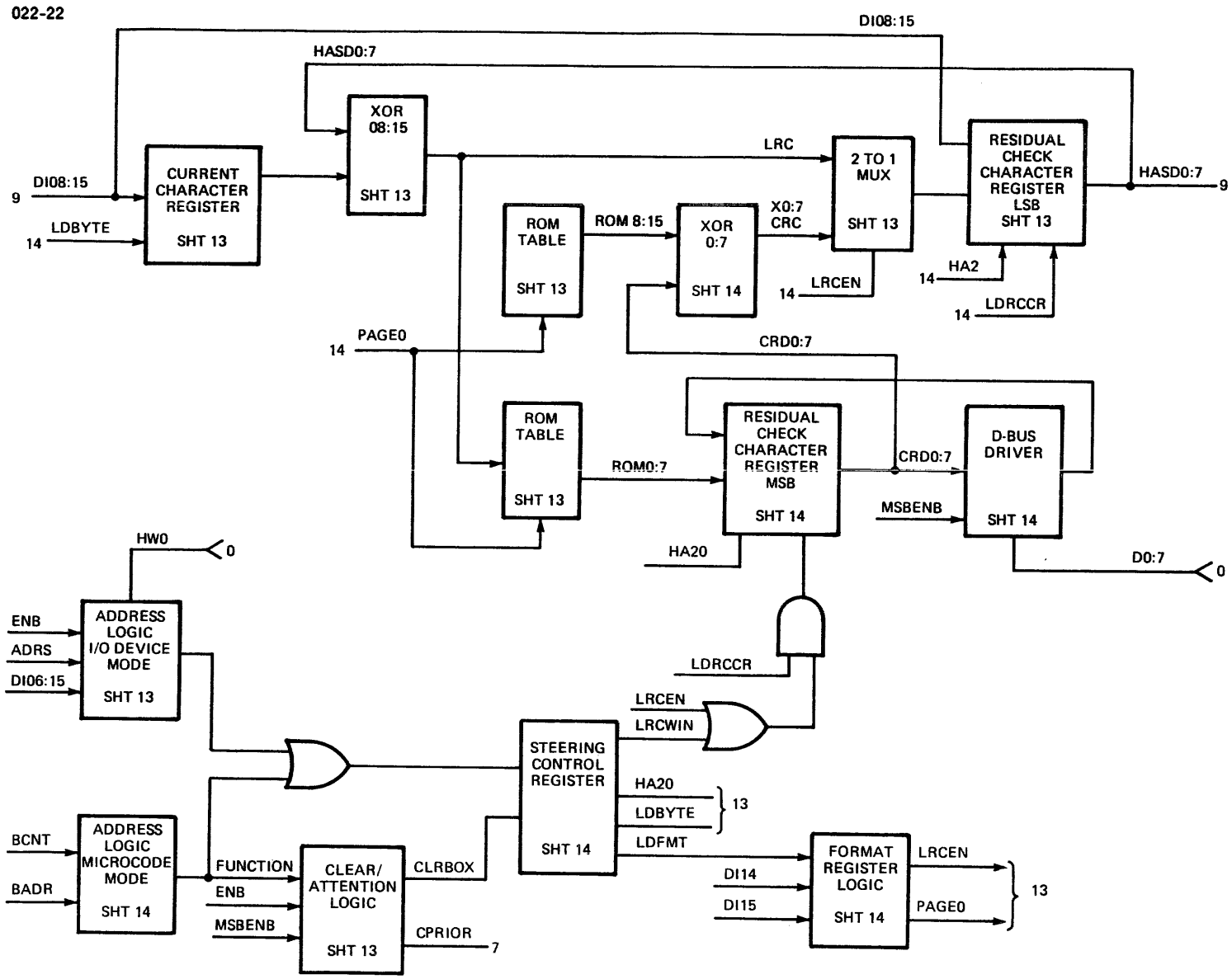


Figure 7-1 Hardware Communication Assist Block Diagram

The current data character register (A204), loaded from the least significant bits (LSBs) of the MUX bus by the steering control logic, contains the current data character which is exclusive ORed (A200, A202) (13H7) with the LSBs of the RCCR. The resultant data is used as the new residual check character in the LRC mode of error checking or as the resultant data applied as an address to the CRC table ROMs (A178, A191) (13L6).

ROM Tables 1 and 2 contain base numbers used to calculate the residual check character. Table 1 is used to calculate CRC-BISYNC and Table 2 is used to calculate CRC-SDLC. Selection of a specific character within the tables is accomplished by the address data from the exclusive ORed gates A200 and A202. This address information selects one 16-bit character out of a possible 256 in a given table. Table selection is accomplished by the signal PAGE0 from the format register initially loaded from the MUX bus.

The check character buffers A179, A180, A199, and A203 contain the residual check character and are updated with a new check character each time the current data character register is loaded. A199 and A203 control the LSBs and can be loaded with three different data formats: data from the MUX bus, from Table 1 or 2, or from the RCCR. A179 and A180 control the most significant bits (MSBs) and can be loaded with two data formats. The major difference is that the latter is loaded with contents of itself (CRC mode) or from table data (CRC mode), while the former is loaded with the exclusive ORed data of the most significant eight bits of the RCCR (CRC mode) or the least significant eight bits of the table data (CRC mode).

After the calculation the resultant data from the LSBs is gated onto the HASD0:7 lines and multiplexed (Sheet 9) to the MUX bus. The rest of the resultant data from the MSBs is gated directly through onto the MUX bus.

The following are examples of character error checking calculation for the LRC, CRC-BISYNC, and CRC-SDLC formats.

LRC:

1. The FMTR (A98) is loaded with X'02', placing the board in the LRC mode.

2. The RCCR (A179, A180, A199, and A203) is loaded with an initial residual of X'0000'. The initial residual can be any number.

3. The CCR (A204) is loaded with X'01' and is exclusive ORed (A200, A202) with the least significant eight bits of the RCCR.

4. The resultant data (Step 3) is loaded into the least significant eight bits of the RCCR, leaving the most significant bits unchanged. The RCCR contains the value of X'0001'.

5. The CCR is loaded next with an X'03' and exclusive ORed with the current contents of the RCCR. The resultant data is loaded into the RCCR. The RCCR contains the value X'0002'.

CRC-BISYNC:

1. The FMTR (A98) is loaded with X'00' placing the board into the CRC-BISYNC mode.

2. The RCCR (A179, A180, A199, and A203) is loaded with an initial residual value of X'0000' but can be any number.

3. The CRC (A204) is loaded with X'01' and exclusive ORed (A200, A202) with the least significant eight bits of the RCCR.

4. The resulting data (Step 3) is applied to the address inputs of the ROM table (A178, A191) indicated by PAGE0 being high. The table output is X'C0C1'.

5. The most significant eight bits of the ROM table output (A191) are loaded into the most significant eight bits of the RCCR (A179, A180), and the least significant eight bits of the ROM table output (A178) is exclusive ORed (A170, A192) with the initial most significant eight bits of the RCCR.

6. The resulting data (Step 5) is loaded into the least significant eight bits of the RCCR (A199, A203). The RCCR contains the value X'C0C1'.

7. The CCR is next loaded with X'02' and exclusive ORed with the least significant eight bits of the RCCR. The output of the ROM table is now X'5140'.

8. The least significant eight bits of the ROM table is exclusive ORed with the most significant eight bits of the RCCR. The RCCR still contains the X'C0C1' residual. The most significant eight bits of the ROM table are loaded into the most significant eight bits of the RCCR, and the least significant eight bits of the RCCR are loaded with the exclusive ORed result.

CRC-SDLC:

The calculations for CRC-SDLC are identical to CRC-BISYNC, with the execption that the FMTR is loaded with an X'01', and the ROM table is selected with PAGE0 being low.

APPENDIX A
MNEMONICS

The following list provides a description of each mnemonic found in the MPC. The source of each signal on Functional Schematic 35-910 D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
A1:15	Microprocessor address bus lines 1:15	Sheet 3
ARTS(CA): HRTS(CA)	Request to send signal from the data communications channel (A:H) to the user devices	Sheets 15,16
ACKLG0	Acknowledge from the line printer	10G5
ACLATN0	AC LFC attention signal	12M4
ACTS(CB): HCTS(CB)	Clear to send signal from the user devices to the data communications channels (A:H)	Sheets 15,16
AD0:7	Address data bus lines 0:7 between the microprocessor and the serial communications controllers	8R7
ADCD(CF): HDCD(CF)	Data carrier detect signal from the user devices to the data communications channels (A:H)	Sheets 15,16
ADRS0	Address control signal from the MUX bus	9A8
ADSR(CC): HDSR(CC)	Data set ready from the user devices to the data communications channels (A:H)	Sheets 15,16
ADSYN0	Address control signal SYNC return	13B1
ADTR(CD): HDTR(CD)	Data terminal ready signal from the data communications channels (A:H) to to the user devices	Sheets 15,16
ARING(CE): HRING(CE)	Ring signal from the user devices to the data communications channels (A:H)	Sheets 15,16

MNEMONIC	MEANING	SCHEMATIC LOCATION
ARXD(BB): HRXD(BB)	Receive data from the user devices to the data communications channels (A:H)	Sheets 15,16
ARTXC: HRTXC	Receive clocks from the user devices to the data communications channels (A:H) for synchronous mode	Sheets 15,16
AS0:1	Address strobe indicating a valid address on the microprocessor address bus	3H8,3M9
ATN0	Attention signal to the processor via the MUX bus	7H2
ATRXC: HTRXC	Transmit clocks from the user devices to the data communications channels (A:H) for synchronous mode	Sheets 15,16
ATSYN1	Attention SYNC pulse for acknowledge (ACK) address	7J4
ATXDATA(CA):	Transmit data from the data communications devices	Sheets 15,16
AUTOVEC0	Microprocessor vector acknowledge for LSU	3J8
BA1:15	Buffered microprocessor address bus	Sheet 3
BADR0	Hardware assist address line	14L8
BAS1	Buffered microprocessor address strobe	3L9
BCNT0	Hardware assist control line	14L7
BD0:15	Buffered microprocessor data bits	Sheets 4,5,6
BDR0	Select baud rate	5J3
BITS0	Read parity bits from command line input	5J3
BLDS	Buffered microprocessor lower data strobe	3E4
BOXDT0	Box active on the hardware assist	13G4
BOXDTD0	Box active delayed on the hardware assist	14K6

MNEMONIC	MEANING	SCHEMATIC LOCATION
BR/W	Buffered microprocessor read/write	3M7
BUDS	Buffered microprocessor upper data strobe	3E4
BUSY1	Busy from the line printer	10F4
BY1:1000	Resolution register output for the PIC	11H4
CAD12:15	Data communications device address bits	5N4
CINT1	Counter interrupt-pulsed on completion on interval counts	11K5
CLKC	Baud rate clock C selection	4K5
CLKD	Baud rate clock D selection	4R5
CLOCK1	Clock pulse of selected resolution rate	12M6
CLRACL0	Clear AC LFC interrupt	7M2
CLRBOX0	Clear box active in the hardware assist	13F6
CLRPIC0	Clear PIC interrupt	7M2
CLRPR0	Clear line printer interrupt	7M2
CMD0	Command signal from the MUX bus	9A8
CMDI1	Command interrupt	12A4
COM1:4	Data communications channel select lines	5J5
COMACK0	Data communications channel interrupt acknowledge	3H9
COMAD1	Data communications address	9M8
COMATN0	Interrupt from one of the data communications channels (A:H)	6E6
COMDR0	Common data request from MUX bus	9E6
COMEN0	Data communications channel mapping enable	5J6

MNEMONIC	MEANING	SCHEMATIC LOCATION
COMEQL1	Data communications device addressed	9M5
COMINT0	Communication interrupt from one of eight data communications channels (A:H)	8A4
COMRAC0	Clear data communications interrupt	7M2
COMSR0	Common status request from MUX bus	9E6
COMSW0:3	Data communications address bits	9M7
CPRIOR1	Hardware assist interrupt	13F5
CRD0:7	Hardware assist data lines	Sheet 14
D0:15	Microprocessor data lines 0:15	Sheets 3,4
D000:070	MUX bus data lines D000:070	14G4
D080:150	MUX bus data lines D080:150	9M3
DA0	Data available from the MUX bus	9A9
DCR0	Indicates the presence of hardware assist to the processor	6R7
DD0:7	Internal data lines	5G1,10N2 11M4
DELATS1	Delayed attention SYNC pulse for interrupt acknowledge	7M5
DI00:07	Data internal bits	14G3
DI08:15	Data internal lines	9M1
DSRM	Command disarm	12C5
DR0	Data request from MUX bus	9A8
DS0	Data strobe for line printer	10K8
DSR0	Read data set ready status	5M2
DSR0:7	Data set ready from the user devices communications channels (A:H)	Sheets 5,15,16
DT1:8	Data lines to the printer	Sheet 10
DTACK0	Data transfer acknowledge	3D5

MNEMONIC	MEANING	SCHEMATIC LOCATION
EXTCLR0	External board clear	3A1
FAULT0	Fault status line from the line printer	10H4
FB	Force baud rate	4L4
FUNC1	Hardware assist function selected	14R6
HALT	Halt microprocessor	3G2
HA2	Hardware assist clock 2	14M1
HASD0:7	Hardware assist data lines	13N4
HIBYTE	High byte selected (PIC)	11M3
HIOUT0	High byte output enable (PIC)	11L4
HSAD0	Hardware assist device address	13D4
HW	Halfword enable	13G2
IACK0:1	Interrupt acknowledge from microprocessor	3K7
IAD0:3	Data communications interrupt address decoded	6F6
ICMD	Internal command	11H1
IDA	Internal data available	11H2
IDR	Internal data request	11H3
INPRM	Line printer reset	10L6
INTA:C	Interrupt request decoded	7G1
INTAD0:3	Data communications interrupt address bits	6K6
IO0	I/O mapping enable	5J6
IPL0:2	Microprocessor interrupt level input	3G7
ITACK1	MUX bus interrupt acknowledge for the microprocessor	3K9
LDBYTE1	Load data byte for the hardware assist	14N4

MNEMONIC	MEANING	SCHEMATIC LOCATION
LDFMT1	Load translation format byte for the hardware assist	14K3
LDH1	Load high byte into the PIC	11C6
LDL0	Load low byte into the PIC	11C8
LDRCCR0	Load receive check character register, hardware assist	14N5
LDS	Microprocessor lower data strobe	3J5
LEDIN/OUT	Fault indicator, data communications lines (0:7)	12L7
LFCAD0	LFC address clock address	12A4
LFCDSRM0	LCF disarm	12D4
LFCENB	LFC enable	12D3
LOBYTE	Low byte selected (PIC)	11M2
LRCEN0	LRC mode enable, hardware assist	14N6
LRCWIN	LRC window, assist	14L1
LSU0	LSU disable from consolette	14M8
LSUAD0	LSU address	6K7
LSUDR1	LSU data request	6M9
LSUINT0	LSU interrupt to the microprocessor	6M8
L0TXD:L7TXD	Transmit data, data communications lines (0:7)	Sheet 8
L0CTS:L7CTS	Clear to send, data communications lines (0:7)	Sheets 8,15,16
L0DCD:L7DCD	Carrier detect, data communications lines (0:7)	Sheets 8,15,16
L0DTR:L7DTR	Data terminal ready, communications lines (0:7)	Sheet 8
L0R1:L7R1	Ring, data communications lines (0:7)	Sheets 5,15,16

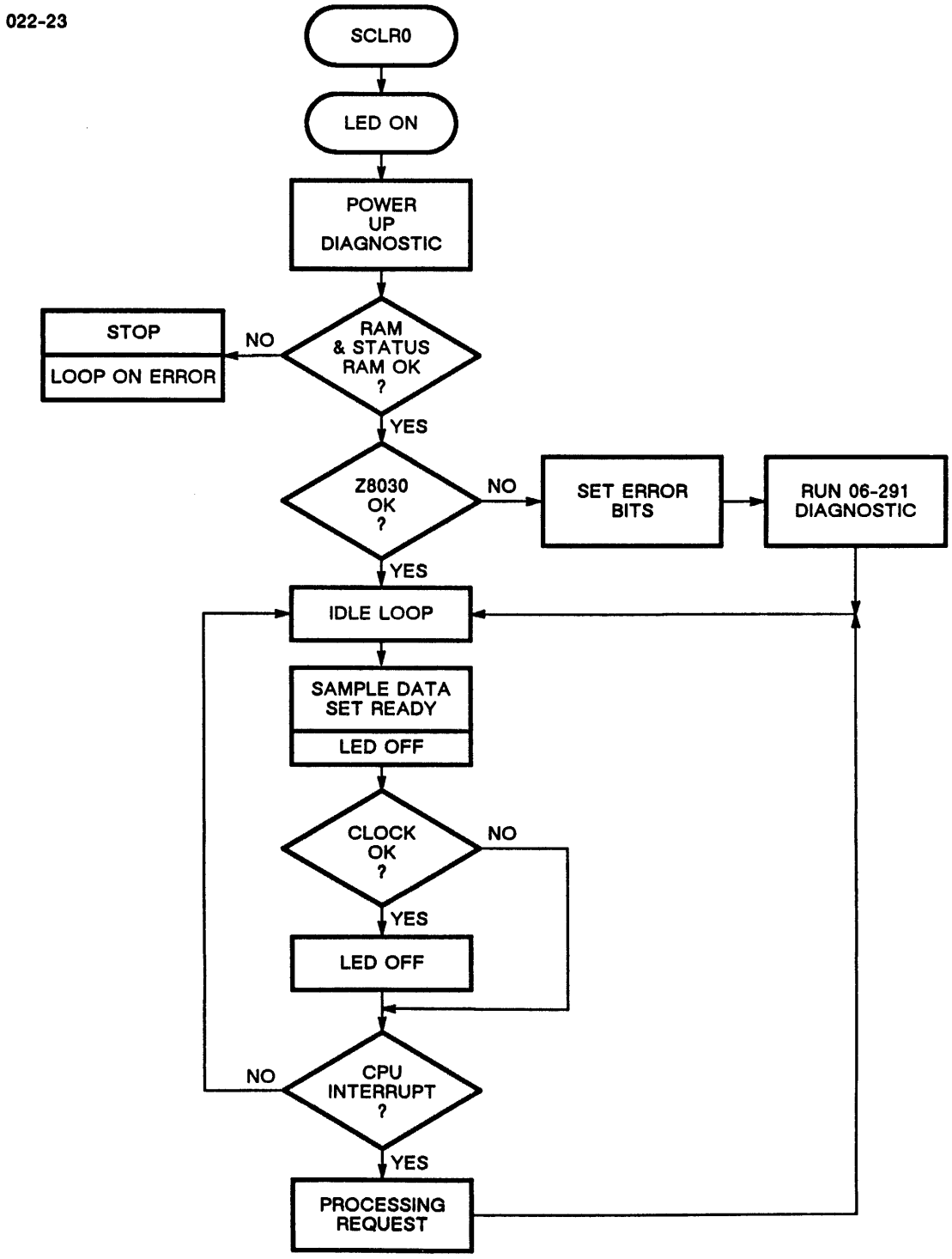
MNEMONIC	MEANING	SCHEMATIC LOCATION
L0RTS:L7RTS	Request to send, data communications lines (0:7)	Sheet 8
L0RTXC:L7RTXC	Receive clock, sync mode, data communications lines (0:7)	Sheets 8,15,16
L0RXD0:L7RXD0	Receive data, data communications lines (0:7)	Sheets 8,15,16
L0TRXC:L7TRXC	Transmit clock, sync mode, communications lines (0:7)	Sheets 8,15,16
MCLK	M clock	3E3
MICROINIT0	Microprocessor initialization, invokes power-fail detection on the backpanel	5M3
MICROSEC	Microsecond pulse	12E6
MPSYNC1	Common MUX sync decoded except for microprocessor functions	13C3
MSBENB0	Most significant bit enable, hardware assist	13C2
MUXEN0	MUX bus enable	13C2
MUXINT0	MUX bus interrupt	13C2
MUXIN/OUT0	MUX input/output	5J2
MUXRAC0	Microprocessor acknowledge to a MUXINT	3K9
MUXVECT0	Microprocessor vector enable to read MUX bus request	3H9
MXSGL0	Microprocessor MUX bus request signal enable	5M2
PE	Line printer paper empty	10J3
PFDT0	Power fail detect	6N7
PICAD0	PIC address	11F2
PCLK	P clock	12C7
PICATN0	PIC attention	12H1

MNEMONIC	MEANING	SCHEMATIC LOCATION
PICCMD1	PIC command	11J1
PICDA	PIC data available	11J2
PICDR	PIC data request	11J3
PICDSRM0	PIC data disarm	12D3
PICENB1	PIC enable	12D1
PICSR1	PIC status	11J2
PRAD1	Line printer address	10E5
PRATN0	Line printer attention	12H1
PRCMD0	Line printer command	10G6
PRDR0	Line printer data request	10L9
PRDSRM0	Line printer disarm	10J7
PREQL0	Line printer addressed	10F3
PRSR1	Line printer status request	10H4
PRSW0:7	Line printer address switch setting	Sheet 10
RACK0	Receive acknowledge	9A9
RACVECT0	Microprocessor vector acknowledge for data communications channels	3H9
RAM0	RAM selected	5J5
RAMLDS0 RAMUDS0	RAM lower data strobe RAM upper data strobe	3M8
RAMLSEL0 RAMUSEL0	RAM lower select enable RAM upper select enable	3M1
RDCTL1	Read control 1	5J2
RESET	Reset	3G2
RESTART	Precision clock restart	12N2
RIR0	Read ring status lines	5M2
ROM0	EPROM selected	5K5
ROM0:15	ROM data lines 0:15 hardware assist	13N5

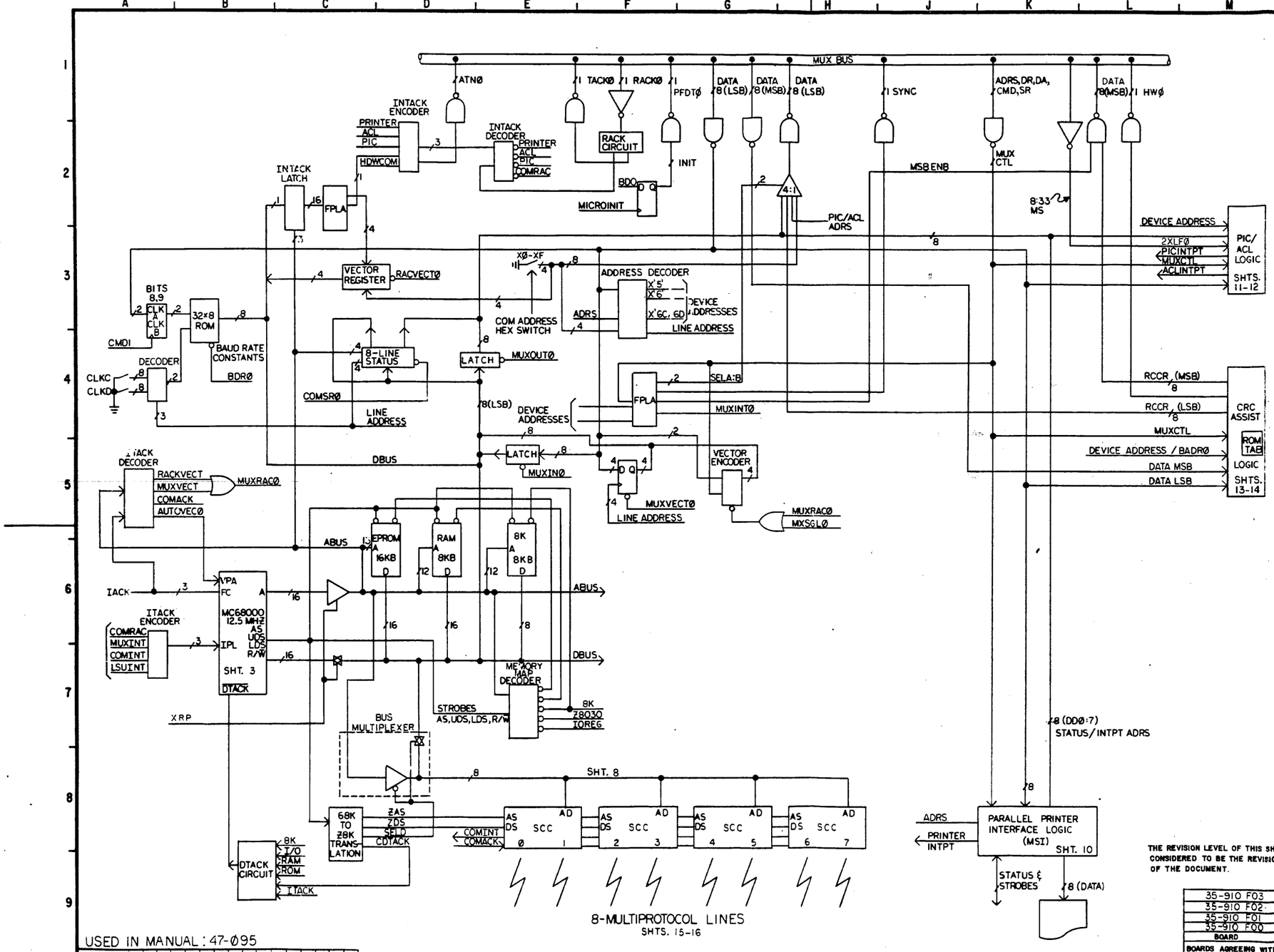
MNEMONIC	MEANING	SCHEMATIC LOCATION
ROMCK1	ROM DTACK delay for ROM and serial communications controller	3D5
RST10:20	Buffered reset	3E3
R/W	Read/write	3J4
SCLK	System clock	3E3
SCLR0	System clear	3B1
SELA/B	Select A or B, outputs 0D0:7 to MUX bus	13C2
SELD0:1	Multiplexes microprocessor bus to serial communications bus	7M9
SETATN00	Set attention for lines 0-3	5M2
SETATN1	Set attention for lines 4-7	5M2
SLCT1	Line printer selected	10E1
SR0	Status request	9A8
START0:1	Start precision clock	11M1
STATE 1,3,7	State sequence for data communications bus translator	Sheet 7
STATUS0	Dual-ported status RAM enable	5J2
SYN0	Synchronization signal to MUX bus	13G2
TACK0	Transmit acknowledge	7M4
TSTCLK1:5	Sync mode test clock	Sheets 12,15,16
UDS	Microprocessor upper data strobe	3J5
X0:7	Exclusive ORed bus 0:7 hardware assist	14G8
ZAS0	Address strobe for data communications channel bus	7M7
ZDS0	Data strobe for data communications channel bus	7M8
68KSYN0	Microprocessor sync	5J2

MNEMONIC	MEANING	SCHEMATIC LOCATION
8K0	8K enable	5J6
8KLSEL0	8K lower select enable	4L8
8KUSEL0	8K upper select enable	4L8
8KWS0	Write 8K	4L9

APPENDIX B
ERROR LED INDICATOR



INDEX



USED IN MANUAL: 47-095

REVISION	07	05	02	01	03	01	02	01	01	02	01	02				
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

NOTES 1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE IN OHMS, 5%, 1/4W

BRUNING 44-131-4057

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	

REVISED SHTS 1, 2, 5, 6, 8 & 12. AREA M9, 35-910 F00-F03 WAS R00.

DB		5841	M	1-28-85	R01

AREA M9, 35-910 WAS R01. AREA A9, REVISED SHT'S 1 & 11.

MF		5892	M	3-8-85	R02

AREA M9, BOARD REV LEVEL TABLE; 35-910 F00 WAS R01, F01 WAS R01, F02 WAS R02 & F03 WAS R01. REVISED SHTS. 1, 2, 7 & 10.

DB		6068	M	6-25-85	R03

AREA M9 BOARD REV LEVEL TABLE 35-910 F00 WAS R03, F01 WAS R05 F02 WAS R04, F03 WAS R05. SHEETS 3 & 9 WERE R00, SHEETS 5 & 12 WERE R01, SHEET 2 WAS R02, SHEET 1 WAS R03

REM		6260	MS	1-13-86	R04

AREA M9 BOARD REV LEVEL TABLE, 35-910 F00 WAS R04, F01 WAS R07, F02 WAS R05, F03 WAS R07. SHT 1 WAS R04, SHT 2 WAS R03, REVISED SHTS. 1 & 2.

PE		6378	MS	3-18-86	R05

RELEASED FOR PRODUCTION
ENG. BH DATE 1/13/86

REWORKED SHTS 7 & 10 REWORKED BD REV LEVEL CHART F00 WAS R04, F01 & F02 WAS R10, F03 WAS R07

BP		6736	MS	1-09-87	R06

REVISED SHTS 2, 3, 4 & 5. REWORKED BD REV LEVEL CHART F00 WAS R08, F01 WAS R14, F02 WAS R09, F03 WAS R14.

BH		7116	MS	1-27-88	R07

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
J. BIELSKIE	K. REED	DES/DFT	8-5-84
R. CERO		SUPV	9-9-86
E. GREENSTEIN		TEST	9-9-86
B. HEITMUELLER		ENG	9-9-86
W. RICE		MGR	9-9-86
R. BARKER		QC	9-9-86

Concurrent Computer Corporation
Oceanport, N.J. 07757

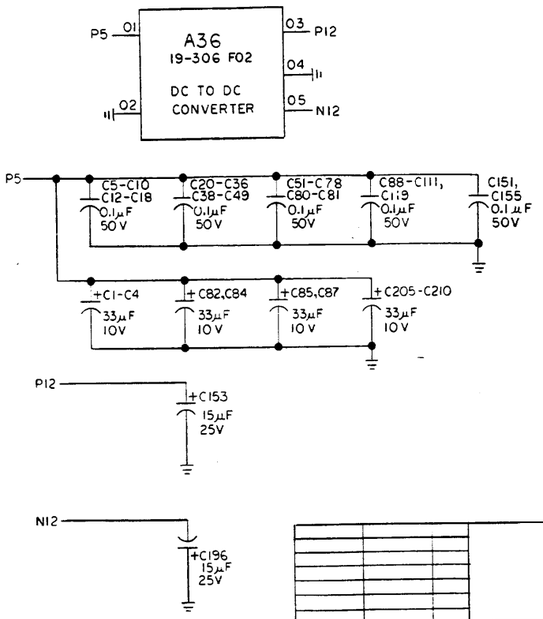
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

BOARD	REV LEVEL
35-910 F03	R15
35-910 F02	R10
35-910 F01	R15
35-910 F00	R09

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

TITLE
MULTIPERIPHERAL CONTROLLER
FUNCTIONAL BLOCK DIAGRAM

TASK 03199	SHT
DWG 35-910 R07 D08	1-16



CONN	TERM. NO.	CABLE CONNECTOR MAP ROW 2	ROW 1
7	04	WZ	WX
	03	TSTCLK1	WY
	02	TPA	
	01	TPB	
	00	GND	LSU DISABLE
6	16	INPRMO	GND
	15	FAULTO	GND
	14	SLCT	GND
	13	PEI	GND
	12	BUSY	GND
	11	ACKLGO	GND
	10	DT8I	GND
	09	DT7I	GND
	08	DT6I	GND
	07	DT5I	GND
	06	DT4I	GND
	05	DT3I	GND
	04	DT2I	GND
	03	DT1I	GND
	02	KEYED	GND
	01	DSO	GND
	00		GND
5	16		GND
	15	GRTxC	GTXDATA(BA)
	14		GRTS(CA)
	13	GTRxC	GDSR(CC)
	12	GDCD(CF)	GRXD(BB)
	11	GCTS(CB)	TSTCLK5
	10	GDTR(CD)	GRING(CE)
	09		GND
	08	GND	GND
	07	GND	
	06	GND	HRTxC
	05	HTXDATA(BA)	
	04	HRTS(CA)	HTRxC
	03	HDSR(CC)	HDCD(CF)
	02	HRXD(BB)	HCTS(CB)
	01	TSTCLK5	HDTR(CD)
	00	HRING(CE)	
4	16		GND
	15	ERTxC	ETXDATA(BA)
	14		ERTS(CA)
	13	ETRxC	EDSR(CC)
	12	EDCD(CF)	ERXD(BB)
	11	ECTS(CB)	TSTCLK4
	10	EDTR(CD)	ERING(CE)
	09		GND
	08	GND	GND
	07	GND	
	06	GND	FRTxC
	05	FTXDATA(BA)	
	04	FRTS(CA)	FTRxC
	03	FDSR(CC)	FDCD(CF)
	02	FRXD(BB)	FCTS(CB)
	01	TSTCLK4	FDTR(CD)
	00	FRING(CE)	
3	16		GND
	15	CRTxC	CTXDATA(BA)
	14		CRTS(CA)
	13	CTRxC	CDSR(CC)
	12	CDCD(CF)	CRXD(BB)
	11	CCTS(CB)	TSTCLK3
	10	CDTR(CD)	CRING(CE)
	09		GND
	08	GND	GND
	07	GND	
	06	GND	DRTxC
	05	DTXDATA(BA)	
	04	DRTS(CA)	DTRxC
	03	DDSR(CC)	DDCD(CF)
	02	DRXD(BB)	DCTS(CB)
	01	TSTCLK3	DDTR(CD)
	00	DRING(CE)	
2	16		GND
	15	ARTxC	ATXDATA(BA)
	14		ARTS(CA)
	13	ATRxC	ADSR(CC)
	12	ADCD(CF)	ARXD(BB)
	11	ACTS(CB)	TSTCLK2
	10	ADTR(CD)	ARING(CE)
	09	FB	GND
	08	GND	GND
	07	GND	
	06	GND	BRTxC
	05	BTXDATA(BA)	
	04	BRTS(CA)	BTRxC
	03	[illegible]	[illegible]
	02	BRXD(BB)	BCTS(CF)
	01	TSTCLK2	BDTR(CD)
	00	BRING(CE)	

BACK PANEL MAP ROW 1	ROW 2	TERM. NO.	CONN
P5	GND	41	
GND	GND	40	
		39	
		38	
		37	
		36	
		35	
		34	
		33	
		32	
		31	
		30	
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		08	
		07	
		06	
		05	
		04	
		03	
		02	
GND	GND	01	
P5	GND	00	
P5	GND	41	
GND	GND	40	
		39	
		38	
		37	
		36	
		35	
BCNTO	BADRO	34	
		33	
		32	
		31	
		30	
		29	
		28	
	DCRO	27	
SCLRO	HWO	26	
PRACKO		25	
DBCNTO/LSUØ	PFDTØ	24	
SYNO	AINO	23	
RACKO	TACKO	22	
	DAO	21	
DRQ	CMDO	20	
SRQ	ADRSO	19	
DI4O	DI5O	18	
DI2O	DI3O	17	
DIOO	DI1O	16	
DO8O	DO9O	15	
DO6O	DO7O	14	
DO4O	DO5O	13	
DO2O	DO3O	12	
DOOO	DO1O	11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
2XLFØ		01	
GND	GND	00	
P5	GND		

21-099 F02	RM6 (10K)	03,08,09,10
21-099 F02	RM5 (10K)	10
21-099 F02	RM3 (10K)	10
21-099 F02	RM1 (10K)	02,03,04,09,10
19-251	A163	04,08,10,12
19-251	A8	06,12
19-166	A20	07,09
19-165	A188	05,06
19-161	A129	06
19-159	A61	03
19-159	A3	06,08,11
19-154	A155	02,04,06,10
19-154	A123	08,12
19-154	A39	08
19-125	A110	08,11
19-063	A49A	05,06
19-059	A154	08
19-058	A148	08
19-057	A152	12
19-057	A130	12
19-046	A195	11
19-046	A158	11
19-046	A55	11

PART NO.	REF DESIGNATION	SPARE OUTPUT NO

FROM	TO	SHT	NOTES
E27-1	TSTCLKEN	7	TEST CLOCK EXT CLEAR
E27-2	GND	7	
E27-3	EXTCLRØ	3	
204-7	WX	4	REMOTE
103-7	WY	4	
204-7	WZ	4	
202-7	TPA	5	IDLE
203-7	TSTCLK1	12	TEST CLOCK
A606	TPB	5	68K AS
A6011	TPE	5	MC CHECK

TEST POINTS

TP	MNEM	SHT	NOTES
E20-1	GND	6	LSU DISABLE
E20-2	A17604	6	
E1-1	GND	6	MICROINIT
E1-2	PFDTØ	6	
E1-3	DCRØ	6	
E1-4	A13708	6	
E19-1	A14001	10	PRINTER DISABLE
E19-2	GND	10	
E18-1	DI6I	10	U/L CASE DISABLE
E18-2	AI08	10	
E21-1	LENB	11	UNLOCK DISABLE
E21-2	GND	11	
E21-3	A16104	11	DEV ADD SELECTION
E21-4	DI06A	11	
E21-5	U6	11	
E21-6	A16102	11	
E21-7	DI07A	11	
E21-8	U7	11	
E8-1	A18912	13	HDA COM ASSIST DISABLE
E8-2	GND	13	
E8-3	A14609	13	
E2-1	DBCNTØ	14	OPERATION SELECTION
E3-1	A14711	14	
E3-2	BCNTØ	14	
E4-1	A14701	14	
E4-2	BADRØ	14	

STRAPPING INFO

TP	MNEM	SHT	NOTES
E11-1	A9903	3	
E11-2	GND	3	
E11-3	A9905	3	
E11-4	A9906	3	
E25-1	GND	3	
E25-2	GND	3	
E25-3	GND	3	
E25-4	GND	3	
E13-1	A11101	3	
E13-2	GND	3	
E13-3	OSCIN	3	
E5-1	PRACKO	7	
E5-2	A14812	7	
E5-3	TACKO	7	
E6-1		12	
E6-2		12	
E6-3		12	
E7-1	PCLK	12	
E7-2	PCLKEN	12	
E7-3	GND	12	
E26-1	A19815	12	
E26-2	A19801	12	
E26-3	A19802	12	
E26-4	A19803	12	
E26-5	A19804	12	
E26-6	A19805	12	
E26-7	A19806	12	
E26-8	GND	12	

FACTORY USE

NOTES:

REVISIONS

EXTENSIVE CHANGES, SEE R00 MICROFILM.					
DB	JLZ	5841	M	1-28-85	R01
AREA B6, CAPS C153, C154, C196 & C197 WERE 33 μF 10V'. (AREA G8) DELETED FROM SPARE OUTPUT LIST, "19-057 · A2 · 10", "19-064 · A45 · 01, 09", "19-125 · A1 · 06" & "21-099 F02 · RM4 (10K) 10".					
DB	JLZ	6068	M	6-24-85	R02
AREA G7 & G8 DELETED FROM SPARE OUTPUT LIST: 19-064 A150-05606, 19-158 A176A-08610					
REM	JLZ	6260	MS	1-13-86	R03
AREA B5 REMOVED CAP C196 & C153 WAS C197, AREA B6 REMOVED CAP C153 & C196 WAS C154.					
PE	JLZ	6378	MS	3-18-86	R04
AREA G6, EXAMINED IC A23.5, A17, 11. AREA G7, REMOVED IC 19-154, A100, 06.					
BM	JLZ	7118	MS	1-27-88	R05

UNLESS OTHERWISE SPECIFIED

SCALE: ~

TOLERANCE:

DIMENSIONS ARE IN INCHES

.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

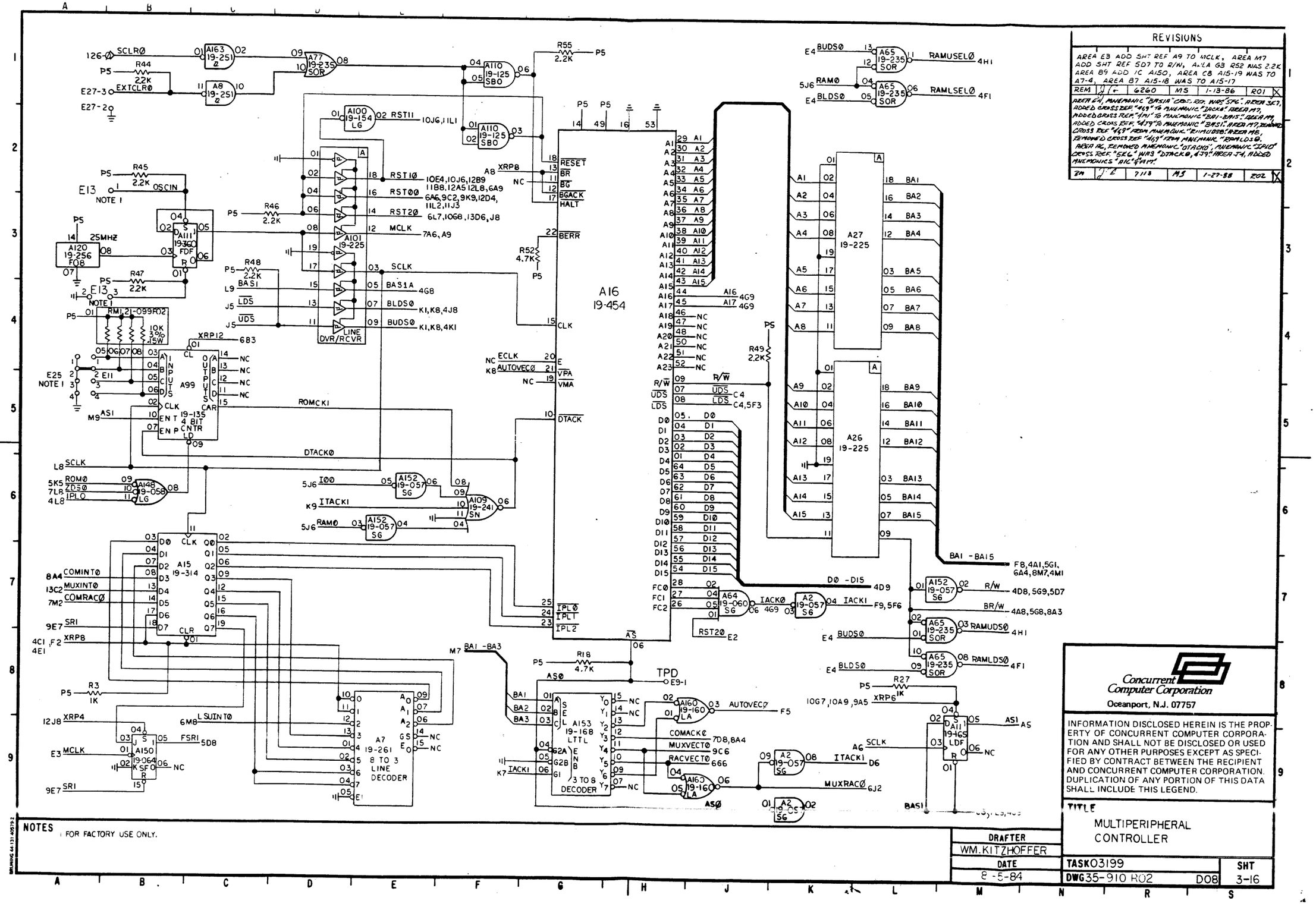
NAME	TITLE	DATE
J.BIELSKIE WM KITZ	DES/DFT	8-5-84
R.CERO	SUPV	
	CHK	
B.HEITMUELLER	ENG	
W.RICE	MGR	
R.BARKER	QC	

Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE SCHEMATIC
MULTIPERIPHERAL CONTROLLER

TASK 03199 SHT 2 - 16

DWG 35-910 R05 D08



REVISIONS

REM					
		6260	MS	1-13-86	201

AREA E4, MNEMONIC "BASIA" CROSS REF. WAS "STA". AREA 5K7, ADDED CROSS REF. "469" TO MNEMONIC "JACKA" AREA M7, ADDED CROSS REF. "4M1" TO MNEMONIC "BA1-BA15". AREA M7, ADDED CROSS REF. "439" TO MNEMONIC "BAS1". AREA M7, REMOVED CROSS REF. "469" FROM MNEMONIC "RAMUDSØ". AREA M6, REMOVED CROSS REF. "469" FROM MNEMONIC "RAMLDSØ". AREA J6, REMOVED MNEMONIC "DTACKØ", MNEMONIC "IPLØ" CROSS REF. "5K6" WAS "DTACKØ, 439". AREA J4, ADDED MNEMONICS "AIC" & "AM1".

2A		7118	MS	1-27-88	202

NOTES
1. FOR FACTORY USE ONLY.

Concurrent Computer Corporation
Oceanport, N.J. 07757

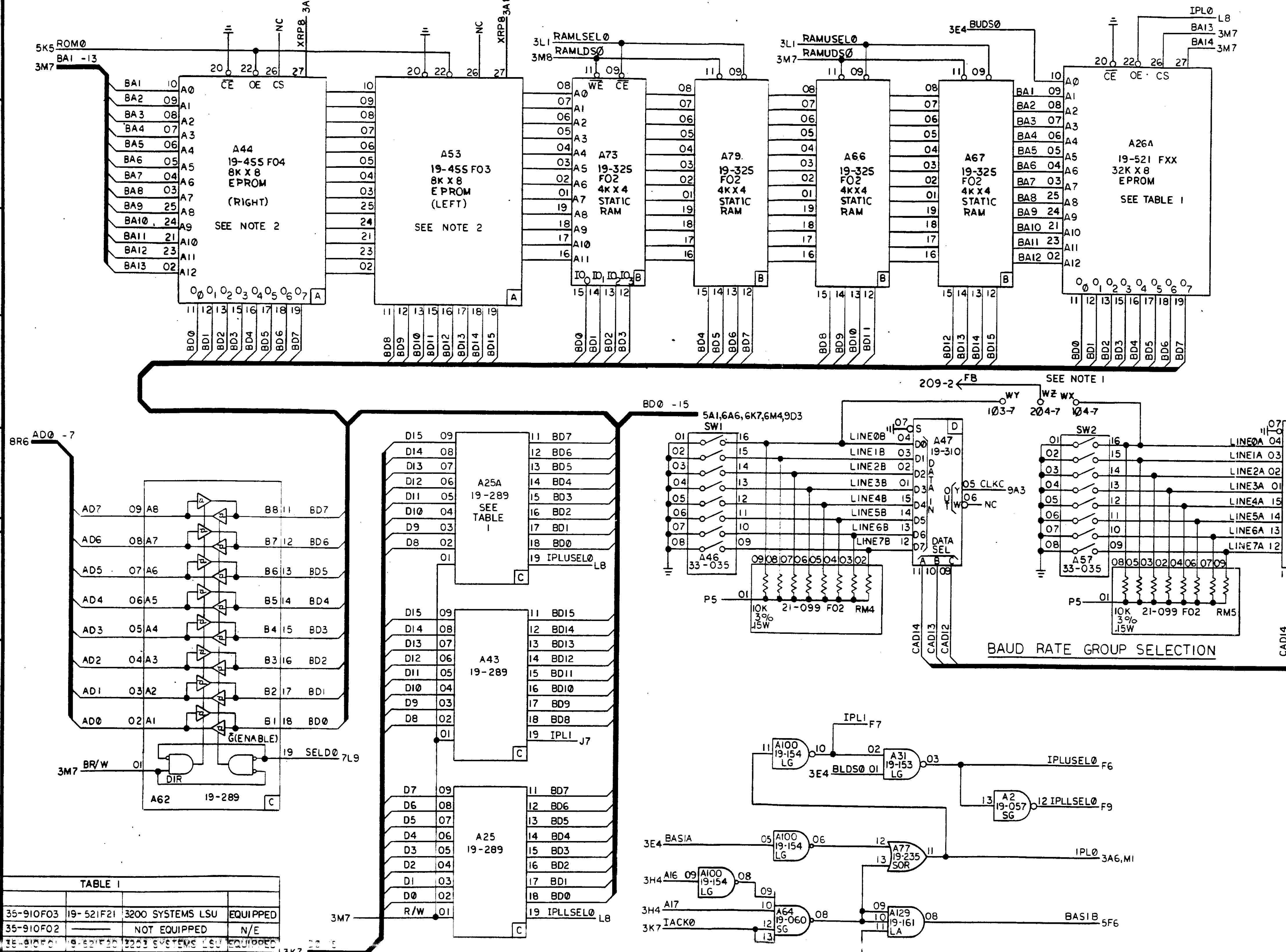
TITLE
MULTIPERIPHERAL CONTROLLER

DRAFTER	WM. KITZHOFFER
DATE	8-5-84
TASK	03199
DWG	35-910 R02 D08
SHT	3-16

REVISIONS

AREA M2, IC "A26A" WAS "19-455 FXX 8K X8". AREA M1, MNEMONICS "IPLO" WAS "8KO XREF 5K6, BA13 WAS 8K1 XREF J7, BA14 WAS 8KVI... X..F L4. AREA J8, ADDED IC'S A100 & A77. AREA F7, MNEMONIC "IPL1" WAS "8K1". AREA F6, MNEMONIC "IPLUSELO" WAS "8K..SELO". AREA F9, MNEMONIC "IPLLSELO" WAS "8KLSELO." ... K1, ... 19 455 F05 & F12.

BA		7112	MS	1-27-86	201	X



PART NO.	A26A	COMMENTS	A25A
35-910F03	19-521F21	3200 SYSTEMS LSU	EQUIPPED
35-910F02	———	NOT EQUIPPED	N/E
35-910F01	19-521F20	3203 SYSTEMS LSU	EQUIPPED
35-910F00	———	NOT EQUIPPED	EQUIPPED

TABLE I

NOTES

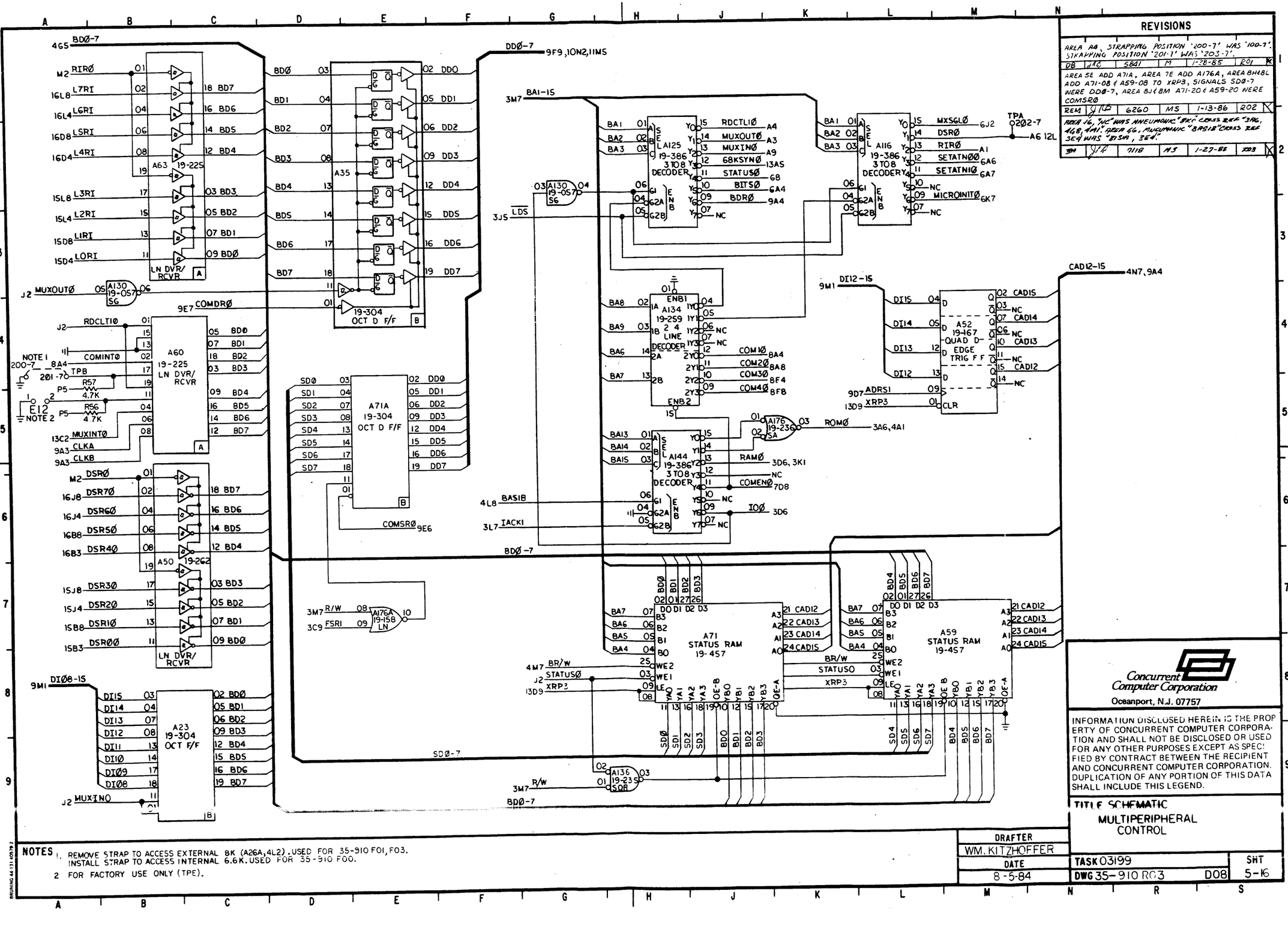
1. USE TO EXTERNALLY FORCE LINE Ø BAUD RATE.
2. A44, A53 MUST BE SAME REVISION

Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE: MULTIPERIPHERAL CONTROLLER

DRAFTER	DATE	TASK	DWG		SHT
WM. KITZHOFFER	8-5-84	03199	35-910 R01	D08	4-16

REVISIONS					
AREA A8, STRAPPING POSITION '200-7' WAS '100-7'. STRAPPING POSITION '201-1' WAS '203-7'.					
DB	JAC	5841	M	1-26-85	R01 K
AREA 5E ADD A71A, AREA 7E ADD A176A, AREA 8H&8L ADD A71-08 & A59-08 TO XRP3, SIGNALS SD0-7 WERE DD0-7, AREA 8J & 8M A71-20 & A59-20 WERE COMSR0					
REM	JAC	6260	MS	1-13-86	R02 K
AREA 1G, "NC" WAS MNEUMONIC "BKC" CROSS REF "3A6, 4G8, 4A1". AREA 6G, MNEUMONIC "BA9,8" CROSS REF SE4 WAS "9D5A, 3E4".					
3M	JAC	7118	MS	1-27-86	R03 K



NOTES

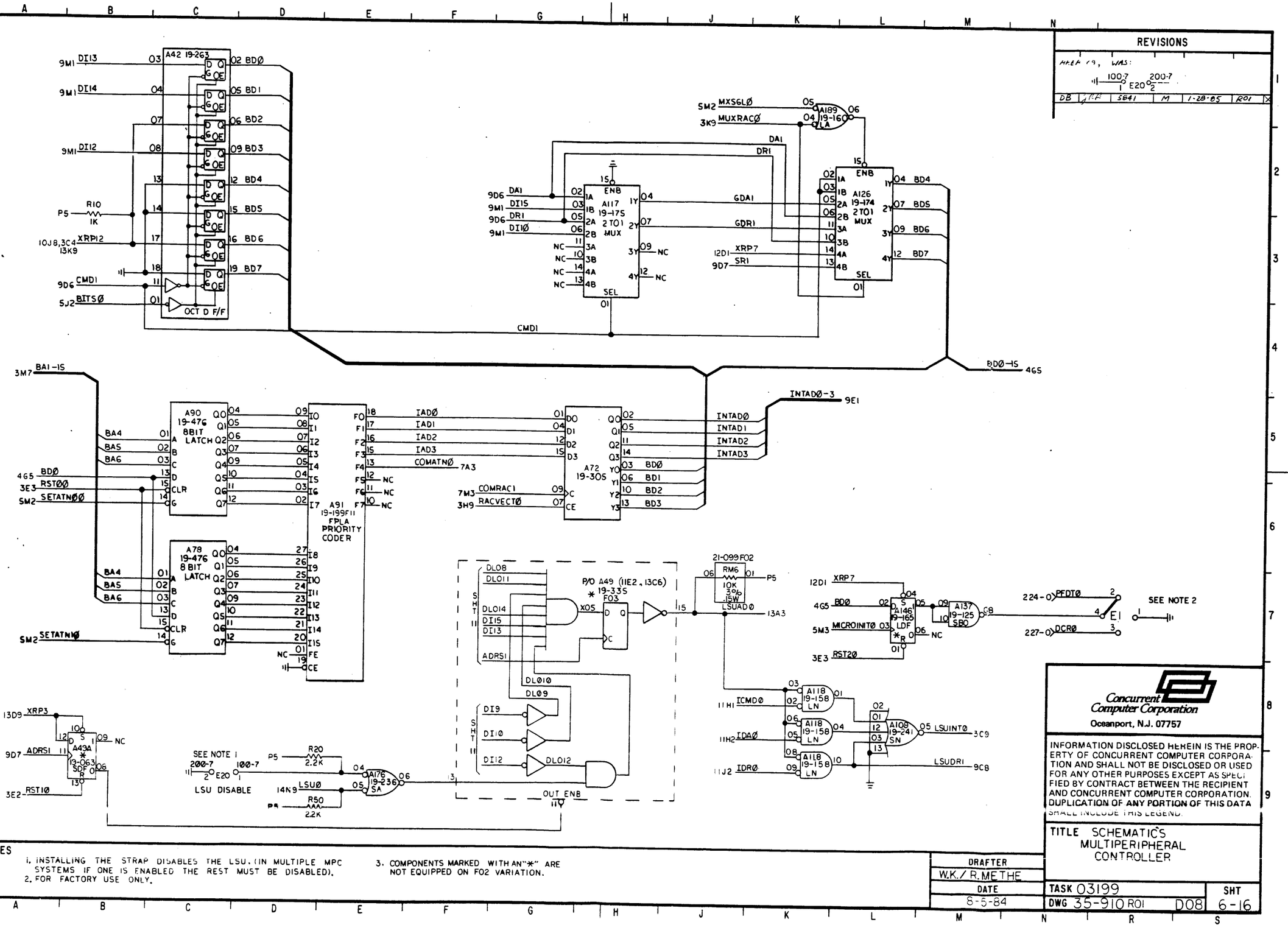
1. REMOVE STRAP TO ACCESS EXTERNAL 8K (A26A,4L2), USED FOR 35-910 F01, F03. INSTALL STRAP TO ACCESS INTERNAL 6.6K. USED FOR 35-910 F00.
2. FOR FACTORY USE ONLY (TPE).

DRAFTER	WM. KITZHOFFER
DATE	8-5-84

Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE SCHEMATIC
MULTIPERIPHERAL CONTROL

TASK 03199		SHT
DWG 35-910 R03	D08	5-16



REVISIONS

HREV 19, WAS:
100-7 1 E20 200-7 2

DB		5841	M	1-28-85	R01	X

NOTES

1. INSTALLING THE STRAP DISABLES THE LSU. (IN MULTIPLE MPC SYSTEMS IF ONE IS ENABLED THE REST MUST BE DISABLED).
2. FOR FACTORY USE ONLY.
3. COMPONENTS MARKED WITH AN "*" ARE NOT EQUIPPED ON F02 VARIATION.

TITLE SCHEMATICS MULTIPERIPHERAL CONTROLLER

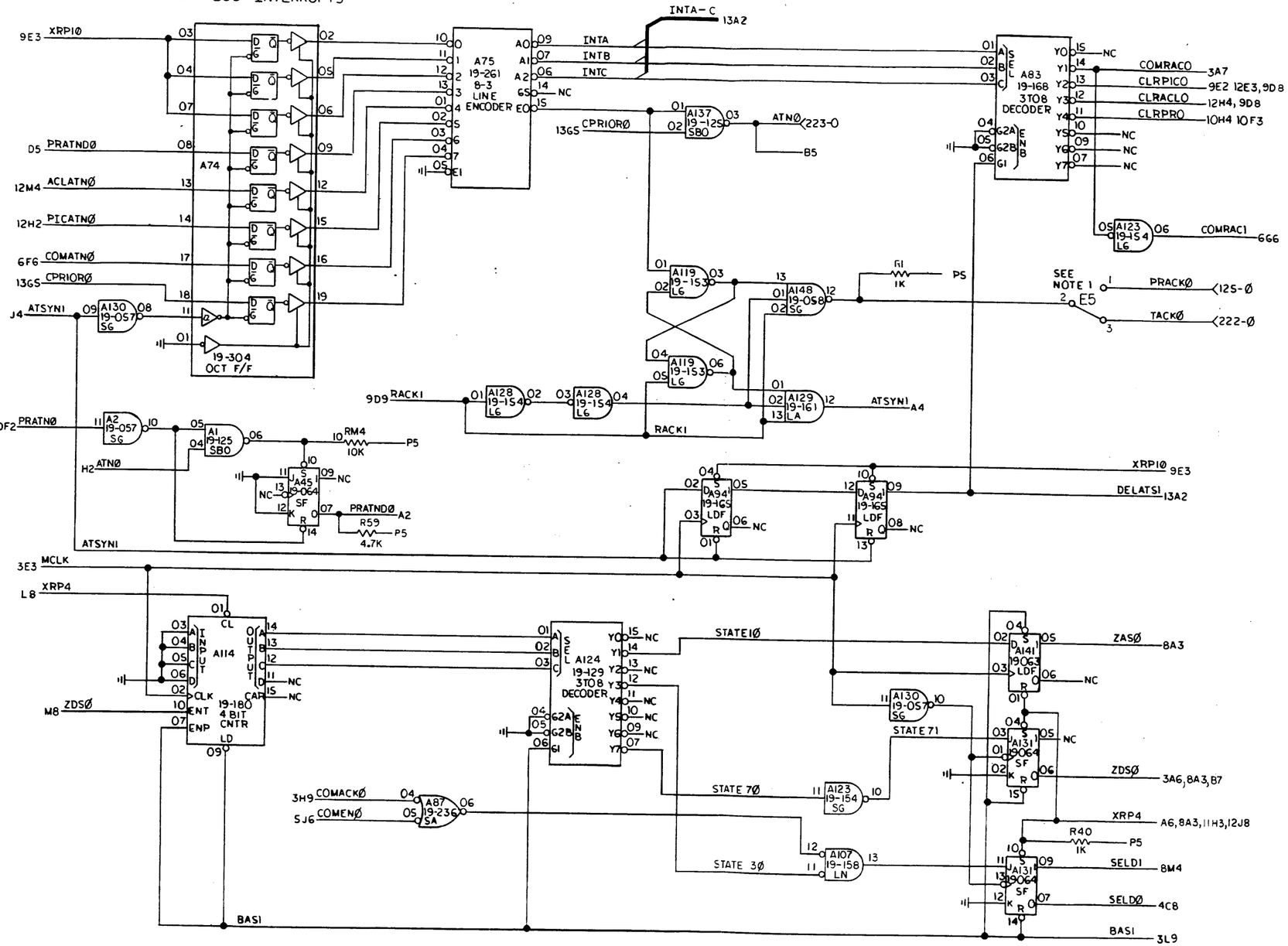
DRAFTER	
W.K./R.METHE	
DATE	
8-5-84	

TASK 03199

DWG 35-910 R01 D08

SHT 6-16

MUX BUS INTERRUPTS



REVISIONS

(AREA C5) ADDED GATES A2, A1, A45 AND RESISTOR MODULE RM4. (AREA A2) MNEMONIC PRATNDØ ≤ CROSS REF. DS WERE "PRATNØ" & "10F2". (AREA H2) ADDED CROSS REF "B5" TO MNEMONIC ATNØ.					
DB	[illegible]	6068	M	6-25-85	R01
REWIRED MNEM DS PULLED & "59 TO MNEMONIC PCATNDØ.					
BP	[illegible]	6736	M5	1-09-87	E02

NOTES

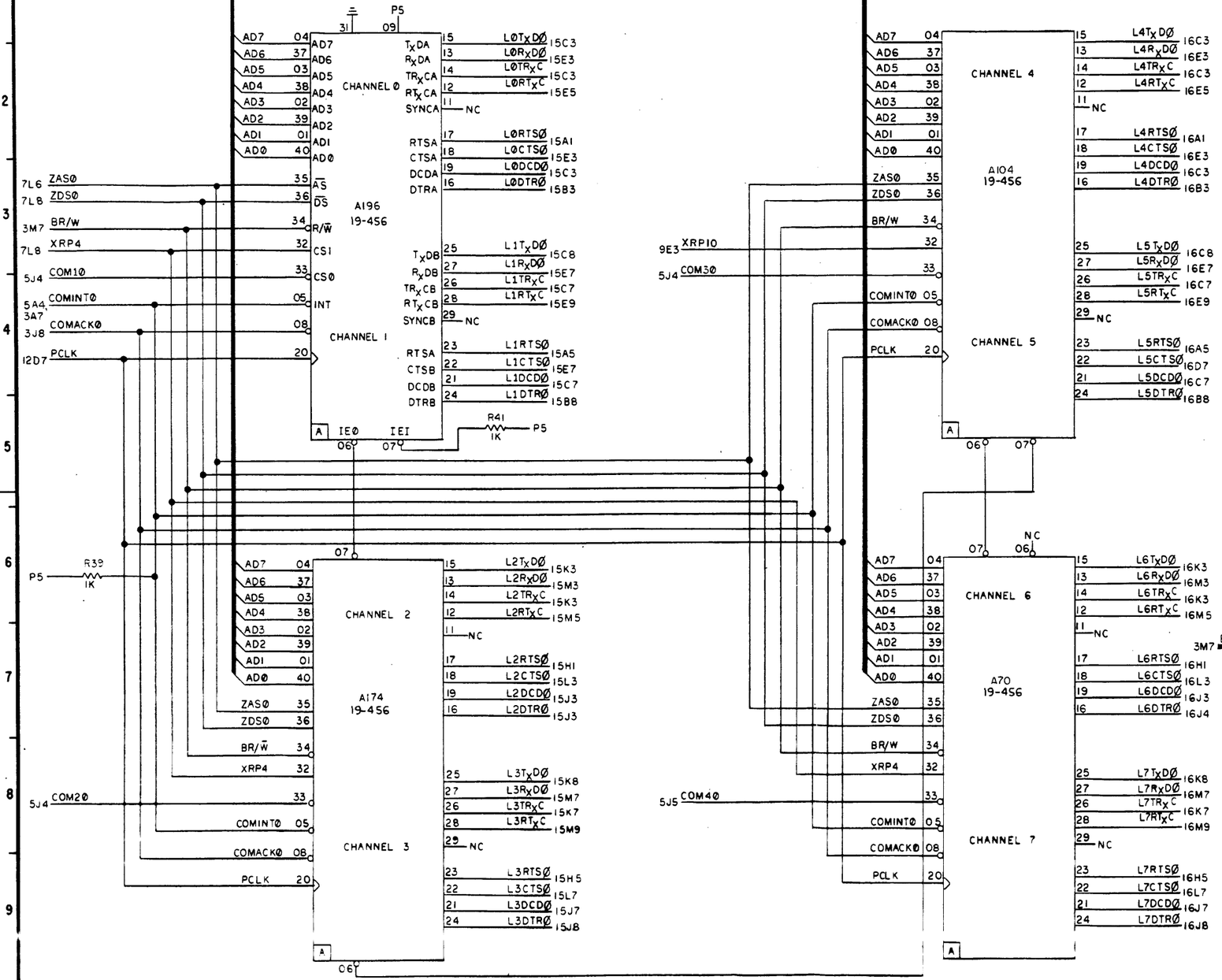
1. STRAP E5-2 TO E5-3 FOR NORMAL USE.
   STRAP E5-2 TO E5-1 FOR FACTORY USE.

BRUNING 44-131 40979-2

Concurrent Computer Corporation
Oceanport, N.J. 07757

DRAFTER	WM. KITZHOFFER
DATE	8-5-84
TITLE SCHEMATIC	MULTIPERIPHERAL CONTROLLER
TASK 03199	
DWG 35-910 R02 D08	SHT 7-16

REVISIONS					
REMOVED NOTE 1. "Z-SCC: VCC: PIN 9, GND: 31." AREA D2, ON IC A196, ADDED LEADS 09 & 31.					
DB	DCB	5841	M	1-28-85	R01



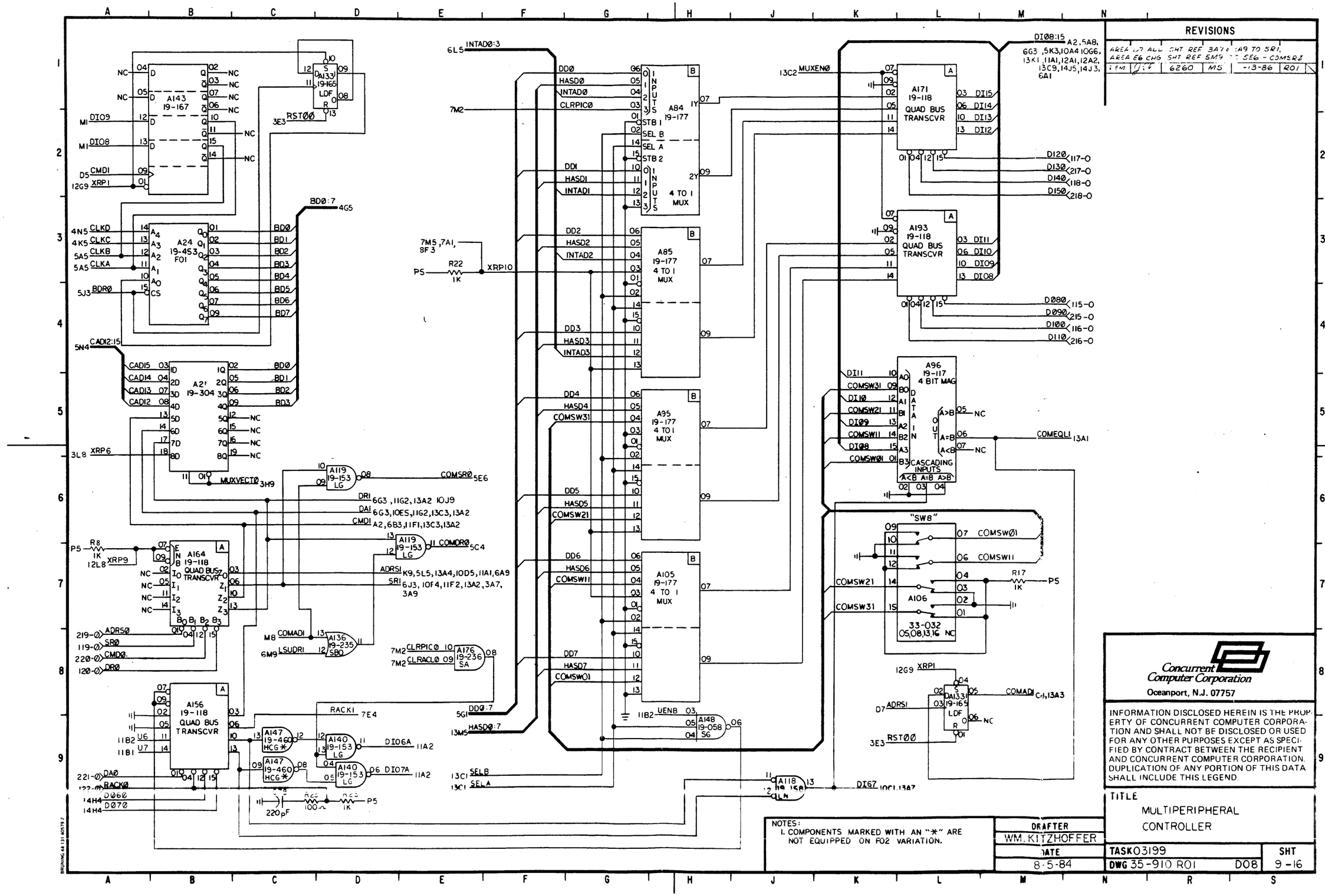
NOTES

Concurrent Computer Corporation
Oceanport, N.J. 07757

DRAFTER	WM. KITZHOFFER
DATE	9-5-84

TITLE: MULTIPERIPHERAL CONTROLLER

TASK 03199		SHT
DWG 35-910 R01	D08	8-16


REVISIONS
AREA 07 ALL SHT REF BA7 TO A9 TO SR1.
AREA E6 CHG SHT REF SM9 TO SE6 - COMSR2
ITEM | DIR | 6260 | MS | -13-86 | R01
A143 19-167
A133 19-165
A24 19-453 F01
A2' 19-304
A119 19-153 LG
A164 19-118 QUAD BUS TRANSCVR
A136 19-235 SBO
A176 19-236 SA
A156 19-118 QUAD BUS TRANSCVR
A147 19-460 HCG*
A140 19-153 LG
A84 19-177 4 TO 1 MUX
A85 19-177 4 TO 1 MUX
A95 19-177 4 TO 1 MUX
A105 19-177 4 TO 1 MUX
A148 19-058 SG
A118 19-158
A171 19-118 QUAD BUS TRANSCVR
A193 19-118 QUAD BUS TRANSCVR
A96 19-117 4 BIT MAG
A106
"SW8"
33-032
INTAD0:3
DI08:15 A2,5A8, 6G3,5K3,10A4 10G6, 13K1,11A1,12A1,12A2, 13C9,14J5,14J3, 6A1
MUXEN0 13C2
XRP1 12G9
XRP6 3L8
XRP9 12L8
XRP10 P5
RST00 3E3
CMDI D5
DIO9 M1
DIO8 M1
CLKD 4N5
CLKC 4K5
CLKB 5A5
CLKA 5A5
BDR0 5J3
CADI2:15 5N4
BD0:7 4G5
DRI 6G3,11G2,13A2 10J9
DAI 6G3,10E5,11G2,13C3,13A2
CMDI A2,6B3,11F1,13C3,13A2
ADRSI K9,5L5,13A4,10D5,11A1,6A9
SRI 6J3,10F4,11F2,13A2,3A7, 3A9
MUXVECT2 3H9
COMSR0 5E6
COMDR0 5C4
COMADI M8
LSUDRI 6M9
CLRPIC0 7M2
CLRACL0 7M2
RACK1 7E4
RACK0
D060 14H4
D070 14H4
DA0 221-0
ADRS0 219-0
SR0 119-0
CMD0 220-0
DR0 120-0
U6 11B2
U7 11B1
DD0:7 5G1
HASD0:7 13M5
SELB 13C1
SELA 13C1
UENB 11B2
DI06A 11A2
DI07A 11A2
DI67 10C1,13A7
COMEQLI 13A1
D120 117-0
D130 217-0
D140 118-0
D150 218-0
D080 115-0
D090 215-0
D100 116-0
D110 216-0
COMADI C-1,13A3
R8 1K
R22 1K
R17 1K
220pF
100Ω
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Oceanport, N.J. 07757
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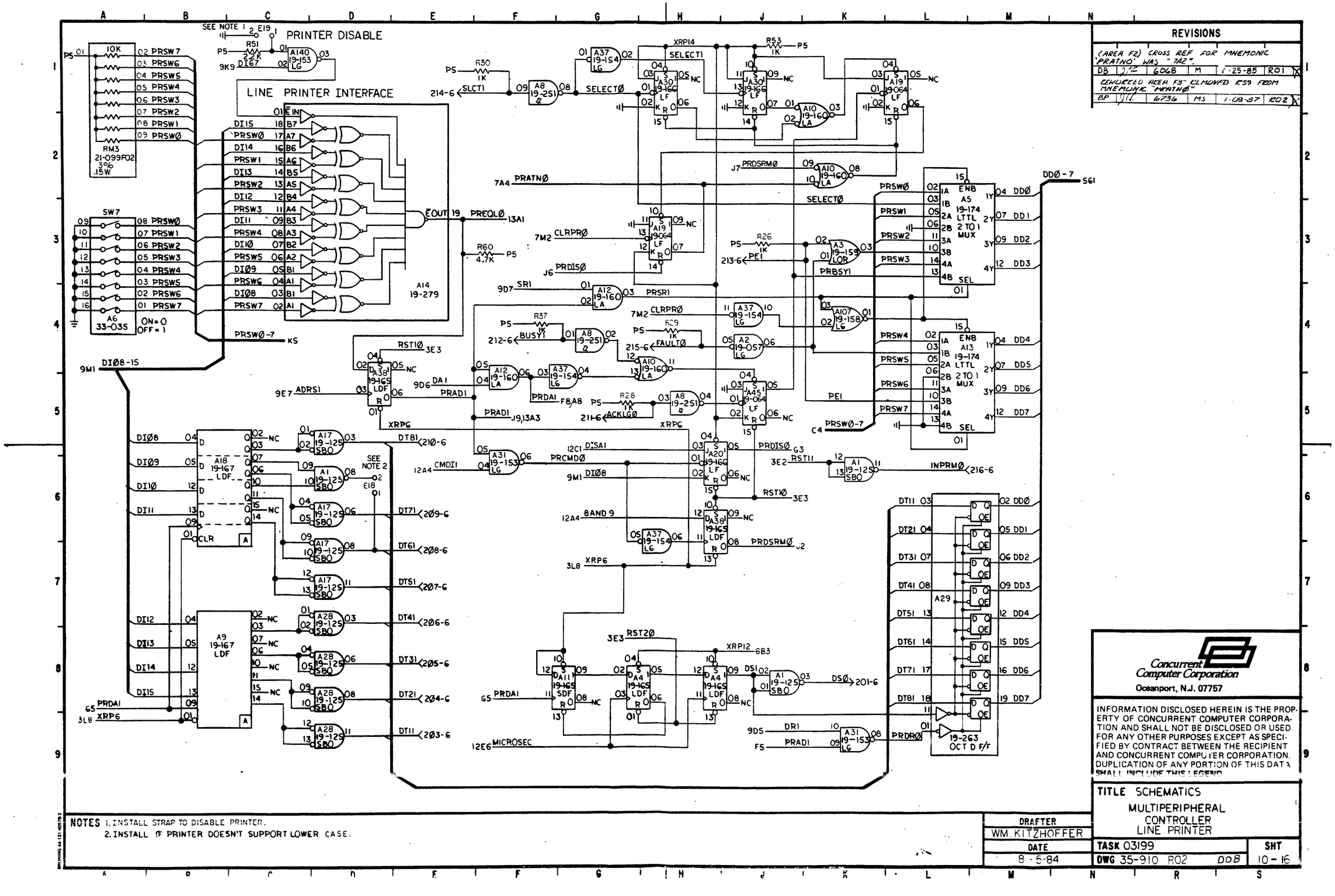
NOTES:
1. COMPONENTS MARKED WITH AN "*" ARE NOT EQUIPPED ON F02 VARIATION.
DRAFTER WM. KITZHOFFER
DATE 8-5-84
TITLE MULTIPERIPHERAL CONTROLLER
TASK 03199
DWG 35-910 R01 D08
SHT 9-16
BRUNING 44 131 405792



NOTES 1. INSTALL STRAP TO DISABLE PRINTER.
2. INSTALL IF PRINTER DOESN'T SUPPORT LOWER CASE.

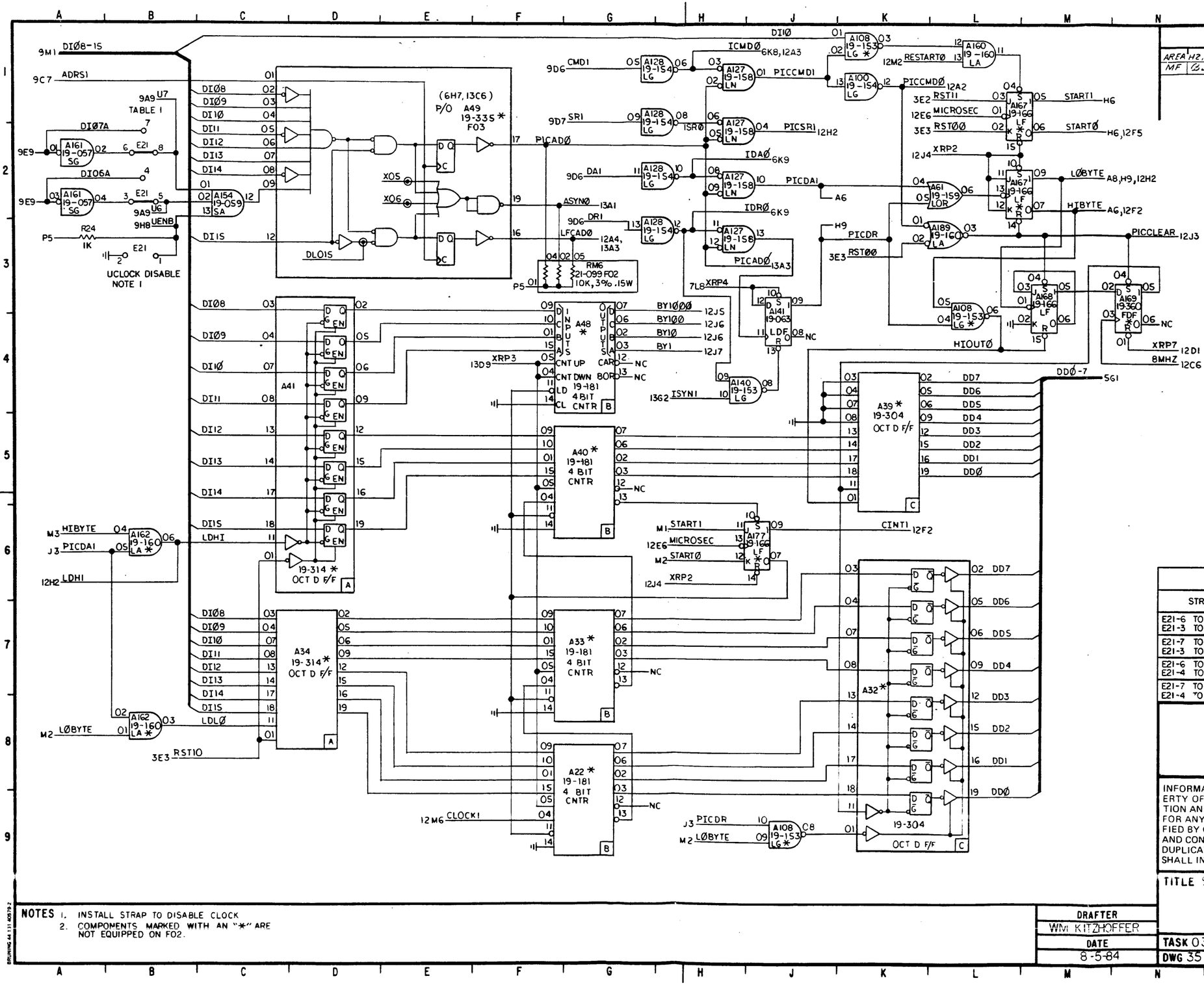
REVISIONS					
(AREA F2) CROSS REF FOR MNEMONIC 'PRATNO' WAS "7A2".					
DB	7.12	6068	M	1-25-85	R01
LENGTHED HIGH F3" CLMOMFD R59 FROM MNEMONIC "PRATNØ"					
BP	7.11	6736	M3	1-09-87	R02

Concurrent Computer Corporation
Oceanport, N.J. 07757

DRAFTER	WM. KITZHOFFER
DATE	8-5-84

TITLE SCHEMATICS
MULTIPERIPHERAL CONTROLLER LINE PRINTER

TASK 03199 | SHT 10-16
DWG 35-910 R02 D08



REVISIONS					
AREA #2. REMOVED ASTERISK FROM A127.					
MF	B.J.	5892	M	3-8-85	R01

TABLE 1		
STRAP	UCLOCK DEVICE ADDRESS	NOTE
E21-6 TO E21-8 E21-3 TO E21-5	06C / 06D	NORMAL STRAP
E21-7 TO E21-8 E21-3 TO E21-5	16C / 16D	
E21-6 TO E21-8 E21-4 TO E21-5	26C / 26D	
E21-7 TO E21-8 E21-4 TO E21-5	36C / 36D	

Concurrent Computer Corporation
Oceanport, N.J. 07757

NOTES
1. INSTALL STRAP TO DISABLE CLOCK
2. COMPONENTS MARKED WITH AN "*" ARE NOT EQUIPPED ON FO2.

DRAFTER	WM KITZHOFFER
DATE	8-5-84
TITLE	SCHEMATIC MULTIPERIPHERAL CONTROLLER (UNIVERSAL CLOCK)
TASK	03199
DWG	35-910 R01 D08
SHT	11-16

BRUNING 44 131 40579.2

REVISIONS				
AREA BB, REVISED STRAPPING AT E26. (AREA L4) CROSS REF FOR CONNECTOR WAS '201-7'.				
DB	5841	M	1-28-85	R01
AREA J8 ADD SHT REF 3A9 TO XRP4				
REM	6260	MS	1-13-86	R02

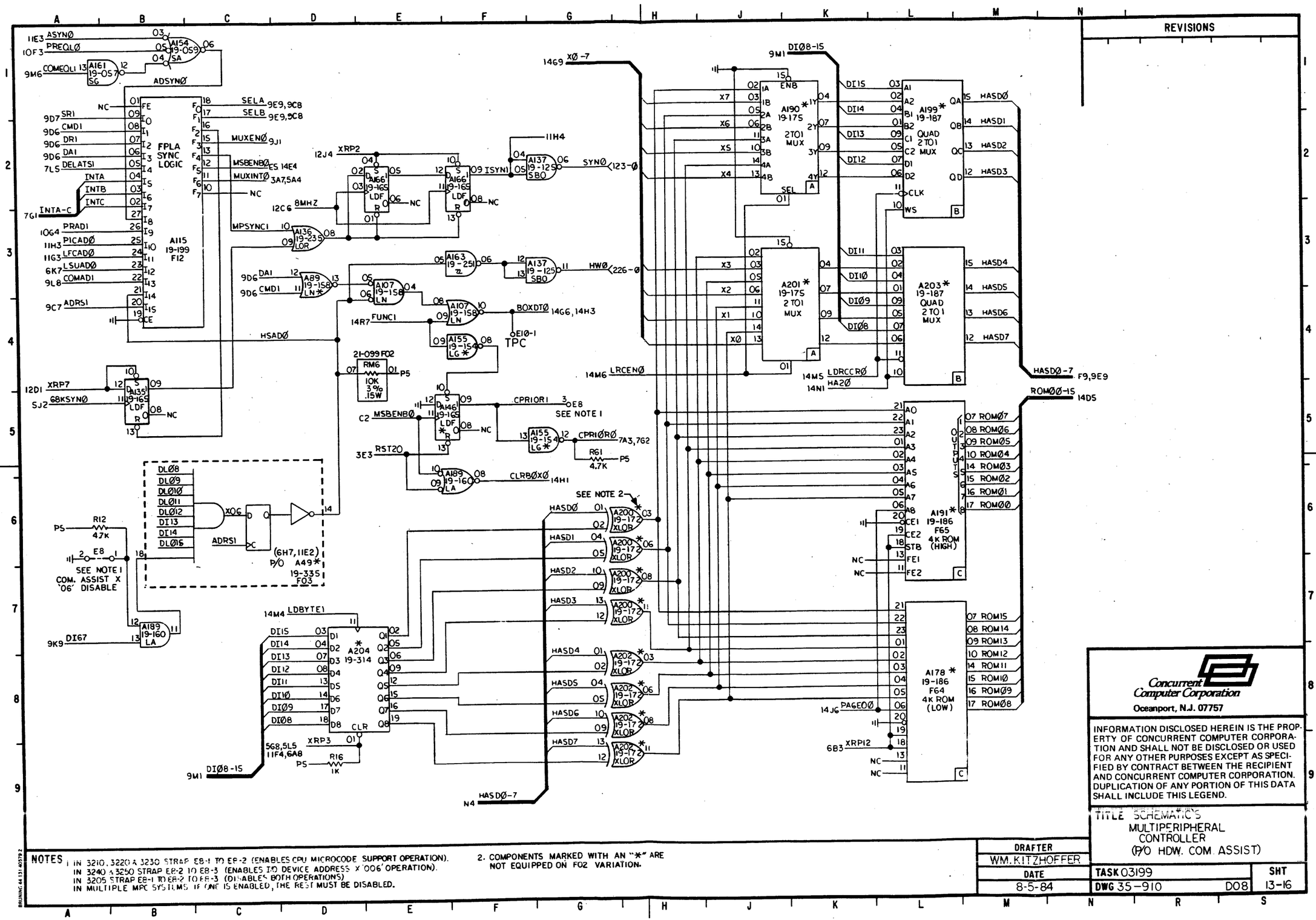
NOTES
1. INSTALL STRAP FOR DIAGNOSTIC TESTING. REMOVE FOR NORMAL USE.
2. FACTORY USE SET FOR 19.2KB.
3. FOR FACTORY USE ONLY.
4. COMPONENTS MARKED WITH AN "*" ARE NOT EQUIPPED ON F02 VARIATION.

Concurrent Computer Corporation
Oceanport, N.J. 07757

DRAFTER	WM. KITZHOFFER
DATE	8-5-84

TITLE SCHEMATIC'S MULTIPERIPHERAL CONTROLLER (UNIVERSAL CLOCK)

TASK 03199 | SHT 12-16 | DWG 35-910 R02 | DOC


REVISIONS
FPLA SYNC LOGIC
A115 19-199 F12
A154 19-059 SA
A161 19-057 SG
ADSYNØ
ASYNØ
PREQLØ
COMEQLI
SELA 9E9,9C8
SELB 9E9,9C8
MUXENØ 9J1
MSBENBØ ES 14E4
MUXINTØ 3A7,5A4
NC
SRI
CMDI
DRI
DAI
DELATSI
INTA
INTB
INTC
INTA-C
PRADI
PICADØ
LFCADØ
LSUADØ
COMADI
ADRSI
8MHZ
MPSYNCI
XRP2
A166 19-165 LDF
A137 19-125 SBO
ISYNI
SYNØ <123-Ø
A136 19-235 LOR
A163 19-251
HWØ <226-Ø
A89 19-158 LN*
A107 19-158 LN
FUNCI
BOXDTØ 14G6, 14H3
EIØ-1
TPC
A155 19-154 LG*
21-099 F02
RM6 10K 3% .15W
P5
XRP7
SJ2 68KSYNØ
A135 19-165 LDF
A146 19-165 LDF*
CPRIØRI
SEE NOTE 1
MSBENBØ
RST20
A155 19-154 LG*
CPRIØRØ 7A3,7G2
R61 4.7K
A189 19-160 LA
CLRBØXØ 14H1
SEE NOTE 2
DLØ8
DLØ9
DLØ10
DLØ11
DLØ12
DI13
DI14
DLØ16
XOR
ADRSI
(6H7, 11E2) P/O A49* 19-335 F03
R12 4.7K
SEE NOTE 1 COM. ASSIST X '06' DISABLE
DI67
LDBYTE1
A204 19-314
DIØ8-15
XRP3
R16 1K
5G8,5L5 11F4,6A8
HASDØ-7
N4
HASDØ
HASD1
HASD2
HASD3
HASD4
HASD5
HASD6
HASD7
A200 19-172 XLOR
XØ-7
1469
DIØ8-15
9M1
ENB
A190* 19-175 2TO1 MUX
A201* 19-175 2TO1 MUX
A199* 19-187 QUAD 2TO1 MUX
A203* 19-187 QUAD 2TO1 MUX
DI15
DI14
DI13
DI12
DI11
DIØ
DIØ9
DIØ8
CLK
WS
HASDØ
HASD1
HASD2
HASD3
HASD4
HASD5
HASD6
HASD7
HASDØ-7 F9,9E9
LRCENØ
14M6
LDRCCRØ
HA2Ø
14M5
14N1
ROMØØ-15 14D5
A191* 19-186 F65 4K ROM (HIGH)
A178* 19-186 F64 4K ROM (LOW)
ROM15
ROM14
ROM13
ROM12
ROM11
ROM10
ROM09
ROM08
ROM07
ROM06
ROM05
ROM04
ROM03
ROM02
ROM01
ROMØØ
PAGEØØ
14J6
XRPI2
6B3
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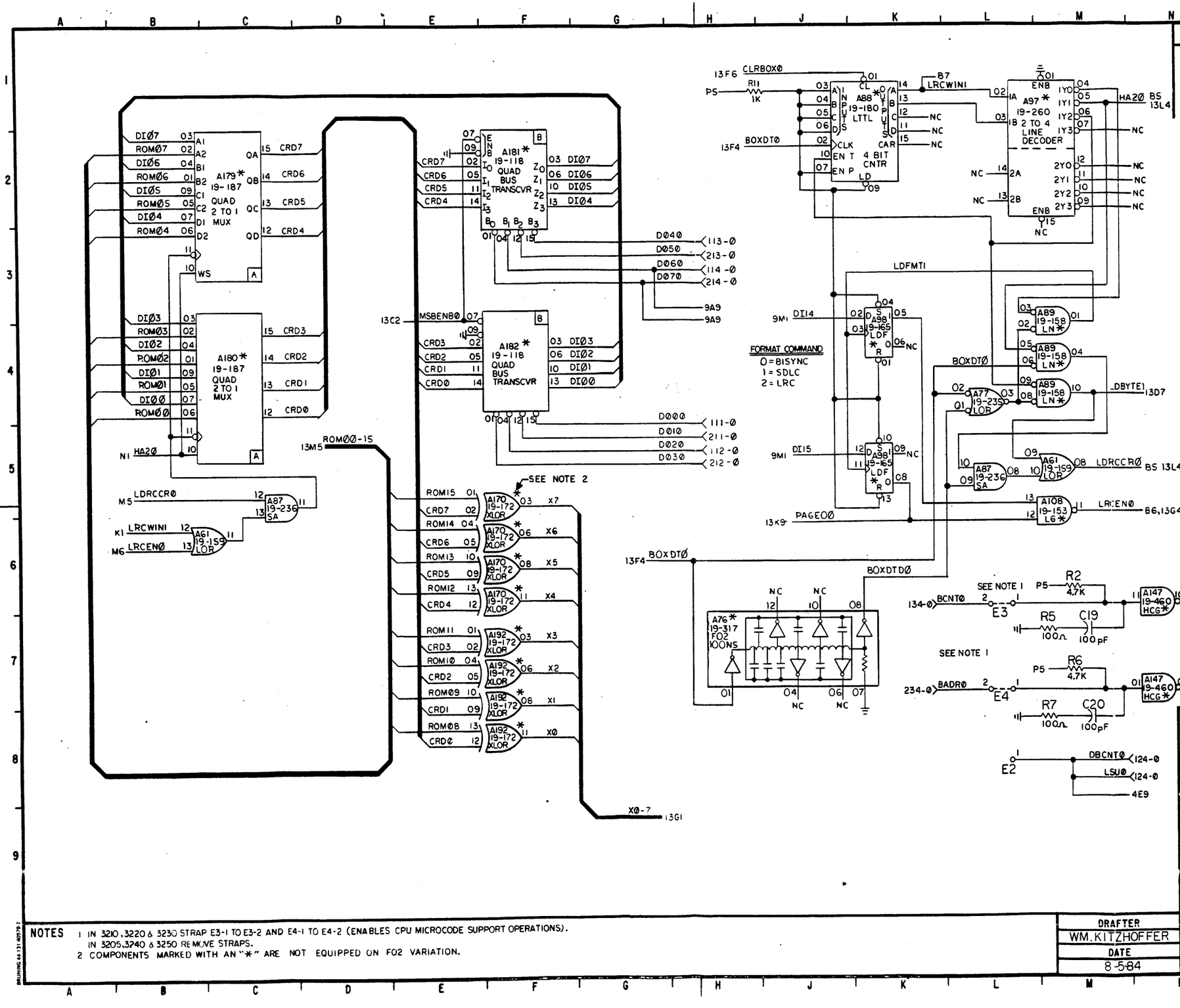
TITLE SCHEMATICS
MULTIPERIPHERAL CONTROLLER
(P/O HDW. COM. ASSIST)
DRAFTER WM. KITZHOFFER
DATE 8-5-84
TASK 03199
DWG 35-910 D08
SHT 13-16
NOTES
1. IN 3210, 3220 & 3230 STRAP E8-1 TO E8-2 (ENABLES CPU MICROCODE SUPPORT OPERATION).
IN 3240 & 3250 STRAP E8-2 TO E8-3 (ENABLES I/O DEVICE ADDRESS X'006' OPERATION).
IN 3205 STRAP E8-1 TO E8-2 TO E8-3 (DISABLES BOTH OPERATIONS)
IN MULTIPLE MPC SYSTEMS, IF ONE IS ENABLED, THE REST MUST BE DISABLED.
2. COMPONENTS MARKED WITH AN "*" ARE NOT EQUIPPED ON F02 VARIATION.



NOTES
1 IN 3210, 3220 & 3230 STRAP E3-1 TO E3-2 AND E4-1 TO E4-2 (ENABLES CPU MICROCODE SUPPORT OPERATIONS).
IN 3205, 3240 & 3250 REMOVE STRAPS.
2 COMPONENTS MARKED WITH AN "*" ARE NOT EQUIPPED ON FO2 VARIATION.

REVISIONS

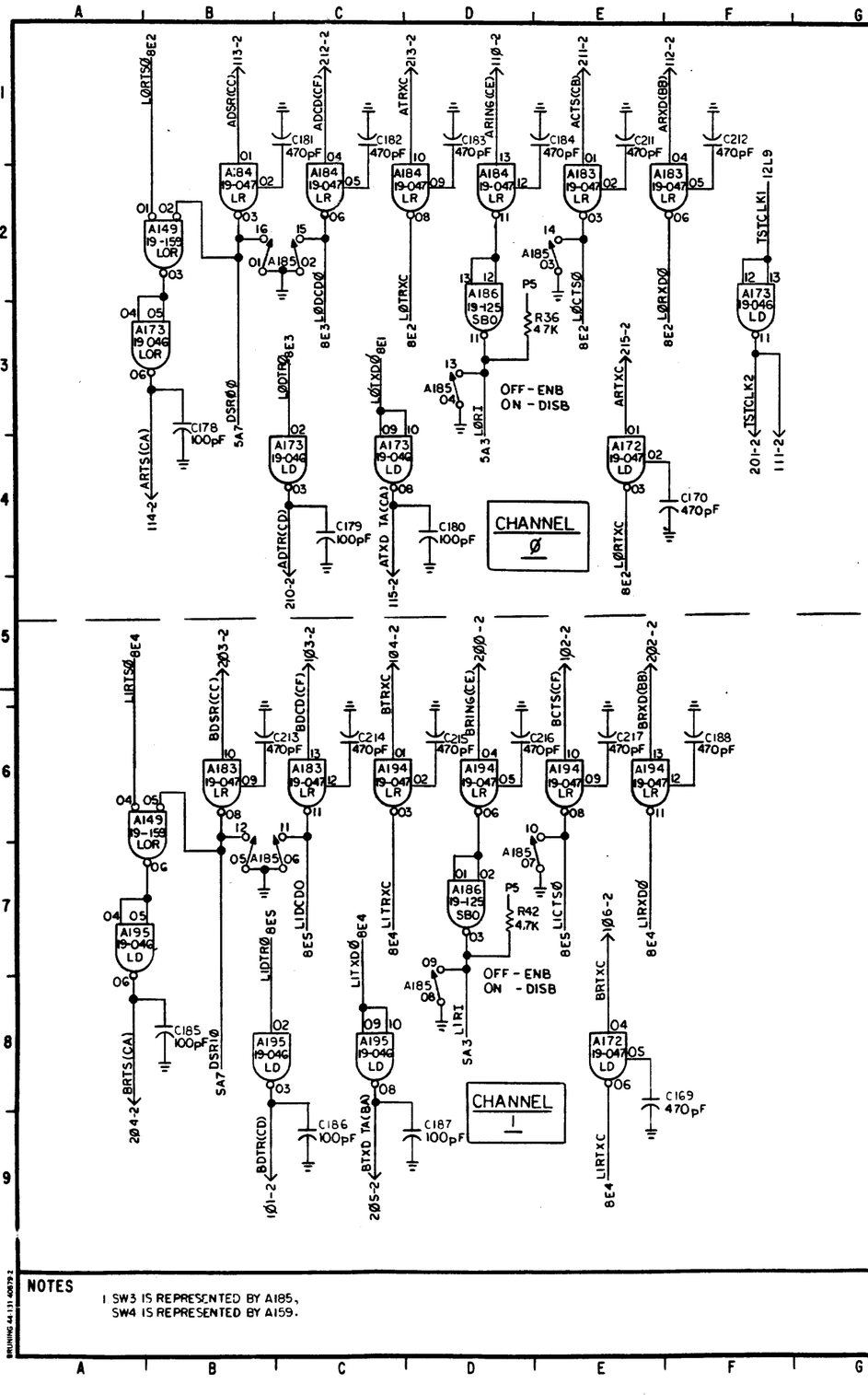
Concurrent Computer Corporation
Oceanport, N.J. 07757

DRAFTER	WM. KITZHOFFER
DATE	8-5-84

TITLE
MULTIPERIPHERAL CONTROLLER (HDW. COM. ASSIST)

TASK 03199 SHT 14-16
DWG 35-910 D08

BRUNING 44 131 40572



NOTES

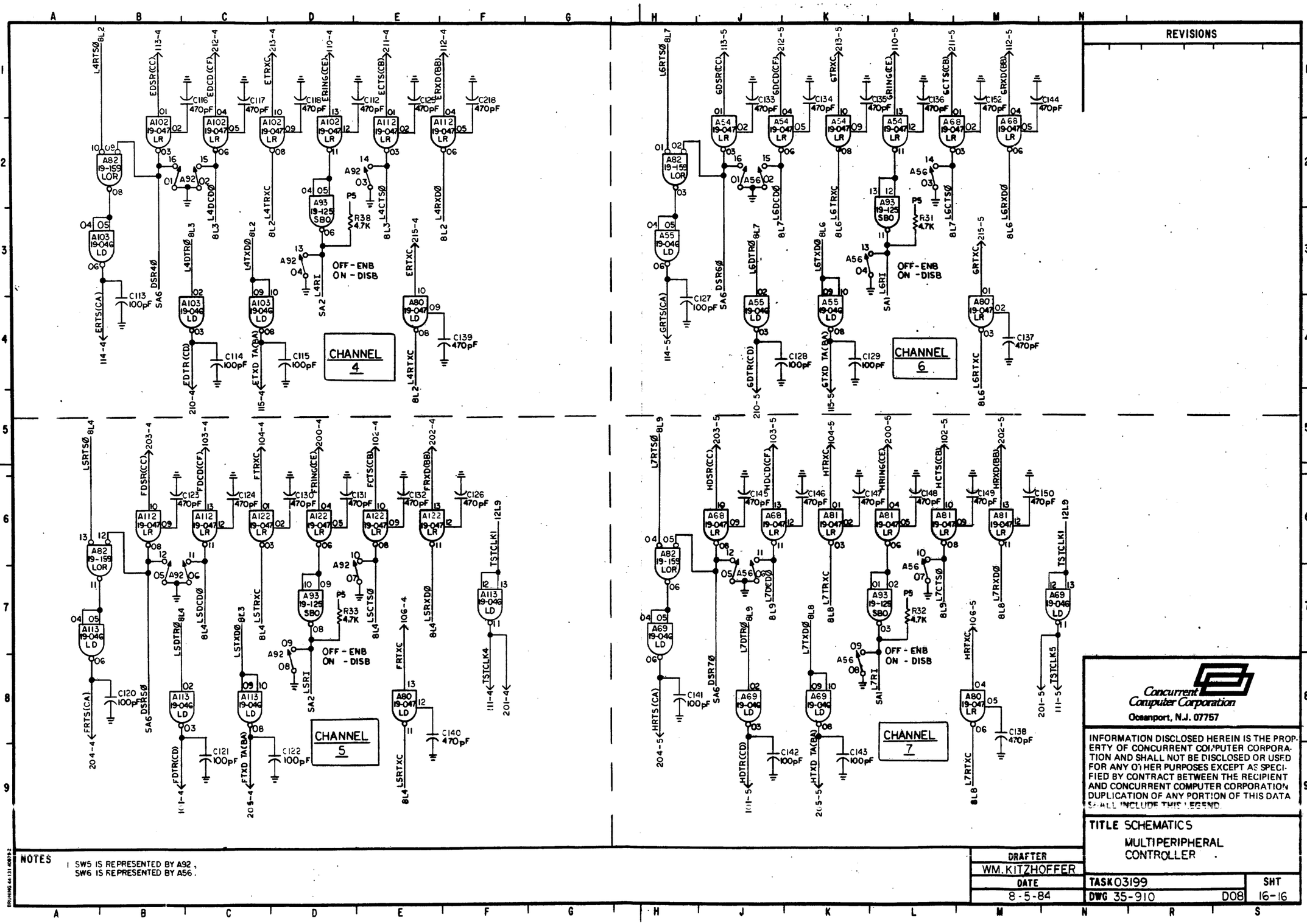
1 SW3 IS REPRESENTED BY A185,
SW4 IS REPRESENTED BY A159.

DRAWING 44 131 40972

Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE SCHEMATICS
MULTIPERIPHERAL CONTROLLER

DRAWER	
WM. KITZHOFFER	
DATE	TASK 03199
8-9-84	DWG 35-910 D08
	SHT 15-16


REVISIONS
L4RTSØ
EDSR(CC)
EDCD(CF)
ETRXC
ERING(CE)
ECTS(CB)
ERXD(BB)
A82 19-159 LOR
A103 19-046 LD
A112 19-047 LR
A92
A93 19-125 SBO
R38 4.7K
OFF-ENB ON-DISB
L4RI
L4DCDØ
L4DTRØ
L4TXDØ
L4CTSØ
L4RXDØ
L4TRXC
ERTXC
ERTS(CA)
DSRSØ
EDTR(CD)
ETXD TA(BA)
L4RTXC
C113 100pF
C114 100pF
C115 100pF
C116 470pF
C117 470pF
C118 470pF
C112 470pF
C125 470pF
C218 470pF
C139 470pF
CHANNEL 4
L6RTSØ
GDSR(CC)
GDCD(CF)
GTRXC
GRING(CE)
GCTS(CB)
GRXD(BB)
A54 19-047 LR
A55 19-046 LD
A68 19-047 LR
A56
L6RI
L6DCDØ
L6DTRØ
L6TXDØ
L6CTSØ
L6RXDØ
L6TRXC
GRTXC
GRTS(CA)
DSR6Ø
GDTR(CD)
GTXD TA(BA)
L6RTXC
C127 100pF
C128 100pF
C129 100pF
C133 470pF
C134 470pF
C135 470pF
C136 470pF
C152 470pF
C144 470pF
C137 470pF
CHANNEL 6
LSRTSØ
FDSR(CC)
FDCD(CF)
FTRXC
FRING(CE)
FCTS(CB)
FRXD(BB)
A122 19-047 LR
A113 19-046 LD
LSRI
LSDCDØ
LSDTRØ
LSTXDØ
LSCTSØ
LSRXDØ
LSTRXC
FRTXC
FRTS(CA)
DSRSØ
FDTR(CD)
FTXD TA(BA)
LSRTXC
C120 100pF
C121 100pF
C122 100pF
C123 470pF
C124 470pF
C130 470pF
C131 470pF
C132 470pF
C126 470pF
C140 470pF
CHANNEL 5
L7RTSØ
HDSR(CC)
HDCD(CF)
HTRXC
HRING(CE)
HCTS(CB)
HRXD(BB)
A68 19-047 LR
A81 19-047 LR
A69 19-046 LD
L7RI
L7DCDØ
L7DTRØ
L7TXDØ
L7CTSØ
L7RXDØ
L7TRXC
HRTXC
HRTS(CA)
DSR7Ø
HDTR(CD)
HTXD TA(BA)
L7RTXC
C141 100pF
C142 100pF
C143 100pF
C145 470pF
C146 470pF
C147 470pF
C148 470pF
C149 470pF
C150 470pF
C138 470pF
CHANNEL 7
TSTCLK1
TSTCLK4
TSTCLK5
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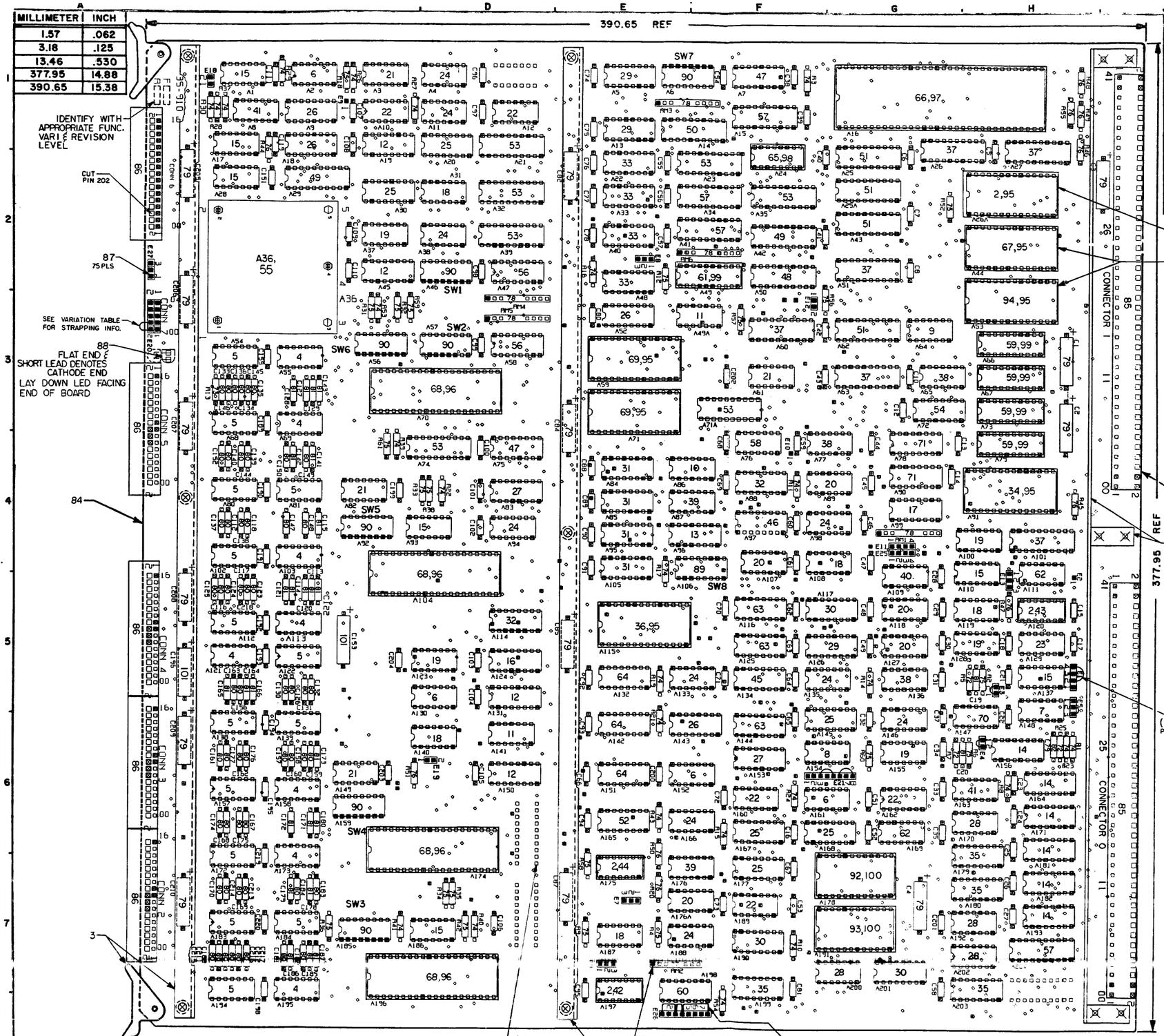
TITLE SCHEMATICS
MULTIPERIPHERAL CONTROLLER
DRAFTER WM. KITZHOFFER
DATE 8-5-84
TASK 03199
DWG 35-910 D08
SHT 16-16
NOTES
1 SW5 IS REPRESENTED BY A92, SW6 IS REPRESENTED BY A56.

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530
377.95	14.88
390.65	15.38



35-910 F03	AS SHOWN PER SHT 1 W/A26A	W/ 3200 IPL
35-910 F02	AS SHOWN PER SHT 2	8 LINE/PRINTER ONLY
35-910 F01	AS SHOWN PER SHT 1 W/A25A	W/ 3203 IPL
35-910 F00	AS SHOWN PER SHT 1 W/O A26A W/STRAP 201-T TO 200-T	W/O EXT IPL
PART NO.	DESCRIPTION	TITLE

FUNCTIONAL VARIATION TABLE

NOTES

1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
2. HEADER STIFFENER TO BE SOLDERED TO GROUND BUS AT 2 ENDS AND CENTER. (APP SIDE)
3. ALL UNSPECIFIED COMPONENTS ARE ITEM 83, 113 PLS.
4. A44 & A53 MUST BE SAME REVISION LEVEL.
5. THIS SPARE LOCATION NOT AVAILABLE. (USED ON EARLIER REVISION) (ECR 6260)

USED IN MANUAL: 47-095

S-T #	2
REVISION	06.06

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	
	PROD	

AREA K5 ADDED A49A TO REF. DESIGNATIONS. AREA A8 ADDED REV. BLOCK. REVISED SHT'S 1 & 2.

MF	GAB	5892	M	2-19-85	R01

(AREA B6) ITEM NO. ON CAPACITORS C53, C54, C96 & C97 WERE #79. REVISED SHTS 1 & 2.

DB	GEB	6068	M	6-25-85	R02

AREA F3 ADDED IC A71A, ITEM 53 (79-304) REVISED SHTS 1 & 2

REA	WHG	6260	MS	7-19-86	R03

REMOVED EJECTOR EARS FROM CONN. 2-6. REVISED SHTS 1 & 2

PE	GEB	6349	E	3-14-86	R04

AREA B6 & C6 REMOVED CAPS. C154 & C97. REVISED SHTS 1 & 2

PE	GEB	6378	MS	3-18-86	R05

RELEASED FOR PRODUCTION

MFG. ENG. MK DATE 9/9/86

MFG. ENGR. ADDED NOTE TO EXCLUDE ETCH #3.

RH	7424	E	2-2-87	R06

RESISTOR	R1-R61, RM1-RM6
TRANSISTOR	
DIODE	L1
CAPACITOR	C1-C8, C10, C12-C35, C37-C49
	C51-C82, C84, C85, C87-C220
INTEGRATED CIRCUIT	A1-A204, A25A, A26A, A176A, A49A, A71A
COMPONENT	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED

SCALE: 2/1	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

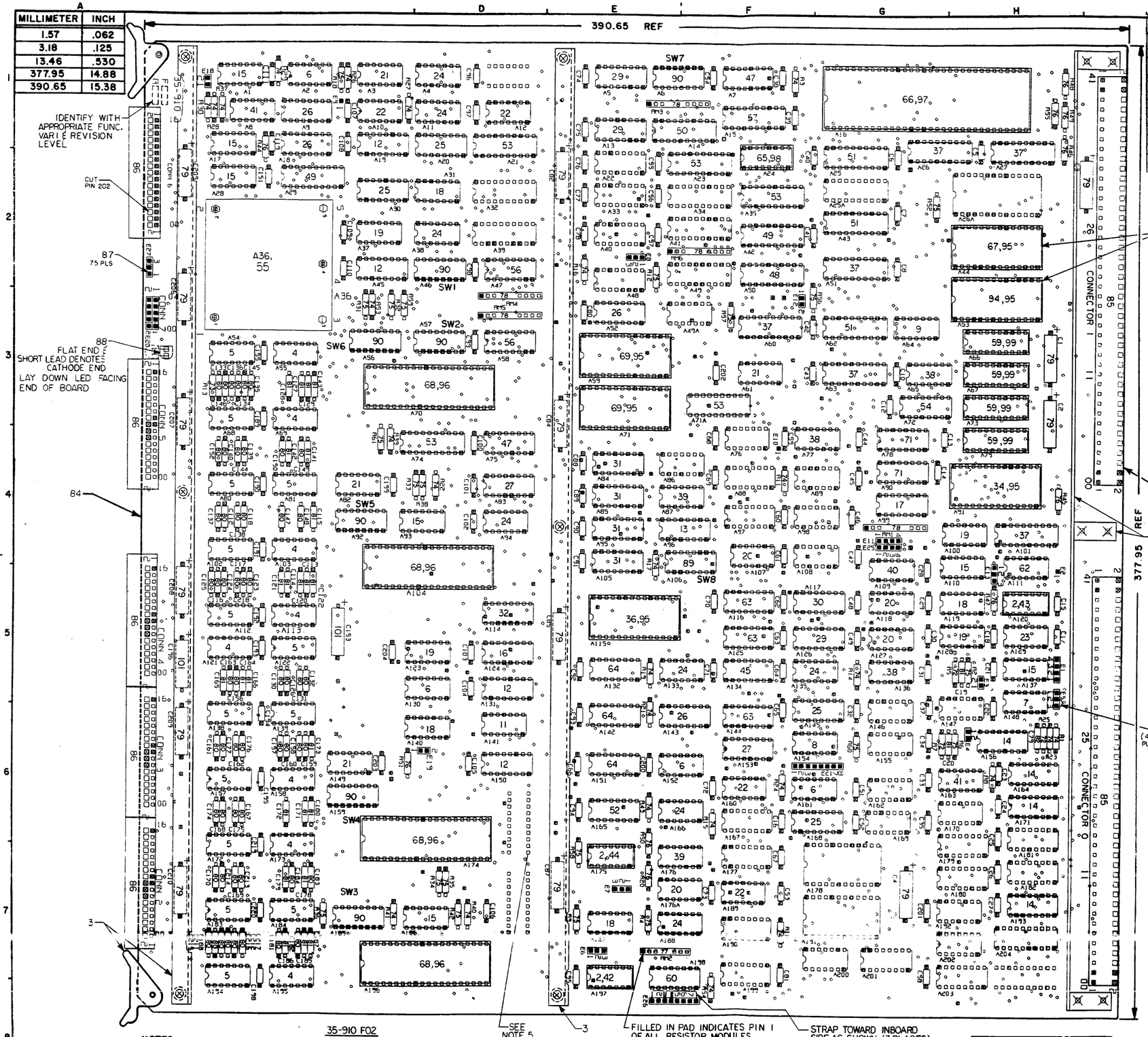
NAME		TITLE	DATE
J. BIELSKIE	K. REED	DES/DFT	11-1-84
R. CERO		SUPV	9-9-86
		CHK	
B. HEITMUELLER		ENG	9-9-86
W. RICE		MGR	9-9-86
R. BARKER		QC	9-9-86

Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE **ASSEMBLY PRINTED CIRCUIT BOARD** MPC

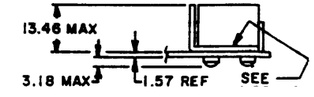
TASK 03107	SHT
DWG 35-910 R06 E03	1-2

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530
377.95	14.88
390.65	15.38



NOTES

1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
2. HEADER STIFFENER TO BE SOLDERED TO GROUND BUS AT 2 ENDS AND CENTER. (APP SIDE)
3. ALL UNSPECIFIED COMPONENTS ARE ITEM 83, 113 PLS.
4. A44 & A53 MUST BE SAME REVISION LEVEL.
5. THIS SPARE LOCATION NOT AVAILABLE. (USE ON EARLIER REVISION) (ECR 6260)



REVISIONS

AREA G5 ADDED IC AT A127. ITEM 20. AREA A5 ADDED REF DESIGNATION A127.				
MF	GJ.	5892	M	2-19-85 R01
(AREA B6) ITEM NO. FOR CAPACITORS C53, C154, C176 & C197 WERE "79"				
DB	MD	6068	M	4-26-86 R02
AREA F3 ADDED IC A71A, ITEM 53 (19-304)				
REM	MD	5260	MS	1-13-86 203
REMOVED EJECTOR EARS FROM CONN. 2-0.				
PE	MD	6349	R	3-14-86 R04
AREA B6 & C6, REMOVED CAPACITORS C154 & C197.				
PE	MD	6378	MS	3-18-86 R05
AREA 28 ADDED NOTE TO REROUTE STRAPS				
RM	MD	7426	R	2-02-89 R06

METRIC

RESISTOR	R1-R61, RM1-RM6
TRANSISTOR	
DIODE	L1
CAPACITOR	C1-C8, C10, C12-C35, C37-C49
	C51-C82, C84, C85, C87-C220
INTEGRATED CIRCUIT	A1-A21, A23-A31, A35-A38, A42-A47, A50-A75, A77-A85, A87, A90-A96, A99-A107, A109-A127, A128-A145, A148-A154, A156-A161, A163-A166, A168, A171-A176, A183-A189, A193-A198, A71A
COMPONENT	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED

SCALE: 2/1

TOLERANCE: .XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°

DIMENSIONS ARE IN INCHES

NAME	TITLE	DATE
	DES/DFT	
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE **ASSEMBLY PRINTED CIRCUIT BOARD** MPC

TASK 03107 SHT

Document Comment Form

In reference to...

Multiperipheral Controller (Multi-Layer MPC) Theory of Operation Manual — 63-022 R00

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Please send us comments, corrections, suggestions, etc. Use the SCR system to report software documentation or software problems.

I think this manual...

	Strongly Agree	Agree	Disagree	Strongly Disagree
is easy to read	☐	☐	☐	☐
is easily understood	☐	☐	☐	☐
is concise & to the point	☐	☐	☐	☐
covers the subject	☐	☐	☐	☐
has enough detail	☐	☐	☐	☐
is well organized	☐	☐	☐	☐
provides easy-to-locate information	☐	☐	☐	☐
is aesthetically pleasing	☐	☐	☐	☐
has clear illustrations	☐	☐	☐	☐
has enough illustrations	☐	☐	☐	☐
has meaningful examples	☐	☐	☐	☐
has a helpful index	☐	☐	☐	☐

My other comments...

Please make any additional specific comments. (Include chapter, page, table or figure number.)

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☐ Service Eng. ☐ Operator ☐ Other _____

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_____

What revision level of system software are you using? _____

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