

# **16-BIT EXTENDED SELECTOR CHANNEL (ESELCH) PROGRAMMING MANUAL**

  
**INTERDATA®**  
A UNIT OF  
**PERKIN-ELMER DATA SYSTEMS**  
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## FOREWORD

This manual explains how the Extended Selector Channel (ESELCH) and a 16-bit processor generate an 18-bit address to access expanded memory. The ESELCH can access up to four 64KB blocks of memory for a total of 256KB of memory. It can also operate with only one 64KB block of memory. Programming instructions and three sample programs are provided for the user.

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# 16-BIT ESELCH PROGRAMMING MANUAL

## 1. INTRODUCTION

The 16-Bit Extended Selector Channel (ESELCH) operates in a 16-bit system and controls data transfers between I/O devices and memory at rates up to two megabytes per second. A maximum of 16 I/O devices can be connected to the ESELCH, but only one device at a time can transfer data.

The advantage of using an ESELCH is that other program processing can occur simultaneously with the transfer of data between the I/O device and memory. This is accomplished by allowing the ESELCH and the processor to access memory on a cycle-stealing basis. In some instances, the execution times of the program in process are affected; while in others, the effect is negligible. This depends upon the INTERDATA Processor being used and the rate at which both the ESELCH and the processor compete for memory access.

Figure 1 shows the ESELCH incorporated into the INTERDATA peripheral system.

The Appendices contain three programming examples showing use of the ESELCH.

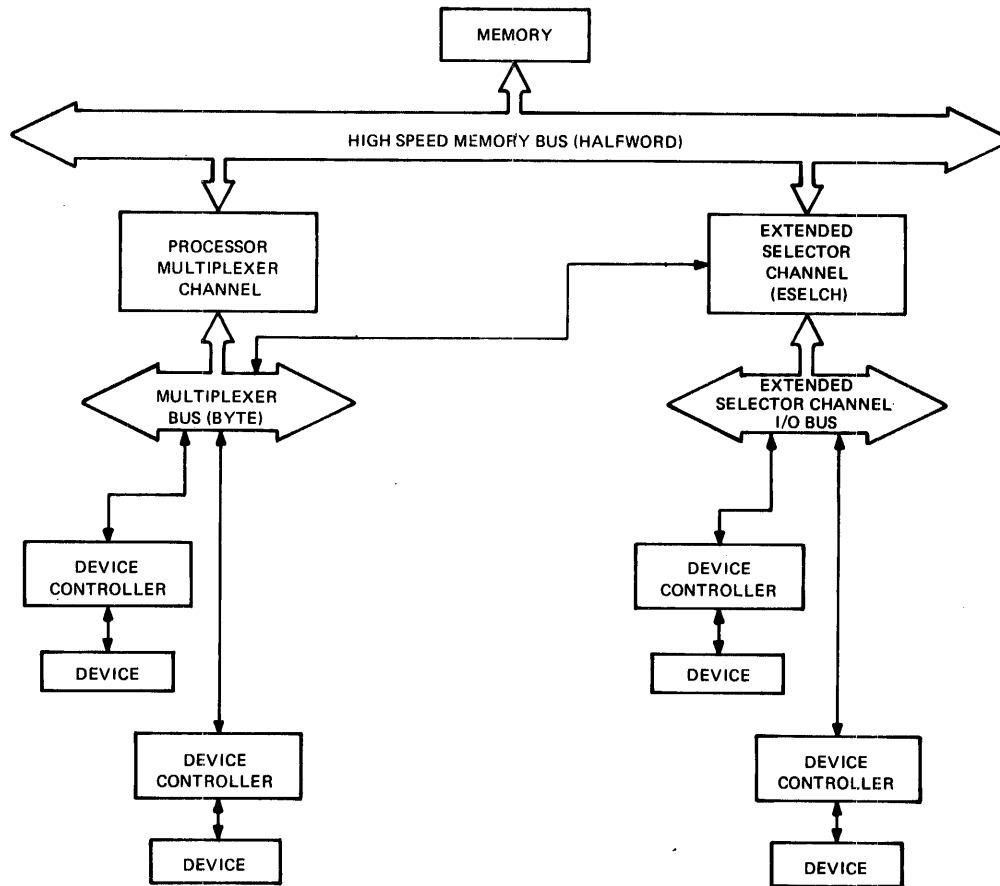


Figure 1. System Interface Block Diagram

## 2. CONFIGURATION

The Extended Selector Channel (ESELCH) and a 16-bit series processor, which can accommodate the 18-bit address required to access extended memory (e.g., 8/16E Processor), are used in a 16-bit extended memory system containing up to 256KB (Kilo Bytes) of memory. The ESELCH can be used with a 16-bit series processor as a non-extended memory system containing up to 64KB of memory. Refer to the appropriate processor maintenance manual for configuration details.

## 3. PROGRAMMING INSTRUCTIONS

A Sense Status (SS or SSR) instruction transfers the ESELCH status byte to the processor. Refer to Section 5 for status and command byte information. This instruction should not be used under interrupt control because it could cause the ESELCH to become idle and the interrupt condition to reset.

The Output Command (OC or OCR) instruction causes a command byte to be sent to the ESELCH.

The Write Data (WD or WDR) or Write Halfword (WH or WHR) instructions send the starting and final addresses to the ESELCH.

The Read Data (RD or RDR) or Read Halfword (RH or RHR) instructions obtain the last processor memory location either written into or read from memory.

## 4. MEMORY

A 16-bit system can have an extended memory containing up to 256KB of memory or a non-extended memory containing up to 64KB of memory.

### 4.1 Extended Memory System

An extended memory system is composed of one to four memory segments. Each segment contains 64KB of memory with the exception of the last segment which may contain only 32KB of memory.

The extended memory requires an 18-bit address. The Extended Selector Channel generates the 18-bit address in two parts. The two most significant bits of the address (XMA140 and XMA150) which define a particular memory segment are specified in the Output Command instruction. The remaining 16-bits are specified in the Write (byte or halfword) instruction and address memory within the segment.

An extended memory system requires a processor which can accommodate the 18-bit address required to access the extended memory; however, the processor may address memory differently than the Extended Selector Channel (ESELCH). Refer to the appropriate processor maintenance manual for details (e.g., 8/16E Processor Maintenance Manual, Publication Number 29-618).

## 4.2 Non-Extended Memory System


The Extended Selector Channel (ESELCH) can be used with a non-extended memory by maintaining the value of the two most significant bits (XMA140 and XMA150) of the 18-bit address at zero. In this condition, the ESELCH operates identically to the 16-bit Selector Channel (SELCH).

## 5. STATUS AND COMMAND BYTE INFORMATION

Table 1 shows ESELCH Status and Command Byte Data.

TABLE 1. ESELCH STATUS AND COMMAND BYTE

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE					BSY			
COMMAND BYTE			READ	GO	STOP		XMA 140	XMA 150


  
64KB Address  
Segment

**BSY** This bit is set when the ESELCH is in the process of transferring data. It is reset when the ESELCH terminates or is stopped by an Output Command.

**READ** This command changes the mode of the ESELCH from Write to Read. The data is then transmitted from the active device on the private ESELCH I/O Bus and written into memory. When a data transmission has been completed, the ESELCH is placed in the Write mode. Each time a Read operation is required, an Output Command must be issued with the READ and GO bits set.

**GO** This command initiates a data transmission and can be issued at the same time the Read/Write mode is established.

**STOP** This command halts any data transmission in process and initializes the ESELCH for starting a new operation. It is given when the ESELCH terminates.

**XMA140** These bits are the two most significant bits of the  
**XMA150** 18-bit address. They define the memory segment where the Write or Read operation is to occur. See Table 2.

TABLE 2. XMA 140:150 - MEMORY SEGMENT AND ADDRESS

XMA		MEMORY SEGMENT	MEMORY ADDRESS
140	150		
0	0	0	X`00000' to X`0FFFF'
0	1	1	X`10000' to X`1FFFF'
1	0	2	X`20000' to X`2FFFF'
1	1	3	X`30000' to X`3FFFF'

XMA140 and XMA150 must be specified in the same command byte that commands the ESELCH to perform a Write or Read and GO operation.

XMA140 and XMA150 must be reset when a STOP command (Bit 4 set) is issued to the ESELCH.

## 6. PROGRAMMING SEQUENCES

Programming a device on the ESELCH consists of setting up the ESELCH, setting up the device, and sending a GO command to the ESELCH as explained in Section 5. Setting up or initiating a device on the ESELCH is device dependent and the user should refer to the appropriate device programming manual for specifics. If the ESELCH is Busy, I/O instructions should not be issued, but the STOP command can be issued. The ESELCH has its own unique device number and is affected by an Output Command, if the correct device address is used. If an I/O instruction is directed to a device on the private ESELCH I/O Bus while the ESELCH is Busy, a False SYNC is indicated by the Condition Code (CVGL = 0100) and the command is ignored.

The ESELCH is idle (not Busy) after Initialize (see Section 7.6), after a STOP command is issued to the ESELCH, or when transfers are complete. Prior to starting an I/O operation with the ESELCH or any device on the private ESELCH I/O Bus, the program must do one of the following:

1. Wait until the ESELCH completes an I/O transfer (Busy resets); then issue a STOP command to the ESELCH.
2. Issue a STOP command to the ESELCH.



The ESELCH operates within one 64KB memory segment at a time. Programming the ESELCH to access memory requires defining the memory segment through the Output Command. Writing to the device or reading from the device via the ESELCH can occur only within the defined memory segment; therefore, transmitting the start and final addresses to the ESELCH or reading the terminating address from the ESELCH must be done relative to the defined memory segment. The memory segment bits cannot be read out of the ESELCH.

To perform a Read or Write operation on a device using an ESELCH, the following steps are required:

1. Wait for the ESELCH to become not Busy or issue a STOP Command. The STOP Command stops any transfer in progress and should be used wisely.
2. Send the starting and ending addresses to the ESELCH.
3. Set up the device on the ESELCH by issuing the appropriate I/O commands.
4. Send an Output Command to the ESELCH with the GO bit set. The READ bit should be set for a Read operation and reset for a Write operation. In this command byte, the two most significant bits (XMA140 and XMA150) must be specified to define the memory segment of the starting and terminating addresses.

#### NOTE

No I/O instruction can be issued to any other device during the execution of the program instructions in Steps 2 through 4. When the GO command is issued, the ESELCH does the following:

1. Transfers data to the last device addressed by the processor (i.e., by the user program or by the microprogram) if that device is connected to the ESELCH.

2. Because the ESELCH does not react to false sync if no device attached to the ESELCH has been addressed by the processor since initialization, the ESELCH hangs up attempting to communicate with a non-existent device. See Section 7.6. For this reason, the program instructions in Steps 2 through 4 must be executed with processor I/O interrupts disabled. Otherwise, it is possible to detect an external interrupt and the interrupt driver in the user program (or the microprogram in the case of an immediate interrupt) can address any other device. Also, the single cycle mode of the display may not be used since the microcode addresses the display panel after each instruction execution.

#### Transmission of Starting and Final Addresses

A STOP Output Command is issued prior to starting any operation on the ESELCH. Four successive bytes are required to specify the start and final addresses. The Write Data (WD or WDR) or Write Halfword (WH or WHR) instructions send the start and final addresses to the ESELCH Controller. Figure 2 illustrates the meaning of four bytes used for addressing.

	0 ← HIGH → 7	8 ← LOW → 15
START ADDRESS	1	2
FINAL ADDRESS	3	4

1. START ADDRESS HIGH (BITS 0-7)
2. START ADDRESS LOW (BITS 8-15)
3. FINAL ADDRESS HIGH (BITS 0-7)
4. FINAL ADDRESS LOW (BITS 8-15)

Figure 2. Memory of Data Bytes for Start and Final Addresses

For example, if the start address is X`0ABC` and the ending address is X`CFAB`, the following addressing sequences are correct:

1. WD (or WDR) SELCH, START (0A)  
 WD (or WDR) SELCH, START+1 (BC)  
 WD (or WDR) SELCH, END (CF)  
 WD (or WDR) SELCH, END+1 (AB)
2. WH (or WHR) SELCH, START (0ABC)  
 WH (or WHR) SELCH, END (CFAB)

### 7. PROGRAMMING NOTES

The ESELCH has a 16-bit incrementing Address Register (AR) and a 16-bit Final Address Register (FAR). XMA14 and XMA15 are not part of the AR or FAR. The user program loads the starting memory address into the incrementing Address Register (AR) and the final memory address into the Final Address Register (FAR). Transfer is completed when the incrementing Address Register (AR) matches the Final Address Register (FAR). The address limits are expressed inclusively; transfers begin and end on the addresses placed in the start and final address registers.

Memories in INTERDATA processors are addressed on halfword boundaries; that is, each time memory is accessed, two bytes (a halfword) are obtained. Therefore, Bit 15 of the 16-bit incrementing Address Register (AR) is used to determine the bytes desired. See Figure 3.

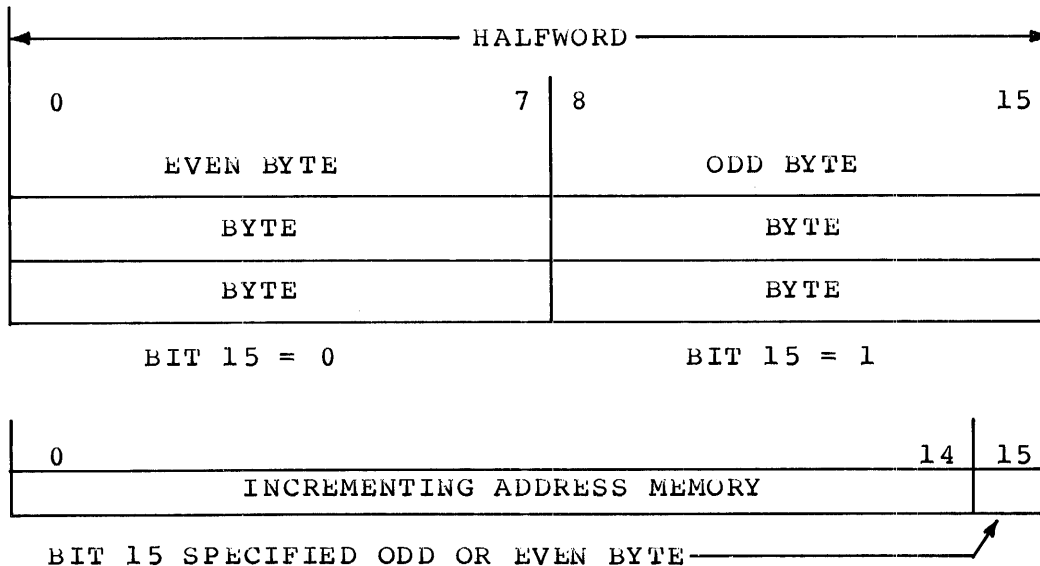


Figure 3. Memory Addressing

Each time the ESELCH accesses memory, two bytes (a halfword) are transmitted. It is mandatory for data transfers to begin on a halfword boundary, but it is not mandatory for them to end on a halfword boundary. The following results if data transfers are ended on byte boundaries:

1. Write mode (Memory to Device) - End on byte boundary (Bit 15 = 0) with no effect.
2. Read mode (Device to Memory) - End on byte boundary (Bit 15 = 0). The previous content of the last odd byte in memory is written into the current odd byte. See Figure 4.

	0	7	8	15
NEXT TO LAST HALFWORD	EVEN BYTE*		ODD BYTE**	
LAST HALFWORD	BYTE*		BYTE**	

\* LAST BYTE SPECIFIED  
 \*\*BOTH BYTES HAVE SAME VALUE

Figure 4. Memory Configuration End on Byte Boundary

### 7.1 Termination

Data transmission between the ESELCH and the device presently connected to it is halted when any of the following conditions occur:

1. The start incrementing address matches the final address. This denotes normal termination.
2. The start incrementing address changes from all ones to all zeros (maximum count). In this case, a match has not occurred and is considered an abnormal termination.
3. Bit 5, 6, or 7 is set in the status byte of the device presently connected to the ESELCH. This may be an abnormal termination, depending on the application.
4. A STOP command is sent to the ESELCH by a user program.
5. The processor is initialized or a power failure is detected. Memory cycle in process is completed.

The termination condition is determined in one of two ways: by a status scan or by the interrupt method. The methods are described in the following paragraphs. A STOP Output Command is issued to the ESELCH following its termination.

## 7.2 Status Scan

The status of the ESELCH may be examined by issuing a Sense Status (SS or SSR) instruction. The BUSY bit (Bit 4) is set while transmission is in progress and reset when transmission is terminated. One method of testing for termination is to continually or periodically test the BUSY bit of the ESELCH. The change from set to reset indicates the termination of a data transfer. In the status scan method of programming, it is possible for the BUSY bit to change from set to reset during a Sense Status instruction without returning the ESELCH to idle. To guarantee the idle mode after BUSY resets on a Sense Status instruction, a STOP Command must be sent to the ESELCH.

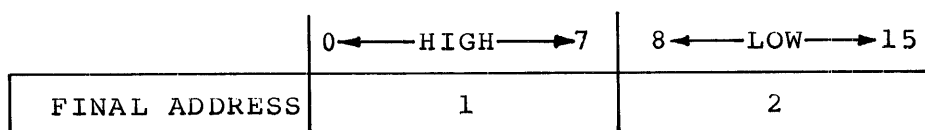
## 7.3 Interrupt Method

When data transmission is initiated on the ESELCH, the interrupt is effectively enabled. If external device interrupts are permitted (Bit 1 of the PSW set) to enter the processor at termination, the processor is interrupted. The interrupt handler address must be stored in the proper dedicated memory location. The Acknowledge Interrupt (ACK or ACKR) instruction causes the device number of the ESELCH (normally X`F0') and the status of the peripheral device to be brought into the processor and it also clears the interrupt condition. The BUSY bit is treated in the manner previously described for the Status Scan.

## 7.4 Reading the Final Address

The last processor memory location either written into or read by the ESELCH (incrementing Address Register) may be obtained by executing a pair of Read Data (RD or RDR) instructions or a Read Halfword (RH or RHR) instruction. This information permits a user program to verify a successful data transmission or determine the address termination occurred. If the ending address returned by the ESELCH is not equal to the ending address written to the ESELCH, then the ESELCH terminated early with all of the specified memory not written or read. See Section 7.1.

Figure 5 shows the order in which data is read into the processor.



1. FINAL ADDRESS HIGH (BITS 0-7)
2. FINAL ADDRESS LOW (BITS 8-15)

Figure 5. Execution Order for Read Data Instructions

## 7.5 Device Number

The ESELCH is normally assigned device number X`F0` but may easily be changed on the ESELCH Device Controller board. Refer to the ESELCH Installation and Maintenance Manual, Publication Number 29-619, for details.

## 7.6 Initialization

Whenever the Initialize switch (INT) on the display panel is depressed, or a STOP command is issued, the following action occurs:

1. Any data transmission in process is halted and the Stop mode is affected.
2. The ESELCH is placed in the Write mode.
3. The ESELCH is made idle.
4. The ESELCH interrupt is reset.

## 8. SAMPLE PROGRAMS

The Appendices contain three sample programs for demonstrating the use of the 16-Bit ESELCH. The first two programs involve the use of the INTERDATA 1600 BPI and 800 BPI Read-After-Write Magnetic Tape Systems. The third program involves the INTERDATA 2.5 and 10-Megabyte Removable Cartridge Disc. For further information pertaining to programming the Magnetic Tape System or Cartridge Disc, refer to the following INTERDATA manuals:

1. Magnetic Tape Programming Manual, Publication Number 29-530.
2. 2.5 and 10 Megabyte Removable Cartridge Disc Programming Manual, Publication Number 29-454.

Descriptions of the sample programs are given below.

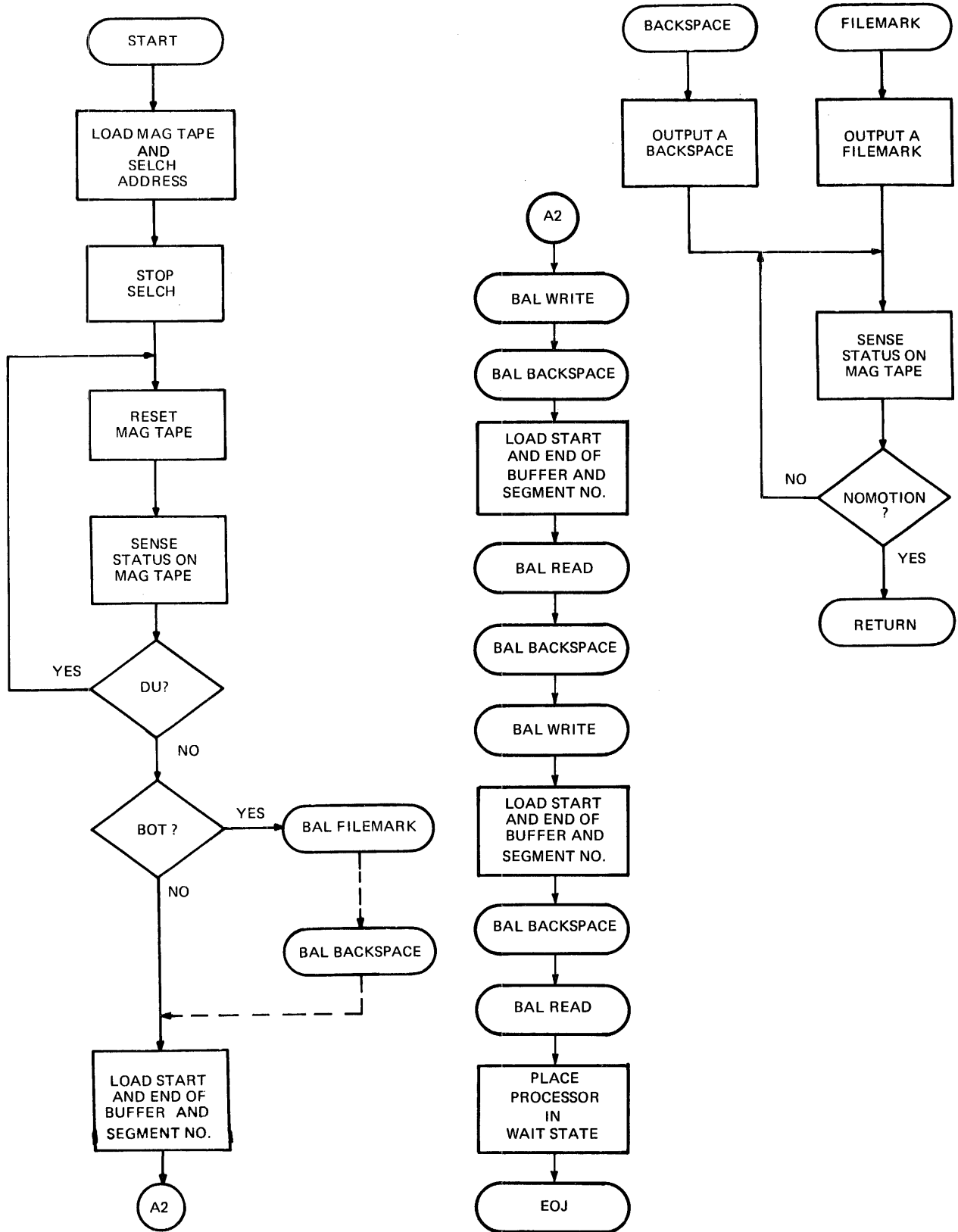
### 8.1 Magnetic Tape System with ESELCH

The first program uses the ESELCH and Sense Status Loops to read and write on magnetic tape. The second program uses the ESELCH and External Interrupts to read and write on magnetic tape.

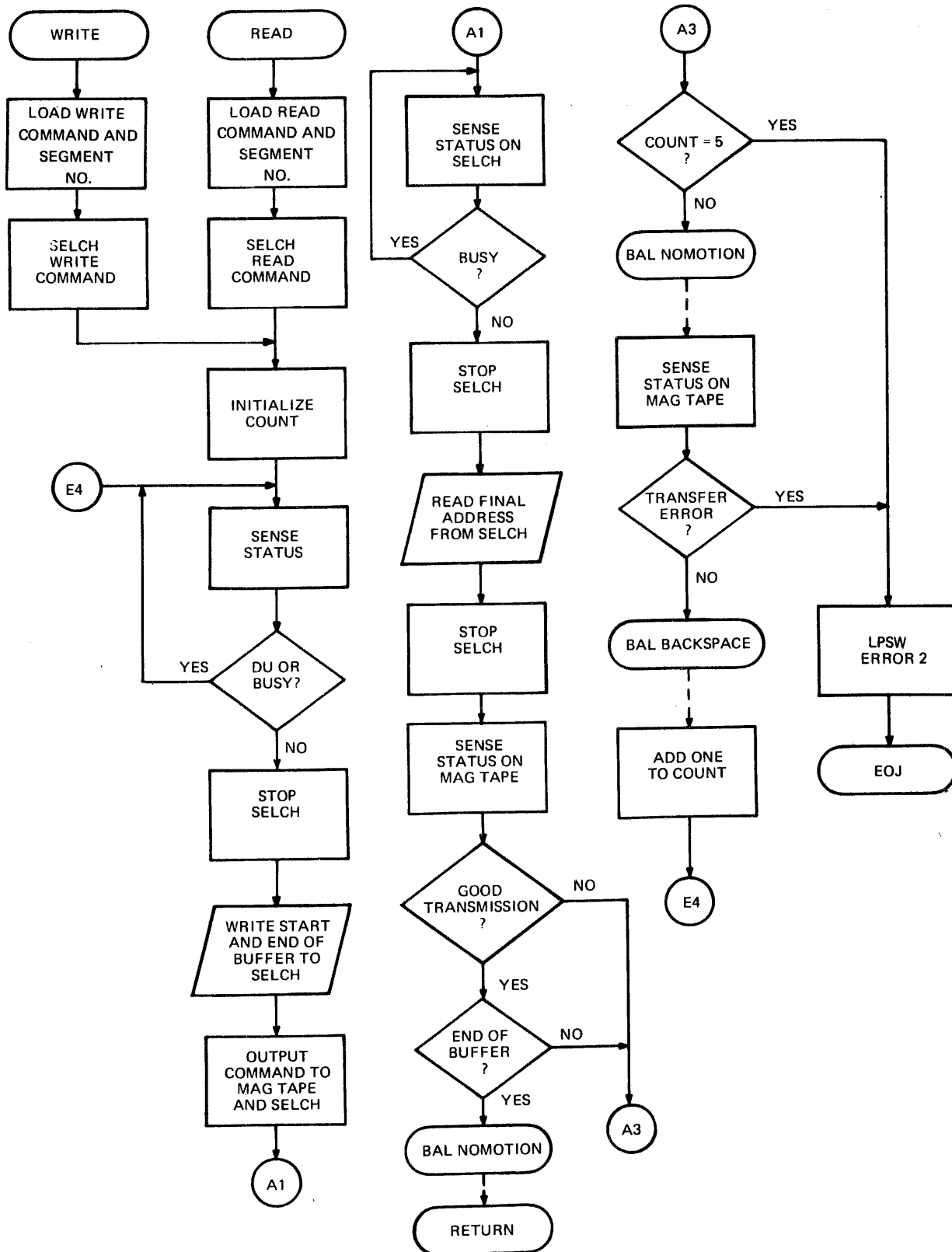
### 8.2 Cartridge Disc with ESELCH

The first part of this program uses the ESELCH and Sense Status Loops to read and write on the disc. The second part of the program uses the ESELCH and External Interrupts to read and write on the disc.

APPENDIX 1  
 16 BIT EXTENDED SELCH (MAG TAPE WITH SENSE STATUS)



APPENDIX 1 (Continued)





PROG= ESELMG ASSEMBLED BY CAL 03-066R04-01 (16-BIT)

		1	SCRAT			MAG00020
		2	WIDTH 120			MAG00030
		3	CROSS			MAG00040
		4	TARGT 16			MAG00050
		5	*			MAG00060
		6	* THIS PROGRAM USES THE 16 BIT EXT SELCH & SENSE STATUS			MAG00070
		7	* LOOPS TO:			MAG00080
		8	* (1) WRITE A BUFFER FROM MEMORY SEGMENT ZERO (0)			MAG00090
		9	* TO MAG TAPE.			MAG00100
		10	* (2) READ FROM MAG TAPE TO A BUFFER IN MEMORY			MAG00110
		11	* SEGMENT ONE (1).			MAG00120
		12	* (3) WRITE THIS BUFFER TO MAG TAPE.			MAG00130
		13	* (4) READ THE DATA FROM MAG TAPE BACK TO THE			MAG00140
		14	* ORIGINAL BUFFER IN SEGMENT ZERO (0).			MAG00150
		15	*			MAG00160
		16	* 16-BIT PROCESSORS			MAG00170
		17	*			MAG00180
		18	* REGISTER ASSIGNMENTS:			MAG00190
		19	*			MAG00200
	0000 0001	20	R1 EQU 1	START OF BUFFER REGISTER		MAG00210
	0000 0001	21	DU EQU 1	DEVICE UNAVAILABLE		MAG00220
	0000 0002	22	R2 EQU 2	END OF BUFFER REGISTER		MAG00230
	0000 0003	23	R3 EQU 3	DEVICE ADDRESS REGISTER		MAG00240
	0000 0004	24	R4 EQU 4	STATUS		MAG00250
	0000 0005	25	R5 EQU 5	RETURN REGISTER		MAG00260
	0000 0006	26	R6 EQU 6	MOST SIG 2 BITS OF MEMORY		MAG00270
	0000 0007	27	R7 EQU 7	COUNTER		MAG00280
	0000 0008	28	BSY EQU 8	BUSY		MAG00290
	0000 0008	29	R8 EQU 8	COMMAND BYTE STORE		MAG00300
	0000 0009	30	R9 EQU 9	SELCH ADDRESS REGISTER		MAG00310
	0000 000A	31	R10 EQU 10	SELCH COMMAND HOLD REGISTER		MAG00320
	0000 000B	32	R11 EQU 11	WORK REGISTER		MAG00330
	0000 000C	33	R12 EQU 12	RETURN REGISTER		MAG00340
	0000 0010	34	TEST EQU X'10'	TEST=NOMOTION BIT		MAG00350
	0000 0020	35	BOT EQU X'20'	TEST FOR BOT		MAG00360
	0000 00C0	36	TERM EQU X'C0'	TERMINATION STATUS=X'C0'		MAG00370
0000R	4830 013AR	37	LH R3,MTADR	LOAD MAG TAPE ADDRESS		MAG00380
0004R	4890 0138R	38	LH R9,SELCH	LOAD SELCH ADDRESS		MAG00390
0008R	DE90 013ER	39	OC R9,STOP	STOP SELCH		MAG00400
000CR	DE30 013FR	40	DUTEST OC R3,RESET	OUTPUT RESET		MAG00410
0010R	9D34	41	SSR R3,R4	SENSE STATUS ON MAG TAPE		MAG00420
0012R	4210 000CR	42	BTC DU,DUTEST	IS MAG TAPE UNAVAILABLE		MAG00430
0016R	C340 0020	43	THI R4,BOT	TEST FOR BOT		MAG00440
001AR	2335	44	BZS WRT	BRANCH TO WRITE		MAG00450
001CR	4150 0068R	45	BAL R5,FLMK	FILEMARK ROUTINE		MAG00460
0020R	4150 0062R	46	BAL R5,BAKSP	BACKSPACE TAPE ROUTINE		MAG00470
0024R	C810 00F8R	47	WRT LHI R1,BUFSRT	LOAD START OF BUFFER		MAG00480
0028R	C820 012FR	48	LHI R2,BUFEND	LOAD END OF BUFFER		MAG00490
002CR	0766	49	XHR R6,R6	LOAD 2 MOST SIG BITS OF MEM (0)		MAG00500
002ER	41C0 0076R	50	BAL R12,WRITE	WRITE TO DEVICE		MAG00510
		51	*			MAG00520
0032R	4150 0062R	52	BAL R5,BAKSP	BACK SPACE		MAG00530
0036R	0711	53	XHR R1,R1	LOAD START OF BUFFER (0)		MAG00540
0038R	C820 0037	54	LHI R2,BUFEND-BUFSRT	LOAD END OF BUFFER		MAG00550

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APPENDIX I (Continued)

003CR	D360	0145R	55	LB	R6, MEMSEG	LOAD 2 MOST SIG BITS OF MEM	MAG00560
0040R	41C0	008AR	56	BAL	R12, READ	READ FOR DEVICE	MAG00570
			57	*			MAG00580
0044R	4150	0062R	58	BAL	R5, BAKSP	BACKSPACE	MAG00590
0048R	41C0	0076R	59	BAL	R12, WRITE	WRITE TO DEVICE	MAG00600
			60	*			MAG00610
004CR	C810	00F8R	61	LHI	R1, BUFRT	LOAD START OF BUFFER	MAG00620
0050R	C820	012FR	62	LHI	R2, BUFEND	LOAD END OF BUFFER	MAG00630
0054R	0766		63	XHR	R6, R6	LOAD 2 MOST SIG BITS OF MEM (0)	MAG00640
0056R	4150	0062R	64	BAL	R5, BAKSP	BACKSPACE	MAG00650
005AR	41C0	008AR	65	BAL	R12, READ	READ FROM DEVICE	MAG00660
			66	*			MAG00670
005ER	C200	0134R	67	END1	LPSW END		MAG00680
			68	*	*****		MAG00690
			69	*	SUBROUTINE: BAKSP		MAG00700
			70	*	THIS SUBROUTINE BACKSPACES ONE RECORD.		MAG00710
			71	*	SEE CALLING SEQUENCE BELOW.		MAG00720
			72	*			MAG00730
			73	*	SUBROUTINE: FLMK		MAG00740
			74	*	THIS SUBROUTINE WRITES A FILEMARK		MAG00750
			75	*	SEE CALLING SEQUENCE BELOW.		MAG00760
			76	*			MAG00770
			77	*			MAG00780
			78	*	*****		MAG00790
			79	*			MAG00800
			80	*	SUBROUTINE: NOMOT		MAG00810
			81	*	THIS SUBROUTINE WAITS FOR THE MAG TAPE TO		MAG00820
			82	*	STOP MOVING.		MAG00830
			83	*			MAG00840
			84	*	CALLING SEQUENCE: BAL R5, BAKSP		MAG00850
			85	*	----- BAL R5, FLMK		MAG00860
			86	*	BAL R5, NOMOT		MAG00870
			87	*	R3=DEVICE ADDRESS REGISTER		MAG00880
			88	*	R5=RETURN REGISTER		MAG00890
			89	*			MAG00900
			90	*	WORK REGISTERS:		MAG00910
			91	*	-----		MAG00920
			92	*	R4=DEVICE STATUS REGISTER		MAG00930
			93	*			MAG00940
			94	*	*****		MAG00950
			95	*			MAG00960
0062R	DE30	0141R	96	BAKSP	OC R3, BKSP	OUTPUT BACKSPACE	MAG00970
0066R	2303		97		BS NOMOT	BRANCH TO NOMOTION	MAG00980
0068R	DE30	0140R	98	FLMK	OC R3, FILMRK	OUTPUT FILEMARK	MAG00990
006CR	9D34		99	NOMOT	SSR R3, R4	SENSE STATUS ON MAG TAPE	MAG01000
006ER	C340	0010	100		THI R4, TEST	TEST FOR NO MOTION	MAG01010
0072R	2233		101		BZS NOMOT	SENSE AGAIN	MAG01020
0074R	0305		102		BR R5	RETURN	MAG01030
			103	*	*****		MAG01040
			104	*	SUBROUTINE: WRITE		MAG01050
			105	*	THIS SUBROUTINE WRITES ONE BLOCK OF DATA TO THE		MAG01060
			106	*	MAG TAPE.		MAG01070
			107	*	SEE CALLING SEQUENCE BELOW		MAG01080
			108	*	SUBROUTINE READ		MAG01090
			109	*	THIS SUBROUTINE READS A BLOCK OF DATA FROM THE		MAG01100
			110	*	MAG TAPE.		MAG01110

APPENDIX 1 (Continued)

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111 *
112 * CALLING SEQUENCE: BAL R12,WRITE
113 * ----- BAL R12,READ
114 * R1=START OF BUFFER
115 * R2=END OF BUFFER
116 * R3=DEVICE ADDRESS REGISTER
117 * R9=SELCH ADDRESS REGISTER
118 * R12=RETURN REGISTER
119 *
120 * WORK REGISTERS:
121 * -----
122 * R4=STATUS REGISTER
123 * R5=NOMOTION RETURN REGISTER
124 * R7=RETRY COUNT
125 * R8=COMMAND REGISTER
126 * R10=SELCH COMMAND REGISTER
127 * R11=WORK REGISTER
128 * *****
0076R D380 0143R 129 WRITE LB R8,WRTCMD LOAD WRITE COMMAND
007AR D3A0 013DR 130 LB R10,SELWRT LOAD SELCH WRITE
007ER C4A0 00FC 131 NHI R10,X'FC' BIT 0-5 OF COMMAND
0082R C460 0003 132 NHI R6,X'03' BITS 6-7 OF COMMAND
0086R 06A6 133 OHR R10,R6 COMPOSE SELCH COMMAND
0088R 230A 134 BS RETRY BRANCH TO RETRY
008AR D380 0144R 135 READ LB R8,RDCMD LOAD READ COMMAND
008ER D3A0 013CR 136 LB R10,SELRD LOAD SELCH READ
0092R C4A0 00FC 137 NHI R10,X'FC' BITS 0-5 OF COMMAND
0096R C460 0003 138 NHI R6,X'03' BITS 6-7 OF COMMAND
009AR 06A6 139 OHR R10,R6 COMPOSE SELCH COMMAND
009CR 0777 140 RETRY XHR R7,R7 ZERO OUT COUNT
009ER 9D34 141 SENSE1 SSR R3,R4 SENSE STATUS ON MAG TAPE
00A0R 2091 142 BTBS DU+BSY,SENSE1 TEST FOR BUSY+DEVICE UNAVAILABLE
00A2R DE90 013ER 143 OC R9,STOP STOP SELCH
00A6R 9891 144 WHR R9,R1 WRITE START OF BUFFER TO SELCH
00A8R 9892 145 WHR R9,R2 WRITE END OF BUFFER TO SELCH
00AAR 9E38 146 OCR R3,R8 OUTPUT COMMAND TO MT
00ACR 9E9A 147 OCR R9,R10 OUTPUT COMMAND TO SELCH
00AER 9D94 148 SSR R9,R4 SENSE STATUS ON SELCH
00BOR 2081 149 BTBS BSY,1 TEST FOR BUSY
00B2R DE90 013ER 150 OC R9,STOP STOP THE SELCH
00B6R 999B 151 RHR R9,R11 READ FINAL ADR. FROM SELCH
00BR R DE90 013ER 152 OC R9,STOP STOP THE SELCH
00BCR 9D34 153 SSR R3,R4 SENSE STATUS ON THE MAG TAPE
00BER C340 00C0 154 THI R4,TERM TEST FOR GOOD TERMINATION
00C2R 4230 00D2R 155 BNZ ERROR BRANCH TO TRY AGAIN
00C6R 05B2 156 CLHR R11,R2 TEST END OF BUFFER
00C8R 4230 00D2R 157 BNE ERROR
00CCR 4150 006CR 158 BAL R5,NOMOT WAIT FOR TAPE TO STOP
00D0R 030C 159 BR R12 RETURN
160 *
161 * THIS ROUTINE ABORTS THE PROGRAM ON NON-RECOVERABLE STATUS ERRORS
162 * AND TRIES 5 TIMES TO RECOVER ON DATA TRANSFER STATUS ERRORS
163 * BEFORE TERMINATING.
164 *
00D2R C570 0005 165 ERROR CLHI R7,5 TEST FOR 5 TRIES
00D6R 4330 00F2R 166 BE ERROR1 BRANCH TO ERROR1

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MAG01120  
MAG01130  
MAG01140  
MAG01150  
MAG01160  
MAG01170  
MAG01180  
MAG01190  
MAG01200  
MAG01210  
MAG01220  
MAG01230  
MAG01240  
MAG01250  
MAG01260  
MAG01270  
MAG01280  
MAG01290  
MAG01300  
MAG01310  
MAG01320  
MAG01330  
MAG01340  
MAG01350  
MAG01360  
MAG01370  
MAG01380  
MAG01390  
MAG01400  
MAG01410  
MAG01420  
MAG01430  
MAG01440  
MAG01450  
MAG01460  
MAG01470  
MAG01480  
MAG01490  
MAG01500  
MAG01510  
MAG01520  
MAG01530  
MAG01540  
MAG01550  
MAG01560  
MAG01570  
MAG01580  
MAG01590  
MAG01600  
MAG01610  
MAG01620  
MAG01630  
MAG01640  
MAG01650  
MAG01660  
MAG01670

APPENDIX 1 (Continued)

00DAR	4150	006CR	167	BAL	R5,NOMOT	STOP MOTION OF TAPE	MAG01680
00DER	9034		168	SSR	R3,R4	SENSE STATUS ON MAG TAPE	MAG01690
00EOR	C340	00C0	169	THI	R4,TERM	TEST FOR GOOD TERMINATION	MAG01700
00E4R	4330	00F2R	170	BZ	ERROR1	BRANCH TO ERROR1	MAG01710
00E8R	4150	0062R	171	BAL	R5,BAKSP	BACKSPACE ROUTINE	MAG01720
00ECR	2671		172	AIS	R7,1	ADD ONE TO COUNT	MAG01730
00EER	4300	009ER	173	B	SENSE1	BRANCH TO SENSE1	MAG01740
			174	*			MAG01750
00F2R	C200	0130R	175	ERROR1	LPSW ERROR2		MAG01760
			176	*			MAG01770
			177	*	BUFFER		MAG01780
			178	*			MAG01790
00F8R			179		ALIGN 4	ALIGN START OF BUFFER	MAG01800
			180	*		ON HALFWORD BOUNDARY	MAG01810
00F8R	0123		181	BUFSRT	DC X'0123',X'4567'		MAG01820
00FAR	4567						
00FCR	89AB		182	DC	X'89AB',X'CDEF'		MAG01830
00FER	CDEF						
0100R	0123		183	DC	X'0123',X'4567'		MAG01840
0102R	4567						
0104R	89AB		184	DC	X'89AB',X'CDEF'		MAG01850
0106R	CDEF						
0108R	0123		185	DC	X'0123',X'4567'		MAG01860
010AR	4567						
010CR	89AB		186	DC	X'89AB',X'CDEF'		MAG01870
010ER	CDEF						
0110R	0123		187	DC	X'0123',X'4567'		MAG01880
0112R	4567						
0114R	89AB		188	DC	X'89AB',X'CDEF'		MAG01890
0116R	CDEF						
0118R	0123		189	DC	X'0123',X'4567'		MAG01900
011AR	4567						
011CR	89AB		190	DC	X'89AB',X'CDEF'		MAG01910
011ER	CDEF						
0120R	0123		191	DC	X'0123',X'4567'		MAG01920
0122R	4567						
0124R	89AB		192	DC	X'89AB',X'CDEF'		MAG01930
0126R	CDEF						
0128R	0123		193	DC	X'0123',X'4567'		MAG01940
012AR	4567						
012CR	89AB		194	DC	X'89AB',X'CDEF'		MAG01950
012ER	CDEF						
	0000	012FR	195	BUFEND	EQU *-1		MAG01960
0130R	8000		196	ERROR2	DC X'8000',A(ERROR1)		MAG01970
0132R	00F2R						
0134R	8000		197	END	DC X'8000'		MAG01980
0136R	005ER		198	DC	A(END1)		MAG01990
0138R	00F0		199	SELCH	DC X'F0'	SELECTOR CHANNEL ADDRESS	MAG02000
013AR	0085		200	MTADR	DC X'85'	MAG TAPE ADDRESS	MAG02010
013CR	30		201	SELRD	DB X'30'	SELCH READ COMMAND	MAG02020
013DR	10		202	SELWRT	DB X'10'	SELCH WRITE COMMAND	MAG02030
013ER	08		203	STOP	DB X'08'	SELCH STOP COMMAND	MAG02040
013FR	E0		204	RESET	DB X'E0'	RESET COMMAND	MAG02050
0140R	30		205	FILMRK	DB X'30'	FILEMARK COMMAND	MAG02060
0141R	11		206	BKSP	DB X'11'	BACKSPACE COMMAND	MAG02070
0142R	38		207	REWIND	DB X'38'	REWIND COMMAND	MAG02080

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A1-7

16 BIT EXTENDED SELCH (MAG TAPE WITH SENSE STATUS)

PAGE 5

0143R	22	208	WRTCMD	DB	X'22'	WRITE COMMAND FOR MAG TAPE	MAG02090
0144R	21	209	RDCMD	DB	X'21'	READ COMMAND FOR MAG TAPE	MAG02100
0145R	01	210	MEMSEG	DB	X'01'	MEMORY SEGMENT 1	MAG02110
0146R		211		END			MAG02120

APPENDIX 1 (Continued)

NO ERRORS 0 SQUEZ PASSES

CAL 04-01

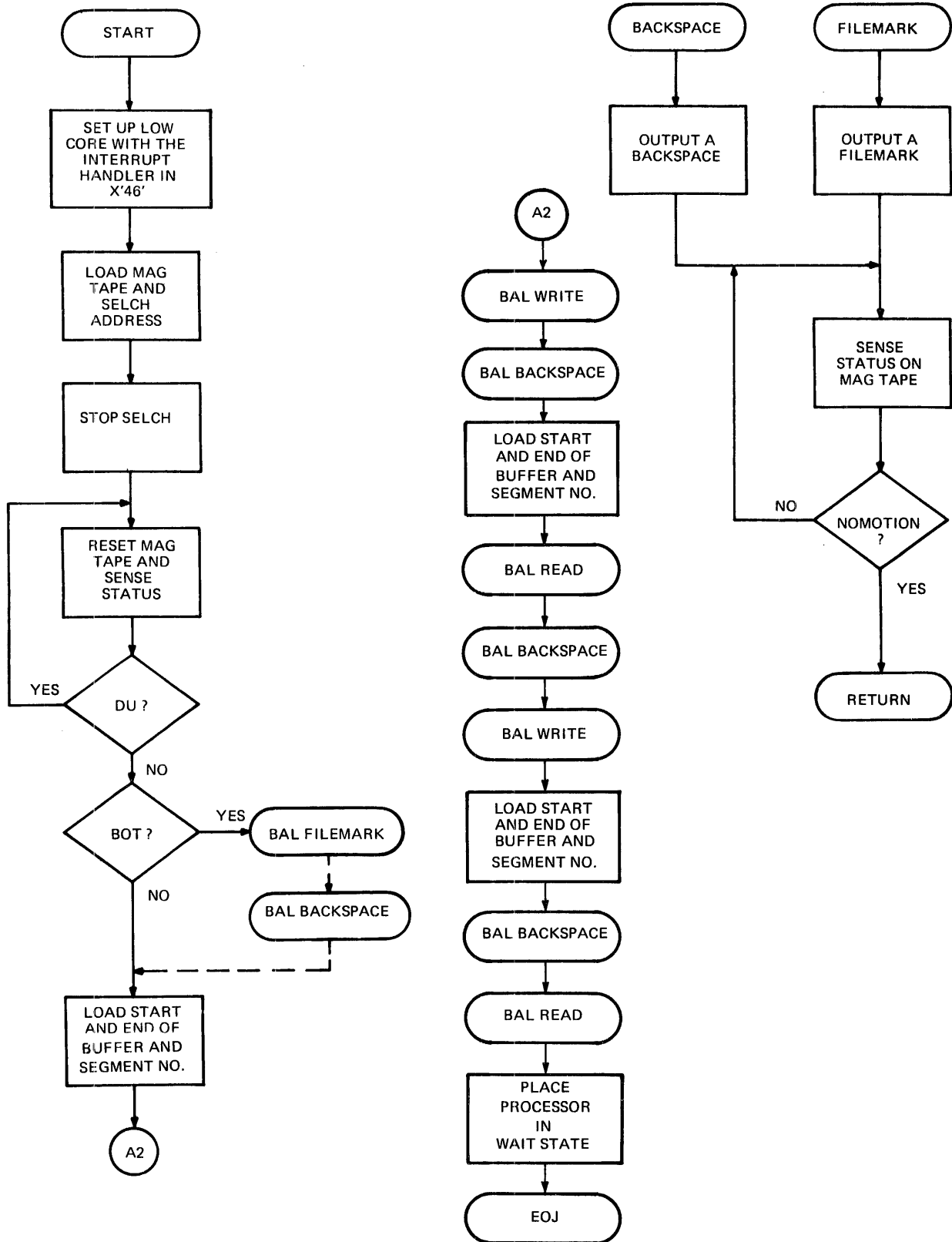
ABSTOP	0000																				
ADC	0002																				
BAKSP	0062R	46	52	58	64	171															
BKSP	0141R	96																			
BOT	0020	43																			
BSY	0008	142	149																		
BUFEND	012FR	48	54	62																	
BUFSRT	00F8R	47	54	61																	
DJ	0001	42	142																		
DUTEST	000CR	42																			
END	0134R	67																			
END1	005ER	198																			
ERROR	00D2R	155	157																		
ERROR1	00F2R	166	170	196																	
ERROR2	0130R	175																			
FILMRK	0140R	98																			
FLMK	0068R	45																			
IMPTOP	0146R																				
LADC	0001																				
MEMSEG	0145R	55																			
MTADR	013AR	37																			
NOMOT	006CR	97	101	158	167																
PURETOP	0000R																				
R1	0001	47	53	53	61	144															
R10	000A	130	131	133	136	137	139	147													
R11	000B	151	156																		
R12	000C	50	56	59	65	159															
R2	0002	48	54	62	145	156															
R3	0003	37	40	41	96	98	99	141	146	153	153	168	169								
R4	0004	41	43	99	100	141	148	153	154	168	169										
R5	0005	45	46	52	58	64	102	158	167	171											
R6	0006	49	49	55	63	63	132	133	138	139											
R7	0007	140	140	165	172																
R8	0008	129	135	146																	
R9	0009	38	39	143	144	145	147	148	150	151	152										
RDCMD	0144R	135																			
READ	008AR	56	65																		
RESET	013FR	40																			
RETRY	009CR	134																			
REWIND	0142R																				
SELCH	0138R	38																			
SELRD	013CR	136																			
SELWRT	013DR	130																			
SENSE1	009ER	142	173																		
STOP	013ER	39	143	150	152																
TERM	00C0	154	169																		
TEST	0010	100																			
WRITE	0076R	50	59																		
WRT	0024R	44																			
WRTCMD	0143R	129																			

APPENDIX 1 (Continued)

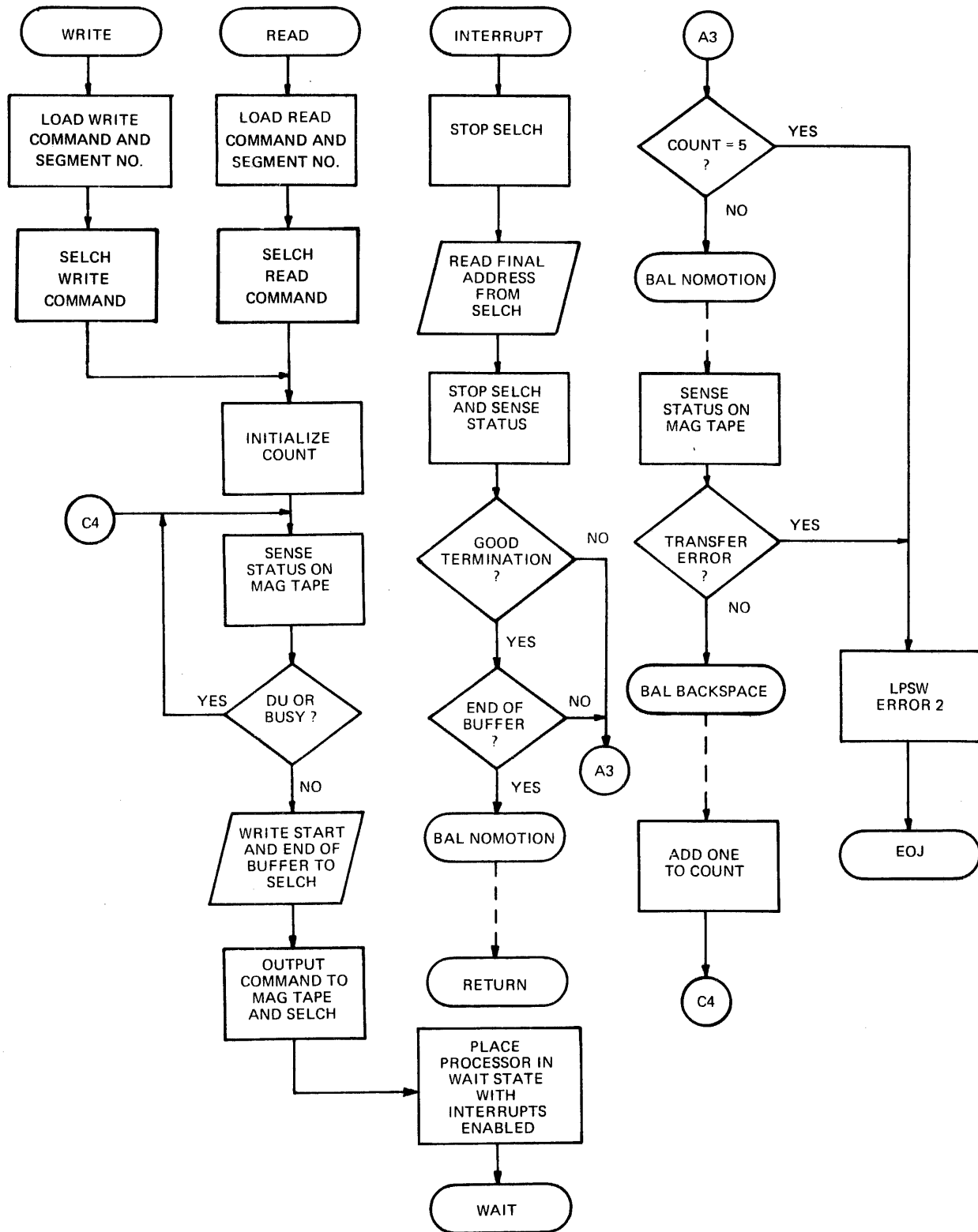
A1-8

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APPENDIX 2  
 16 BIT EXTENDED SELCH (MAG TAPE & EXT INTERRUPTS)



APPENDIX 2 (Continued)





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A2-3

PROG= ESELME ASSEMBLED BY CAL 03-066R04-01 (16-BIT)

	1	SCRAT			MAG00020
	2	WIDTH 120			MAG00030
	3	CROSS			MAG00040
	4	TARGT 16			MAG00050
	5	*			MAG00060
	6	* THIS PROGRAM USES THE 16 BIT EXTENDED SELCH & EXTERNAL			MAG00070
	7	* INTERRUPTS TO:			MAG00080
	8	* (1) WRITE A BUFFER FROM MEMORY SEGMENT ZERO (0)			MAG00090
	9	* TO THE MAG TAPE.			MAG00100
	10	* (2) READ FROM THE MAG TAPE TO A BUFFER IN MEMORY			MAG00110
	11	* SEGMENT ONE (1).			MAG00120
	12	* (3) WRITE THE DATA BACK TO THE MAG TAPE.			MAG00130
	13	* (4) READ THE DATA FROM THE MAG TAPE BACK TO			MAG00140
	14	* THE ORIGINAL BUFFER IN MEMORY SEGMENT ZERO (0).			MAG00150
	15	*			MAG00160
	16	* 16-BIT PROCESSORS			MAG00170
	17	*			MAG00180
	18	* REGISTER ASSIGNMENTS:			MAG00190
	19	*			MAG00200
	20	R1 EQU 1	START OF BUFFER REGISTER		MAG00210
	21	DU EQU 1	DEVICE UNAVAILABLE		MAG00220
	22	R2 EQU 2	END OF BUFFER REGISTER		MAG00230
	23	R3 EQU 3	DEVICE ADDRESS REGISTER		MAG00240
	24	R4 EQU 4	STATUS		MAG00250
	25	R5 EQU 5	RETURN REGISTER		MAG00260
	26	R6 EQU 6	MOST SIG 2 BITS OF MEMMORY ADDRESS		MAG00270
	27	R7 EQU 7	COUNTER		MAG00280
	28	BSY EQU 8	BUSY		MAG00290
	29	R8 EQU 8	COMMAND BYTE STORE		MAG00300
	30	R9 EQU 9	SELCH ADDRESS REGISTER		MAG00310
	31	R10 EQU 10	SELCH COMMAND HOLD REGISTER		MAG00320
	32	R11 EQU 11	WORK REGISTER		MAG00330
	33	R12 EQU 12	RETURN REGISTER		MAG00340
	34	R13 EQU 13	INTERRUPT DEVICE REGISTER		MAG00350
	35	R14 EQU 14	INTERRUPT STATUS REGISTER		MAG00360
	36	R15 EQU 15	WORK REGISTER		MAG00370
	37	TEST EQU X'10'	TEST=NOMOTION BIT		MAG00380
	38	BOT EQU X'20'	TEST FOR BOT		MAG00390
	39	TERM EQU X'C0'	TERMINATION STATUS=X'C0'		MAG00400
	40	XHR R15,R15	ZERO OUT REGISTER 15		MAG00410
	41	STH R15,X'44'	ZERO OUT NEW PSW		MAG00420
	42	LHI R15,MTINT	LOAD INTERRUPT HANDLER		MAG00430
	43	STH R15,X'46'	STORE INTEKRUPT HANDLER IN NEW LOC		MAG00440
	44	LH R3,MTADR	LOAD MAG TAPE ADDRESS		MAG00450
	45	LH R9,SELCH	LOAD SELCH ADDRESS		MAG00460
	46	OC R9,STOP	STOP SELCH		MAG00470
	47	DUTEST OC R3,RESET	OUTPUT RESET TO MAG TAPE		MAG00480
	48	SSR R3,R4	SENSE STATUS ON MAG TAPE		MAG00490
	49	BTC DU,DUTEST	IS MAG TAPE UNAVAILABLE		MAG00500
	50	THI R4,BOT	TEST FOR BOT		MAG00510
	51	BZS WRT	BRANCH TO WRITE		MAG00520
	52	BAL R5,FLMK	FILEMARK ROUTINE		MAG00530
	53	BAL R5,BAKSP	BACKSPACE ROUTINE		MAG00540
	54	WRT LHI R1,BUFSRT	LOAD START OF BUFFER		MAG00550
0000R	07FF				
0002R	40F0 0044				
0006R	C8F0 00C2R				
000AR	40F0 0046				
000ER	4830 0142R				
0012R	4890 0140R				
0016R	DE90 014AR				
001AR	DE30 014BR				
001ER	9D34				
0020R	4210 001AR				
0024R	C340 0020				
0028R	2335				
002AR	4150 0076R				
002ER	4150 0070R				
0032R	C810 0100R				

APPENDIX 2 (Continued)

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A2-4

0036R	C820	0137R	55	LHI	R2,BUFEND	LOAD END OF BUFFER	MAG00560
003AR	0766		56	XHR	R6,R6	LOAD 2 MOST SIG BITS OF MEM (0)	MAG00570
003CR	41C0	0084R	57	BAL	R12,WRITE	WRITE TO DEVICE	MAG00580
			58	*			MAG00590
0040R	4150	0070R	59	BAL	R5,BAKSP	BACKSPACE	MAG00600
0044R	0711		60	XHR	R1,R1	LOAD START OF BUFFER (0)	MAG00610
0046R	C820	0037	61	LHI	R2,BUFEND-BUFSRT	LOAD END OF BUFFER	MAG00620
004AR	D360	0151R	62	LB	R6,MEMSEG	LOAD 2 MOST SIG BITS OF MEM	MAG00630
004ER	41C0	009AR	63	BAL	R12,READ	READ FROM DEVICE	MAG00640
			64	*			MAG00650
0052R	4150	0070R	65	BAL	R5,BAKSP	BACKSPACE	MAG00660
0056R	41C0	0084R	66	BAL	R12,WRITE	WRITE TO DEVICE	MAG00670
			67	*			MAG00680
005AR	C810	0100R	68	LHI	R1,BUFSRT	LOAD TART OF BUFFER	MAG00690
005ER	C820	0137K	69	LHI	R2,BUFEND	LOAD END OF BUFFER	MAG00700
0062R	0766		70	XHR	R6,R6	LOAD 2 MOST SIG BITS OF ADR	MAG00710
0064R	4150	0070R	71	BAL	R5,BAKSP	BACKSPACE	MAG00720
0068R	41C0	009AR	72	BAL	R12,READ	READ FROM DEVICE	MAG00730
			73	*			MAG00740
006CR	C200	013CR	74	END1	LPSW END		MAG00750
			75	*****			MAG00760
			76	*	SUBROUTINE: BAKSP		MAG00770
			77	*	THIS SUBROUTINE BACKSPACES ONE RECORD.		MAG00780
			78	*	SEE CALLING SEQUENCE BELOW.		MAG00790
			79	*			MAG00800
			80	*	SUBROUTINE: FLMK		MAG00810
			81	*	THIS SUBROUTINE WRITES A FILEMARK		MAG00820
			82	*	SEE CALLING SEQUENCE BELOW.		MAG00830
			83	*			MAG00840
			84	*			MAG00850
			85	*****			MAG00860
			86	*			MAG00870
			87	*	SUBROUTINE: NOMOT		MAG00880
			88	*	THIS SUBROUTINE WAITS FOR THE MAG TAPE TO		MAG00890
			89	*	STOP MOVING.		MAG00900
			90	*			MAG00910
			91	*	CALLING SEQUENCE: BAL R5,BAKSP		MAG00920
			92	*	----- BAL R5,FLMK		MAG00930
			93	*	BAL R5,NOMOT		MAG00940
			94	*	R3=DEVICE ADDRESS REGISTER		MAG00950
			95	*	R5=RETURN REGISTER		MAG00960
			96	*			MAG00970
			97	*	WORK REGISTERS:		MAG00980
			98	*	-----		MAG00990
			99	*	R4=DEVICE STATUS REGISTER		MAG01000
			100	*			MAG01010
			101	*****			MAG01020
			102	*			MAG01030
0070R	DE30	014DR	103	BAKSP	OC R3,BKSP	OUTPUT A BACKSPACE	MAG01040
0074R	2303		104		BS NOMOT	BRANCH TO NOMOTION	MAG01050
0076R	DE30	014CR	105	FLMK	OC R3,FILMRK	OUTPUT A FILEMARK	MAG01060
007AR	9034		106	NOMOT	SSR R3,R4	SENSE STATUS	MAG01070
007CR	C340	0010	107		THI R4,TEST	TEST FOR NO MOTION	MAG01080
0080R	2233		108		BZS NOMOT	SENSE AGAIN	MAG01090
0082R	0305		109		BR R5	RETURN	MAG01100
			110	*****			MAG01110

APPENDIX 2 (Continued)

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		111 *				MAG01120
		112 *	SUBROUTINE: WRITE			MAG01130
		113 *	THIS SUBROUTINE WRITES ONE BLOCK OF DATA TO THE			MAG01140
		114 *	MAG TAPE.			MAG01150
		115 *	SEE CALLING SEQUENCE BELOW			MAG01160
		116 *				MAG01170
		117 *	SUBROUTINE READ			MAG01180
		118 *	THIS SUBROUTINE READS A BLOCK OF DATA FROM THE			MAG01190
		119 *	MAG TAPE.			MAG01200
		120 *				MAG01210
		121 *	CALLING SEQUENCE: BAL R12,WRITE			MAG01220
		122 *	----- BAL R12,READ			MAG01230
		123 *	R1=START OF BUFFER			MAG01240
		124 *	R2=END OF BUFFER			MAG01250
		125 *	R3=DEVICE ADDRESS REGISTER			MAG01260
		126 *	R9=SELCH ADDRESS REGISTER			MAG01270
		127 *	R12=RETURN REGISTER			MAG01280
		128 *				MAG01290
		129 *	WORK REGISTERS:			MAG01300
		130 *	-----			MAG01310
		131 *	R4=STATUS REGISTER			MAG01320
		132 *	R5=NOMOTION RETURN REGISTER			MAG01330
		133 *	R7=RETRY COUNT			MAG01340
		134 *	R8=COMMAND REGISTER			MAG01350
		135 *	R10=SELCH COMMAND REGISTER			MAG01360
		136 *	R11=WORK REGISTER			MAG01370
		137 *	R13=INTERRUPT DEVICE REGISTER			MAG01380
		138 *	R14=INTERRUPT STATUS REGISTER			MAG01390
		139 *	*****			MAG01400
0084R	D380 014FR	140	WRITE LB R8,WRTCMD	LOAD WRITE COMMAND		MAG01410
0088R	D3A0 0149R	141	LB R10,SELWRT	LOAD SELCH WRITE		MAG01420
008CR	C4A0 00FC	142	NHI R10,X'FC'	BITS 0-5 OF COMMAND		MAG01430
0090R	C460 0003	143	NHI R6,X'03'	BITS 6-7 OF COMMAND		MAG01440
0094R	06A6	144	OHR R10,R6	COMPOSE SELCH COMMAND		MAG01450
0096R	4300 00ACR	145	B RETRY	BRANCH TO RETRY		MAG01460
		146 *				MAG01470
009AR	D380 0150R	147	READ LB R8,RDCMD	LOAD READ COMMAND		MAG01480
009ER	D3A0 0148R	148	LB R10,SELRD	LOAD SELCH READ		MAG01490
00A2R	C4A0 00FC	149	VHI R10,X'FC'	BITS 0-5 OF COMMAND		MAG01500
00A6R	C460 0003	150	NHI R6,X'03'	BITS 6-7 OF COMMAND		MAG01510
00AAR	06A6	151	OHR R10,R6	COMPOSE SELCH COMMAND		MAG01520
00ACR	0777	152	RETRY XHR R7,R7	ZERO OUT COUNT		MAG01530
00AER	9D34	153	SENSE1 SSK R3,R4	SENSE STATUS		MAG01540
00BOR	2091	154	BTBS DU+BSY,SENSE1	TEST FOR BUSY+DEVICE UNAVAILABLE		MAG01550
00B2R	DE90 014AR	155	OC R9,STOP	STOP SELCH		MAG01560
00B6R	9891	156	WHR R9,R1	WRITE START OF BUFFER TO SELCH		MAG01570
00B8R	9892	157	WHR R9,R2	WRITE END OF BUFFER TO SELCH		MAG01580
00BAR	9E38	158	OCR R3,R8	OUTPUT COMMAND TO MT		MAG01590
00BCR	9E9A	159	OCR R9,R10	OUTPUT COMMAND TO SELCH		MAG01600
00BER	C200 0144R	160	WAIT1 LPSW WAIT			MAG01610
00C2R	9FDE	161	MTINT AIR R13,R14			MAG01620
00C4R	DE90 014AR	162	OC R9,STOP	STOP THE SELCH		MAG01630
00C8R	999B	163	RHR R9,R11	READ FINAL ADR. FROM SELCH		MAG01640
00CAR	DE90 014AR	164	OC R9,STOP	STOP THE SELCH		MAG01650
00CER	9D34	165	SSR R3,R4	SENSE STATUS OF MAG TAPE		MAG01660
00D0R	C340 00C0	166	THI R4,TERM	TEST FOR GOOD TERMINATION		MAG01670

00D4R	4230	00E4R	167	BNZ	ERROR	BRANCH TO TRY AGAIN.	MAG01680
00D8R	05B2		168	CLHR	R11,R2	TEST FOR END OF BUFFER	MAG01690
00DAR	4230	00E4R	169	BNE	ERROR		MAG01700
00DER	4150	007AR	170	BAL	R5,NOMOT	WAIT FOR TAPE TO STOP	MAG01710
00E2R	030C		171	BR	R12	RETURN	MAG01720
			172	*			MAG01730
			173	*	THIS ROUTINE ABORTS THE PROGRAM ON NON-RECOVERABLE STATUS ERRORS		MAG01740
			174	*	AND TRIES 5 TIMES TO RECOVER ON DATA TRANSFER STATUS ERRORS		MAG01750
			175	*	BEFORE TERMINATING.		MAG01760
			176	*			MAG01770
00E4R	C570	0005	177	ERROR	CLHI R7,5	TEST FOR 5 TRIES	MAG01780
00E8R	4330	00FAR	178		BE ERROR1	BRANCH TO ERROR1	MAG01790
00ECR	4150	007AR	179		BAL R5,NOMOT	WAIT FOR TAPE TO STOP	MAG01800
00FOR	4150	007OR	180		BAL R5,BAKSP	OUTPUT A BACKSPACE	MAG01810
00F4R	2671		181		AIS K7,1	ADD ONE TO COUNT	MAG01820
00F6R	4300	00AER	182		B SENSE1	BRANCH TO SENSE1	MAG01830
00FAR	C200	0138R	183	ERROR1	LPSW ERROR2		MAG01840
0100R			184		ALIGN 4	ALIGN START OF BUFFER	MAG01850
			185	*		ON HALFWORD BOUNDARY	MAG01860
0100R	0123		186	BUFSRT	DC X'0123',X'4567'		MAG01870
0102R	4567						
0104R	89AB		187		DC X'89AB',X'CDEF'		MAG01880
0106R	CDEF						
0108R	0123		188		DC X'0123',X'4567'		MAG01890
010AR	4567						
010CR	89AB		189		DC X'89AB',X'CDEF'		MAG01900
010ER	CDEF						
0110R	0123		190		DC X'0123',X'4567'		MAG01910
0112R	4567						
0114R	89AB		191		DC X'89AB',X'CDEF'		MAG01920
0116R	CDEF						
0118R	0123		192		DC X'0123',X'4567'		MAG01930
011AR	4567						
011CR	89AB		193		DC X'89AB',X'CDEF'		MAG01940
011ER	CDEF						
0120R	0123		194		DC X'0123',X'4567'		MAG01950
0122R	4567						
0124R	89AB		195		DC X'89AB',X'CDEF'		MAG01960
0126R	CDEF						
0128R	0123		196		DC X'0123',X'4567'		MAG01970
012AR	4567						
012CR	89AB		197		DC X'89AB',X'CDEF'		MAG01980
012ER	CDEF						
0130R	0123		198		DC X'0123',X'4567'		MAG01990
0132R	4567						
0134R	89AB		199		DC X'89AB',X'CDEF'		MAG02000
0136R	CDEF						
	0000	0137R	200	BUFEND	EQU *-1		MAG02010
0138R	8000		201	ERROR2	DC X'8000',A(ERROR1)		MAG02020
013AR	00FAR						
013CR	8000		202	END	DC X'8000'		MAG02030
013ER	006CR		203		DC A(END1)		MAG02040
0140R	00F0		204	SELCH	DC X'F0'	SELECTOR CHANNEL ADDRESS	MAG02050
0142R	00B5		205	MTADR	DC X'85'	MAG TAPE ADDRESS	MAG02060
0144R	C000		206	WAIT	DC X'C000'	PUT PROCESSOR IN WAIT STATE	MAG02070
0146R	00BER		207		DC WAIT1	WITH EXTERNAL INTERRUPTS ENABLED	MAG02080

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16 BIT EXTENDED SELCH (MAG TAPE & EXT INTERRUPTS)

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0148R	30	208	SELRD	DB	X*30*	SELCH READ COMMAND	MAG02090
0149R	10	209	SELWRT	DB	X*10*	SELCH WRITE COMMAND	MAG02100
014AR	08	210	STOP	DB	X*08*	SELCH STOP COMMAND	MAG02110
014BR	E0	211	RESET	DB	X*E0*	RESET COMMAND	MAG02120
014CR	30	212	FILMRK	DB	X*30*	FILEMARK COMMAND	MAG02130
014DR	11	213	BKSP	DB	X*11*	BACKSPACE COMMAND	MAG02140
014ER	38	214	REWIND	DB	X*38*	REWIND COMMAND	MAG02150
014FR	22	215	WRTCMD	DB	X*22*	WRITE COMMAND FOR MAG TAPE	MAG02160
0150R	21	216	RDCMD	DB	X*21*	READ COMMAND FOR MAG TAPE	MAG02170
0151R	01	217	MEMSEG	DB	X*01*	MEMORY SEGMENT 1	MAG02180
0152R		218	END				MAG02190

APPENDIX 2 (Continued)

NO ERRORS 0 SQUEZ PASSES

CAL 04-01

ABSTOP	0000													
ADC	0002													
BAKSP	0070R	53	59	65	71	180								
BKSP	0140R	103												
BOT	0020	50												
BSY	0008	154												
BUFEND	0137R	55	61	69										
BUFSRT	0100R	54	61	68										
DU	0001	49	154											
DUTEST	001AR	49												
END	013CR	74												
END1	006CR	203												
ERROR	00E4R	167	169											
ERROR1	00FAR	178	201											
ERROR2	0138R	183												
FILMRK	014CR	105												
FLMK	0076R	52												
IMPTOP	0152R													
LAOC	0001													
MEMSEG	0151R	62												
MTADR	0142R	44												
MTINT	00C2R	42												
NOMOT	007AR	104	108	170	179									
PURETOP	0000R													
R1	0001	54	60	60	68	156								
R10	000A	141	142	144	148	149	151	159						
R11	000B	163	168											
R12	000C	57	63	66	72	171								
R13	0000	161												
R14	000E	161												
R15	000F	40	40	41	42	43								
R2	0002	55	61	69	157	168								
R3	0003	44	47	48	103	105	106	153	158	165				
R4	0004	48	50	106	107	153	165	166						
R5	0005	52	53	59	65	71	109	170	179	180				
R6	0006	56	56	62	70	70	143	144	150	151				
R7	0007	152	152	177	181									
R8	0008	140	147	158										
R9	0009	45	46	155	156	157	159	162	163	164				
RDCMD	0150R	147												
READ	009AR	63	72											
RESET	014BR	47												
RETRY	00ACR	145												
REWIND	014ER													
SELCH	0140R	45												
SELKD	0148R	148												
SELWRT	0149R	141												
SENSE1	00AER	154	182											
STOP	014AR	46	155	162	164									
TERM	00C0	166												
TEST	0010	107												
WAIT	0144R	160												

APPENDIX 2 (Continued)

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16 BIT EXTENDED SELCH (MAG TAPE & EXT INTERRUPTS)

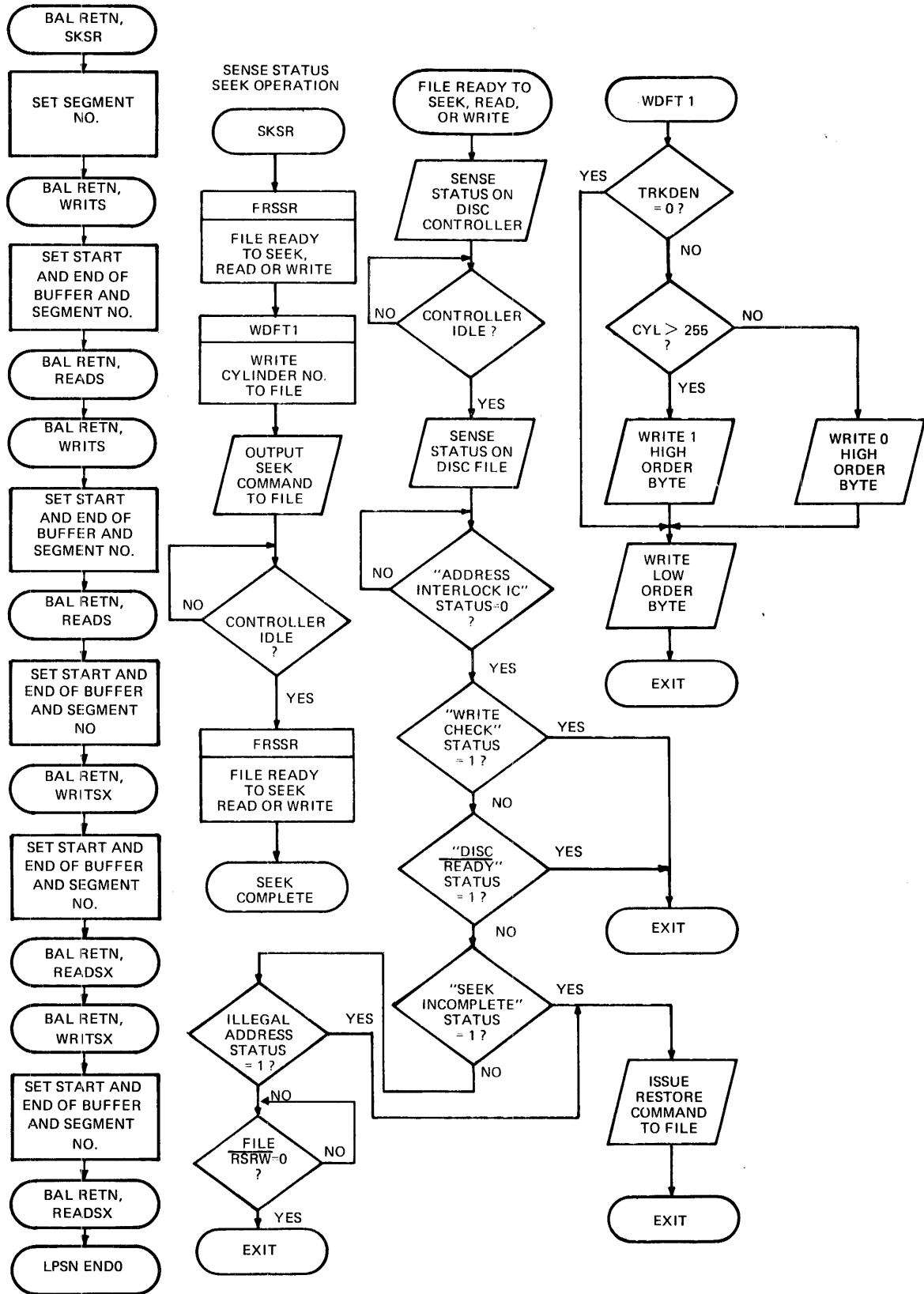
PAGE 7

WAIT1	00BER	207	
WRITE	0084R	57	66
WRT	0032R	51	
WRTCMD	014FR	140	

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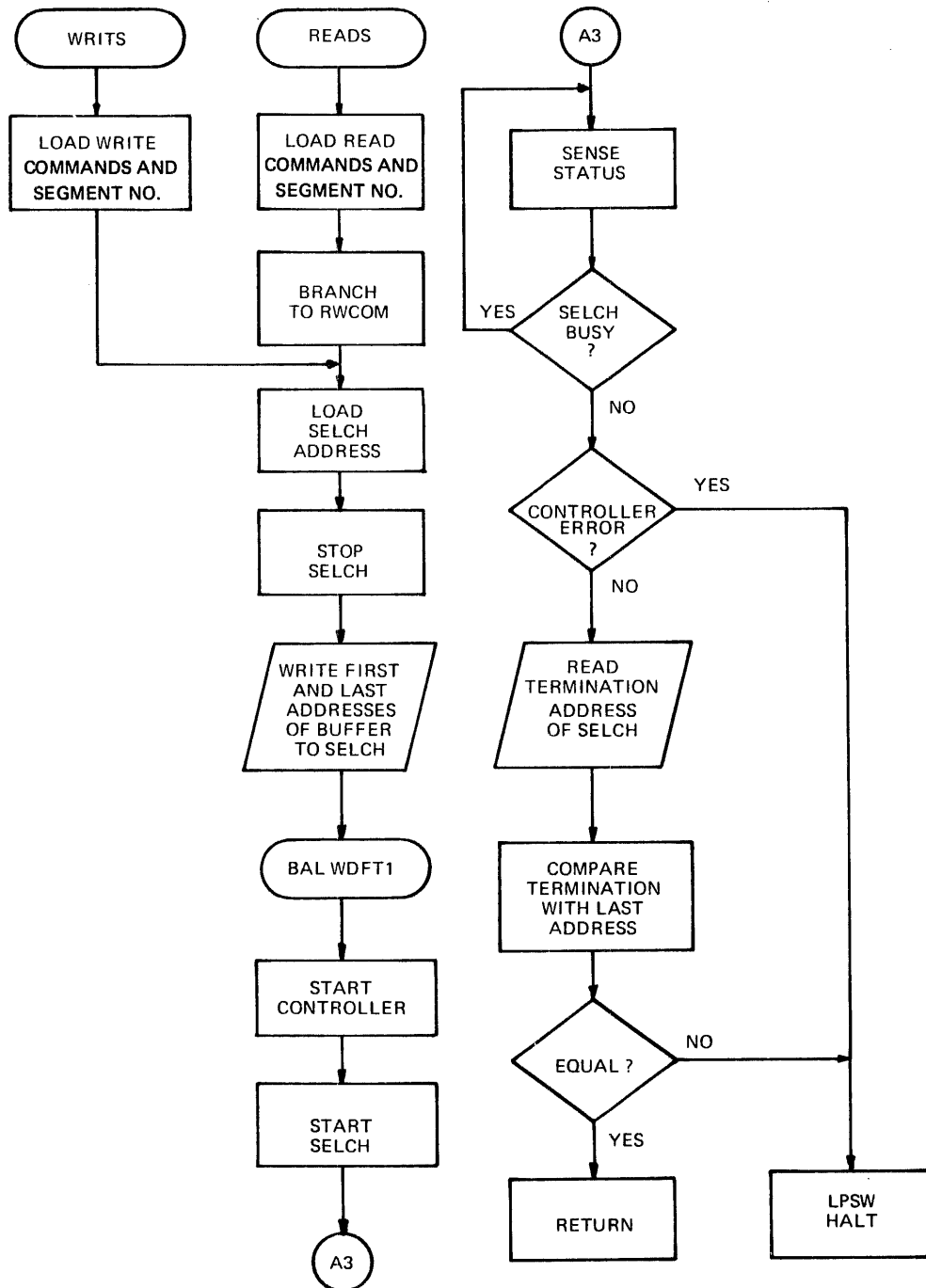
A2-9/A2-10

APPENDIX 3  
 16 BIT EXTENDED SELCH (DISC WITH SENSE STATUS & EXT INT)

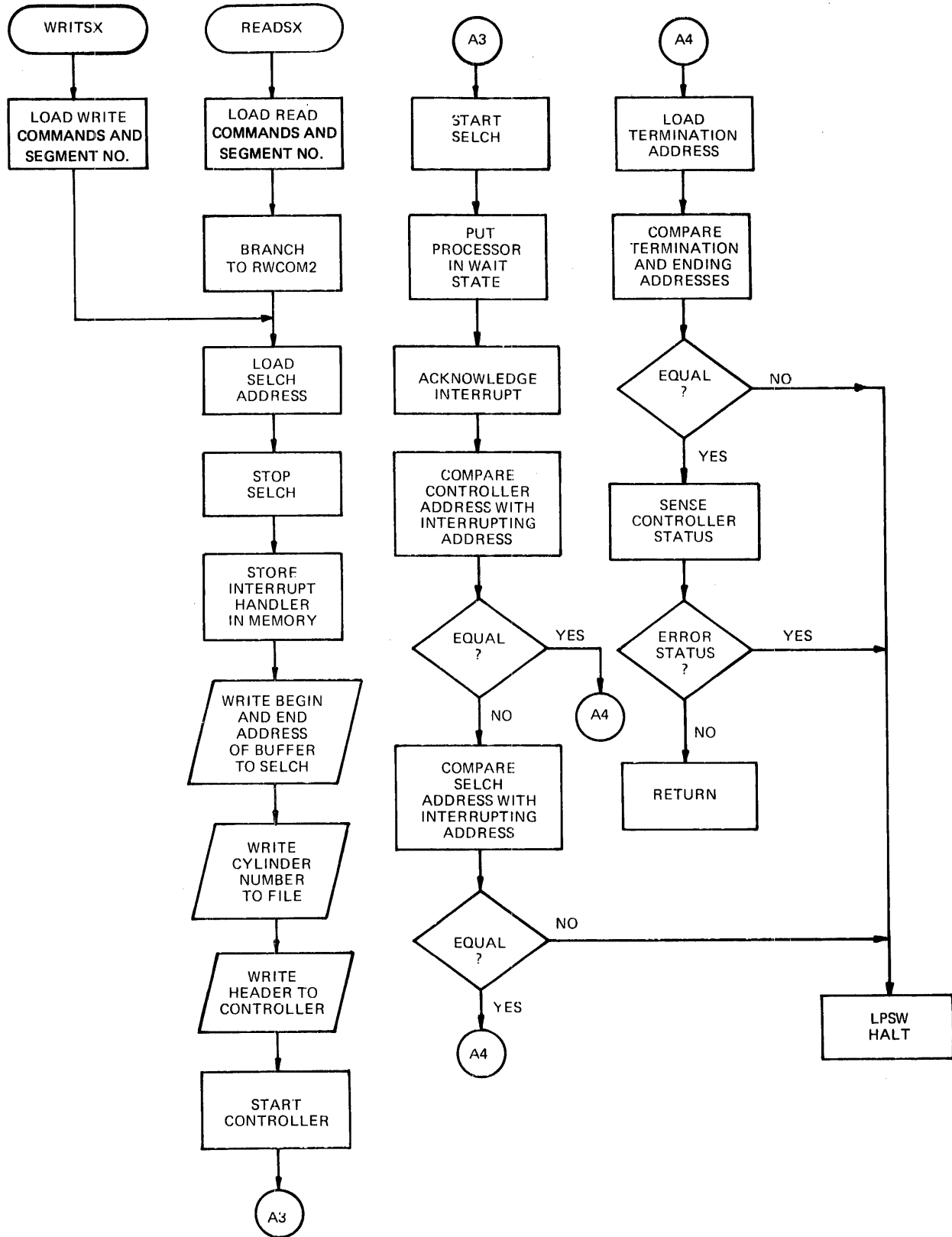




APPENDIX 3 (Continued)



APPENDIX 3 (Continued)



PROG= ESELDI ASSEMBLED BY CAL 03-066R04-01 (16-BIT)

		1	SCRAT		
		2	CROSS		
		3	TARGT 16		
		4	WIDTH 120		
		5	* THE FIRST PART OF THIS PROGRAM PERFORMS WRITE AND READ		
		6	* OPERATIONS WITH THE SELCH USING SENSE STATUS LOOPS.		
		7	*		
		8	* THE SECOND PART OF THIS PROGRAM PERFORMS WRITE AND READ		
		9	* OPERATIONS WITH THE SELCH USING INTERRUPTS CONTROL.		
		10	*		
		11	* IN BOTH CASES, DATA IS TRANSFERRED FROM MEMORY SEGMENT		
		12	* ZERO (0) TO MEMORY SEGMENT ONE (1) AND BACK AGAIN.		
		13	*		
	0000 0000	14	R0 EQU 0		
	0000 0001	15	R1 EQU 1		
	0000 0001	16	MEMSEG EQU 1	MEMORY SEGMENT NO.	
	0000 0004	17	SLAD EQU 4	SELCH ADDRESS	
	0000 0005	18	FUT EQU 5	FILE ADDRESS	
	0000 0006	19	WK0 EQU 6	WORK REGISTER 0	
	0000 0007	20	WK1 EQU 7	WORK REGISTER 1	
	0000 0008	21	WK2 EQU 8	WORK REGISTER 2	
	0000 0009	22	WK3 EQU 9	WORK REGISTER 3	
	0000 000B	23	TRACK EQU 11		
	0000 000D	24	STAT EQU 13	DEVICE STATUS	
	0000 000E	25	RETN2 EQU 14	RETURN REGISTER 2	
	0000 000F	26	RETN EQU 15	RETURN REGISTER 1	
	0000 000F	27	R15 EQU 15		
	0000 000A	28	DCAD EQU 10	DISC CONTROLLER ADDRESS	
	0000 000C	29	SECT EQU 12	DISC SECTOR NUMBER	
	0000 0008	30	SLCHBSY EQU 8	SELCH BUSY STATUS	
	0000 0002	31	CONTIDLE EQU 2	DISC CONTROLLER IDLE	
	0000 0010	32	ADRINTLK EQU X'10'	FILE ADDR INTLK STATUS	
	0000 0043	33	FLUNRECV EQU X'43'	WRCHK+SEEKING+DISCNTROY (FILE STAT)	
	0000 0008	34	RSRWT EQU 8	FILE READY TO SEEK,READ,OR WRITE	
	0000 0005	35	CNTUNREC EQU 5	EX+DATATRNSERERR (CONT STAT)	
	0000 0080	36	OVERRUN EQU X'80'	CONTROLLER OVERRUN STATUS	
	0000 0044	37	NEWPSWST EQU X'44'	EXTERNAL INT. NEW PSW STAT	
	0000 0046	38	NEWPSWLC EQU X'46'	EXTERNAL INT NEW PSW LOC.	
0000R	41F0 0070R	39	BAL RETN,SKSR		
0004R	0711	40	XHR R1,R1	MEMORY SEGMENT 0	
0006R	41F0 00E4R	41	BAL RETN,WRITS	WRITE TO DEVICE	
000AR	07FF	42	XHR R15,R15		
000CR	40F0 022ER	43	STH R15,SA	START ADR 0	
0010R	C8F0 0037	44	LHI R15,SAFA	GET BUFFER SIZE	
0014R	40F0 0230R	45	STH R15,FA	FINAL ADR	
0018R	2411	46	LIS MEMSEG,1	MEMORY SEGMENT 1	
001AR	41F0 00D4R	47	BAL RETN,READS	READ FROM DEVICE	
001ER	41F0 00E4R	48	BAL RETN,WRITS	WRITE TO DEVICE	
0022R	C8F0 01D4R	49	LHI R15,BUFSRT	START ADR	
0026R	40F0 022ER	50	STH R15,SA		
002AR	C8F0 020BR	51	LHI R15,BUFEND	END ADR	
002ER	40F0 0230R	52	STH R15,FA		
0032R	0711	53	XHR R1,R1	MEMORY SEGMENT 1	
0034R	41F0 00D4R	54	BAL RETN,READS		

APPENDIX 3 (Continued)

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55 *
56 * INTERRUPT CONTROL
57 *
0038R 0711          58      XHR      R1,R1          MEMORY MODULE 0
003AR 41F0 014ER   59      BAL      RETN,WRITSX      WRITE TO DEVICE
003ER 07FF          60      XHR      R15,R15
0040R 40F0 022ER   61      STH      R15,SA          START ADR 0
0044R C8F0 0037   62      LHI      R15,SAFA        GET BUFFER SIZE
0048R 40F0 0230R   63      STH      R15,FA          FINAL ADR
004CR 2411          64      LIS      MEMSEG,1        MEMORY SEGMENT 1
004ER 41F0 013CR   65      BAL      RETN,READSX      READ FROM DEVICE
0052R 41F0 014ER   66      BAL      RETN,WRITSX      WRITE TO DEVICE
0056R C8F0 01D4R   67      LHI      R15,BUFSRT        START AADR
005AR 40F0 022ER   68      STH      R15,SA
005ER C8F0 020BR   69      LHI      R15,BUFEND        END ADR
0062R 40F0 0230R   70      STH      R15,FA
0066R 0711          71      XHR      R1,R1          MEMORY MODULE 0
0068R 41F0 013CR   72      BAL      RETN,READSX      READ FROM DEVICE
006CR C200 020CR   73      EOP      LPSW      ENDO
74 * SUBROUTINE: SENSE STATUS SEEK
75 * FUNCTION:PERFORMS SENSE STATUS SEEK OPERATIONS
76 * CALLING SEQUENCE: BAL REIN,SKSR
77 * INPUT
78 * REGISTERS: TRACK= DESTRED CYLINDER NUMBER
79 *          FUT= FILE ADDRESS
80 *          SLAD= SELCH ADDRESS
81 *          DCAD= DISC CONTROLLER ADDRESS
82 * NOTE: IF LOCATION TRKDEN=0, A 2.5 MEGABYTE DRIVE IS ASSUMED
83 *          IF LOCATION TRKDEN=1, A 10 MEGABYTE DRIVE IS ASSUMED
0070R 07CC          84      SKSR     XHR      SECT,SECT      REGISTER SECT IS DESTROYED
0072R 41E0 0084R   85      BAL      RETN2,FRSSR      FILE READY TO SEEK,READ,WRITE SEQ
0076R 41E0 00AER   86      BAL      RETN2,WDFST1      WRITE CYLINDER NUMBER TO FILE
007AR DE50 0210R   87      OC       FUT,SEEKC      OUTPUT SEEK COMMAND (INPTS DISARMD)
007ER 41E0 0084R   88      BAL      RETN2,FRSSR      WAIT FOR SEEK COMPLETE W/ GOOD STAT
0082R 030F          89      BR       RETN          RETURN TO USER
90 *
91 *
92 *SUBROUTINE: FILE READY TO SEEK,READ OR WRITE
93 *FUNCTION: PERFORMS NECESSARY STATUS CHECK ON CONTROLLER AND FILE TO
94 *          INSURE CORRECT FILE OPERATION
95 * CALLING SEQUENCE: BAL RFTN2,FRSSR
96 * INPUT
97 * REGISTERS: FUT= FILE ADDRESS
98 *          SLAD= SELCH ADDRESS
99 *          DCAD= CONTROLLER ADDRESS
0084R 48A0 0222R   100     FRSSR    LH       DCAD,DISCONAD
0088R 9DAD          101     SSR      DCAD,STAT
008AR 4320 0084R   102     BFC     CONTIDLE,FRSSR      IF CONTROLLER NOT IDLE WAIT
008ER 4850 0224R   103     LH       FUT,FOT
0092R 905D          104     SSR      FUT,STAT          SENSE FILE STATUS
0094R C300 0010   105     THI     STAT,ADRINTLK      TEST FILE STATUS FOR ADRINTLK=0
0098R 4230 0084R   106     BNZ     FRSSR          ADRINTLK=1 WAIT FOR IT TO GO TO ZERO
009CR C3D0 0043   107     THI     STAT,FLUNRECV      UNRECOVERABLE FILE ERROR
00A0R 4230 01CER   108     BNZ     ERRSTOP        ABORT THE OPERATION
109 * AT THIS POINT USER COULD ATTEMPT TO CORRECT SEEK INCOMPLETE STATUS
110 * BY ISSUING A RESTORE COMMAND AND REPEATING THE DESIRED SEEK

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APPENDIX 3 (Continued)

00A4R	C3D0	0008	111	FRSSR1	THI	STAT,RSRWT	FILE RSWRT=1
00A8R	4230	00A4R	112		BNZ	FRSSR1	IF YES WAIT FOR RSRWT=0
00ACR	030E		113		BR	RETN2	RETURN
			114	*			
			115	*			
			116	*	SUBROUTINE: WRITE CYLINDER NUMBER TO THE FILE		
			117	*	FUNCTION: WRITE CYLINDER # TO THE DISC FILE		
			118	*	CALLING SEQUENCE: BAL RFTN2,WDF1		
			119	*	INPUT		
			120	*	REGISTERS: TRACK=DESIRED BYLINDER NUMBER		
			121	*	FUT=FILE ADDRESS		
			122	*	SLAD=SELCH ADDRESS		
			123	*	DCAD=DISC CONTROLLER ADDRESS		
			124	*	R0=ZERO UPON ENTRY TO ROUTINE		
			125	*	NOTE: IF LOCATION TRKDEN=0, A 2.5 MEGABYTE DRIVE IS ASSUMED		
			126	*	IF LOCATION TRKDEN=1, A 10 MEGABYTE DRIVE IS ASSUMED		
00AER	4500	0228R	127	WDF1	CLH	R0,TRKDEN	TRACK DENSITY=0
00B2R	4330	00D0R	128		BE	WDF1A	YES- ASSUME 2.5 DRIVE GO TO WDF1A
00B6R	C5B0	0100	129		CLHI	TRACK,256	CYLINDER NUMBER= OR > 256
00BAR	4380	00D0R	130		BNL	WDF1A	YES- SET MSB IN CONTROLLER AT WDF1
00BER	48B0	0226R	131		LH	TRACK,TRCK	
00C2R	4850	0224R	132		LH	FUT,FOT	
00C6R	DA50	022AR	133		WD	FUT,ZERO	
00CAR	2303		134		BS	WDF1A	
00CCR	JA50	022BR	135	WDF1	WD	FUT,ONE	IF THE DESIRED DRIVE IS A 10 MB TOP
00D0R	9A5B		136	WDF1A	WDR	FUT,TRACK	OR BOTTOM AND THE DESIRED SEEK IS TO
00D2R	030E		137		BR	RETN2	A CYLINDER > 256 THEN A HALFWORD
			138	*			MUST BE WRITTEN TO THE DRIVE TO
			139	*			INSURE THAT THE CORRECT CYLINDER
			140	*			NUMBER IS WRITTEN TO THE FILE
			141	*	SUBROUTINE: READ/WRITE(SENSE STATUS CONTROL)		
			142	*	FUNCTION: PERFORMS SENSE STATUS READ/WRITE OPERATION TO DISC		
			143	*	CALLING SEQUENCE FOR READ: BAL RETN,READS		
			144	*	CALLING SEQUENCE FOR WRITE: BAL RETN,WRITS		
			145	*	INPUT		
			146	*	REGISTERS: FUT=FILE ADDRESS		
			147	*	DCADE= DISC CONTROLLER ADDRESS		
			148	*	SLADE= SELCH ADDRESS		
			149	*	TRACK=CYLINDER ADDRESS		
			150	*	SECT= DESIRED SECTOR		
			151	*	MEMORY LOCATIONS: HEAD=DESIRED HEAD		
			152	*	SA= STARTING BUFFER ADDRESS		
			153	*	FA= ENDING BUFFER ADDRESS		
00D4R	D370	0211R	154	READS	LB	WK1,RCMD	DISC READ COMMAND
00D8R	C880	0030	155		LHI	WK2,X'30'	SELCH READ/GO COMMAND
00DCR	C410	0003	156		NHI	MEMSEG,X'03'	BITS 6,7 ONLY
00E0R	0681		157		OHR	WK2,MEMSEG	ADD MEMORY SEGMENT
00E2R	2308		158		BS	RWCOM	
00E4R	D370	0212R	159	WRITS	LB	WK1,WCMD	DISC WRITE COMMAND
00E8R	C880	0010	160		LHI	WK2,X'10'	SELCH WRITE COMMAND
00ECR	C410	0003	161		NHI	MEMSEG,X'03'	BITS 6,7 ONLY
00FOR	0681		162		OHR	WK2,MEMSEG	ADD MEMORY SEGMENT.
00F2R	4840	022CR	163	RWCOM	LH	SLAD,SELAD1	LOAD SELCH ADDRESS
00F6R	DE40	021AR	164		OC	SLAD,STOP	STOP SELCH, IDLE
00FAR	D840	022ER	165		WH	SLAD,SA	WRITE BEGINNING ADDRESS TO SELCH
00FER	D840	0230R	166		WH	SLAD,FA	WRITE ENDING ADDRESS TO SELCH

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0102R	41E0	00AER	167	BAL	RETN2,WOFT1	WRITE THE CYLINDER NUMBER TO FILE
0106R	4890	021CR	168	LH	WK3,HEAD	
010AR	9195		169	SLLS	WK3,5	
010CR	080C		170	LHR	R0,SECT	
010ER	0609		171	OHR	R0,WK3	
0110R	9AA0		172	WDR	DCAD,R0	WRITE HEADER TO CONTROLLER
0112R	9EA7		173	OCR	DCAD,WK1	START CONTROLLER
0114R	9E48		174	OCR	SLAD,WK2	START THE SELCH
0116R	9D4D		175	DXTL	SSR	SLAD,STAT
0118R	4280	0116R	176	BTC	SLCHBSY,DXTL	WAIT FOR SELCH TO COMPLETE
011CR	DE40	021AR	177	OC	SLAD,STOP	STOP THE SELCH- SELCH IDLE
0120R	9DAD		178	DXTL1	SSR	DCAD,STAT
0122R	4320	0120R	179	BFC	CONTIDLE,DXTL1	WAIT FOR CONTROLLER TO GO IDLE
0126R	4250	01CER	180	BTC	CNTUNREC,ERRSTOP	BRANCH IF CONTROLLER ERROR
012AR	D940	0232R	181	RH	SLAD,SELAD	GET THE SELCH TERMINATION ADDRESS
012ER	4860	0232R	182	LH	WK0,SELAD	COMPARE SELCH TERMINAL ADDRESS
0132R	4560	0230R	183	CLH	WK0,FA	TO SELCH ENDING ADDRESS
0136R	4230	01CER	184	BNE	ERRSTOP	IF NOT EQUAL, GO TO ERRSTOP
013AR	030F		185	BR	RETN	RETURN TO NEXT BAL STATEMENT
			186	* SUBROUTINE: READ/WRITE (INTERRUPT CONTROL)		
			187	* FUNCTION: PERFORMS INTERRUPT READ/WRITE OPERATION TO DISC)		
			188	* CALLING SEQUENCE FOR READ: BAL RETN,READX		
			189	* CALLING SEQUENCE FOR WRITE: BAL RETN,WRITX		
			190	* INPUT		
			191	* REGISTERS: FUT=FILE ADDRESS		
			192	* DCAD=DISC CONTROLLER ADDRESS		
			193	* SLAD=SELCH ADDRESS		
			194	* TRACK=CYLINDER ADDRESS		
			195	* SECT= DESIRED SECTOR		
			196	* REGISTERS DESTROYED: NONE		
013CR	D370	0213R	197	READSX	LB	WK1,RCMDX
0140R	C880	0030	198		LHI	WK2,X'30'
0144R	C410	0003	199		NHI	MEMSEG,X'03'
0148R	0681		200		OHR	WK2,MEMSEG
014AR	4300	015CR	201		R	RWCOM2
014ER	D370	0214R	202	WRITSX	LB	WK1,WCMDX
0152R	C880	0010	203		LHI	WK2,X'10'
0156R	C410	0003	204		NHI	MEMSEG,X'03'
015AR	0681		205		OHR	WK2,MEMSEG
015CR	4840	022CR	206	RWCOM2	L4	SLAD,SELAD1
0160R	DE40	021AR	207		OC	SLAD,STOP
0164R	0766		208		XHR	WK0,WK0
0166R	4060	0044	209		STH	WK0,NEWPSWST
016AR	C860	0192R	210		LHI	WK0,SELCHNT1
016ER	4060	0046	211		STH	WK0,NEWPSWLC
0172R	D840	022ER	212		WH	SLAD,SA
0176R	D840	0230R	213		WH	SLAD,FA
017AR	41E0	00AER	214		BAL	RETN2,WOFT1
017ER	4890	021CR	215		LH	WK3,HEAD
0182R	9195		216		SLLS	WK3,5
0184R	080C		217		LHR	R0,SECT
0186R	0609		218		OHR	R0,WK3
0188R	9AA0		219		WDR	DCAD,R0
018AR	9EA7		220		OCR	DCAD,WK1
018CR	9E48		221		OCR	SLAD,WK2
018ER	C200	021ER	222	WAIT	LPSW	WAIT1
						WRITE THE CYLINDER NUMBER TO FILE
						WRITE HEADER TO CONTROLLER
						START CONTROLLER
						START SELCH
						WAIT FOR INTERRUPT

0192R	9F6D	223	*SELCH INTERRUPT ENTERS BELOW:		
0194R	056A	224	SELCHNT1 ACKR	WK0,STAT	ACKNOWLEDGE INTERRUPT
0196R	4330 01BAR	225	CLHR	WK0,DCAD	CONTROLLER INTERRUPTING?
019AR	0564	226	BE	CNTRLINT	IF YES GO SERVICE IT
019CR	4230 01CER	227	CLHR	WK0,SLAD	IF SELCH SERVICE IT
01A0R	DE40 021AR	228	BNE	ERRSTOP	IF NEITHER STOP IN ERROR
01A4R	D940 0234R	229	OC	SLAD,STOP	STOP THE SELCH- SELCH IDLE
01A8R	DE40 021AR	230	RH	SLAD,FADR	READ FINAL SELCH ADDRESS
01ACR	9DAD	231	OC	SLAD,STOP	
01AER	C3D0 0080	232	SSR	DCAD,STAT	SENSE CONTROLLER STATUS
01B2R	4230 01BAR	233	THI	STAT,OVERRUN	IF CONTROLLER OVERRUN STATUS IS SET
01B6R	4300 018ER	234	BNZ	CNTRLINT	DO NOT EXPECT CONTROLLER INTERRUPT
01BAR	4860 0234R	235	B	WAIT	BRA TO WAIT FOR CONTROLLER INTERRUPT
01BER	4560 0230R	236	CNTRLINT LH	WK0,FADR	GET THE FINAL ADDRESS
01C2R	4230 01CER	237	CLH	WK0,FA	COMPARE EXPECTED FINAL WITH THE LAST ADDRESS
01C6R	9DAD	238	BNE	ERRSTOP	IF NOT EQUAL GO TO ERROR
01C8R	4250 01CER	239	SSR	DCAD,STAT	SENSE CONTROLLER STATUS
01CCR	030F	240	BTC	CNTUNREC,ERRSTOP	IF OK EXIT OTHERWISE
01CER	C200 0216R	241	BR	RETN	RETURN TO NEXT BAL STATEMENT OR EOP
01D4R		242	ERRSTOP LPSW	HALT	IF ERROR, THEN HALT PROCESSOR
		243	ALIGN	4	ALIGN START OF BUFFER
		244	*		ON HALFWORD BOUNDARY
01D4R	0123	245	BUFSRT DC	X'0123',X'4567'	
01D6R	4567				
01D8R	89AB	246	DC	X'89AB',X'CDEF'	
01DAR	CDEF				
01DCR	0123	247	DC	X'0123',X'4567'	
01DER	4567				
01E0R	89AB	248	DC	X'89AB',X'CDEF'	
01E2R	CDEF				
01E4R	0123	249	DC	X'0123',X'4567'	
01E6R	4567				
01E8R	89AB	250	DC	X'89AB',X'CDEF'	
01EAR	CDEF				
01ECR	0123	251	DC	X'0123',X'4567'	
01EER	4567				
01FOR	89AB	252	DC	X'89AB',X'CDEF'	
01F2R	CDEF				
01F4R	0123	253	DC	X'0123',X'4567'	
01F6R	4567				
01F8R	89AB	254	DC	X'89AB',X'CDEF'	
01FAR	CDEF				
01FCR	0123	255	DC	X'0123',X'4567'	
01FER	4567				
0200R	89AB	256	DC	X'89AB',X'CDEF'	
0202R	CDEF				
0204R	0123	257	DC	X'0123',X'4567'	
0206R	4567				
0208R	89AB	258	DC	X'89AB',X'CDEF'	
020AR	CDEF				
	0000 020BR	259	BUFEND EQU	*-1	
	0000 0037	260	SAFA EQU	BUFEND-BUFSRT	
020CR	8000	261	ENDO DC	X'8000'	
020ER	006CR	262	DC	Z(EOP)	
0210R	C2	263	SEEKC DB	X'C2'	SEEK COMMAND
0211R	01	264	RCMD DB	X'01'	

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16 BIT EXTENDED SELCH (DISC WITH SENSE STATUS & EXT INT) PAGE 6

0212R	02	265	WCMD	DB	X*02*	
0213R	41	266	RCMDX	DB	X*41*	
0214R	42	267	WCMDX	DB	X*42*	
0216R	8000	268	HALT	DC	X*8000*	
0218R	01CER	269		DC	Z(ERRSTOP)	
021AR	08	270	STOP	DB	X*08*	SELCH STOP COMMAND
021CR	0000	271	HEAD	DC	X*0*	
021ER	C000	272	WAIT1	DC	X*C000*	
0220R	018ER	273		DC	Z(WAIT)	
0222R	00B6	274	DISCONAD	DC	X*B6*	DISC CONTROLLER ADDR.
0224R	00C6	275	FOT	DC	X*C6*	
0226R	0004	276	TRUCK	DC	X*04*	
0228R	0000	277	TRKDEN	DC	X*0*	TRACK DENSITY USED IN SENSE ST SK
022AR	00	278	ZERO	DB	0	ZERO CONSTANT
022BR	01	279	ONE	DB	1	ONE CONSTANT
022CR	00F0	280	SELAD1	DC	X*F0*	SELCH ADDRESS
		281	*			
022ER	01D4R	282	SA	DC	A(BUFSRT)	
0230R	020BR	283	FA	DC	A(BUFEND)	
0232R	0000	284	SELAD	DC	X*0*	FINAL SELCH TERMINATION ADDRESS
0234R	0000	285	FADR	DC	X*0*	FINAL BUFFER ADDRESS
		286	*			
0236R		287	ALIGN	2		
0236R		288	REGSAVE	DSH	16	REG SAVE AREA FOR REG SET
0256R		289		END		

APPENDIX 3 (Continued)



NO ERRORS 0 SQUEZ PASSES

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ABSTOP	0000																			
ADC	0002																			
ADRINTLK	0010	105																		
BUFEND	020BR	51	69	260	283															
BUFSRT	01D4R	49	67	260	282															
CNTRLINT	01BAR	226	234																	
CNTUNREC	0005	180	240																	
CONTIDLE	0002	102	179																	
DCAD	000A	100	101	172	173	178	219	220	225	232	239									
DISCONAD	0222R	100																		
DXTL	0116R	176																		
DXTL1	0120R	179																		
END0	020CR	73																		
EOP	006CR	262																		
ERRSTOP	01CER	108	180	184	228	238	240	269												
FA	0230R	45	52	63	70	166	183	213	237											
FADR	0234R	230	236																	
FLUNRECV	0043	107																		
FOT	0224R	103	132																	
FRSSR	0084R	85	88	102	106															
FRSSR1	00A4R	112																		
FUT	0005	87	103	104	132	133	135	136												
HALT	0216R	242																		
HEAD	021CR	168	215																	
IMPTOP	0256R																			
LADC	0001																			
MEMSEG	0001	46	64	156	157	161	162	199	200	204	205									
NEWPSWLC	0046	211																		
NEWPSWST	0044	209																		
ONE	022BR	135																		
OVERRUN	0080	233																		
PURETOP	0000R																			
R0	0000	127	170	171	172	217	218	219												
R1	0001	40	40	53	53	58	58	71	71											
R15	000F	42	42	43	44	45	49	50	51	52	60	60	61	62						
		63	67	68	69	70														
RCMD	0211R	154																		
RCMDX	0213R	197																		
READS	00D4R	47	54																	
READSX	013CR	65	72																	
REGSAVE	0236R																			
RETN	000F	39	41	47	48	54	59	65	66	72	89	185	241							
RETN2	000E	85	86	88	113	137	167	214												
RSRWT	0008	111																		
RWCOM	00F2R	158																		
RWCOM2	015CR	201																		
SA	022ER	43	50	61	68	165	212													
SAFA	0037	44	62																	
SECT	000C	84	84	170	217															
SEEKC	0210R	87																		
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SELAD1	022CR	163	206																	

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SELCHNT1	0192R	210												
SKSR	0070R	39												
SLAD	0004	163	164	165	166	174	175	177	181	206	207	212	213	221
		227	229	230	231									
SLCHBSY	0008	176												
STAT	000D	101	104	105	107	111	175	178	224	232	233	239		
STOP	021AR	164	177	207	229	231								
TRACK	000B	129	131	136										
TRKDEN	0228R	127												
TROCK	0226R	131												
WAIT	018FR	235	273											
WAIT1	021ER	222												
WCMD	0212R	159												
WCMOX	0214R	202												
WOFT0	00CCR													
WOFT1	00AER	86	167	214										
WOFT1A	00DOR	128	130	134										
WK0	0006	182	183	208	208	209	210	211	224	225	227	236	237	
WK1	0007	154	159	173	197	202	220							
WK2	0008	155	157	160	162	174	198	200	203	205	221			
WK3	0009	168	169	171	215	216	218							
WRITS	00E4R	41	48											
WRITSX	014ER	59	66											
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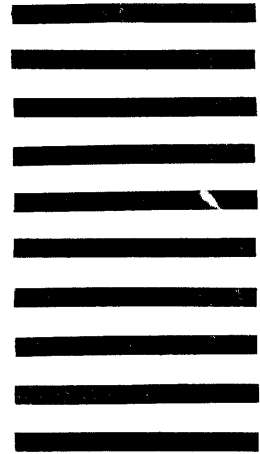
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