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32-198 CARTRIDGE DISC CONTROLLER INSTRUCTION MANUAL

Consists of:

Information Specification	B29-254R01-A12
Cartridge Disc Programming Specification	02-222A22
Schematics	B32-189R01B08

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DISC CONTROLLER
INFORMATION SPECIFICATION

1. INSTALLATION

1.1 Introduction

This controller, Product Number M07-735 and M07-736, consists of two INTERDATA printed circuit boards. The boards are called D and F; D for Data Control, and F for File Control. The boards are plugged into the Selector Channel bus in an INTERDATA expansion chassis.

The boards may be inserted into any two adjacent positions on the selector bus, but the D board must be to the right of the F board looking from the front of the expansion chassis. It is suggested that these boards be installed in the first two positions of the selector bus to give the controller highest priority on the selector RACKO-TACKO Chain.

The RACKO-TACKO straps (114-0 to 214-0) of the position occupied by the F board should be removed. The RACKO-TACKO straps should not be removed from the position occupied by the D board.

1.2 Disk File Installation

Refer to the Disk File Maintenance Manual provided by the vendor.

1.3 Power

This controller draws +5 volts DC from the computer supply. The user must furnish power for the files.

1.4 Cables

File 0 to Controller

Refer to Figure 1. A cable with a Winchester connector on one end and three daughter board connectors on the other is furnished for use between the controller and File 0. The Winchester connector is connected to P2 of File 0 and the daughter board connectors are plugged into positions 40 and 41 of the D board and position 40 of the F board. The connectors are marked accordingly.

If one file is used, the terminator furnished must be installed on P5 of the file.

Files 1, 2, and 3, if used

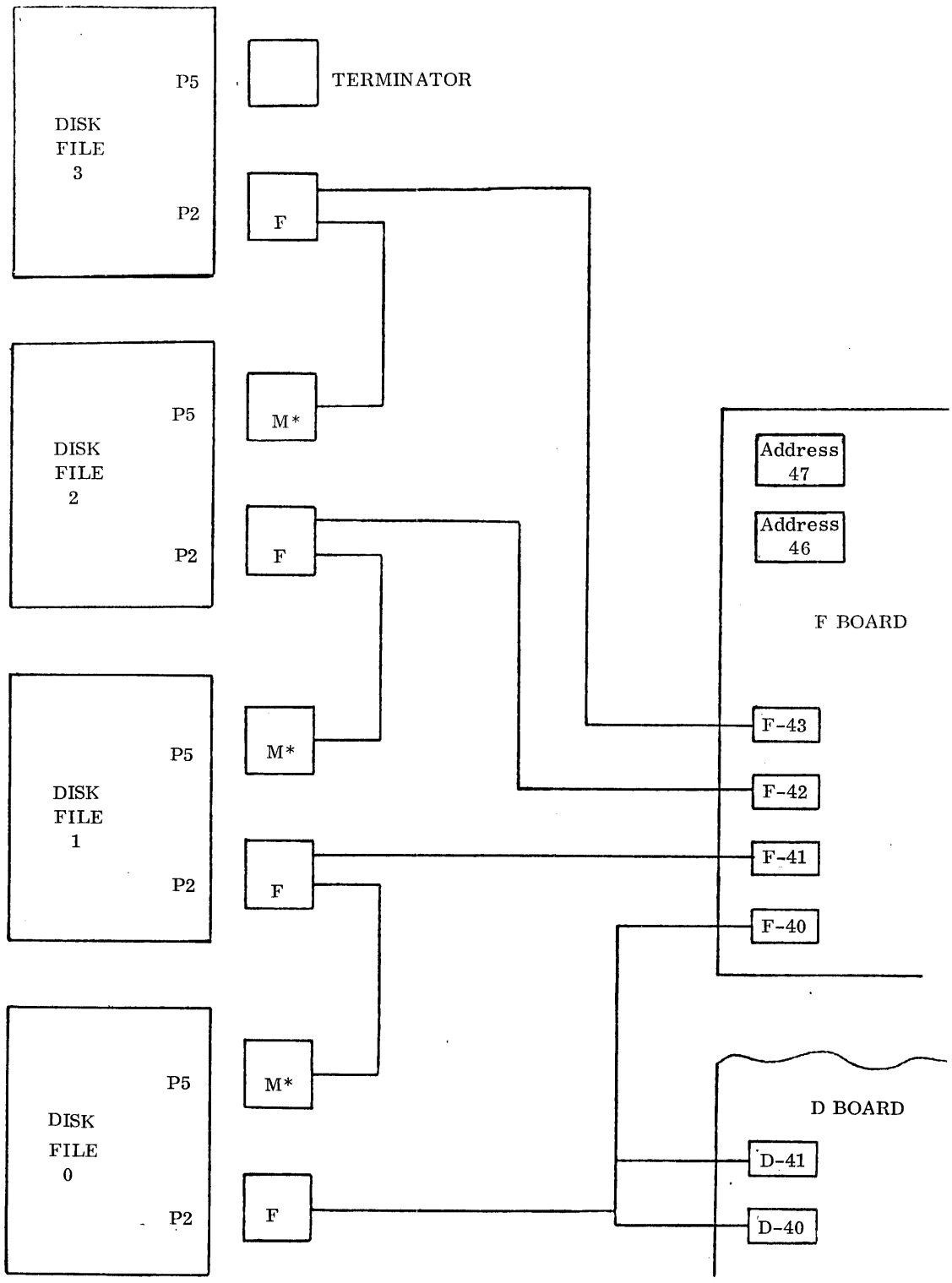
Two cables are furnished for each additional file. See Figure 1 for use.

The cable with Winchester connectors on each end connects each file to the next one. Note that the female Winchester connects to P2 of the next file, while the male Winchester connects to P5 of the previous file. The daughter board connector plugs into F-41, F-42, or F-43 depending on the file number.

File 1	F-41
File 2	F-42
File 3	F-43

The file select jumpers inside each file should be set to 1. File selection is determined by cable connections as described above. The terminator furnished should be connected to P5 of the last file in the chain.

Note that the small Viking connector is a push-on-lock type. To unlock, squeeze the sides of the connector at the finger grips and pull off.



*Terminator or Daisy-Chain Cable

Figure 1. File Controller Cables

2. OPERATION AND MAINTENANCE

2.1 Computer Addresses

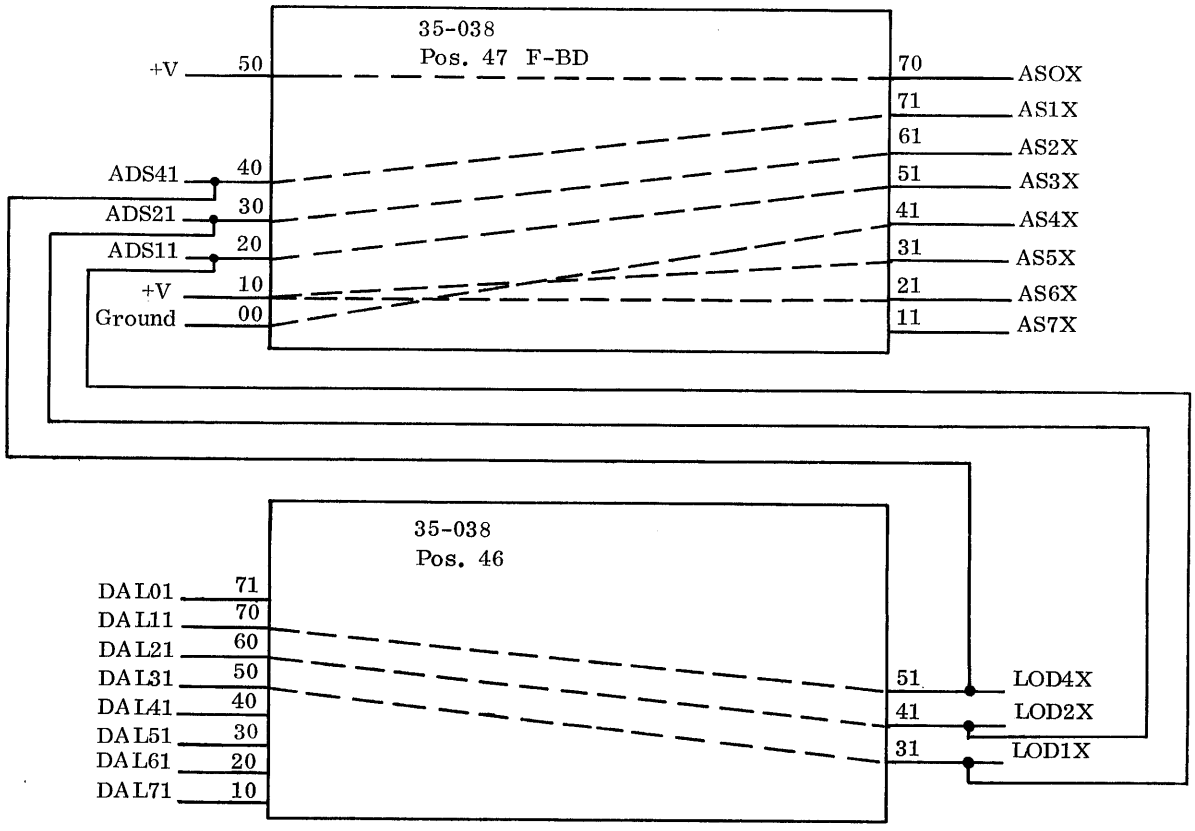
Each disk file has its own address, and the data transfer controller has its address. These addresses must be consecutive. Of the eight address bits, five bits must be identical for the files and the data controller. The three remaining bits must be as follows:

011	Data Controller
100	Disk File 0
101	Disk File 1
110	Disk File 2
111	Disk File 3

For example:

B 6	Data Controller
C 6	Disk File 0
D6	Disk File 1
E6	Disk File 2
F6	Disk File 3

See Figure 2 for address daughter board wiring.



ADDRESS DAUGHTER BOARDS

Strapped for Addresses:

Data Controller	B6
File 0	C6
File 1	D6
File 2	E6
File 3	F6

Figure 2. Address Daughter Boards

2.2 Format

Each disk track is divided into 24 sectors; each sector stores 256 eight bit bytes.

Each sector contains an address field and a data field. The address field is written and checked during a format pass; during normal operation, the address field from the disk is checked against address data from the computer and, if OK, data is transferred to or from the data field. See Figure 3.

2.3 Controller

The controller can be functionally divided into three parts: the computer interface (including address decoding), the file controls (which are concerned with file status and head position), and the data transfer portion (which is concerned with reading and writing).

2.3.1 Computer Interface. The computer interface is similar to a standard INTERDATA interface except that it responds to five different addresses, stores data as to the last file addressed, queues interrupts from any of the files or the data control, and responds with the proper interrupt address for the interrupt source.

2.3.2 File Controller. The file controller portion may be regarded as four separate controllers except that only one may be addressed at any one time. The file controller responds to a Sense Status instruction with the status of the file addressed; see Figure 4.

2.3.3 Seek. To cause a file to seek an address:

1) Sense status of the selector channel. If not busy,

2) Sense Status of the data transfer portion of the controller. If controller idle (DRL Bit 6) is one, controller is not busy. Then,

3) Sense Status of desired disk file. If Bit 3, File Address interlock, is one, loop until it goes to zero. See Data Transfer, Section 2.4. If all status bits are zero, with the possible exception of DRL Bit 0, Write Protect On, then,

4) Write Data to the desired file with the effective address containing the cylinder address desired. See Figure 4.

5) Then execute an Output Command to the file desired with the data format as shown in Figure 4. The heads should move to the desired cylinder.

6) If under interrupt control, see Section 2.6, Interrupt Control.

7) If not running under interrupt control, sense status of data control. When Controller Idle (DRL Bit 6) becomes one, the Seek has started, and the controller is no longer busy. A Seek or a Data Transfer may now be started on another disk file.

8) To determine when seek ends, after Controller Idle goes to one, sense status of the disk file in question. When Not RSRW goes to zero, the Seek is over. If Illegal Address or Seek Incomplete come on, see Section 2.7, Status and Error Flags. When seeking to the same address (no head motion). Not RSRW stays zero.

9) In a multiple disk file system, several or all files may be moving heads at the same time; each must be started separately, but as soon as Controller Idle on the data controller goes to one, but not more than 40 microseconds after the Output Command to the file, a Seek on another file may be started.

10) To restore a file to zero, follow the same procedure as in Seek, except the restore bit in the command should be one. If both Seek and Restore bits are one, Restore governs. Restore should be conditioned only on the file being ready. Restore is the method of clearing a Seek Incomplete, and Seek Incomplete removes RSRW.

11) If a file Output Command is given without Seek or Restore, this command will select the file addressed and may also set Disarm or Disable as specified. See Figure 4, and Section 2.6, Interrupt Control.

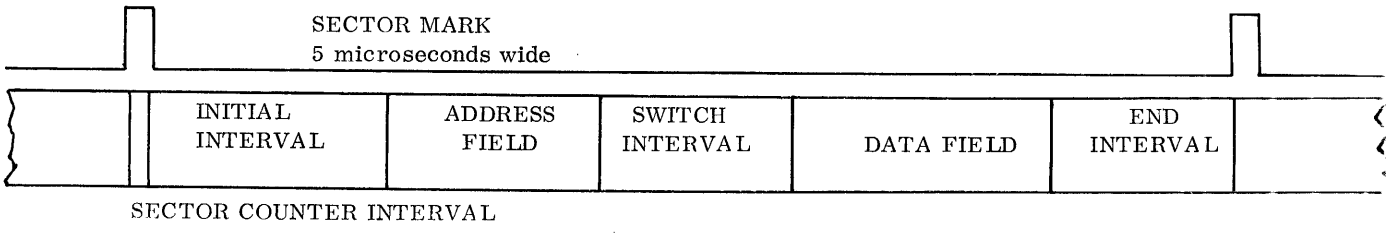


Figure 3. Fields Within a Sector

FILE CONTROL PORTION OF CONTROLLER

DAL/DRL BITS	0	1	2	3	4	5	6	7
OC TO FILE	DISABLE	ENABLE					SEEK	RE-STORE
WD TO FILE	128	CYLINDER ADDRESS 64	32	16	8	4	2	1
SS TO FILE	WRITE PROTECT STATUS	WRITE CHECK	ILLEGAL ADDRESS	FILE ADDRESS INTER-LOCK	NOT RSRW	EXAM	SEEK INC.	FILE NOT READY
SET EXAM		X	X	X				
INTERRUPT		X	X		X		X	X

Illegal Address, Seek INC, and File not Ready can interrupt when they go to one; not RSRW can interrupt when it goes to zero.

Figure 4. File Controller Commands

During a period starting at the Output Command Seek or Restore, and continuing for not more than 40 microseconds thereafter, any I/O Command addressed to the file controls will not be accepted and the Processor will generate a false Synch. During this time, the data controller will respond Controller Not Idle to a Sense Status Command. Therefore, to determine status of a disk file after starting a Seek or a Restore, either Sense Status of the data control section and wait for Control Idle before sensing status of the disk file, or sense status of the disk file twice, ignoring the first one. The time before a false Synch will completely cover the 40 microsecond period.

CAUTION

Do not attempt to Seek a file which is not ready to Seek, Read, or Write (RSRW), nor to Restore a file which is not ready. The controller will hang up under these conditions. The controller can be reset to initial conditions by using the command reset, which is DAL Bit 4, a one on an Output Command to the data controller section. A non-existant file will respond Not Ready and Not RSRW to a Sense Status Command. The caution applies to this case also.

If Status Bit 3, File Address Interlock, is a one, the file address will not change from its previous setting. If a different file is addressed during this time, the new address will not be accepted.

2.4 Data Transfer

The normal data transfer commands are Read, Read Check and Write. For the commands Read Format and Write Format, see Section 2.5, Formatting the Disk. Data is transferred to or from the disks in records. A record may be 1 byte up to 12,288 bytes long. Data is written on the disk in sectors, each of which holds 256 bytes. The Write or Read command specifies a sector address and head where data transfer is to begin. If more than one sector of data is to be transferred, the record is continued on the next sector. This extension continues up to the last sector of the track. If the head called for by the computer was head zero, the head will then switch to Head 1 and continue with Sector 0, Head 1. This process will continue, if necessary, through the sectors of Head 1. If data remains after the last sector, Head 1, data transfer will stop and a cylinder overflow error flag will be set. If data transfer began at Sector 0, Head 0, it may continue through all sectors of Head 0 and all sectors of Head 1, 48 sectors, 12,228 bytes. If data transfer began at Sector 23, Head 1, only one sector would be available; i.e. 256 bytes.

When transferring data it is assumed that the heads of the disk file of interest are at the proper cylinder; see Section 2.3.3, Seek.

To cause data transfer to occur:

1) Sense status of the Selector Channel control. If not busy, then

2) Reset the Selector Channel.

3) Sense status of the data control. If flag Controller Idle is a one, control is not busy, then,

4) Sense status of the file. If all status bits are zero, except for possibly the Write Protect flag, the file may be read from. If Write Protect is zero, the file may be written on.

5) Load the Selector Channel with initial and final address.

6) Write data to the file involved, giving the cylinder address. This operation selects the file and gives the controller the cylinder address it should find written on the disk.

7) Write data to the data control section, giving the sector address and the head. See Figure 5.

8) Output Command to the data control section, giving the operation required. The operation will begin. No data transfer will be requested for at least 90 microseconds, allowing time to,

9) Start the Selector Channel.

10) When the Selector Channel has ended, the disk controller may not have ended. If the amount of data transferred on the last sector was small, more than 1 ms may remain before the sector ends. If reading, the cyclic check will not be tested until the end of the sector. If writing, the controller will fill with the last byte received, and then write the cyclic check bytes. The Controller Idle Flag will go to one when the sector has ended and the controller is not busy. The error flags should be tested at this time.

11) When reading or writing, the sector counter is compared with the sector number from the computer. When the two are equal, reading begins. The address is read from the disk and compared with the address from the computer. If the addresses are equal, data transfer continues. If not equal, the address comparison failure flag is set, and data transfer stops. The head selected is checked against the head number from the disk. The defective track bit is tested and will set the defective track flag if a one.

12) The address is not tested again if the record is longer than one sector. However, the head and defective track flags are tested each sector, and will set the address comparison failure flag and defective track flags, respectively. These flags may be set at any sector, but especially at the first sector after a head switch.

13) Read check is identical to read except that no data transfer is involved, the Selector Channel is not used, and one sector only may be tested with one command. Data is read from the disk and the cyclic check is done. See Figure 6.

14) In order to permit access to the next sector on the same file after a Write or Read format operation is completed, the Controller Idle Flag goes to one while the last sector is still being filled with zeros. During this zero fill time, which continues until the next sector mark, if another file was to be addressed, the new file would be selected and writing would transfer to the new file. In order to prevent this from occurring, a new file address will not be accepted while the Write Gate is on. Write Gate On is indicated on File Status Bit 3, File Address Interlock. This bit sets Examine. Any I/O command addressed to a file while this bit is one will not change the file address, and thus will refer to the previously addressed file. Before any operation to a file, the status of that file should be tested. If Bit 3 is one, wait until it goes to zero, and then sense status of the new file. The time between the Controller Idle Flag setting and the File Address Interlock resetting should be about 160 microseconds for a 24 sector disk.

2.5 Formatting The Disk

2.5.1 Write Format. Formatting the disk involves writing the address headers at the beginning of each sector and then checking for bad spots on the disk using the Write Format and Read Format commands, with the format enable jumper on the data control card connected.

The data pattern should be 1 sector of 270 bytes. The following should be written in sequence:

1. The two address bytes. See Figure 7.
2. 8 bytes (4 half-words) of zeros.
3. 2 bytes (1 half-word). Hex '00'03'.
4. 258 bytes (129 half-words) of test pattern.

The controller will write the prefix (including the Synch bits) to the address field, but the code must write the gap (including Synch bits) between the address field and the data field. This is done by items 2 and 3 above. The controller will add the cyclic check at the end of the data field. The data field of Write Format is 2 bytes longer than the data field of normal write, so that the entire used portion of the sector may be checked for bad spots, allowing for variations in speed and timing.

NOTE

If Field 4 above is less than 258 bytes, the last byte written will be repeated to fill the field. If more than 258 bytes are written, the excess will continue into the next sector.

DATA TRANSFER SECTION OF CONTROLLER

DAL/DRL BITS	0	1	2	3	4	5	6	7	
OC to data					0	0	0	0	
					0	0	0	1	READ
					0	0	1	0	WRITE
					0	0	1	1	READ BACK CHECK
					0	1	0	1	READ FORMAT
					0	1	1	0	WRITE FORMAT
					1	0	0	0	COMMAND RESET
WD to data controller			HEAD			SECTOR ADDRESS			
	0	0	1	16	8	4	2	1	
RD to data controller CONTROLLER IDLE			CONTENTS OF SECTOR COUNTER						
	0	0	0	16	8	4	2	1	
RD to data controller CONTROLLER BUSY			DATA						

SS to data controller	OVERRUN	ADR CMP FAIL	DEF TRACK	CYL OVERFLOW	BUSY (not data req.)	EXAM	CONTROLLER IDLE	CYC CK ERROR OR WR. PROT. VIOLATION
SETS EXAMINE	X	X	X	X				
CAUSES SELCH TO INTERRUPT	X	X	X	X		X	X	X
CAUSES INTERRUPT AT END OF DATA TRANSFER							X	

Figure 5. Data Transfer Commands

2.5.2 Format Check The Read Format Command may be used to check for proper addresses and for bad spots. The Read Format Command will read 270 bytes, which should be identical with the pattern described in Write Format above. The cyclic check is operative during Read Format and may be tested.

NOTE

Using Read Format after normal Write may give unforseeable results. Normal Read after Write Format, without normal Write in between, may give cyclic check errors.

2.6 Interrupt Control

The disk files and controller may be operated under Interrupt Control.

2.6.1 File Interrupt. Each file may be enabled and armed independently. If the file is addressed with an Output Command, DAL Bits 0 and 1 control these functions as follows:

DAL BITS 0	1	FUNCTION
0	0	No change
0	1	Enable, Arm
1	0	Disable, Arm
1	1	Disable, Disarm

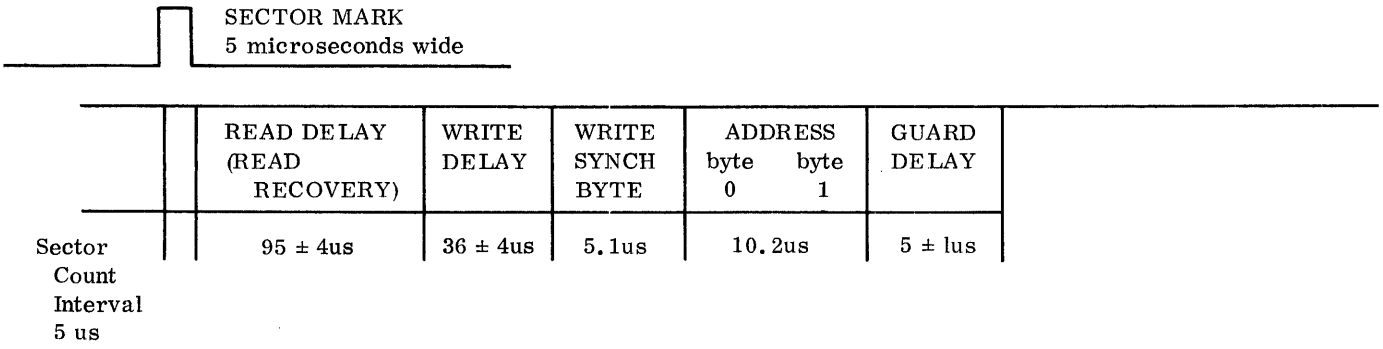


Figure 6. Sector Timing

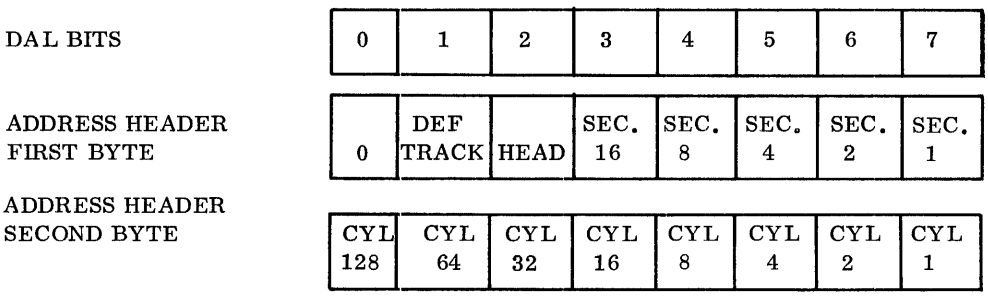


Figure 7. Address Header

Where Enable permits an interrupt Attention, Disable prevents an interrupt Attention; Arm permits queuing interrupt requests, Disarm prevents queuing interrupt requests.

Thus, Arm and Enable enable the interrupt for the file, Disable and Disarm prevent interrupts from the file, and Disable and Arm prevent interrupts, but allow storage of interrupt requests in the Queue flip-flop.

Each file has its own Disable and Disarm storage. Each file and the data controller has its own queue flip-flop.

If the I/O Interrupt System is enabled (by setting the proper bit in the PSW) and a particular file is enabled and armed, an interrupt will occur when:

1. Seek is completed (normal completion), Illegal address (logical address interlock), or Seek incomplete.
2. The file goes ready
   or
3. The file goes not ready.

The Acknowledge Interrupt Command will return the status and address of the file interrupting.

2.6.2 Data Interrupt. The data control section will interrupt if the I/O Interrupt System is on and a data transfer operation is complete; at this time the Controller Idle flag goes to one, which is at the end of the last sector included in the operation. Note that errors will terminate the Selector Channel, and the Selector Channel will then interrupt.

2.6.3 Interrupt Priority. This controller contains a built-in priority for disk interrupts. The order of priority is:

Data Control
File 0
File 1
File 2
File 3

with data control having the highest priority and File 3 the lowest.

The disk controller priority depends on the controller location in the RACKO-TACKO chain.

2.7 Status And Error Flags

2.7.1 File Position Control When sensing status of a file, certain status bits are returned. These status bits are:

Write Protect - DRL Bit 0:

This bit indicates that the file addressed is in the Write Protect condition and writing is not possible unless the Write Protect Button on the file is pressed. This is not an error and does not appear on Examine, nor does it cause an interrupt.

Write Check - DRL Bit 1:

Write check can be caused by two conditions:

1) Improper head selection - two heads or no heads selected. This is a file hardware fault, and cannot be corrected by software. This fault prevents writing.
2) Low DC voltage.

This flag set also sets Examine and can cause an interrupt.

Illegal Address - DRL Bit 2:

If the track address called for at a Seek or Restore operation is greater than 202, no Seek occurs (Restore will occur if commanded) and an illegal address signal is generated. This signal will be cleared by the next legal Seek or Restore command. This flag sets Examine and can interrupt.

File Address Interlock - DRL Bit 3:

This bit is one while Write Gate is on. During this time, file selection cannot be changed. If a Sense Status command shows that this bit is set and if this command addresses a different file than the last file I/O command, then the file selection may not have changed. Wait until Bit 3 goes to zero, then test the state of the new file. See Section 2.4, Data Transfer.

Not Ready to Seek, Read, or Write (Not RSRW) - DRL Bit 4:

This bit is zero if the file is ready to Seek, Read, or Write. It is one during Seek or Restore, and its return to zero indicates the end of the Seek or Restore. It does not change during Reading or Writing. This bit must be zero before Seeking, Reading, or Writing. It need not be zero before restoring (see Seek incomplete below). This flag can interrupt when the file goes ready to SRW, whether the particular file is the selected file or not. This interrupt signifies end of Seek or Restore, or file going ready.

Examine - DRL Bit 5:

This bit is present if either Write Check or Illegal Address or File Address Interlock is set.

Seek Incomplete - DRL Bit 6:

This bit is present if the file is unable to complete a Seek, probably because it hit the head motion stops. The file's internal address register is probably out of step with the head. The only cure is to Restore, which will reset both the head and register to zero. Seek Incomplete can interrupt.

File Not Ready - DRL Bit 7:

A file is not ready if it is not in the run state with a disk cartridge loaded and initial sequence completed. This flag repeats the Ready light on the file. A non-existant file will respond Not Ready to a Sense Status command. An interrupt will occur on the edge of this flag going Not Ready if the interrupt is enabled.

2.7.2 Data Transfer Control Read data from the data control section while the controller is idle will give the contents of the sector counter of the file selected.

CAUTION

It is possible to test while the counter is changing, in which case the readings may not be correct.

The Sense Status command to the data controller gives the status bits as follows:

Overrun - DRL Bit 0:

This flag is set if no sector compare has occurred within 2 disk revolutions of a data transfer command. Probably a non-existant sector was called for (sector number too large). This flag sets examine and can interrupt.

Address Compare Fail - DRL Bit 1:

This flag is set if, during Read or Write, the address header from the disk does not agree with the data from the computer. This flag may also be set if the head comparison bit is set. The complete address is checked before the first sector of a record; only the head bit is checked before the other sectors of a multi-sector record. This bit sets Examine and can interrupt.

Defective Track - DRL Bit 2:

If the defective track bit in the disk address header is a one, this flag will be set. This bit is tested at the beginning of each sector. This flag sets examine and can interrupt.

Cylinder Overflow - DRL Bit 3:

This flag is set if the Selector Channel has more data to transfer at the end of a cylinder, that is, after the last sector, Head 1. This flag sets Examine and can interrupt.

Busy - DRL Bit 4:

This bit is used only by the Selector Channel. This signal is called Data Request within the controller. Programmers should ignore this bit.

Examine - DRL Bit 5:

This bit is one if the Overrun, Address Compare Fail, Defective track, or Cylinder Overflow flag is set.

Controller Idle - DRL Bit 6:

This flag is one if the controller is not busy. This flag is zero if the controller is busy, either transferring data or setting up a Seek or Restore. An interrupt can occur when this flag goes to one as a result of ending a data transfer.

Cyclic Check Error or Write Protect Violation - DRL Bit 7:

This flag will be set if, during a Read, Read Check, or Read Format operation, a cyclic check error is detected at the end of any sector. This flag will be set during a Write or Write Format operation if the Write Protect bit is one.

NOTE

For detailed programming information, see 02-222A22.

2.8 Mnemonics

The following is a list of the mnemonics used in the Disk Controller. A brief description and the B32-189B08 schematic source of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC SHEET
ACMPF	Address Compare Failure	8F4
ADCMP	Address Compare	8K5
ADRS	Address (From 01-013D08, Sheet 2, Processor)	2A1
ADSY	Address Synch	1S4
AG	Address Gated (Interrupt Address)	2M1-2M6
ARDCM	Address Read Complete	8L1
ARDGT	Address Read Gate	8J1
AS 0-7	Address Source	1J1-1J4
ATEN	Attention	5H1
B 1-4	Bit Counter, Bit 1-4	6D6-6D7
BIT 3	Bit Counter = 3	6C7
BIT 7	Bit Counter = 7	6B6
BUSY	Busy (D or F Board Busy)	3E1
BY269	Byte Counter = 269	6A5
BYEND	Byte End (Signals end of data transfer for current sector)	6A1
CBSY	Controller Busy (D Board Busy)	7E1
CKCY	Cyclic Check	9E1
CKDA	Check Data	10S4
CMD	Command (From 01-013D08, Sheet 2, Processor)	2A5

MNEMONIC	MEANING	SCHEMATIC SHEET
CMP 1	Compare Byte 1	8K1
CMPCL	Completed or General Clear	6M1
CNT 5	Control 5 (A Format Command)	6K1
CNTAD	Controller Addressed	1S3
CNTCM	Controller Command	1S7
CNTDR	Controller Data Request	1S8
CNTDT	Controller Data Transfer	1S6
CNTSR	Controller Status Request	1S7
CONT	Continue (Multiple Sector Data Transfer)	6R1
CRD	Combined Read Command (Read Check + Read)	6J1
CTLGT	Control Gate	1S3
CYER	Cyclic Check Error	8S1
CYLOF	Cylinder Overflow	8E4
CYOUT	Cyclic (Check Register Serial) out	8N1
DA	Data Available (From 01-013D08, Sheet 2, Processor)	2A4
DADRS	Delayed Address	2F1
DAL	Data Available Lines (From 01-013D08, Sheet 1 Processor)	1A1-1A3
DDGRK	Double Delayed Gated RAKO	5J1
DFTRK	Defective Track	8F4
DIR 0-7	Data Input Register Bits 0-7	Sheet 10
DOR 0-7	Data Output Register Bits 0-7	Sheet 10
DOROT	Data Output Register Out	10S2
DRBCG	Data Read Bit Counter Gate	9B1
DRDGT	Data Read Gate	9A1
DR	Data Request (From 01-013D08, Sheet 2, Processor)	2A4
DRL 0-7	Data Request Lines 0-7	2S1-2S6
DSCON	Display Connector	2L2
DSARM	Interrupt Disarm, File 0-3	5C1-5G1
DTARQ	Data Request (to SELCH)	6S1

MNEMONIC	MEANING	SCHEMATIC SHEET
DTST	Data Start (Start Read or Write after Address Compare in Normal Mode)	9A1
ENBL 0-3	Interrupt Enable, File 0-3	5C1-5G1
ENCY	Enable (Write) Cyclic (Check)	9J1
ENDTA	Enable (Write) Data	9J1
ENSYN	Enable (Write) Synch	9H1
EXAM	Examine	2M4 and 8A1
FA 0, 1	File Address (File Currently Selected)	5A4-5B4
FLAD	File Addressed	1S4
FLSEL 0-3	File Selected 0-3 (to File)	3G6-3H6
FRSRW	File Ready to Seek, Read or Write (Selected File)	2S7, 3K1-3M1
GCLR	General Clear	2E2
GCMD	Gated Command	2E5
GDA	Gated Data Available	2E4
GDR	Gated Data Request	2E5
GSR	Gated Status Request	2E4
HD	Head 1 Selected	6M1
HDSEL	Head Select	7K1
IA 0-3	Illegal Address, File 0-3	4K1-4N1
IAD 1, 2	Interrupt Address 1, 2	5R1
IDXST	Index Pulse Store	7F1
INAKC	Interrupt Acknowledge Controller	5K1
INAKF 0-3	Interrupt Acknowledge File 0-3	5L1-5N1
INDTA	In Data	9F1
INDX	Index Mark	7K6
IXSMC	Index + Sector Mark + Continue	6N1
LOD 1-4	Logical Address	1D2-1D3
LSTBY	Last Byte	9H1
NTRQC	Interrupt Request from Data Controller	7E1
NTRQF 0-3	Interrupt Request, File 0-3	4A1-4G1
OPCMP	Operation Completed	6N1

MNEMONIC	MEANING	SCHEMATIC SHEET
OPEND	Operation End	6N1
RACK	Receive Acknowledge (From 01-013D08, Sheet 6, Processor)	5H8
RCBCT	Read Count Bit Counter	8K1
RDAD	Read With Address (Read Format Command)	6K1
RDCK	Read/Check Command	6J4
RDCLK	Read Clock	7N6
RDGT	Read Gate	9B1
RDEND	Read End	9E1
RDTA	Read Data	7R8
RDTAC	Read Data Control	9C1
RDWT	Read or Write (Command) (Read Check + Read + Write)	6J8
RLDDO	Read Load Data Output Register	9C1
RSTR	Restore (to File)	3B1
SCCMP	Sector Compare	7C1
SCLR	System Clear (From 01-013D08, Sheet 2, Processor)	2A2
SEC 1-16	Sector Counter Bits 1-16	7A8-7C8, 7L8-7N8
SECLR	Sector Mark + Operation Completed + General Clear	7G1
SHDIR	Shift Data Input Register	9B1
SM	Sector Mark	7J6
SMCLR	Sector Mark + General Clear	7G1
SR	Status Request (From 01-013D08, Sheet 2, Processor)	2A4
STCLR	Start or General Clear	7G1
STRB	Strobe (Address Strobe) (to File)	3B1
SYNBK	Synch Block	7H1
SYNDT	Synch (Character) Detected	8M1
SYNO	SYNC to Computer	2F8
TA 1-128	Track Address 1-128	7M1-7S1
TACK	Transmit Acknowledge	5H1
WAWAD	Write and Write with Address (Write and Write Format Command)	6K1
WCBCT	Write Count Bit Counter	9L1

MNEMONIC	MEANING	SCHEMATIC SHEET
WCKDT	Write Clock and Data	9N1
WCYCK	Write Clock	9N1
WLDOR	Write Load Data Output Register	9G1
WLSBY	Write Last Byte	9J1
WT	Write (Command)	6J1
WTAD	Write with Address (Write Format Command)	6K1
WTDAC	Write Data and Clock	7M1
WTDLY	Write Delay	9G1
WTDTA	Write Data	9M1
WTED	Write End	9K1
WTGT	Write Gate	2G3
WTOSC	Write Oscillator	1G7
WTST	Write Start	9G6
Y 1-Y256	Byte Counter Bits	6D1-6D6

CARTRIDGE DISC PROGRAMMING SPECIFICATION

1. INTRODUCTION

The INTERDATA Removable Cartridge Disc System (Product Numbers M07-735 and M07-736) provides a random access, removable media, rotating memory, storage facility for the family of INTERDATA computers. The system consists of a single Controller which can handle up to four disc drives.

Data is recorded in a fixed-sector format, where each sector contains 256 data bytes. Data transfers are under control of a Selector Channel and can be from 1 to 12,288 bytes since the Controller permits data transfer across sector and head boundaries. Simultaneous seek and overlapping seek/data transfers are permitted in multiple disc systems.

Table 1 summarizes specifications pertinent to programming the system.

TABLE 1. DISC SYSTEM SPECIFICATIONS

DATA STORAGE CHARACTERISTICS:	
Uses IBM 2315-type cartridges, double frequency recording at 2200 bits per inch and 100 tracks per inch.	
MAXIMUM TRANSFER RATE:	180K bytes per second
START-UP TIME:	1 minute
ACCESS TIME:	
Average Latency	20 milliseconds
Maximum Latency	40 milliseconds
*Average Head Positioning	70 milliseconds
*Maximum Head Positioning	150 milliseconds
*Maximum Between Adjacent Tracks	15 milliseconds
Maximum Restore Time	≤ 1.75 seconds
CAPACITY:	
Sector	256 data bytes
Track	6,144 data bytes
Cylinder	12,288 data bytes
FORMAT:	
Sectors Per Track	24
Tracks Per Cylinder	2
Cylinders Per Cartridge	203
Tracks Per Cartridge	406
PARITY:	Halfword odd longitudinal parity
WRITE PROTECT (OPTIONAL):	Protects full cartridge

*Includes head-settling time.

2. CONFIGURATION

The Removable Cartridge Disc System must operate through a Selector Channel. The Selector Channel must be assigned a high priority on the memory bus to insure that the 180K byte transfer rate can be maintained.

3. OPERATING PROCEDURES

The Disc provides the following switches and indicators.

LOAD/RUN Switch - This two position switch is located at the left of the front panel. In the LOAD position, the drive is not operating, the door may be opened, and cartridges may be loaded or unloaded.

When the switch is moved to the RUN position, the drive begins its start-up cycle which lasts for approximately one minute. Checks are made to insure that the door is closed and locked, a cartridge is in place, and that the correct spindle speed has been reached. After one minute has elapsed and the checks are completed successfully, the drive is ready for operation.

LOAD - This lamp lights to indicate that the drive is ready to load or unload cartridges; that the spindle has stopped turning, that the heads are positioned away from the disc surface, and that the door is unlocked. The LOAD lamp goes off when the LOAD/RUN switch is moved to the RUN position.

READY - This lamp lights when the drive is ready to receive commands. This lamp goes on at the same time the File Ready line goes "true". The lamp goes out when the LOAD/RUN switch is moved to the LOAD position.

CHECK - This lamp indicates the same status as the Write CHK status, except for the temporary voltage fluctuation condition. The Write Check is reset by moving the LOAD/RUN switch to LOAD, then back to RUN.

POWER - This lamp indicates that power is available to the drive. When power is not available, the door is locked and a flag is imposed between the door and the cartridge receiver. This prevents inadvertent loading or unloading of cartridges in an unpowered condition.

NOTE

When the Write Protect Option is installed, the POWER lamp is replaced by the PROTECT indicating switch. In this case, the operator may observe whether power is available by viewing the other three lamps. One of these is always lit, except during cycle-up and cycle-down operations.

WRITE PROTECT - When installed, the Write Protect Option enables the operator to protect a cartridge against inadvertent write operations. He does this through the operation of the LOAD/RUN switch and the PROTECT switch. The PROTECT switch is also an indicating lamp.

The Write Protect function is automatically set during each cycle-up (each time the LOAD/RUN switch is moved into the RUN position). To allow writing on a disc after a cycle-up, the operator must momentarily depress the PROTECT switch. This extinguishes the lamp and sets the Write Protect Status line. The operator may reset the Write Protect by moving the LOAD/RUN switch to LOAD, then immediately back to RUN.

4. DATA FORMAT

4.1 Disc Format

The disc is segmented into 24 sectors per track. Each sector contains a two byte header field and a 256 byte data field followed by a two byte longitudinal parity field. See Figure 1. The number of bytes in a data transfer is not limited to sector or track boundaries. Therefore, as few as one byte and as many as 12,288 bytes may be transferred at one time. However, the disc continues the Write or Read operation until a complete sector is encountered, even if a complete sector is not specified. In a Write operation, the sector is "filled" with the last data byte specified. In the Read Mode, the number of bytes that were specified are read into the Selector Channel and the SELCH interrupts when this is complete, but the Controller continues reading until the sector boundary is reached. At this time, the user may interrogate the Controller status to verify that the data transfer was error free.

The header field in Figure 1 is not normally written or read. It is used when formatting the disc. A disc format program is run on each disc to insure the integrity of the disc. This is normally performed by commanding the Controller into the Write Format Mode and then writing a worse case pattern (or patterns) into the complete sector including header and data fields. The program then commands the Controller into the Read Format Mode and reads the sector. If the data compares, the user may then write the correct address into the header field with the DEF TRK bit = 0 and continue to the next sector. If the data does not compare, the user may choose to do a more complete surface analysis and, based on the results, program the DEF TRK bit to a 1 or 0. The user can access the header field by programming the FORMAT Mode and also by operating the FORMAT switch in the Controller. The hardware uses the header field for two purposes: to inhibit data transfers on tracks which are flagged as defective and to guard against attempted transfers where the heads are not properly positioned.

To increase system throughput (minimize head-positioning time), refer to Figure 1, which shows the physical layout of data on the disc.

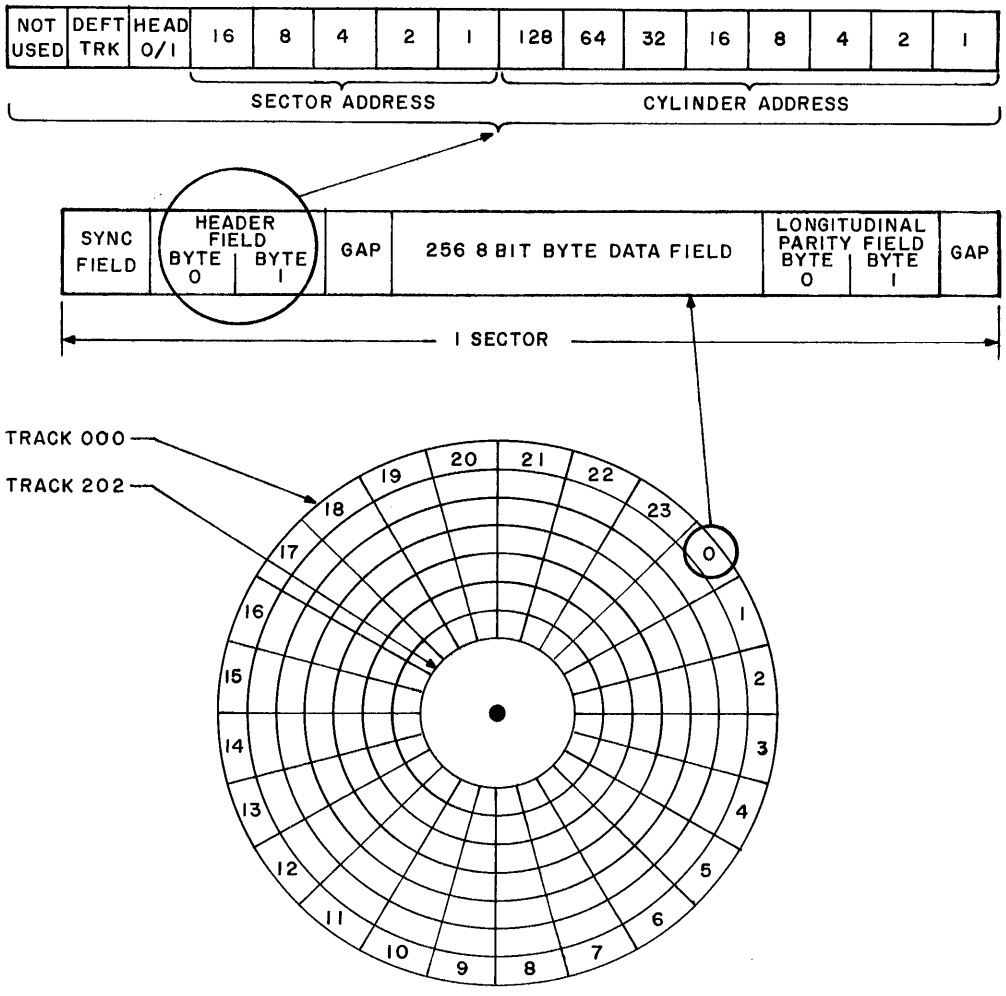


Figure 1. Removable Cartridge Disk Format

4.2 Disc Test/Format

Each cartridge supplied by INTERDATA is tested to ensure the integrity of the disc surface. The Disc Test/Format Program performs this qualification. The following defines the characteristics of the program and defines a defective track.

Figure 2 shows the data format for a sector.

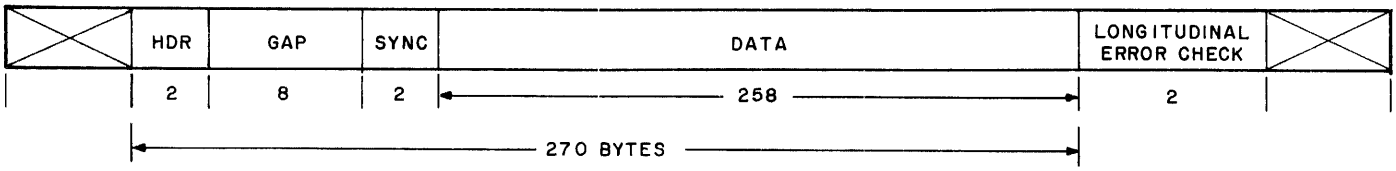


Figure 2. Sector Format (For Format Mode Only)

In the Format Mode, the program will Write/Read the 270 bytes in the sequence shown. Note that the data field in this case is 258 bytes. This permits testing the field which contains the Longitudinal Parity bytes in the normal data mode. For this reason, the sequence Normal Write/Read Format or Write Format/Normal Read generally produces Longitudinal Parity errors and/or bad data.

The Format Program Writes a prescribed pattern, reads it back a specified number of times and verifies that the data is correct and that there are no Longitudinal Parity errors. If there are no errors on any of the read operations, the program writes the header with the correct address with the DEF TRK bit=0.

If a data or Longitudinal Parity error is detected on any of the read operations, the program will set DEF TRK=1. Using this method, each disc cartridge supplied by INTERDATA is specified to have 400 of its 406 tracks error-free.

5. PROGRAMMING INSTRUCTIONS

5.1 Processor Instructions

Data transfers to and from the Disc are accomplished via the Selector Channel; but the Processor I/O instructions are used to communicate with the Disc, Controller, and SELCH. The following is a brief description of each of these instructions.

SENSE STATUS (SS OR SSR) - Used to interrogate the Disc and Controller to insure that data transfers are complete and correct. It may also be used to determine if the Selector Channel is busy.

OUTPUT COMMAND (OC OR OCR) - Used to control Disc operations and to set up the desired mode of operation and to initialize and set up the SELCH.

WRITE DATA (WD OR WDR) - Loads the Cylinder Address, Sector Address, and Head Number in the Controller and to load the SELCH Address Registers.

READ DATA (RD OR RDR) - Used to determine the current rotational position of an addressed Disc and to interrogate the Address Register in the SELCH to determine if a data transfer terminated correctly.

ACKNOWLEDGE INTERRUPT (AI OR AIR) - Used to service the Controller and SELCH interrupts. It also returns the interrupting device number.

The Controller and each disc have a separate address. This is a strap option which can be altered with a minor wiring modification. The Controller is always the lowest address. The Disc addresses follow in sequence by adding one to the most significant hexadecimal digit. The standard addresses are:

X'B6'	CONTROLLER
X'C6'	DISC 0
X'D6'	DISC 1
X'E6'	DISC 2
X'F6'	DISC 3

5.2 Controller Command, Status, and Data Bytes (Table 2)

TABLE 2. CONTROLLER COMMAND, STATUS, AND DATA BYTES

INST BIT	0	1	2	3	4	5	6	7	
CMD	X	X	X	X	0	0	0	1	READ
	X	X	X	X	0	0	1	0	WRITE
	X	X	X	X	0	0	1	1	READ CHECK
	X	X	X	X	0	1	0	1	READ FORMAT
	X	X	X	X	0	1	1	0	WRITE FORMAT
	X	X	0	0	1	0	0	0	RESET
WD	X	X	HEAD 0/1	SECT 16	SECT 8	SECT 4	SECT 2	SECT 1	
RD (CONTROLLER IDLE)	0	0	0	SECT 16	SECT 8	SECT 4	SECT 2	SECT 1	
SS	OVER-RUN	ADDR COMP FAIL	DEF TRK	CYL OV	BSY	EX	CONT IDLE	LONGITUDINAL PARITY ERROR WPV	
RD (CONTROLLER NOT IDLE)	DATA 0	DATA 1	DATA 2	DATA 3	DATA 4	DATA 5	DATA 6	DATA 7	See Note 1.

X=DON'T CARE

Note 1. This RD is generated by SELCH hardware. The programmer should not write RD while CONTROLLER NOT IDLE.

CONTROLLER COMMAND DEFINITIONS

The Controller contains interrupt circuits which are always enabled, therefore, the standard Enable/Disable Command bits are not used.

READ — Enables the Controller to perform a normal data read. The Selector Channel must be set up prior to the Command, the heads must be positioned and the Sector Address loaded in the Controller. The data transfer from the Controller will delay for at least 90 microseconds after a sector match. The Selector Channel must be started before this time. If the last sector read is not a complete sector, the Selector Channel will terminate after the last byte is read into core but the Controller will continue reading until the Longitudinal Parity Error is verified, then set CONT IDLE.

WRITE — Enables the Controller to perform a normal Data Write. The Selector Channel must be set up prior to the Command, the heads must be positioned and the Sector Address must be loaded in the Controller. Data transfer to the Controller will delay for at least 90 microseconds after a sector match. The Selector Channel must be started before this time. If the last sector written is not a complete sector, the Selector Channel terminates after the last data byte is written, but the Controller continues and fills the remainder of the sector with the last data byte, writes the Longitudinal Parity Error, and then sets CONT IDLE.

READ CHECK — Causes the Controller to perform an off-line Read of a single sector. The Selector Channel is not used but the heads must be positioned and the Sector Address must be loaded before this Command is issued. While in the READ CHECK Mode, no data is passed to the Selector Channel, but the interface cannot be used until this mode is terminated (Controller Idle=1). The OVERRUN, ADDR COMP FAIL, DEF TRK, CONT IDLE, and LONGITUDINAL PARITY ERROR status bits have the same meaning as in the normal Read. An interrupt will be generated when the READ CHECK is completed (CONT IDLE → 1).

WRITE FORMAT — This command, together with the FORMAT switch in the Controller ON, permits writing into the header field of the sector. This is normally used only when performing a surface analysis of a new cartridge. Normally, 270_{10} bytes are written in the FORMAT Mode. This includes the synch field, header field, gap, data field, and longitudinal parity error field in that order. See Figure 2 and refer to Section 4.2 for a complete discussion of the FORMAT Mode.

READ FORMAT — This command, together with the FORMAT switch in the Controller ON, permits reading from the header field of the sector. This is normally used only when performing a surface analysis of a new cartridge. Figure 2 and Section 4.2 show the details for the FORMAT Mode.

RESET — This command disarms all the files, resets the Attention flip-flop, Mode flip-flop, Head Select flip-flop, Data Input Register, OVERRUN, ADDR COMP FAIL, DEF TRK, CYL OV, LONGITUDINAL PARITY ERROR and WPV and sets CONT IDLE, and Controller BUSY. In addition, it terminates any data transfers in progress and inhibits writing. This command does not affect a SEEK in progress. This command is normally required to reset status bits.

CONTROLLER READ DATA DEFINITION

This read data must be issued when CONT IDLE=1 and causes the Sector Byte of the previously selected disc to be returned to the Processor. This sector byte may be changing at the time of the RD. For this reason, it is necessary to issue consecutive RDs and verify that the bytes are the same; if not, it will be necessary to issue another RD.

CONTROLLER WRITE DATA DEFINITION

This byte represents the starting sector and head address for a data transfer and must be loaded before every data transfer. Sector Addresses between zero and 23_{10} only, are valid. Any out-of-range sector address will result in an OVERRUN status.

CONTROLLER STATUS DEFINITIONS

OVERRUN — This status bit is active if the sector address (set up by the WD), does not compare with any sector address from the selected disc. This bit is active after two revolutions of the disc when a sector match is not found and sets EX to generate a SELCH interrupt. When OVERRUN→1, CONT IDLE will be zero and will remain zero until INITIALIZE is depressed or a Command RESET is issued. These conditions also reset OVERRUN. OVERRUN occurs as a result of the program selecting a sector address $> 23_{10}$, or for certain hardware malfunctions.

ADDRESS COMPARE FAILURE — This status bit is set only in the normal READ, normal WRITE, or READ CHECK Modes if the CYLINDER ADDRESS, head and sector bytes from the Processor do not agree with the cylinder address, head and sector read from the header. (See Figure 1.) The cylinder address and sector are only tested on the first sector of a record. The Head bit, however, is tested on each sector of a record. ADDRESS COMPARE FAILURE will cause the READ/WRITE/READ CHECK to abort (no further data transfers will occur). EX is set and an interrupt is generated when this bit gets set. This bit is reset by INITIALIZE or a command to the Controller.

DEF TRK — This status bit is set only in the normal READ, normal WRITE, or READ CHECK Modes when a data transfer is attempted on a sector which is flagged as defective (DEF TRK bit in the header field is set). The data transfer is aborted and DEF TRK sets EX and generates a SELCH interrupt. This bit is reset by INITIALIZE or by a Command to the Controller. This bit is tested on each sector of a record.

CYL OV — Cylinder Overflow is set when a data transfer is attempted across a cylinder boundary (Head 1, Sector 23). CYL OV will set EX and generate a SELCH interrupt. CYL OV is reset by INITIALIZE or a Command to the Controller. In the latter case, CYL OV is reset while CONT IDLE is being set.

BSY — This status bit is only used by the SELCH and should be ignored by Programmers.

EX — EXAMINE will be active while any of the following bits are set: OVERRUN + ADDR COMP FAIL + DEF TRK + CYL OV. EX, when set, causes a SELCH interrupt.

CONTROLLER IDLE

This bit will be zero when a command is sent to the Controller or when Seek or Restore command is being initiated on a disc. It is set when the operation is complete, or by INITIALIZE, or by COMMAND RESET. In the case of Seek or Restore, it will be reset for approximately 40 microseconds after receipt of the command.

CYL CHK/WPV

This status bit has a separate meaning for Read or Write data transfers:

A. READ OPERATION

If the Controller is in the READ, READ FORMAT, or READ CHECK Mode, this bit is set if a Longitudinal Parity Error occurs. For multi-sector Read Operations, this bit may be set at the end of any sector. In the case of a partial sector Read operation, the SELCH interrupts after the last byte is read from the disc, but the Controller continues reading until the end of sector and sets CONT IDLE. If this sector has a Longitudinal Parity Error, this status bit is set before CONT IDLE→1. This status bit is reset by INITIALIZE or a command to the Controller.

B. WRITE PROTECT VIOLATION (WPV)

If the Controller is in the WRITE or WRITE FORMAT Mode, this bit is set when a WRITE PROTECTed disc is addressed and the Controller is commanded to the WRITE or WRITE FORMAT Mode. This bit, when set, will cause a SELCH interrupt. This status bit can only be reset by manually removing the WRITE PROTECT condition (see Section 3) or by issuing a command to the Controller which does not specify WRITE or WRITE FORMAT. WRITE PROTECT is optional on each physical disc. If this option is not provided, the WPV status is forced to zero. Any Read operation is performed normally on a Write Protected disc. Note that each disc has a separate status byte which includes a bit to indicate that the disc is or is not Write Protected.

5.2 Disc Command, Status and Data Bytes (Table 3)

TABLE 3. DISC COMMAND, STATUS, AND DATA BYTES

BITS INST	0	1	2	3	4	5	6	7	
CMD	DIS	EN	X	X	X	X	SEEK	RESTORE	
WD	128	64	32	16	8	4	2	1	CYLINDER ADDRESS
SS	WRT PROT	WRT CHK	ILL ADDR	DISC ADDR INTLK	$\overline{\text{RSRW}}$	EX	SEEK INC	$\overline{\text{DISC}}$ READY	

The Command, Status, and Data Bytes in Table 3 are valid for each disc. If a Command is directed to an unequipped disc, the hardware will respond as if the disc was equipped, i.e., a False Synch will not result. If the Command specifies SEEK or RESTORE, the Controller will lock up waiting for control signals from a non-existent disc. In this case, it is necessary to issue a Controller Command RESET.

If a Write Data is directed to an unequipped disc, the hardware responds as if the disc was equipped.

If a Sense Status is directed to an unequipped disc, the returned status byte is X'09'.

DISC COMMAND DEFINITIONS

DISABLE/ENABLE

The bits control the Enable/Disable/Disarm functions as follows:

BIT NUMBER 0 1

1 1 DISARM - Interrupts are not queued.

1 0 DISABLE - Interrupts are queued, but not passed to the Processor.

0 1 ENABLE - Interrupts are passed to the Processor as they occur.

0 0 NO CHANGE

SEEK

This command is used to reposition the heads to a different cylinder. The user must issue a WD CYL ADDR prior to issuing a Command SEEK. The status bits SEEK INC, RSRW and DISC ADDR INTLK must be inactive (0) before issuing a SEEK. The success or failure of a SEEK will be reflected in the RSRW and SEEK INC status bits. When attempting consecutive SEEKs to more than one drive, the user must Sense Status of CONT IDLE and wait for CONT IDLE →1 (no interrupt will be generated in this case). After issuing a SEEK to the first disc, it will take approximately 40 microseconds for CONT IDLE →1.

RESTORE

This command causes the heads to move to Cylinder 000. A WD CYL ADDR, with a data byte of zero, must be issued prior to the RESTORE. Failure to do this may result in ILL ADDR status. A command RESTORE is required to clear the SEEK INC status. The RSRW need not be zero before issuing this command, but while a RESTORE is in progress, RSRW will be active. DISC ADDR INTLK must be zero before issuing a RESTORE. Worst case RESTORE time is 1.75 seconds.

DISC WRITE DATA DEFINITION

This Write Data is used to load the Cylinder Address prior to a SEEK or RESTORE. A Cylinder Address of 000 to 202_{10} is valid. Cylinder 000 is at the outer periphery of the disc and 202 is at the inner periphery. An out-of-range Cylinder Address will result in ILL ADDR when a SEEK or RESTORE is attempted.

DISC STATUS DEFINITIONS (VALID ONLY WHEN CONT IDLE=1)

WRT PROT

If the Write Protect option is equipped and activated (as indicated by the PROTECT lamp on the disc being ON), this status bit is active. This status bit should be tested before attempting a WRITE or WRITE FORMAT operation. See Section 3 for WRITE PROTECT manual controls.

WRT CHK

This status bit is active if the disc hardware detects a fault which would affect reliable WRITE operations. This fault can be improper hardware head selection or DC voltages out of specification. A permanent fault will latch WRT CHK and also activate DISC READY to generate an interrupt. A voltage fluctuation can cause this bit to become momentarily active. If this bit is permanently active, the disc must be shut down to determine the fault. No software recovery is possible.

ILL ADDR

This status bit is active when a SEEK or RESTORE is attempted to an out-of-range cylinder address. If a SEEK is attempted to an out-of-range address, the SEEK will not occur. If a RESTORE is attempted to an out-of-range address, the operation will continue normally. ILL ADDR is only reset by a legal (in-range) SEEK or a RESTORE.

DISC ADDR INTLK

This bit is active when the disc is in the WRITE/WRITE FORMAT Mode and is in the process of Writing or tunnel erase. This bit is active for approximately 160 microseconds after CONT IDLE →1 at the termination of a WRITE/WRITE FORMAT. At the termination of the above operation, the user must verify that DISC ADDR INTLK →0 before addressing any other disc. It also sets EX.

$\overline{\text{RSRW}}$

Not Ready to Seek Read or Write - This bit is active while the heads are being repositioned as a result of a SEEK or RESTORE. This bit must be inactive before a SEEK, Read or Write. When this status bit goes inactive a Read or Write may be performed. Note that if a SEEK is attempted to the present cylinder address, RSRW will not become active but an interrupt will be generated.

EX=WRT CHK + ILL ADDR + DISC ADDR INTLK

SEEK INC

This bit becomes active if the disc is unable to complete a SEEK operation. This is probably a hardware fault and can only be cleared by a RESTORE. When SEEK INC goes active, RSRW will also be active and will also be cleared by RESTORE.

DISC $\overline{\text{READY}}$

Active if disc is not operational, i.e., power not applied, cartridge not loaded, etc. A non-equipped disc will respond with DISC READY and RSRW (X'09') to a Sense Status.

6. PROGRAMMING SEQUENCES

Programming sequences are shown in the sample program in Appendix 1.

To initiate an operation on the disc, a certain mandatory sequence must be followed if the status of the Controller and file is unknown upon entry to the routine. This sequence is implemented in the sample drivers (see Appendices 1 and 2)

Some programming considerations are:

1. The program must wait for Selector Channel not busy, or must stop the Selector Channel, prior to sensing any disc status.

2. The program must then sense the Controller status. If CONTROLLER IDLE=0, the file status cannot be sensed. Furthermore, if OVERRUN=1, the Controller will not become idle of its own accord.

3. If OVERRUN=1, the program must issue a RESET command to the Controller before it can proceed. Note that this RESET command will disarm interrupts on all individual files, so that if an interrupt is expected from a file at this time, it may not be taken.

4. When CONTROLLER IDLE=1, the file status may be sensed. If ADS INTERLOCK=1, no command may be given the file, and in fact, the remaining status bits may not be applicable to the file being sensed.

5. When ADS INTERLOCK=0, the other file status bits may be checked. WRITE CHECK and DISC $\overline{\text{READY}}$ denote unrecoverable errors. If WRITE PROTECT is set, no write operation may be attempted. The program must now wait for RSRW=0 before attempting an order to the file or Controller. However, if SEEK INCOMPLETE=1, RSRW will never become zero of its own accord.

6. If SEEK INCOMPLETE=1, the file must be restored. The cylinder address, or a byte of zeros, should be written to the file and a RESTORE oommand issued at this time. The program may wait for an interrupt, or may remain in a status loop waiting for $\overline{\text{RSRW}}$=0.

7. When $\overline{\text{RSRW}}$=0, the cylinder address should be written to the file and the SEEK command issued. The program may now wait for an interrupt, or may remain in a status loop, first waiting for CONTROLLER IDLE=1, then for RSRW=0.

8. At this time, the file status should be checked. If the status byte is non-zero, an error has occurred. The program might attempt to correct ILLEGAL ADDRESS status by performing another SEEK, or to correct SEEK INCOMPLETE by attempting another RESTORE; however, if the cylinder address sent to the file was correct, a hardware error has probably occurred, and the program should abort. If no error bits were set, and if this operation was seek-only, the program may now return to the user.

9. The disc heads are now correctly positioned and the data transfer may begin.

   A STOP command should be sent to the Selector Channel in order to set it up for data transfer. The starting address and ending address for the data transfer should be written to the Selector Channel. The cylinder number should be written to the file. The head and sector byte should be written to the Controller. The READ or WRITE command should be sent to the Controller. The GO or READ/GO command should be sent to the Selector Channel.

10. At this time, the program should wait for interrupt or may wait in a status loop until the Selector Channel is not busy. Note that in the case of normal termination of the data transfer, the Selector Channel will interrupt first, followed by Controller interrupt at the end of the next sector. This sequence also occurs in case of error, with the exception that if OVERRUN=1, the Selector Channel will interrupt, but the Controller will neither interrupt nor become idle.

11. When the Selector Channel interrupts (or becomes not busy), the program should send it a STOP command, and then sense the status of the Controller. If OVERRUN is set, the program should abort at this time. Otherwise, the program should wait for an interrupt from the Controller (or should wait in a status loop for Controller Idle).

12. When the Controller interrupts (or becomes idle), the status bits should be checked. If WPV/CYC CHK ERR is set, after a write operation, or if any error bits other than CYL OVERFLOW are set, the program should abort. If WPV/CYC CHK ERR is set after a read operation, the program may attempt to retry the read operation by returning to Step 9 above. If no error bits are set, the program may return to the user.

13. If CYL OVERFLOW was set, the data transfer is not yet complete and the program should begin reading the next cylinder. This may be done as follows:

    a. Read the address of the last data transfer from the Selector Channel. Due to the indeterminate timing of the CYL OVERFLOW error with respect to the Selector Channel/memory cycle, this address may not be correct. Therefore:

    b. Subtract the start address and add two to the result.

    c. Clear the low-order byte of the result and add the start address. This will be the correct start address for the following data transfer.

    d. Increment the desired cylinder number and set the head/sector byte to zeros.

    e. Return to Step 7 above.

7. INTERRUPTS

The Controller will generate a SELCH interrupt when any of the lower three bits of the Controller status byte are set. The Controller and each disc may generate interrupts. The Controller interrupts are always enabled and the individual disc interrupts may be programmed ENABLE/DISABLE/DISARM.

The interrupt priority is:

1. Controller
2. Disc 0
3. Disc 1
4. Disc 2
5. Disc 3

The interrupt conditions are:

CONT IDLE ——→ 1

ILL ADDR ——→ 1

$\overline{\text{RSRW}}$ ——→ 0

SEEK INC ——→ 1

DISC $\overline{\text{READY}}$ ——→ 1

8. INITIALIZATION

Initialization causes the following: Disarms all disc Interrupts, terminates a data transfer in progress; resets the Controller Command Register to zeros (no operation); resets OVERRUN, ADDR COMP FAIL, CYL OV; and sets CONT IDLE.

9. DEVICE NUMBER

The device numbers for the Disc System are:

CONTROLLER	X'B6'
DISC 0	X'C6'
DISC 1	X'D6'
DISC 2	X'E6'
DISC 3	X'F6'

10. SAMPLE PROGRAM

Sample Programs are provided in Appendices 1 and 2.

```
SAMPLE DISC DRIVER (INTERRUPT VERSION)                    PAGE    1

                * DISC DRIVER
                *
                * CALLING SEQUENCE:
                *
                * BAL R15,DSCDRV
                * DC  A(PARAM),A(ERROR)
                *
                * PARAMETER BLOCK:
                *
                * DB  UNIT                          0,1,2,3
                * DB  COMMAND                       0=SEEK,1=READ,2=WRITE
                * DC  LOGICAL SECTOR NUMBER             0 THRU 9743 DECIMAL
                * DC  A(START)                      NOT REQD FOR SEEK COMMAND
                * DC  A(END)                        NOT REQD FOR SEEK COMMAND
                *
                *         REGISTER ADDRESS MNEMONICS
                *
0005            COMAND  EQU   5                   LOWEST
0006            START   EQU   6
0007            ERR     EQU   7
0008            FILE    EQU   8
0009            CONT    EQU   9
000A            SELCH   EQU   10
000B            POINT   EQU   11
000C            SECT    EQU   12                  MUST BE EVEN
000D            CYL     EQU   SECT+1
000E            WORK    EQU   14
000F            RF      EQU   15
                *
0000R                   ENTRY DSCDRV
                *
0000R D050      DSCDRV  STM   COMAND,RSAV         SAVE REGISTERS
      013AR
0004R 48BF              LH    POINT,0(RF)
      0000
0008R D38B              LB    FILE,0(POINT)       GET UNIT NUMBER (0:3)
      0000
000CR 2784              SIS   FILE,4              VALID?
000ER 4380              BNL   ABORT               NO
      0086R
0012R D388              LB    FILE,FATAB+4(FILE)  FILE PHYSICAL ADDRESS
      0134R
0016R D35B              LB    COMAND,1(POINT)     GET COMMAND (0:2)
      0001
001AR C550              CLHI  COMAND,3            VALID?
      0003
001ER 4380              BNL   ABORT               NO
      0086R
0022R C8A0              LHI   SELCH,X'F0'         SELECTOR CHANNEL ADDRESS
      00F0
0026R C890              LHI   CONT,X'B6'          DATA CONTROLLER ADDRESS
      00B6
002AR 48DB              LH    CYL,2(POINT)        LOGICAL SECTOR NUMBER
      0002
002ER C5D0              CLHI  CYL,9744            VALID?
      2610
```

```
0032R 4380          BNL   ABORT          NO
      0036R
0036R 486B          LH    START,4(POINT) GET USER START ADDRESS
      0004
003AR 07CC          XHR   SECT,SECT      BREAK LOGICAL SECTOR
003CR C8E0          LHI   WORK,48        INTO CYLINDER
      0030
0040R 0DCE          DHR   SECT,WORK      AND SECTOR
0042R C5C0          CLHI  SECT,24        IF IT IS ON HEAD 1
      0018
0046R 2187          BLS   DSD2           THEN FIX THE ADDRESS
0048R 26C8          AIS   SECT,8
004AR 07EE          XHR   WORK,WORK      SETUP INTERRUPT
004CR C8F0          LHI   RF,INT         NEW PSW
      00D0R
0050R D0E0          STM   WORK,X'44'
      0044
0054R 9DAE  DSD2    SSR   SELCH,WORK     WAIT FOR SELCH NOT BUSY
0056R 2081          BCS   DSD2
0058R 9D9E  DSD5    SSR   CONT,WORK      NOW CHECK CONTROLLER
005AR 94EE          EXBR  WORK,WORK      PUT BYTE ON HI SIDE
005CR C3E0          THI   WORK,X'8200'   OVERRUN, IDLE BITS
      8200
0060R 2113          BMS   RESET          GO RESET IF OVERRUN
0062R 2235          BZS   DSD5           WAIT FOR IDLE
0064R 2303          BS    WFILE          IDLE AND NOT OVERRUN
0066R DE90  RESET   OC    CONT,RESETC    OVERRUN, RESET EVERYTHING
      0138R
006AR 9D8E  WFILE   SSR   FILE,WORK      FILE STATUS
006CR 2347          BFFS  4,7            BRANCH UNLESS EXAM
006ER C3E0          THI   WORK,X'10'     WAIT FOR ADS INTERLOCK
      0010
0072R 2034          BNZS  WFILE          TO GO AWAY
0074R C3E0          THI   WORK,X'40'     THEN ABORT IF
      0040
0078R 2137          BNZS  ABORT          WRITE CHECK
007AR C550          CLHI  COMAND,2       WRITE COMMAND?
      0002
007ER 2139          BNES  WFILE2         NO
0080R C3E0          THI   WORK,X'80'     YES, IS WRITE PROTECT SET?
      0080
0084R 2336          BZS   WFILE2         BRANCH IF NOT
0086R D150  ABORT   LM    COMAND,RSAV    RESTORE REGISTERS
      013AR
008AR 48FF          LH    RF,2(RF)       RETURN TO USER'S
      0002
008ER 03CF          BR    RF             ERROR ADDRESS
                    *
0090R 9D8E  WFILE2  SSR   FILE,WORK      RESET CONDITION CODES
0092R 2016          BMS   ABORT          FILE NOT READY
0094R 2388          BNCS  SEEK           GO SEEK WHEN RSRW
0096R 4320          BNP   WFILE
      006AR
009AR 9A8D          WDR   FILE,CYL       SEEK INCOMPLETE
009CR DE80          OC    FILE,RESTOC    RESTORE FILE TO ZERO
      0134R
```

```
00A0R 41F0          BAL   RF,WAIT          WAIT FOR SEEK COMPLETE
      00F4R
00A4R 9A8D    SEEK  WDR   FILE,CYL         CYL NUMBER TO FILE
00A6R DE80          OC    FILE,SEEKC       SEEK COMMAND
      0135R
00A8R 41F0          BAL   RF,WAIT          WAIT FOR SEEK COMPLETE
      00F4R
00AER 0855          LHR   COMAND,COMAND    SEEK-ONLY COMMAND?
00B0R 4330          BZ    RETURN           THEN RETURN TO USER
      00FAR
00B4R 2578          LCS   ERR,8            INITIALIZE REREAD COUNTER
00B6R DEA0          OC    SELCH,STOP       KNOCK DOWN SELCH
      0138R
00B8R 98A6    REREAD WHR  SELCH,START      SEND START ADDRESS TO SELCH
00BCR D8AB          WH    SELCH,6(POINT)   END ADDRESS TO SELCH
      0006
00C0R 9A8D          WDR   FILE,CYL         CYLINDER NUMBER TO FILE
00C2R 9A9C          WDR   CONT,SECT        SECTOR ADDRESS TO CONTROLLER
00C4R DE95          OC    CONT,DRWC-1(COMAND) READ OR WRITE DISC
      0133R
00C8R DEA5          OC    SELCH,SRWC-1(COMAND) START SELCH
      0135R
00CCR 4330          B     WAIT             WAIT FOR INTERRUPT
      00F0R
                    *
                    *       INTERRUPT
                    *
00D0R DFE0    INT   AI    WORK,STAT        ACK INTERRUPT
      0139R
00D4R 05E8          CLHR  WORK,FILE        FILE CONTROLLER?
00D6R 2135          BNES  TSEL             B IF NO
00D8R 9D8E          SSR   FILE,WORK        YES
00DAR 03FF          BFCR  15,RF            RETURN IF STATUS ZERO
00DCR 4330    BAB01 B     ABORT            ELSE ABORT
      0086R
                    *
                    *       SELCH OR DC INTERRUPT
                    *
00E0R 05EA    TSEL  CLHR  WORK,SELCH       SELCH?
00E2R 2139          BNES  CONTI            NO, MUST BE CONTROLLER
00E4R DEA0          OC    SELCH,STOP       OK, NOW KNOCK IT DOWN
      0138R
00E8R 9D9E          SSR   CONT,WORK        CONT STATUS
00EAR C3E0          THI   WORK,X'80'       TEST FOR OVERRUN
      0080
00EER 2039          BNZS  BAB01            ABORT IF OVERRUN
00F0R C2C0    WAIT  LPSW  WAITP            WAIT FOR INTERRUPT
      012CR
                    *
                    *       CONTROLLER INTERRUPT
                    *
00F4R 9D9E    CONTI SSR   CONT,WORK        CONTROLLER STATUS
00F6R 214E          BOS   TCYLOV           BRANCH IF EXAM
00F8R 2115          BMS   TWPCC            WPV/CYC CHK?
00FAR D150    RETURN LM   COMAND,RSAV      NO, TAKE GOOD RETURN
      013AR
```

```
00FEP 43?F            B     4(RF)
      0014
                      *
                      *        WRITE PROTECT VIOLATION OR CYCLIC CHECK ERROR
                      *
0102R C550    TWPCC   CLHI  COMAND,2        WRITE COMMAND?
      0002
0106R 2334            BFS   BABO           YES, ABORT
0108R 2671            AIS   ERR,1          NO, BUMP REREAD COUNTER
010AR 421A            BM    REREAD         GO REREAD
      00BAR
010ER 4300    BABO    B     ABORT          BUT ABORT IF HARD ERROR
      0086R
                      *
                      *        CYLINDER OVERFLOW
                      *
0112R C3E0    TCYLOV  THI   WORK,X'10'     CYLINDER OVERFLOW?
      0010
0116R 2234            BZS   BABO           NO, ABORT
0118R 99AE            RHR   SELCH,WORK     YES, SET FOR
011AR 0BE6            SHR   WORK,START     ANOTHER CYLINDER
011CR 26E2            AIS   WORK,2
011ER C4E0            NHI   WORK,X'FF00'
      FF00
0122R 0A6E            AHR   START,WORK
0124R 07CC            XHR   SECT,SECT      START AT SECTOR 0
0126R 26D1            AIS   CYL,1
0128R 4300            B     SEEK           CONTINUE
      0044R
                      *
012CR C000    WAITP   DC    X'C000',A(WAIT)
      00F0R
                      *
0130R C6D6    FATAB   DC    X'C6D6',X'E6F6' FILE ADDRESS TABLE
      E6F6
                      *
                      *        COMMAND BYTES
                      *
0134R 4142    DRWC    DC    X'4142'
0136R 3010    SRWC    DC    X'3010'
0135R         SEEKC   EQU   DRWC+1
0134R         RESTOC  EQU   DRWC
0138R 08      STOP    DB    X'08'
0138R         RESETC  EQU   STOP
0139R 00      STAT    DB    0              WORK LOC
013AR                 DB    *
                      *
                      *        REGISTER SAVE AREA
                      *
013AR         RSAV    DS    22
0150R                 END
```

```
NO ERRORS

   ABORT    0086R
   BAB0     010ER
   BAB01    00DCR
   COMAND   0005
   CONT     0009
   CONTI    00F4R
   CYL      000D
   DRWC     0134R
 * DSCDRV   0000R
   DSD2     0054R
   DSD5     0058R
   ERR      0007
   FATAB    0130R
   FILE     0008
   INT      00D0R
   POINT    000B
   REREAD   00BAR
   RESET    0066R
   RESETC   0138R
   RESTOC   0134R
   RETURN   00FAR
   RF       000F
   RSAV     013AR
   SECT     000C
   SEEK     00A4R
   SEEKC    0135R
   SELCH    000A
   SRWC     0136R
   START    0006
   STAT     0139R
   STOP     0138R
   TCYLOV   0112R
   TSEL     00E0R
   TWPCC    0102R
   WAIT     00F0R
   WAITP    012CR
   WFILE    006AR
   WFILE2   0090R
   WORK     000E
```

```
SAMPLE DISC DRIVER (STATUS LOOP VERSION)                    PAGE    1

                * DISC DRIVER
                *
                * CALLING SEQUENCE:
                *
                * BAL R15,DSCDRV
                * DC  A(PARAM),A(ERROR)
                *
                * PARAMETER BLOCK:
                *
                * DB  UNIT                          0,1,2,3
                * DB  COMMAND                       0=SEEK,1=READ,2=WRITE
                * DC  LOGICAL SECTOR NUMBER             0 THRU 9743 DECIMAL
                * DC  A(START)                      NOT REQD FOR SEEK COMMAND
                * DC  A(END)                        NOT REQD FOR SEEK COMMAND
                *
                *         REGISTER ADDRESS MNEMONICS
                *
0005            COMAND  EQU   5                   LOWEST
0006            START   EQU   6
0007            ERR     EQU   7
0008            FILE    EQU   8
0009            CONT    EQU   9
000A            SELCH   EQU   10
000B            POINT   EQU   11
000C            SECT    EQU   12                  MUST BE EVEN
000D            CYL     EQU   SECT+1
000E            WORK    EQU   14
000F            RF      EQU   15
                *
0000R                   ENTRY DSCDRV
                *
0000R D050      DSCDRV  STM   COMAND,RSAV         SAVE REGISTERS
      0124R
0004R 48BF              LH    POINT,0(RF)
      0000
0008R D38B              LB    FILE,0(POINT)       GET UNIT NUMBER (0:3)
      0000
000CR 2784              SIS   FILE,4              VALID?
000ER 4380              BNL   ABORT               NO
      007CR
0012R D388              LB    FILE,FATAB+4(FILE)  FILE PHYSICAL ADDRESS
      011ER
0016R D358              LB    COMAND,1(POINT)     GET COMMAND (0:2)
      0001
001AR C550              CLHI  COMAND,3            VALID?
      0003
001ER 4380              BNL   ABORT               NO
      007CR
0022R C8A0              LHI   SELCH,X'F0'         SELECTOR CHANNEL ADDRESS
      00F0
0026R C890              LHI   CONT,X'B6'          DATA CONTROLLER ADDRESS
      00B6
002AR 48DB              LH    CYL,2(POINT)        LOGICAL SECTOR NUMBER
      0002
002ER C5D0              CLHI  CYL,9744            VALID?
      2610
```

```
0032R 4380            BNL   ABORT            NO
      007CR
0036R 486B            LH    START,4(POINT)   GET USER START ADDRESS
      0004
003AR 07CC            XHR   SECT,SECT        BREAK LOGICAL SECTOR
003CR C8E0            LHI   WORK,48          INTO CYLINDER
      0030
0040R 0DCE            DHR   SECT,WORK        AND SECTOR
0042R C5C0            CLHI  SECT,24          IF IT IS ON HEAD 1
      0018
0046R 2182            BLS   DSD2             THEN FIX THE ADDRESS
0048R 26C8            AIS   SECT,8
004AR 9DAE    DSD2    SSR   SELCH,WORK       WAIT FOR SELCH NOT BUSY
004CR 2081            BCS   DSD2
004ER 9D9E    DSD5    SSR   CONT,WORK        NOW CHECK CONTROLLER
0050R 94EE            EXBR  WORK,WORK        GET BYTE UP TO MS SIDE
0052R C3E0            THI   WORK,X'8200'     OVERRUN AND IDLE BITS
      8200
0056R 2113            BMS   RESET            GO RESET IF OVERRUN
0058R 2235            BZS   DSD5             WAIT FOR IDLE
005AR 2303            BS    WFILE            IDLE AND NOT OVERRUN
005CR DE90    RESET   OC    CONT,RESETC      OVERRUN, RESET EVERYTHING
      0122R
0060R 9D8E    WFILE   SSR   FILE,WORK        FILE STATUS
0062R 2347            BFFS  4,7              BRANCH UNLESS EXAM
0064R C3E0            THI   WORK,X'10'       WAIT FOR ADS INTERLOCK
      0010
0068R 2034            BNZS  WFILE            TO GO AWAY
006AR C3E0            THI   WORK,X'40'       THEN ABORT IF
      0040
006ER 2137            BNZS  ABORT            WRITE CHECK
0070R C550            CLHI  COMAND,2         WRITE COMMAND?
      0002
0074R 2139            BNES  WFILE2           NO
0076R C3E0            THI   WORK,X'80'       YES, IS WRITE PROTECT SET?
      0080
007AR 2336            BZS   WFILE2           BRANCH IF NOT
007CR D150    ABORT   LM    COMAND,RSAV      RESTORE REGISTERS
      0124R
0080R 48FF            LH    RF,2(RF)         RETURN TO USER'S
      0002
0084R 030F            BR    RF               ERROR ADDRESS
                      *
0086R 9D8E    WFILE2  SSR   FILE,WORK        RESET CONDITION CODES
0088R 2016            BMS   ABORT            FILE NOT READY
008AR 2388            BNCS  SEEK             GO SEEK WHEN RSRW
008CR 4320            BNP   WFILE
      0060R
0090R 9A8D            WDR   FILE,CYL         SEEK INCOMPLETE
0092R DE80            OC    FILE,RESTOC      RESTORE FILE TO ZERO
      011ER
0096R 41F0            BAL   RF,WSEEKC        WAIT FOR SEEK COMPLETE
      010CR
009AR 9A8D    SEEK    WDR   FILE,CYL         CYL NUMBER TO FILE
009CR DE80            OC    FILE,SEEKC       SEEK COMMAND
      011FR
```

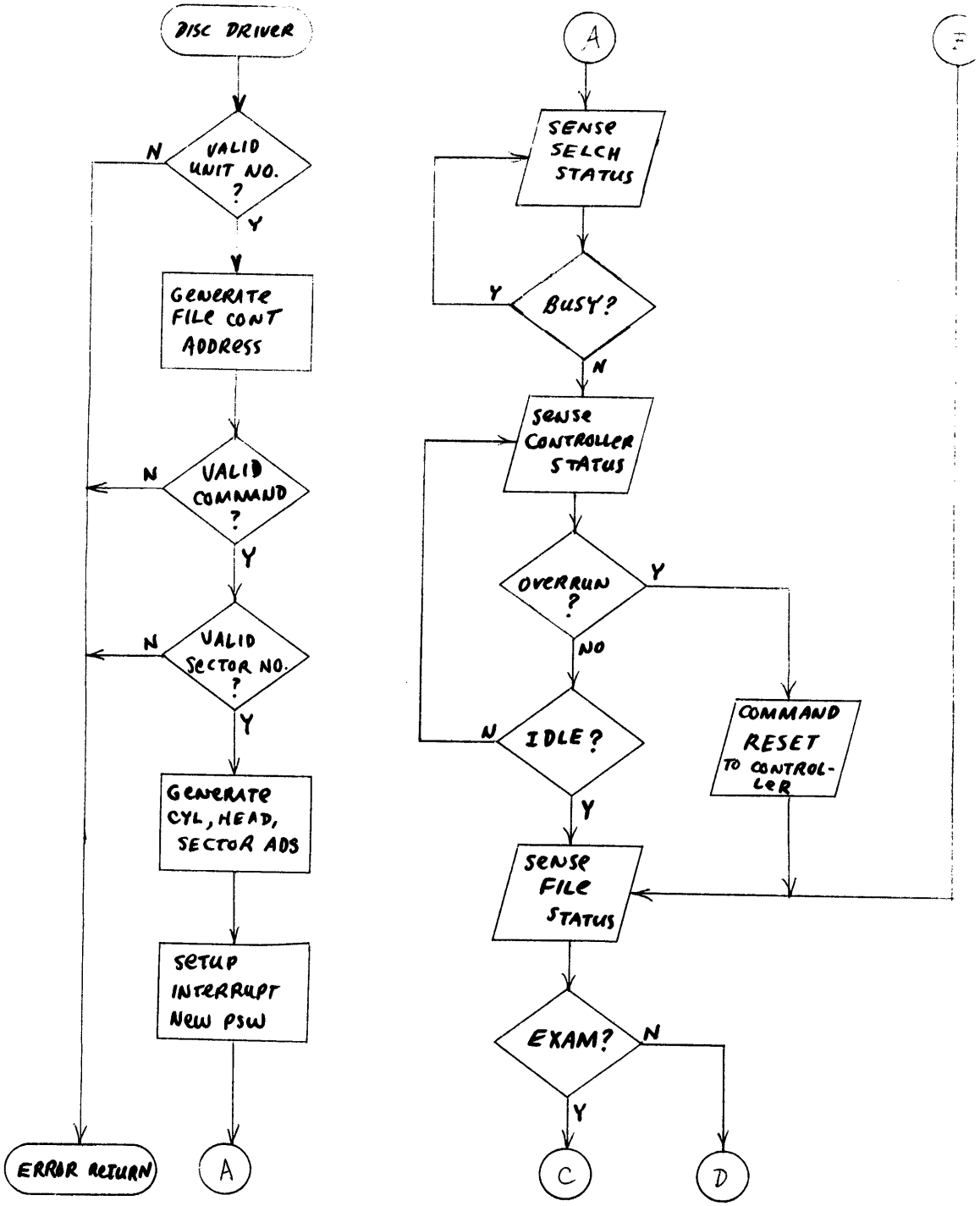
```
00A0R 41F0              BAL   RF,WSEEKC        WAIT FOR SEEK COMPLETE
      010CR
00A4R 0855              LHR   COMAND,COMAND    SEEK-ONLY COMMAND?
00A6R 4330              BZ    RETURN           THEN RETURN TO USER
      00DAR
00AAR 2578              LCS   ERR,8            INITIALIZE REREAD COUNTER
00ACR DEA0              OC    SELCH,STOP       KNOCK DOWN SELCH
      0122R
00B0R 98A6    REREAD    WHR   SELCH,START      SEND START ADDRESS TO SELCH
00B2R D8AB              WH    SELCH,6(POINT)   END ADDRESS TO SELCH
      0006
00B6R 9A8D              WDR   FILE,CYL         CYLINDER NUMBER TO FILE
00B8R 9A9C              WDR   CONT,SECT        SECTOR ADDRESS TO CONTROLLER
00BAR DE95              OC    CONT,DRWC-1(COMAND) READ OR WRITE DISC
      011DR
00BER DEA5              OC    SELCH,SRWC-1(COMAND) START SELCH
      011FR
00C2R 9DAE    WSELCH    SSR   SELCH,WORK       WAIT FOR SELCH NOT BUSY
00C4R 2081              BCS   WSELCH
00C6R DEA0              OC    SELCH,STOP       OK, NOW KNOCK IT DOWN
      0122R
00CAR 9D9E    WCONT     SSR   CONT,WORK        AND CHECK CONTROLLER STATUS
00CCR 2125              BPS   TERROR           IF IDLE, TEST FOR ERROR
00CER C3E0              THI   WORK,X'80'       ELSE CHECK FOR OVERRUN
      0080
00D2R 2234              BZS   WCONT            WHICH COULD HANG US UP
00D4R 230D              BS    BABO             ABORT IF OVERRUN
                      *
                      *       READ COMPLETE, TEST FOR ERRORS
                      *
00D6R 214E    TERROR    BOS   TCYLOV           BRANCH IF EXAM
00D8R 2115              BMS   TWPCC            WPV/CYC CHK?
00DAR D150    RETURN    LM    COMAND,RSAV      NO, TAKE GOOD RETURN
      0124R
00DER 430F              B     4(RF)
      0004
                      *
                      *       WRITE PROTECT VIOLATION OR CYCLIC CHECK ERROR
                      *
00E2R C550    TWPCC     CLHI  COMAND,2         WRITE COMMAND?
      0002
00E6R 2334              BES   BABO             YES, ABORT
00E8R 2671              AIS   ERR,1            NO, BUMP REREAD COUNTER
00EAR 4210              BM    REREAD           GO REREAD
      00B0R
00EER 4300    BABO      B     ABORT            BUT ABORT IF HARD ERROR
      007CR
                      *
                      *       CYLINDER OVERFLOW
                      *
00F2R C3E0    TCYLOV    THI   WORK,X'10'       CYLINDER OVERFLOW?
      0010
00F6R 2234              BZS   BABO             NO, ABORT
00F8R 99AE              RHR   SELCH,WORK       YES, SET FOR
00FAR 0BE6              SHR   WORK,START       ANOTHER CYLINDER
00FCR 26E2              AIS   WORK,2
```

```
00FER C4E0             NHI    WORK,X'FF00'
      FF00
0102R 0A6E             AHR    START,WORK
0104R 07CC             XHR    SECT,SECT        START AT SECTOR 0
0106R 2601             AIS    CYL,1
0108R 4300             B      SEEK             CONTINUE
      009AR
                *
                *        WAIT FOR SEEK COMPLETE
                *
010CR 9D9E     WSEEKC  SSR    CONT,WORK        WAIT FOR CONTROLLER IDLE
010ER 2221             BNPS   WSEEKC
0110R 9D8E     WSEEK1  SSR    FILE,WORK        NOW FILE STATUS
0112R 4270             BTC    7,ABORT          ABORT IF STATUS NONZERO
      007CR
0116R 2083             BCS    WSEEK1           EXCEPT FOR NRSRW
0118R 030F             BR     RF               RETURN WHEN RSRW
                *
011AR C6D6     FATAB   DC     X'C6D6',X'E6F6'  FILE ADDRESS TABLE
      E6F6
                *
                *        COMMAND BYTES
                *
011ER C1C2     DRWC    DC     X'C1C2'
0120R 3010     SRWC    DC     X'3010'
011FR          SEEKC   EQU    DRWC+1
011ER          RESTOC  EQU    DRWC
0122R 08       STOP    DB     X'08'
0122R          RESETC  EQU    STOP
0123R 00               DB     *
                *
                *        REGISTER SAVE AREA
                *
0124R          RSAV    DS     22
013AR                  END
```

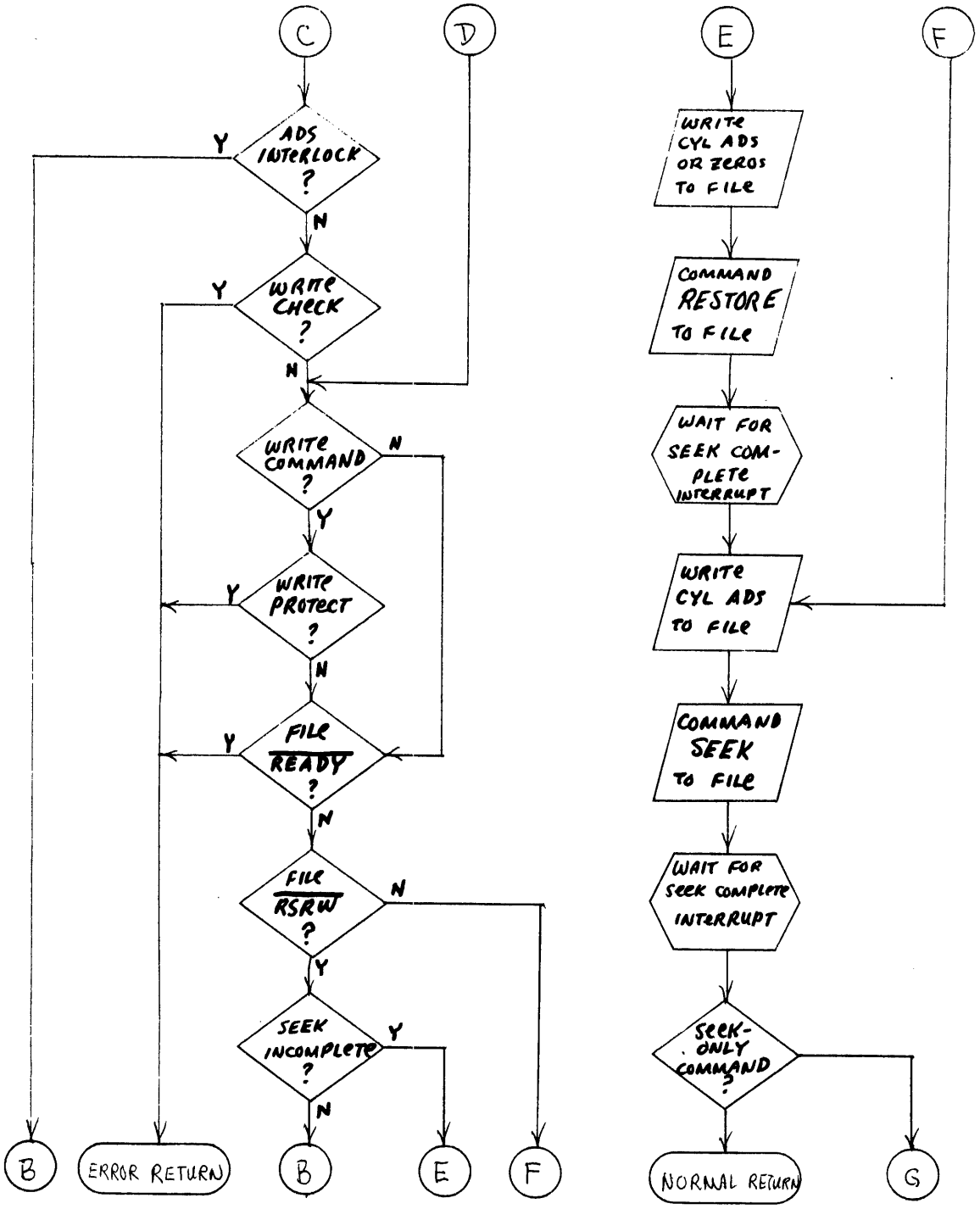
NO ERRORS

```
  ABORT    007CR
  BABO     00EER
  COMAND   0005
  CONT     0009
  CYL      000D
  DRWC     011ER
* DSCDRV   0000R
  DSD2     004AR
  DSD5     004ER
  ERR      0007
  FATAB    011AR
  FILE     0008
  POINT    000B
  REREAD   00B0R
  RESET    005CR
  RESETC   0122R
  RESTOC   011ER
  RETURN   00DAR
  RF       000F
  RSAV     0124R
  SECT     000C
  SEEK     009AR
  SEEKC    011FR
  SELCH    000A
  SRWC     0120R
  START    0006
  STOP     0122R
  TCYLOV   00F2R
  TERROR   00D6R
  TWPCC    00E2R
  WCONT    00CAR
  WFILE    0060R
  WFILE2   0086R
  WORK     000E
  WSEEK1   0110R
  WSEEKC   010CR
  WSELCH   00C2R
```

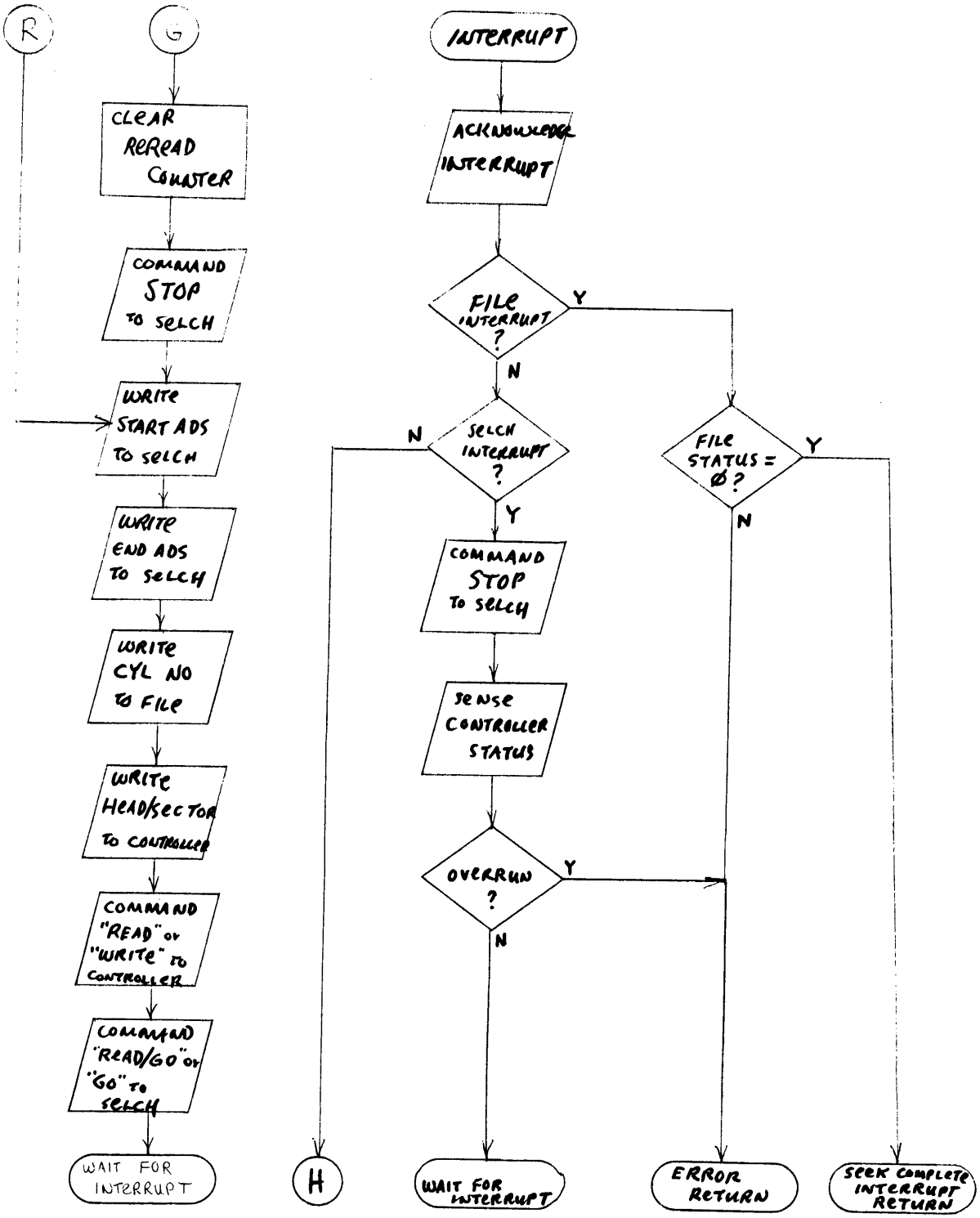
APPENDIX 3
FLOW CHART



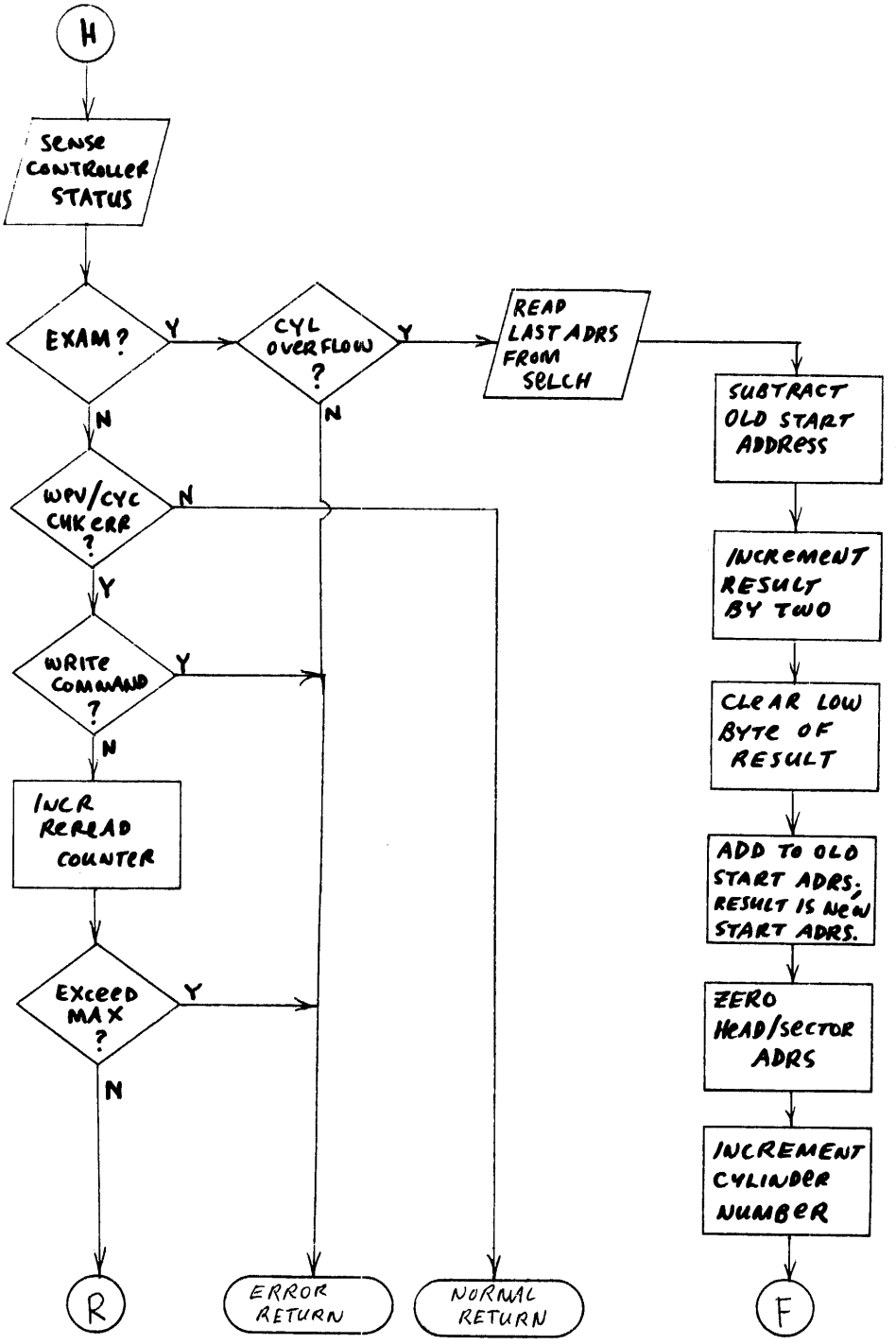
SAMPLE DRIVER-INTERRUPT (SHEET 1 OF 4)



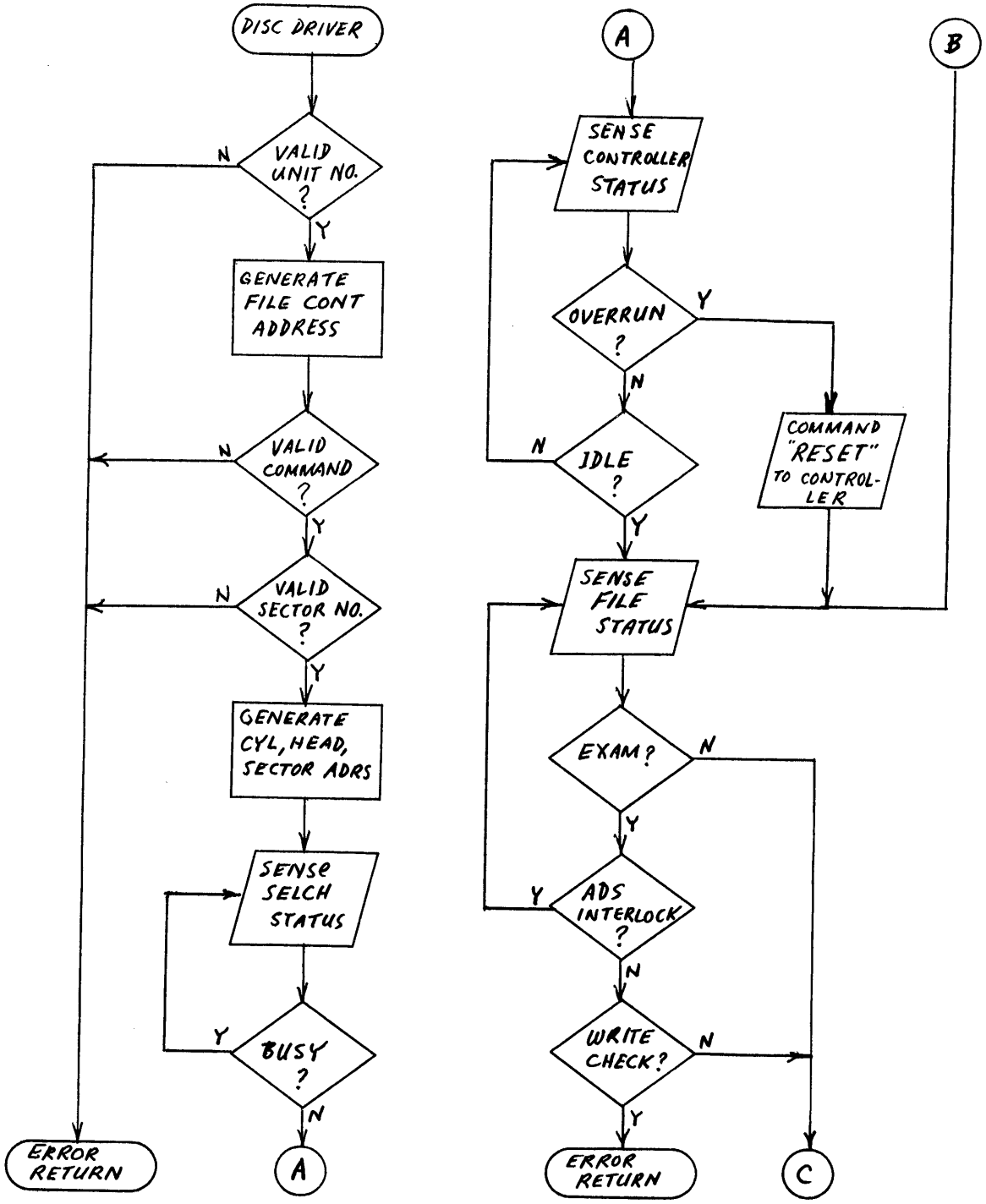
SAMPLE DRIVER - INTERRUPT (SHEET 2 OF 4)



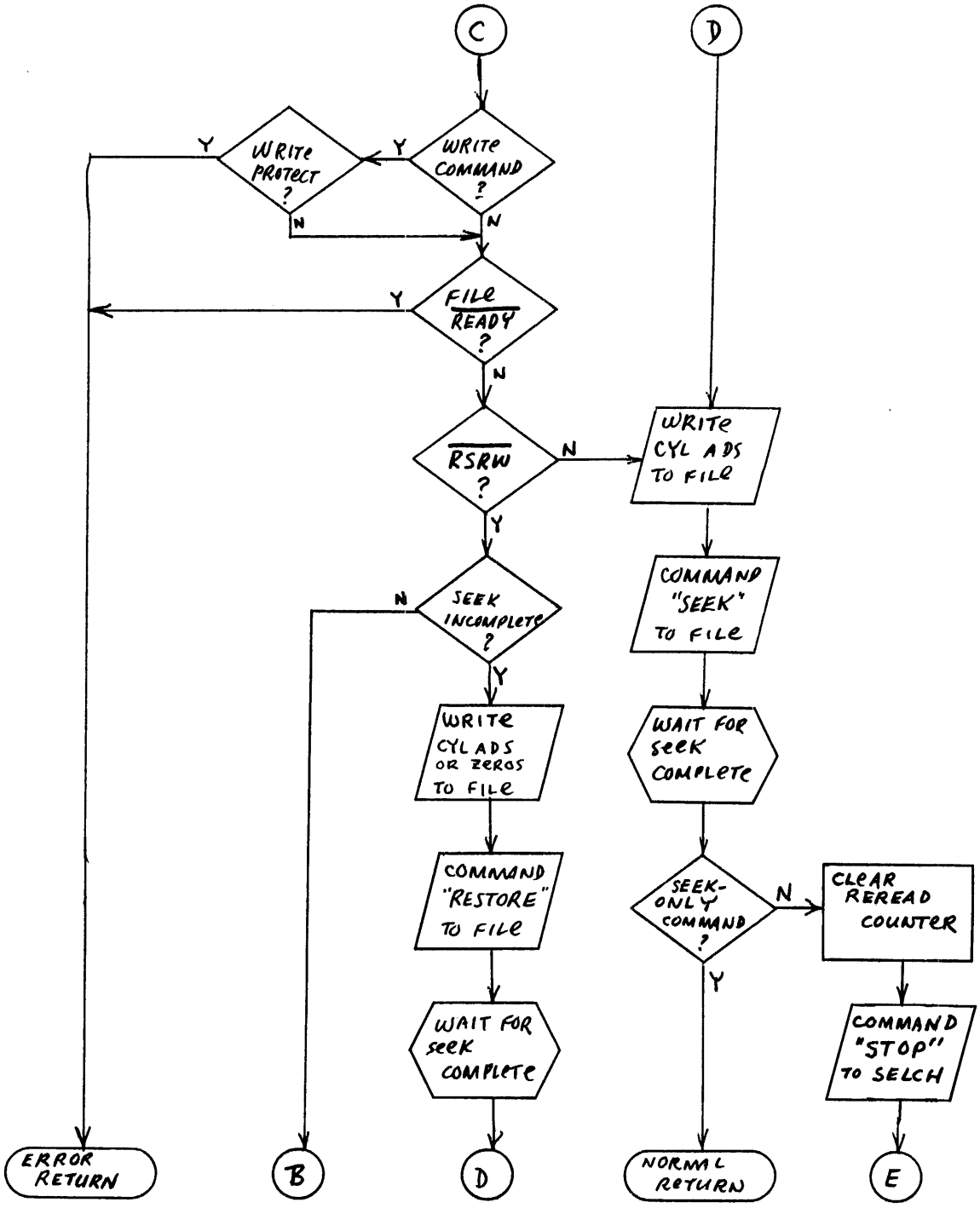
SAMPLE DRIVER - INTERRUPT (SHEET 3 OF 4)



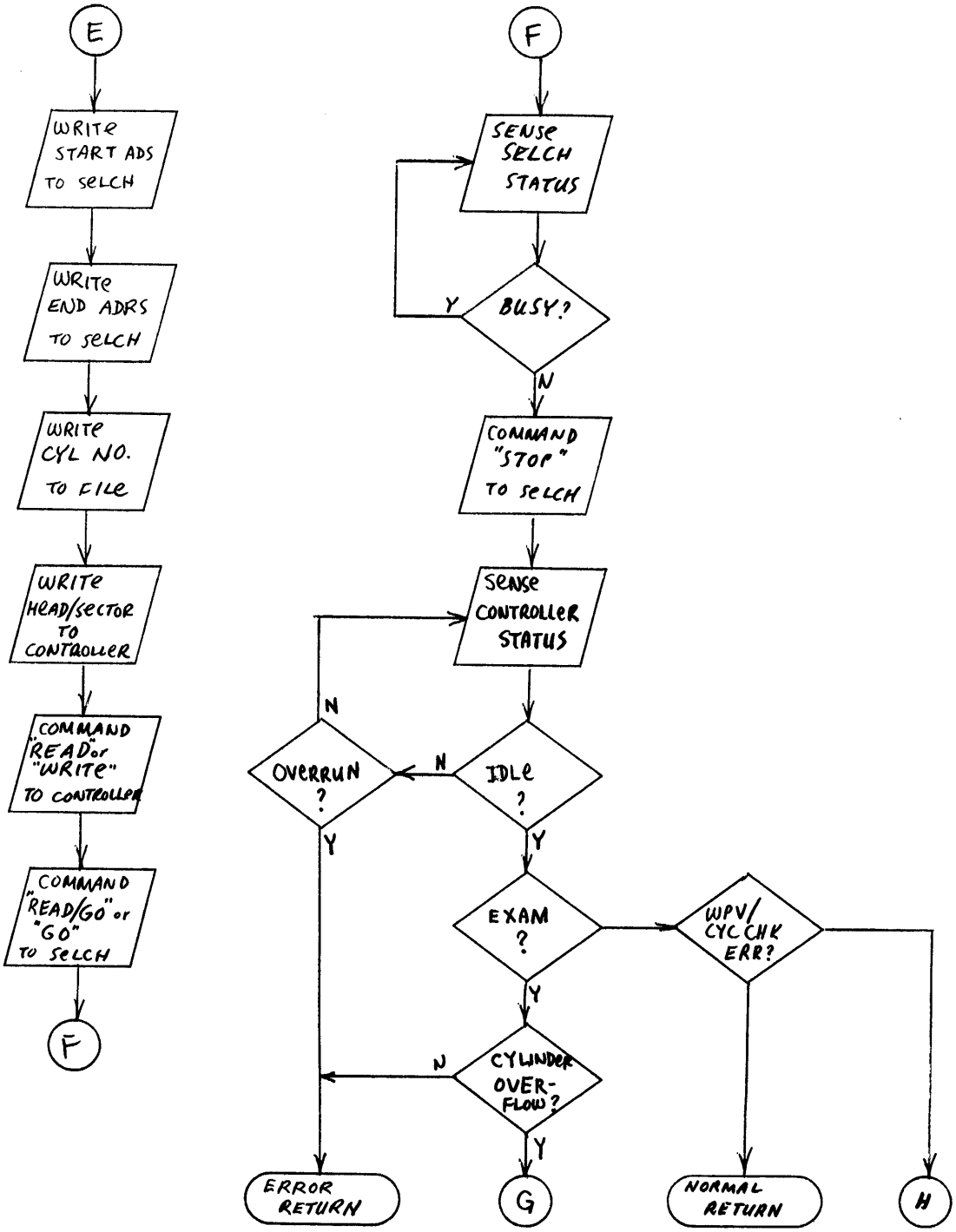
SAMPLE DRIVER-INTERRUPT (SHEET 4 OF 4)



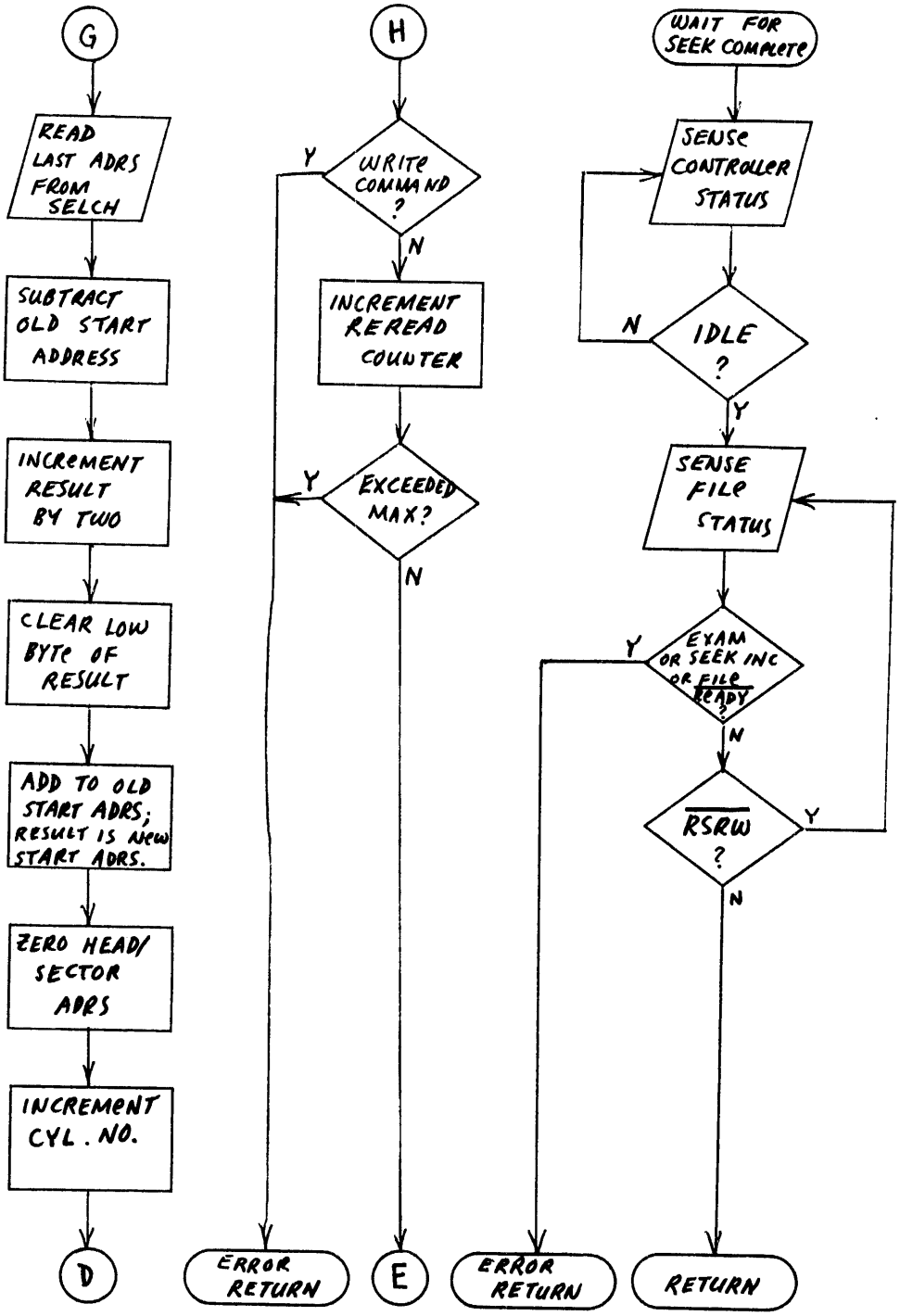
SAMPLE DRIVER - STATUS LOOP (SHEET 1 OF 4)



SAMPLE DRIVER-STATUS LOOP (SHEET 2 OF 4)



SAMPLE DRIVER - STATUS LOOP (SHEET 3 OF 4)



SAMPLE DRIVER - STATUS LOOP (SHEET 4 OF 4)

ADDRESS ASSIGNMENT
STRAPS SHOWN FOR
B6 = CONT
C6 = FILEØ
D6 = 1
E6 = 2
F6 = 3

102-Ø DALØØØ
103-Ø DALØ1Ø
104-Ø DALØ2Ø
105-Ø DALØ3Ø
202-Ø DALØ4Ø
203-Ø DALØ5Ø
204-Ø DALØ6Ø
205-Ø DALØ7Ø

02
35-038
ADDRESS STRAP
BOARD NO. 1

5K1 INAKCØ
5S1 IAD21
5R1 IAD11
5J1 DDGRKØ
2E2 GCLRØ
2E1 ADRS1

04L 9322 QUAD 2-WAY MULTIPLEXER
LOD4X
LOD2X
LOD1X
ADS41
ADS21
ADS11

03
35-038
ADDRESS STRAP
BOARD NO. 2
+V
GND
AS0X
AS1X
AS2X
AS3X
AS4X
AS5X
AS6X
AS7X

DALØØ1 118-1, 10N8 5C8 2M1
AGØØ1
DALØ11 218-1, 10M8 5D8 2M2
AGØ11
DALØ21 116-1, 10L8 2M3
AGØ21
DALØ31 216-1, 10K8 2M3
AGØ31
DALØ41 114-1, 10J8 2A2 2M5
AGØ41
DALØ51 214-1, 10H8 2M4
AGØ51
DALØ61 112-1, 10G8 3C8 2M5
AGØ61
DALØ71 212-1, 10F8 3B8 2M6
AGØ71

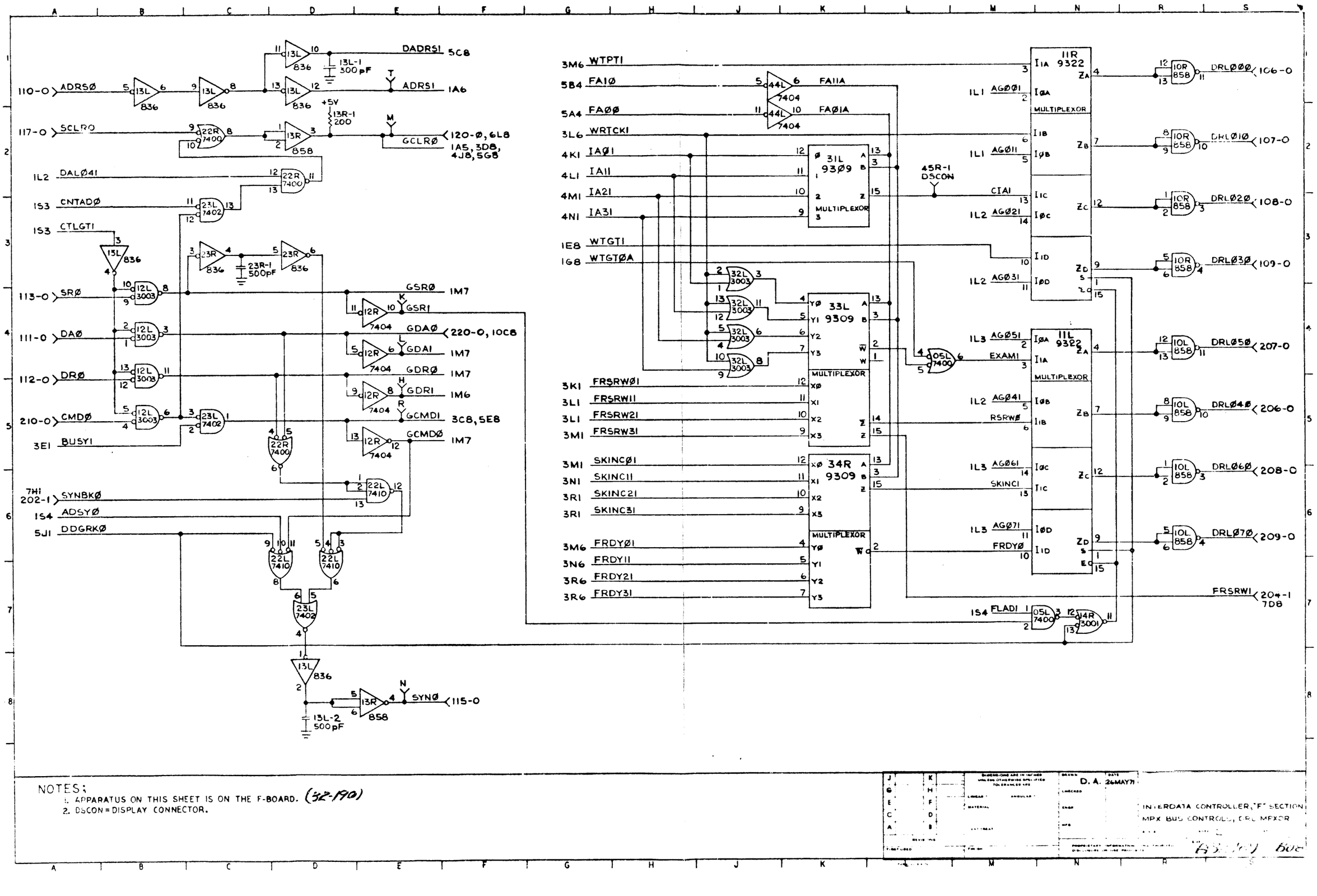
07L 6.248 MHZ
07R-1 1K
07R-2 200pF
07R-3 1K
07R-4 1.8K
07L-1 1.8K
17L 7474
WTOSCI 12Ø-1 958
3EI BUSY1
BUSYØ 22Ø-1 8C3
1Ø4-1 9G1 WTGT1
WTGTØA 2G3, 3C8, 5B8
WTGT1 2G3

24L 7474
CNTADI
CNTADØ 2A3
CTLGT1 2A3
FLAD1 2M7, 3C8, 5E8
ADSYØ 2A6
LODIX 5A8
LOD2X 5B8

2E4 GDA1
2E5 GDR1
CNTDTØ 2Ø8-1 6S8
2E4 GSRØ
CNTSRØ 11Ø-1 8B8
2E5 GCMDØ
CNTCMØ 1Ø8-1 6L8
2E4 GDRØ
CNTDR1 21Ø-1 8B8

NOTES;
1. +V IS SUPPLIED BY 1K RESISTOR TO +5V.
2. APPARATUS ON THIS SHEET IS ON THE F-BOARD. (52-190)
3. DSCON = DISPLAY CONNECTOR.

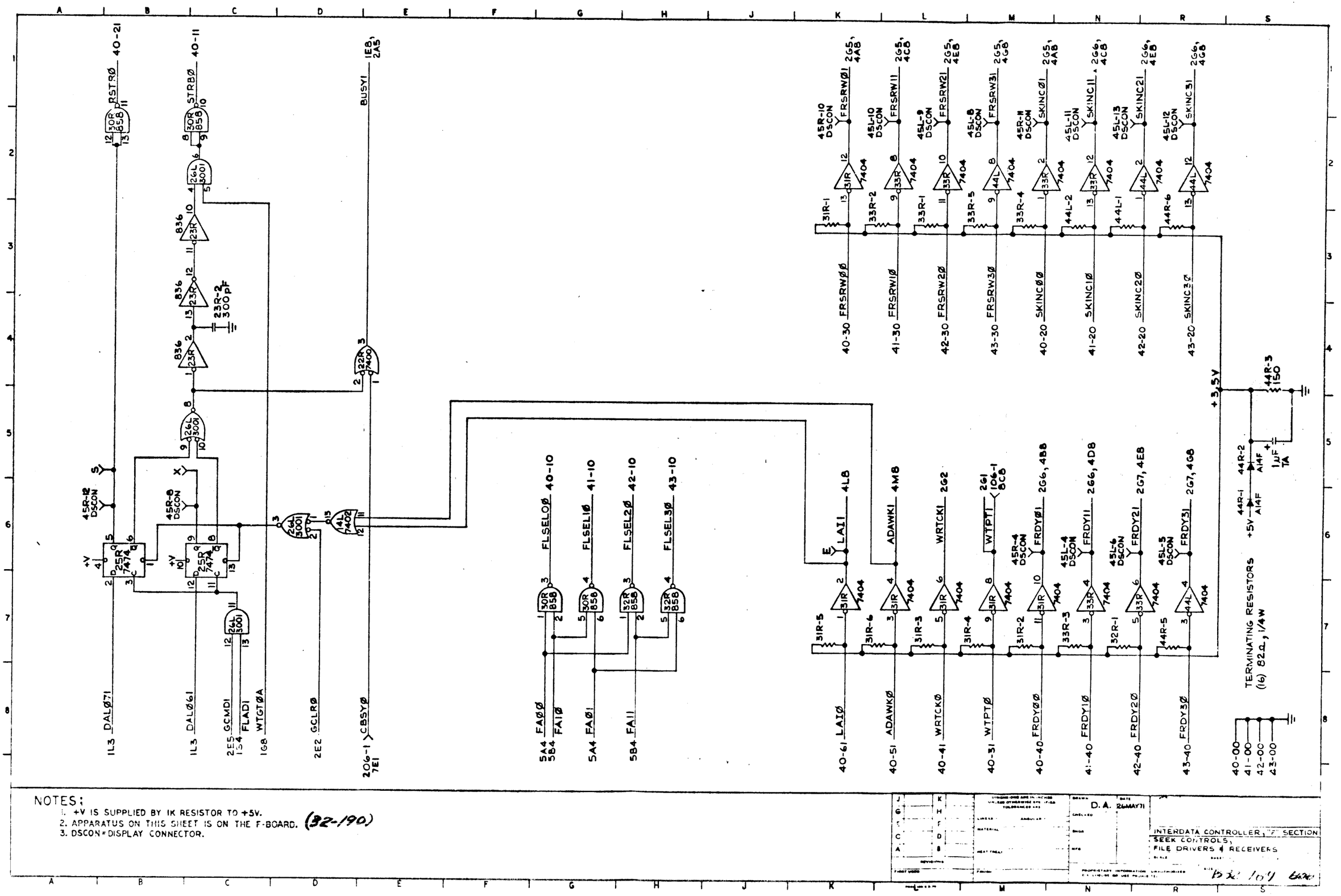
D. A. 26MAY71
WJM 7-27-71
INTERDATA CONTROLLER "F" SECTION
MPX ADDRESS DECODE, WRITE OSC
STITCH DRIVERS & RECEIVERS
12
B32-184 B08



NOTES;
1. APPARATUS ON THIS SHEET IS ON THE F-BOARD. (32-190)
2. DSCON = DISPLAY CONNECTOR.

D. A. 26MAY71

INTERDATA CONTROLLER, 'F' SECTION
MPX BUS CONTROL, CRC MPXR



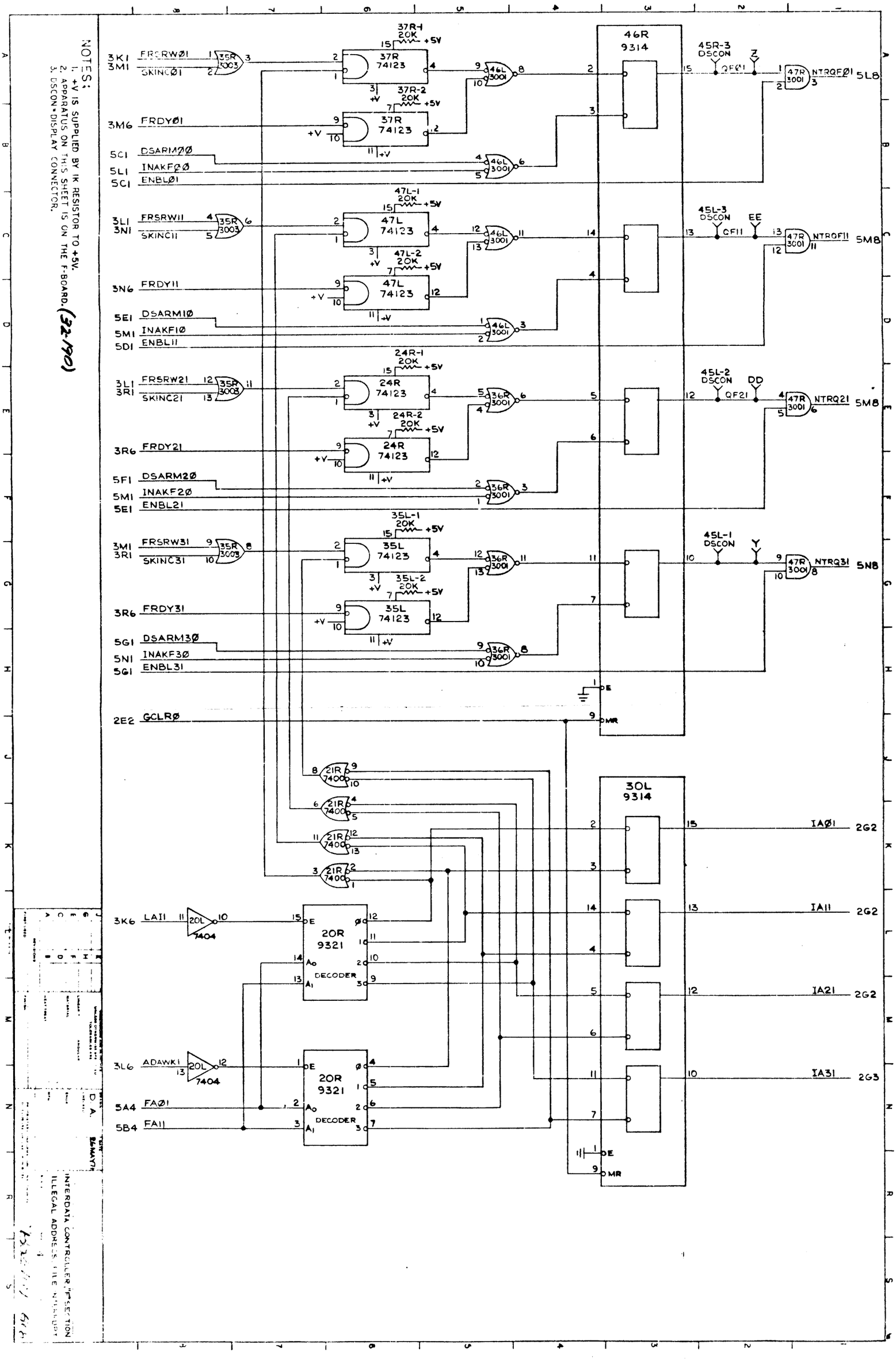
NOTES:
1. +V IS SUPPLIED BY 1K RESISTOR TO +5V.
2. APPARATUS ON THIS SHEET IS ON THE F-BOARD. (32-190)
3. DSCON = DISPLAY CONNECTOR.

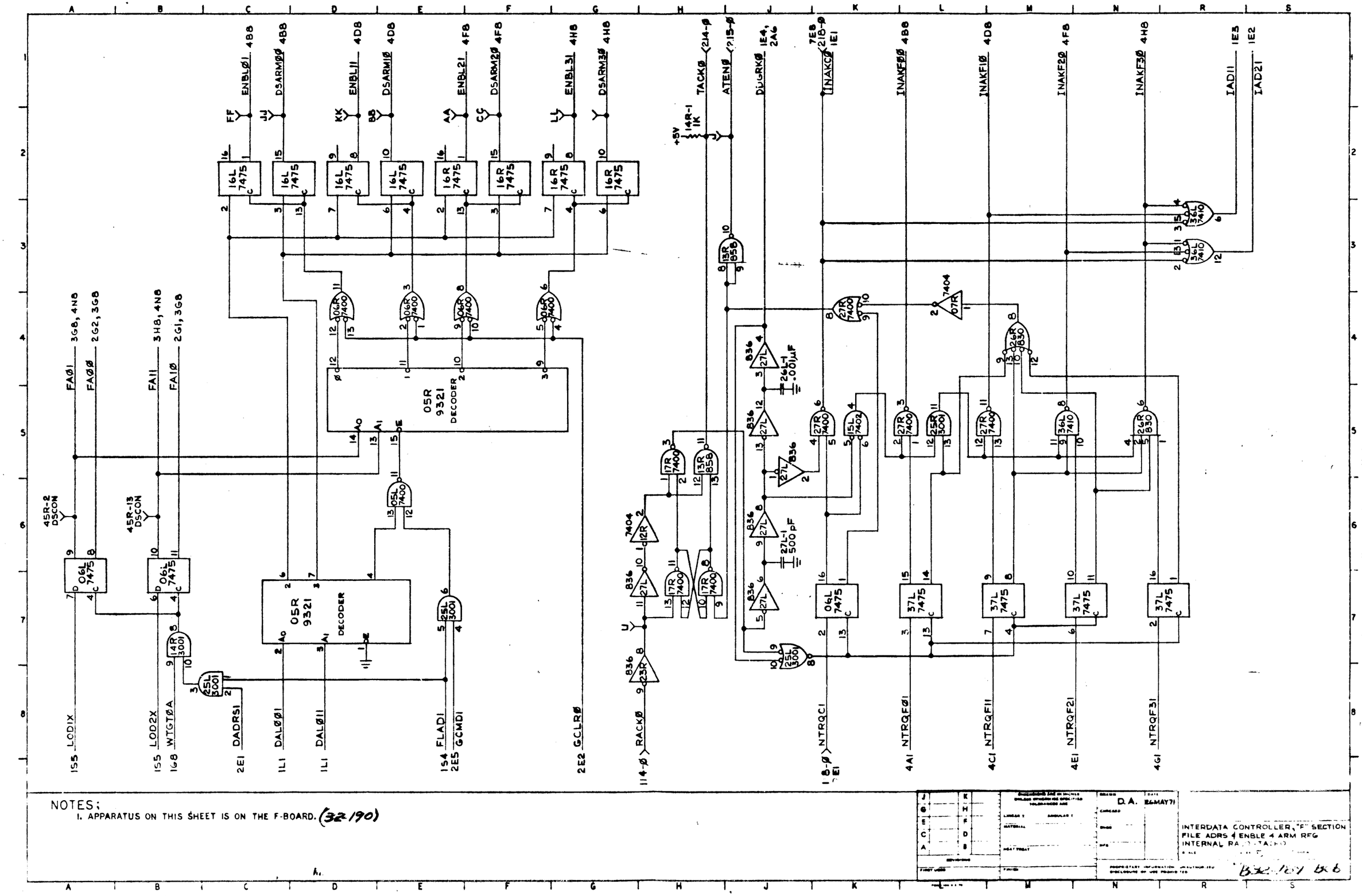
D. A. 26MAY71

INTERDATA CONTROLLER "F" SECTION
SEEK CONTROLS,
FILE DRIVERS & RECEIVERS

PROPRIETARY INFORMATION

32-109


NOTES:
1. +V IS SUPPLIED BY 1K RESISTOR TO +5V.
2. APPARATUS ON THIS SHEET IS ON THE F-BOARD. (32-401)
3. DSCON = DISPLAY CONNECTOR.
3K1 FRCRW01
3M1 SKINC01
3M6 FRDY01
5C1 DSARM00
5L1 INAKF00
5C1 ENBL01
37R-1 20K +5V
37R 74123
37R-2 20K +5V
37R 74123
46R 9314
45R-3 DSCON QF01
NTRQF01 5L8
3L1 FRSRW11
3N1 SKINC11
3N6 FRDY11
5E1 DSARM10
5M1 INAKF10
5D1 ENBL11
47L-1 20K +5V
47L 74123
47L-2 20K +5V
47L 74123
45L-3 DSCON QF11
NTRQF11 5M8
3L1 FRSRW21
3R1 SKINC21
3R6 FRDY21
5F1 DSARM20
5M1 INAKF20
5E1 ENBL21
24R-1 20K +5V
24R 74123
24R-2 20K +5V
24R 74123
45L-2 DSCON QF21
NTRQ21 5M8
3M1 FRSRW31
3R1 SKINC31
3R6 FRDY31
5G1 DSARM30
5N1 INAKF30
5G1 ENBL31
35L-1 20K +5V
35L 74123
35L-2 20K +5V
35L 74123
45L-1 DSCON Y
NTRQ31 5N8
2E2 GCLR0
30L 9314
IA00 2G2
IA11 2G2
IA21 2G2
IA31 2G3
3K6 LA11
3L6 ADAWK1
5A4 FA01
5B4 FA11
20R 9321 DECODER
7404
INTERDATA CONTROLLER INTERFACE
ILLEGAL ADDRESS FILE INTERRUPT

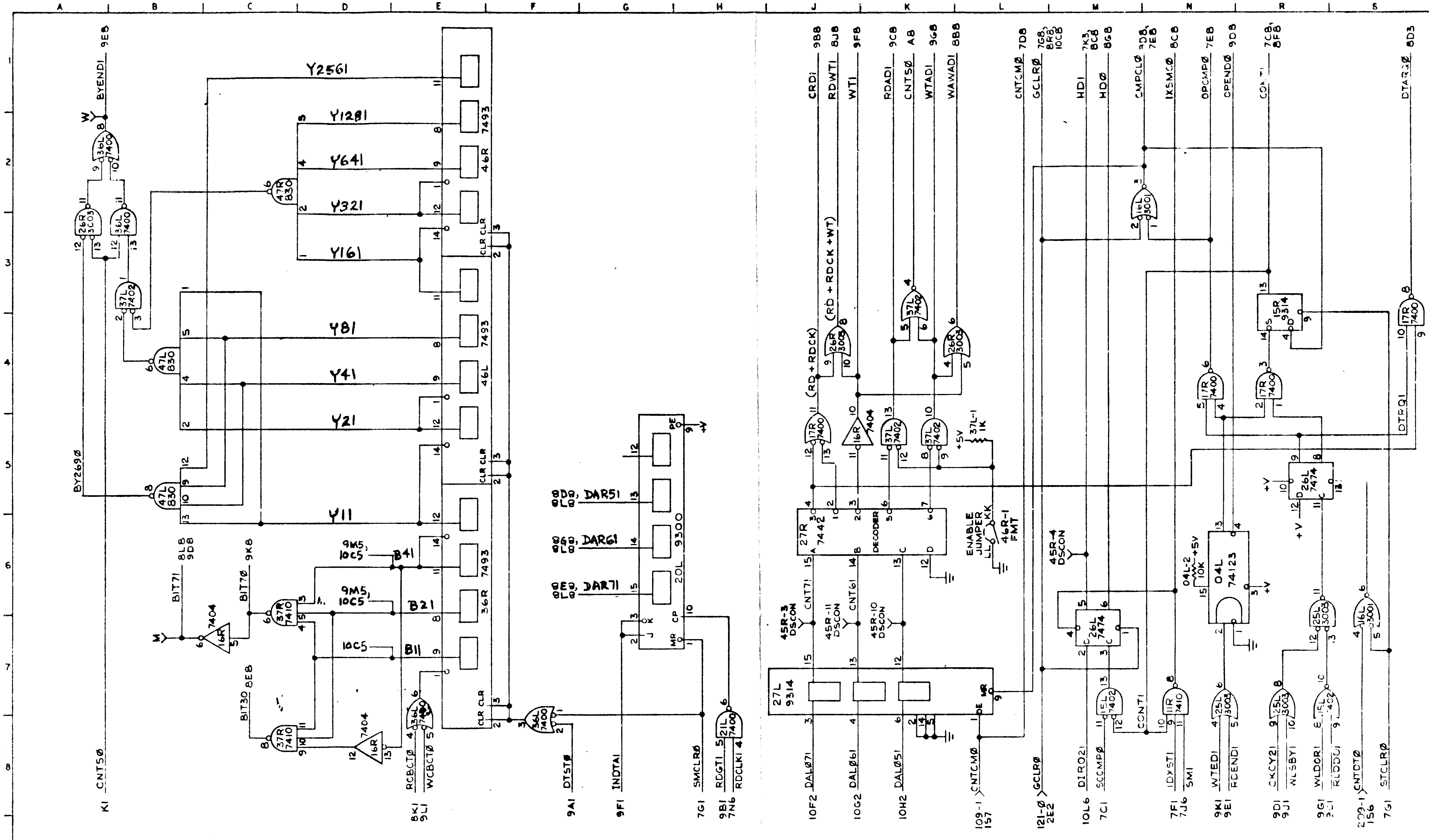


NOTES:
1. APPARATUS ON THIS SHEET IS ON THE F-BOARD. (32/190)

D.A. 26-MAY-71

INTERDATA CONTROLLER, "F" SECTION
FILE ADRS & ENBLE & ARM RFG
INTERNAL RA[illegible]

32/107 B6



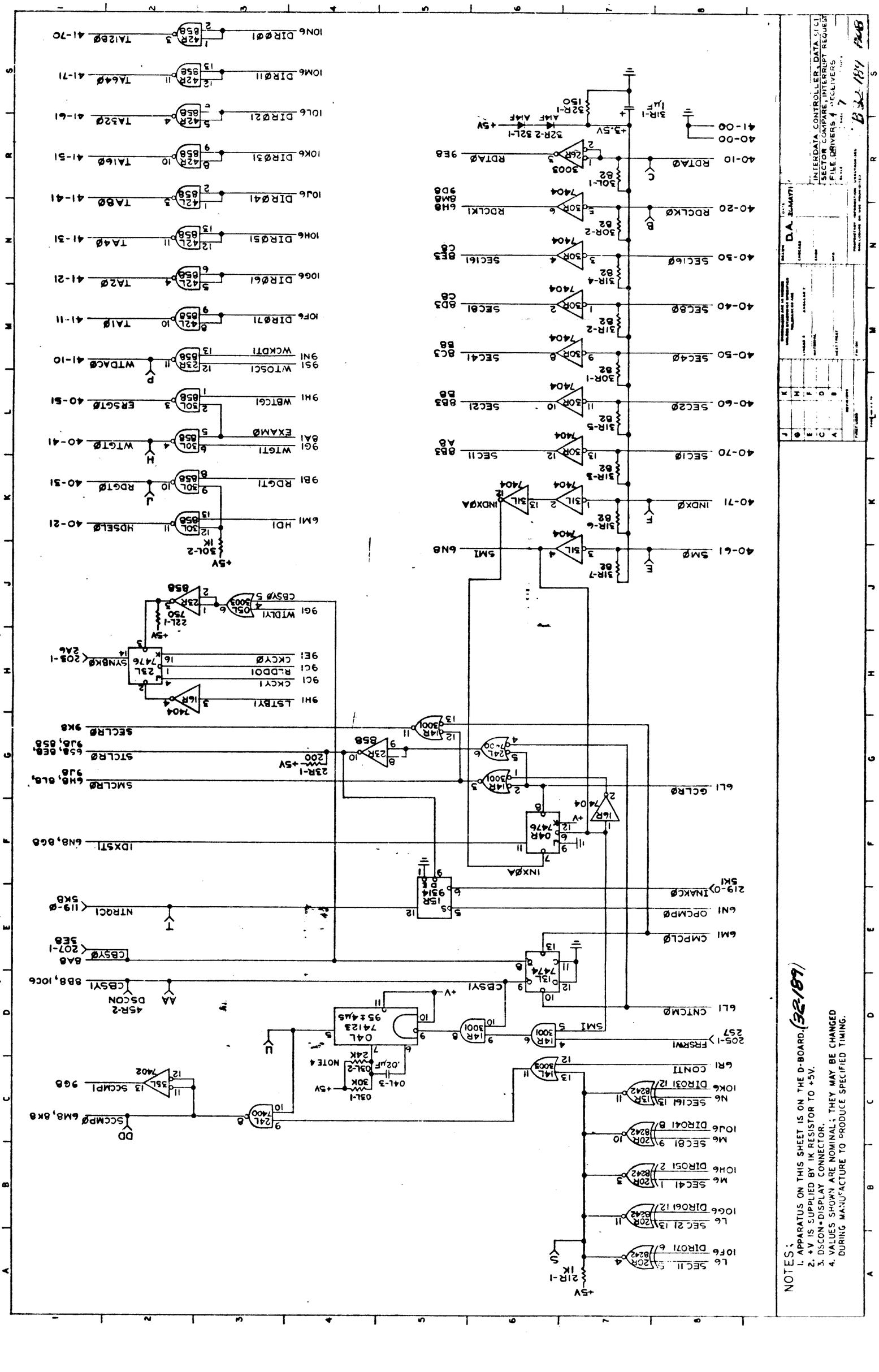
NOTES:

1. APPARATUS ON THIS SHEET IS ON THE D-BOARD (32/B9)
2. +V IS SUPPLIED BY 1K RESISTOR TO +5V.
3. DSCON=DISPLAY CONNECTOR.

D. A. 26MAY71

INTERDATA CONTROLLER, DATA SEC

CONTROLS, COUNTERS, DAR


INTERDATA CONTROLLER DATA SHEET
SECTOR COMPARE, INTERRUPT REQUEST
FILE DRIVERS & RECEIVERS
D.A. BLANATH
NOTES:
1. APPARATUS ON THIS SHEET IS ON THE D-BOARD. (32/89)
2. +V IS SUPPLIED BY IK RESISTOR TO +5V.
3. DSCON=DISPLAY CONNECTOR.
4. VALUES SHOWN ARE NOMINAL; THEY MAY BE CHANGED DURING MANUFACTURE TO PRODUCE SPECIFIED TIMING.

NOTES:

1. APPARATUS ON THIS SHEET IS ON THE D-BOARD. (32189)
2. +V IS SUPPLIED BY IK RESISTOR TO +5V.
3. DSCON = DISPLAY CONNECTOR.
4. VALUES SHOWN ARE NOMINAL; THEY MAY BE CHANGED DURING MANUFACTURE TO PRODUCE SPECIFIED TIMING.

D. A. 26MAY71

INT RDATA CONTROLLER, DATA SECT
DRL MPROR & ERROR DETECTORS
ADDRESS READ, CYCLIC CHECK

NOTES:
1. APPARATUS ON THIS SHEET IS ON THE D-BOARD. (32-189 A.)
2. +V IS SUPPLIED BY 1K RESISTOR TO +5V.
3. VALUES SHOWN ARE NOMINAL; THEY MAY BE CHANGED DURING MANUFACTURE TO PRODUCE SPECIFIED TIMING.

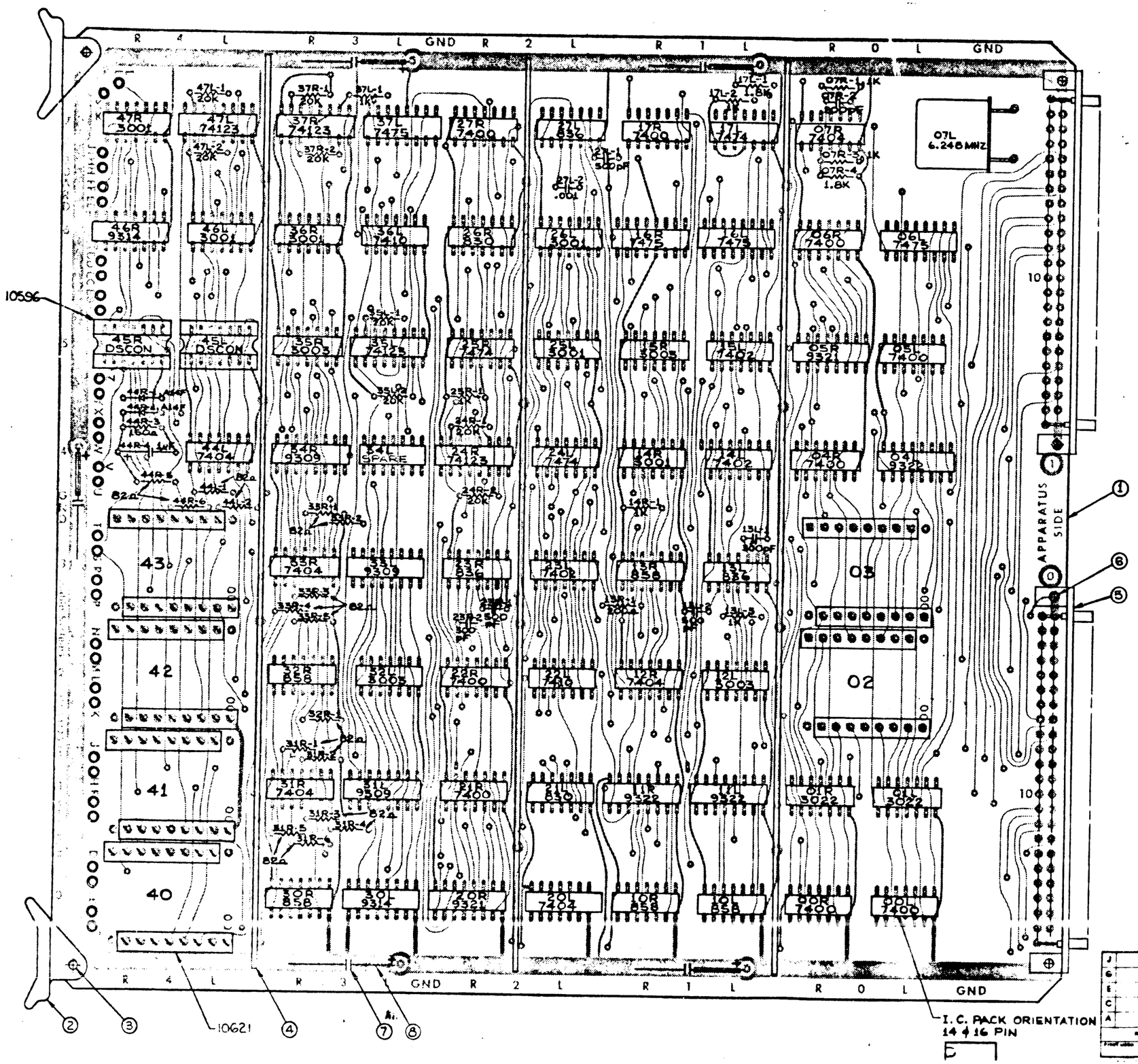
D. A. 26MAY71

INTERDATA CONTROLLER, DATA SECT.
READ DATA & WRITE CONTROLS

32-181 D

8K1 CMPIØ
7404
9 C16R 8
10
11 A
12 B
13 C
8A3
DALØ71 6J8
8B3
DALØ61 6J8
8C3
DALØ51 6K8
8D3
8E3
8E3
8F3
8G3
06R
9312
8 BIT
MULTIPLEXOR
x7 x6 x5 x4 x3 x2 x1 x0
9 7 6 5 4 3 2 1
14
DOROTØ 9M5
DORØ71
DORØ61
DORØ51
DORØ41
DORØ31
DORØ21
DORØ11
DORØØ1
9 10 15 16 9 10 15 16
05R
7475
06L
7475
13 14 7 6 3 2 13 14 7 6 3 2
9C1 RLDDO1
13 05L 3003 11
12
3
05L
3003
2
1
9G1 WLDORI
6D7 B11
6D6 B21
6D6 B41
10
11 A
12 B
13 C
07R
9312
8 BIT
MULTIPLEXOR
x7 x6 x5 x4 x3 x2 x1 x0
9 7 6 5 4 3 2 1
14
4
15L
7402
5 6
7D1 CBSYI
9F1 INDTAI
DIRØ71
DIRØ61
DIRØ51
DIRØ41
DIRØ31
DIRØ21
DIRØ11
DIRØØ1
7M3 7A8
7N3 7B8
7N3 7B8
7R3 7C8
7R3 7C8
6M8 7R3
7S3
7S3
2 3 15 14 13 12 2 3 15 14 13 12
L
K
17L
9300
07L
9300
D
MR PE CP
1 9 10 4 5 6 7 1 9 10 4 5 6 7
6L1 GCLRØ
9A1 DRDGT1
2E4
221-Ø GDAØ
9B1 SWDIRØ
12 16L 3001 11
13
DALØ71 213-1 1L3
DALØ61 113-1 1L3
DALØ51 215-1 1L3
DALØ41 115-1 1L2
DALØ31 217-1 1L2
DALØ21 117-1 1L1
DALØ11 219-1 1L1
DALØØ1 119-1 1L1
10 16L 3001 8 CKDAØ 8F8
9
D.A 26MAY71

NOTES:
1. APPARATUS ON THIS SHEET IS ON THE D-BOARD. (32-1891)



PARTS LISTS			
ITEM	PART NO.	DESCRIPTION	QTY
1	11230	PC BOARD	1
2	10622-01	EJECTOR	2
3	10622-02	MOUNTING PIN	2
4	10623	STIFFENER	3
5	10624	CONNECTOR	2
6	10625	RIVET	4
7	10077-39	CAPACITOR, 39μF 10V	5
8	10568-20	SLEEVE, TEFLON	5

COMPONENT LOCATOR FOR 32-140 BOARD

D.A.

ASSEMBLY "F" BOARD

SCALE 2:1 SIZE 11

B32-187 006

PARTS LISTS			
ITEM	PART NO	DESCRIPTION	QTY
1	11228	P.C. BOARD	1
2	10622-01	EJECTOR	2
3	10622-02	MOUNTING PIN	2
4	10623	STIFFENER	3
5	10624	CONNECTOR	2
6	10625	RIVET	4
7	10077-39	CAPACITOR, 39μF 10V	5
8	10568-20	SLEEVE, TEFLON	5