MODEL 3205 PROCESSOR

OVERVIEW

The Model 3205 is a low-cost, physically small 32-bit Processor designed specifically for the Original Equipment Manufacturer (OEM). The advantage of the Model 3205's processing power and the growth potential of its 32-bit architecture make it suitable for a wide range of applications.

The Model 3205 is packaged in an eight-slot, seven-inch high chassis for mounting in a 19″ EIA cabinet or enclosure. The Model 3205 processor is implemented as a single board with features such as floating point, Selector Channel and up to 1 MB of memory integral to the design. A second board, the Multi-Peripheral Controller (MPC), contains the most commonly used peripheral items such as clocks, a boot loader, eight asynchronous or synchronous communications lines, and a parallel line printer interface. A third board is optional for expansion of memory up to a maximum of four megabytes.

The Model 3205 continues the Perkin-Elmer tradition of providing total upward compatibility within the Series 3200 MEGAMINI® line of products. The Model 3205 offers compatible migration of application and system software to the larger more powerful Series 3200 systems. The Model 3205's compatibility extends beyond software in that it can use all Series 3200 high-performance peripherals.

PRODUCT DESCRIPTION

The Model 3205 is designed to fill application needs which require very low-cost 32-bit processing power. Figure 1 is a functional block diagram of the Model 3205 and shows the breadth of capabilities that exists within this product. The Model 3205 provides the ideal entry into the Series 3200 processors for the following reasons:

- Small Physical Size — the Model 3205 comes in a chassis 7 inches high x 19 inches wide x 17 inches deep for ease of placement and cooling, thus reducing extensive mechanical and packaging requirements.
- 32-bit Architecture — The Model 3205 supports the full line of features characteristic of the Series 3200, thus allowing the user to take advantage of one family of products, regardless of application.
- Extensive User Available Registers — The Model 3205 incorporates eight sets of sixteen 32-bit general-purpose registers. Register-to-register instructions permit operations between any of the 16 registers within a set, eliminating redundant loads and stores. One set of registers is dedicated for handling the external interrupt level. Multiple register sets alleviate the need to save and restore the general registers every time there is a context switch, thus significantly reducing the context switching time.

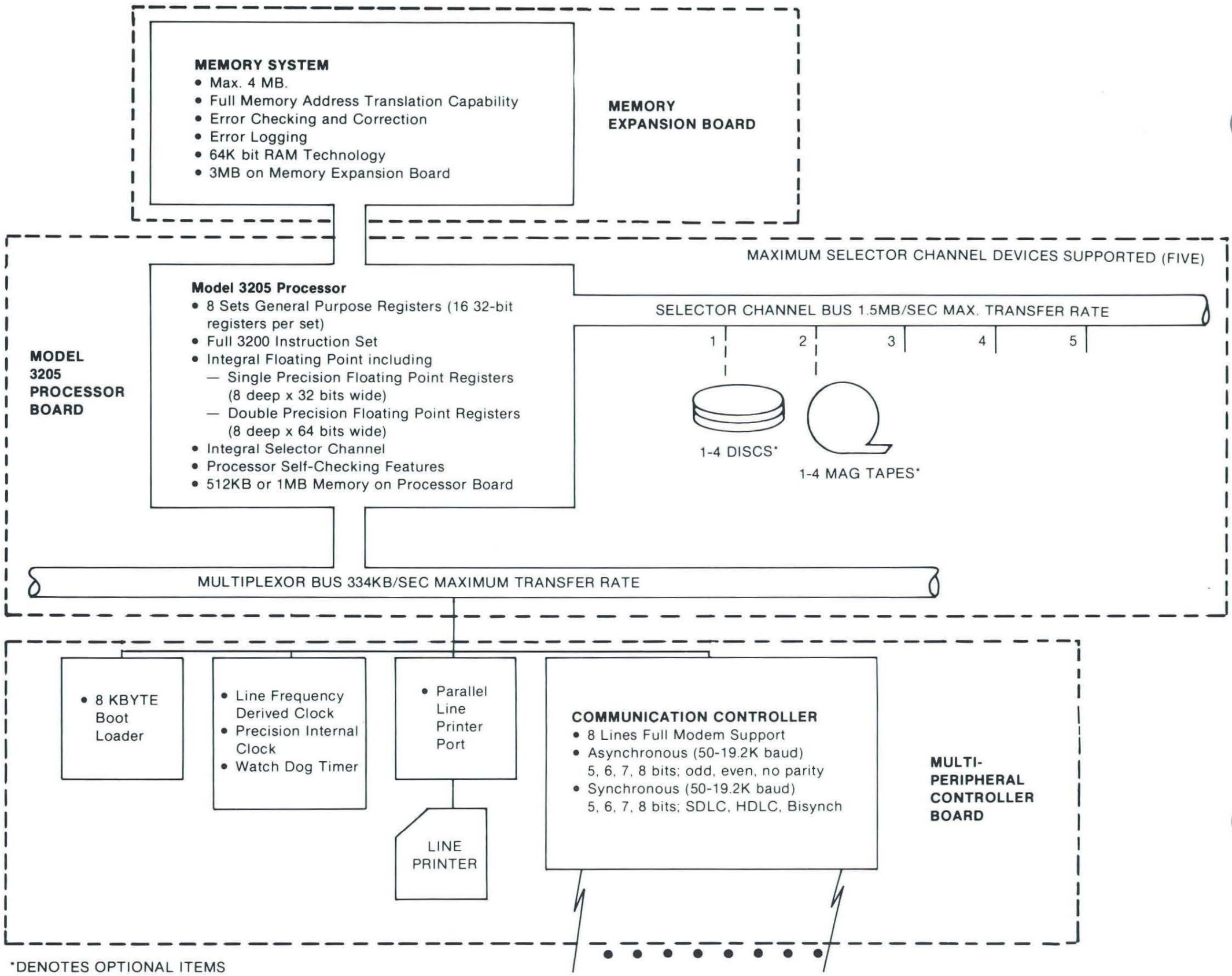


FIGURE 1. MODEL 3205 BLOCK DIAGRAM

- Comprehensive Instruction Set — The Series 3200 instruction set includes a comprehensive array of instructions for general-purpose processing. The Model 3205 includes, as standard in its repertoire of instructions, a full set of single and double precision floating point instructions.
- Memory Management — Integral to the processor is a Memory Manager which provides memory segmentation, relocation and protection under operating system control. This feature provides translation of a program address into a physical memory address. It also provides read, write and execute protection for specified blocks of memory. Memory management ensures that a task can exist in a fully protected environment.
- Dual Bus Architecture — The Model 3205 supports two communications buses: A man/machine path referred to as the Multiplexor Bus, and a high-speed machine/machine path, referred to as the Selector Channel Bus. The I/O configuration can thus be optimized to meet specific application needs.

MEMORY SYSTEM

The Model 3205 supports up to four megabytes of directly addressable main memory using 64K RAM technology. This memory uses state-of-the-art leadless carrier packaging technology for substantial reduction in physical size. This enables the processor to support up to one megabyte on the CPU board with an additional three megabytes of memory being packaged on the memory expansion board. Memory is expandable in increments of one, two or three megabytes.

- Error Correcting Code — Error detection and correction is a standard feature of the Model 3205 memory system. Error correction is performed via a modified Hamming Code. Additional bits on each word in memory allow detection and correction on all single-bit errors. All double-bit errors and some multi-bit errors are detected.
- Error Logger — The Error Logger is a standard feature of the Model 3205. It records data that allows the identification of error trends. The collected data is used to isolate faulty memory chips before they affect memory system reliability.

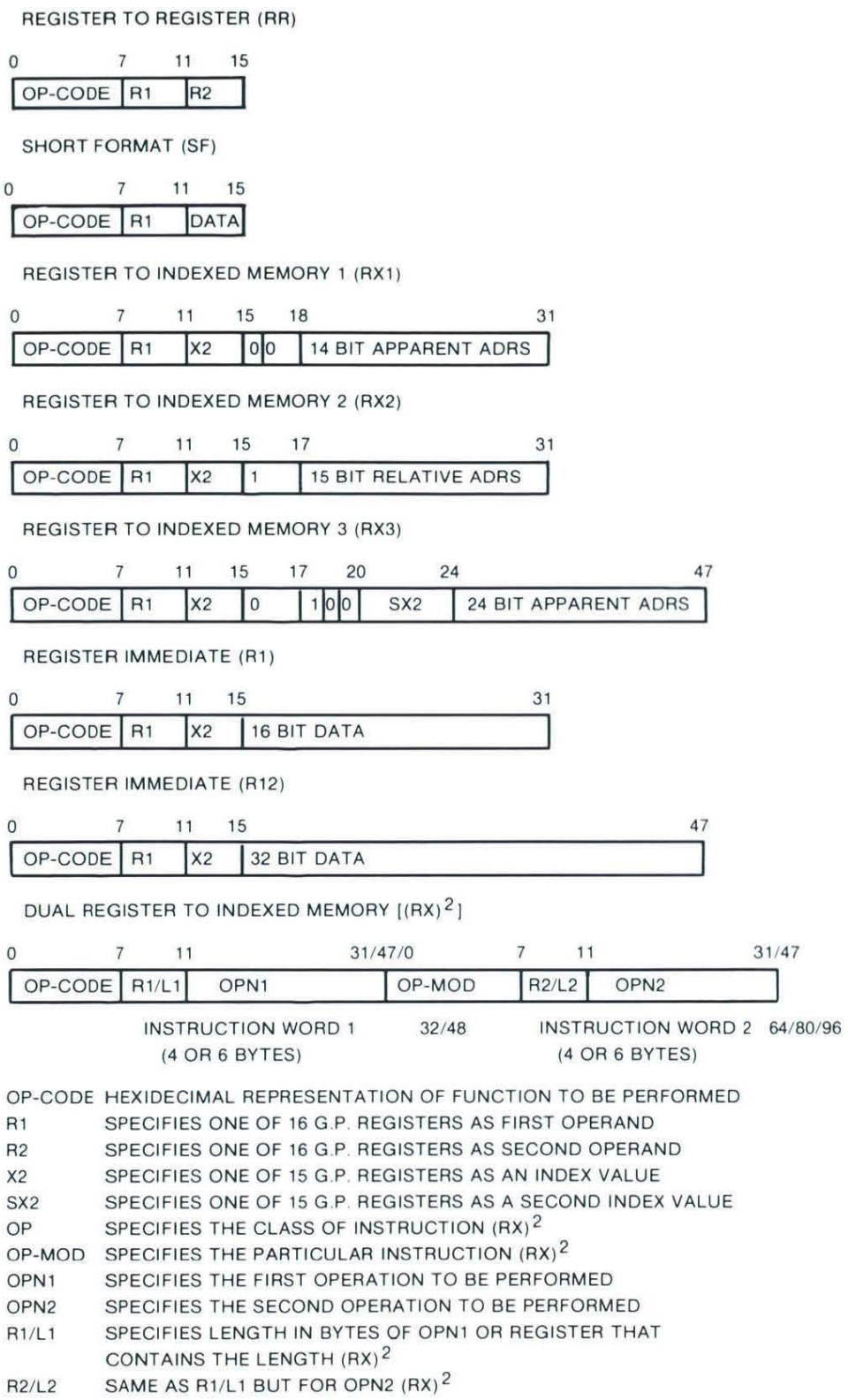
- Battery Backup — Since MOS memory is volatile, the Model 3205 options include a battery power retention system. It provides power to maintain the contents of the memory, based on the configuration, for up to 8 minutes. When line power is lost, the battery system automatically provides the power to maintain memory contents. Upon restoration of power, the processor reloads its registers and resumes operation.

INSTRUCTIONS

The Series 3200 instruction set is a comprehensive array of instructions for simulation, scientific, seismic, CAD/CAM, data communications, commercial and general applications. The instruction set performs the following classes of operations:

- Load/store halfwords, fullwords and multiple words
- Fixed-point arithmetic on halfwords and fullwords
- Logical operations (AND, OR, exclusive OR, Compare and Test) on halfwords or fullwords
- Logical and arithmetic shifts and rotation of halfwords and fullwords
- Extensive bit manipulation
- Floating-point arithmetic on single (32-bit) and double (64-bit) precision operands
- List operations
- Data handling operations
- Input/output
- Byte manipulations
- Privileged system functions
- Storage-to-storage functions
- Decimal conversion

The Series 3200 instruction set uses the eight different instruction formats illustrated in Figure 2.



OP-CODE HEXIDECIMAL REPRESENTATION OF FUNCTION TO BE PERFORMED
R1 SPECIFIES ONE OF 16 G.P. REGISTERS AS FIRST OPERAND
R2 SPECIFIES ONE OF 16 G.P. REGISTERS AS SECOND OPERAND
X2 SPECIFIES ONE OF 15 G.P. REGISTERS AS AN INDEX VALUE
SX2 SPECIFIES ONE OF 15 G.P. REGISTERS AS A SECOND INDEX VALUE
OP SPECIFIES THE CLASS OF INSTRUCTION (RX)2
OP-MOD SPECIFIES THE PARTICULAR INSTRUCTION (RX)2
OPN1 SPECIFIES THE FIRST OPERATION TO BE PERFORMED
OPN2 SPECIFIES THE SECOND OPERATION TO BE PERFORMED
R1/L1 SPECIFIES LENGTH IN BYTES OF OPN1 OR REGISTER THAT CONTAINS THE LENGTH (RX)2
R2/L2 SAME AS R1/L1 BUT FOR OPN2 (RX)2

FIGURE 2. SERIES 3200 INSTRUCTION FORMATS

I/O ARCHITECTURE

The Model 3205 incorporates two communications buses. The man/machine Multiplexor Bus interfaces medium-speed devices such as printers, consoles, card readers, etc.

The machine/machine Selector Channel Bus interfaces secondary storage devices such as discs and magnetic tapes. Thus, the I/O configuration can be optimized to specific application needs.

MULTIPLEXOR BUS

The Multiplexor Bus supports up to 1023 device addresses. The register set associated with the I/O interrupt level speeds context switching.

Data transfers over the Multiplexor Bus are accomplished in two ways:

(1) A byte or halfword transferred between a Multiplexor Bus device and memory, under control of an I/O instruction.

(2) The Auto Driver Channel transfers blocks of data between a Multiplexor Bus device and the memory. This is accomplished via interrupt driven control store sequences. The Auto Driver Channel offers faster and more efficient operation than the comparable assembly-level instruction sequences. The channel performs automatic character translation and computes CRC/LRC values used in communication devices.

SELECTOR CHANNEL BUS

The Selector Channel Bus supports data transfers to and from memory. The Selector Channel is programmed using the Multiplexor Bus commands. Once the channel is activated, the processor is free to continue processing. The Selector Channel initiates and terminates data transfers. The Selector Channel can support 5 device controllers and transfers bytes or halfwords to or from the memory. Selector Channel controllers typically support four devices.

The Selector Channel transfers data to or from the memory by employing a cycle stealing operation. Once initiated, the Selector Channel functions in a completely autonomous fashion with one controller or device actively transferring data at any one time.

Data transfer is programmed by loading a starting and ending address to specify the address range for the data transfer. A GO command is then issued by the processor and the data transfer proceeds without further direction from, or interaction with, the processor. The GO command also inhibits activity with the processor and any other device on the Selector Channel Bus. All set-up commands for controller and channel operation are transferred via the Multiplexor Bus.

Upon termination of the data block transfer, the Selector Channel interrupts the processor to signal activity completion. The processor then returns the Selector Channel to an idle mode.

When idle, the Selector Channel Bus is connected to the Multiplexor Bus and functions as a bus buffer.

MULTI-PERIPHERAL CONTROLLER

The MPC uses state-of-the-art microprocessor technology to implement the most commonly used input/output functions on a single card. A list and characterization of these features is as follows:

- Eight RS-232 full duplex communication lines. These lines support anynchronous, synchronous, SDLC, HDLC or BISYNC operations. Line speed capabilities are from 50-19.2K baud in any mode. Full modem support is offered on all lines.
- Data Handling Assist — The Data Handling Assist is primarily used for data communications applications and provides fast, more efficient operation. Two instructions, Process Byte and Process Byte Register, are used to calculate a cumulative checksum based on an old checksum and a new data byte. The check can be used for BISYNC or SDLC protocols.
- Loader Storage Unit — The OS/32 operating system is automatically loaded from a secondary storage device. This can occur after a power fail/restart sequence or upon operator intervention for initial program load. The loader performs additional memory/processor tests before the operating system is loaded.
- Universal Clock — Includes a programmable precision interval clock and an AC line frequency derived clock.
- Watchdog Timer — The watchdog timer interrupts the processor if deadlocked and forces a system reload through the Loader Storage Unit.
- A Parallel Line Printer Port — Provides the capability of supporting line printers with parallel interfaces from 120 CPS to 200 lines per minute.
- Self-Test Feature — Upon power up, the MPC tests itself for board integrity.

RELIABILITY/MAINTAINABILITY

The Model 3205 continues to reinforce Perkin-Elmer's reputation for producing the most reliable 32-bit processors in the marketplace today. Features that provide the highest kind of reliability and maintainability have been designed into all aspects of component production and continue with one of the most extensive system testing procedures in the industry. These features include:

- Self Test — When power is applied to the system, the basic memory and processor functions are tested. Additional memory and processor checks are performed when the operating system is loaded.
- Register Parity — Parity is provided on all user level registers in the system to ensure integrity of data.
- Reduced Component Count — Use of VLSI and LSI technology permits higher density packaging on each board and reduces the number of board intraconnects.
- Power Fail/Auto Restart (PF/AR) — Provides system integrity in case of power failure. Upon power restoration, the processor will restore its environment and resume operation.
- Illegal Instruction Trap — All instruction operation codes are tested for validity prior to execution. Invalid instructions are trapped and execution is prevented. An illegal instruction interrupt is generated.
- Error Checking and Correcting (ECC) — The ECC feature will detect and correct all single-bit errors, detect all double-bit errors, and detect some multiple-bit errors.
- Memory Error Logging — The error log is a journal of memory recorded errors that have been detected by the ECC and logged under OS/32. The contents of the journal can be examined at any time in the form of a report. Suspected problems in memory can be repaired during scheduled preventive maintenance periods, eliminating costly downtime.
- Diagnostics — Multimedia diagnostic programs for the processor, memory and all peripherals are available with the purchase of the operating system.
- Remote Diagnostics — Provides the ability to remotely demonstrate a hardware problem to a highly trained support engineer located in one of Perkin-Elmer's nationwide service centers. The Remote Center can completely exercise and diagnose the system.
- Product Testing — An extensive automated test process which includes testing through the full operational temperature range.

COMPATIBILITY

The Model 3205 is user software compatible with all other Perkin-Elmer Series 3200 processors. This protects user software investments and provides cost-effective growth potential. All Series 3200 processors run under Perkin-Elmer's standard operating system, OS/32, and Edition VII Workbench* (similar to UNIX** Software) with all high-level languages being totally compatible.

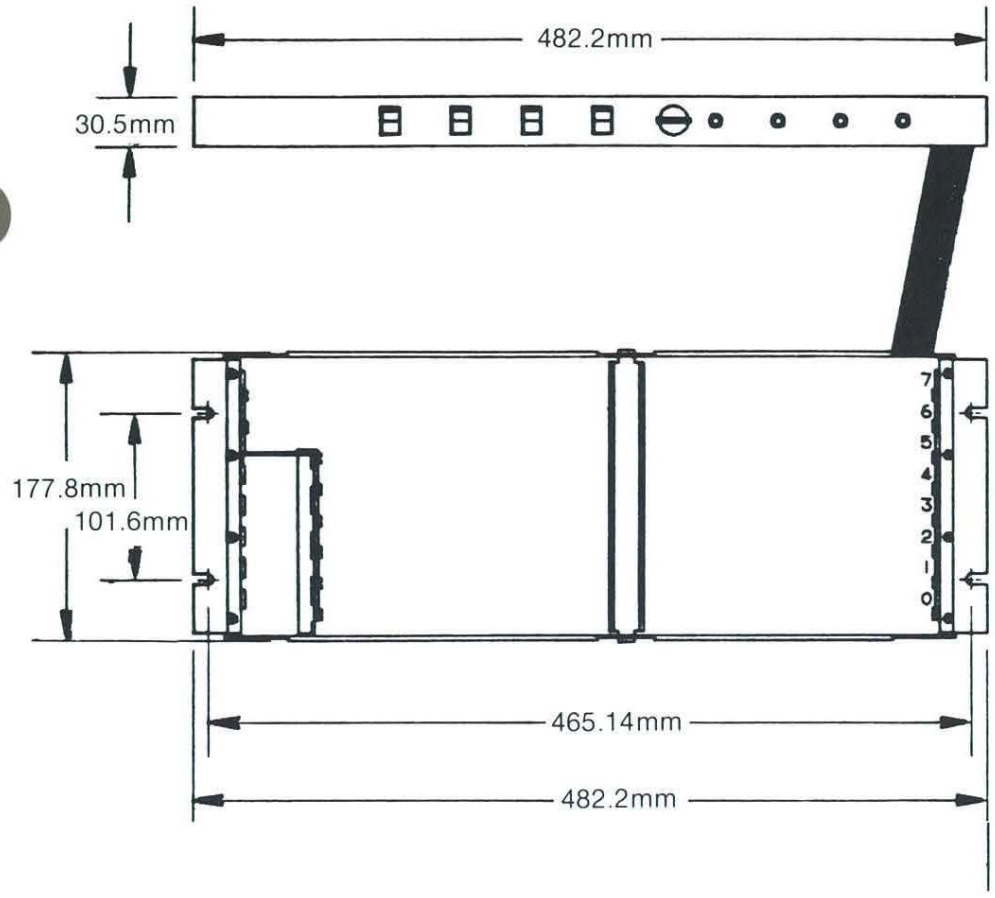
PACKAGING

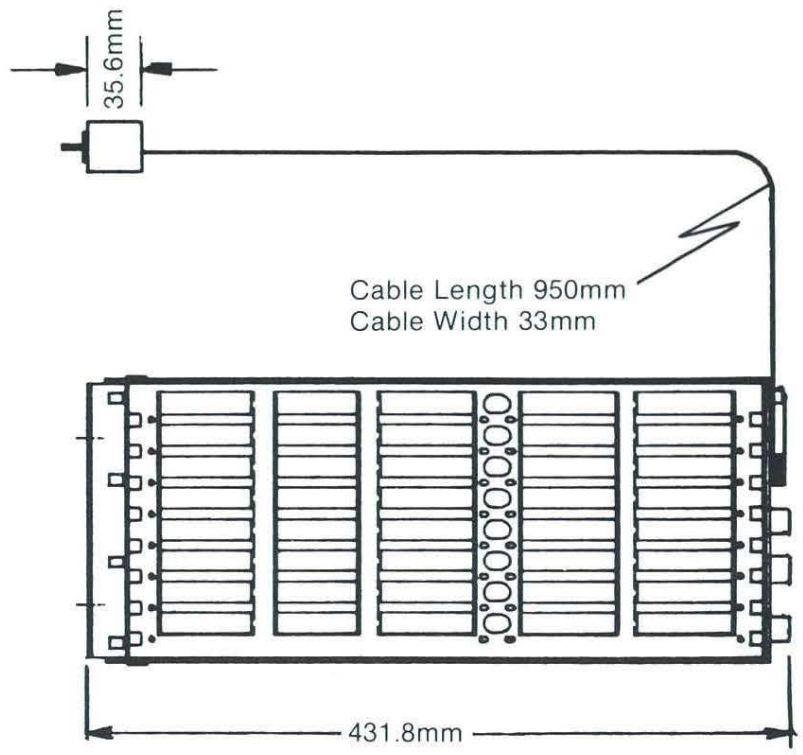
The Model 3205 is contained in a single chassis as shown in Figure 3. The backpanel provides for modular connection and forms an integral member of the chassis for increased rigidity. Bullet pins are used on the backpanel for ease of board alignment and additional board support. Board connections to the backpanel are via a two part connector system using gold plated .025 inch square pins. This ensures maximum power and signal integrity throughout the system. Full side board supports, front edge retaining bars, and on board stiffeners ensure added support and elimination of problems from shock and vibration.

Cooling is accomplished via a side mounted fan assembly with the air flow going from right to left across the boards.

The optional power subsystem connects to the back-

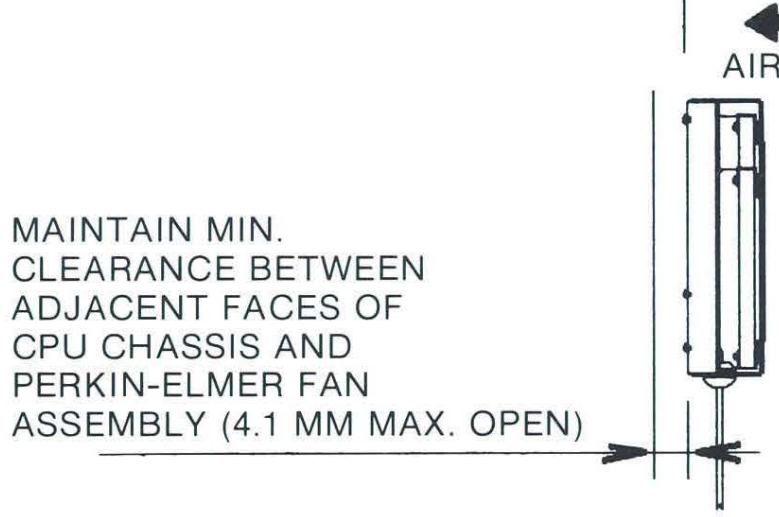
*Edition VII Workbench is a product of The Wollongong Group.
**UNIX is a trademark of Bell Laboratories.

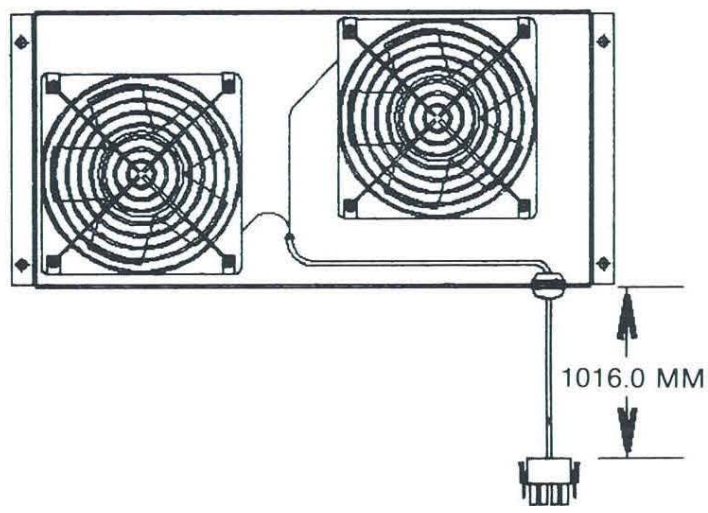




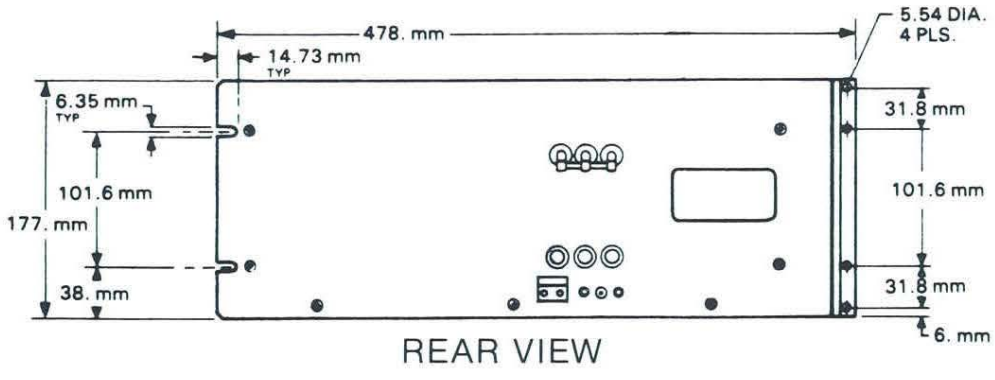
AIR FLOW

FAN ASSEMBLY

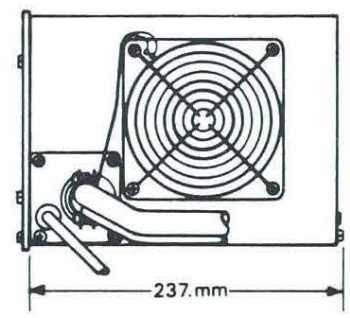




POWER SUPPLY PHYSICAL SPECIFICATIONS



REAR VIEW



SIDE VIEW

FIGURE 3 — CPU CHASSIS

panel via a 28 inch cable for ease of positioning behind, above or below the chassis.

The operator control panel is connected via a 950 mm (37.4 inch) flat ribbon cable for convenient location.

Specifications

Technology

Processor: VLSI,LSI,MSI
Memory: LSI
MultiPeripheral Controller: VLSI,LSI,MSI

Processor

General Registers: 8 sets of 16, 32 bit wide

Floating Point Registers: 8 single precision floating point registers, 32 bits wide
8 double precision floating point registers, 64 bits wide

User Instructions: 202 instructions including floating point commercial and data handling

Address Range: 4 MB real, 16 MB virtual
Addressing Modes: Direct, program relative, single and double indexing

Micro-Instruction Word Size: 64 bits
Micro-Instruction Cycle Time: 200 ns
Control Store Size: 64-bit x 4K words

Memory

Type: 64K Dynamic RAM
Correction Mechanism: ECC and Error Logging
Access Time: 300 nanoseconds
Cycle Time: 400 nanoseconds
Minimum Size: 512KB
Maximum Size: 4MB
Battery Backup for Main Memory: up to eight minutes

Input/Output

Multiplexor Bus —
- Device Addresses: 1023
- Maximum Transfer Rate: 334 Kbytes/Second
- Priority: 1023 Hardware vectored positional priorities
- Interrupt Levels: One

Selector Channel Bus —
- Maximum Transfer Rate: 1.5 MB/SEC maximum
- Maximum Number of Controllers: 5 independent device controllers
- Addressing Capability: 16 Megabytes
- Data Transfer Formats: Bytes (8 bits), halfwords (16 bits)
- Memory Access Method: Memory Cycle stealing

Multi-Peripheral Controller
- Clock Types:
- Precision Interval:
  - Accuracy: ± .01% Crystal Controlled Oscillator
  - Resolution: 1μs, 10μs, 100μ, 1ms
  - Interval: 1ms to 4095ms
- AC Line Frequency:
  - Interval: 8.33ms on 60Hz line
  - 10 ms on 50Hz line
- Line Printer Port:
  - Centronics-type, parallel interface with loopback for self-check
  - Devices Supported:
    - 120 CPS to 180 CPS Matrix Printers
    - 300 LPM to 1200 LPM Band Printers (64 character set 132 columns Print Operation)

Communications Capability:
- Number of Lines: Eight full duplex, software selectable for asynchronous or synchronous operation
- Communication Lines Interface: RS-232C
- Data Rate: 50 to 19.2K baud asynchronous or synchronous, independently selectable baud rates
- Character Format: Programmable, 5, 6, 7, 8 bits
- Parity: Programmable, odd, even or none
- Modem Control: Programmable control for asynchronous or synchronous operation
- Communications Protocols:
  - Asynchronous
  - Synchronous — binary synchronous,
  - Zero-bit insertion/deletion (ZBID) and flag insertion/deletion as required for bit oriented protocols such as SDLC, HDLC and ADCAP

Power Subsystem (Optional)
- Regulation: Off-line switching using pulse width modulation
- Frequency: 25 KHz
- Protection: Overvoltage, overcurrent, high temperature, short circuit
- Orderly Shutdown: Signal (PFDT) to CPU on loss of power
- AC Power Requirement for Optional Power Subsystem:

AC Voltage:	90-132 VRMS	180-264 VRMS
Frequency:	47-63Hz	47-63Hz
Phase:	3-wire single phase	3-wire single phase
Input hardware rating:	20 amps	15 amps
Circuit breaker rating:	20 amps	15 amps
Power Cord Length:	711mm (28 inches)	711mm (28 inches)

Physical Characteristics —
- Processor Dimensions: 177mm (7.0 in) Height
  - 482.2mm (19 in) Width
  - 432mm (17in) Depth
- Unpackaged Weight: 17.69 Kg (39 lb)

Optional Power Subsystem
- Dimensions: 177.0mm (7 in) Height
  - 478.0mm (18.82 in) Width
  - 237.0mm (19.4 in) Depth
- Unpackaged Weight: 7.26 Kg (16 lb)

Environment —
- Temperature
- Operating: 0° to 50°C
- Storage: -55° to 85°C

Humidity
- Operating: 50-90% (non-condensing)

Vibration:
- Operating: 0-55 Hz, 1.25 G's @ 55 Hz

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Printed in U.S.A. April, 1983