CPZ - 4800X

SINGLE BOARD CENTRAL PROCESSOR

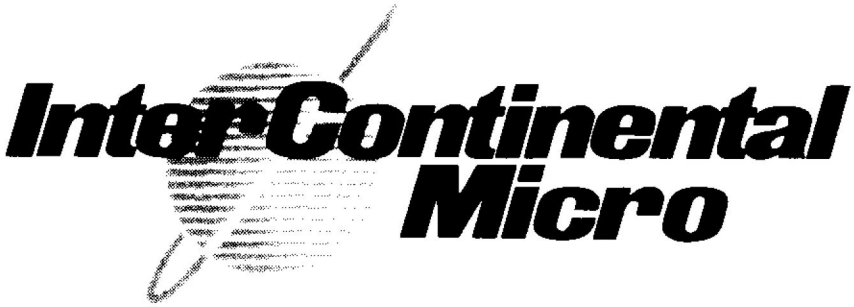

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TABLE OF CONTENTS

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**** INTRODUCTION ****

The **INTERCONTINENTAL MICRO SYSTEMS CORP.** (**ICM**) CPZ-4800X single board central processor (SBCP) is a Z80A (tm) [CPZ-48004] or Z80B (tm) [CPZ-48006] based computer board designed to meet or exceed the IEEE S-100 Bus specification. This third generation computer incorporates all the features necessary for a complete, stand alone CP/M (tm) system and is perfect for use in multi-processor or multi-user /multi-tasking architectures utilizing operating systems such as TurboDOS (tm), MP/M (tm), OASIS (tm) and CP/NET (tm).

Features such as an independent interrupt structure, Direct Memory Access, a 16 Megabyte Memory Management Unit and a bank selectable on-board 64K byte memory coupled with I/O devices such as a floppy disk controller which controls 5 1/4" or 8" drives simultaneously, a 2-port serial controller and a 2-port parallel controller provides the user computing power on a single board heretofore unmatched in the S-100 Bus industry. Other features incorporated are listed as follows:

FEATURES

* IEEE S-100 Bus Compliance
* Z80A (tm) 4MHz Operation [CPZ-48004] or Z80B (tm) 6MHz operation [CPZ-48006]
* Single or Double Density Floppy Disk controller with up to four 8", four 5 1/4" or four 8" and 5 1/4" floppy drives in any combination programmable in either DMA, Interrupt or programmed I/O mode
* Two Serial I/O channels with one channel programmable in either DMA, Interrupt or Programmed I/O mode.
* Two Parallel I/O channels with one channel programmable in either DMA, Interrupt or Programmed I/O mode.
* Four Channel Direct Memory Access Controller
* 64 Kbytes of On-Board Dynamic RAM with Memory Deselect of 4 Kbytes to 64 Kbytes under software control
* Memory Management of 16 Megabytes of system memory
* Eighteen Vectored Priority Interrupts chained together with I/O Interrupts for use with Z-80 Mode 2 Interrupts
* Provisions for either a 2 Kbyte, 4 Kbyte or 8 Kbyte on-board EPROM (Monitor in a 2 Kbyte EPROM supplied with board.)
* Software Selectable Baud Rates
* Real Time Clock
* Synchronous or Asynchronous operation using the Z80 SIO chip
* CP/M (tm), MP/M (tm) and TurboDOS (tm) Operating Systems available
* Turbo-Disk (tm) Implementation Included with Software

CPZ-48000 Single Board Computer

A HOST OF USES

As the most sophisticated, competitively priced Single Board Computer (SBC) in the S-100 market, the CPZ-48000 series is more than just a CPU. It will act as a sophisticated single board Personal Computer or as a master CPU in a master slave network. The CPZ-48000 can also be used as a single processor, multi-user/multi-tasking host, or as a CPU with high speed serial data link for local area networking.

In both 4 and 6 MHz versions, the CPZ-48000 is fast and versatile, but don't be deceived by clock rate alone—the CPZ-48000 provides many advantages for system architectures requiring high speed and high throughput processing. In fact, our **4 MHz** CPZ-48004 with our memory mapped slaves is 37% faster than the competitions' **6 MHz** master, I/O mapped slave combination. Our 6 MHz CPZ-48006 master is 106% faster.

That's because a powerful on-board Memory Management Unit (MMU) controls 24 bits of address for up to 16 MBytes of extended memory, equal to or better than any 16 bit CPU available today.

THERE'S MORE

- ☐ IEEE 696.1/D2 S-100 compliance. The CPZ-48000 will interface with most IEEE S-100 bus products on the market.
- ☐ RS232 communications and floppy controller Personality Boards included.
- ☐ 6 MHz Z80B, 4 MHz Z80A Operation.
- ☐ Floppy disk controller (FDC) with on-chip data separator. Single or double density, 8" and 5¼" in any combination. The choice is yours, up to 4 drives.
- ☐ Two synchronous or asynchronous serial I/O channels (SIO). One channel can be programmed in direct memory access (DMA), interrupt, or programmable I/O mode.
- ☐ Two parallel I/O channels (PIO). One channel is programmable in DMA, interrupt or programmable I/O mode.
- ☐ Four channel DMA controller.
- ☐ 64K on-board RAM. Bank selection puts from 4K to 64K under software control.
- ☐ Memory management unit (MMU). Addresses up to 16 megabytes of system memory.
- ☐ Eighteen vectored priority interrupts are chained with serial and parallel I/O interrupts for use with Z-80 mode 2 interrupts.
- ☐ Provisions for 2K, 4K or 8K on-board EPROM. A boot up function and monitor in a 2K EPROM is supplied.
- ☐ Software selectable baud rates. Eliminates costly, complicated hardware modifications to change baud rates. Up to 800K BAUD in synchronous mode, 50K BAUD in asynchronous mode.
- ☐ IBM Bisync, HDLC, SDLC and other protocols. All are handled through a Z-80 SIO chip. Permits communication with micro's, mini's or mainframes.
- ☐ CP/M,™ MP/M™ and TurboDOS™ operating systems available.
- ☐ Turbo-Disk® implementation included.

INDEPENDENT COMPARISON OF S-100 SBC's BY MICROSYSTEMS MAGAZINE

FEATURES	ICM	TELETEK	SIERRA	ADC
Channels of DMA	4	4	0	4
Memory Management Unit (16 MByte	YES	NO	NO	NO
Interrupt Control	VECTORED PRIORITY	NO	PIO	PIO
RAM Disk Software	YES	NO	NO	NO
Window Deselection	YES	NO	NO	NO
Peripheral Interface Through Personality Boards	YES	NO	NO	YES

A 4-channel Direct Memory Access (DMA) controller provides data transfer rates over 300% faster than standard Z80™ block move rates. DMA transfers off-board memory directly, bypassing the CPU. No other S-100 SBC offers **both** MMU and DMA in combination. Significant increases in speed result.

Vectored Priority Interrupt (VPI) allows the CPU to recognize and prioritize simultaneous service requests for up to 18 interrupt sources. VPI increases CPU efficiency and eliminates potential data loss due to simultaneous service requests, often a problem with standard "polled I/O" methods.

Turbodisk (RAM disk) allows any extended address RAM memory to emulate a disk, and is the fastest method of storing and retrieving data in the S100 market. Transfer rate in file accessing is 1 MByte/sec—vs—60KByte/sec floppy or .5 MByte/sec hard disk rates.

Peripheral Interface through ICM's small, inexpensive personality boards allows extremely versatile interfacing and eliminates costly modifications to the CPU. New personality boards are constantly being developed as new peripherals are introduced into the market.

TurboDOS,™ CP/M™ and MP/M™ compatible. TurboDOS is compatible with virtually all off-the-shelf CP/M application software. Since CP/M has been the standard 8-bit Operating System for a number of years, there are literally thousands of applications software packages readily available.

Master/Slave Networking allows putting up to 1 master (CPZ 48000) and 16 slaves (CPS-MX) in an S-100 bus. Up to 16 masters can be networked together for 256 users with an ethernet or arcnet S-100 board. Each slave CPU can act independently of the master, so each user has a dedicated processor, making the network much faster than a shared processor multiuser system. Master/Slave networks are also very cost effective—all users can share common peripherals. Overall, savings of up to 65% can be realized by using a Master/Slave TurboDOS Network as opposed to a PC OMNINET.™

In short, the CPZ-48000 series is sophisticated and fast. The CPZ-48004 and CPZ-48006 offer more processing power and yet are some of the most competitively priced SBC's on the market.

HOW USING OUR WHOLE PRODUCT LINE WILL HELP YOU

The CPZ-48000 CPU, CPS-MX slaves, and 256KMB-100 memories from Intercontinental Micro Systems give you the perfect team for the most demanding of tasks—multi-user/ multi-tasking, RAM disk or single user functions.

WE'VE GOT PERSONALITY

So you've got a sophisticated Single Board System. It won't do you much good if you can't interface with peripherals. Intercontinental Micro has designed a full line of personality boards that allow you to interface with anything from floppies to hard disks including modems and printers. They're also small and won't take up any S100 Bus space.

Here it is in black and white. Have a look. Then give us a call. We'd love to help with your CPU or single board system applications.

MICROPROCESSOR
Clock rate...6 MHz Z80B CPZ-48006 or 4 MHz CPZ-48004

BUS INTERFACE...IEEE 696, 1/D2 S100

SERIAL I/O CHANNELS
Synchronous Operation
- Baud Rate...Up to 800 K Baud
- Data Transfer...DMA, Interrupt or Programmed I/O

Asynchronous Operation
- Baud Rate...Up to 50K Baud
- Clock Rate...1, 16, 32 or 64 Times Baud Rate
- Bits/Character...5, 6, 7 or 8
- Stop Bits...1, 1½ or 2
- Parity...Odd, Even or None
- Data Transfer...DMA, Interrupt or Programmed I/O
- I/O Interface...Through Personality Boards

PARALLEL I/O CHANNELS
- Data Rate...Up to 300 KBytes/Sec
- Channel A Data Transfer...DMA, Interrupt or Programmed I/O
- Channel B Data Transfer...Interrupt or Programmed I/O
- Interface Signals...16 Data Lines Plus 4 Handshaking Lines
- I/O Interface...Through Personality Boards

FLOPPY DISK CONTROLLER
- Data Rate/8-Inch Single-Density...250,000 Bits/Sec
- Data Rate/8-Inch Double-Density...500,000 Bits/Sec
- Data Rates/5¼-Inch Single-Density...125,000 Bits/Sec
- Data Rate/5¼-Inch Double-Density...250,000 Bits/Sec
- Format...IBM 3740 or 512 x 16 Sectors
- Data Transfer...DMA, Interrupt or Programmed I/O
- I/O Interface...Through Personality Boards

INTERRUPT CONTROL
- Number of channels...18
- Priority...Rotating or Fixed
- Interrupt Modes...Z80 Mode 0, Mode 1 or Mode 2

REAL-TIME CLOCK
- Operation...Software Polled or Interrupt Driven
- Range...37.5 Hz to 1.2288 MHz

64K DYNAMIC RAM MEMORY
- Bank Selection...May be bank selected in increments of 4K to 64K commencing at 4K boundaries, e.g., 8K of memory may be selected or deselected commencing at location C000 (hex) as defined by software
- Wait states...None
- Direct Memory Transfers...To/From SIO, PIO or FDC

DIRECT MEMORY ACCESS CONTROLLER
- Channel 0...Cascade Mode for IEEE S-100 Bus or Used with Channel 1 in Memory to Memory Transfers
- Channel 1...Channel A of SIO Controller
- Channel 2...Floppy Disk Controller
- Channel 3...Channel A of PIO Controller

DIRECT EXTERNAL MEMORY TRANSFERS
To/From SIO, PIO or FDC

EPROM
- Type...2716 2K EPROM, 2732 4K EPROM or 2768 8K EPROM
- Wait States...None with CPZ-48004, 1 in CPZ-48006
- Function...Boot up and monitor

POWER REQUIREMENTS
- Voltages...+8 VDC @ 2.2A (max)
  +16 VDC @ 0.2A (max)
  −16 VDC @ 0.15A (max)
- Power...23W (max)

OPERATING ENVIRONMENT
- Temperature...0 to 45 Degrees Celsius
- Relative Humidity...0 to 95%

CONSTRUCTION
- Circuit Board...Four Layer Glass Epoxy, Soldermask over Copper
- All IC's in Sockets
- Connectors...Shrouded for Protection
- TESTING...Completely tested and 24 hour burned-in
- WARRANTY...One Year Warranty (Parts and Labor)

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ANSWERS TO QUESTIONS YOUR CUSTOMERS MAY BE ASKING

1. WHY GO INTO THE 8-BIT MARKET, WHEN IBM HAS ESTABLISHED THE 16-BIT MARKET AS THE FUTURE STANDARD FOR MICROCOMPUTERS?

We disagree with the basic promise that everyone will eventually be going to a 16-bit computer. There are currently a large number of users that have a considerable investment in their 8-bit Application Software packages. They also have found that the 8-bit software packages are more than adequate for their business needs. They may consider converting to a 16-bit machine, but the expense of conversion will discourage a number of them. This group of people will decide to stay with an 8-bit machine.

We liken this to the hand held calculator. Sure, the Scientific Calculator is now affordable by most people; but surprisingly enough, you'll find a basic 4 function calculator in most businessmen's office. The price of that 4 function calculator makes it very difficult to justify the Scientific Calculator, and it is usually much easier to use. Thus we believe that, just like the 4 function calculator, there will always be an 8-bit market.

Granted, quite a few people will eventually convert to 16-bit. By offering a TurboDOS based system, you can offer a system that will accept both 8-bit and 16-bit computers on the same network. Thus you can position yourself in both (or is it 3?) markets: the 8-bit and the 16-bit market. The end user may eventually want to convert only a portion of his system to 16-bit.

2. WHY SHOULD I USE ICM BOARDS?

Our current 8-bit boards contain technical features that are state-of-the-art, features hard to find, even on 16-bit computers. Features such as:

1. 4 channels of DIRECT MEMORY ACCESS (DMA), whereas many 16-bit computers offer only 1 DMA channel. DMA has increased memory transfers by 300%, and we offer 4 DMA channels, not 1.

2. MEMORY MANAGEMENT UNIT (MMU) which increases the address bus to 24 bits, and allows addressing up to 16MBytes of memory, 24 bits of address, not the 20 bits that most 16-bit CPU's offer. 16MB of main memory addressing, not 1MB.

3. VECTORED PRIORITY INTERRUPT (VPI) allows the CPU to recognize, prioritize, and respond to simultaneous requests for service from up to 18 interrupt sources. VPI eliminates the problems usually associated with "Polled I/O": Failure to recognize (much less respond to) simultaneous requests for service, and the resultant data loss.

4. TURBODISK (RAM disk) allows using RAM memory to emulate a disk at data transfer rates of 1 MByte/sec – the fastest method of storing and retrieving data.

5. MEMORY MAPPED SLAVES eliminate expensive on-board hardware such as EPROM and FIFO buffers. Data transfers to the slaves are 200% faster than standard I/O mapped slaves. Memory mapping also eliminates much of the code usually required to access a slave, thus leaving more memory for TPA.

OUR FUTURE PRODUCTS WILL CONTAIN THESE FEATURES AND ADDITIONAL "LEADING EDGE TECHNOLOGY" AS WELL.

In addition, we offer all of the Single Board Computer features that you would expect from the technological leader in the field. By the way, Microsystems magazine's review of S-100 single board computers concluded that our CPZ-48000 is "the most hardward advanced" and a programmer's "Nirvana".

3. WHAT IS ICM DOING TO HELP ME GET POSITIONED IN THE 16-BIT MARKETPLACE?

We considered the entire family 8086 CPU's, including the 186 and 286 CPU's. However, the 186 & 286 are highly allocated, and won't be available in production level quantities for quite some time. In addition, our 16-bit 8086 board will contain all of the features that a 186 can offer, and then some. For instance, MMU is already an onboard feature of our 8-bit board. We also offer 4 channels of DMA. An 8086 SBC will allow you to deliver a 16-bit product in a very timely fashion. You won't be facing 6 week delays in delivery from ICM. We will be releasing an 8086 based, 16-BIT Slave Processor in April, 1984. We are also designing a 16-bit Master Processor for future TurboDOS configurations.

4. EVERYONE'S TALKING THE MULTI-USER MARKET. AGAIN, WHY ICM BOARDS, AND WHAT CAN WE DO WITH THE PC'S ALREADY PURCHASED?

Our CPZ-48000 is a true single board computer. It is an excellent stand alone, single-user computer; but it also has been specifically designed as a master computer for networking applications. Our Master/Slave TurboDOS architecture is a true multi-user system that assigns an independent processor to each user. This multi-user/multi-processor network is inherently faster than a multi-tasking, time shared network, because all users are not sharing a single processor's time. TurboDOS offers a number of features that are hard to match - Features such as Record AND File Locking, shared peripherals AND dedicated peripherals.

TurboDOS connects 16 SLAVES per MASTER on an S-100 bus. Our ARCNET capability now allows building a 4000 user system by networking up to 256 MASTERS. Now you can build a cost effective BUS STRUCTURED NETWORK and add the flexibility of LOCAL AREA NETWORKING.

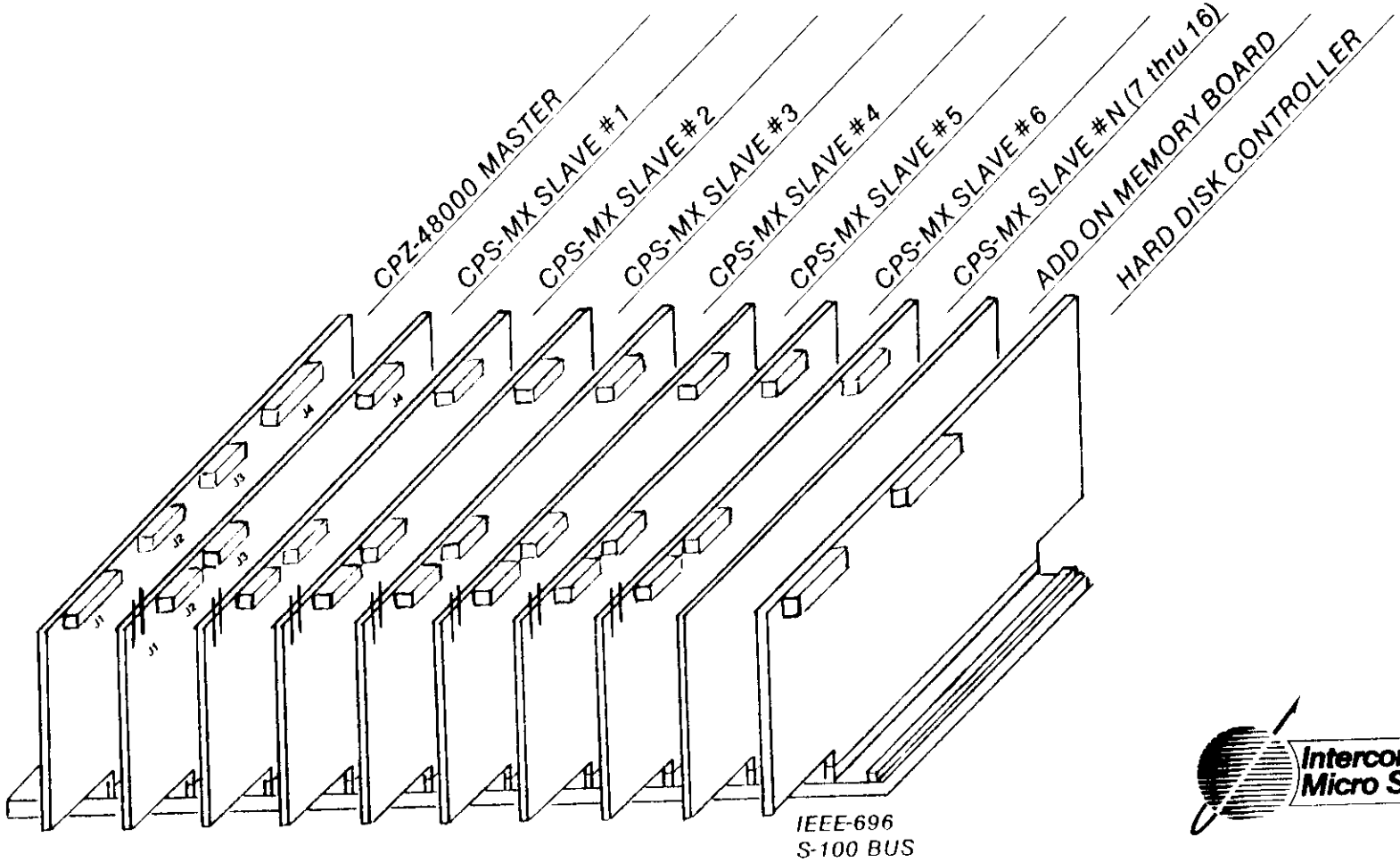
In addition, TurboDOS 1.4 (which went into beta-test in January, 1984) will permit connecting PC's onto the network as slaves via ARCNET. Thus, the businessman who has already bought a PC will be able to build a low-cost, sophisticated, ICM based, TurboDOS multi-user system, and also add his existing PC's to that network.

TurboDOS 1.4 will also allow building a network with 8-bit and 16-bit processors on the same bus. This type of flexibility is hard to beat.

DON'T FORGET! A TurboDOS network is the most cost effective network available today. You can build a multi-user/multi-processor network for approximately 1/3 to 1/2 the cost of a network of PC's. The Master/Slave architecture puts all the processors and peripheral controller boards in one S-100 chassis (mainframe). The user ties into his slave processor via a "dumb" terminal and an RS-232 interface. The master processor, slave processors, and peripheral controllers are networked together on the S-100 bus. With this architecture, a user can be added to a network for less than $1000, including terminal. REMEMBER - LOW COST DOES NOT MEAN LESS SOPHISTICATION, ICM OFFERS THE MOST SOPHISTICATED BOARDS IN THE S-100 MARKET.

5. PC-DOS IS THE STANDARD OF THE FUTURE, CP/M IS DEAD.

Again, we do not accept this premise, CP/M is too prevelant in the market. There are literally thousands of CP/M software packages available. Perhaps the CP/M market will slow down, but it will not go away for quite a few years. Not to be redundant, but why not take advantage of both worlds. TurboDOS will soon be CP/M, CP/M 86 and PC-DOS compatible. You could be hedging your bets by offering a product that will be compatible with all the major software available not only tomorrow, but today as well.



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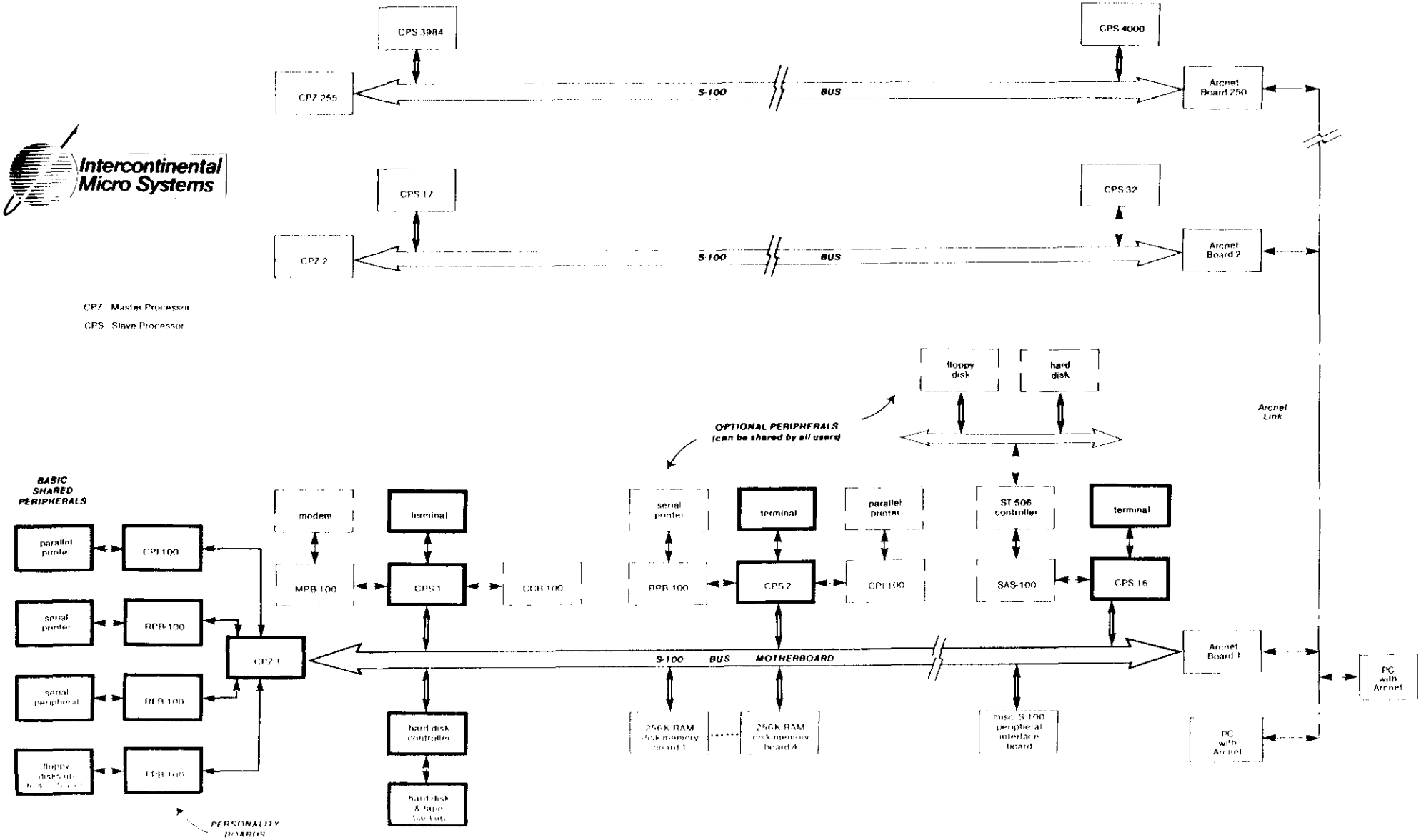
TYPICAL TURBODOS MASTER / SLAVE NETWORK



TURBODOS MASTER / SLAVE NETWORK ARCHITECTURE

PERFORMANCE SPECIFICATIONS

MICROPROCESSOR
- Clock rate.....4MHz or 6Mhz
- Type.....Z80A or Z80B

BUS INTERFACE.....IEEE 696.1/D2(S-100)

SERIAL I/O CHANNELS
- Synchronous Operation
  - Baud Rate.....Up to 800K Baud
  - Data Transfer.....DMA, Interrupt or Programmed I/O
- Asynchronous Operation
  - Baud Rate.....Up to 50K Baud
  - Clock Rate.....1, 16, 32 or 64 Times Baud Rate
  - Bits/Character.....5, 6, 7 or 8
  - Stop Bits..... 1, 1 1/2 or 2
  - Parity.....Odd, Even or None
  - Data Transfer.....DMA, Interrupt or Programmed I/O
  - I/O Interface.....Through Personality Boards

PARALLEL I/O CHANNELS
- Data Rate.....Up to 300K Bytes/Sec
- Channel A Data Transfer.....DMA, Interrupt or Programmed I/O
- Channel B Data Transfer.....Interrupt or Programmed I/O
- Interface Signals.....16 Data Lines Plus 4 Handshaking Lines
- I/O Interface.....Through Personality Boards

FLOPPY DISK CONTROLLER
- Data Rate/8-Inch Double-Density.....500,000 Bits/Sec
- Data Rate/8-Inch Single-Density.....250,000 Bits/Sec
- Data Rate/5 1/4-Inch Double-Density.....250,000 Bits/Sec
- Data Rate/5 1/4-Inch Single-Density.....125,000 Bits/Sec
- Format.....IBM 3740 or 512 sectors
- Data Transfer.....DMA, Interrupt or Programmed I/O
- I/O Interface.....Through Personality Boards

INTERRUPT CONTROL
- Number of Channels.....18
- Priority.....Rotating or Fixed
- Interrupt Modes.....Z80 Mode 0, Mode 1 or Mode 2

REAL-TIME CLOCK
- Operation.....Software Polled or Interrupt Driven
- Range.....37.5 Hz to 1.2288 MHz

64K DYNAMIC RAM MEMORY
- Bank Selection.....May be bank selected in increments of 4K to 64K commencing at 4K boundaries; e.g. 8K of memory may be selected or deselected commencing at location C000(hex) as defined by software.
- Wait States.....None
- Direct Memory Transfers.....To/From SIO, PIO or FDC

DIRECT MEMORY ACCESS CONTROLLER
- Channel 0.....Cascade Mode for IEEE S-100 Bus or Used with Channel 1 in Memory-to-Memory Transfers
- Channel 1.....Channel A of SIO Controller
- Channel 2.....Floppy Disk Controller
- Channel 3.....Channel A of PIO Controller

EPROM
- Type.....2716 2K EPROM, 2732 4K EPROM or 2768 EPROM
- Wait States On Eprom Access.....None in CPZ-48004, 1 in CPZ-48006
- Functions.....Bootup and Monitor

POWER REQUIREMENTS
- Voltages.....+8 VDC @ 2.5 A (max)
+16 VDC @ 0.2 A (max)
-16 VDC @ 0.2 A (max)
- Power.....22 W (max)

OPERATING ENVIRONMENT
- Temperature.....0 to 45 Degrees Celsius
- Relative Humidity.....0 to 95%

CONSTRUCTION
- Circuit Board.....Four Layer Glass Epoxy, Soldermask over Copper. All IC's in Sockets
- Connectors.....Shrouded for Protection

TESTING.....Tested and Burned-In

WARRANTY.....Full One Year Warranty (Parts and Labor)

**** FUNCTIONAL DESCRIPTION ****

The CPZ-4800X is functionally partitioned into the following major groups:

- INPUT/OUTPUT STRUCTURE
  - OFF-BOARD PERIPHERAL CONTROLLERS
    - SERIAL I/O PORT CONTROL
    - PARALLEL I/O PORT CONTROL
    - FLOPPY DISK CONTROL
  - ON-BOARD PERIPHERAL CONTROLLERS
    - DMA CONTROL
    - INTERRUPT CONTROL
    - MEMORY MANAGEMENT UNIT
- 64 KBYTE DYNAMIC RAM/LOGIC
- 2/4/8 KBYTE EPROM
- INPUT/OUTPUT CHIP SELECT LOGIC
- CPU CONTROL SIGNALS GENERATOR
- CLOCK GENERATOR
- POWER-ON CLEAR/RESET LOGIC
- S-100 BUS INTERFACE

Each group is described below to give the user a clear understanding of the hardware and software setup options and to give a full appreciation of the computing power available to the user. A block diagram is included in the following page.

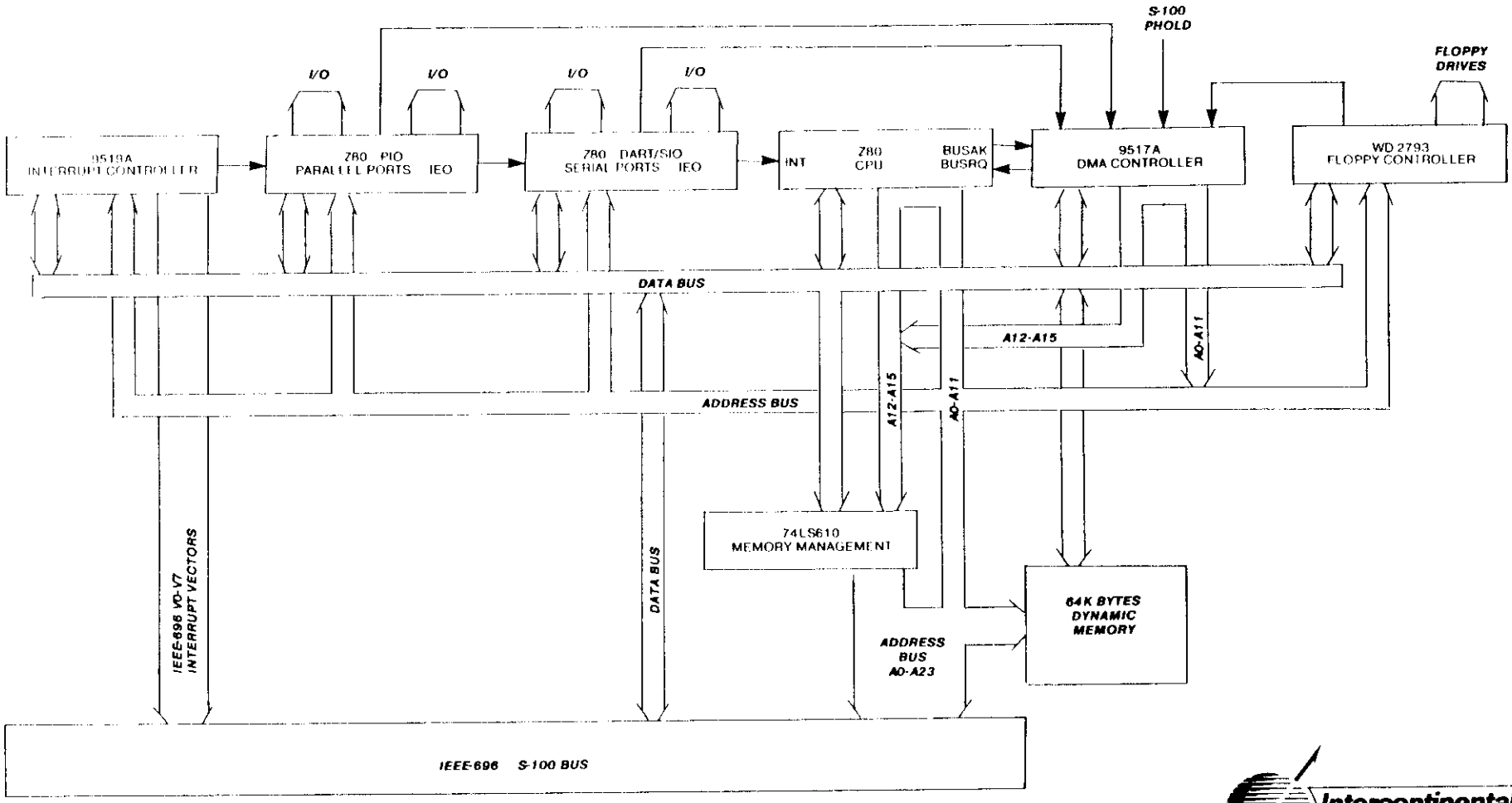
INPUT/OUTPUT STRUCTURE

As a point of reference, an I/O device is defined as a device which, under program control of the Z80 CPU, controls a peripheral device or memory.

The I/O devices contained on the CPZ-4800X consist of:

- Z80A/B DART-0 (Serial Port Controller, DART, SIO Optional)
- Z80A/B PIO (Parallel Port Controller, PIO)
- WD2793 (Floppy Disk Controller, FDC)
- AM 9517A-4/5 (Direct Memory Access Controller, DMA)
- AM 9519A (Universal Interrupt Controller, UIC)
- 8253 (Programmable Timer/Counter, PTC)
- 74LS610 (Memory Management Unit, MMU)

Of these, the first three are used to communicate with off-board peripheral devices and will be referred to as the "OFF-BOARD" peripheral I/O controllers. The remaining are "ON-BOARD" I/O controllers.



CPZ-4800X BLOCK DIAGRAM

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Programmed I/O, Interrupt or Direct Memory Access (DMA) is possible to/from SIO port A, PIO port A and the FDC. No DMA is possible for SIO port B or PIO port B. A DMA port is assigned to the S-100 Bus DMA request line to allow temporary bus masters to capture the bus for DMA transfers to off-board memory. Either fixed or rotating priority selection allows arbitration between internal DMA and external DMA requests from the S-100 Bus. Selection of fixed priority gives the S-100 Bus the highest priority and PIO port A, the lowest. Thus,

DEVICE	PRIORITY
S-100 Bus	1 High
DART/SIO A	2
FDC	3
PIO A	4 Low

The CPZ-4800X uses 128 of it's possible 256 I/O port address for on-board use. The range used is from 80 Hex to FF Hex. Please refer to the SOFTWARE Section of this manual for further explanation.

OFF-BOARD I/O CONTROLLERS

The Off-Board I/O Controllers consist of the Serial I/O Port Control, Parallel I/O Port Control and the Floppy Disk Control.

SERIAL I/O PORT CONTROL

The Serial I/O Port Control consists of the Serial I/O Controller and the Baud Rate Clock Generator.

Serial I/O Controller

The Serial I/O (SIO) Controller is a programmable dual channel device which provides formatting for serial data communications. The channels can handle either asynchronous or synchronous data transfers to/from serial peripheral devices. The SIO operates either under programmed I/O, Interrupt Control or DMA control. DMA is provided for Port A only. All lines necessary to handle asynchronous, synchronous, synchronous bit oriented protocols and other serial protocols are available to the user at the interface connectors. In addition, +/- 16 volt DC and +5 volt DC power are available at these connectors. The SIO may be interfaced to peripheral devices requiring differing protocols. This interface is tailored to the exact device requirements by use of a Personality Module. The interface is implemented through two 16-pin Ansley connectors.

To program the DART or SIO, the system software issues commands to initiate the mode of operation. Seven write registers exist for that purpose. In addition, three read registers allow the programmer to read the status of each channel.

Baud Rate Clock Generator

The Baud Rate Clock Generator consists of a clock generator and an 8253 Programmable Interval Timer. The 8253 is a device which, under software control, can generate variable clock periods which are a multiple of the base input clock. The device has other modes of operation; however, only the mode applicable to the CPZ-4800X operation will be described here. This is Mode 3, the square wave generator mode.

The 8253 consists of three channels, each with a clock input and a gate input. Channel 0 is tied to Serial channel A transmit and receiver clock inputs, channel 1 to Serial Channel B transmit and receiver clock inputs, and channel 2 to the interrupt select jumper area (as a select input to the 9519A Interrupt Controller). Channels 0 and 1 are intended for baud rate clocks, whereas channel 2 is intended for the "real time" clock.

Channels 0 and 1 are connected to the Serial inputs via jumper options PJA and PJB. These signals are also tied to the serial interface connectors. If clock signals are originated by the interfacing devices, the jumpers are cut appropriately. The channel A jumper provides for separate transmit and receive clock inputs from the interface (connector J2) or may serve as baud rate generator outputs to the interface. This arrangement is intended to provide a clock to synchronous MODEM's via "external" clock (pin 24 of the S-100 Bus) in accordance with the EIA RS-232C standards. The modem can then return a transmit/receive clock to the serial controller. In summary, means are provided to implement serial interfaces accommodating asynchronous, synchronous, HDLC and a great number of currently defined communications protocols.

While operating in Mode 3, the 8253 generates a square wave whose period is defined by a count programmed into the respective channel's counter. The square wave will remain at a logical ZERO state for one half the count, and at logical ONE for the remaining half of the count. The counter decrements for each clock period that is received.

The 8253 is programmed by the CPU specifying the mode, loading sequence and counter contents. The Baud rates that can be derived from the 2.4576 Megahertz clock are listed as follows:

Baud Rate	Theoretical Frequency (16 x clock)
50	0.8 kiloHertz
75	1.2 kiloHertz
110	1.76 kiloHertz
134.5	2.152 kiloHertz
150	2.4 kiloHertz
300	4.8 kiloHertz
600	9.6 kiloHertz
1200	19.2 kiloHertz
1800	28.8 kiloHertz
2000	32.0 kiloHertz
2400	38.4 kiloHertz
3600	57.6 kiloHertz
4800	76.8 kiloHertz
7200	115.2 kiloHertz
9600	153.6 kiloHertz
19200	307.2 kiloHertz

PARALLEL I/O PORT CONTROL INTERFACE

The parallel I/O Port Control Interface consists of the Parallel I/O Controller (PIO). The Parallel I/O Controller is a programmable two-port LSI component, which interfaces peripheral devices to the Z80 microprocessor. The PIO provides data transfer to and from peripheral devices under programmed I/O, interrupt control or DMA control. Handshaking data transfer control lines are provided to the interface in addition to the two eight-bit data ports. The CPU reset line and the CPU clock are also connected to this interface. The PIO is flexible and may be connected to peripheral devices requiring differing protocols.

The interface is tailored to the exact device requirements by use of a "Personality Module". The Personality Module is a small external circuit board which connects to the CPZ-4800X to provide the hardware drivers and receivers, logic and other circuitry as required. Refer to Personality Board Users Guide Section for a description of the parallel Personality Modules currently available.

An interrupt line is brought into the interface to give the user the capability of servicing interrupts. The interface is implemented through a 26-pin Ansley connector.

To program the PIO, the system software issues commands to initialize the mode of operation. Initialization is provided by loading the interrupt vector, mode, I/O and interrupt control registers.

Double- or Single-Density Floppy Disk Controller (FDC)

The CPZ-48004 and the CPZ-48006 uses the Western Digital WD2793 Floppy Disk Controller plus descrete support circuitry as the basis for the controller. A reliable phase-lock-loop circuit is implemented giving the user error free disk operation. Up to four 8-inch, four 5 1/4-inch or any combination of four 8 or 5 1/4-inch Floppy Disk drives may be connected. A mix of single- or double-sided drives and of single- or double-density drives may be interconnected. Any combination of single/double sided and single/double density drives may be connected.

The FDC is connected to the drives via Personality boards FPB100-XY or FPB158-XY and adaptor boards FPB100-XY or FPB158-XY The FPB158-30 accomodates both 5 1/4 and 8-inch drives by providing means to connect a 34 pin edge card connector for 5 1/4-inch drives and a 50 pin box connector for 8-inch drives. The FPB100-11 adapts 8-inch drives only and the FPB100-22 adapts 5 1/4-inch drives only. This technique greatly reduces the overall cost of interfacing to floppy drives. With a low cost personality board and even lower cost adaptor, the user may connect the drive configuration fitting their particular needs.

See the "PERSONALITY BOARD USERS GUIDE" section for clarification on the use of the Floppy Personality boards discussed above.

ON-BOARD I/O CONTROLLERS

The On-Board I/O controllers consist of the DMA Controller, Interrupt Control Logic and the Memory Management Unit.

DMA Controller

The DMA Controller consists of the 9517A Multimode DMA Controller, which is a LSI component designed to allow external peripheral devices to transfer data directly to and from the on-board system memory. The use of this data transfer technique greatly enhances the system data throughput because the Z80 microprocessor does not have to deal directly with the transfers, and is free to perform other computing functions.

Combining DMA with the Memory Management Unit (MMU), a block of memory may be transferred from the on-board system memory to off-board system memory and vice-versa at DMA speeds. Additionally, FDC, SIO or PIO data may be transfered directly to off-board memory and vice-versa at DMA speeds. The MMU is loaded with appropriate address translation information. When the DMA transfers data to addresses translated by the MMU, the data is directed to the off-board memory. Memory-to-memory transfers within the on-board memory may also be made. While the Z80 executes block move transfers (LDIR etc...) at 21 clock cycles per byte, the memory-to-memory function of the DMA controller will move a byte in 7 clock cycles, or 3 times faster.

The S-100 Bus channel (channel 0) is normally operated in "CASCADE" mode. Under cascade mode, the DMA Controller simply isolates the CPZ-4800X from the S-100 Bus while the off-board DMA transfer occurs. The power of this technique is that any number of DMA type devices may reside on the S-100 Bus limited only by system data throughput considerations.

During power-up or reset, the DMA Controller is cleared to a state in which DMA requests registers are masked. The cascade mode and other registers must be programmed before channel 0 is active. This should be done as part of an initialize sequence.

Interrupt Control Logic

The interrupt control logic gives the CPZ-4800X user the power to respond to the maskable interrupt (INT*) in any of three modes. These are referred to as modes 0, 1 and 2. Mode 0 is identical to the 8080 interrupt response mode, whereby the interrupt controller instead of memory can place a restart instruction on the data bus and the CPU will execute it. Mode 1 response is identical to that of a non maskable interrupt, except that a restart to location 0038H is executed instead of to 0066H. Mode 2 response allows the user an indirect call to any memory location within a 64 kilobyte memory address space by forming a 16-bit pointer to a table of interrupt service pointers. The 16-bit address is formed by combining the upper 8-bits of register I of the CPU chip with the lower 8-bits of the interrupting device address to form a pointer to a table of 16-bit address pointers to the interrupt service routine.

Interrupt Controller/Select

The CPZ-4800X interrupt controller consists of the 9519A Universal Interrupt Controller. This is a LSI device which provides up to eight maskable interrupt request inputs. Upon receipt of an unmasked interrupt request, a byte of previously stored information is output to the data bus. This enables the CPU to process interrupt service routines by executing restarts or indirect jumps to those service routines. Expansion to the interrupt structure is provided by a priority technique in which enable in/enable out signals are connected in series ("daisy-chained").

DMA Operations

The 9517A is a programmable device, which enables the programmer to free the CPU from the repetitive task of controlling data block transfers by providing "external" hardware control over such operations. For example, the programmer may specify that a data block of "X" number of bytes contained in system memory starting at location "Y" is to be transferred. The programmer may further specify that at the end of said transfer an interrupt is to be generated (perhaps to initiate a subsequent transfer, or to determine the peripheral device status prior to initiating a subsequent transfer). Alternately, the programmer may wish to automatically re-initialize the data block transfer. Once the software command is transmitted to the 9517A, it performs all of the indicated actions without further supervision from the Z80 microprocessor. In all cases, the user of the CPZ-4800X has full control over these parameters and events by having the capability to access any of 27 data and control registers. Once the DMA transfer has begun (also enabled under software control), the CPU may then be used for other processing or for controlling other peripheral data transfers in a similar manner.

The DMA Controller may be operated in either burst or cycle-stealing mode. Cycle-stealing is recommended if concurrent CPU processing is desired while I/O processing is taking place. Burst mode is recommended for operating with fast peripheral devices which could lose data if not responded to in a timely fashion. The transfer rate is 1 megabyte/sec. with DMA operating in burst mode.

DMA Channel Assignments

The CPZ-4800X utilizes all four channels of the 9517A. Channel 0 is dedicated to the S-100 Bus pHOLD line, channel 1 to the SIO serial data channel A, channel 2 to the FDC Data Request Line, and channel 3 to channel A of the PIO parallel I/O port. The DMA channels may be programmed for either fixed or rotating service priority. Selection of fixed priority gives the S-100 Bus the highest priority and parallel port A the lowest. The peripheral device which has higher throughput and which may require closer supervision could connect via the S-100 Bus, or reside in the peripheral device enclosure and communicate via data ports. Should that peripheral be connected directly to the S-100 Bus, fixed priority servicing is recommended. A memory-to-memory block transfer feature is provided which enables the user to transfer blocks of data from a source area of memory to a destination area of memory with an overall throughput increase of 3 times that available using Z80 block moves. Further, programming overhead is reduced in that the CPU need only initiate the DMA device and enable the DMA transfer. The CPU may then execute other code if so desired.

The higher priority interrupting device's enable input is set to logical ONE by permanently connecting it to a pull-up resistor. The SIO/DART enable input line is pulled up to a logical ONE, its enable output line is tied to the enable input line of the PIO and the PIO enable output line is tied to the enable input line of the 9519A. The enable output line of the 9519A is tied to an S-100 Bus. The eight interrupting channels are serviced on a fixed or rotating basis. Within the SIO, priority is fixed, Channel A is assigned a higher priority than Channel B. The receiver, transmitter, and external status are assigned priority in that order within each channel. Similarly, interrupt priority for thePIO is fixed, with Port A having higher priority than Port B.

In summary, the CPZ-4800X interrupt priority daisy chain is as follows:

Priority	Device
1	DART/SIO channel A receiver
2	DART/SIO channel A transmitter
3	DART/SIO channel A external status
4	DART/SIO channel B receiver
5	DART/SIO channel B transmitter
6	DART/SIO channel B external status
7	PIO port A
8	PIO port B
9-16	9519A inputs (fixed or rotating)
17-nn	S-100 Bus interrupt device(s)

NOTE: Any I/O device in the S-100 Bus which uses the INT* line must use this priority chain scheme and must supply its vector. The I/O device must connect to IPROCESS* (response in progress line, pin 65 of the S-100 Bus) and to the PCHAIN (Priority enable output Line, pin 21 of the S-100 Bus). The IPROCESS* connection must be made with an open-collector driver. If the I/O device does not meet these conditions, then it must use the vectored interrupt facility of the S-100 Bus (lines V10*-V17*).

An additional feature of the CPZ-4800X is that data transfers from the peripheral devices may be handled in a polled mode. This requires that the 9519A device be programmed for polled mode and the status register interrogated for the occurrence of the interrupt source signal. In polled mode no interrupts are generated, but the status signal indicating the occurrence of an event remains active. Having detected that occurrence, the remaining status is then interrogated to determine which of the eighteen events occurred.

Jumper options allow the user to choose among twelve S-100 Bus interrupt signals (VIO* to V17*, INT*, PWRFAIL*, NMI* and ERROR*), as well as six internally generated interrupt signals corresponding to the completion of each of the three DMA transfers, FDC interrupt, the parallel port interrupt, and the real time clock. The user selects eight of these signals to be inputs to the Interrupt Controller. The real time clock allows interrupts to be generated at a programmable rate, or they may be software polled.

Signal	Source
VIO*-V17*	S-100 Bus
FINT*	FDC Interrupt
EDMA1*	DART/SIO channel A DMA end of transfer
EDMA2*	FDC DMA end of transfer
EDMA3*	PIO port A DMA end of transfer
SERR*	S-100 BUS ERROR
RTCLK	Real time clock
PINT*	Parallel port interrupt

The S-100 Bus signal INT* is connected to the CPU's INT* bus via an open-collector gate to OR-tie onto the bus to which the on-board interrupt devices are connected (DART/SIO, PIO and 9519A).

The CPU's non-maskable interrupt line (NMI*) may be selected to respond to signals on the S-100 Bus NMI* or PWRFAIL* line. All of these options are implemented by use of jumper plugs.

MEMORY MANAGEMENT UNIT

The Memory Management Unit consists of the 74LS610 MEMORY MAPPING DEVICE plus associated logic. The 74LS610 is a paged memory mapping device which expands the Z80 16-bit address to 24 bits, increasing the addressing capability of the Z80 from 64K bytes to 16 Megabytes. Two modes of operation are possible. These are the "PASS" and "MAP" modes. The 4 MSBits of the Z80 are input to the 74LS610. These bits address one of sixteen 12-bit registers, the outputs of which are output on the address bus. In pass mode, the Z80's 4 MSBits merely pass through the 74LS610 to the corresponding 74LS610 address outputs. The remaining 8 bits of extended address lines are forced to logic zero. In map mode, the contents of the addressed mapping register are output on the address bus. This technique proves to be quite powerful since the extended address lines appear on the bus dynamically. The 12 bits of extended address constitute a "PAGE" address. The remaining 12 lower order address lines address the locations within each page. A "PAGE" consists of 4 Kbytes. There are two hundred and fifty-six 4K pages to give a total of 16 megabytes of storage.

The Memory Management Unit allows the user to map any logical 4K block of memory to any physical 4K block within the 16 megabyte range. Thus, several programs or "TASKS" can share one main program by changing logical 4K block addresses.

The Memory Management Unit lends itself to the generation of address lines in compliance with the IEEE S-100 Bus specification. The signal PSTVAL* is input to the 74LS610 to control the transparent latch function. Thus, the address lines as sampled on the falling edge of PSTVAL* are latched for the duration of a memory cycle as required by the specification. The latching operation functions in both the pass and map mode.

64 Kbyte Dynamic RAM/Logic

The 64 Kbyte Dynamic RAM and associated logic consist of eight 64K-by-one-bit Dynamic RAM's, an address multiplexer, RAS/CAS/REFRESH generator, RAM enable logic and the Window Deselect circuitry.

External logic provides effective refresh techniques suitable for Z80 and S-100 Bus operations. Two octal drivers are utilized to multiplex the 16-bit address lines to the RAM's. A RAS/CAS/REFRESH circuit generates the required timing for the proper reading, writing and refresh operations of the RAM. The RAM enable logic disables the on-board 64 Kbyte RAM when off-board RAM is addressed. The S-100 Bus signal PHANTOM is also sensed to disable the on-board RAM when this signal is active. A Window Deselect Circuitry is provided to perform two functions. The first function is to deselect a portion of RAM during cold-start boot-up to allow a 2 or 4 Kbyte monitor/boot-up PROM to exist in the 64 Kbyte address space without bus conflicts with the RAM. The cold-start boot-up process consists of:

- Deselecting the 1st 4 kbyte locations of the RAM address space.
- Deselecting all of RAM through commands from the EPROM.
- Relocating the EPROM address to the upper 8K locations of the address space through commands from the EPROM.
- Re-enabling all of RAM except the area in which the EPROM exists (E000-FFFF).
- Performing the Operating System load process.
- At completion of the Operating System load process, deselecting the EPROM through commands loaded in the RAM & enabling all of RAM.

The second function is to deselect a "Window" of RAM as specified under software commands. This "Window" is defined as a section of memory which is enabled or disabled under software control. The window boundaries are specified by the contents of two four-bit registers. One register holds the lower boundary and the other holds the upper boundary. The values of the register can take on any value from 0(hex) to F(hex). In this manner, any window commencing and ending at any 4 Kbyte boundary may be specified. This feature enables the user to configure multi-user bank select architectures using bank selectable memory boards installed in the S-100 Bus. The feature also enables the user to configure systems where an external memory, such as a memory mapped video board, is required to co-exist in the 64 Kbyte address space with the on-board RAM.

2K/4K/8K EPROM

The CPZ-4800X may accommodate either a 2K (2716), 4K (2732) or 8K (2764) EPROM. A jumper (jumper JC) is made available to select either of the three EPROM types. The EPROM functions as both a boot-up and a monitor PROM. As a boot-up PROM, the EPROM contains the software routines necessary to manipulate the Window Deselect Circuitry and to load the required Disk Operating System contained on Floppy Disk Drive diskettes. The EPROM also contains monitor routines which are discussed in the SOFTWARE/PROM MONITOR sections.

I/O Chip Select Logic

The I/O Chip Select logic generates the "chip select" signals for the DART/SIO, PIO, programmable counter, universal interrupt controller, FDC, Memory Management Unit (MMU), Boot/Monitor Enable, Memory Deselect Logic, FDC Configuration register and the DMA Controller. In addition, the required control and data signals are generated for the DART/SIO, FDC and PIO. Because the DART/SIO, FDC and PIO may be operated under DMA control (as well as programmed I/O), the chip select, control and data signals are generated to handle each case within this logic.

POWER-ON CLEAR/RESET LOGIC

This logic provides reset signals to the CPU as well as to the S-100 Bus interface. The logic is activated under two conditions, when power is first applied to the board, and when the S-100 Bus signal RESET* is activated.

Signals asserted upon applying power are:

a. S-100 Bus signals POC*, RESET*, and SLAVE CLR*
b. Internal CPZ-4800X reset

Signals assered when RESET* is asserted are:

a. S-100 Bus signal SLAVE CLR*
b. Internal CPZ-4800X reset

CLOCK GENERATOR

The clock generator divides an 8 or 12 Megahertz crystal-generated clock signal to provide the internal CPU clock (OCLK), the S-100 Bus clocks (O and CLOCK) and internal clocks BUSCLK and SCLK. These clock signals are utilized to implement S-100 Bus signals in conformance with the IEEE standard for the S-100 Bus on a well-defined, clocked-logic basis.

CPU Control Signals Generator

The CPZ-4800X architecture is enhanced by use of state-of-the-art LSI components. The board utilizes a mix of Z80 support components (DART/SIO and PIO) and 8080 support devices (8253, 9519A and 9517A). A variety of logical conflicts arise due to the differing requirements of these components and those of the S-100 control bus. Further, the control signals generated by the DMA Controller differ from Z80-type control signals. It is the function of the CONTROL SIGNALS GENERATOR to generate all of the appropriate control signals required by each of these components and the S-100 BUS CONTROL SIGNALS GENERATOR (described below).

S-100 BUS CONTROL SIGNALS GENERATOR

The S-100 Bus Control Signals Generator consists of the logic necessary to generate key S-100 Bus signals such as pSYNC, pSTVAL*, pWR*, and pDBIN.

pSTVAL* is of particular importance, as this signal is used to to perform a transparent latch function for other signals, the result of which is to generate S-100 Bus signals in conformance with the IEEE timing standards. Address and data lines are latched with this signal whereby status is latched or unlatched as selected by a jumper. While in the latched mode, the CPZ-4800X is set for full IEEE timing conformance. The transparent mode enables systems to operate in conformance with Z80 timing.

Jumper option JB is provided to configure pDBIN to any given system which may not tolerate the stringent IEEE timing requirements for this signal. Read access time can be adjusted by selecting one of the two positions on the header.

S-100 Bus Interface

The S-100 Bus consists of 100 electrical signal lines. These are grouped into sets of lines used to transmit data and control among interconnected devices.

The groups are:

Group	No. of Lines
Address Bus	24
Input Data Bus	8
Output Data Bus	8
Status Bus	8
Control Input Bus	5
Control Output Bus	6
DMA Control Bus	8
Vectored Interrupt Bus	8
Utility Bus	8
System Power	9
Manufacturer specified lines	3
Reserved lines	5

Devices connected on the bus are classified as either bus masters or bus slaves and as either permanent or temporary masters. The CPZ-4800X is a permanent bus master. Any other master connected to the S-100 bus may take control of the bus by making the appropriate DMA request provided no internal DMA by the DART/SIO, FDC, or PIO is in progress. If the DMA controller is programmed for fixed priority operation then the S-100 Bus DMA request will be honored first if simultaneous DMA requests occur.

Each of the S-100 Bus signals utilized by the CPZ-4800X are described on the following pages.

Address Bus

The address bus consists of 24 lines used to select a memory location or an input/output device during a bus cycle. All 24 lines are active during a memory read, write or opcode fetch (M1) cycle unless the Memory Management Unit has been programmed for pass mode in which case the uppermost 8 bits (A16-A23) are forced to logic zero. The least significant byte of the address lines is active for input or output cycles. Address bus lines are enabled while ADSB* is inactive (no S-100 Bus DMA cycle in progress). The address bus lines are denoted as A0 through A23, with line A0 representing the least significant bit. Lines A0 through A7 compromise the least significant byte and lines A8 through A15 make up the "high" address byte with bits A16 through A23 constituting the extended address byte. Two octal-drivers and the Memory Management Unit are used to condition the lines in conformance with the characteristics required by the IEEE S-100 Bus standard.

Input Data Bus

There are eight input data lines which are enabled onto the CPU data bus when the enabling signal DIEN* is active. This signal is active under the following conditions:

1. AN EXTERNAL I/O CYCLE IS INITIATED.
2. AN EXTERNAL MEMORY CYCLE IS INITIATED.
3. AN EXTERNAL DEVICE INTERRUPTS THE CPU AND PLACES A VECTOR ON THE DATA BUS.

Output Data Bus

There are eight data output lines which are enabled by the signal DODSB*. A line driver conditions these lines to conform with the IEEE S-100 Bus standard.

Output Data Bus lines are designated D00 through D07, with line D00 representing the least significant bit.

Status Bus

The status bus consists of eight output lines which define the current CPU bus cycle type. Seven of the eight lines defined in the S-100 Bus specification are utilized by the CPZ-4800X. These lines are enabled while the enabling signal SDSB* is inactive. Status signals may be selected for full IEEE timing performance (latched mode) or for Z80 timing (transparent). This selection is made through jumper option JD. An octal latch/line driver is used to condition all lines of the Status Bus in conformance with the IEEE S-100 Bus standard. The seven lines of the Status Bus are:

Status	Function
sMEMR	Memory Read
sM1	Opcode Fetch
sINP	Input
sOUT	Output
sWO*	Write cycle
sINTA	Interrupt acknowledge
sHLTA	Halt acknowledge

The status signal SXTRQ* (16-bit data transfer request) is not used in the CPZ-4800X and is left open. The remaining Status Bus lines are described in the following paragraphs.

sMEMR (Memory Read)

sMEMR is a status signal indicating that a memory read cycle is in progress. This signal is valid during a normal memory read cycle (memory read or opcode fetch cycle).

sM1 (Opcode Fetch)

sM1 is a status signal indicating that a memory read/opcode fetch cycle is in progress.

sINP (Input)

sINP is a status signal indicating that a peripheral device read cycle is in progress.

sOUT (Output)

sOUT is a status signal indicating that a peripheral device write cycle is in progress.

sWO* (Write Cycle)

sWO* is a status signal indicating that a write cycle is in progress, wherein data is transferred from an S-100 Bus master to a slave.

sINTA (Interrupt Acknowledge)

sINTA is a status signal indicating that an interrupt acknowledge cycle is in progress.

sHLTA (Halt Acknowledge)

sHLTA is a status signal indicating that the CPU is in a halt state.

Control Input Bus

The Control Input Bus consists of six signals, five of which are used in the CPZ-4800X. These lines allow S-100 Bus slaves to synchronize the CPZ-4800X with conditions internal to the bus slave, to request the relinquishment of the S-100 Bus (DMA request) and to disable the CPU from the S-100 Bus. The signals are conditioned by pull-up resistors and Schmitt-trigger input receivers.

The five lines of the Control Input Bus are:

Line	Function
RDY	Slave ready
XRDY	Special ready
INT*	Maskable interrupt request
NMI*	Non-maskable interrupt request
HOLD*	DMA request

These lines are described in the following paragraphs.

RDY (Slave Ready)

This control line is used by S-100 Bus slaves to suspend bus cycles by inserting wait states in a CPU cycle. Slaves may connect to this line by using an open-collector driver.

XRDY (Special Ready)

This control line is used as a special ready line to accommodate devices such as front panels. Only one slave device should connect into the XRDY line. This line also suspends bus cycles by introducing wait states to the CPU.

INT* (Maskable Int. Req.)

This control line is used to request service from the CPU on an interrupt basis. The INT* line is enabled (unmasked) or disabled (masked) under software control. When the INT* line is activated, the CPU responds with an acknowledge signal and subsequently gates the opcode or vector information asserted on the bus by the bus slave initiating the interrupt. Interrupt may be asserted on the INT* line by the DART/SIO, PIO or the 9519A interrupt controller. Logic is provided to sense these conditions and to respond appropriately. INT* should be asserted as a continuous level and held active until a response is received.

NMI* (Non-maskable Int. Req.)

This control line is used to request service from the CPU on an interrupt basis. The NMI* is non-maskable, meaning it is always enabled. When an interrupt occurs on NMI*, a CPU acknowledge cycle is not generated.

Normally, only critical signals are connected to the NMI* line. The CPZ-4800X provides the option to connect the S-100 Bus signal PWRFAIL* to the NMI* line via a jumper option. NMI* is sensed on a signal edge transition.

HOLD* (DMA Request)

This control line is used by S-100 temporary bus masters to request control of the S-100 Bus from the CPZ-4800X. This line may be disabled under software control through the 9517A controller. When enabled, a DMA cycle may be initiated by asserting this line. The 9517A DMA controller will respond with the signal pHLDA when the cycle is initiated, and will relinquish control to the temporary bus master.

Control Output Bus

The control output bus consists of six lines, one of which is optional. These lines are enabled when the enabling signal CDSB* is inactive. A line driver is used to condition these lines to conform with the characteristics required by the IEEE S-100 Bus standard.

The six lines of the Control Output Bus are:

Line	Function
pSYNC	Cycle start
pSTVAL*	Status valid
pDBIN	Read strobe
pWR*	Write strobe
pHLDA	Hold acknowledge
pWAIT	Wait (Optional)

These lines are described in the following paragraphs.

pSYNC (Cycle Start)

pSYNC is a control signal which indicates the start of a new bus cycle. The signal becomes active when an I/O cycle, memory cycle, DMA read or DMA write cycle occurs. The signal remains active for approximately one bus clock in accordance with the IEEE S-100 Bus standard. pSYNC does not become active during a refresh cycle.

pSTVAL* (Status Valid)

pSTVAL* is a control signal which indicates that address, Data and Status signals have stabilized on the bus during the current bus cycle. It becomes active on the first CPU clock cycle after pSYNC becomes active, and goes inactive on the first CPU clock cycle after the bus cycle is complete. By using this signal as the latching signal, the address, data, and status signal timing will conform to the timing specified in the IEEE standard.

pDBIN (Read Strobe)

pDBIN is a control signal which gates data arriving on the CPU data bus from an external source. Header jumper option JB is provided to specify the pulse width and timing for this signal.

Two options are available:

a. FULL IEEE TIMING CONFORMANCE: In this option, pDBIN goes active at a specified time after pSTVAL* goes active. This presents the smallest read access time window available. A single clock cycle duration is typical.

b. Z80 TIMING: In this option, pDBIN goes active when the Z80 read signal goes active, thereby giving the user a maximum read access time window. This is typically one and one-half clock cycles in duration.

pWR* (Write Strobe)

pWR* is a control signal which performs the function of a write strobe to write data from the CPU data bus to an addressed peripheral or memory device. pWR* goes active at the specified time after pSTVAL goes active for I/O write cycles, DMA memory write cycles and CPU memory write cycles.

pHLDA (Hold Acknowledge)

pHLDA is a control signal which is active when the CPZ-4800X relinquishes the address, data, control and status buses in response to a temporary master DMA request. This signal is generated by the 9517A DMA controller, channel 0 DMA acknowledge output.

pWAIT (Wait [optional])

pWAIT is a control signal which is active when any wait condition is active within the CPZ-4800X. Thus, pWAIT goes active when either of the two S-100 Bus wait lines (RDY or XRDY) go active, the FDC programmed I/O wait state generator goes active or when the 9519A interrupt controller "pause" signal goes active (indicating that an interrupt cycle is in progress and the daisy chain priority is being resolved). pWAIT is optional and may be connected or disconnected via a jumper option. pWAIT is not a signal required by the IEEE S-100 Bus standard.

DMA Control Bus

The DMA Control Bus consists of eight input lines. Four of these are activated as required for the permanent bus master. The remaining four lines are utilized to isolate the CPU from the S-100 when the permanent bus master relinquishes control to the temporary bus master. The disable lines are connected to schmitt-trigger input receivers to provide noise immunity. The conditioned signals then disable the respective output line drivers. The DMA arbitration lines are used by the temporary masters to determine which temporary master has the use of the bus during a DMA cycle. The permanent bus master need not arbitrate. The eight DMA Control Bus lines are:

Line	Function
DMA0*	DMA arbitration line
DMA1*	DMA arbitration line
DMA2*	DMA arbitration line
DMA3*	DMA arbitration line
ADSB*	Address disable
DODSB*	Data out disable
SDSB*	Status disable
CDSB*	Control output disable

Vector Interrupt Bus

The Vectored Interrupt Bus consists of eight lines, designated VI0* through V17*. VI0* is treated as the highest priority interrupt line. These lines should be asserted as levels, and should remain asserted until a response is received.

The Vectored Interrupt Bus lines are connected to interrupt option jumpers to connect the appropriate lines to the 9519A interrupt controller. This device then masks or unmasks the interrupts, prioritizes the requests, and asserts the INT* signal to the CPU.

Utility Bus

The Utility Bus consists of eight lines. Output lines are conditioned by drivers to conform with characteristics required by the IEEE S-100 Bus standard. The eight Utility Bus lines are:

Line	Function
0 (clock)	System clock (output)
CLOCK	Clock (output)
MWRITE	Memory write strobe (output)
POC*	Power-on clear (output)
SLAVE CLR*	Slave clear (output)
RESET*	Reset (input/output)

Each of these Utility Bus signals are described in the following paragraphs.

0 (System Clock)

0 is the S-100 Bus system clock. 0 has the same sense as the inverted CPU computer clock (BCLK).

CLOCK (Clock)

CLOCK is a 2 Megahertz Utility clock signal to be used by slave devices.

MWRITE (Memory write)

This line is optional on the CPZ-4800X. It may be connected to the bus via jumper option JE, or this signal may be generated externally to the CPZ-4800X, in which case the jumper would be omitted.

Logic is provided so that MWRITE is generated by either CPZ-4800X on-board signals (pWR* & sOUT) or by off-board signals if the status and control bus drivers are disabled. This signal is active during DMA and CPU memory write cycles.

*** N O T E ***
Care must be taken that the signal is generated at only one point in the system.

POC* (Power-on Clear)

The POC* line is active when initial power-up occurs on the S-100 Bus. When POC* is active, SLAVE CLR* and RESET* are asserted. POC* is guaranteed to stay active for at least 50 milliseconds.

SLAVE CLR* (Slave Clear)

SLAVE CLR* is the signal line which resets all slave devices on the S-100 bus. During power-on clear, this line is asserted by the CPZ-4800X power-on clear logic. External devices may assert RESET* and, in doing so, assert SLAVE CLR* as well. RESET* is driven by an open-collector driver.

ERROR* (Error)

Error* is a signal generated by a slave device to indicate abnormal conditions such as parity error, CRC error, out of tape, etc. This line is connected to a jumper option where it may be selected as an interrupt source.

PWRFAIL* (Power Failure)

PWRFAIL* is a signal generated external to the CPZ-4800X to indicate that a power failure has occurred. This signal remains active until power is restored and POC* is active. The signal is available to the user via a jumper so that it may be connected to the NMI* line of the CPU.

System Power

The system power lines consist of all lines supplying unregulated power to the CPZ-4800X and other devices connected to the S-100 Bus. The nine System Power lines are:

Lines	Quantity
+8 VOLTS	2
+16 VOLTS	1
-16 VOLTS	1
GND	5

The +8 VOLT lines are connected to a +5 VDC regulator to supply +5 volt of regulated power to the CPZ-4800X. This line should not be greater than +10.0 VDC for best opperation.

The +16 VOLT connects to a +12 VDC regulator and the two serial port connectors. The -16 VDC line connects to the two serial port connectors. The 16 volt lines are utilized on the serial ports for supplying power to RS-232C driver circuitry.

All ground lines are connected to the ground plane to provide a low impedance path from the S-100 Bus ground to the CPZ-4800X ground.

MANUFACTURER SPECIFIED LINES

The IEEE S-100 Bus standard reserves three of the 100 lines for special use by the manufacturer. The CPZ-4800X utilizes these lines. Two of these are required to implement the daisy chained priority interrupt expansion. The third supplies the Z80 refresh signal.

All lines may be connected through solder jumpers. See the section on Solder/Trace Cut Options.

The three Manufacturer specified lines are described in the following paragraphs.

IPROCESS* (Interrupt in Progress)

IPROCESS* is a bi-directional signal which indicates that an interrupt cycle is in process. This line is required to cascade external 9519A Universal Interrupt Controllers. IPROCESS* utilizes pin 65 of the S-100 Bus.

PCHAIN (Interrupt Priority)

PCHAIN is an output signal which indicates the priority level of the interrupt in progress. If it is high, the interrupt response action is passed to the next interrupt device in the serial interrupt structure. PCHAIN utilizes pin 21 of the S-100 Bus.

RFSH* (Refresh)

RFSH* is the Z80 refresh signal buffered for use by external dynamic RAM memory devices connected to the S-100 Bus. RFSH* utilizes pin 66 of the S-100 Bus.

Reserved Lines

Five of the S-100 Bus lines are reserved for future use by the IEEE specification. The CPZ-4800X makes no connection to these lines.

**** OPERATING INSTRUCTIONS ****

Instructions are given herein to configure the CPZ-4800X from both the hardware and software standpoint. The user will be pleased to find that minimal setup procedures are required.

HARDWARE SETUP INSTRUCTIONS

The hardware is configured via jumper options and solder/trace cut areas. The solder/trace cut areas are referred to as PJX, where X is the area designator. These jumpers are by nature rarely reconfigured. PJX options are located on the "solder" side of the board. The jumper options referred to as JX, where X is the jumper designator, gives the user flexibility in setting up the CPZ-4800X for a multitude of applications. Jumper options are located on the "component" side of the board.

Instructions are also included on providing jumper option modifications for various popular floppy drives. These modifications must be executed prior to integrating the CPZ4800X to the floppy drives.

A section is included on instructions for connecting personality boards to the CPZ4800X.

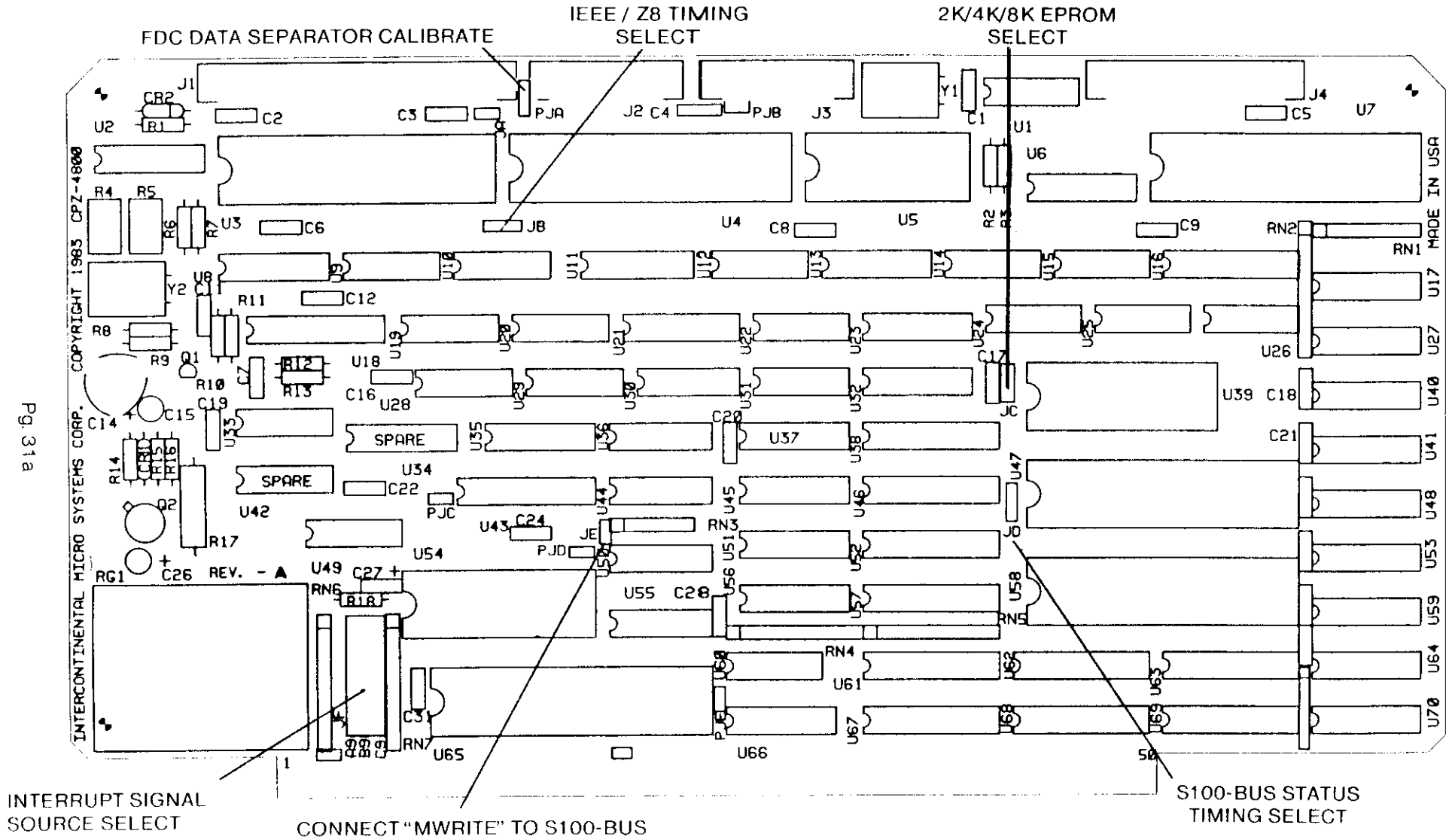

FIGURE 1 - JX JUMPER OPTIONS

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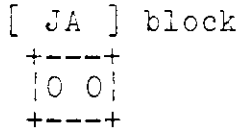
JUMPER OPTIONS

Refer to figure 1 to locate the JX header positions. The JX jumper blocks are listed as follows:

JA - FDC DATA SEPARATOR CALIBRATE
JB - IEEE/Z80 TIMING SELECT
JC - 2K/4K/8K EPROM SELECT
JD - S-100 BUS STATUS (IEEE OR TRANSPARENT SELECT)
JE - CONNECT "MWRITE" TO S-100 BUS
JF - INTERRUPT SIGNAL SOURCE SELECT

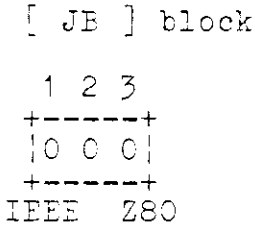
JA

This jumper option is for factory use only. The jumper is connected to enable the calibration of the FDC data separator circuitry through adjustments on potentiometers R4 & R5 and variable capacitor C14. These adjustments must not be modified in the field.



JB

The CPZ-4800X may be configured to output S-100 Bus signals PDBIN and PWR* in compliance with the IEEE specifications for the S-100 Bus timing, or it may be configured to output these bus signals in Z80 mode. The selection is made via jumper JB. To select IEEE timing, jumper position 1-2 of JB. To select Z80 timing, jumper position 2-3 of JB.

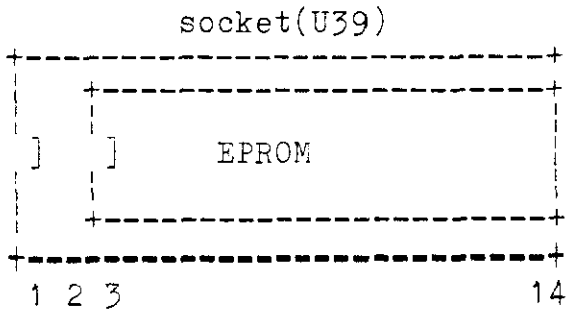


JC

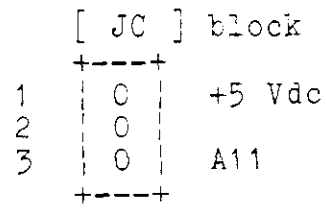
Either a 2716, 2732 or 2764 EPROM may be used with the CPZ-4800X. Instructions are given to incorporate any of these three EPROMS.

2716/2732

A 28 pin socket is provided on the CPZ-4800x in order to accommodate any of the three EPROM sizes. In the case of the 2716 and 2732, pin1 ofthe EPROM must connect to pin threeof the socket. This is illustrated below:



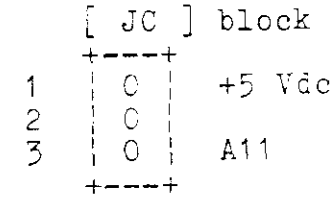
On jumper JC, for the 2716 connect 1-2 and for the 2732 connect 2-3.



2764

Install the EPROM in the normal fashion; i.e., pin 1 mates with pin 1.

On jumper JC connect 2-3.

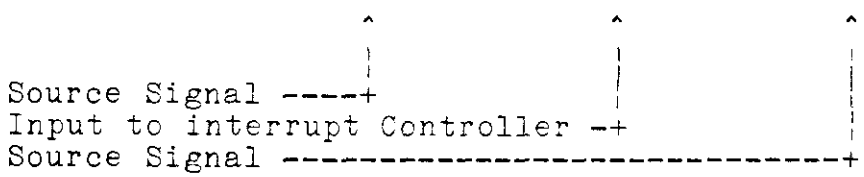


JF

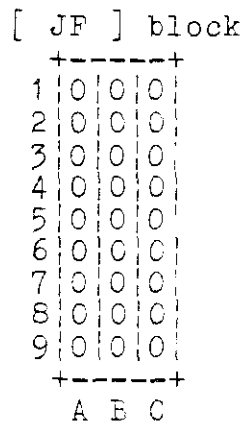
JF may be configured to select various signals as inputs to the interrupt controller. Jumpers are provided to select one of two signals available for each of 9 inputs. Wire-wrap or other means of interconnection may be used to select a signal in a different order from that assigned to the jumper block. This is clarified below:

Connection Table

Pin	A	B	C
1	NMI*	INMI*	PWRFAIL*
2	(SPARE)	IREQ7*	V7*
3	SERR*	IREQ6*	V6*
4	PINT*	IREQ5*	V5*
5	EDMA3*	IREQ4*	V4*
6	EDMA2*	IREQ3*	V3*
7	EDMA1*	IREQ2*	V2*
8	FINT*	IREQ1*	V1*
9	RTCLK	IREQ0*	V0*

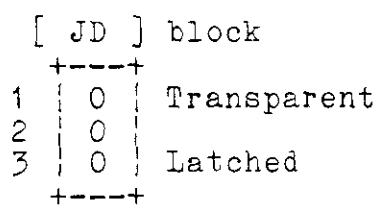


** N O T E ** (B-1 is input to NMI* of CPU)



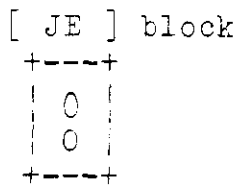
JD

The S-100 Bus status signals may be output from the CPZ-4800X in latched mode which makes timing conform to the IEEE specification or may be output in transparent mode which makes the timing correspond to that of the Z80. To select Z80 timing, jumper position 1-2 of JD. To select IEEE timing, jumper position 2-3 of JD.



JE

The signal "MWRITE" may be generated on the CPZ-4800X or it may be generated from signals external to the CPZ-4800X like a front panel. In any case, the signal should be sourced by one device only. If the CPZ-4800X is to be the source of the signal, install the jumper provided on jumper block JE, otherwise, leave the jumper off.



EXAMPLES:

1) To connect S-100 Bus Vector line V5* to the interrupt controller, install a jumper from position C4 to B4.
2) To connect Floppy interrupt signal *FINT** to the interrupt controller, install a jumper from A8 to B8.
3) To connect the parallel port interrupt line to the highest priority interrupt input (IREQ0), install wire-wrap or any other adequate interconnection means from A4 to B9.

**** N O T E ****

a.) Highest priority input is IREQ 0 and the lowest is IREQ 7.
b.) *NMI and PWRFAIL are sources to the CPU non-maskable* interrupt input.
c.) Signal source definition are as follows:

Vx = S-100 Bus vectored interrupt (X = 0 --> 7)
PWRFAIL = S-100 Bus power fail
RTCLK = Real Time Clock
FINT = Floppy interrupt
EDMAX = Channel X end of DMA process (X = 1 --> 3)
PINT = Parallel port interrupt
SERR = S-100 Bus error
NMI = S-100 Bus non-maskable interrupt

SOLDER/TRACE CUT OPTIONS

Refer to figure 2 to locate the PJX solder/trace options. The PJX options are listed as follows:

PJA - DART/SIO PORT A CLOCK SOURCE SELECT
PJB - DART/SIO PORT B CLOCK SOURCE SELECT
PJC - CONNECT Z80 REFRESH TO S-100 BUS
PJD - CONNECT INTERRUPT-IN-PROCESS TO S-100 BUS
PJE - CONNECT pWAIT TO S-100 BUS
PJF - CONNECT S-100 BUS GROUND TO PCB GROUND PLANE(PIN 53)
PJG - CONNECT S-100 BUS GROUND TO PCB GROUND PLANE(PINS 20/70)
PJH - CONNECT INTERRUPT PRIORITY CHAIN TO S-100 BUS

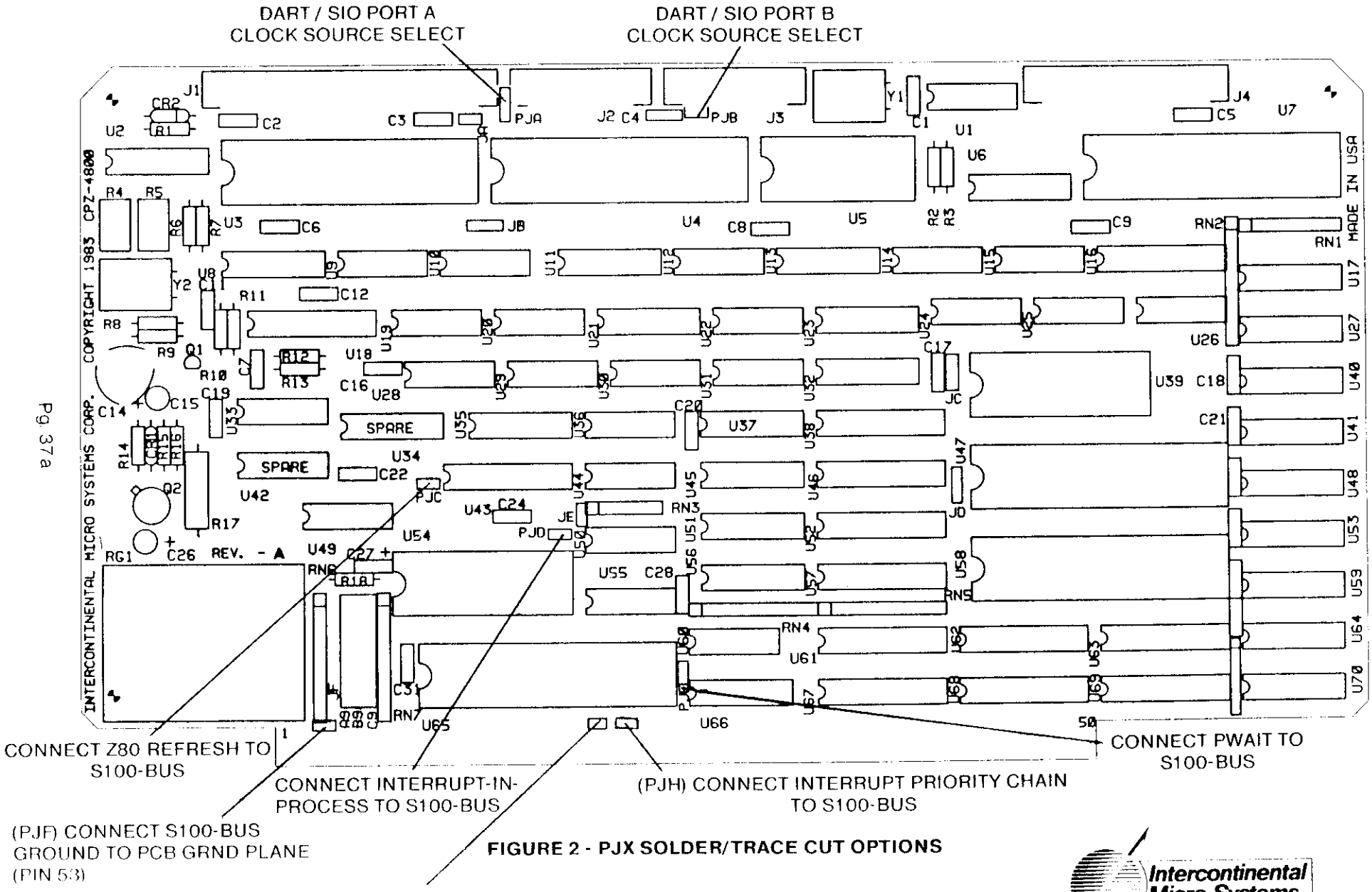


FIGURE 2 - PJX SOLDER/TRACE CUT OPTIONS

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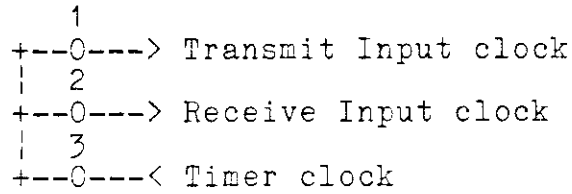
PJA

The CPZ-4800X comes configured so that the DART/SIO ports receive their baud rate clocks from an on-board programmable timer. The board could be reconfigured to source the clocks from the DART/SIO serial port connectors. Such is the case when synchronous modems connect to the serial ports. The modem provides a clock to the DART/SIO. Furthermore, the modem may receive the clock from the on-board timer, condition the clock and return it to the input of the DART/SIO. The transmit and receive clocks may be sourced separately on Port A. All combinations are possible through this jumper.

To source DART/SIO PORT A inputs from the DART/SIO connector only, cut the trace from PJA-2 to PJB-3. The source can now be connected through the personality board on either PIN P2-2 or P2-3. If the DART/SIO PORT A inputs are to be sourced separately from the SIO connector, cut the trace from PJB-1 to PJB-2. The receive clock is now input on P2-3 and the transmit clock is input on P2-2.

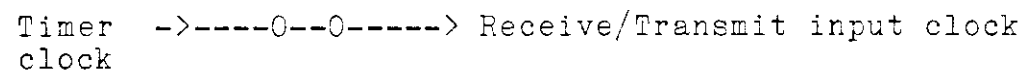
[PJA] area



PJB

To source DART/SIO Port B input from the DART/SIO connector only, cut the trace at PJB. The source can now be connected through the personality board on pin P3-3.

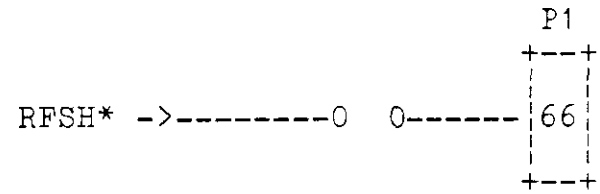
[PJB] area



PJC

If the S-100 Bus dynamic RAM memory boards require the Z80 refresh signal for proper operation, PJC may be connected to provide that signal.

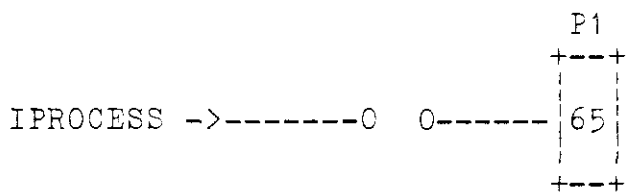
[PJC] area



PJD

The CPZ-4800X may connect to off-board devices with priority interrupt structures which comply with the Advanced Micro Digital Universal Interrupt Controller AM9519A method of resolving interrupt priority level. The method consists of serially chaining interrupt devices via a signal referred to as "PCHAIN" and connecting in parallel the signal "IPROCESS". The CPZ-4800X is factory configured so that both these signals are NOT connected to the S-100 Bus. Solder a jumper in PJD if the interrupt structure is to be extended to other boards outside of the CPZ-4800X.

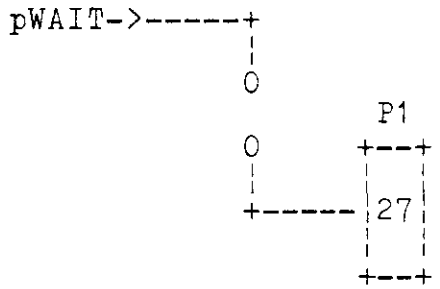
[PJD] area



PJE
---

pWAIT is not a signal specified to be connected to the S-100 bus. however, some bus slaves need to detect wait conditions on the bus simultaneous to the bus master. An option is provided on this bus master to connect pWAIT to pin 27 of the bus if this signal is required. If so, solder a jumper in jumper area PJE.

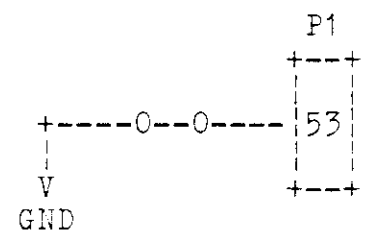
[PJE] area



PJF

Some S-100 Bus boards utilize pin 53 for signals other than ground. The IEEE specification requires that pin 53 be connected to ground. If a board is installed in the bus and pin 53 is to used for other than ground, the corresponding trace at PJF must be cut.

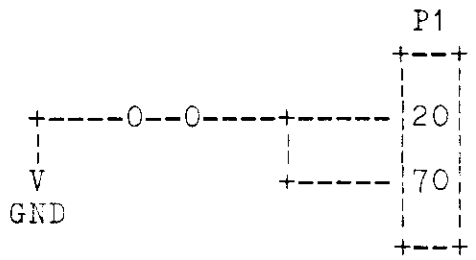
[PJF] area



PJG

Some S-100 Bus boards utilize pin 20 and 70 for signals other than ground. The IEEE specification requires that these be connected to ground. If a board is installed in the bus and these pins are required for signals other than ground, cut the trace in jumper area PJG to break ground connection to pins 20 and 70.

[PJG] area

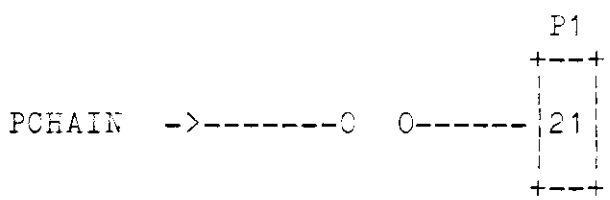


PJH

See PJD.

Solder a jumper in PJH if the interrupt structure is to be extended to other boards outside of the CPZ-4800X.

[PJH] area



FLOPPY DRIVE JUMPER OPTIONS

The CPZ4800X is compatible with all floppy drives which have Shugart standard interfaces. However various drives require particular jumper option settings to make them compatible with the CPZ4800X hardware. Jumper settings are given for the following Floppy drives:

SHUGART MODEL 800/801
SHUGART MODEL 850/851
QUME DATATRACK 8
TANDON TM848-1
TANDON TM848-2E
MITSUBISHI M2896-63
MITSUBISHI M2894-63
SEIMENS FDD100-8D
TANDON TM100-2

ICM technical support personnel shall provide the necessary assistance to customers wishing to integrate other drives compatible with the SHUGART standard interface.

SHUGART MODEL 800/801

(a) Do not modify etched trace options as delivered from the factory.

(b) Remove all jumpers on the disk drive and install the following:

A	Y
B	T1
C	T2
DS	800

(c) Install the following terminators in the last drive connected to the CPZ4800X:

T3	T5
T4	T6

(d) Connect drive select jumpers as follows:

DS1= Drive A
DS2= Drive B
DS3= Drive C
DS4= Drive D

SHUGART MODEL 850/851

(a) Do not modify etched trace options as delivered from the factory.

(b) Open the following shunts:

HL
X
S

(c) Remove all the jumpers on the disk drive and install the following:

A	FS
B	IW
C	RS
D	S2
I	2S
R	850
Z	

(d) Install the terminator pack in the last drive connected to the CPZ4800X.

(e) Connect drive select jumpers as follows:

DS1= Drive A
DS2= Drive B
DS3= Drive C
DS4= Drive D

QUME DATATRACK 8

(a) Close or open the following jumper options as indicated:

close	open
C	D
Y	DC
DS	DL
	HA
	T40
	2S

(b) Close or open the following shunts as indicated:

close	open
A	X
B	Z
I	HL
R	

(c) Leave all other drive options as delivered from the factory.

(d) Connect drive select jumpers as follows:

DS1= Drive A
DS2= Drive B
DS3= Drive C
DS4= Drive D

TANDON TM848-1

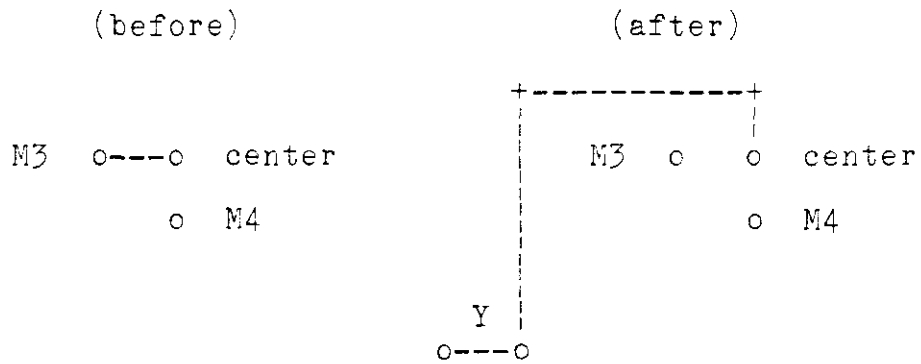
(a) Open the following shunts installed in U3:

1-to-16
2-to-15
5-to-12

(b) Open or close the following drive jumper options as indicated:

close	open
Y	M2
DS	
C	

(c) Remove connection from M3 to "center" and with a wire, connect "center" to Y as illustrated below:



(d) Connect drive select jumpers as follows:

DS1= Drive A
DS2= Drive B
DS3= Drive C
DS4= Drive D

TANDON TM848-2E

(a) Install the following jumpers:

NL
M3
M4
IC
R

(b) Connect drive select jumpers as follows:

DS1= Drive A
DS2= Drive B
DS3= Drive C
DS4= Drive D

(c) Install the terminator pack in the last drive in the chain.

MITSUBISHI M2896-63 (HALF HEIGHT)

(a) Open or close the following jumper options as indicated. All other jumper options are to remain as delivered from the factory except for the drive select jumpers and the terminator at location D2.

close	open
C	X
RM	RS

(b) Install the terminator at location D2 only on the last drive.

(c) Connect drive select jumpers as follows:

DS1= Drive A
DS2= Drive B
DS3= Drive C
DS4= Drive D

MITSUBISHI M2894-63 (FULL HEIGHT)

(a) Open or close the following jumper options as indicated. All other jumper options are to remain as delivered from the factory except for the drive select jumpers and the terminator at location A5.

close	open
Z	Y
HUN	HUD

(b) Open the following shunts:

PJ4
PJ5
PJ8

(c) Install the terminator at location A5 only on the last drive.

(d) Connect drive select jumpers as follows:

DS1= Drive A
DS2= Drive B
DS3= Drive C
DS4= Drive D

SEIMENS FDD100-8D

(a) Install jumper SS.

(b) Open trace from G to "center" and connect "center" to H as indicated below:

(c) Connect drive select jumpers as follows:

DS1= Drive A
DS2= Drive B
DS3= Drive C
DS4= Drive D

TANDON TM100-2 (5 1/4" drive)

Open or close the indicated shunts for drives A through D, respectively:

	DRIVE A	DRIVE B	DRIVE C	DRIVE D
1-16	open	open	open	open
2-15	close	open	open	open
3-14	open	close	open	open
4-13	open	open	close	open
5-12	open	open	open	close
6-11	open	open	open	open
7-10	open	open	open	open
8-9	open	open	open	open

****** PERSONALITY BOARD USERS GUIDE ******
**** SECTION ****

PERSONALITY BOARD INDEX

INTRODUCTION

Since the introduction of the S100 Bus standard, compatability amongst S100 Bus products has been difficult to achieve. The CPZ4800X Single Board Central Processor(SBCP) solved these problems by effectively replacing four to five boards. By implementing the functions necessary to construct a system all on one board, interface and timing problems quickly disappeared. One problem, however, remained. The problem was to find an effective way of interfacing the SBCP with a great variety of peripheral devices without the necessity of modifying the SBCP for each devise. In the past, this entailed the necessity of modifying the PCB's with etch cuts and straps. This usually resulted in unattractive modifications to say nothing of the resultant inflexability for later integrating still other peripheral devices. This problem was effectively solved by customizing the peripheral interfaces through "personality" boards. Thus, the floppy, serial and parallel interfaces were brought out to connectors at the top of the board and those interfaces were tailored through small printed circuit boards connected to the main board by ribbon cables. In short, a personality board is a small circuit board containing line drivers/receivers, logic and other circuitry required to connect the CPZ4800X SBCP I/O controllers (Floppy Disk, Serial Controller and Parallel Controller) to a variety of peripheral devices.

ICM'S PERSONALITY BOARDS offer a very versatile, cost effective technique for peripheral interface. The personality boards mount on the back of your system's mainframe or chassis. Whenever you decide to change peripherals or protocols, all you have to do is change the small, inexpensive personality board - not make expensive and complicated changes to your CPU board. ICM has existing PERSONALITY BOARDS and Software Drivers for most peripherals and protocols on the market today. New PERSONALITY BOARDS are constantly being developed as new peripherals enter the market.

Personality Board Buyer's Guide
From Intercontinental Micro Systems

PERSONALITY BOARDS:
PERIPHERAL INTERFACE

ICM'S PERSONALITY BOARDS offer a very versatile, cost effective technique for peripheral interface. The personality boards mount on the back of your system's mainframe or chassis. Whenever you decide to change peripherals or protocols, all you have to do is change the small, inexpensive personality board - not make expensive and complicated changes to your CPU board. ICM has existing PERSONALITY BOARDS and Software Drivers for most peripherals and protocols on the market today. New PERSONALITY BOARDS are constantly being developed as new peripherals enter the market.

PERSONALITY BOARDS are not only cost effective and inexpensive, they also protect the CPZ48000 SBC whenever new or different peripherals are placed on your system. First, since the buffers and drivers necessary to interface to the peripherals are on the personality board and not on the CPZ, there is no need to make costly and complicated cuts or jumpers on the CPZ. Second, any current surges on the communication lines between the CPZ and the peripheral will blow the surge suppressors on the Personality Board and not the CPZ. Thus you only have to replace a small, inexpensive board - not a large,expensive SBC board.

PERSONALITY BOARD - RS232/NO MODEM
Part Number - RPB100
Function

The RS232/NO MODEM Personality Board provides RS232 drivers and receivers, terminations and jumper options to interface any simple RS232 device such as CRT terminals, serial printers or any other serial device not requiring an extensive handshake protocol.

This module may be used with either the CPZ48000 SBCP or the CPS-MX SBSP.

PERSONALITY BOARD - RS232/FULL MODEM
Part Number - MPB100
Function

The RS232C/FULL MODEM Personality Board provides RS232 drivers/receivers and jumper options to interface asynchronous or synchronous modems with varying types of bit oriented protocols such as IBM Bi-Sync, HDLC or SDLC. Jumpers provided enable the user to configure the board for either asynchronous or synchronous operation.

This module may be used with either the CPZ48000 SBCP or the CPS-MX SBSP.

PERSONALITY BOARD - RS422 SERIAL COMMUNICATIONS
Part Number - FFT100
Function

The FFT100 personality board provides RS422 differential line drivers and receivers. These balanced drivers and receivers can provide serial communications for distances of up to 4000 feet at a communications rate of 100 Kbits/second. This assumes that 24 AWG twisted pair cable is used. Higher rates may be attained for shorter cable lengths. If the CPU's SIO controller is used in synchronous communications mode at its maximum rate of 800 Kbits/second, the maximum cable length recommended is 325 feet. Drivers and receivers are provided for all signals of the SIO to support full handshake protocols.

The FFT100 in combination with the Long Distance Serial Personality Board (LDS100), provides a means of connecting terminals, printers and other RS232 serial devices remotely located from the CPU mainframe. CPU-to-CPU communications may also be set-up over long distances by using the FFT100 at both CPUs. In this case, the interconnecting cable is cross-connected to tie receiver-to-transmitter and transmitter-to-receiver devices. No cross-connection is required between the FFT100 and the LDS100.

Jumper options are provided to minimize the number of cable lines required if no handshaking signals are required as in the case of simple RS232 Terminals where only transmit and receive signals are required. Ground is also provided but is not used in most cases.

This module may be used with either the CPZ48000 SBCP or the CPS-MX SBSP.

PERSONALITY BOARD - LONG DISTANCE SERIAL COMMUNICATIONS
Part Number - LDS100
Function

The LDS100 personality board provides RS422 differential line drivers and receivers. This SHORT HAUL MODEM can provide serial communications for distances of up to 4000 feet at a communications rate of 100 Kbits/second. This assumes that 24 AWG twisted pair cable is used. Drivers and receivers are provided to support full handshake protocols.

The LDS100 in combination with the RS422 Serial Communications Personality Board (FFT100), provides a means of connecting terminals, printers and other RS232 serial devices remotely located from the CPU mainframe. Jumper options are provided to minimize the number of cable lines connected if no handshaking signals are required as in the case of simple RS232 Terminals where only transmit and receive signals are used. Ground is also provided but is not used in most cases.

AC power must be provided to the board. The board may be strapped for either 115VAC/60HZ or 230VAC/50HZ operation.

PERSONALITY BOARD - FLOPPY DISK CONTROLLER
Part Number - FPB100-XY
Function

The FLOPPY DISK CONTROLLER personality board provides line drivers and receivers, terminators, logic and a jumper option to interface either an 8-inch of a 5¼-inch floppy disk drive with the CPZ48000 SBCP. A DB25 connector is available as the means to interface with the drive interface; however, if other types of commonly used connectors are required, adapters are available to tailor the interface appropriately.

This module is used only on the CPZ48000 SBCP.

PERSONALITY BOARD - CENTRONICS PRINTER
Part Number - CPI100
Function

The Centronics Printer Personality Board provides line drivers receivers, terminators, jumper options and data strobe generator logic to interface to any printer compatible with the Centronics parallel interface.

This module may be used with either the CPZ48000 SBCP or the CPS-MX SBSP.

PERSONALITY BOARD - PRIAM INTELLIGENT HARD DISK
Part Number - PRI100
Function

PRIAM provides two intelligent hard disk interface controllers referred to as the "SMART" and the "SMART-E". These are preprogrammed microprocessor based controllers. They may be used for the entire line of PRIAM Winchester disc drives which range in capacity from 10 megabytes to 157 megabytes and come in eight or fourteen inch packaging. Up to four drives in any combination of drive sizes may be interconnected. The controllers support a variety of read sector, write sector and format commands. Data transfers may be either programmed I/O or DMA. The SMART-E has all the features that the SMART has in addition to error detection & correction, logical sector addressing, sector interleaving, parity generation & testing, direct data transfers and a 2 Kbyte data buffer (SMART has a 1 Kbyte buffer). The interface performs the entire function of detailed disc control while presenting to the host a basic and cost effective interface.

The PRI100 Personality Board connects the parallel port of the CPZ48000 SBCP or the CPS-MX SBSP to the SMART or SMART-E controllers. Thus, a very powerful disc subsystem may be directly connected to the ICM line of processors via the PRI100.

A jumper option is provided on the PRI100 to configure it for either the SMART or the SMART-E controller. The controllers mount along the drive sides alleviating the need for additional S-100 Bus slots. An adapter, PRI100-1, is provided allowing direct connection of the PRI100 to the smart controllers.

PERSONALITY BOARD - SHUGART ASSOCIATES SYSTEM INTERFACE
Part Number - SAS100
Function

The Shugart Associates System Interface (SASI) defines a Local I/O Bus which can be operated at data rates up to 1.5 megabytes per second. This bus provides I/O device independence so that disk drives, tape drives, printers and various other peripherals may be interfaced on the same I/O bus without modification to the host CPU's hardware or software. The interface protocol provides for connection of multiple initiators (devices capable of initiating an operation) and multiple targets (devices capable of responding to requests for operations). Arbitration logic is built in and a priority system awards control to the device that wins arbitration.

The SAS100 personality board converts the parallel port of either the CPZ48000 SBCP or the CPS-MX SBSP to a SASI I/O bus. Software is provided to emit bus timing in conformance with the SASI specification. The system integrator may interface SASI controllers such as the Data Technology Corporation, Zebec and Sysgen line of controllers. Each have powerful attributes such as connecting hard disks with floppies, hard disks with tape streamers and connecting to high performance SMD hard disk drives.

The SAS100 personality board is accompanied by an adapter board (SAS100-1). This adapter board converts the SAS100 DB25 connector interface to a 50 pin header connector interface with a pin assignment in exact conformance with the SASI Bus specification. The integrator may connect directly to the SAS100 with a DB25-to-SASI Interface cable or may connect via the SAS100-1 with a 50 pin flat ribbon cable.

PERSONALITY BOARD - CLOCK/CALENDAR
Part Number - CCB100
Function

The CCB100 provides a highly accurate real time clock which may be set by the CPZ48000 SBCP or the CPS-MX SBSP under software control. The time of year, month, day, hour, minute and second is maintained and may be read back by the CPU. A Ni-Cad battery is used to provide backup power to the time control chip. In this manner the real time clock is continuously maintained even during extensive down time. This feature is quite useful for point-of-sale systems, inventory systems and other applications where continuous clock monitoring is required. This board is also very useful in operating systems which feature date and time stamping such as TurboDOS. In a TurboDOS based system, this board may be connected to the master (CPZ48000) parallel port or may be connected to any one slave (CPS-MX) parallel port.

Personality Board Index

		part number
1	RS232C/ NO MODEM	RPB100
2	RS232C/ FULL MODEM	MPB100
3	RS422 SERIAL COMMUNICATIONS	FFT100
4	LONG DISTANCE SERIAL COMMUNICATIONS	LDS100
5	FLOPPY DISK	FPB100
6	CENTRONICS PRINTER	CPI100
7	PRIAM INTELLIGENT HARD DISK	PRI100
8	SHUGART ASSOCIATES SYSTEMS INTERFACE	SAS100
9	CLOCK/CALENDAR (WITH BATTERY BACKUP)	CCB100

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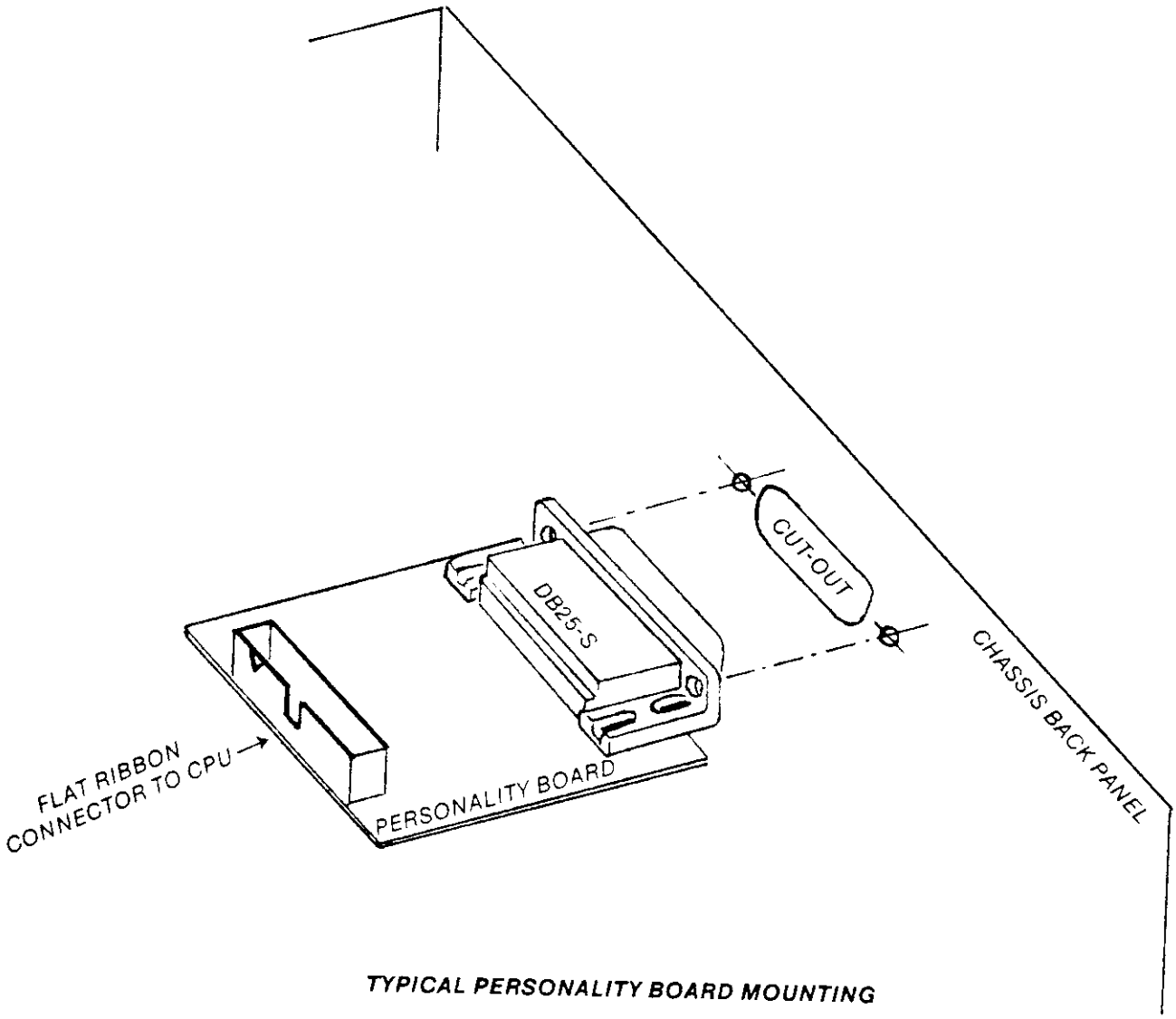


TYPICAL PERSONALITY BOARD MOUNTING

PERSONALITY BOARDS are not only cost effective and inexpensive, they also protect the CPZ-4800X SBC whenever new or different peripherals are placed on your system. First, since the buffers and drivers necessary to interface to the peripherals are on the personality board and not on the CPZ, there is no need to make costly and complicated cuts or jumpers on the CPZ. Second, any current surges on the communication lines between the CPZ and the peripheral will blow the surge suppressors on the Personality Board and not the CPZ. Thus you only have to replace a small, inexpensive board not a large, expensive SBC board.

Typical S-100 Bus chassis provide DB25 connector cutouts at the chassis rear. The personality boards are designed to mount on DB25 connectors which in turn are mounted in the cutouts. In this manner, the personality boards do not require additional S-100 Bus slots and are conveniently mounted within the chassis. An additional connector is provided to connect the personality board to the SBCP. The connection is made with a simple point-to-point flat ribbon cable. See figure 1.

Intercontinental Micro Systems Corporation invites you, our valued customer, to submit your interface requirements if they are not covered by the line of personality boards available. Our engineering staff will evaluate those requirements and advice you of the feasibility of constructing your custom personality board.

PERSONALITY BOARD INTERCONNECTION INSTRUCTIONS

The CPZ-4800X has four connectors at the top of the board numbered J1 through J4. These are listed below:

J1 - FDC Connector
J2 - DART/SIO Port A Connector
J3 - DART/SIO Port B Connector
J4 - PIO Connector

Tables A through D describe signal pin assignments for connectors J1 through J4 respectively.

At a minimum, the FDC and DART/SIO Port B personality boards must be installed. The instructions follow:

1.- Select a DB25 connector cutout at the rear of the chassis for the FDC personality board.
2.- Insert and hold the FDC personality board in the cutout. External to the chassis, plug in the desired connector adaptor and hold in place.
3.- Install #6 nuts, washers and bolts passing the bolts through the connector adapter and through the personality board's DB25 connector.
4.- Install the flat ribbon cable provided at the personality board and at the CPZ-4800X, connector J1.
5.- Follow the above procedure, except that an adapter is not used, for the DART/SIO Port B personality board.
6.- Install cables from the chassis connectors to the respective peripherals.

Table A

Connector J1 Pin Assignments

PIN NO.	SIGNAL NAME	DESCRIPTION
1	INT7*	INTERRUPT (LEVEL 7) TO CPU
2	DS1*	DRIVE SELECT #1 FROM CPU
3	GND	GROUND
4	DS2*	DRIVE SELECT #2 FROM CPU
5	GND	GROUND
6	DS3*	DRIVE SELECT #3 FROM CPU
7	GND	GROUND
8	DS4*	DRIVE SELECT #4 FROM CPU
9	GND	GROUND
10	DIRC	DIRECTION CONTROL FROM CPU
11	GND	GROUND
12	STEP	STEP CONTROL FROM CPU
13	GND	GROUND
14	WRITE DATA	WRITE DATA FROM CPU
15	GND	GROUND
16	WGATE	WRITE GATE FROM CPU
17	GND	GROUND
18	TRACK 0*	TRACK 0 STATUS TO CPU
19	GND	GROUND
20	WRITE PROT*	WRITE PROTECT TO CPU
21	GND	GROUND
22	READ DATA*	READ DATA TO CPU
23	GND	GROUND
24	SSO	SIDE SELECT OUTPUT FROM CPU
25	GND	GROUND
26	HLD	HEAD LOAD COMMAND FROM CPU
27	GND	GROUND
28	INDEX*	INDEX PULSE TO CPU
29	GND	GROUND
30	READY	READY STATUS TO CPU
31	GND	GROUND
32	MOTOR ON	MOTOR ON STATUS FROM CPU
33	GND	GROUND
34	TK43	TRACK 43 STATUS FROM CPU
35	GND	GROUND
36	+8VDC	+8VDC
37	GND	GROUND
38	HLTIMER	HEAD LOAD TIMER TO CPU
39	GND	GROUND
40	+5VDC	+5VDC

Table B

Connector J2 Pin Assignments

PIN NO.	SIGNAL NAME	DESCRIPTION
1	ADSR*	DATA SET READY TO CPU
2	ATXC*	TRANSMIT CLOCK TO/FROM CPU
3	ARXC*	RECEIVE CLOCK TO/FROM CPU
4	ATxD	TRANSMIT DATA FROM CPU
5	ARxD	RECEIVE DATA TO CPU
6	ARTS*	REQUEST TO SEND DATA FROM CPU
7	ACTS*	CLEAR TO SEND TO CPU
8	ADCD*	DATA CARRIER DETECT TO CPU
9	ADTR*	DATA TERMINAL READY FROM CPU
10	ARNG*	RINGING INDICATOR TO CPU
11	ABRCLK	BAUD RATE CLOCK FROM CPU
12	GND	GROUND
13	+16VDC	+16VDC
14	-16VDC	-16VDC
15	+5VDC	+5VDC
16	GND	GND

TABLE C

Connector J3 Pin Assignments

PIN NO.	SIGNAL NAME	DESCRIPTION
1	BDSR*	DATA SET READY TO CPU
2	BTXC*	TRANSMIT CLOCK TO/FROM CPU
3	BRXC*	RECEIVE CLOCK TO/FROM CPU
4	BTxD	TRANSMIT DATA FROM CPU
5	BRxD	RECEIVE DATA TO CPU
6	BRTS*	REQUEST TO SEND DATA FROM CPU
7	BCTS*	CLEAR TO SEND TO CPU
8	BDCD*	DATA CARRIER DETECT TO CPU
9	BDTR*	DATA TERMINAL READY FROM CPU
10	BRNG*	RINGING INDICATOR TO CPU
11	BBRCLK	BAUD RATE CLOCK FROM CPU
12	GND	GROUND
13	+16VDC	+16VDC
14	-16VDC	-16VDC
15	+5VDC	+5VDC
16	GND	GND

TABLE D

Connector J4 Pin Assignments

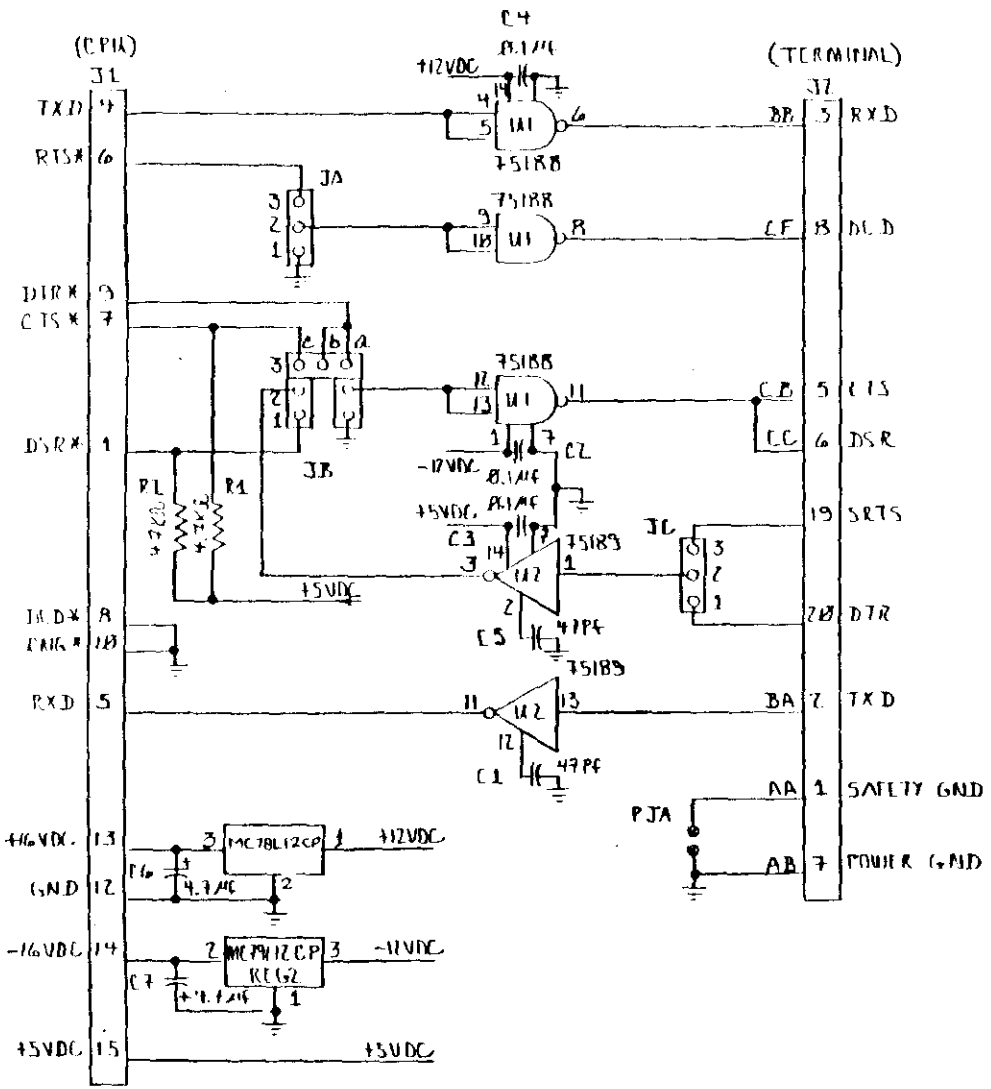
PIN NO.	SIGNAL NAME	DESCRIPTION
1	RDYA	PORT A READY TO PERIPHERAL
2	STBA*	PORT A STROBE TO CPU
3	RDYB	PORT B READY TO PERIPHERAL
4	STBB*	PORT B STROBE TO CPU
5	D0A	PORT A DATA BIT 0
6	D1A	PORT A DATA BIT 1
7	D2A	PORT A DATA BIT 2
8	D3A	PORT A DATA BIT 3
9	D4A	PORT A DATA BIT 4
10	D5A	PORT A DATA BIT 5
11	D6A	PORT A DATA BIT 6
12	D7A	PORT A DATA BIT 7
13	D0B	PORT B DATA BIT 0
14	D1B	PORT B DATA BIT 1
15	D2B	PORT B DATA BIT 2
16	D3B	PORT B DATA BIT 3
17	D4B	PORT B DATA BIT 4
18	D5B	PORT B DATA BIT 5
19	D6B	PORT B DATA BIT 6
20	D7B	PORT B DATA BIT 7
21	RESET*	SYSTEM RESET FROM CPU
22	GND	GROUND
23	PINT*	PARALLEL PORT INTERRUPT TO CPU
24	GND	GROUND
25	PCLK	PARALLEL PORT CLOCK FROM CPU
26	+5VDC	+5VDC

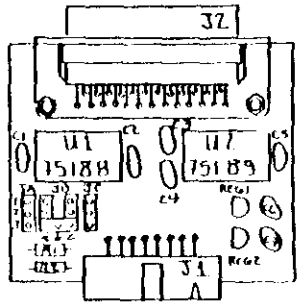
DESCRIPTION

Each personality board shall be described in the following sections. A brief functional description, interface requirements, mating connector requirements and set-up instructions, where applicable, are given for each board.

****
* WARNING *
****

Do not install or remove any personality board while the CPZ4800X SBCP or the CPS-MX SBSP power is on. This may result in damage to the personality board and/or the CPU board.





JUMPER OPTIONS

(1) 3 WIRE / NO HANDSHAKE :

JA	JB	JC
1-2	A1-A2	1-2 = CRT
	C1-C2	2-3 = PRINTER (CHECK PRINTER MANUAL)
	B3-C3	

(2) FULL HANDSHAKE :

JA	JB	JC
2-3	A2-A3	1-2 = CRT
	C2-C3 OR	2-3 = PRINTER (CHECK PRINTER MANUAL)
	C1-C2	

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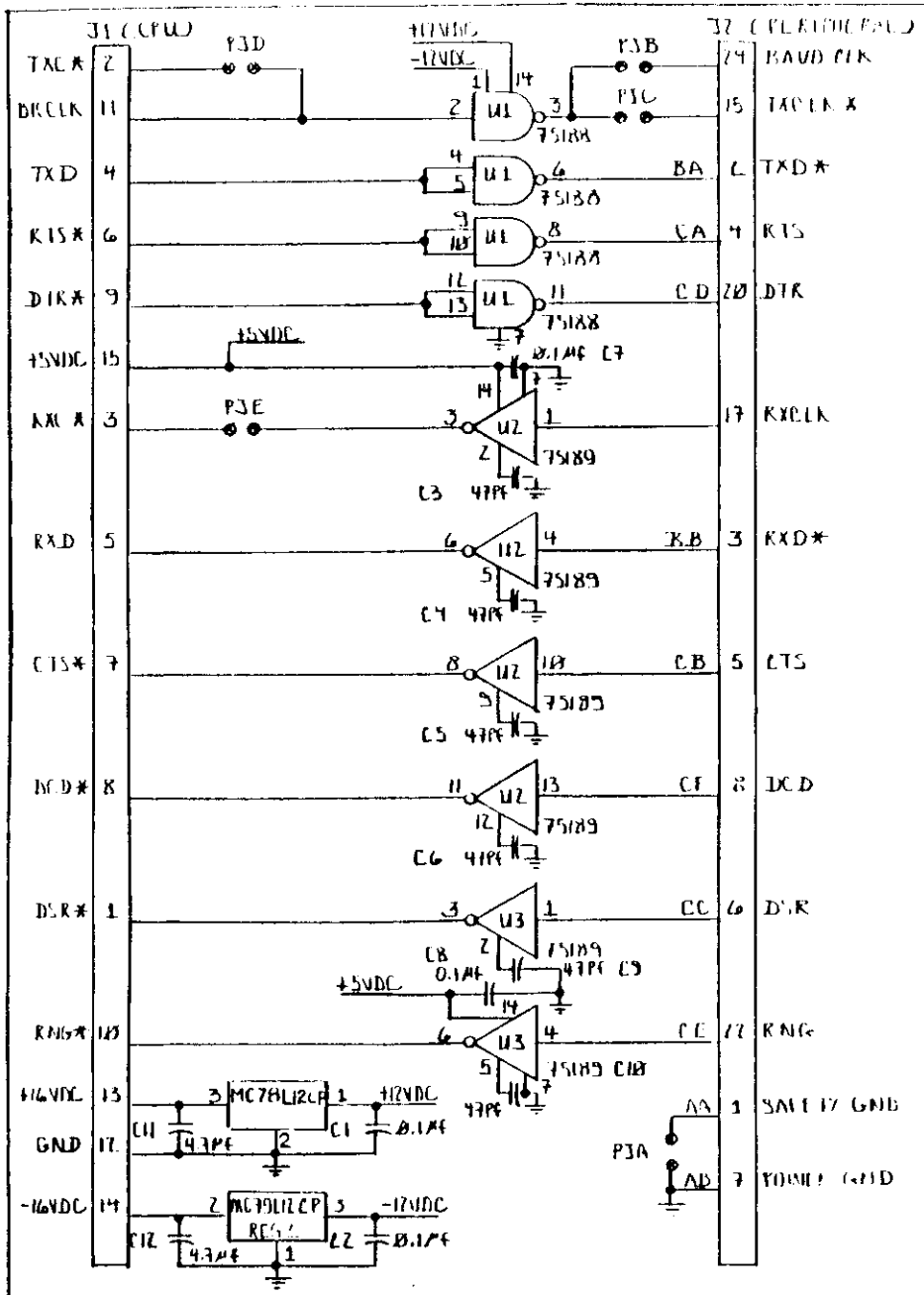
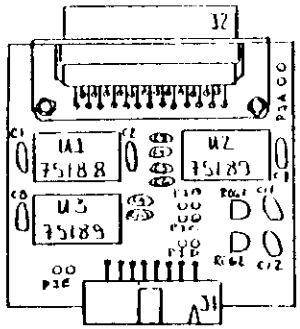
DESIGNED:	SCHEMATIC / LOGIC DIAGRAM FOR RS 232 / NO MODEM PERSONALITY BOARD
REV: A	
	PART NO R PB 1000
	SHT OF 1





JUMPER OPTIONS

(1) ASYNCHRONOUS MODEM:

P3B, P3C, P3D, P3E ALL OPEN

(2) SYNCHRONOUS MODEM:

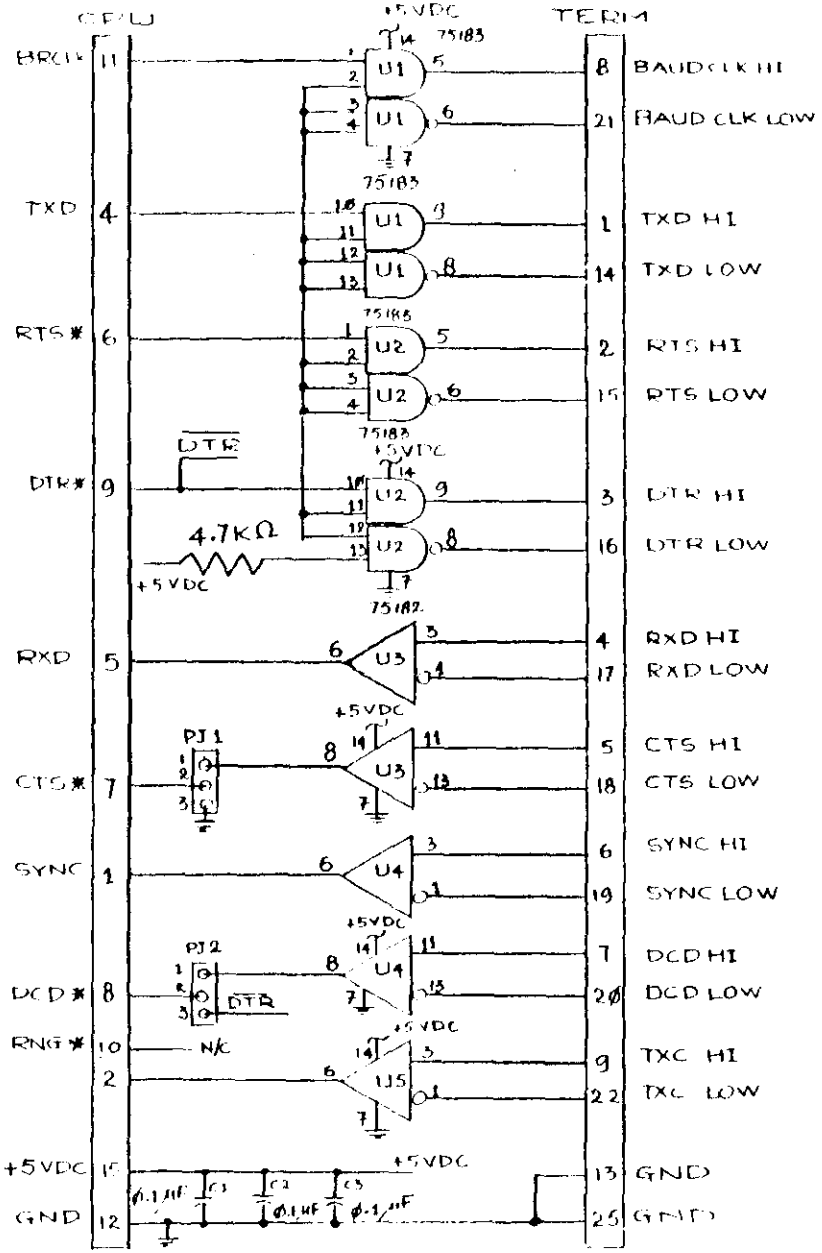
P3D & P3E CONNECTED & CUT P3D 1-2 & 2-3 ON CPZ-430001 IF PORT A

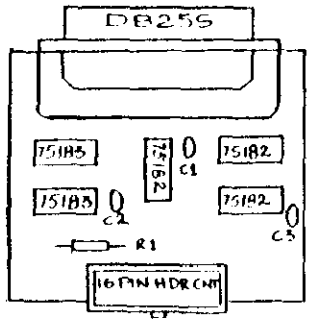
CUT P3A ON CPZ-430001 IF PORT B

P3B OR P3C CONNECTED (FUNCTION OF MODEM TYPE)

Intercontinental Micro Systems

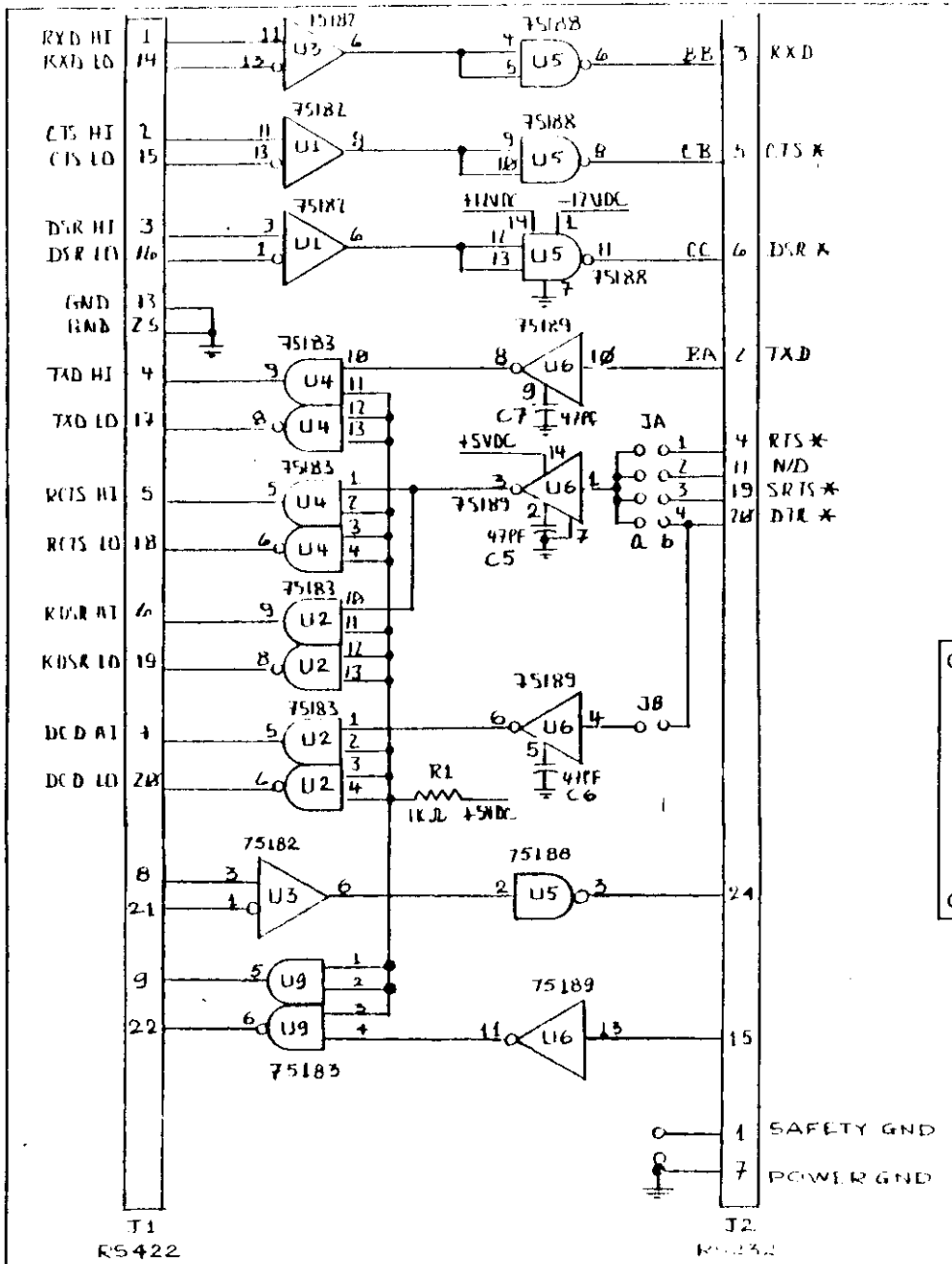
DESIGNED:	SCHEMATIC/LOGIC DIAGRAM FOR RS232C FULL MODEM PERSONALITY BOARD
REV: A	
	PART NO. 999-0000
	SHT 01 OF 1

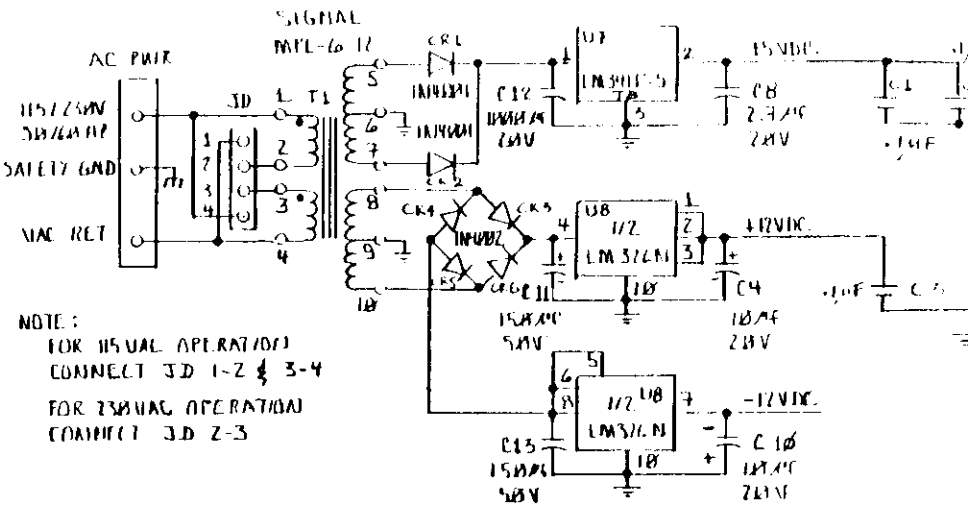


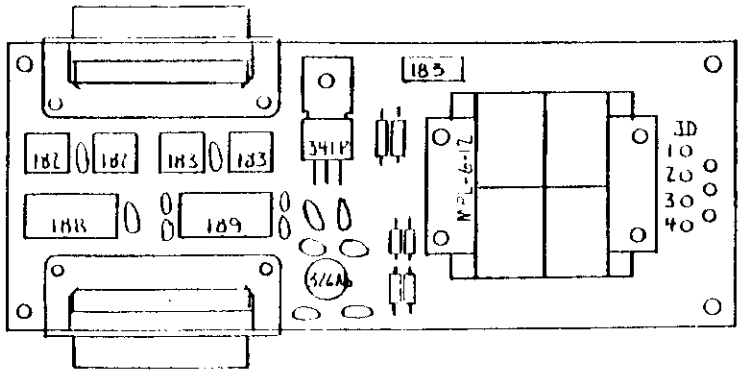


Intercontinental Micro Systems

DESIGNED:	
REV: A	SCHEMATIC/LOGIC DIAGRAM FOR RS-422 SERIAL COMMUNICATION PERSONALITY BOARD
	PART NO. FTTIØØ-1
	SHT OF 1

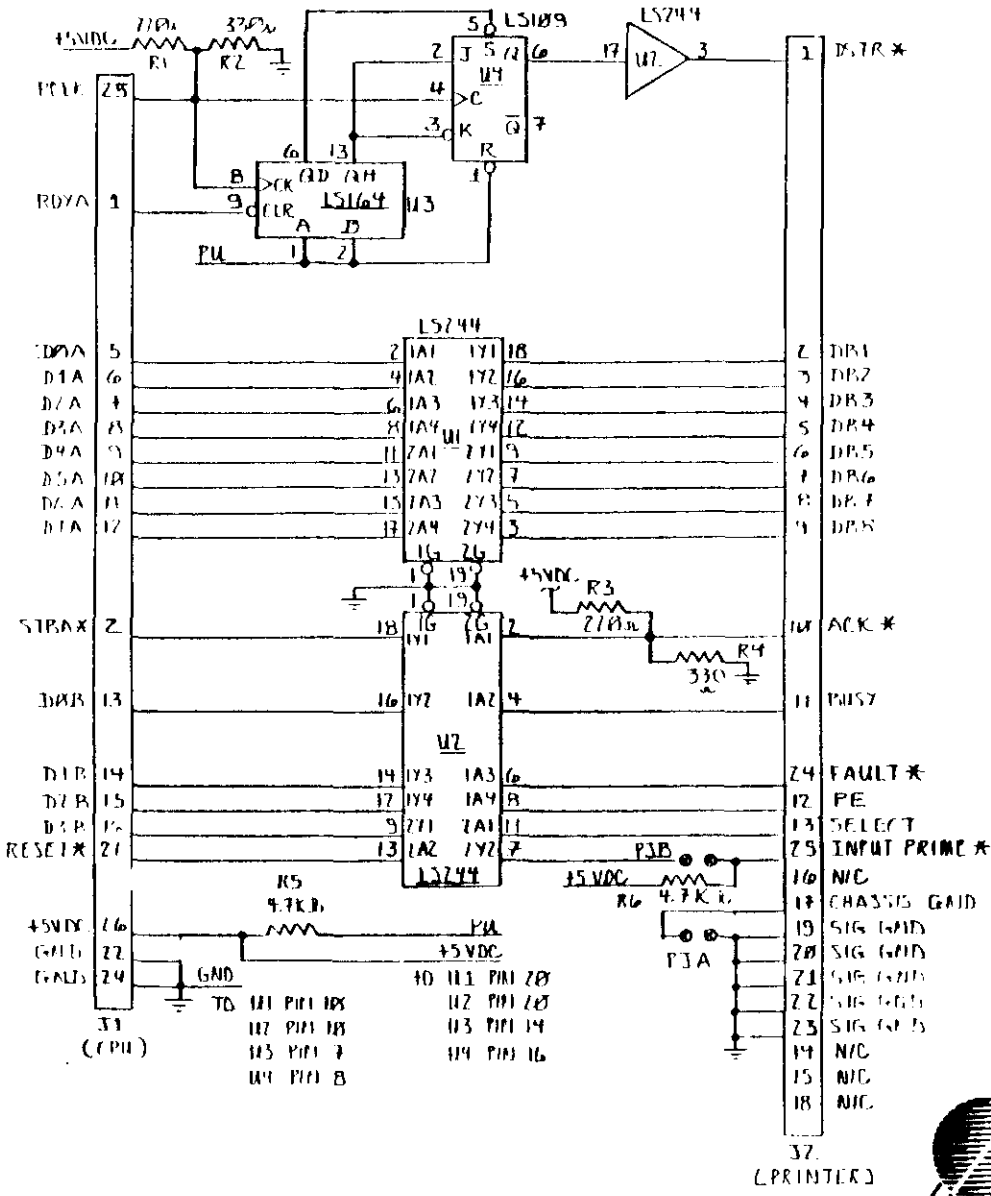


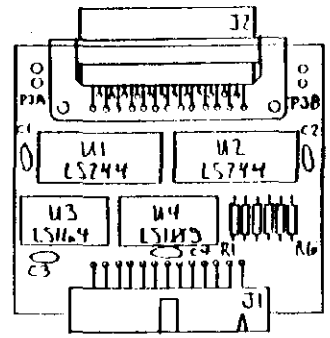




Intercontinental Micro Systems

DESIGNED:	SCHEMATIC / LOGIC DIAGRAM FOR LONG DISTANCE SERIAL LINK PERSONALITY BOARD
REV: A	PART NO. LDS188





NOTE : C1 - C4 = DECOUPLING CAPS. 0.1 μf

Intercontinental Micro Systems

DESIGNED:	
REV: -	SCHEMATIC/LOGIC DIAGRAM FOR CENTRONICS PRINTER PARALLEL INTERFACE PERSONALITY BOARD
	PART NO. CPI 100
	SHT 01 OF 2

CENTRONICS		P1	
1	DATA STROBE	1	DSTR *
2	DATA 1	2	DB1
3	DATA 2	3	DB2
4	DATA 3	4	DB3
5	DATA 4	5	DB4
6	DATA 5	6	DB5
7	DATA 6	7	DB6
8	DATA 7	8	DB7
9	DATA 8	9	DB8
10	ACKNLG*	10	ACK *
11	BUSY	11	BUSY
12	PE	12	PE
13	SLCT	13	SELECT
14	+/- 5V		N/C
15	OSC X		N/C
16	+/- 5V OR EMPTY	16	EMPTY *
17	CHASSIS GND	17	CHASSIS GND
18	+5V		N/C
19	GND	19	GND
20	GND	20	GND
21	GND	21	GND
22	GND	22	GND
23	GND	23	GND
24	GND		GND
25	GND		GND
26	GND		GND
27	GND		GND
28	GND		GND
29	GND		GND
30	GND		GND
31	INPUT PRIME *	25	INPUT PRIME *
32	FAULT *	24	FAULT
33	N/C		N/C

CENTRONICS		P1
34	LINE PRINT PULSE	N/C
35	GND	GND
36	N/C	N/C

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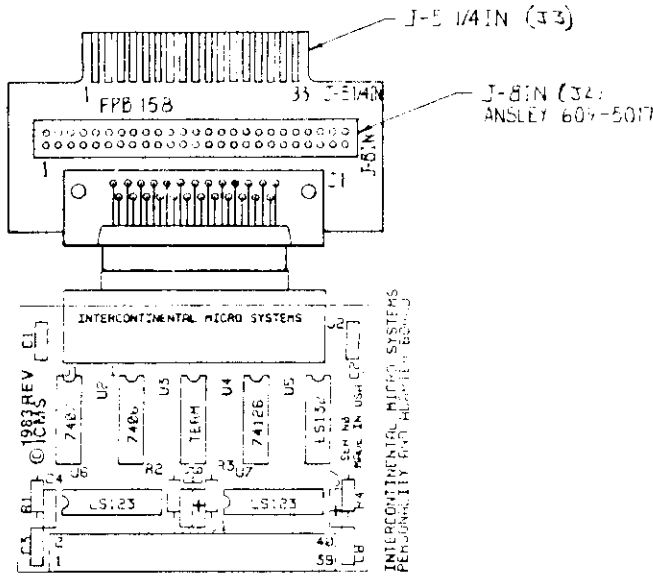
CONNECTION TABLE

FUNCTION	J2	J-8IN[1]	J-5¼IN[1]
DS1*	1	26	10
DS2*	2	28	12
DS3*	3	30	14
DS4*	4	32	6
DIRC*	5	34	18
STEP*	6	36	20
WRITE DATA*	7	38	22
WRITE GATE*	8	40	24
TRACK 0*	9	42	26
WRITE PROT*	10	44	28
READ DATA*	11	46	30
SSO*	12	14	32
HEAD LOAD*	13	18	--
INDEX*	14	20	8
READY*	15	22	--
MOTOR ON*	16	24	16
TK 43*	17	2	--
--	18	--	--
--	19	--	--
GND	20	--	--
GND	21	--	--
GND	22	--	--
GND	23	--	--
GND	24	--	--
GND	25	--	--

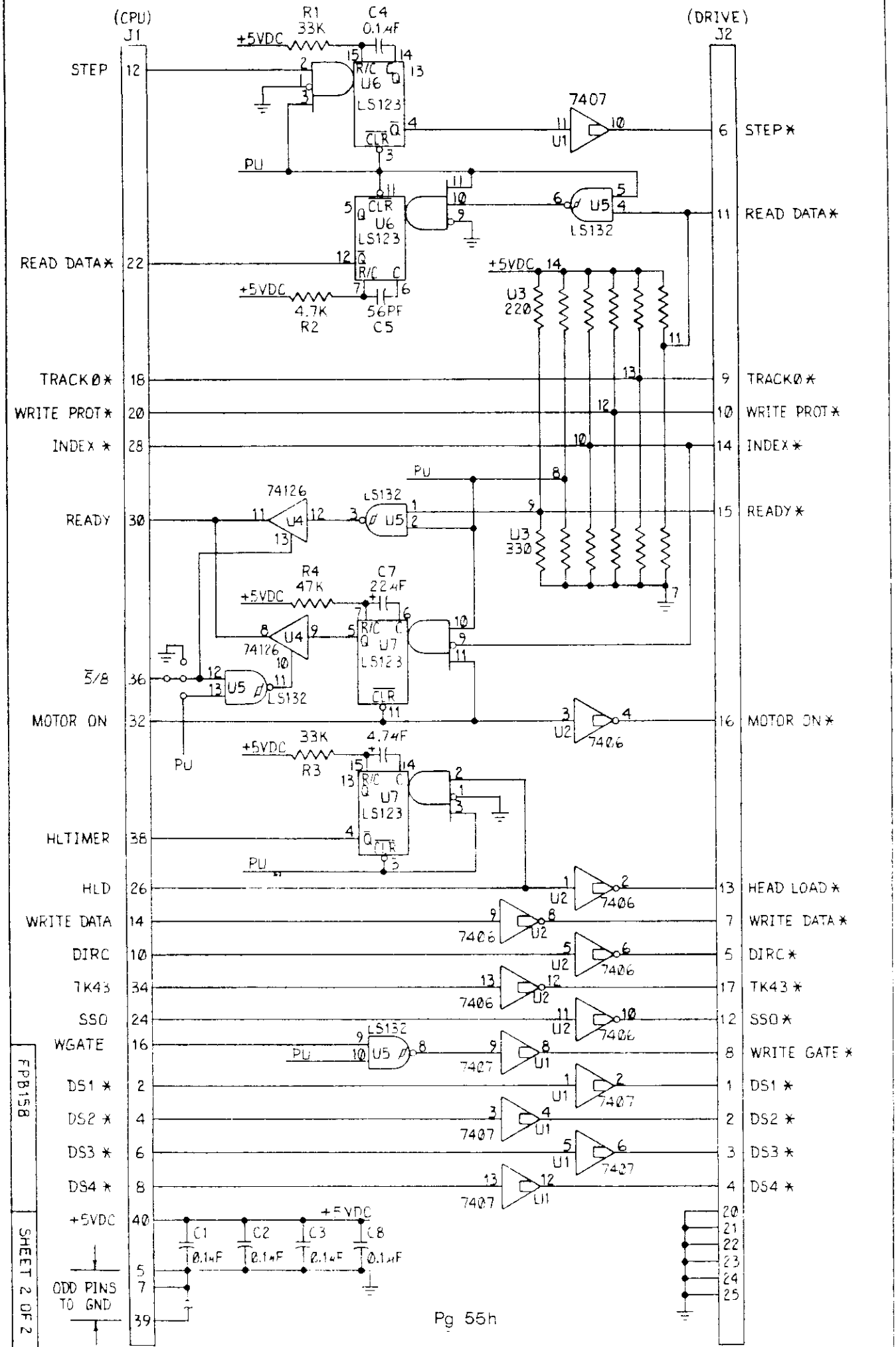
NOTE 1: On J-8IN & J-5¼IN, all odd pins are grounded; all even pins not listed are open.



SCHEMATIC/LOGIC DIAGRAM
8-5¼ INCH
FLOPPY DISK CONTROLLER
PERSONALITY BOARD

PART NO. FPB 158-XY

OCT. 25. 1983 SHEET 1 OF 2


(CPU)
J1
(DRIVE)
J2
STEP
READ DATA*
TRACK0*
WRITE PROT*
INDEX*
READY
5/8
MOTOR ON
HLTIMER
HLD
WRITE DATA
DIRC
TK43
SSO
WGATE
DS1*
DS2*
DS3*
DS4*
+5VDC
ODD PINS TO GND
R1 33K
C4 0.1uF
R2 4.7K
C5 56PF
R3 33K
C6 4.7uF
R4 47K
C7 22uF
U1 7407
U2 7406
U3 220
U3 330
U4 74126
U5 LS132
U6 LS123
U7 LS123
PU
STEP*
READ DATA*
TRACK0*
WRITE PROT*
INDEX*
READY*
MOTOR ON*
HEAD LOAD*
WRITE DATA*
DIRC*
TK43*
SSO*
WRITE GATE*
DS1*
DS2*
DS3*
DS4*
C1 0.1uF
C2 0.1uF
C3 0.1uF
C8 0.1uF
FPB158
SHEET 2 OF 2

PERSONALITY BOARD - RS232/NO MODEM

PART NUMBER - RPB100

FUNCTION

The RS232/NO MODEM Personality Board provides RS232 drivers and receivers, terminations and jumper options to interface any simple RS232 device such as CRT terminals, serial printers or any other serial device not requiring an extensive handshake protocol.

This module may be used with either the CPZ4800X SBCP or the CPS-MX SBSP.

INTERFACE REQUIREMENTS

Connects to J2 or J3 of the CPZ4800X or the CCPS-MX.

J1(CPU)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DSR*	DATA SET READY TO CPU
2	n/c	n/c
3	n/c	n/c
4	TxD	TRANSMIT DATA FROM CPU
5	RxD	RECEIVE DATA TO CPU
6	RTS*	REQUEST TO SEND DATA FROM CPU
7	CTS*	CLEAR TO SEND TO CPU
8	DCD*	DATA CARRIER DETECT TO CPU
9	DTR*	DATA TERMINAL READY FROM CPU
10	RNG*	RINGING INDICATOR TO CPU
11	n/c	n/c
12	GND	GROUND
13	+16VDC	+16VDC
14	-16VDC	-16VDC
15	+5VDC	+5VDC
16	n/c	n/c

J2(PERIPHERAL)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	SAFETY GND	SAFETY GROUND
2	TXD	TRANSMIT DATA TO PERIPHERAL
3	RXD	RECEIVE DATA FROM PERIPHERAL
4	n/c	n/c
5	CTS*	CLEAR TO SEND TO PERIPHERAL
6	DSR*	DATA SET READY TO PERIPHERAL
7	POWER GND	POWER GROUND
8	DCD*	DATA CARRIER DETECT TO PERIPHERAL
9	n/c	n/c
10	n/c	n/c
11	n/c	n/c
12	n/c	n/c
13	n/c	n/c
14	n/c	n/c
15	n/c	n/c
16	n/c	n/c
17	n/c	n/c
18	n/c	n/c
19	SRTS*	SECONDARY REQUEST TO SEND FROM PERIPHERAL
20	DTR*	DATA TERMINAL READY FROM PERIPHERAL
21	n/c	n/c
22	n/c	n/c
23	n/c	n/c
24	n/c	n/c
25	n/c	n/c

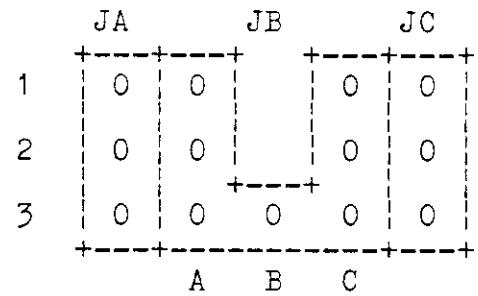
CONNECTOR REQUIREMENTS

PERSONALITY BOARD CONNECTORS	MATING CONNECTORS
J1 - ANSLEY 609-1617	ANSLEY 609-1630 (ICM SUPPLIED)
J2 - CANNON DB25P-731	CANNON DB 25S-731 (CUSTOMER SUPPLIED)

SET UP INSTRUCTIONS

Three Jumper Areas are provided: JA, JB and JC. Refer to the figure below for the following set-up instructions:

[JA/JB/JC] area



JA

The CPU may be required to provide handshaking with the peripheral through the signal "DCD". If that handshaking signal is required, connect pin 2 to pin 3 with the jumper provided. If no handshaking signal is required , connect pin 2 to pin 1.

JB

The CPU may required to provide handshaking with the peripheral through the signall "CTS". Furthermore, it may accept the signals "DTR" or "SRTS" through the input "CTS". The following options are available:

JB	Configuration
1A-2A	no handshaking provided to peripheral at "CTS"
2A-3A	peripheral's "CTS" activated by CPU's "DTR"
3A-3B	not used
3B-3C	no handshaking provided to CPU's "CTS" by peripheral's "DTR" or "SRTS"
2C-3C	peripheral's "DTR" or "SRTS" activates CPU's "CTS"
1C-2C	peripheral's "DTR" or "SRTS" activates CPU's "DSR"

JC

The peripheral may provide either of two handshaking signals "SRTS" or "DTR". This jumper may select either signal as the source to the CPU's "CTS" or "DSR" inputs.

To connect "DTR" handshaking which is on pin 20 of the RS232/C interface, connect JC-1 to JC-2.

To connect "SRTS" handshaking which is on pin 19 of the RS232/C interface, connect JC-2 to JC-3.

EXAMPLES

1) Configure JA, JB and JC as follows for a simple terminal interface:

JA = 1-2
JB = 1A-2A / 3B-3C
JC = none required

2) Configure JA, JB and JC as follows for an Anadex Serial Printer, model DP-9501

JA = 2-3
JB = 1A-2A / 2C-3C
JC = 2-3

PERSONALITY BOARD - RS232/FULL MODEM

PART NUMBER - MPB100

FUNCTION

The RS232C/FULL MODEM PERSONALITY BOARD provides RS232 drivers/receivers and jumper options to interface asynchronous or synchronous modems with varying types of bit oriented protocols such as IBM Bi-Sync, HDLC or SDLC. Jumpers provided enable the user to configure the board for either asynchronous or synchronous operation.

This module may be used with either the CPZ4800X SBCP or the CPS-MX SBSP.

INTERFACE REQUIREMENTS

Connects to J1 or J2 of the CPZ4800X or the CPS-MX.

CPU (J1)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DSR*	DATA SET READY TO CPU
2	n/c	n/c
3	n/c	n/c
4	TXD	TRANSMIT DATA FROM CPU
5	RXD	RECEIVE DATA TO CPU
6	RTS*	REQUEST-TO-SEND FROM CPU
7	CTS*	CLEAR-TO-SEND TO CPU
8	DCD*	DATA CARRIER DETECT TO CPU
9	DTR*	DATA TERMINAL READY FROM CPU
10	RNG*	RINGING INDICATOR TO CPU
11	n/c	n/c
12	GND	GROUND
13	+16VDC	+16VDC
14	-16VDC	-16VDC
15	+5VDC	+5VDC
16	n/c	n/c

J2(PERIPHERAL)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	SAFETY GND	SAFETY GROUND
2	TXD	TRANSMIT DATA TO PERIPHERAL
3	RXD	RECEIVE DATA FROM PERIPHERAL
4	RTS*	REQUEST-TO-SEND TO PERIPHERAL
5	CTS*	CLEAR-TO-SEND FROM PERIPHERAL
6	DSR*	DATA SET READY FROM PERIPHERAL
7	POWER GND	POWER GROUND
8	DCD*	DATA CARRIER DETECT FROM PERIPHERAL
9	n/c	n/c
10	n/c	n/c
11	n/c	n/c
12	n/c	n/c
13	n/c	n/c
14	n/c	n/c
15	TXCLK*	TRANSMIT CLOCK TO PERIPHERAL
16	n/c	n/c
17	RXCLK*	RECEIVE CLOCK FROM PERIPHERAL
18	n/c	n/c
19	n/c	n/c
20	DTR*	DATA TERMINAL READY TO PERIPHERAL
21	n/c	n/c
22	RNG*	RINGING INDICATOR FROM PERIPHERAL
23	n/c	n/c
24	BAUD CLK	BAUD CLOCK TO PERIPHERAL
25	n/c	n/c

CONNECTOR REQUIREMENTS

PERSONALITY BOARD CONNECTORS	MATING CONNECTORS
J1 - ANSLEY 609-1617	ANSLEY 609-1630 (ICM SUPPLIED)
J2 - CANNON DB25P-731	CANNON DB 25S-731 (CUSTOMER SUPPLIED)

SET UP INSTRUCTIONS

The board may be configured for either asynchronous or synchronous modem requirements.

a) Asynchronous Modems

PJB, PJC, PJD, PJE and PJF are all open.

b) Synchronous Modems

1) MODEM SUPPLIES TRANSMIT AND RECEIVE CLOCK

Connect PJE and PJF only.

2) CPZ4800X OR CPS-MX SUPPLY TRANSMIT CLOCK

Connect PJC, PJD and PJE of MPB100 only.

Note: If using CPZ4800X Port A of the SIO, cut PJB A-B and B-C.

If using CPZ4800X Port B of the SIO, cut PJC.

If using CPS-MX Port A of the SIO, cut PJA A-B and B-C.

If using CPS-MX Port B of the SIO, cut PJB.

3) CPZ4800X OR CPS-MX SUPPLY BAUD RATE CLOCK

Same as (2) above except that on the MPB100, PJB is connected instead of PJC and PJF is disconnected.

c) If safety ground of the modem is to be tied to logic ground. connect PJA on the MPB100.

PERSONALITY BOARD - RS422 SERIAL COMMUNICATIONS

PART NUMBER - FTT100

FUNCTION

The FTT100 personality board provides RS422 differential line drivers and receivers. These balanced drivers and receivers can provide serial communications for distances of up to 4000 feet at a communications rate of 100 kbits/second. This assumes that 24 AWG twisted pair cable is used. Higher rates may be attained for shorter cable lengths. If the CPU's DART/SIO controller is used in synchronous communications mode at its maximum rate of 800 kbits/second, the maximum cable length recommended is 325 feet. Drivers and receivers are provided for all signals of the SIO to support full handshake protocols.

The FTT100 in combination with the Long Distance Serial Personality Board (LDS100), provides a means of connecting terminals, printers and other RS232 serial devices remotely located from the CPU mainframe. CPU-TO-CPU communications may also be set-up over long distances by using the FTT100 at both CPUs. In this case, the interconnecting cable is cross-connected to tie receiver-to-transmiter and tansmiter-to-receiver devices. No cross-connection is required between the FTT100 and the LDS100.

Jumper options are provided to minimize the number of cable lines required if no handshaking signals are required as in the case of simple RS232 Terminals where only transmit and receive signals are required. Ground is also provided but is not used in most cases.

This module may be used with either the CPZ4800X SBCP or the CPS-MX SBSP.

INTERFACE REQUIREMENTS

Connects to J1 or J2 of the CPZ4800X or the CPS-MX.

J1(CPU)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DSR*	DATA SET READY TO CPU
2	TXC*	TRANSMIT CLOCK FROM CPU
3	n/c	n/c
4	TXD	TRANSMIT DATA FROM CPU
5	RXD	RECEIVE DATA TO CPU
6	RTS*	REQUEST-TO-SEND FROM CPU
7	CTS*	CLEAR-TO-SEND TO CPU
8	DCD*	DATA CARRIER DETECT TO CPU
9	DTR*	DATA TERMINAL READY FROM CPU
10	n/c	n/c
11	BRCLK	BAUD RATE CLOCK FROM CPU
12	GND	GROUND
13	+16VDC	+16VDC
14	-16VDC	-16VDC
15	+5VDC	+5VDC
16	n/c	n/c

J2(TERMINAL)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	TXD HI	TRANSMIT DATA HIGH to terminal
2	RTS HI	REQUEST-TO-SEND HIGH to terminal
3	DTR HI	DATA TERMINAL READY to terminal
4	RXD HI	RECEIVE DATA HIGH from terminal
5	CTS HI	CLEAR-TO-SEND HIGH from terminal
6	SYNC HI	SYNC HIGH from terminal
7	DCD HI	DATA CARRIER DETECT HIGH from terminal
8	BAUDCLK HI	BAUD RATE CLOCK HIGH to terminal
9	TXC HI	TRANSMIT CLOCK HIGH from terminal
10	n/c	n/c
11	n/c	n/c
12	n/c	n/c
13	GND	GROUND
14	TXD LO	TRANSMIT DATA LOW to terminal
15	RTS LO	REQUEST-TO-SEND LOW to terminal
16	DTR LO	DATA TERMINAL READY LOW to terminal
17	RXD LO	RECEIVE DATA LOW from terminal
18	CTS LO	CLEAR-TO-SEND LOW from terminal
19	SYNC LO	SYNC LOW from terminal
20	DCD LO	DATA CARRIER DETECT LOW from terminal
21	BAUDCLK LO	BAUD RATE CLOCK LOW to terminal
22	TXC LO	TRANSMIT CLOCK LOW from terminal
23	n/c	n/c
24	n/c	n/c
25	GND	GROUND

CONNECTOR REQUIREMENTS

PERSONALITY BOARD CONNECTORS	MATING CONNECTORS
J1 - ANSLEY 609-1617	ANSLEY 609-1630 (ICM SUPPLIED)
J2 - CANNON DB25P-731	CANNON DB 25S-731 (CUSTOMER SUPPLIED)

SET UP INSTRUCTIONS

SIMPLE TERMINAL

To provide less interconnecting lines for terminal not requiring full handshake protocol, jumper PJ1 2-to-3 and PJ2 2-to-3. Provide twisted pair lines for TXD and RXD only.

FULL PROTOCOL

To provide for full handshaking, jumper PJ1 1-to-2 and PJ2 1-to-2. Provide twisted pair lines for the signals required.

SYNCHRONOUS TERMINAL

To use CPZ4800X Port A of the SIO, cut PJB B-C on the CPZ4800X.

To use CPS-MX Port A of the SIO, cut PJA B-C on the CPS-MX.

PERSONALITY BOARD - LONG DISTANCE SERIAL COMMUNICATIONS

PART NUMBER - LDS100

FUNCTION

The LDS100 personality board provides RS422 differential line drivers and receivers. These balanced drivers and receivers can provide serial communications for distances of up to 4000 feet at a communications rate of 100 kbits/second. This assumes that 24 AWG twisted pair cable is used. Drivers and receivers are provided to support full handshake protocols.

The LDS100 in combination with the RS422 Serial Communications Personality Board (FTT100), provides a means of connecting terminals, printers and other RS232 serial devices remotely located from the CPU mainframe. Jumper options are provided to minimize the number of cable lines required if no handshaking signals are required as in the case of simple RS232 Terminals where only transmit and receive signals are required. Ground is also provided but is not used in most cases.

AC power must be provided to the board. The board may be strapped for either 115VAC/60HZ or 230 VAC/50HZ operation.

INTERFACE REQUIREMENTS

J1 connects to RS422 Personality Board via long distance cable.
J2 connects to RS232 serial device with standard RS232 cable.

J1(RS422 INTERFACE)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	TXD HI	TRANSMIT DATA HIGH to terminal
2	RTS HI	REQUEST-TO-SEND HIGH to terminal
3	DTR HI	DATA TERMINAL READY to terminal
4	RXD HI	RECEIVE DATA HIGH from terminal
5	CTS HI	CLEAR-TO-SEND HIGH from terminal
6	SYNC HI	SYNC HIGH from terminal
7	DCD HI	DATA CARRIER DETECT HIGH from terminal
8	BAUDCLK HI	BAUD RATE CLOCK HIGH to terminal
9	TXC HI	TRANSMIT CLOCK HIGH from terminal
10	n/c	n/c
11	n/c	n/c
12	n/c	n/c
13	GND	GROUND
14	TXD LO	TRANSMIT DATA LOW to terminal
15	RTS LO	REQUEST-TO-SEND LOW to terminal
16	DTR LO	DATA TERMINAL READY LOW to terminal
17	RXD LO	RECEIVE DATA LOW from terminal
18	CTS LO	CLEAR-TO-SEND LOW from terminal
19	SYNC LO	SYNC LOW from terminal
20	DCD LO	DATA CARRIER DETECT LOW from terminal
21	BAUDCLK LO	BAUD RATE CLOCK LOW to terminal
22	TXC LO	TRANSMIT CLOCK LOW from terminal
23	n/c	n/c
24	n/c	n/c
25	GND	GROUND

J2(PERIPHERAL)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	SAFETY GND	SAFETY GROUND
2	TXD	TRANSMIT DATA TO PERIPHERAL
3	RXD	RECEIVE DATA FROM PERIPHERAL
4	RTS*	REQUEST-TO-SEND TO PERIPHERAL
5	CTS*	CLEAR-TO-SEND FROM PERIPHERAL
6	DSR*	DATA SET READY FROM PERIPHERAL
7	POWER GND	POWER GROUND
8	n/c	n/c
9	n/c	n/c
10	n/c	n/c
11	RESERVED	RESERVED FOR SPECIAL USE HANDSHAKE
12	n/c	n/c
13	n/c	n/c
14	n/c	n/c
15	TXCLK*	TRANSMIT CLOCK FROM PERIPHERAL
16	n/c	n/c
17	n/c	n/c
18	n/c	n/c
19	SRTS*	SECONDARY REQUEST-TO-SEND FROM PERIPHERAL
20	DTR*	DATA TERMINAL READY TO PERIPHERAL
21	n/c	n/c
22	n/c	n/c
23	n/c	n/c
24	BAUDCLK	BAUD CLOCK TO PERIPHERAL
25	n/c	n/c

CONNECTOR REQUIREMENTS

PERSONALITY BOARD CONNECTORS	MATING CONNECTORS
J1 - CANNON DB25S-731	CANNON DB25P-731 (CUSTOMER SUPPLIED)
J2 - CANNON DB25S-731	CANNON DB25P-731 (CUSTOMER SUPPLIED)

SET UP INSTRUCTIONS

(1)AC POWER SET-UP

The LDS100 may be configured to operate with 115VAC/60HZ or 230VAC/50HZ through jumper options. Use 18 or 16 AWG wire for jumpers in this setting.

To configure the LDS100 for 115VAC, solder two jumpers. One is soldered at JD 1-to-2 and the other is soldered at JD 3-to-4.

To configure the LDS100 for 230VAC, solder one jumper at JD 2-to-3.

AC power may now be installed. Connect AC HI and AC LO in the indicated solder pads. Connect SAFETY GROUND to the pad marked "CH".

(2)SAFETY GROUND CONNECTION

Solder a strap in jumper area JC if Safety Ground should be connected to Power Ground.

(3)SIMPLE TERMINAL(NO HANDSHAKING) SET-UP

Most terminals do not require handshaking for RS232/C communication. In this case, no jumpers are required in jumper areas JA and JB. Connect receive and transmit data lines only between the FTT100 and the LDS100 boards.

(4)TERMINAL/PRINTER(FULL HANDSHAKING)

Connect JA in accordance with the type of handshaking signal required to be transmited to the CLEAR-TO-SEND input of the CPU. The options are as follows:

JA	handshake signal
a1-to-b1	request-to-send(RTS)
a2-to-b2	manufacture defined
a3-to-b3	secondary request-to-send(SRTS)
a4-to-b4	data terminal ready(DTR)

Connect JB if DATA TERMINAL READY(DTR) is required to be connected to the DATA CARRIER DETECT(DCD) signal of the CPU. Connect all corresponding signal lines from FTT100 to the LDS100.

PERSONALITY BOARD - FLOPPY DISK CONTROLLER

PART NUMBER - FPB158-XY

FUNCTION

The FLOPPY DISK CONTROLLER personality board provides line drivers and receivers, terminators and logic to interface either an 8-inch or a 5 1/4-inch or both 8-inch and 5 1/4-inch floppy disk drives with the CPZ4800X SBCP. A DB25 connector is available as the means to interface with the drive interface; however, if other types of commonly used connectors are required, adapters are available to tailor the interface appropriately.

This module is used ONLY on the CPZ4800X SBCP. It is not to be used with the CPZ48000 SBCP.

```
**********
*        *
*  WARNING  *
*        *
**********
```

THE FPB158-XY BASE BOARD MUST NOT BE CONNECTED TO THE MODEL CPZ48000 SBCP AS DAMAGE MAY RESULT TO THE SBCP. NOTE HOWEVER THAT THE FPB100-11 OR THE FPB100-22 ADAPTERS MAY BE USED WITH THE FPB158-XY BASE BOARD. THE FPB158-30, AN ADAPTER WHICH ACCOMMODATES BOTH 5 1/4- INCH EDGE CARD AND 8-INCH HEADER CONNECTORS, IS TO BE USED ONLY WITH THE FPB158-XY BASE BOARD.

INTERFACE REQUIREMENTS

FPB158-XY

J1(CPU)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	n/c	n/c
2	DS1*	DRIVE SELECT #1 FROM CPU
3	n/c	n/c
4	DS2*	DRIVE SELECT #2 FROM CPU
5	GND	GROUND
6	DS3*	DRIVE SELECT #3 FROM CPU
7	GND	GROUND
8	DS4*	DRIVE SELECT #4 FROM CPU
9	GND	GROUND
10	DIRC	DIRECTION CONTROL FROM CPU
11	GND	GROUND
12	STEP	STEP CONTROL FROM CPU
13	GND	GROUND
14	WRITE DATA	WRITE DATA FROM CPU
15	GND	GROUND
16	WGATE	WRITE GATE FROM CPU
17	GND	GROUND
18	TRACK 0*	TRACK 0 STATUS TO CPU
19	GND	GROUND
20	WRITE PROT*	WRITE PROTECT TO CPU
21	GND	GROUND
22	READ DATA*	READ DATA TO CPU
23	GND	GROUND
24	SSO	SIDE SELECT OUTPUT FROM CPU
25	GND	GROUND
26	HLD	HEAD LOAD COMMAND FROM CPU
27	GND	GROUND
28	INDEX*	INDEX PULSE TO CPU
29	GND	GROUND
30	READY	READY STATUS TO CPU
31	GND	GROUND
32	MOTOR ON	MOTOR ON STATUS FROM CPU
33	GND	GROUND
34	TK43	TRACK 43 STATUS FROM CPU
35	GND	GROUND
36	5*/8	DRIVE SIZE SELECT
37	GND	GROUND
38	HLTIMER	HEAD LOAD TIMER
39	GND	GROUND
40	+5VDC	+5VDC

J2(MODIFIED DRIVE INTERFACE)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DS1*	DRIVE SELECT #1 to DRIVE interface
2	DS2*	DRIVE SELECT #2 to DRIVE interface
3	DS3*	DRIVE SELECT #3 to DRIVE interface
4	DS4*	DRIVE SELECT #4 to DRIVE interface
5	DIRC*	DIRECTION CONTROL to DRIVE interface
6	STEP*	STEP CONTROL to DRIVE interface
7	WRITE DATA*	WRITE DATA to DRIVE interface
8	WRITE GATE*	WRITE GATE to DRIVE interface
9	TRACK 0 *	TRACK 0 STATUS from DRIVE interface
10	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
11	READ DATA*	READ DATA to DRIVE inerface
12	SSO*	SIDE SELECT OUTPUT to DRIVE interface
13	HEAD LOAD*	HEAD LOAD COMMAND to DRIVE interface
14	INDEX*	INDEX PULSES from DRIVE interface
15	READY*	READY STATUS from DRIVE interface
16	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
17	TK43*	TRACK 43 STATUS to DRIVE interface
18	n/c	n/c
19	n/c	n/c
20	GND	GROUND
21	GND	GROUND
22	GND	GROUND
23	GND	GROUND
24	GND	GROUND
25	GND	GROUND

ADAPTER FPB100-11

Connects to FPB100 or FPB158 Personality Board.

J1(MODIFIED DRIVE INTERFACE)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DS1*	DRIVE SELECT #1 to DRIVE interface
2	DS2*	DRIVE SELECT #2 to DRIVE interface
3	DS3*	DRIVE SELECT #3 to DRIVE interface
4	DS4*	DRIVE SELECT #4 to DRIVE interface
5	DIRC*	DIRECTION CONTROL to DRIVE interface
6	STEP*	STEP CONTROL to DRIVE interface
7	WRITE DATA*	WRITE DATA to DRIVE interface
8	WRITE GATE*	WRITE GATE to DRIVE interface
9	TRACK 0 *	TRACK 0 STATUS from DRIVE interface
10	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
11	READ DATA*	READ DATA to DRIVE inerface
12	SSO*	SIDE SELECT OUTPUT to DRIVE interface
13	HEAD LOAD*	HEAD LOAD COMMAND to DRIVE interface
14	INDEX*	INDEX PULSES from DRIVE interface
15	READY*	READY STATUS from DRIVE interface
16	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
17	TK43*	TRACK 43 STATUS to DRIVE interface
18	GND	GROUND
19	GND	GROUND
20	GND	GROUND
21	GND	GROUND
22	GND	GROUND
23	GND	GROUND
24	GND	GROUND
25	GND	GROUND

ADAPTER FPB100-11

J2(8-INCH DRIVE INTERFACE)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	TK43*	TRACK 43 STATUS to DRIVE interface
3	GND	GROUND
4	n/c	n/c
5	GND	GROUND
6	n/c	n/c
7	GND	GND
8	n/c	n/c
9	GND	GROUND
10	n/c	n/c
11	GND	GROUND
12	n/c	n/c
13	GND	GROUND
14	SSO	SIDE SELECT OUTPUT to DRIVE interface
15	GND	GROUND
16	n/c	n/c
17	GND	GROUND
18	HEAD LOAD*	HEAD LOAD COMMAND to DRIVE interface
19	GND	GROUND
20	INDEX*	INDEX PULSES from DRIVE interface
21	GND	GROUND
22	READY*	READY STATUS from DRIVE interface
23	GND	GROUND
24	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
25	GND	GROUND
26	DS1*	DRIVE SELECT #1 to DRIVE interface
27	GND	GROUND
28	DS2*	DRIVE SELECT #2 to DRIVE interface
29	GND	GROUND
30	DS3*	DRIVE SELECT #3 to DRIVE interface
31	GND	GROUND
32	DS4*	DRIVE SELECT #4 to DRIVE interface
33	GND	GROUND
34	DIRC*	DIRECTION CONTROL to DRIVE interface
35	GND	GROUND
36	STEP*	STEP COMMAND to DRIVE interface
37	GND	GROUND
38	WRITE DATA*	WRITE DATA to DRIVE interface
39	GND	GROUND
40	WRITE GATE*	WRITE GATE to DRIVE interface

41	GND	GROUND
42	TRACK 0 *	TRACK ZERO STATUS from DRIVE interface
43	GND	GROUND
44	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
45	GND	GROUND
46	READ DATA*	READ DATA to DRIVE interface
47	GND	GROUND
48	n/c	n/c
49	GND	GROUND
50	n/c	n/c

ADAPTER FPB100-22

Connects to FPB100 or FPB158 Personality Board.

J1(MODIFIED DRIVE INTERFACE)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DS1*	DRIVE SELECT #1 to DRIVE interface
2	DS2*	DRIVE SELECT #2 to DRIVE interface
3	DS3*	DRIVE SELECT #3 to DRIVE interface
4	DS4*	DRIVE SELECT #4 to DRIVE interface
5	DIRC*	DIRECTION CONTROL to DRIVE interface
6	STEP*	STEP CONTROL to DRIVE interface
7	WRITE DATA*	WRITE DATA to DRIVE interface
8	WRITE GATE*	WRITE GATE to DRIVE interface
9	TRACK 0 *	TRACK 0 STATUS from DRIVE interface
10	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
11	READ DATA*	READ DATA to DRIVE inerface
12	SS0*	SIDE SELECT OUTPUT to DRIVE interface
13	HEAD LOAD*	HEAD LOAD COMMAND to DRIVE interface
14	INDEX*	INDEX PULSES from DRIVE interface
15	READY*	READY STATUS from DRIVE interface
16	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
17	TK43*	TRACK 43 STATUS to DRIVE interface
18	GND	GROUND
19	GND	GROUND
20	GND	GROUND
21	GND	GROUND
22	GND	GROUND
23	GND	GROUND
24	GND	GROUND
25	GND	GROUND

ADAPTER FPB100-22

J2(5 1/4-INCH DRIVE INTERFACE)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	n/c	n/c
3	GND	GROUND
4	n/c	n/c
5	GND	GROUND
6	DS4*	DRIVE SELECT #4 to DRIVE interface
7	GND	GROUND
8	INDEX*	INDEX* PULSE STATUS from DRIVE interface
9	GND	GROUND
10	DS1*	DRIVE SELECT #1 to DRIVE interface
11	GND	GROUND
12	DS2*	DRIVE SELECT #2 to DRIVE interface
13	GND	GROUND
14	DS3*	DRIVE SELECT #3 to DRIVE interface
15	GND	GROUND
16	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
17	GND	GROUND
18	DIRC*	DIRECTION CONTROL to DRIVE interface
19	GND	GROUND
20	STEP*	STEP COMMAND to DRIVE interface
21	GND	GROUND
22	WRITE DATA*	WRITE DATA to DRIVE interface
23	GND	GROUND
24	WRITE GATE*	WRITE GATE to DRIVE interface
25	GND	GROUND
26	TRACK 0 *	TRACK ZERO STATUS from DRIVE interface
27	GND	GROUND
28	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
29	GND	GROUND
30	READ DATA*	READ DATA to DRIVE interface
31	GND	GROUND
32	SSO*	SIDE SELECT OUTPUT to DRIVE interface
33	GND	GROUND
34	n/c	n/c

ADAPTER FPB158-30

Connects to FPB158 Personality Board.

J1(MODIFIED DRIVE INTERFACE)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DS1*	DRIVE SELECT #1 to DRIVE interface
2	DS2*	DRIVE SELECT #2 to DRIVE interface
3	DS3*	DRIVE SELECT #3 to DRIVE interface
4	DS4*	DRIVE SELECT #4 to DRIVE interface
5	DIRC*	DIRECTION CONTROL to DRIVE interface
6	STEP*	STEP CONTROL to DRIVE interface
7	WRITE DATA*	WRITE DATA to DRIVE interface
8	WRITE GATE*	WRITE GATE to DRIVE interface
9	TRACK 0 *	TRACK 0 STATUS from DRIVE interface
10	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
11	READ DATA*	READ DATA to DRIVE inerface
12	SS0*	SIDE SELECT OUTPUT to DRIVE interface
13	HEAD LOAD*	HEAD LOAD COMMAND to DRIVE interface
14	INDEX*	INDEX PULSES from DRIVE interface
15	READY*	READY STATUS from DRIVE interface
16	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
17	TK43*	TRACK 43 STATUS to DRIVE interface
18	n/c	n/c
19	n/c	n/c
20	GND	GROUND
21	GND	GROUND
22	GND	GROUND
23	GND	GROUND
24	GND	GROUND
25	GND	GROUND

ADAPTER FPB158-30

J2(8-INCH DRIVE INTERFACE)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	TK43*	TRACK 43 STATUS to DRIVE interface
3	GND	GROUND
4	n/c	n/c
5	GND	GROUND
6	n/c	n/c
7	GND	GND
8	n/c	n/c
9	GND	GROUND
10	n/c	n/c
11	GND	GROUND
12	n/c	n/c
13	GND	GROUND
14	SS0	SIDE SELECT OUTPUT to DRIVE interface
15	GND	GROUND
16	n/c	n/c
17	GND	GROUND
18	HEAD LOAD*	HEAD LOAD COMMAND to DRIVE interface
19	GND	GROUND
20	INDEX*	INDEX PULSES from DRIVE interface
21	GND	GROUND
22	READY*	READY STATUS from DRIVE interface
23	GND	GROUND
24	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
25	GND	GROUND
26	DS1*	DRIVE SELECT #1 to DRIVE interface
27	GND	GROUND
28	DS2*	DRIVE SELECT #2 to DRIVE interface
29	GND	GROUND
30	DS3*	DRIVE SELECT #3 to DRIVE interface
31	GND	GROUND
32	DS4*	DRIVE SELECT #4 to DRIVE interface
33	GND	GROUND
34	DIRC*	DIRECTION CONTROL to DRIVE interface
35	GND	GROUND
36	STEP*	STEP COMMAND to DRIVE interface
37	GND	GROUND
38	WRITE DATA*	WRITE DATA to DRIVE interface
39	GND	GROUND
40	WRITE GATE*	WRITE GATE to DRIVE interface

41	GND	GROUND
42	TRACK 0 *	TRACK ZERO STATUS from DRIVE interface
43	GND	GROUND
44	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
45	GND	GROUND
46	READ DATA*	READ DATA to DRIVE interface
47	GND	GROUND
48	n/c	n/c
49	GND	GROUND
50	n/c	n/c

ADAPTER FPB158-30

J3(5 1/4-INCH DRIVE INTERFACE)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	n/c	n/c
3	GND	GROUND
4	n/c	n/c
5	GND	GROUND
6	DS4*	DRIVE SELECT #4 to DRIVE interface
7	GND	GROUND
8	INDEX*	INDEX* PULSE STATUS from DRIVE interface
9	GND	GROUND
10	DS1*	DRIVE SELECT #1 to DRIVE interface
11	GND	GROUND
12	DS2*	DRIVE SELECT #2 to DRIVE interface
13	GND	GROUND
14	DS3*	DRIVE SELECT #3 to DRIVE interface
15	GND	GROUND
16	MOTOR ON*	MOTOR ON COMMAND to DRIVE interface
17	GND	GROUND
18	DIRC*	DIRECTION CONTROL to DRIVE interface
19	GND	GROUND
20	STEP*	STEP COMMAND to DRIVE interface
21	GND	GROUND
22	WRITE DATA*	WRITE DATA to DRIVE interface
23	GND	GROUND
24	WRITE GATE*	WRITE GATE to DRIVE interface
25	GND	GROUND
26	TRACK 0 *	TRACK ZERO STATUS from DRIVE interface
27	GND	GROUND
28	WRITE PROT*	WRITE PROTECT STATUS from DRIVE interface
29	GND	GROUND
30	READ DATA*	READ DATA to DRIVE interface
31	GND	GROUND
32	SSO*	SIDE SELECT OUTPUT to DRIVE interface
33	GND	GROUND
34	n/c	n/c

CONNECTOR REQUIREMENTS

Use the following table to determine the type of mating connector to use:

CONFIGURATION	PART NUMBER	CONNECTOR TYPE
8-INCH OR 5 1/4-INCH W/O ADAPTER	FPB158	CANNON DB23S-731
8-INCH/HEADER PLUG ADAPTER	FPB100-11	ANSLEY 609-5017
5 1/4-INCH/EDGE CONNECTOR ADAPTER	FPB100-22	AMP 840-225F-A34-1
8 OR 5 1/4-INCH ADAPTER	FPB158-30	ANSLEY 609-5017 & AMP 840-225F-A34-1

FPB158	MATING CONNECTORS
J1 - ANSLEY 609-4017	ANSLEY 609-4030 (ICM SUPPLIED)
J2 - CANNON DB25S-731	CANNON DB25P-731 (*see note below)

FPB100-11	MATING CONNECTORS
J1 - CANNON DB25P-731	CANNON DB25S-731 (ICM SUPPLIED)
J2 - ANSLEY 609-5017	ANSLEY 609-5030 (CUSTOMER SUPPLIED)

FPB100-22	MATING CONNECTORS
J1 - CANNON DB25P-731	CANNON DB25S-731 (ICM SUPPLIED)
J2 - (34 PIN EDGE)	AMP 840-225F-A34-1(CUSTOMER SUPPLIED)

FPB158-30	MATING CONNECTORS
J1 - CANNON DB25P-731	CANNON DB25S-731 (ICM SUPPLIED)
J2 - (34 PIN EDGE)	AMP 840-225F-A34-1(CUSTOMER SUPPLIED)
J3 - ANSLEY 609-5017	ANSLEY 609-5030 (CUSTOMER SUPPLIED)

* Customer supplied if connecting directly to FPB158. ICM supplied if using FPB100-XY or FPB158-XY Adapters.

SET UP INSTRUCTIONS

None Required.

PERSONALITY BOARD - CENTRONICS PRINTER

PART NUMBER - CPI100

FUNCTION

The Centronics Printer Personality Board provides line drivers, receivers, terminators, jumper options and data strobe generator logic to interface to any printer compatible with the Centronics parallel interface.

This module may be used with either the CPZ4800X SBCP or the CPS-MX SBSP.

INTERFACE REQUIREMENTS

Connects to J4 of CPZ4800X SBCP or CPS-MX SBSP.

J1(CPU)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	RDYA	READY handshake from CPU, Channel A
2	STBA	STROBE handshake to CPU, Channel A
3	n/c	n/c
4	n/c	n/c
5	D0A	DATA BIT 0, Channel A
6	D1A	DATA BIT 1, Channel A
7	D2A	DATA BIT 2, Channel A
8	D3A	DATA BIT 3, Channel A
9	D4A	DATA BIT 4, Channel A
10	D5A	DATA BIT 5, Channel A
11	D6A	DATA BIT 6, Channel A
12	D7A	DATA BIT 7, Channel A
13	D0B	DATA BIT 0, Channel B
14	D1B	DATA BIT 1, Channel B
15	D2B	DATA BIT 2, Channel B
16	D3B	DATA BIT 3, Channel B
17	D4B	DATA BIT 4, Channel B
18	D5B	DATA BIT 5, Channel B
19	D6B	DATA BIT 6, Channel B
20	D7B	DATA BIT 7, Channel B
21	RESET*	RESET from CPU (active low)
22	GND	GROUND
23	n/c	n/c
24	GND	GROUND
25	PCLK	4 MHZ Auxilliary Clock from CPU
26	+5VDC	+5VDC

J2(PRINTER)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DSTR*	DATA STROBE to the Printer
2	DB1	DATA BIT 1 to the Printer
3	DB2	DATA BIT 2 to the Printer
4	DB3	DATA BIT 3 to the Printer
5	DB4	DATA BIT 4 to the Printer
6	DB5	DATA BIT 5 to the Printer
7	DB6	DATA BIT 6 to the Printer
8	DB7	DATA BIT 7 to the Printer
9	DB8	DATA BIT 8 to the Printer
10	ACK*	ACKNOWLEDGE from the Printer
11	BUSY	BUSY Status from the Printer
12	PE	PAPER EMPTY Status from the Printer
13	SELECT	SELECT Status from the Printer
14	n/c	n/c
15	n/c	n/c
16	n/c	n/c
17	CHASSIS GND	Printer Chassis Ground
18	n/c	n/c
19	SIG GND	SIGNAL GROUND
20	SIG GND	SIGNAL GROUND
21	SIG GND	SIGNAL GROUND
23	SIG GND	SIGNAL GROUND
24	FAULT*	FAULT Status from the Printer
25	INPUT PRIME*	RESET to the Printer

CONNECTOR REQUIREMENTS

CPI100	MATING CONNECTORS
J1 - ANSLEY 609-2617	ANSLEY 609-2630 (ICM SUPPLIED)
J2 - CANNON DB25S-731	CANNON DB25P-731 (* see note below)

*NOTE: Customer is to supply cabling from the CPI100 to the Centronics compatible printer. If a flat ribbon cable is desired, one can be provided by using a flat ribbon type DB25 connector at one end and a Centronics type connector (AMP 57-10360 or equivalent) at the other end. In this case, all pins are to be connected at the DB25 end except for pins 24 and 25. The software normally does not use the FAULT status and most printers have a power-up reset circuit and do not need subsequent reset operations; therefore, pins 24 and 25 are not required and a flat ribbon cable will be usable. If all signals are required, the customer must use a descrete wire harness to connect all signals.

SET UP INSTRUCTIONS

If signal ground is to be connected to chassis ground, solder a jumper in jumper area PJA.

If the CPU is to provide reset signals to the printer, solder a jumper in jumper area PJB.

PERSONALITY BOARD - PRIAM INTELLIGENT HARD DISK

PART NUMBER - PRI100

FUNCTION

PRIAM provides two intelligent hard disk interface controllers referred to as the "SMART" and the "SMART-E". These are preprogrammed microprocessor based controllers. They may be used for the entire line of PRIAM Winchester disc drives which range in capacity from 10 megabytes to 157 megabytes and come in eight or fourteen inch packaging. Up to four drives in any combination of drive sizes may be interconnected. The controllers support a variety of read sector, write sector and format commands. Data transfers may be either programmed I/O or DMA. The SMART-E has all the features that the SMART has in addition to error detection & correction, logical sector addressing, sector interleaving, parity generation & testing, direct data transfers and a 2 Kbyte data buffer (SMART has a 1 Kbyte buffer). The interface performs the entire function of detailed disc control while presenting to the host a basic and cost effective interface.

The PRI100 Personality Board connects the parallel port of the CPZ4800X SBCP or the CPS-MX SBSP to the SMART or SMART-E controllers. Thus, a very powerful disc subsystem may be directly connected to the ICM line of processors via the PRI100.

A jumper option is provided on the PRI100 to configure it for either the SMART or the SMART-E controller. The controllers mount along the drive sides alleviating the need for additional S-100 Bus slots. An adapter, PRI100-1, is provided allowing direct connection of the PRI100 to the smart controllers.

INTERFACE REQUIREMENTS

Connects to J4 of either the CPZ4800X SBCP or the CPS-MX SBSP.

J1(CPU)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	RDYA	READY handshake from CPU, Channel A
2	STBA*	STROBE handshake to CPU, Channel A
3	n/c	n/c
4	n/c	n/c
5	D0A	DATA BIT 0, Channel A
6	D1A	DATA BIT 1, Channel A
7	D2A	DATA BIT 2, Channel A
8	D3A	DATA BIT 3, Channel A
9	D4A	DATA BIT 4, Channel A
10	D5A	DATA BIT 5, Channel A
11	D6A	DATA BIT 6, Channel A
12	D7A	DATA BIT 7, Channel A
13	D0B	DATA BIT 0, Channel B
14	D1B	DATA BIT 1, Channel B
15	D2B	DATA BIT 2, Channel B
16	D3B	DATA BIT 3, Channel B
17	D4B	DATA BIT 4, Channel B
18	D5B	DATA BIT 5, Channel B
19	D6B	DATA BIT 6, Channel B
20	D7B	DATA BIT 7, Channel B
21	RESET*	RESET from CPU (active low)
22	GND	GROUND
23	PINT*	PORT INTERRUPT (active low)
24	GND	GROUND
25	n/c	n/c
26	+5VDC	+5VDC

J2(MODIFIED PRIAM)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	HCBUS0	HOST DATA BUS 0
3	HCBUS1	HOST DATA BUS 1
4	HCBUS2	HOST DATA BUS 2
5	HCBUS3	HOST DATA BUS 3
6	HCBUS4	HOST DATA BUS 4
7	HCBUS5	HOST DATA BUS 5
8	HCBUS6	HOST DATA BUS 6
9	HCBUS7	HOST DATA BUS 7
10	GND	GROUND
11	HRD*	ENABLE REGISTER TO HOST-BUS
12	GND	GROUND
13	HWR*	ENABLE HOST-BUS TO REGISTER
14	GND	GROUND
15	HAD2	HOST ADDRESS BUS 2
16	HAD1	HOST ADDRESS BUS 1
17	HAD0	HOST ADDRESS BUS 0
18	GND	GROUND
19	RESET*	RESET TO CONTROLLER
20	GND	GROUND
21	HIR*	HOST INTERRUPT
22	DTREQ*	DATA TRANSFER REQUEST TO HOST
23	HREAD*	DATA DIRECTION CONTROL TO CONTROLLER
24	DBUSENA*	CONTROLLER-READY TO HOST
25	BUSREQ*	DATA TRANSFER REQUEST TO HOST (SMART-E ONLY)

ADAPTER PRI100-1

J1(MODIFIED PRIAM)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	HCBUS0	HOST DATA BUS 0
3	HCBUS1	HOST DATA BUS 1
4	HCBUS2	HOST DATA BUS 2
5	HCBUS3	HOST DATA BUS 3
6	HCBUS4	HOST DATA BUS 4
7	HCBUS5	HOST DATA BUS 5
8	HCBUS6	HOST DATA BUS 6
9	HCBUS7	HOST DATA BUS 7
10	GND	GROUND
11	HRD*	ENABLE REGISTER TO HOST-BUS
12	GND	GROUND
13	HWR*	ENABLE HOST-BUS TO REGISTER
14	GND	GROUND
15	HAD2	HOST ADDRESS BUS 2
16	HAD1	HOST ADDRESS BUS 1
17	HAD0	HOST ADDRESS BUS 0
18	GND	GROUND
19	RESET*	RESET TO CONTROLLER
20	GND	GROUND
21	HIR*	HOST INTERRUPT
22	DTREQ*	DATA TRANSFER REQUEST TO HOST
23	HREAD*	DATA DIRECTION CONTROL TO CONTROLLER
24	DBUSENA*	CONTROLLER-READY TO HOST
25	BUSREQ*	DATA TRANSFER REQUEST TO HOST (SMART-E ONLY)

ADAPTER PRI100-1

J2(PRIAM)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	HCBUS0	HOST DATA BUS 0
3	HCBUS1	HOST DATA BUS 1
4	HCBUS2	HOST DATA BUS 2
5	HCBUS3	HOST DATA BUS 3
6	HCBUS4	HOST DATA BUS 4
7	HCBUS5	HOST DATA BUS 5
8	HCBUS6	HOST DATA BUS 6
9	HCBUS7	HOST DATA BUS 7
10	GND	GROUND
11	HRD*	ENABLE REGISTER TO HOST-BUS
12	GND	GROUND
13	HWR*	ENABLE HOST-BUS TO REGISTER
14	GND	GROUND
15	HAD2	HOST ADDRESS BUS 2
16	HAD1	HOST ADDRESS BUS 1
17	HAD0	HOST ADDRESS BUS 0
18	GND	GROUND
19	RESET*	RESET TO CONTROLLER
20	GND	GROUND
21	HIR*	HOST INTERRUPT
22	GND	GROUND
23	HREAD	DATA DIRECTION CONTROL TO CONTROLLER
24	DBUSENA*	CONTROLLER-READY TO HOST
25	GND	GROUND
26	DTREQ*	DATA TRANSFER REQUEST TO HOST
27	GND	GROUND
28	BUSREQ*	DATA TRANSFER REQUEST TO HOST (SMART-E ONLY)
29	GND	GROUND
30	HCBUS8	HOST DATA BUS PARITY (SMART-E ONLY)
31	GND	GROUND
32	RES	RESERVED
33	RES	RESERVED
34	RES	RESERVED
35	RES	RESERVED
36	RES	RESERVED
37	RES	RESERVED
38	RES	RESERVED
39	RES	RESERVED
40	RES	RESERVED

CONNECTOR REQUIREMENTS

PRI100	MATING CONNECTORS
J1 - ANSLEY 609-2617	ANSLEY 609-2630 (ICM SUPPLIED)
J2 - CANNON DB25S-731	CANNON DB25P-731 (* see note below)

PRI100-1	MATING CONNECTORS
J1 - CANNON DB25P-731	CANNON DB25S-731 (ICM SUPPLIED)
J2 - ANSLEY 609-4017	ANSLEY 609-4030 (CUSTOMER SUPPLIED)

* Customer supplied if connecting directly to PRI100. ICM supplied if using PRI100-1 Adapter.

SET-UP INSTRUCTIONS

To configure the PRI100 for the SMART controller, solder a jumper on JA from B-to-C.

To configure the PRI100 for the SMART-E controller, solder a jumper on JA from A-to-B.

PERSONALITY BOARD - SHUGART ASSOCIATES SYSTEM INTERFACE

PART NUMBER - SAS100

FUNCTION

The Shugart Associates System Interface(SASI) defines a Local I/O Bus which can be operated at data rates up to 1.5 megabytes per second. This bus provides I/O device independence so that disk drives, tape drives, printers and various other peripherals may be interfaced on the same I/O bus without modification to the host CPU's hardware or software. The interface protocol provides for connection of multiple initiators (devices capable of initiating an operation) and multiple targets(devices capable of responding to requests for operations). Arbitration logic is built in and a priority system awards control to the device that wins arbitration.

The SAS100 personality board converts the parallel port of either the CPZ4800X SBCP or the CPS-MX SBSP to a SASI I/O bus. Software is provided to emit bus timing in conformance with the SASI specification. The system integrator may interface SASI controllers such as the Data Technology Corporation's, Zebec and Sysgen line of controllers. Each have powerful attributes such as connecting hard disks with floppies, hard disks with tape streamers and connecting to high performance SMD type hard disks.

The SAS100 personality board is accompanied by an adapter board (SAS100-1). This adapter board converts the SAS100 DB25 connector interface to a 50 pin header connector interface with a pin assignment in exact conformance with the SASI Bus specification. The integrator may connect directly to the SAS100 with a DB25-to-SASI Interface cable or may connect via the SAS100-1 with a 50 pin flat ribbon cable.

INTERFACE REQUIREMENTS

Connects to J4 of either the CPZ4800X SBCP or the CPS-MX SBSP.

J1(CPU)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	RDYA	READY handshake from CPU, Channel A
2	STBA*	STROBE handshake to CPU, Channel A
3	RDYB	READY handshake from CPU, Channel B
4	STBB*	STROBE handshake to CPU, Channel B
5	D0A	DATA BIT 0, Channel A
6	D1A	DATA BIT 1, Channel A
7	D2A	DATA BIT 2, Channel A
8	D3A	DATA BIT 3, Channel A
9	D4A	DATA BIT 4, Channel A
10	D5A	DATA BIT 5, Channel A
11	D6A	DATA BIT 6, Channel A
12	D7A	DATA BIT 7, Channel A
13	D0B	DATA BIT 0, Channel B
14	D1B	DATA BIT 1, Channel B
15	D2B	DATA BIT 2, Channel B
16	D3B	DATA BIT 3, Channel B
17	D4B	DATA BIT 4, Channel B
18	D5B	DATA BIT 5, Channel B
19	DB6	DATA BIT 6, Channel B
20	D7B	DATA BIT 7, Channel B
21	n/c	n/c
22	GND	GROUND
23	PINT*	PORT INTERRUPT (active low)
24	GND	GROUND
25	n/c	n/c
26	+5VDC	+5VDC

J2(MODIFIED SASI)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	DO	DATA BIT 0
2	D2	DATA BIT 2
3	D4	DATA BIT 4
4	D6	DATA BIT 6
5	GND	GROUND
6	BSY*	BUSY
7	ACK*	ACKNOWLEDGE
8	RST*	RESET
9	MSG*	MESSAGE
10	SEL*	SELECT
11	C/D*	CONTROL/DATA
12	REQ*	REQUEST
13	I/O*	INPUT/OUTPUT
14	D1	DATA BIT 1
15	D3	DATA BIT 3
16	D4	DATA BIT 5
17	D7	DATA BIT 7
18	GND	GROUND
19	GND	GROUND
20	GND	GROUND
21	GND	GROUND
22	GND	GROUND
23	GND	GROUND
24	GND	GROUND
25	GND	GROUND

APAPTER SAS100-1

Connects to J2 of the SAS100 Personality Board.

J1(MODIFIED SASI)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	D0	DATA BIT 0
2	D2	DATA BIT 2
3	D4	DATA BIT 4
4	D6	DATA BIT 6
5	GND	GROUND
6	BSY*	BUSY
7	ACK*	ACKNOWLEDGE
8	RST*	RESET
9	MSG*	MESSAGE
10	SEL*	SELECT
11	C/D*	CONTROL/DATA
12	REQ*	REQUEST
13	I/O*	INPUT/OUTPUT
14	D1	DATA BIT 1
15	D3	DATA BIT 3
16	D4	DATA BIT 5
17	D7	DATA BIT 7
18	GND	GROUND
19	GND	GROUND
20	GND	GROUND
21	GND	GROUND
22	GND	GROUND
23	GND	GROUND
24	GND	GROUND
25	GND	GROUND

ADAPTER SAS100-1

J2(SASI)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	GND	GROUND
2	DB0	DATA BIT 0
3	GND	GROUND
4	DB1	DATA BIT 1
5	GND	GROUND
6	DB2	DATA BIT 2
7	GND	GROUND
8	DB3	DATA BIT 3
9	GND	GROUND
10	DB4	DATA BIT 4
11	GND	GROUND
12	DB5	DATA BIT 5
13	GND	GROUND
14	DB6	DATA BIT 6
15	GND	GROUND
16	DB7	DATA BIT 7
17	GND	GROUND
18	n/u	n/u
19	GND	GROUND
20	n/u	n/u
21	GND	GROUND
22	n/u	n/u
23	GND	GROUND
24	n/u	n/u
25	GND	GROUND
26	n/u	n/u
27	GND	GROUND
28	n/u	n/u
29	GND	GROUND
30	n/u	n/u
31	GND	GROUND
32	n/u	n/u
33	GND	GROUND
34	n/u	n/u
35	GND	GROUND
36	BSY*	BUSY
37	GND	GROUND
38	ACK*	ACKNOWLEDGE
39	GND	GROUND

40	RST*	RESET
41	GND	GROUND
42	MSG*	MESSAGE
43	GND	GROUND
44	SEL*	SELECT
45	GND	GROUND
46	C/D*	CONTROL/DATA
47	GND	GROUND
48	REQ*	REQUEST
49	GND	GROUND
50	I/O*	INPUT/OUTPUT

CONNECTOR REQUIREMENTS

SAS100	MATING CONNECTORS
J1 - ANSLEY 609-2617	ANSLEY 609-2630 (ICM SUPPLIED)
J2 - CANNON DB25S-731	CANNON DB25P-731 (*see note below)

SAS100-1	MATING CONNECTORS
J1 - CANNON DB25P-731	CANNON DB25S-731 (ICM SUPPLIED)
J2 - ANSLEY 609-5017	ANSLEY 609-5030 (CUSTOMER SUPPLIED)

* Customer supplied if connecting directly to SAS100. ICM supplied if using SAS100-1 Adapter.

SET-UP INSTRUCTIONS

(none required)

PERSONALITY BOARD - CLOCK/CALENDAR

PART NUMBER - CCB100

FUNCTION

The CCB100 provides a highly accurate real time clock which may be set by the CPZ4800X SBCP or the CPS-MX SBSP under software control. The time of year, month, day, hour, minute and second is maintained and may be read back by the CPU. A Ni-Cad battery is used to provide backup power to the time control chip. In this manner the real time clock is continously maintained even during extensive down time. This feature is quite useful for point-of-sale systems, inventory systems and other applications where continous clock monitoring is required. This board is also very useful in operating systems which feature date and time stamping such as TurboDOS. In a TurboDOS based system, this board may be connected to the master (CPZ4800X) parallel port or may be connected to any one slave (CPS-MX) parallel port.

INTERFACE REQUIREMENTS

Connects to J4 of the CPZ4800X SBCP or the CPS-MX SBSP. No other interface cable is required.

CPU (J1)

PIN NO.	SIGNAL NAME	DESCRIPTION
1	n/c	n/c
2	GND	GROUND
3	n/c	n/c
4	n/c	n/c
5	D0A	DATA BIT 0, Channel A
6	D1A	DATA BIT 1, Channel A
7	D2A	DATA BIT 2, Channel A
8	D3A	DATA BIT 3, Channel A
9	GND	GROUND
10	GND	GROUND
11	GND	GROUND
12	GND	GROUND
13	D0B	DATA BIT 0, Channel B
14	D1B	DATA BIT 1, Channel B
15	D2B	DATA BIT 2, Channel B
16	D3B	DATA BIT 3, Channel B
17	D4B	DATA BIT 4, Channel B
18	D5B	DATA BIT 5, Channel B
19	D6B	DATA BIT 6, Channel B
20	D7B	DATA BIT 7, Channel B
21	n/c	n/c
22	GND	GROUND
23	n/c	n/c
24	GND	GROUND
25	n/c	n/c
26	+5VDC	+5VDC

CONNECTOR REQUIREMENTS

J1(CPU) - Ansley 609-2617 or equivalent

SETUP INSTRUCTIONS

No hardware setup instructions are required, software instructions follow.

The CCB-100 can be used under CP/M by attaching the personality board to the parallel port of the CPZ-4800X and using the CLKSETM program to set the time and DSPCLKM to display the time.

Under the TurboDOS operating system the CCB-100 clock module can be placed on the CPZ-4800X master or any CPS-MX slave processor.

If the CCB is on the CPZ-4800X the user can set the time by using the program CLKSETM. The time can be displayed by executing the program DSPCLKM. The CCB can automatically be read as system date and time when the module MSTRCLK is included in the sys file that is loaded into the CPZ-4800X.

If the CCB is on the CPS-MX slave processor the user can set the time by using the program CLKSETS. The time can be displayed by executing the program DSPCLKS. The CCB can automatically be read as system date and time when the program SLVCLK.AUT is executed as a TurboDOS cold start program. There is no problem executing the program if the card is not attached, since it will simply return to the operating system.

CRT TERMINAL SET-UP INSTRUCTIONS

Firmware in the CPZ4800X is structured to communicate with RS232 terminals and with the terminals set-up in a particular fashion. The terminals must be set-up as described below otherwise booting-up the CPZ4800X will not be possible. The description given is for CP/M configurations only. Refer to the " TurboDOS Users Guide" manual for instructions on setting-up terminals for TurboDOS based systems:

number of stop bits = 2
number of data bits = 8
parity bit = not used

When the CPZ4800X is shipped configured for CP/M, a PROM monitor is installed which stores firmware to examine the baud rate of the terminal. The user must strike the "return" key function until the CPZ4800X adjusts itself to the rate set-up on the terminal. The baud rates which may be set-up on the terminal are listed below:

Baud Rate
300
600
1200
2400
4800
9600
19200
38400
76800

HARD DISK COMPATABILITY GUIDE

Two general methods exist for integrating hard disk drives with the CPZ4800X. The system integrator may install hard disk drives through the parallel port using personality boards which interface to various intelligent hard disk controllers. The other option is to install an IEEE hard disk controller in the S100 Bus. Each are discussed below:

PARALLEL PORT INTERFACE

The following personality boards are available:

-PRIAM INTELLIGENT HARD DISK PERSONALITY BOARD [PRI100]

Compatible with "SMART" or "SMART-E" Priam Intelligent Hard Disk controller. These controllers interface any PRIAM drive ranging in capacity from 10 to 157 megabytes and in 8 or 14 inch packaging.

-SHUGART ASSOCIATES SYSTEMS INTERFACE (SASI) PERSONALITY BOARD [SAS100]

Compatible with boards from the following manufactures:

-XEBEC Systems, Inc.
-Data Technology, Corp.
-Sysgen, Inc.

Any SASI compatible controller should interface with the SAS100. Some boards provide features others don't. For example, a XEBEC board allows SMD removable hard disk drives whereas the Sysgen controller interfaces ST506 drives on the same bus astape streaming drives.

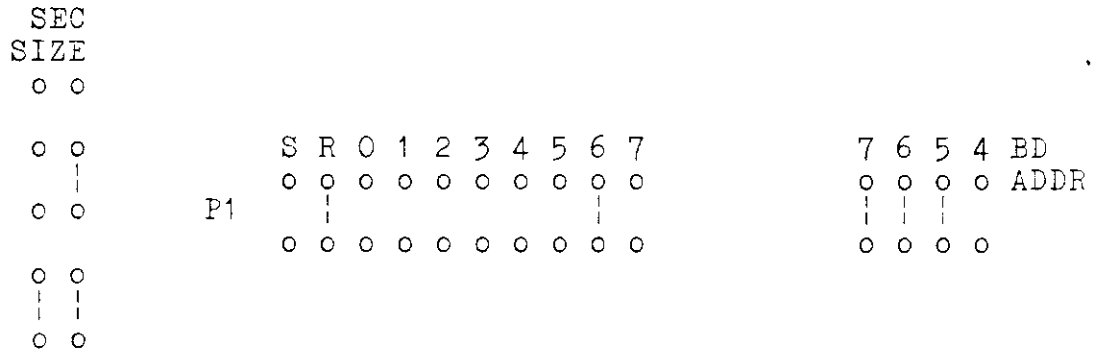
S100 BUS

Any hard disk controller which is IEEE 696.D2 compatible may be integrated with the CPZ4800X. CP/M and TurboDOS drivers are available for the MONITOR DYNAMICS, INC. hard disk controller. TurboDOS drivers are also available for the ADES GYPSY hard disk/tape backup controller and the KONAN SMC200 Removable Cartridge hard disk drive controller. In any case, the only condition imposed is that the controller be compatible with the IEEE specification.

Much experience has been gained in the field with the MONITOR DYNAMICS hard disk controller and has received wide acceptance. Benchmarks have proven this controller to be the fastest in its catagory. To assist in the integration of this controller, the following instructions are given:

The CPZ-4800X communicates with the Monitor Dymnamics Modules 1010, 1012 , 1016 or 1013 using I/O port 10 hex and interrupt vector 6 on the S-100 bus. The CPZ-4800X must be configured to detect interupt vector 6 (see JUMPER OPTIONS-JF section). To enable the Monitor Dynamics controller to communicate and issue interrupts, place jumpers as follows:

MONITOR DYNAMICS MD1010 & MD1013 JUMPER OPTIONS



The Monitor Dynamics 1013 controller uses the program TESTMD1.COM to format, verify and set the disk paramater block for the hard disk drive being used. The model 1013 is being directly sold and supported by I.C.M. and will control the following 5 1/4" drives:

Manafacture	Model
Atasi	3020/3033/3046
Rodime	R201/202/203/204
Tandon	TM602/TM603/TM502/TM503
Quantum	Q2020/30/40/80 (8 inch)
Ampex Corp.	PYXIS 7/13/20/27
Seagate Technology	ST506/406/412/418
CDC	9415-5 (WREN)
Micropolis	1303/1303/1304
Evotek	ET-5510/ET-5520/ET-5530/EY-5540
Vertex	V130/V150/V170
Shugart Associates	SA1002/1004 (8 Inch)
Shugart Associates	SA602/604/606
Computer Memories	CM5206/5412/5619
Rotating Memories	RM504/509/513/518
Memorex/Fujitsu	MRX101/102 (8 inch)
Memorex/Fujitsu	MRX306/310/512/513/514
Olivetti	HD561/1,/2,/3
IMI	5006H/5012H/5018H
Miniscribe Corp.	II (2006), III (3006,3012) IV (2012)

For other controller models or Hard disk drives please feel free to contact Richard Turner or Gary Clinard at Monitor Dynamics Inc., 1121 West 9th Street, Upland CA (714)985-7214.

**** SOFTWARE SECTION ***

This section of the manual describes the Software Interface for the CPZ-4800X.

PROM Monitor

76800,38400,19200,9600,4800,2400,1200,600,300 baud.

Below is a description of the built-in Monitor commands using CP/M Prom V2.1 and their functions. Commands may be either a single letter, single letter followed by 1, 2 or 3 parameters, or double letter commands followed by 1, 2 or 3 parameters and depends upon the function desired.

Basic PROM Commands

*** Note: *** <cr> = carriage return
---------- all entries are in hex.

---- Register definitions ----
A=accumulator, F=flags, B=register B, C=register C
D=register D, E=register E, H=register HL
X=register IX, Y=register IY, P=program counter
I=interrupt register, N=interrupt flip-flop

Letter	Function	Description
A	not used	
B<cr>	Boot disk drive A:	Load operating system on drive A: (CP/M disk)
Cxxxx,yyyy,zzzz<cr>	Compare memory	Will compare the block of memory starting with xxxx to yyyy with zzzz.
DMxxxx,yyyy>cr>	Dump Memory	Will display memory from xxxx to yyyy hex.
DMxxxx,S100<cr>		Will dump memory starting at xxxx with a swath of 100.
DR<cr>	Display Registers	Will display all Z-80 CPU registers.
E	not used	

Fxxxx,yyyy,zz<cr>	Fill memory	Will fill memory starting at xxxx to yyyy with the hex byte zz.
G<cr>	Go command	Will execute the program pointed to by the breakpoint PC value without trace or breakpoint active.
Gxxxx<cr>	Go at address	Will set the Program counter to address xxxx and begin execution there.
Gxxxx/yyyy<cr>	Go with Breakpoint	Begin execution at address xxxx with a breakpoint at address yyyy.
G/yyyy<cr>	Go with Breakpoint	Use present Program counter value to execute until address yyyy is reached.
Hxxxx,yyyy<cr>	Hex Math	Display the hex SUM and Difference of xxxx and yyyy
I	not used	
J	not used	
K	not used	
L	not used	
Mxxxx,yyyy,zzzz<cr>	Move memory	Will move the memory contents xxxx to yyyy stating at zzzz.
N	not used	
Oxx,yy<cr>	Output to port	Will output the byte xx to port yy hex.
P	not used	
Qxx<cr>	Query input port	Will display the hex and binary contents of port xx hex.
R<cr>	Read disk	Will read the diskette in drive A:, track 0 sector 1 starting location 0000 hex of memory.
SMxxxx<cr>	Substitute Memory	Allows the substitution of memory contents starting at xxxx. Carriage return will abort, space bar advances to next location.

SRx<cr>	Substitute Register	Allows the substitution of all break point register values and flags as shown in notes.
T	not used	
U	not used	
V	not used	
W<cr>	Write disk	Will write memory contents at location 0000 hex of memory onto the diskette in drive A:
X	not used	
Y	not used	
Zxxxx,yyyy	Zero memory	Will zero memory between xxxx and yyyy.

PROM Monitor Display Options

The monitor has several display options which allow the control of screen dumps and control of listings using a printer. These options are listed below.

Function	Option	Description
Memory Dumps	- Control-S	Stops Display scroll.
	- Control-Q	Starts Display scroll.
	- Esc key	Aborts dump and returns to command level.
Printer listing	- Control-P	Enables console dumps to printer. This is a toggle function, where a second control-P will stop printer listing.

(NOTE) Control P option valid only while in the monitor command mode.

I/O Port Address Assignments

The CPZ-4800X uses the last 128 I/O ports assignment of it's 256 I/O port address space for use with it's on-board peripheral chips. Below is a breakdown of these i/o ports by port function and it's corresponding address in hex.

[Serial Port A and B Assignments]

DART/SIO Port A Data Reg.	80 Hex
DART/SIO Port A Control Reg.	81 Hex
DART/SIO Port B Data Reg.	82 Hex
DART/SIO Port B Control Reg.	83 Hex

[Floppy Disk Controller Assignment]

FDC Command/Status Reg.	90 Hex
FDC Track Reg.	91 Hex
FDC Sector Reg.	92 Hex
FDC Data Reg.	93 Hex

[Parallel Port A and B Assignment]

PIO Port A Data Reg.	A0 Hex
PIO Port A Control Reg.	A1 Hex
PIO Port B Data Reg.	A2 Hex
PIO Port B Control Reg.	A3 Hex

[Timer Port Assignments]

Timer Channel 0	B0 Hex
Timer Channel 1	B1 Hex
Timer Channel 2	B2 Hex
Timer Control Reg.	B3 Hex

[Interrupt Controller Assignments]

Interrupt Select Reg.	C0 Hex
Interrupt Command Reg.	C1 Hex

[Control Registers]

Prom/Boot Reg.	D0 Hex
Deselect Window Reg.	D1 Hex
FDC Drive Select Reg.	D2 Hex
FDC Wait Reg. (program data xfer use)	D3 Hex

[Memory Management Registers]

MMU Address Reg 1	E0 Hex
MMU Address Reg 2	E1 Hex
MMU Address Reg 3	E2 Hex
MMU Address Reg 4	E3 Hex
MMU Address Reg 5	E4 Hex
MMU Address Reg 6	E5 Hex
MMU Address Reg 7	E6 Hex
MMU Address Reg 8	E7 Hex
MMU Address Reg 9	E8 Hex
MMU Address Reg 10	E9 Hex
MMU Address Reg 11	EA Hex
MMU Address Reg 12	EB Hex
MMU Address Reg 13	EC Hex
MMU Address Reg 14	ED Hex
MMU Address Reg 15	EE Hex
MMU Address Reg 16	EF Hex

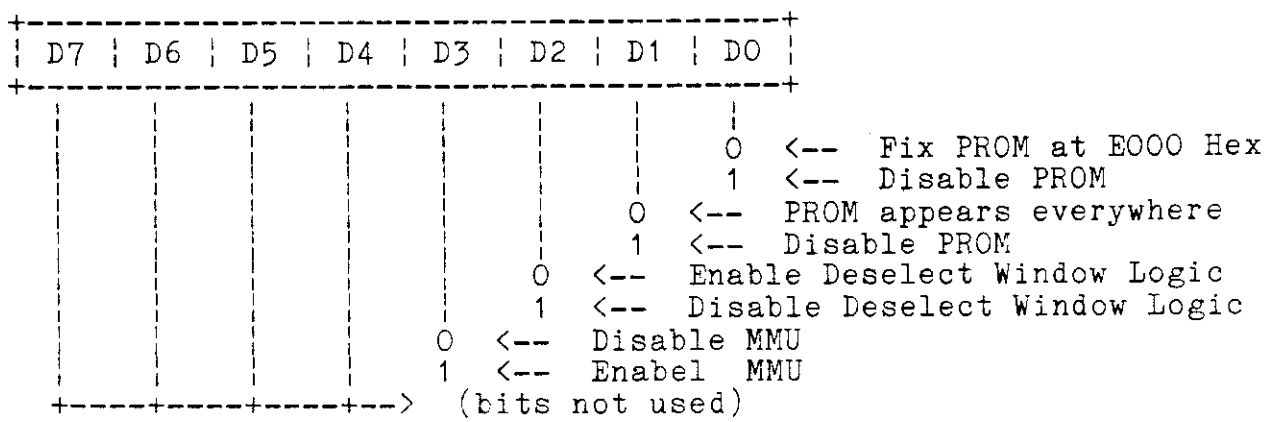
[Direct Memory Access Registers]

DMA Base/Current Address Reg. 0	F0 Hex
DMA Base/Current Word Count Reg. 0	F1 Hex
DMA Base/Current Address Reg. 1	F2 Hex
DMA Base/Current Word Count Reg. 1	F3 Hex
DMA Base/Current Address Reg. 2	F4 Hex
DMA Base/Current Word Count Reg. 2	F5 Hex
DMA Base/Current Address Reg. 3	F6 Hex
DMA Base/Current Word Count Reg. 3	F7 Hex
DMA Status/Command Register	F8 Hex
DMA Write Request Register (software)	F9 Hex
DMA Write Single Mask Reg.	FA Hex
DMA Write Mode Reg.	FB Hex
DMA Clear Byte Pointer Flip-Flop	FC Hex
DMA Master Clear/Read Temp. Reg.	FD Hex
DMA (not used)	FE Hex
DMA Write All Mask Reg.	FF Hex

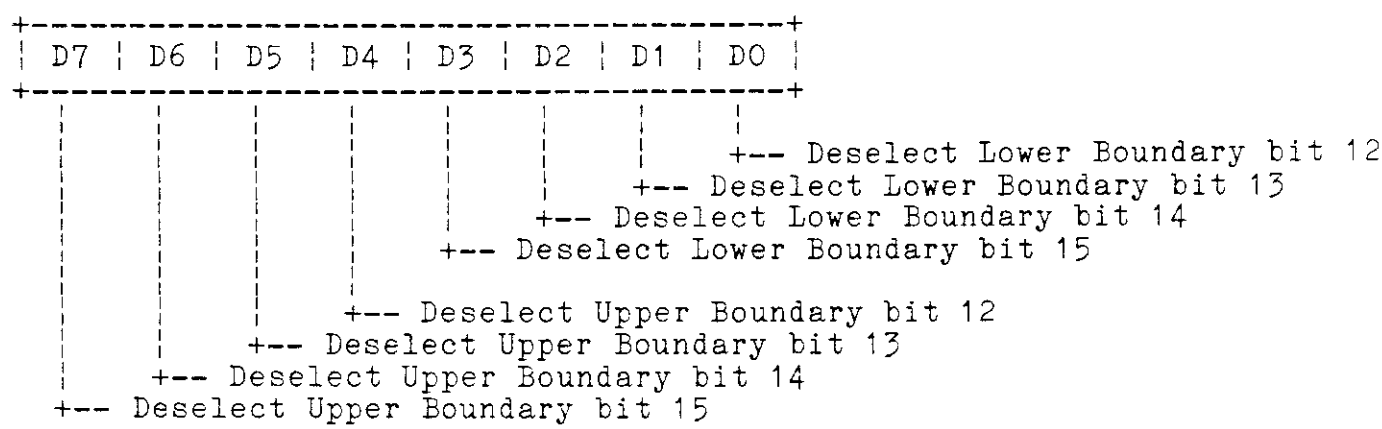
Control Register Bit Assignments

This is a description of the Control Registers and the corresponding bit assignments used on the CPZ4800X.

[PROM / Boot Register (Port D0 Hex)]



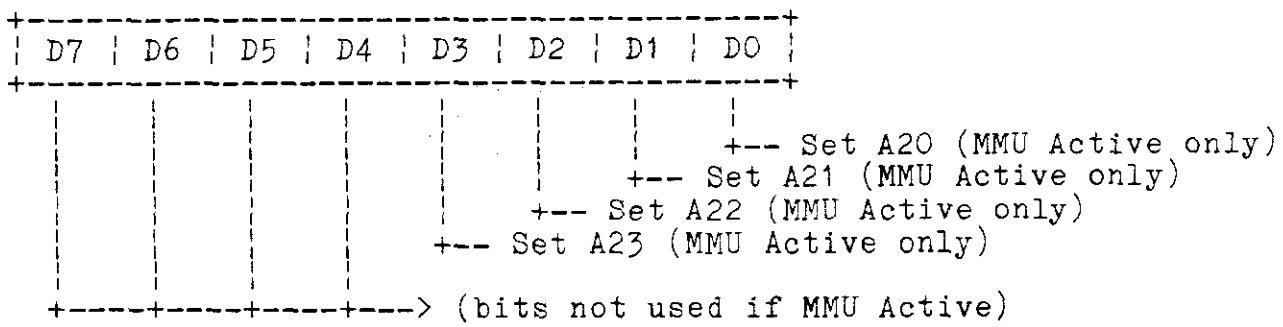
[Deselect Memory Window (Port D1 Hex)]



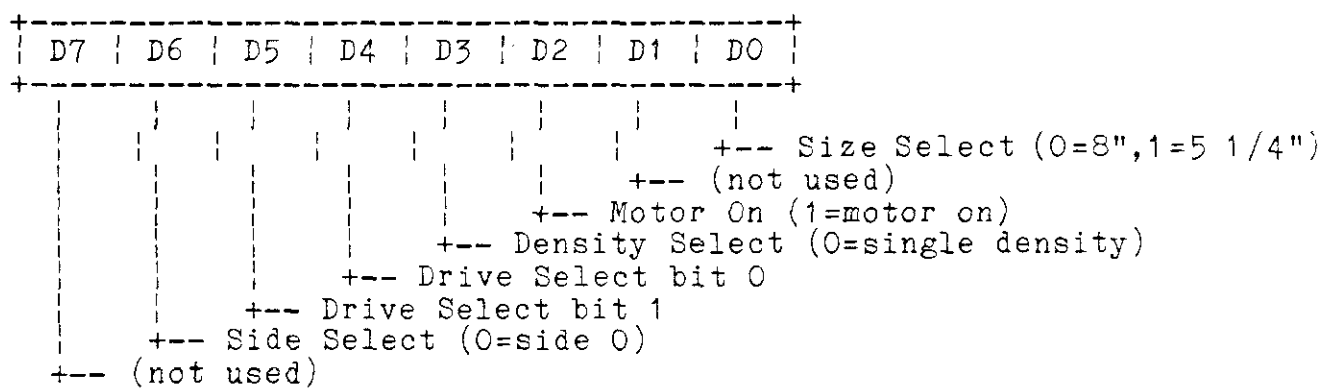
****** N O T E ******

The Deselect Window logic has a secondary function which is only active if the PROM Monitor is not active. The lower 4 bits of this control register sets the range for the extended groups of each 1 megabyte of extended address lines A20 to A23. Below is a table showing the bit assignments for this function.

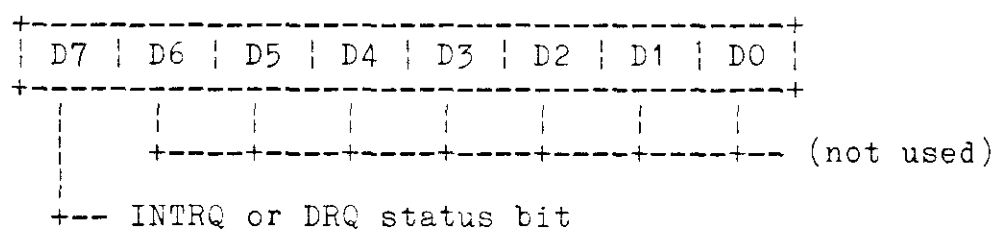
[Extended Megabyte Set Register (Port D1 Hex)]



[FDC Drive Select Register (Port D2 Hex)]

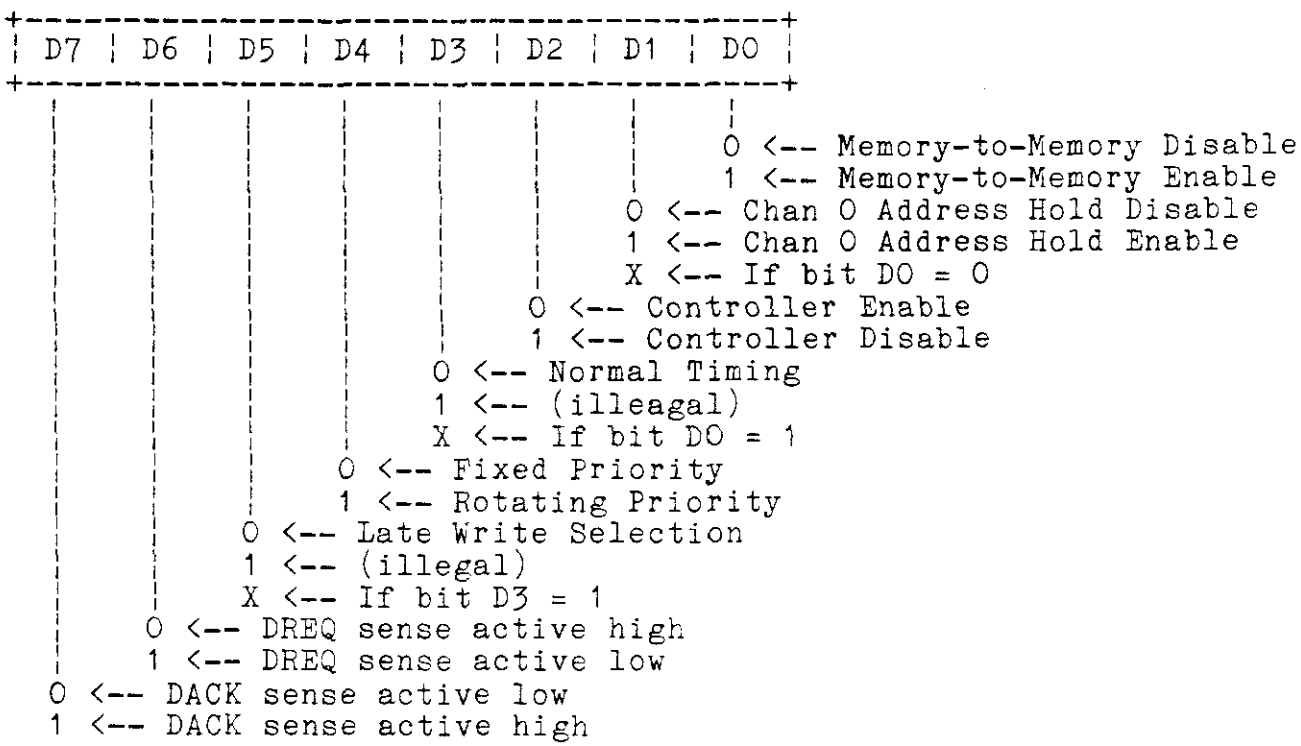


[FDC Wait Register (Port D3 Hex)]

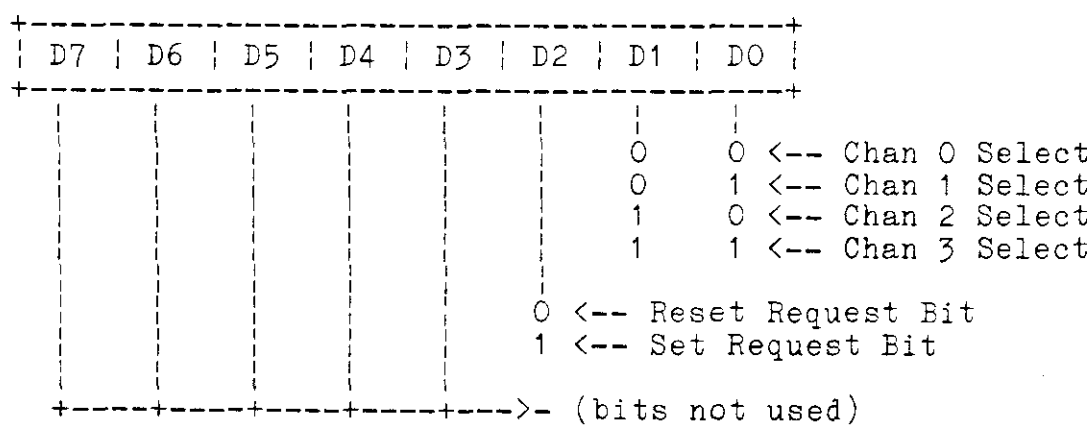


DMA Register Bit Assignments

[Command Register]



[Request Register bits]



[Mode Register Bit Assignments]

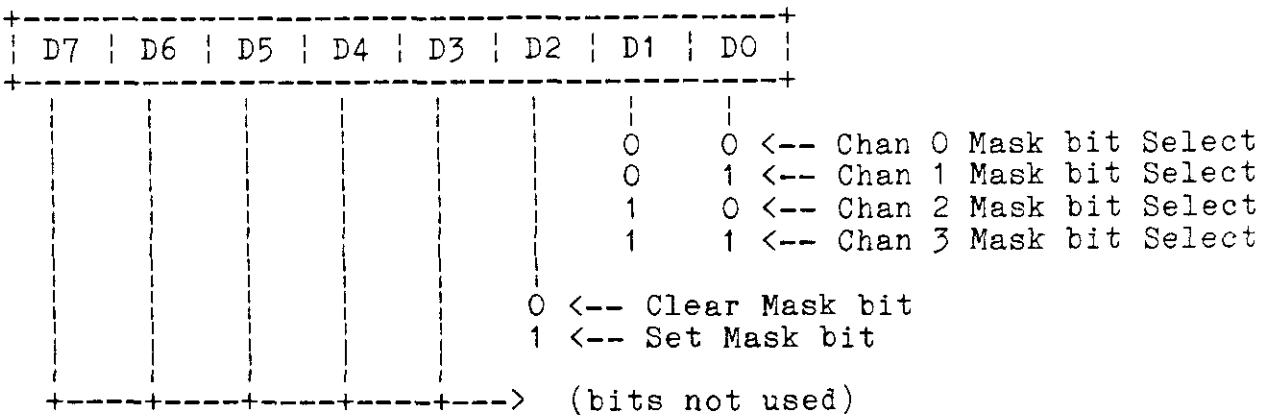
```
+-----------------------------------------+
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | DO |
+-----------------------------------------+
                                  0    0 <-- Chan 0 Select
                                  0    1 <-- Chan 1 Select
                                  1    0 <-- Chan 2 Select
                                  1    1 <-- Chan 3 Select
                             0    0 <-- Verify Transfer (not used)
                             0    1 <-- Write Transfer
                             1    0 <-- Read Transfer
                             1    1 <-- (illegal)
                             X    X <-- If bits D6 & D7 = 11
                        0 <-- Disable Autoinitialize
                        1 <-- Enable Autoinitialize
                   0 <-- Select Address Increment
                   1 <-- Select Address Decrement
   0    0 <-- Demand Mode Select
   0    1 <-- Single Mode Select
   1    0 <-- Block Mode Select
   1    1 <-- Cascade Mode Select
```

[Status Register Bit Assignments]

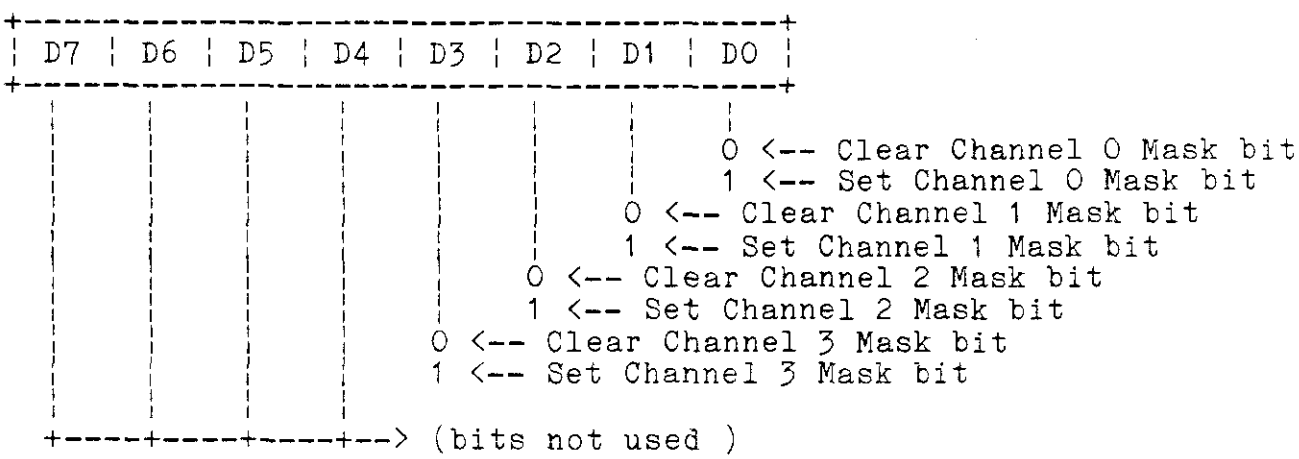
```
+-----------------------------------------+
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | DO |
+-----------------------------------------+
                                  1 = Chan 0 has reached T.C.
                                1 = Chan 1 has reached T.C.
                              1 = Chan 2 has reached T.C.
                            1 = Chan 3 has reached T.C.


                        1 = Chan 0 is Requesting
                   1 = Chan 1 is Requesting
              1 = Chan 2 is Requesting
   1 = Chan 3 is Requesting
```

[Mask Register (single mask bit) Assignments]



[Mask Register (all mask bits) Assignment]



Serial Port A and B Software Description

Both serial ports A and B must be initialized after a system reset is performed before they will communicate with any terminals or the like. Each channel has a set of registers which program the device for a certain function. As we are only concerned with programming each channel for standard RS-232C interfacing, we will not describe the other functions that each channel contains here. For further information about the SDLC/HDLC functions, refer to the ZILOG support chip manuals.

Below is a software example for initializing the SIO ports A and B for standard RS-232C interfacing.

```
CMNDA   EQU     81H             ;command port chan A
CMNDB   EQU     83H             ;command port chan B
;
;init channel A:
;get length of init table in reg b
;get command port into reg c.
;
INITA:  LD      BC,(CHANAE-CHANA) SHL 8 OR CMNDA
        LD      HL,CHANA                ;point to chan A init table
        OTIR                            ;block i/o send it
;
;init channel B:
;get length of init table in reg b,
;get command port into reg c.
;
INITB:  LD      BC,(CHANBE-CHANB) SHL 8 OR CMNDB
        LD      HL,CHANB                ;point to chan B init table
        OTIR                            ;block i/o send it
        RET
;
;init tables for channel A and B
;
CHANA:  DB      18H,04H         ;reset A, write reg 4
        DB      4CH,01H         ;x16 clk, 1 stopbit,no parity, write reg 1
        DB      00H,03H         ;no interrupts, write reg 3
        DB      0E1H,05H        ;rx 8 bits, autoenables, rx enable,
                                ;write reg 5
        DB      0EAH            ;tx 8 bits, tx enable
CHANAE  EQU     $               ;end of table marker
;
CHANB:  DB      18H,04H
        DB      4CH,01H
        DB      00H,03H
        DB      0E1H,05H
        DB      0EAH
CHANBE  EQU     $               ;end of table marker
```

Channel A and B Baud Rate Software Example

After the SIO has been initialized, you should next set the Baud Rate for each of the two ports to match the device to which it is attached. Below is an example of setting the timer channel for each of the serial ports. Timer channel 0 controls serial port A, and Timer channel 1 controls serial port B. The crystal frequency used to control the timer is a 2.4576 MHz crystal. This value lends itself to even binary divisions as illustrated below and can be used to program the timer channel directly as the count.

```
;
;equates for timer channel
;
TCH0    EQU     0B0H            ;channel 0 timer
TCH1    EQU     0B1H            ;channel 1 timer
TCMND   EQU     0B3H            ;timer command port
CHAMD   EQU     36H             ;chan 0 mode
CHBMD   EQU     76H             ;chan 1 mode
;
;baud rate equates
;
CLK     EQU     24576           ;crystal freq (KHz)
B38400  EQU     CLK/384/16      ;38,400 baud
B19200  EQU     CLK/192/16      ;19,200 baud
B9600   EQU     CLK/96/16       ;9600 baud
B4800   EQU     CLK/48/16       ;4800 baud
B2400   EQU     CLK/24/16       ;2400 baud
B1200   EQU     CLK/12/16       ;1200 baud
B600    EQU     CLK/6/16        ;600 baud
B300    EQU     CLK/3/16        ;300 baud
;
;set chan A baud rate subroutine
;
BAUDA:  LD      DE,B9600        ;select 9600 baud
        LD      C,TCH0          ;reg c = timer chan 0 port
        LD      A,CHAMD         ;get command byte
        OUT     (TCMND),A       ;send to timer command port
        OUT     (C),E           ;send low baud byte
        OUT     (C),D           ;send high baud byte
        RET                     ;return to caller
;
;set chan B baud rate subroutine
;
BAUDB:  LD      DE,B19200       ;select 19200 baud
        LD      C,TCH1          ;reg c = timer chan 1 port
        LD      A,CHBMD         ;get command byte
        OUT     (TCMND),A       ;send to timer command port
        OUT     (C),E           ;send low baud byte
        OUT     (C),D           ;send high baud byte
        RET                     ;return to caller
;
```

Typical CPZ-4800X Initialize routines to setup 74LS610 memory management unit, 9517 INterrupt controller unit, and 9517A DMA controller for S-100 bus DMA operations.

```
;Vector interrupt definitions for
;Intercontinental Micro Systems CPZ-4800X
;
VIBASE  EQU     0010H           ;Base address of VI table
;
IPAGE   EQU     HIGH VIBASE     ;Z80 I register value
;
SIOVEC  EQU     VIBASE+16       ;DART/SIO interrupt address
VIO     EQU     VIBASE+14       ;VIO ISR address (real time clock)
VI1     EQU     VIBASE+12       ;VI1  "  "           (FDC interrupt  )
VI2     EQU     VIBASE+10       ;VI2  "  "           (DMA #1 complete)
VI3     EQU     VIBASE+8        ;VI3  "  "           (DMA #2 complete)
VI4     EQU     VIBASE+6        ;VI4  "  "           (DMA #3 complete)
VI5     EQU     VIBASE+4        ;VI5  "  "           (Parallel port  )
VI6     EQU     VIBASE+2        ;VI6  "  "           (S-100 bus error)
VI7     EQU     VIBASE+0        ;VI7  "  "           (     spare     )
;
;DART/SIO device ports
;
SIOAD   EQU     080H    ;channel A data
SIOAC   EQU     081H    ;channel A control/status
SIOBD   EQU     082H    ;channel B data
SIOBC   EQU     083H    ;channel B control/status
;
;DART/SIO read register 0 bit assignment
;
RDA     EQU     0       ;read data available
TBE     EQU     2       ;transmitter buffer empty
DCD     EQU     3       ;data carrier detect
CTS     EQU     5       ;clear to send
;
;SIO read register 1 bit assignment
;
PE      EQU     4       ;parity error
OE      EQU     5       ;overrun error
FE      EQU     6       ;framing error
;
;Floppy Disk Controller ports and commands.
;
DCOM    EQU     090H    ;disk command register
DSTAT   EQU     DCOM    ;disk status register
DTRACK  EQU     DCOM+1  ;disk track register
SECTP   EQU     DCOM+2  ;disk sector register
DDATA   EQU     DCOM+3  ;disk data register
DWAIT   EQU     0D3H    ;program data xfer wait port
DCONT   EQU     0D2H    ;drv, side, den, motor on, port
;
```

```
;define disk control port
;
SIDEO   EQU     6       ;side select bit (0=side0, 1=side1)
DENSITY EQU     3       ;density bit (0=sing, 1=doub)
MOTON   EQU     2       ;motor on bit (0=off, 1=on)
;
;define wait port bits
;
FINT    EQU     7       ;floppy interrupt bit (intrq)
;
;define floppy commands
;
RESTOR  EQU     00000000B       ;restore command
DSEEK   EQU     00010000B       ;seek command
STEP    EQU     00100000B       ;step command
STEPIN  EQU     01000000B       ;step in command
STEPOUT EQU     01100000B       ;step out command
READSEC EQU     10000000B       ;read sector command
WRTSEC  EQU     10100000B       ;write sector command
RDADDR  EQU     11000000B       ;read address command
RDTRK   EQU     11100000B       ;read track command
WRTTRK  EQU     11110000B       ;write track command
FRCINT  EQU     11010000B       ;force interrupt command
VERIF   EQU     00000100B       ;verify flag bit
UPDATE  EQU     00010000B       ;update flag bit
MULTI   EQU     00010000B       ;multiple record flag
DLAY15  EQU     00000100B       ;delay 15 ms
;
;floppy status register bits (type i some type ii & iii commands)
;
READY   EQU     7       ;floppy ready bit
PROTEC  EQU     6       ;write protect bit
HEADLD  EQU     5       ;head load bit
ERRSEK  EQU     4       ;seek error bit
ERRCRC  EQU     3       ;crc error bit
TRK0    EQU     2       ;track 0 bit
INDX    EQU     1       ;index bit
BUSY    EQU     0       ;busy bit
RECNF   EQU     4       ;record not found bit
LOSTD   EQU     2       ;lost data bit (type ii)
DRQ     EQU     1       ;data request (type ii)
;
;PIO device ports (Centronics compatable mode)
;
PIOAD   EQU     0A0H    ;port A data
PIOAC   EQU     0A1H    ;port A control/status
PIOBD   EQU     0A2H    ;port B data
PIOBC   EQU     0A3H    ;port B control/status
PBSY    EQU     0       ;status bit for printer ready
;
```

```
;8253 Timer ports
CNT0    EQU     0B0H    ;counter 0
CNT1    EQU     0B1H    ;counter 1
CNT2    EQU     0B2H    ;counter 2
CTRL    EQU     0B3H    ;control port
;8253 Timer commands
;
SET0    EQU     036H    ;set counter 0
SET1    EQU     076H    ;set counter 1
SET2    EQU     0B6H    ;set counter 2
;
;AMD 9519 universal interrupt controller ports
;
UICD    EQU     0C0H    ;UIC select register
UICC    EQU     0C1H    ;UIC command/status
;
;Boot PROM control ports
;
BOOTR   EQU     0D0H    ;PROM / Boot register
CSWIND  EQU     0D1H    ;Deselect memory window
;
;74LS610 Memory Management Unit
;
MMU1    EQU     0E0H    ;Address Register 1
MMU2    EQU     0E1H    ;Address Register 2
MMU3    EQU     0E2H
MMU4    EQU     0E3H
MMU5    EQU     0E4H
MMU6    EQU     0E5H
MMU7    EQU     0E6H
MMU8    EQU     0E7H
MMU9    EQU     0E8H
MMU10   EQU     0E9H
MMU11   EQU     0EAH
MMU12   EQU     0EBH
MMU13   EQU     0ECH
MMU14   EQU     0EDH
MMU15   EQU     0EEH
MMU16   EQU     0EFH    ;Address Register 16
;
;9517A DMA ports and commands.
;
DMAP    EQU     0F0H    ;base address of dma chip
ADR0    EQU     DMAP+0  ;address reg chan 0
WCT0    EQU     DMAP+1  ;word count chan 0
ADR1    EQU     DMAP+2  ;address reg chan 1
WCT1    EQU     DMAP+3  ;word count chan 1
ADR2    EQU     DMAP+4  ;address reg chan 2
WCT2    EQU     DMAP+5  ;word count chan 2
ADR3    EQU     DMAP+6  ;address reg chan 3
WCT3    EQU     DMAP+7  ;word count chan 3
CMND    EQU     DMAP+8  ;command/status register
REQREG  EQU     DMAP+9  ;software/hardware request reg
FMASK   EQU     DMAP+10 ;single mask register select
MODE    EQU     DMAP+11 ;mode register
```

```
CLRBP   EQU     DMAP+12 ;clear byte pointer f/f
MSTRCL  EQU     DMAP+13 ;master clear
MASK    EQU     DMAP+15 ;write all mask registers
;
;command register options
;
DMAW    EQU     01000000B       ;DMA write
DMAR    EQU     10000000B       ;DMA read
DMAV    EQU     00000000B       ;DMA verify
DACKL   EQU     00000000B       ;dack active low
DACKH   EQU     10000000B       ;dack active high
DREQH   EQU     00000000B       ;dreq active low
DREQL   EQU     01000000B       ;dreq active high
LWRIT   EQU     00000000B       ;late write selection
EXTWRT  EQU     00100000B       ;extended write selection
FIXPRI  EQU     00000000B       ;fixed priority mode
ROTPRI  EQU     00010000B       ;rotating priority mode
NORTIM  EQU     00000000B       ;normal timing mode
COMTIM  EQU     00001000B       ;compressed timing mode
DMAENB  EQU     00000000B       ;dma chip enable
DMADSB  EQU     00000100B       ;dma chip disable
COHLDD  EQU     00000000B       ;chan 0 addr hold disable
COHLDE  EQU     00000010B       ;chan 0 addr hold enable
MTMDSB  EQU     00000000B       ;memory to memory disable
MTMENB  EQU     00000001B       ;memory to memory enable
;
;mode register options
;
DEMAND  EQU     00000000B       ;demand mode
SINGLE  EQU     01000000B       ;single mode
BLOCK   EQU     10000000B       ;block mode
CASCADE EQU     11000000B       ;cascade mode
ADDRUP  EQU     00000000B       ;addr increment mode
ADDRDN  EQU     00100000B       ;addr decrement mode
AUTODSB EQU     00000000B       ;autoinitialize disable
AUTOENB EQU     00010000B       ;autoinitialize enable
VERIFYT EQU     00000000B       ;verify transfer
WRTXFR  EQU     00000100B       ;write transfer
RDXFR   EQU     00001000B       ;read transfer
CHAN0   EQU     00000000B       ;channel 0 select
CHAN1   EQU     00000001B       ;channel 1 select
CHAN2   EQU     00000010B       ;channel 2 select
CHAN3   EQU     00000011B       ;channel 3 select
;
;request register / mask register options
;       (note: uses regs shown above)
;
CLRREQ  EQU     00000000B       ;reset request bit
SETREQ  EQU     00000100B       ;set request bit
;
;mask register options
;
CLRCH0  EQU     00000000B       ;clear chan 0 mask bit
SETCH0  EQU     00000001B       ;set chan 0 mask bit
CLRCH1  EQU     00000000B       ;clear chan 1 mask bit
```



```
SETCH1  EQU     00000010B       ;set chan 1 mask bit
CLRCH2  EQU     00000000B       ;clear chan 2 mask bit
SETCH2  EQU     00000100B       ;set chan 2 mask bit
CLRCH3  EQU     00000000B       ;clear chan 3 mask bit
SETCH3  EQU     00001000B       ;set chan 3 mask bit
;
;bit positions for status reg.
;
CH3REQ  EQU     7       ;chan 3 request bit
CH2REQ  EQU     6       ;chan 2 reguest bit
CH1REQ  EQU     5       ;chan 1 request bit
CHOREQ  EQU     4       ;chan 0 request bit
CH3TC   EQU     3       ;chan 3 terminal count
CH2TC   EQU     2       ;chan 2 terminal count
CH1TC   EQU     1       ;chan 1 terminal count
CHOTC   EQU     0       ;chan 0 terminal count
;
;end of CPZ-4800X general equate file
;
;begin initialization examples
;
CPZNIT: LD      A,00000110B     ;select in all of memory.
        OUT     (BOOTR),A       ;send to Prom/Boot register control.
;
        XOR     A               ;clear reg A
        OUT     (CSWIND),A      ;clear extended megabyte lines
        LD      B,16            ;set up count value (16 regs in all)
        LD      C,MMU1          ;address of Memory Management chip base
;
;initialize all 16 registers for
;standard 64K bytes of contigues memory.
;
CLOOP:  OUT     (C),A           ;send init byte
        INC     A               ;init next port byte (0,1,2,3,...etc..D,E,F)
        INC     C               ;bump to next mmu register (E0,E1....EE,EF)
        DJNZ    CLOOP           ;loop till done (16 times)
;
        LD      A,0FH           ;establish basic operation of board
        OUT     (BOOTR),A       ;enable m/m unit
;
        LD      A,IPAGE         ;get equated IPAGE address (High Byte)
        LD      I,A             ;load it
        IM      2               ;select mode 2 interrupts
;
;Beginning of the AMD 9519 universal interrupt controller
;initialization routines. This routine allows the user to
;establish the interrupt vector at VIBASE and then enable
;or disable interrupts by calling CLRIMR or SETIMR for any
;user written routines as needed. The 9519 is completely
;initialized by these routines, so all the user has to do
;is define which vector is to be used.
;
        XOR     A               ;clear reg A
        OUT     (UICC),A        ;reset AMD 9519 interrupt controller
;
```

```
;IREQ lines active LOW, Group Interrupt active LOW,
;Fixed Priority with individual vectors, interrupt mode.
;
        LD      A,10000000B
        OUT     (UICC),A        ;send to UIC device
;
        LD      A,10101001B     ;set "M7" (chip armed bit)
        OUT     (UICC),A
;
        LD      A,11000000B     ;pre-select auto clear register
        OUT     (UICC),A
        LD      A,11111111B     ;auto clear all IRR bits
        OUT     (UICD),A        ;load auto clear register
;
        LD      A,01000000B     ;clear all IRR bits
        OUT     (UICC),A
        LD      A,01110000B     ;clear all ISR bits
        OUT     (UICC),A
;
;Initialize the Vector interrupt table within IPAGE
;
        LD      HL,VIBASE       ;get VI table base address
        LD      A,7             ;init counter to VI-7
        LD      C,UICC          ;get UIC command/status port
;
UIC.1:  PUSH    AF              ;save current VI value
        OR      0E0H            ;pre-select response memory (1 byte)
        OUT     (C),A           ;send to command port
        DEC     C               ;reference UIC data port
        OUT     (C),L           ;send low order VI addr for response
        INC     C               ;reference UIC command/status port
        INC     HL
        INC     HL              ;point to next VI address
        POP     AF              ;restore current VI value
        DEC     A               ;select next, done with 7-0?
        JP      P,UIC.1         ;no, continue
;
;end of AMD 9519 initialization routine
;
;place dma into cascade mode for ch 0 so as to acknowledge
;any S-100 bus DMA requests.
;
CASMOD: LD      A,DREQL+ROTPRI  ;DREQ active high, rotating priority
        OUT     (CMND),A        ;send it
        LD      A,CASCADE+CHANO ;channel 0 cascade mode
        OUT     (MODE),A        ;send it
        LD      A,CLRREQ+CHANO  ;reset channel 0 request bit
        OUT     (FMASK),A       ;send it
        RET                     ;done
;
AMD 9519 universal interrupt controller subroutines.
These two routines may be called by the system drivers to unmask (CLEAR)
or mask (SET) bits within the Interrupt Mask Register (IMR) for selected
VI lines. These routines must be called with Reg A = Vector level (0 to 7).
;
```

```
SETIMR: AND     7               ;mask off valid bits
        OR      38H             ;add in command bits
        OUT     (UICC),A        ;send to 9519
        RET                     ;done
;
CLRIMR: AND     7               ;mask off valid bits
        OR      28H             ;add in command bits
        OUT     (UICC),A        ;send to 9519
        RET                     ;done
```


**** WARRANTY ****

All products sold hereunder are under warranty on a return to factory basis against defects in workmanship and material for a period of one (1) year from the date of delivery.

Conditions of this warranty are as follows: Purchaser must 1) obtain a return material authorization (RMA) number and shipping instructions, 2) product must be shipped prepaid, 3) written description of the failure must be included with the defective product. All transportation charges inside the continental U.S. will be paid by Intercontinental Micro Systems (ICM) Corp. For products returned from all other locations, transportation must be prepaid. Should ICM determine that the products are not defective, the purchaser must pay all return transportation charges. All repairs will be provided at repair rates being charged at the time by ICM. Under the above product warranty, ICM may, at its option, either repair or replace any component which fails during the warranty period providing the purchaser has reported same in a prompt manner. All replaced products or parts shall become property of ICM.

All above warranties are contingent upon proper use of the product. These warranties will not apply 1) if any repair, parts replacement, or adjustments are necessary due to accident , unusual physical, electrical or electromagnetic stress, neglect, misuse, failure of electric power, air conditioning, humidity control, transportation, failure of rotating media not furnished by ICM, operation with media not meeting or not maintained in accordance with ICM specifications or causes other than ordinary use, 2) if the product has been modified by purchaser, 3) where ICM's serial numbers or warranty date decals have been removed or altered, 4) if the product has been dismantled by purchaser without the supervision of or prior written approval of ICM.

EXCEPT FOR THE EXPRESS WARRANTIES CONTAINED HEREIN, ICM DISCLAIMS ALL WARRANTIES ON THE PRODUCTS FURNISHED HEREUNDER, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS; and the stated express warranties are in lieu of all obligations or liabilities on the part of ICM arising out of or in connection with the performance of the products. ICM is not liable for any indirect or consequential damages.

After the warranty period, the products will be repaired for a service charge plus parts, provided that it is returned prepaid to ICM after retaining a return material authorization (RMA) number.

**** APPENDIX A ****

SPECIAL-CHIPS DATA SHEETS

Data sheets are included for the following chips used in the CPZ4800X:

- CENTRAL PROCESSOR UNIT [Z80-CPU]
- PARALLEL INPUT/OUTPUT CONTROLLER [Z80-PIO]
- SERIAL INPUT/OUTPUT CONTROLLER [Z80-SIO]
- FLOPPY DISK FORMATTER/CONTROLLER [WD2793]
- MEMORY MAPPER [SN74LS610]
  (DATA SHEET & APPLICATION NOTE)
- UNIVERSAL INTERRUPT CONTROLLER [AM9519A]
- DIRECT MEMORY ACCESS CONTROLLER [AM9517A]

Am9517A

Multimode DMA Controller

DISTINCTIVE CHARACTERISTICS

- Four independent DMA channels, each with separate registers for Mode Control, Current Address, Base Address, Current Word Count and Base Word Count
- Transfer modes: Block, Demand, Single Word, Cascade
- Independent autoinitialization of all channels
- Memory-to-memory transfers
- Memory block initialization
- Address increment or decrement
- Master system disable
- Enable/disable control of individual DMA requests
- Directly expandable to any number of channels
- End of Process input for terminating transfers
- Software DMA requests
- Independent polarity control for DREQ and DACK signals
- Compressed timing option speeds transfers – up to 2.5M bytes/second
- +5 volt power supply
- Advanced N-channel silicon gate MOS technology
- 40 pin Hermetic DIP package
- New 9517A-5 5MHz version for higher speed CPU compatability

GENERAL DESCRIPTION

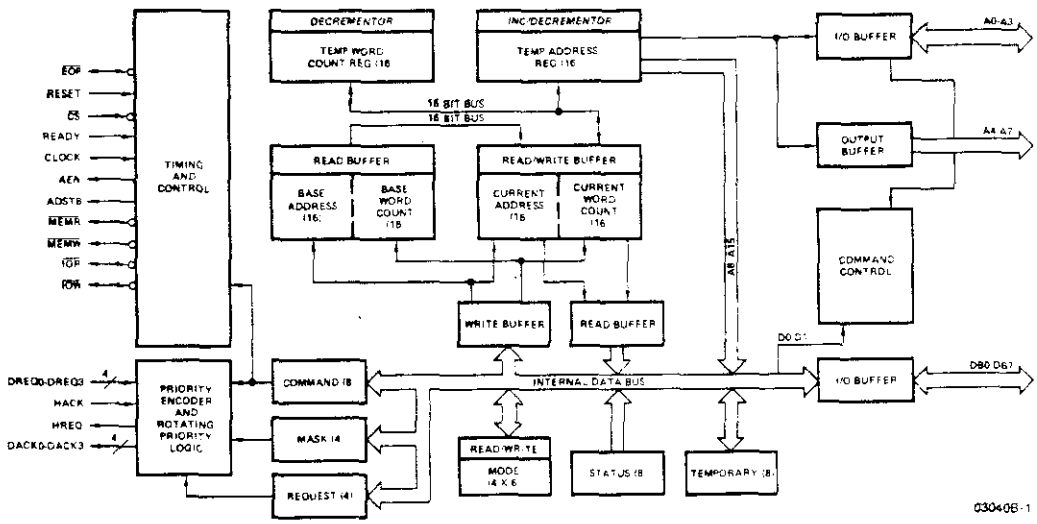
The Am9517A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information to or from the system memory. Memory-to-memory transfer capability is also provided. The Am9517A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The Am9517A is designed to be used in conjunction with an external 8-bit address register such as the Am74LS373. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process ($\overline{EOP}$).

Each channel has a full 64K address and word count capability. An external $\overline{EOP}$ signal can terminate a DMA or memory-to-memory transfer. This is useful for block search or compare operations using external comparators or for intelligent peripherals to abort erroneous services.

BLOCK DIAGRAM

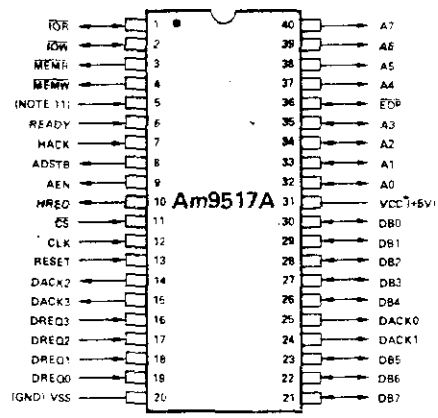


ORDERING INFORMATION

Package Type	Ambient Temperature	Maximum Clock Frequency		
		3MHz	4MHz	5MHz
Hermetic DIP, Molded DIP	$0°C \leq T_A \leq +70°C$	AM9517ADC/PC AM9517A-1DC/PC	AM9517A-4DC/PC	AM9517A-5DC/PC
Hermetic DIP	$-40°C \leq T_A \leq +85°C$	AM9517ADI AM9517A-1DI	AM9517A-4DI/PI	
Hermetic DIP	$-55°C \leq T_A \leq +125°C$	AM9517ADMB		

03040B-MMP

Figure 1. Connection Diagram
D-40, P-40



Top View
Pin 1 is marked for orientation.

INTERFACE SIGNAL DESCRIPTION

VCC: +5 Volt Supply
VSS: Ground

CLK (Clock, Input)

This input controls the internal operations of the Am9517A and its rate of data transfers. The input may be driven at up to 3MHz for the standard Am9517A, up to 4MHz for the Am9517A-4, and up to 5MHz for the Am9517A-5.

$\overline{CS}$ (Chip Select, Input)

Chip Select is an active low input used to select the Am9517A as an I/O device during an I/O Read or I/O Write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the Am9517A by the host CPU, $\overline{CS}$ may be held low providing $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer.

RESET (Reset, Input)

Reset is an asynchronous active high input which clears the Command, Status, Request and Temporary registers. It also clears the First/Last Flip/Flop and sets the Mask register. Following a Reset the device is in the Idle cycle.

READY (Ready, Input)

Ready is an input used to extend the memory read and write pulses from the Am9517A to accommodate slow memories or I/O peripheral devices.

HACK (Hold Acknowledge, Input)

The active high Hold Acknowledge from the CPU indicates that control of the system buses has been relinquished.

DREQ0-DREQ3 (DMA Request, Input)

The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. Polarity of DREQ is programmable. Reset initializes these lines to active high.

DB0-DB7 (Data Bus, Input/Output)

The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled during the I/O Read by the host CPU, permitting the CPU to examine the contents of an Address register, the Status register, the Temporary register or a Word Count register. The Data Bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the Am9517A control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the Am9517A's Temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the Temporary register data into the destination memory location.

$\overline{IOR}$ (I/O Read, Input/Output)

I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the Am9517A to access data from a peripheral during a DMA Write transfer.

$\overline{IOW}$ (I/O Write, Input/Output)

I/O Write is a bidirectional active low three-state line. In the Idle cycle it is an input control signal used by the CPU to load information into the Am9517A. In the Active cycle it is an output control signal used by the Am9517A to load data to the peripheral during a DMA Read transfer.

Write operations by the CPU to the Am9517A require a rising $\overline{IOW}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{IOW}$ pin low and toggle $\overline{CS}$.

$\overline{EOP}$ (End of Process, Input/Output)

$\overline{EOP}$ is an active low bidirectional open-drain signal providing information concerning the completion of DMA service. When a channel's Word Count goes to zero, the Am9517A pulses $\overline{EOP}$ low to provide the peripheral with a completion signal. $\overline{EOP}$ may also be pulled low by the peripheral to cause premature completion. The reception of $\overline{EOP}$, either internal or external, causes the currently active channel to terminate the service, to set its TC bit in the Status register and to reset its request bit. If Autoinitialization is selected for the channel, the current registers will be updated from the base registers. Otherwise the channel's mask bit will be set and the register contents will remain unaltered.

During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ always applies to the channel with an active DACK; external $\overline{EOP}$s are disregarded when DACK0-DACK3 are all inactive if the DMA is in state SI.

In situations where two or more Am9517A DMAs are cascaded, the $\overline{EOP}$ pins should be logically OR'ed (not wire-OR'ed).

Because $\overline{EOP}$ is an open-drain signal, an external pullup resistor is required. Values of 3.3K or 4.7K are recommended; the $\overline{EOP}$ pin cannot sink the current passed by a 1K pullup.

A0-A3 (Address, Input/Output)

The four least significant address lines are bidirectional 3-state signals. During DMA Idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the lower 4-bits of the output address.

A4-A7 (Address, Output)

The four most significant address lines are three-state outputs and provide four bits of address. These lines are enabled only during DMA service.

HREQ (Hold Request, Output)

The Hold Request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the Am9517A to issue HREQ.

DACK0-DACK3 (DMA Acknowledge, Output)

The DMA Acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.

AEN (Address Enable, Output)

Address Enable is an active high signal used to disable the system bus during DMA cycles to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HACK and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed *as programmed I/O during the DMA 'operation. The* Am9517A automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.

ADSTB (Address Strobe, Output)

The active high Address Strobe is used to strobe the upper address byte from DB0-DB7 into an external latch.

Figure 2. Am9517A Internal Registers.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

$\overline{MEMR}$ (Memory Read, Output)

The Memory Read signal is an active low three-state output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.

$\overline{MEMW}$ (Memory Write, Output)

The Memory Write signal is an active low three-state output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.

FUNCTIONAL DESCRIPTION

The Am9517A block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The Am9517A contains 344 bits of internal memory in the form of registers. Figure 2 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

The Am9517A contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the Am9517A. The Program Command Control block decodes the various commands given to the Am9517A by the microprocessor prior to servicing a DMA Request. It also decodes each channel's Mode Control word. The Priority Encoder block resolves priority contention among DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In Am9080A systems this input will usually be the $\phi 2$ TTL clock from an Am8224. However, any appropriate system clock will suffice.

DMA Operation

The Am9517A is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The Am9517A can assume seven separate states, each composed of one full clock period. State I (SI) is the inactive state. It is entered when the Am9517A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The Am9517A has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted before S4 by the use of the Ready line on the Am9517A.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for each complete transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22 S23 and S24) for the write-to-memory half of the transfer. The Temporary Data register is used for intermediate storage of the memory byte.

IDLE Cycle

When no channel is requesting service, the Am9517A will enter the idle cycle and perform "SI" states. In this cycle the Am9517A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the Am9517A. When

$\overline{CS}$ is low and HACK is low the Am9517A enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip/flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip/flop is reset by Master Clear or Reset. A separate software command can also reset this flip/flop.

Special software commands can be executed by the Am9517A in the Program Condition. These commands are decoded as sets of addresses when both $\overline{CS}$ and $\overline{IOW}$ are active and do not make use of the data bus. Functions include Clear First/Last Flip/Flop and Master Clear.

ACTIVE CYCLE

When the Am9517A is in the Idle cycle and a channel requests a DMA service, the device will output a HREQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode: In Single Transfer mode, the Am9517A will make a one-byte transfer during each HREQ/HACK handshake. When DREQ goes active, HREQ will go active. After the CPU responds by driving HACK active, a one-byte transfer will take place. Following the transfer, HREQ will go inactive, the word count will be decremented and the address will be either incremented or decremented. When the word count goes to zero a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.

To perform a single transfer, DREQ must be held active only until the corresponding DACK goes active. If DREQ is held continuously active, HREQ will go inactive following each transfer and then will go active again and a new one-byte transfer will be made following each rising edge of HACK. In 8080A/9080A systems this will ensure one full machine cycle of execution between DMA transfers. Details of timing between the Am9517A and other bus control protocols will depend upon the characteristics of the microprocessor involved.

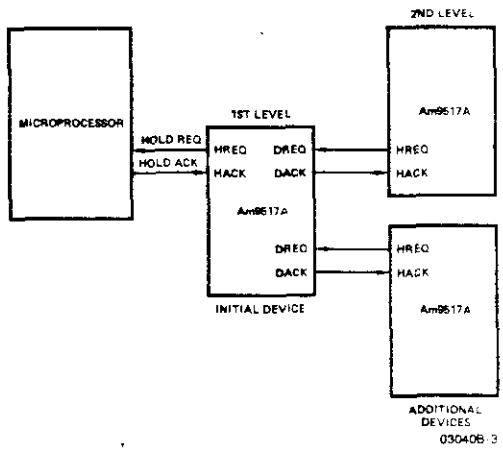
Block Transfer Mode: In Block Transfer mode, the Am9517A will continue making transfers until a TC (caused by the word count going to zero) or an external End of Process ($\overline{EOP}$) is encountered. DREQ need be held active only until DACK becomes active. An autoinitialize will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode: In Demand Transfer mode the device will continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus, the device requesting service may discontinue transfers by bringing DREQ inactive. Service may be resumed by asserting an active DREQ once again. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count may be read from the Am9517A Current Address and Current Word Count registers. Autoinitialization will only occur following a TC or $\overline{EOP}$ at the end of service. Following Autoinitialization, an active-going DREQ edge is required to initiate a new DMA service.

Cascade Mode: This mode is used to cascade more than one Am9517A together for simple system expansion. The HREQ and HACK signals from the additional Am9517A are connected to the DREQ and DACK signals of a channel of the initial Am9517A. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel in the initial device is used only for prioritizing the additional device, it does not output any address or control signals of its own. These would conflict with the outputs of the active channel in the added device. The Am9517A will respond to DREQ with DACK but all other outputs except HREQ will be disabled.

Figure 3 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More Am9517As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices forming a third level.

Figure 3. Cascaded Am9517As.



TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{IOR}$ and $\overline{MEMW}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers; the Am9517A operates as in Read or Write transfers generating addresses, responding to $\overline{EOP}$, etc., however, the memory and I/O control lines remain inactive.

Memory-to-Memory: The Am9517A includes a block move capability that allows blocks of data to be moved from one memory address space to another. When Bit C0 in the Command register is set to a logical 1, channels 0 and 1 will operate as memory-to-memory transfer channels. Channel 0 forms the source address and channel 1 forms the destination address. The channel 1 word count is used. A memory-to-memory transfer is initiated by setting a software DMA request for channel 0. Block Transfer Mode should be used for memory-to-memory. When channel 0 is programmed for a fixed source address, a single source word may be written into a block of memory.

When setting up the Am9517A for memory-to-memory operation, it is suggested that both channels 0 and 1 be masked out.

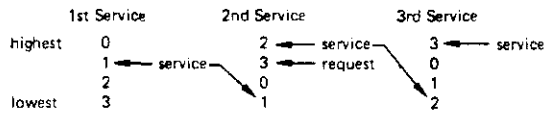
Further, the channel 0 word count should be initialized to the same value used in channel 1. No DACK outputs will be active during memory-to-memory transfers.

The Am9517A will respond to external $\overline{EOP}$ signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers may be found in Timing Diagram 4.

Autointialize: By programming a bit in the Mode register a channel may be set up for an Autoinitialize operation. During Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set by $\overline{EOP}$ when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to repeat its service without CPU intervention.

***Priority**: The Am9517A has two types of priority encoding* available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others *rotating accordingly. With Rotating Priority in a single chip* DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.



The priority encoder selects the highest priority channel requesting service on each active-going HACK edge. Once a channel is started, its operation will not be suspended if a request is received by a higher priority channel. The high priority channel will only gain control after the lower priority channel releases HREQ. When control is passed from one channel to another, the CPU will always gain bus control. This ensures generation of rising HACK edge to be used to initiate selection of the new highest-priority requesting channel.

Compressed Timing: In order to achieve even greater throughput where system characteristics permit, the Am9517A can compress the transfer time to two clock cycles. From Timing Diagram 3 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Timing Diagram 6.

Extended Write: For Flyby Transactions late write is normally used, as this allows sufficient time for the $\overline{IOR}$ signal to get data from the peripheral onto the bus before $\overline{MEMW}$ is activated. In some systems, performance can be improved by starting the write cycle earlier. This is especially true for memory-to-memory *transactions*.

Address Generation: In order to reduce pin count, the Am9517A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a 3-state enable. The lower order address bits are output by the Am9517A directly. Lines A0-A7 should be connected to the address bus. Timing Diagram 3 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode services which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the Am9517A executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

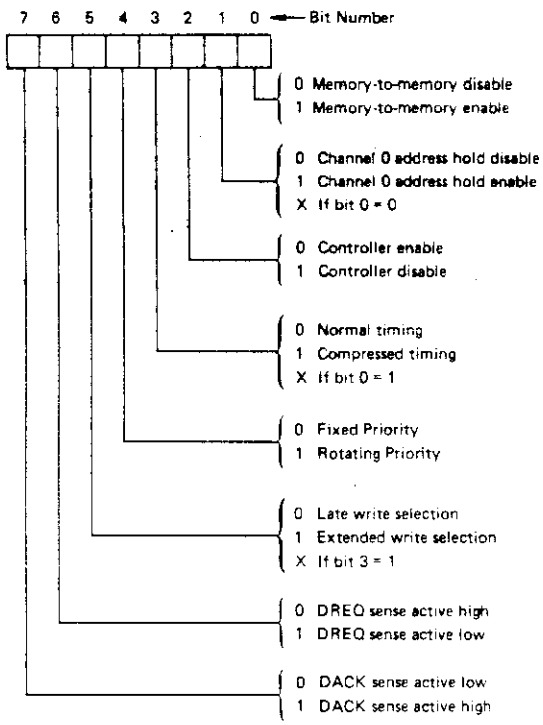
REGISTER DESCRIPTION

Current Address Register: Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialization takes place only after an $\overline{EOP}$.

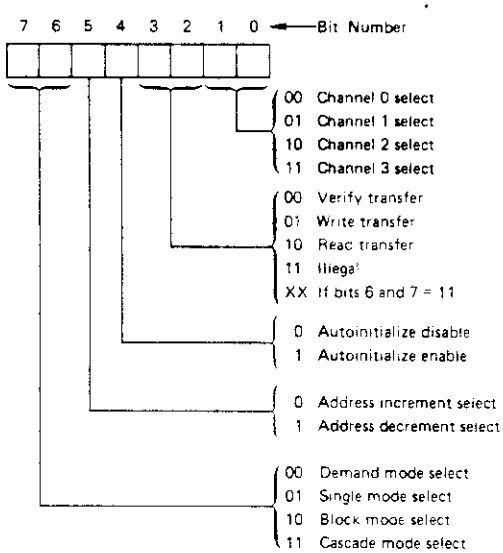
Current Word Count Register: Each channel has a 16-bit Current Word Count register. This register should be programmed with, and will return on a CPU read, a value one less than the number of words to be transferred. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize can occur only when an $\overline{EOP}$ *occurs. Note that the contents of the Word Count register will be* FFFF (hex) following on internally generated $\overline{EOP}$.

Base Address and Base Word Count Registers: Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original values of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes during DMA programming by the microprocessor. Accordingly, writing to these registers when intermediate values are in the Current registers will overwrite the intermediate values. The Base registers cannot be read by the microprocessor.

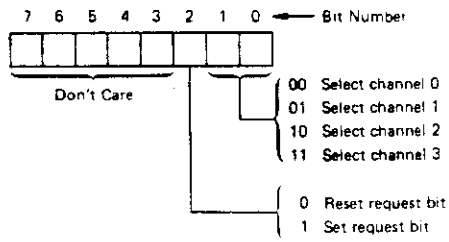
Command Register: This 8-bit register controls the operation of the Am9517A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset. The following table lists the function of the command bits. See Figure 4 for address coding.



Mode Register: Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register it to be written.

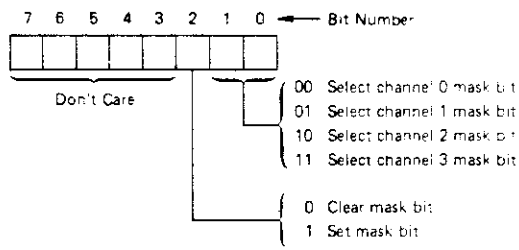


Request Register: The Am9517A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 4 for address coding.

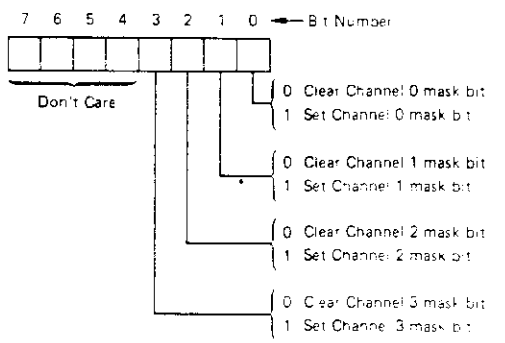


Software requests will be serviced only if the channel is in Block mode. When initiating a memory-to-memory transfer, the software request for channel 0 should be set.

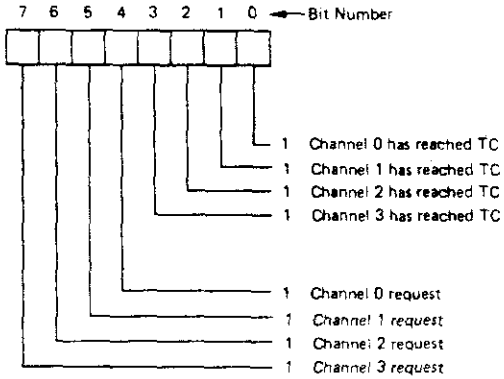
Mask Register: Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 4 for instruction addressing.



All four bits of the Mask Register may also be written with a single command.



Status Register: The Status registers may be read out of the Am9517A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set each time a TC is reached by that channel, including after each Autoinitialization. These bits are cleared by Reset and each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.



Temporary Register: The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands: There are two special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The two software commands are:

Clear First/Last Flip/Flop: This command may be issued prior to writing or reading Am9517A address or word count information. This initializes the Flip/Flop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence. When the Flip/Flop is cleared it addresses the lower byte and when set it addresses the upper byte.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary and Internal First/Last Flip/Flop registers are cleared and the Mask register is set. The Am9517A will enter the Idle cycle.

Figure 4 lists the address codes for the software commands

Figure 4. Register and Function Addressing.

Interface Signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Illegal
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Figure 5. Word Count and Address Register Command Codes.

Channel	Register	Operation	Signals							Internal Flip/Flop	Data Bus DB0–DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base & Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base & Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base & Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base & Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65 to −150°C
VCC with Respect to VSS	−0.5 to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	T_A	V_{CC}
Am9517ADC/PC	0 to +70°C	5.0V ±5%
Am9517A-1DC/PC	0 to +70°C	5.0V ±5%
Am9517A-4DC/PC	0 to +70°C	5.0V ±5%
Am9517A-5DC/PC	0 to +70°C	5.0V ±5%
Am9517ADI	−40 to +85°C	5.0V ±10%
Am9517A-1DI	−40 to +85°C	5.0V ±10%
Am9517A-4DI	−40 to +85°C	5.0V ±10%
Am9517ADMB	−55 to +125°C	5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
VOH	Output HIGH Voltage	IOH = −200μA	2.4			Volts
		IOH = −100μA, (HREQ Only)	3.3			
VOL	Output LOW Voltage	IOL = 3.2mA			0.45	Volts
VIH	Input HIGH Voltage		2.0		VCC+0.5	Volts
VIL	Input LOW Voltage		−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VI ≤ VCC	−10		+10	μA
IOZ	Output Leakage Current	VCC ≤ VO ≤ VSS+.40	−10		+10	μA
ICC	VCC Supply Current	T_A = +25°C		65	130	mA
		T_A = 0°C		75	150	
		T_A = −55°C			175	
CO	Output Capacitance	fc = 1.0MHz, Inputs = 0V		4	8	pF
CI	Input Capacitance			8	15	pF
CIO	I/O Capacitance			10	18	pF

NOTES:

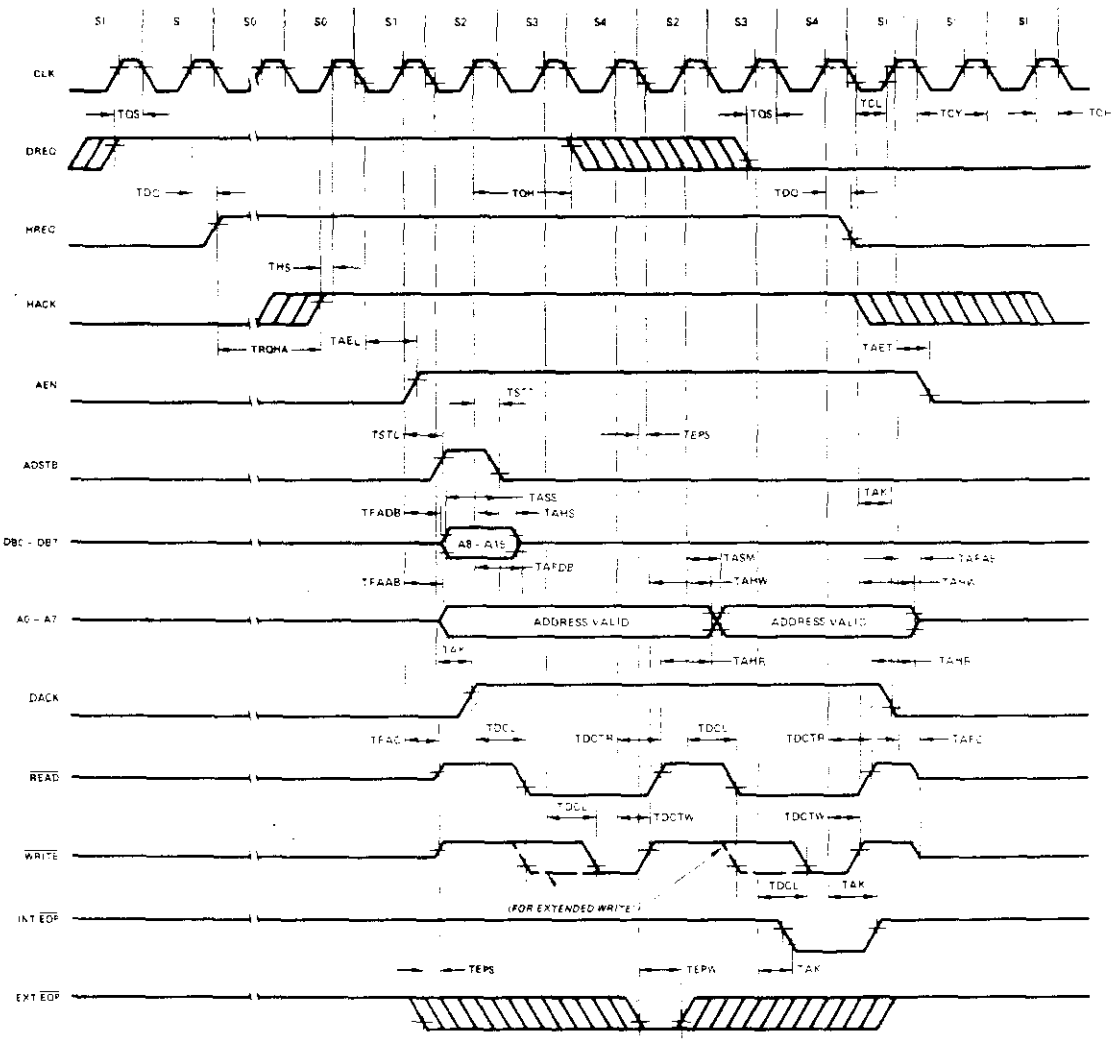
1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. Input timing parameters assume transition times of 20ns or less. Waveform measurement points for both input and output signals are 2.0V for High and 0.8V for Low, unless otherwise noted.
3. Output loading is 1 Standard TTL gate plus 50pF capacitance unless noted otherwise.
4. The new $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be TCY-100ns and for extended write will be 2TCY-100ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY-50ns and for compressed read will be TCY-50ns.
5. TDQ is specified for two different output HIGH levels. TDQ1 is measured at 2.0V. TDQ2 is measured at 3.3V. The value for TDQ2 assumes an external 3.3kΩ pull-up resistor connected from HREQ to VCC.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. Output loading on the data bus is 1 Standard TTL gate plus 15pF for the minimum value and 1 Standard TTL gate plus 100pF for the maximum value.
9. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 600ns for the Am9517A or Am9517A-1, at least 450ns for the Am9517A-4 and 400ns for the Am9517A-5 as recovery time between active read or write pulses.
10. Parameters are listed in alphabetical order.
11. Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. Alternatively, pin 5 may be tied to VCC.
12. Signals $\overline{READ}$ and $\overline{WRITE}$ refer to $\overline{IOR}$ and $\overline{MEMW}$ respectively for peripheral-to-memory DMA operations and to $\overline{MEMR}$ and $\overline{IOW}$ respectively for memory-to-peripheral DMA operations.
13. If N wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by N (TCY).

Am9517A
SWITCHING CHARACTERISTICS
ACTIVE CYCLE (Notes 2, 3, 10, 11 and 12)

Parameters	Description	Am9517A Min	Am9517A Max	Am9517A-1 Min	Am9517A-1 Max	Am9517A-4 Min	Am9517A-4 Max	Am9517A-5 Min	Am9517A-5 Max	Units
TAEL	AEN HIGH from CLK LOW (S1) Delay Time		300		300		225		200	ns
TAET	AEN LOW from CLK HIGH (S1) Delay Time		200		200		150		130	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		150		150		120		90	ns
TAFC	$\overline{READ}$ or $\overline{WRITE}$ Float from CLK HIGH		150		150		120		120	ns
TAFDB	DB Active to Float Delay from CLK HIGH		250		250		190		170	ns
TAHR	ADR from $\overline{READ}$ HIGH Hold Time	TCY-100		TCY-100		TCY-100		TCY-100		ns
TAHS	DB from ADSTB LOW Hold Time	50		50		40		30		ns
TAHW	ADR from WRITE HIGH Hold Time	TCY-50		TCY-50		TCY-50		TCY-50		ns
TAK	DACK Valid from CLK LOW Delay Time		280		280		220		170	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time		250		250		190		170	ns
	$\overline{EOP}$ LOW to CLK HIGH Delay Time		250		250		190		100	ns
TASM	ADR Stable from CLK HIGH		250		250		190		170	ns
TASS	DB to ADSTB LOW Setup Time	100		100		100		100		ns
TCH	Clock High Time (Transitions ≤ 10ns)	120		120		100		80		ns
TCL	Clock Low Time (Transitions ≤ 10ns)	150		150		110		68		ns
TCY	CLK Cycle Time	320		320		250		200		ns
TDCL	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay (Note 4)		270		270		200		190	ns
TDCTR	$\overline{Read}$ HIGH from CLK HIGH (S4) Delay Time (Note 4)		270		270		210		190	ns
TDCTW	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay Time (Note 4)		200		200		150		130	ns
TDQ1	HREQ Valid from CLK HIGH Delay Time (Note 5)		160		160		120		120	ns
TDQ2			250		250		190		120	ns
TEPS	$\overline{EOP}$ LOW from CLK LOW Setup Time	60		60		45		40		ns
TEPW	$\overline{EOP}$ Pulse Width	300		300		225		220		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		250		250		190		170	ns
TFAC	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH		200		200		150		150	ns
TFADB	DB Float to Active Delay from CLK HIGH		300		300		225		200	ns
THS	HACK Valid to CLK HIGH Setup Time	100		100		75		75		ns
TIDH	Input Data from $\overline{MEMR}$ HIGH Hold Time	0		0		0		0		ns
TIDS	Input Data to $\overline{MEMR}$ HIGH Setup Time	250		250		190		170		ns
TODH	Output Data from $\overline{MEMW}$ HIGH Hold Time	20		20		20		10		ns
TODV	Output Data Valid to $\overline{MEMW}$ HIGH (Note 13)	200		200		125		125		ns
TQS	DREQ to CLK LOW (S1, S4) Setup Time	120		0		0		0		ns
TRH	CLK to READY LOW Hold Time	20		20		20		20		ns
TRS	READY to CLK LOW Setup Time	100		100		60		60		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		200		200		150		130	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		140		140		110		90	ns
TQH	DREQ from DACK Valid Hold Time	0		0		0		0		ns
TRQHA	HREQ to HACK Delay Time	1		1		1		1		clk

SWITCHING WAVEFORMS

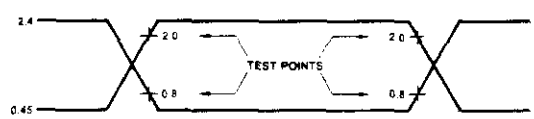
Timing Diagram 1. Active Cycle Timing Diagram



Note: EOP must precede AEN in single transfer mode.

030408-4

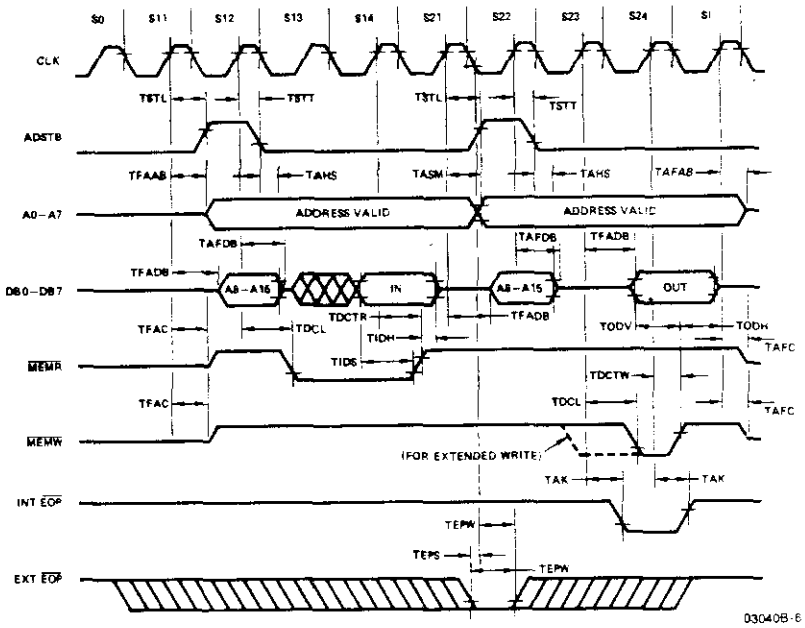
INPUT WAVEFORMS FOR AC TESTS



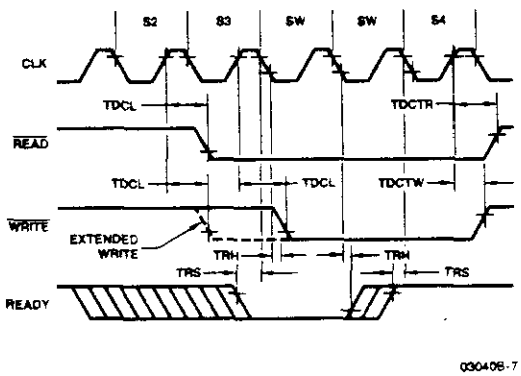
030408-5

SWITCHING WAVEFORMS (Cont.)

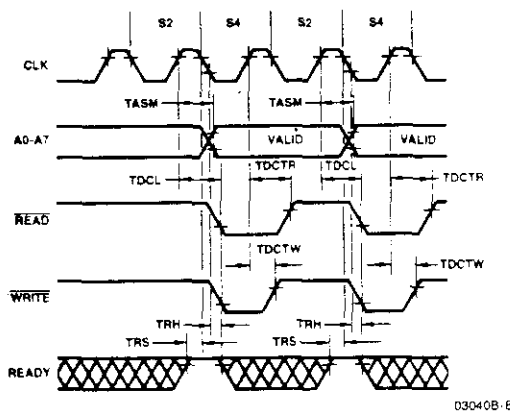
Timing Diagram 2. Memory-to-Memory



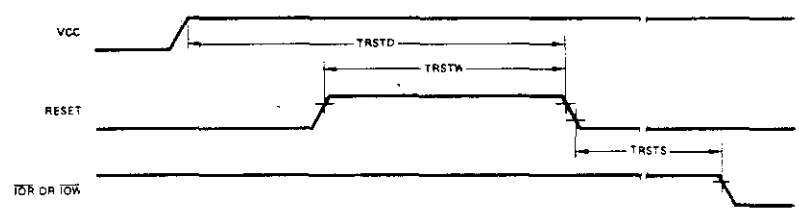
Timing Diagram 3. Ready Timing



Timing Diagram 4. Compressed Timing



Timing Diagram 5. Reset Timing



SWITCHING CHARACTERISTICS

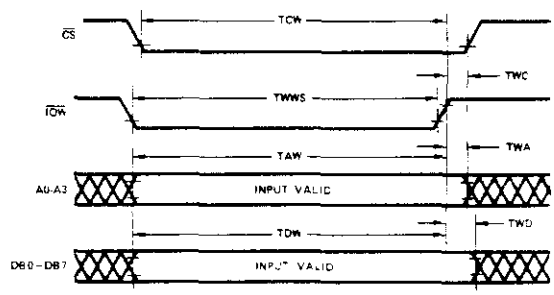
PROGRAM CONDITION (IDLE CYCLE)

(Notes 2, 3, 10, and 11)

Parameters	Description	Am9517A Min	Am9517A Max	Am9517A-1 Min	Am9517A-1 Max	Am9517A-4 Min	Am9517A-4 Max	Am9517A-5 Min	Am9517A-5 Max	Units
TAR	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50		50		50		50		ns
TAW	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	200		200		150		130		ns
TCW	CS LOW to $\overline{WRITE}$ HIGH Setup Time	200		200		150		130		ns
TDW	Data Valid to $\overline{WRITE}$ HIGH Setup Time	200		200		150		130		ns
TRA	ADR or CS Hold from $\overline{READ}$ HIGH	0		0		0		0		ns
TRDE	Data Access from $\overline{READ}$ LOW (Note 8)		300		200		200		140	ns
TRDF	DB Float Delay from $\overline{READ}$ HIGH	20	150	20	100	20	100	0	70	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		500		500		500		ns
TRSTS	RESET to First $\overline{IOWR}$	2TCY		2TCY		2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		300		300		ns
TRW	$\overline{READ}$ Width	300		300		250		200		ns
TWA	ADR from $\overline{WRITE}$ HIGH Hold Time	20		20		20		20		ns
TWC	CS HIGH from $\overline{WRITE}$ HIGH Hold Time	20		20		20		20		ns
TWD	Data from $\overline{WRITE}$ HIGH Hold Time	30		30		30		30		ns
TWWS	Write Width	200		200		200		160		ns

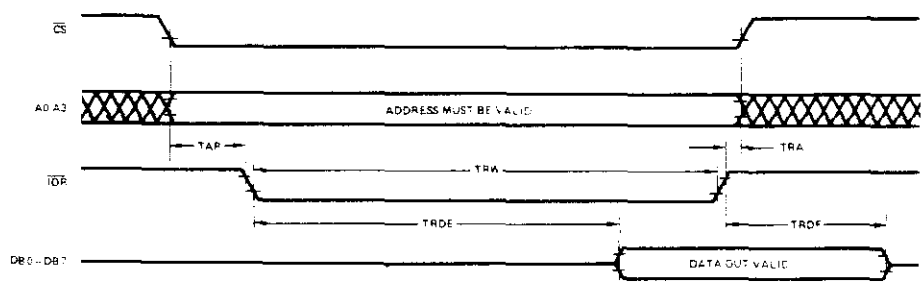
SWITCHING WAVEFORMS (Cont.)

Timing Diagram 6. Program Condition Write Timing (Note 9)



030408-10

Timing Diagram 7. Program Condition Read Cycle (Note 9)

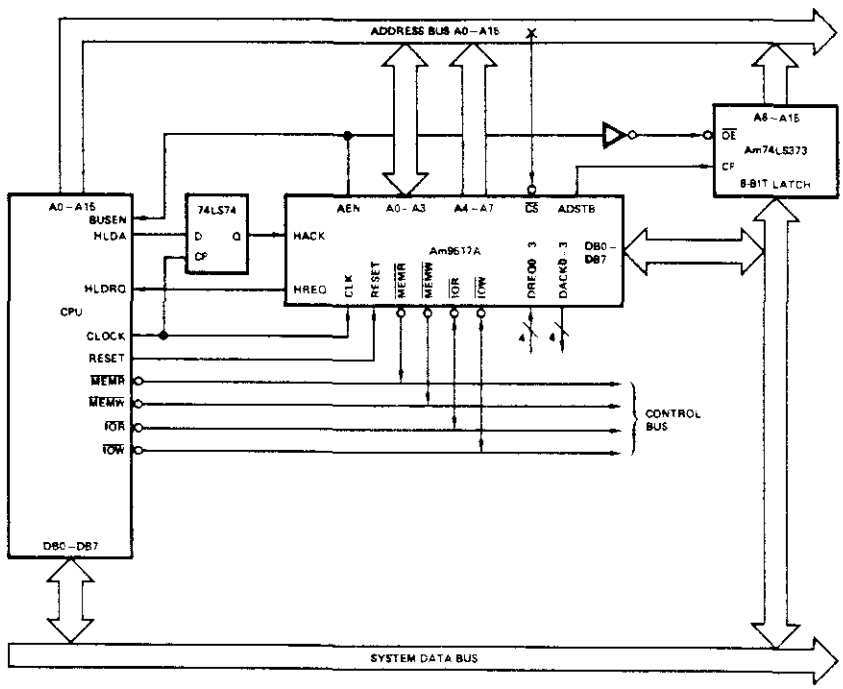


030408-11

APPLICATION INFORMATION

Figure 6 shows a convenient method for configuring a DMA system with the Am9517A Controller and a microprocessor system. The Multimode DMA Controller issues a Hold Request to the processor whenever there is at least one valid DMA Request from a peripheral device. When the processor replies with a Hold Acknowledge signal, the Am9517A takes control of the Address Bus, the Data Bus and the Control Bus. The address for the first transfer operation comes out in two bytes – the least significant eight bits on the eight Address outputs and the most significant eight bits on the Data Bus. The contents of the Data Bus are then latched into the Am74LS373 register to complete the full 16 bits of the Address Bus. The Am74LS373 is a high speed, low power, 8-bit, 3-state register in a 20-pin package. After the initial transfer takes place, the register is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are provided when one Am9517A is used.

Figure 6. Basic DMA Configuration.



030408-12

Am9519A

Universal Interrupt Controller

DISTINCTIVE CHARACTERISTICS

- Eight individually maskable interrupt inputs reduce CPU overhead
- Unlimited interrupt channel expansion with no extra hardware
- Programmable 1-to 4-byte response provides vector address and message protocol for 8-bit CPUs
- Rotating and fixed priority resolution logic
- Software interrupt request capability
- Common vector and polled mode options
- Automatic hardware clear of in-service interrupts reduces software overhead
- Polarity control of interrupt inputs and outputs
- Reset minimizes software initialization by automatically generating CALL to location zero

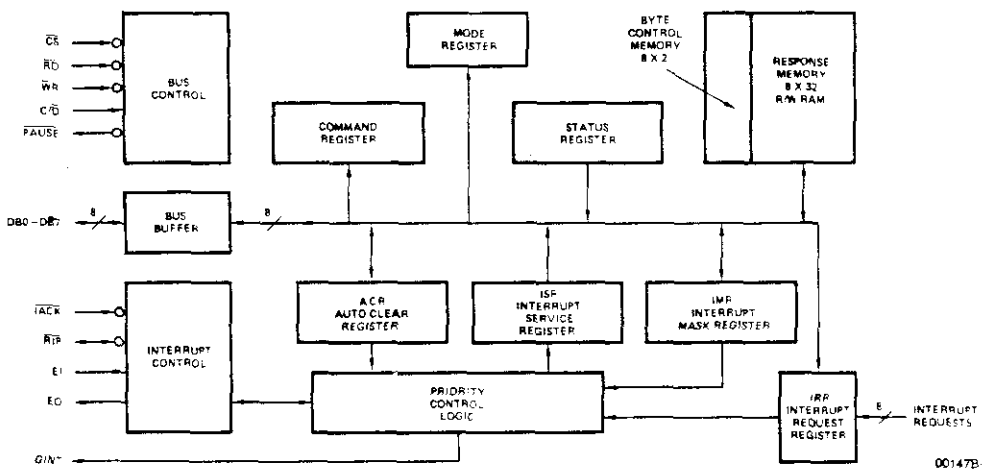
GENERAL DESCRIPTION

The Am9519A Universal Interrupt Controller is a processor support circuit that provides a powerful interrupt structure to increase the efficiency and versatility of microcomputer-based systems. *A single Am9519A manages up to eight* maskable interrupt request inputs, resolves priorities and supplies up to four bytes of fully programmable response for each interrupt. *It uses a simple expansion structure that* allows many units to be cascaded for control of large numbers of interrupts. Several programmable control features are provided to enhance system flexibility and optimization.

The Universal Interrupt Controller is designed with a general purpose interface to facilitate its use with a wide range of digital systems, including most popular 8-bit microprocessors. Since the response bytes are fully programmable, any instruction or vectoring protocol appropriate for the host processor may be used.

When the Am9519A controller receives an unmasked Interrupt Request, it issues a Group Interrupt output to the CPU. When the interrupt is acknowledged, the controller outputs the one-to-four byte response associated with the highest priority unmasked interrupt request. The ability of the CPU to set interrupt requests under software control permits hardware prioritization of software tasks and aids system diagnostic and maintenance procedures.

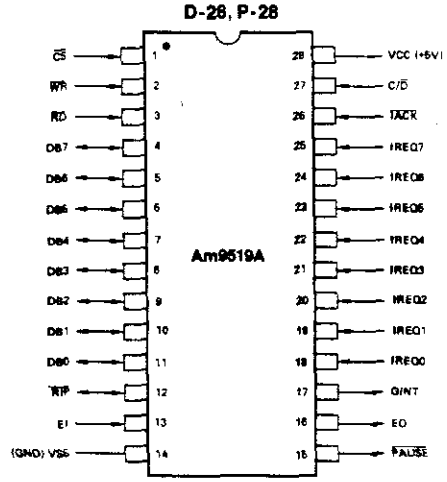
BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Ambient Temperature	Timing Options	
Molded DIP	0°C ≤ T_A ≤ +70°C	Am9519APC	Am9519A-1PC
Hermetic DIP		Am9519ADC	Am9519A-1DC
Hermetic DIP	−40°C ≤ T_A ≤ +85°C	Am9519ADI	
Hermetic DIP	−55°C ≤ T_A ≤ +125°C	Am9519ADMB	

CONNECTION DIAGRAM – Top View
D-28, P-28



Top View

Pin 1 is marked for orientation. 001478-2

INTERFACE SIGNAL DESCRIPTION

VCC: +5 Volt Power Supply
VSS: Ground

DB0 – DB7 (Data Bus, Input/Output)

The eight bidirectional data bus signals are used to transfer information between the Am9519A and the system data bus. The direction of transfer is controlled by the $\overline{IACK}$, $\overline{WR}$ and $\overline{RD}$ input signals. Programming and control information are written into the device; status and response data are output by it.

$\overline{CS}$ (Chip Select, Input)

The active low Chip Select input enables read and write operations on the data bus. Interrupt acknowledge responses are not conditioned by $\overline{CS}$.

$\overline{RD}$ (Read, Input)

The active low Read signal is conditioned by $\overline{CS}$ and indicates that information is to be transferred from the Am9519A to the data bus.

$\overline{WR}$ (Write, Input)

The active low Write signal is conditioned by $\overline{CS}$ and indicates that data bus information is to be transferred from the data bus to a location within the Am9519A.

C/$\overline{D}$ (Control/Data, Input)

The C/$\overline{D}$ control signal selects source and destination locations for data bus read and write operations. Data read or write transfers are made to or from preselected internal registers or memory locations. Control write operations load the command register and control read operations output the status register.

IREQ0 – IREQ7 (Interrupt Request, Input)

The Interrupt Request signals are used by external devices to indicate that service by the host CPU is desired. IREQ inputs are accepted asynchronously and they may be programmed for either a high-to-low or low-to-high edge transition. Active inputs are latched internally in the Interrupt Request Register. After the IRR bit is cleared, an IREQ transition of the programmed polarity must occur to initiate another request.

$\overline{RIP}$ (Response In Process, Input/Output)

Response In Process is a bidirectional signal used when two or more Am9519A circuits are cascaded. It permits multibyte response transfers to be completed without interference from higher priority interrupts. An Am9519A that is responding to an acknowledged interrupt will treat $\overline{RIP}$ as an output and hold it low until the acknowledge response is finished. An Am9519A without an acknowledged interrupt will treat $\overline{RIP}$ as an input and will ignore $\overline{IACK}$ pulses as long as $\overline{RIP}$ is low. The $\overline{RIP}$ output is open drain and requires an external pullup resistor to VCC.

$\overline{IACK}$ (Interrupt Acknowledge, Input)

The active low Interrupt Acknowledge line indicates that the external system is asking for interrupt response information. Depending on the programmed state of the Am9519A, it will accept 1, 2, 3 or 4 $\overline{IACK}$ pulses; one response byte is transferred per pulse. The first $\overline{IACK}$ pulse causes selection of the highest priority unmasked pending interrupt request and generates a $\overline{RIP}$ output signal.

$\overline{PAUSE}$ (Pause, Output)

The active-low Pause signal is used to coordinate interrupt responses with data bus and control timing. Pause goes low when the first $\overline{IACK}$ is received and remains low until $\overline{RIP}$ goes low. The external system can use Pause to stretch the acknowledge cycle and allow the control timing to automatically adjust to the actual priority resolution delays in the interrupt system. Second, third and fourth response bytes do not cause Pause to go low. Pause is an open drain output and requires an external pullup resistor to VCC.

EO (Enable Out, Output)

The active high EO signal is used to implement daisy-chained cascading of several Am9519A circuits. EO is connected to the EI input of the next lower priority chip. On receipt of an interrupt acknowledge, each EO will go inactive until it has been determined that no valid interrupt request is pending on that chip. If an active request is present, EO remains low. EO is also held low when the master mask bit is active, thus disabling all lower priority chips.

EI (Enable In, Input)

The active high EI signal is used to implement daisy-chained cascading of several Am9519A circuits. EI is connected to EO of the next higher priority chip. It may also be used as a hardware disable input for the interrupt system. When EI is low $\overline{IACK}$ inputs will not affect ISR, however. $\overline{PAUSE}$ will go low until $\overline{RIP}$ goes low. EI is internally pulled up to VCC so that no external pullup is needed when EI is not used.

GINT (Group Interrupt, Output)

The Group Interrupt output signal indicates that at least one unmasked interrupt request is pending. It may be programmed for active high or active low polarity. When active low, the output is open drain and requires an external pull up resistor to VCC. Since a glitch on GINT occurs approximately 100nsec after the last IACK pulse this pin should not be connected to edge sensitive devices.

REGISTER DESCRIPTION

Interrupt Request Register (IRR): The 8-bit IRR is used to store pending interrupt requests. A bit in the IRR is set whenever the corresponding IREQ input goes active. Bits may also be set under program control from the CPU, thus permitting software generated interrupts. IRR bits may be cleared under program control. An IRR bit is automatically cleared when its interrupt is acknowledged. All IRR bits are cleared by a reset function.

Interrupt Service Register (ISR): The 8-bit ISR contains one bit for each IREQ input. It is used to indicate that a pending interrupt has been acknowledged and to mask all lower priority interrupts. When a bit is set by the acknowledge logic in the ISR, the corresponding IRR bit is cleared. If an acknowledged interrupt is not programmed to be automatically cleared, its ISR bit must be cleared by the CPU under program control when it is desired to permit interrupts from lower priority devices. When the interrupt is programmed for automatic clearing, the ISR bit is automatically reset during the acknowledge sequence. All ISR bits are cleared by a reset function.

Interrupt Mask Register (IMR): The 8-bit IMR is used to enable or disable the individual interrupt inputs. The IMR bits correspond to the IREQ inputs and all eight may be loaded, set or cleared in parallel under program control. In addition, individual IMR bits may be set or cleared by the CPU. Care must be taken therefore when disabling a specific channel by setting its IMR bit. If that bit is causing the GINT pin to be active a lock-up condition can occur if the CPU recognizes the interrupt and then the Am9519A removes the request. During the $\overline{IACK}$ cycle $\overline{PAUSE}$ will go low and stay low. The solution is to disable CPU interrupts prior to writing to the IMR and then re-enable them. A reset function will set all eight mask bits, disabling all requests. A mask bit that is set does not disable the IRR, and an IREQ that arrives while a corresponding mask bit is set will cause an interrupt later when the mask bit is cleared. Only unmasked interrupt inputs can generate a Group Interrupt output.

Response Memory: An 8 x 32 read/write response memory is included in the Am9519A. It is used to store up to four bytes of response information for each of the eight interrupt request inputs. All bits in the memory are programmable, allowing any desired vector, opcode, instruction or other data to be entered. The Am9519A transfers the interrupt response information for the highest priority unmasked interrupt from the memory to the data bus when the $\overline{IACK}$ input is active.

Auto Clear Register: The 8-bit Auto Clear register contains one bit for each IREQ input and specifies the operating mode for each of the ISR bits. When an auto clear bit is off, the corresponding ISR bit is set when that interrupt is acknowledged and is cleared by software command. When an auto clear bit is on, the corresponding ISR bit is cleared by the hardware by the rising edge of the last acknowledge pulse. A reset function clears all auto clear bits.

Status Register: The 8-bit Status register contains information concerning the internal state of the chip. It is especially useful when operating in the polled mode in order to identify interrupting devices. Figure 1 shows the status register bit assignments. The polarity of the GINT bit 7 is not affected by the GINT polarity control (Mode bit status register bit assignments. Bits S0-S2 are set asynchronously to a status register read operation. It is recommended to read the register twice and to compare the binary vectors for equality prior to the proceeding with device service in polled mode. The polarity of the GINT bit 7 is not affected by the GINT polarity control (Mode bit 3). The Status register is read by executing a read operation ($\overline{CS}$ = 0, RS = 0) with the control location selected (C/$\overline{D}$ = 1).

Mode Register: The 8-bit Mode register controls the operating options of the Am9519A. Figure 2 shows the bit assignments for the Mode register. The five low order mode bits (0 through 4) are loaded in parallel by command. Bits 5, 6 and 7 are controlled by separate commands. (See Figure 4.) The Mode register cannot be read out directly to the data bus, but Mode bits 0, 2 and 7 are available as part of the Status register.

Command Register: The 8-bit Command register stores the last command entered. Depending upon the command opcode, it may initiate internal actions or precondition the part for subsequent data bus transfers. The Command register is loaded by executing a write operation ($\overline{WR}$ = 0) with the control location selected (C/$\overline{D}$ = 1), as shown in Figure 3.

Byte Count Register: The length in bytes of the response associated with each interrupt is independently programmed so that different interrupts may have different length responses. The byte count for each response is stored in eight 2-bit Byte Count registers. For a given interrupt the Am9519A will expect to receive a number of $\overline{IACK}$ pulses that equals the corresponding byte count, and will hold RIP low until the count is satisfied.

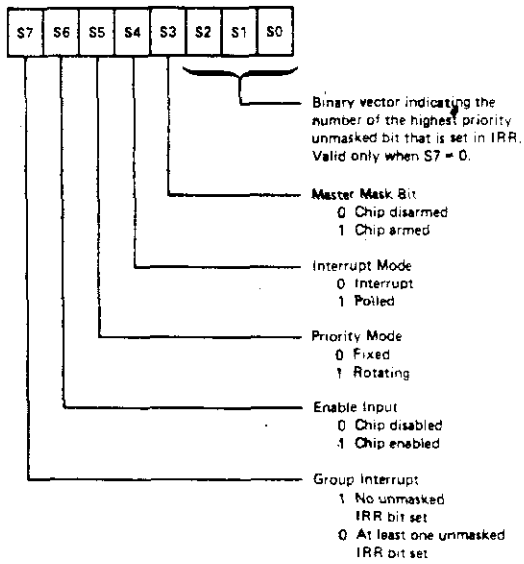


Figure 1. Status Register Bit Assignments. 00147B-3

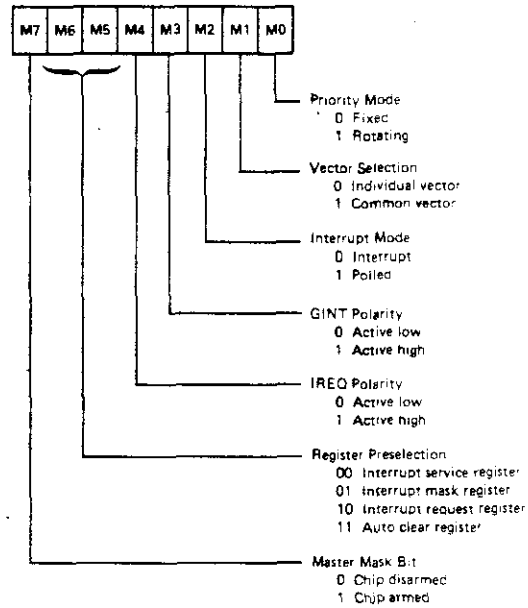


Figure 2. Mode Register Bit Assignments. 00147B-4

FUNCTIONAL DESCRIPTION

Interrupts are used to improve system throughput and response time by eliminating heavy dependence on software polling procedures. Interrupts allow external devices to asynchronously modify the instruction sequence of a program being executed. In systems with multiple interrupts, vectoring can further improve performance by allowing direct identification of the interrupting device and its associated service routine. The Am9519A Universal Interrupt Controller contains, on one chip, all of the circuitry necessary to detect, prioritize and manage eight vectored interrupts. It includes many options and operating modes that permit the design of sophisticated interrupt systems.

Reset

The reset function is accomplished by software command or automatically during power-up. The reset command may be issued by the CPU at any time. Internal power up circuitry is triggered when VCC reaches a predetermined threshold, causing a brief internal reset pulse. In both cases, the resulting internal state of the machine is that all registers are cleared except the Mask register which is set. Thus no Group Interrupt will be generated and no interrupt requests will be recognized. The response memory and Byte Count registers are not affected by reset. Their contents after power-up are unpredictable and must be established by the host CPU during initialization.

Operating Sequence

A brief description of a typical sequence of events in an operating interrupt system will illustrate the general interactions among the host CPU, the interrupt controller and the interrupting peripheral.

1. The Am9519A controller is initialized by the CPU in order to customize its configuration and operation for the application at hand. Both the controller and the CPU are then enabled to accept interrupts.
2. One (or more) of the interrupt request inputs to the controller becomes active indicating that peripheral equipment is asking for service. The controller asynchronously accepts and latches the request(s).
3. If the request is masked, no further action takes place. If the request is not masked, a Group Interrupt output is generated by the controller.
4. The GINT signal is recognized by the CPU which normally will complete the execution of the current instruction, insert an interrupt acknowledge sequence into its instruction execution stream, and disable its internal interrupt structure. The controller expects to receive one or more $\overline{IACK}$ signals from the CPU during the acknowledge sequence.
5. When the controller receives the $\overline{IACK}$ signal, it brings $\overline{PAUSE}$ low and selects the highest priority unmasked pending request. When selection is complete, the $\overline{RIP}$ output is brought low and the first byte in the response memory associated with the selected request is output on the data bus. $\overline{PAUSE}$ stays low until RIP goes low. $\overline{RIP}$ stays low until the last byte of the response has been transferred.
6. During the acknowledge sequence, the IRR bit corresponding to the selected request is automatically cleared, and the corresponding ISR bit is set by the falling edge of $\overline{IACK}$. When the ISR bit is set, the Group Interrupt output is disabled until a higher priority request arrives or the ISR bit is cleared. The ISR bit will be cleared by either hardware or software.
7. If a higher priority request arrives while the current request is being serviced, GINT will be output by the controller, but will be recognized and acknowledged only if the CPU has its interrupt input enabled. If acknowledged, the corresponding higher priority ISR bit will be set and the requests nested.

Information Transfers

Figure 3 shows the control signal configurations for all information transfer operations between the Am9519 and the data bus. The following conventions are assumed: $\overline{RD}$ and $\overline{WR}$ active are mutually exclusive; $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ have no meaning unless $\overline{CS}$ is low; active $\overline{IACK}$ pulses occur only when $\overline{CS}$ is high.

For reading, the Status register is selected directly by the C/$\overline{D}$ control input. Other internal registers are read by preselecting the desired register with mode bits 5 and 6, and then executing a data read. The response memory can be read only with $\overline{IACK}$ pulses. For writing, the Command register is selected directly by the C/$\overline{D}$ control input. The Mask and Auto Clear registers are loaded following specific commands to that effect. To load each level of the response memory, the response preselect command is issued to select the desired level. An appropriate number of data write operations are then executed to load that level.

CONTROL INPUT					DATA BUS OPERATION
$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{IACK}$	
0	0	0	1	1	Transfer contents of preselected data register to data bus
0	0	1	0	1	Transfer contents of data bus to preselected data register
0	1	0	1	1	Transfer contents of status register to data bus
0	1	1	0	1	Transfer contents of data bus to command register
1	X	X	X	0	Transfer contents of selected response memory location to data bus
1	X	X	X	1	No information transferred

Figure 3. Summary of Data Bus Transfers.

The Pause output may be used by the host CPU to ensure that proper timing relationships are maintained with the Am9519A when $\overline{IACK}$ is active. The $\overline{IACK}$ pulse width required depends on several variables, including: operating temperature, internal logic delays, number of interrupt controllers chained together, and the priority level of the interrupt being acknowledged. When delays in these variables combine to delay selection of a request following the falling edge of the first $\overline{IACK}$, the Pause output may be used to extend the $\overline{IACK}$ pulse, if necessary. Pause will remain low until a request has been selected, as indicated by the falling edge of $\overline{RIP}$. Typically, the internal interrupt selection process is quite fast, especially for systems with a single Am9519A and Pause will consequently remain low for only a very brief interval and will not cause extension of the IACK timing.

Operating Options

The Mode register specifies the various combinations of operating options that may be selected by the CPU. It is cleared by power-up or by a reset command.

Mode bit 0 specifies the rotating/fixed priority mode (see Figure 2). In the fixed mode, priority is assigned to the request inputs based upon their physical location at the chip interface, with IREQ0 the highest and IREQ7 the lowest. In the rotating mode, relative priority is the same as for the fixed mode and the most recently serviced request is assigned the lowest priority. In the fixed mode, a lower priority request might never receive service if enough higher priority requests are active. In the rotating mode, any request will receive service within a maximum of seven other service cycles no matter what pattern the request inputs follow.

Mode bit 1 selects the individual/common vector option. Individual vectoring provides a unique location in the response memory for each interrupt request. The common vector option always supplies the response associated with IREQ0 no matter which request is being acknowledged.

Mode bit 2 specifies interrupt or polled operation. In the polled mode the Group Interrupt output is disabled. The CPU may read the Status register to determine if a request is pending. Since $\overline{IACK}$ pulses are not normally supplied in polled mode, the IRR bit is not automatically cleared, but may be cleared by command. With no $\overline{IACK}$ input the ISR and the response memory are not used. An Am9519A in the polled mode has EI connected to EO so that in multichip interrupt systems the polled chip is functionally removed from the priority hierarchy.

Mode bit 3 specifies the sense of the GINT output. When active high polarity is selected the output is a two-state configuration. For active low polarity, the output is open drain and requires an external pull-up resistor to provide the high logic level. The open drain output allows wired-or configurations with other similar output signals.

Mode bit 4 specifies the sense of the IREQ inputs. When active low polarity is selected, the IRR responds to falling edges on the request inputs. When active high is selected, the IRR responds to rising edges.

Mode bits 5 and 6 specify the register that will be read on subsequent data read operations (C/$\overline{D}$ = 0, $\overline{RD}$ = 0). This preselection remains valid until changed by a reset or a command.

Mode bit 7 is the master mask bit that disables all request inputs. It is used to disable all interrupts without modifying the IMR so that the previous IMR contents are valid when interrupts are re-enabled. When the master mask bit is low, it causes the EO line to remain disabled (low). Thus, for multiple-chip interrupt systems, one master mask bit can disable the whole interrupt structure. Alternatively, portions of the structure may be disabled. The state of the master mask bit is available as bit S3 of the Status register.

Programming

After reset, the Am9519A must be initialized by the CPU in order to perform useful work. At a minimum, the master mask bit and at least one of the IMR bits should be enabled. If vectoring is to be used, the response memory must be loaded; if not, the mode must be changed to a non-vectored configuration. Normally, the first step will be to modify the Mode register and the Auto clear register in order to establish the configuration desired for the application. Then the response memory and byte count will be loaded for those request levels that will be in use. The response memory for every channel must be written even if the channel is not used. Every byte need not be written only those specified by the byte count. Finally, the master mask bit and at least portions of the IMR will be enabled to allow interrupt processing to proceed.

Commands

The host CPU configures, changes and inspects the internal condition of the Am9519A using the set of commands shown in Figure 4. An "X" entry in the table indicates a "don't care" state. All commands are entered by directly loading the Command register as shown in Figure 3 ($C/\overline{D}$ = 1, $\overline{WR}$ = 0). Figure 5 shows the coding assignments for the Byte Count registers. A detailed description of each command is contained in the Am9519A Application Note AMPUB-071.

BY1	BY0	COUNT
0	0	1
0	1	2
1	0	3
1	1	4

Figure 5. Byte Count Coding.

COMMAND CODE								COMMAND DESCRIPTION
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	1	0	X	X	X	Clear all IRR and all IMR bits
0	0	0	1	1	B2	B1	B0	Clear IRR and IMR bit specified by B2, B1, B0
0	0	1	0	0	X	X	X	Clear all IMR bits
0	0	1	0	1	B2	B1	B0	Clear IMR bit specified by B2, B1, B0
0	0	1	1	0	X	X	X	Set all IMR bits
0	0	1	1	1	B2	B1	B0	Set IMR bit specified by B2, B1, B0
0	1	0	0	0	X	X	X	Clear all IRR bits
0	1	0	0	1	B2	B1	B0	Clear IRR bit specified by B2, B1, B0
0	1	0	1	0	X	X	X	Set all IRR bits
0	1	0	1	1	B2	B1	B0	Set IRR bit specified by B2, B1, B0
0	1	1	0	X	X	X	X	Clear highest priority ISR bit
0	1	1	1	0	X	X	X	Clear all ISR bits
0	1	1	1	1	B2	B1	B0	Clear ISR bit specified by B2, B1, B0
1	0	0	M4	M3	M2	M1	M0	Load Mode register bits 0–4 with specified pattern
1	0	1	0	M6	M5	0	0	Load Mode register bits 5, 6 with specified pattern
1	0	1	0	M6	M5	0	1	Load Mode register bits 5, 6 and set mode bit 7
1	0	1	0	M6	M5	1	0	Load Mode register bits 5, 6 and clear mode bit 7
1	0	1	1	X	X	X	X	Preselect IMR for subsequent loading from data bus
1	1	0	0	X	X	X	X	Preselect Auto Clear register for subsequent loading from data bus
1	1	1	BY1	BY0	L2	L1	L0	Load BY1, BY0 into byte count register and preselect response memory level specified by L2, L1, L0 for subsequent loading from data bus

Figure 4. Am9519A Command Summary.

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am9519APC, Am9519ADC	0°C ≤ T_A ≤ 70°C	5.0V ±5%	0V
Am9519A-1PC, Am9519A-1DC			
Am9519ADI	−40°C ≤ T_A ≤ 85°C	5.0V ±10%	0V
Am9519ADMB	−55°C ≤ T_A ≤ 125°C	5.0V ±10%	0V

DC CHARACTERISTICS Over Operating Range (Note 1)

Parameter	Description	Test Conditions		Min	Typ	Max	Units
VOH	Output High Voltage (Note 12)	IOH = −200μA		2.4			Volts
		IOH = −100μA (EO only)		2.4			
VOL	Output Low Voltage	IOL = 3.2mA				0.4	Volts
		IOL = 1.0mA (EO only)				0.4	
VIH	Input High Voltage			2.0		VCC	Volts
VIL	Input Low Voltage			−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VIN ≤ VCC	EI Input	−60		10	μA
			Other Inputs	−10		10	
IOZ	Output Leakage Current	VSS ≤ VOUT ≤ VCC, Output Off		−10		10	μA
ICC	VCC Supply Current	T_A = +25°C			60	125	mA
		T_A = 0°C			100	145	
		T_A = −55°C				200	
CO	Output Capacitance	fc = 1.0MHz				15	pF
CI	Input Capacitance	T_A = 25°C				10	
CIO	I/O Capacitance	All pins at 0V				20	

AC TESTING INPUT, OUTPUT WAVEFORM
Input/Output

AC CHARACTERISTICS Over Operating Range (Notes 2, 3, 4, 5)

Parameters	Description		Am9519A Min	Am9519A Max	Am9519A-1 Min	Am9519A-1 Max	Units
TAVRL	C/$\overline{D}$ Valid and $\overline{CS}$ LOW to Read LOW		0		0		ns
TAVWL	C/$\overline{D}$ Valid and $\overline{CS}$ LOW to Write LOW		0		0		ns
TCLPH	$\overline{RIP}$ LOW to $\overline{PAUSE}$ HIGH (Note 6)		75	375	75	375	ns
TCLQV	$\overline{RIP}$ LOW to Data Out Valid (Note 7)			50		40	ns
TDVWH	Data In Valid to Write HIGH		250		200		ns
TEHCL	Enable in HIGH to $\overline{RIP}$ LOW (Notes 8, 9)		30	300	30	300	ns
TIVGV	Interrupt Request Valid to Group Interrupt Valid		100	800		650	ns
TIVIX	Interrupt Request Valid to Interrupt Request Don't Care (IREQ Pulse Duration)		250		250		ns
TKHCH	$\overline{IACK}$ HIGH to $\overline{RIP}$ HIGH (Note 8)			450		350	ns
TKHKL	$\overline{IACK}$ HIGH to $\overline{IACK}$ LOW ($\overline{IACK}$ Recovery)		500		300		ns
TKHNH	$\overline{IACK}$ HIGH to EO HIGH (Notes 10, 11)			975		750	ns
TKHQX	$\overline{IACK}$ HIGH to Data Out Invalid		20	200	20	100	ns
TKLCL	$\overline{IACK}$ LOW to $\overline{RIP}$ LOW (Note 8, 13)	COM'L	75	600	75	450	ns
		IND	75	600			ns
		MIL	75	650			ns
TKLKH	$\overline{IACK}$ LOW to $\overline{IACK}$ HIGH (1st IACK) (Note 13)		975		800		ns
TKLNL	$\overline{IACK}$ LOW to EO LOW (Notes 10, 11, 13)			125		100	ns
TKLPL	$\overline{IACK}$ LOW to $\overline{PAUSE}$ LOW (Note 13)		25	175	25	125	ns
TKLQV	$\overline{IACK}$ LOW to Data Out Valid (Note 7, 13)		25	300	25	200	ns
TKLQV1	1st $\overline{IACK}$ LOW to Data Out Valid (Note 13)		75	650	75	490	ns
TPHKH	$\overline{PAUSE}$ HIGH to $\overline{IACK}$ HIGH		0		0		ns
TRHAX	Read HIGH to C/$\overline{D}$ and $\overline{CS}$ Don't Care		0		0		ns
TRHQX	Read HIGH to Data Out Invalid		20	200	20	100	ns
TRLQV	Read LOW to Data Out Valid			300		200	ns
TRLQX	Read LOW to Data Out Unknown		50		50		ns
TRLRH	Read LOW to Read HIGH ($\overline{RD}$ Pulse Duration)		300		250		ns
TWHAX	Write HIGH to C/$\overline{D}$ and $\overline{CS}$ Don't Care		25		25		ns
TWHDX	Write HIGH to Data In Don't Care		25		25		ns
TWHRW	Write HIGH to Read or Write LOW (Write Recovery)		600		400		ns
TWLWH	Write LOW to Write HIGH ($\overline{WR}$ Pulse Duration)		300		250		ns

NOTES:

1. Typical values for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. Test conditions assume transition times of 20ns or less, timing reference levels of 0.8V and 2.0V and output loading of one TTL gate plus 100pF, unless otherwise noted.
3. Transition abbreviations used for the switching parameter symbols include: H = High, L = Low, V = Valid, X = unknown or don't care, Z = high impedance.
4. Signal abbreviations used for the switching parameter symbols include: R = Read, W = Write, Q = Data Out, D = Data In, A = Address (CS and C/D), K = Interrupt Acknowledge, N = Enable Out, E = Enable In, P = Pause, C = $\overline{RIP}$.
5. Switching parameters are listed in alphabetical order.
6. During the first $\overline{IACK}$ pulse, $\overline{PAUSE}$ will be low long enough to allow for priority resolution and will not go high until after RIP goes low (TCLPH).
7. TKLQV applies only to second, third and fourth $\overline{IACK}$ pulses while $\overline{RIP}$ is low. During the first $\overline{IACK}$ pulse, Data Out will be valid following the falling edge of $\overline{RIP}$ (TCLQV).
8. $\overline{RIP}$ is pulled low to indicate that an interrupt request has been selected. $\overline{RIP}$ cannot be pulled low until EI is high following an internal delay. TKLCL will govern the falling edge of $\overline{RIP}$ when EI is always high or is high early in the acknowledge cycle. TEHCL will govern when EI goes high later in the cycle. The rising edge of EI will be determined by the length of the preceding priority resolution chain. $\overline{RIP}$ remains low until after the rising edge of the $\overline{IACK}$ pulse that transfers the last response byte for the selected IREQ.
9. Test conditions for the EI line assume timing reference levels of 0.8V and 2.0V with transition times of 10ns or less.
10. Test conditions for the EO line assume output loading of two LS TTL gates plus 30pF and timing reference levels of 0.8V and 2.0V. Since EO normally only drives EI of another Am9519A, higher speed operation can be specified with this more realistic test condition.
11. The arrival of $\overline{IACK}$ will cause EO to go low, disabling additional circuits that may be connected to EO. If no valid interrupt is pending, EO will return high when EI is high. If a pending request is selected, EO will stay low until after the last $\overline{IACK}$ pulse for that interrupt is complete and $\overline{RIP}$ goes high.
12. VOH specifications do not apply to $\overline{RIP}$ or to $\overline{GINT}$ when active-low. These outputs are open-drain and VOH levels will be determined by external circuitry.
13. $\overline{CS}$ must be High for at least 100ns prior to $\overline{IACK}$ going Low.

APPLICATIONS

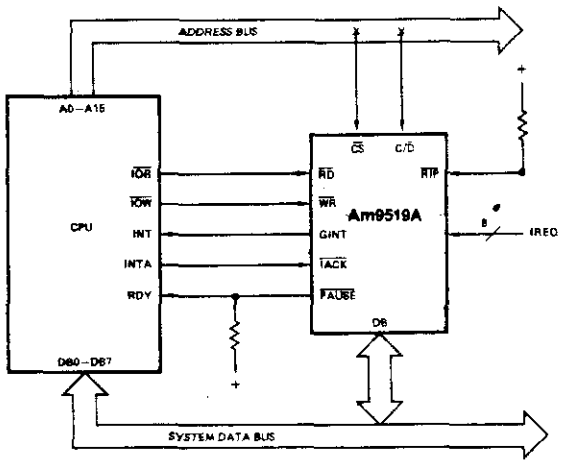


Figure 6. Base Interrupt System Configuration.

00147B-8

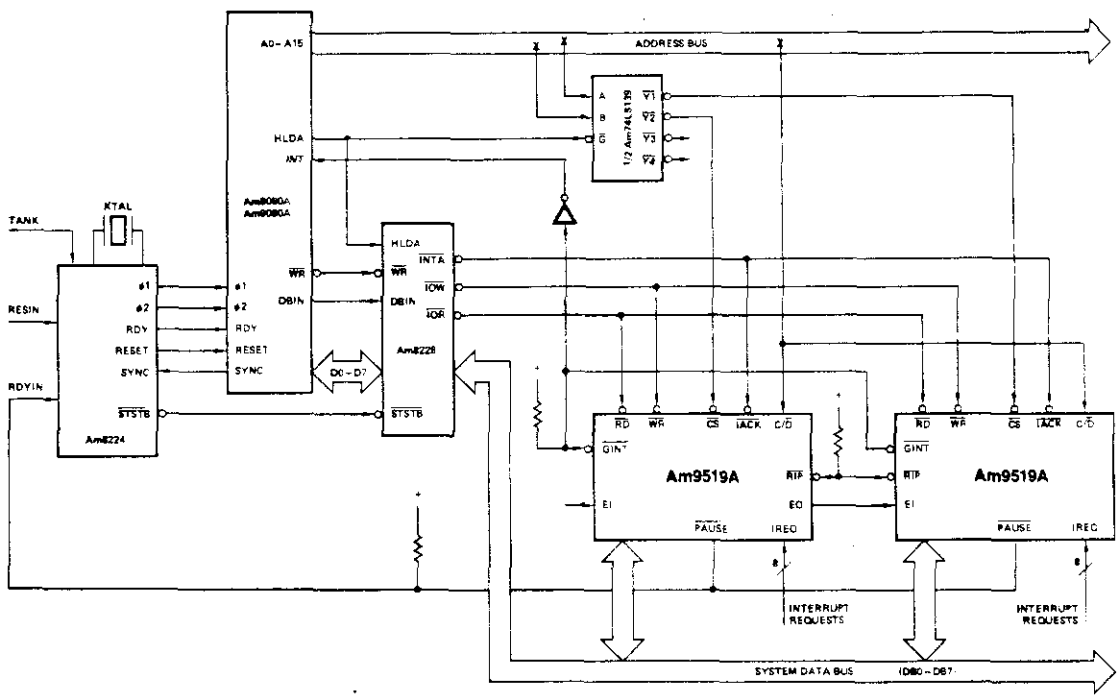
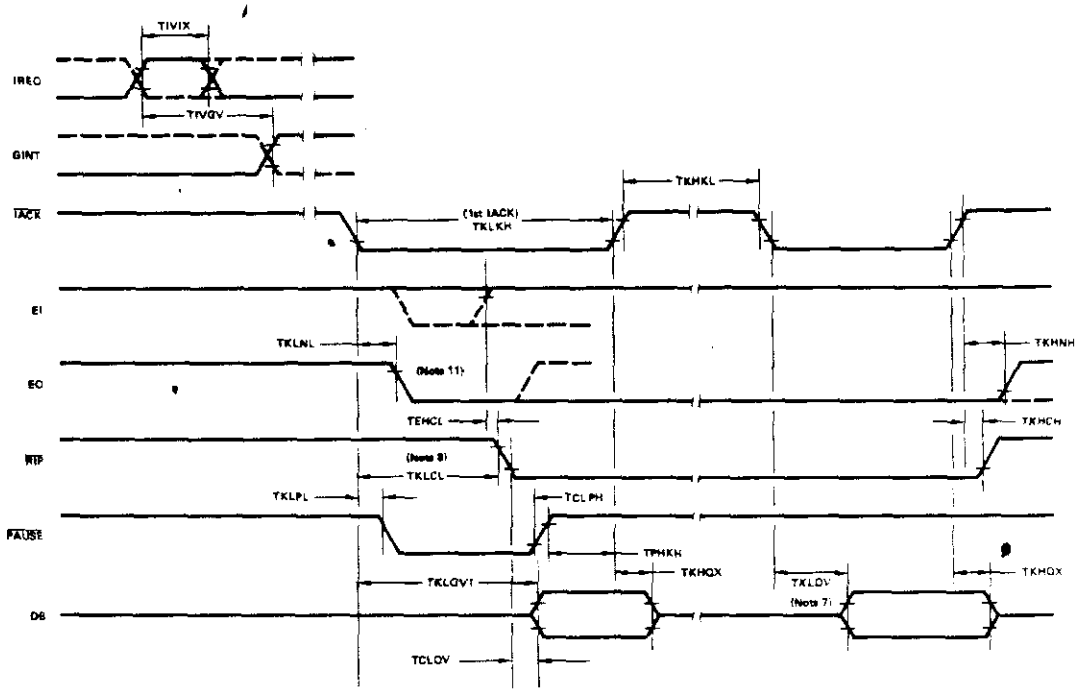


Figure 7. Expanded Interrupt System Configuration.

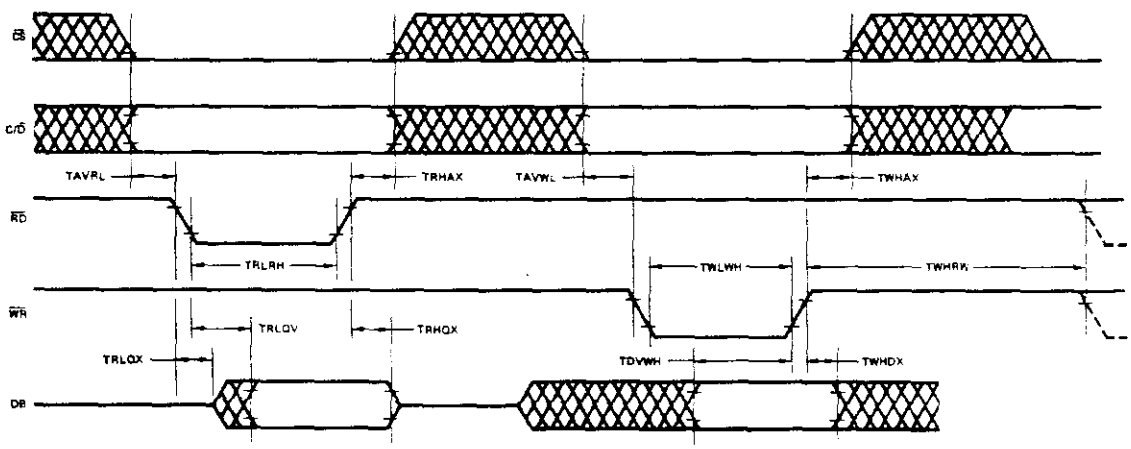
00147B-9

SWITCHING WAVEFORMS



Interrupt Operations

00147B-6



Data Bus Transfers

00147B-7

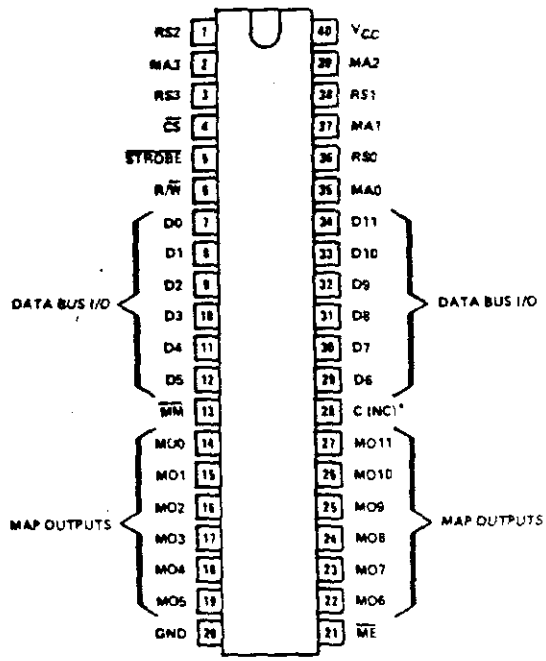
SN74LS610 THRU SN74LS613
MEMORY MAPPERS

(TIM99610 THRU TIM99613)

- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- Output Latches Provided on 'LS610 and 'LS611
- Choice of 3-State or Open-Collector Map Outputs
- Compatible with TMS 9900 and Other Microprocessors

DEVICE	OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	Open-Collector
'LS612	No	3-State
'LS613	No	Open-Collector

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



*NOTE: Pin 28 has no internal connection on 'LS612 and 'LS613

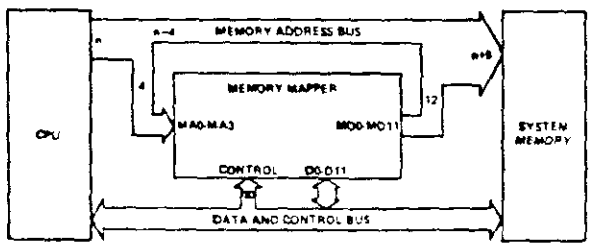
description

These memory-mapper integrated circuits contain a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. The 'LS610 and 'LS611 also contain 12 latches with an enable control.

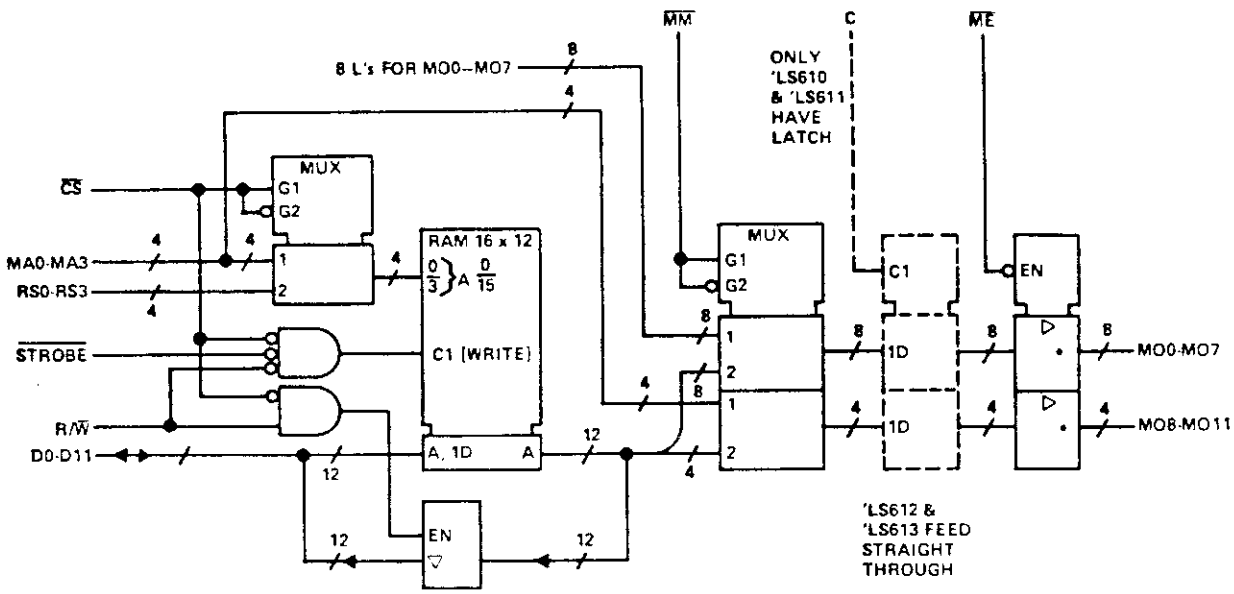
The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see the figure below) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus.

This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).

These devices have four modes of operation (read, write, map, and pass). Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/$\overline{W}$ whenever chip select ($\overline{CS}$) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when $\overline{CS}$ is high and $\overline{MM}$ (map mode control) is low. The 'LS612 and 'LS613 output stages are transparent in this mode, while the 'LS610 and 'LS611 outputs may be transparent or latched. When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bits on MA0 thru MA3 appear at MO8–MO11, respectively, (assuming appropriate latch control) with low levels in the other bit positions of the map outputs.



functional block diagram (positive logic)



*'LS610 and 'LS612 have 3-state (▽) map outputs.
'LS611 and 'LS613 have open-collector (Ω) map outputs.

PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
7–12, 29–34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0–RS3 when $\overline{CS}$ is low. Mode controlled by R/$\overline{W}$.
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations.
6	R/$\overline{W}$	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	$\overline{STROBE}$	Strobe input used to enter data into the selected map register during I/O operations.
4	$\overline{CS}$	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode ($\overline{MM}$ low and $\overline{CS}$ high).
14–19, 22–27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8–MO11 and low levels on MO0–MO7.
13	$\overline{MM}$	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0-MA3 are passed to the map outputs MO8-MO11, respectively, while MO0-MO7 are set low.
21	$\overline{ME}$	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 and 'LS611 (no internal connection for 'LS612 and 'LS613). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	V_{CC}, GND	5-V power supply and network ground (substrate) pins.

MEMORY MAPPING USING SN54/74LS610 THRU SN54/74LS613

Author
Thomas J. Tyson

Contributors
Deene Ogden, Jim Gallia and Dennis Frailey
Low Power Schottky Applications Group

INTRODUCTION

Microprocessors, due to the advent of high density semiconductor memories (i.e., 64K or larger), are being used more and more in systems featuring memory structures larger than 64K bytes. The majority of the microprocessors in use or available today have a 16-bit address bus, with a maximum addressing capability of 64K words. Due to this limitation, some sort of memory mapping is necessary to adapt these microprocessors to applications where large memory structures are required.

The memory mappers (SN54/74LS610 through SN54/74LS613) from TI were designed to alleviate this addressing limitation. These devices employ a paged memory mapping technique in expanding the system memory address bus by 8 bits, thus effectively increasing the system addressing capability by a factor of 2^8 or 256. For microprocessors with a 16-bit address bus (such as the Z-80, the 8085 and the 6800), this results in an increase in the maximum addressing capability from 64K bytes to 16M bytes and for the TMS9900 (which has a 15-bit address bus), the result is an increase from 32K words to 8M words (word = 2 bytes).

In the mapping operation, the four MSBs of the microprocessor address word are used to access one of the sixteen 12-bit registers of the memory mapper's 16 X 12-bit RAM array. Each mapper register is capable of holding a 12-bit address which will be termed the page address and will be used as the 12 MSBs of the memory address bus. The remaining 12 bits (11 in the case of the TMS9900) of the microprocessor address bus will be transferred directly to memory from the microprocessor and will be used to address the memory locations within each page. (See Figure 1)

The memory will be organized into 2^x pages (where x equals the number of bits of the page address) with 2^{n-4} words or bytes (where n is the bit length of the microprocessor address bus) per page. Once loaded, the mapper can access only 16 pages or 64K bytes (32K words in the TMS9900 case). In order to access more pages, the memory mapper RAM array must be reloaded with 16 new page addresses. This is done by the microprocessor via the data bus with the mapper in the WRITE mode. (A more detailed description of the modes of operation will be given later in this report.)

FUNCTIONAL DESCRIPTION

A functional block diagram of the SN54/74LS610 memory mapper, which consists mainly of: a 4-bit 2-to-1 multiplexer, a 16 X 12-bit RAM array, a 12-bit 2-to-1 multiplexer, 24 3-state buffers, control logic and in the case of 'LS610 and 'LS611, a 12-bit transparent latch, as shown in Figure 2. Table I lists the functional differences between the 'LS610, 'LS611, 'LS612, and 'LS613. Table II lists the function of each pin.

Depending on the state of the input control signals (i.e., $\overline{CS}$, R/$\overline{W}$, $\overline{STROBE}$, $\overline{MM}$, and $\overline{ME}$), the mapper can be operated in three basic modes of operation, I/O (READ or WRITE), MAP and PASS. An explanation of each mode and the control signals necessary to achieve that mode of operation is given below. (Refer to Table III)

Input/Output Mode

In this mode a page address can be loaded either into a mapper register or can be read from a memory mapper register depending on the state of the R/$\overline{W}$ (READ/WRITE) input. This input signal controls either the READ or WRITE function of the I/O Mode.

WRITE Mode

One of the sixteen 12-bit registers is loaded with a page address via the D0-D11 I/O ports from the microprocessor. The address of the selected register is inputted via the RS0-RS3 inputs and is usually the four LSBs of the microprocessor address word. The chip select ($\overline{CS}$), the strobe ($\overline{STROBE}$) and R/$\overline{W}$ controls should all be low.

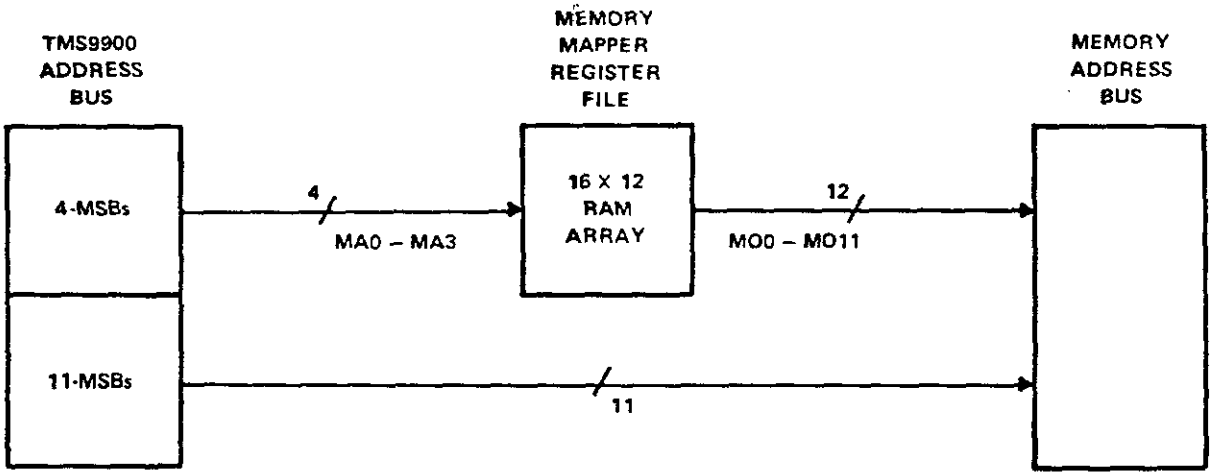


Figure 1. Mapping Operation

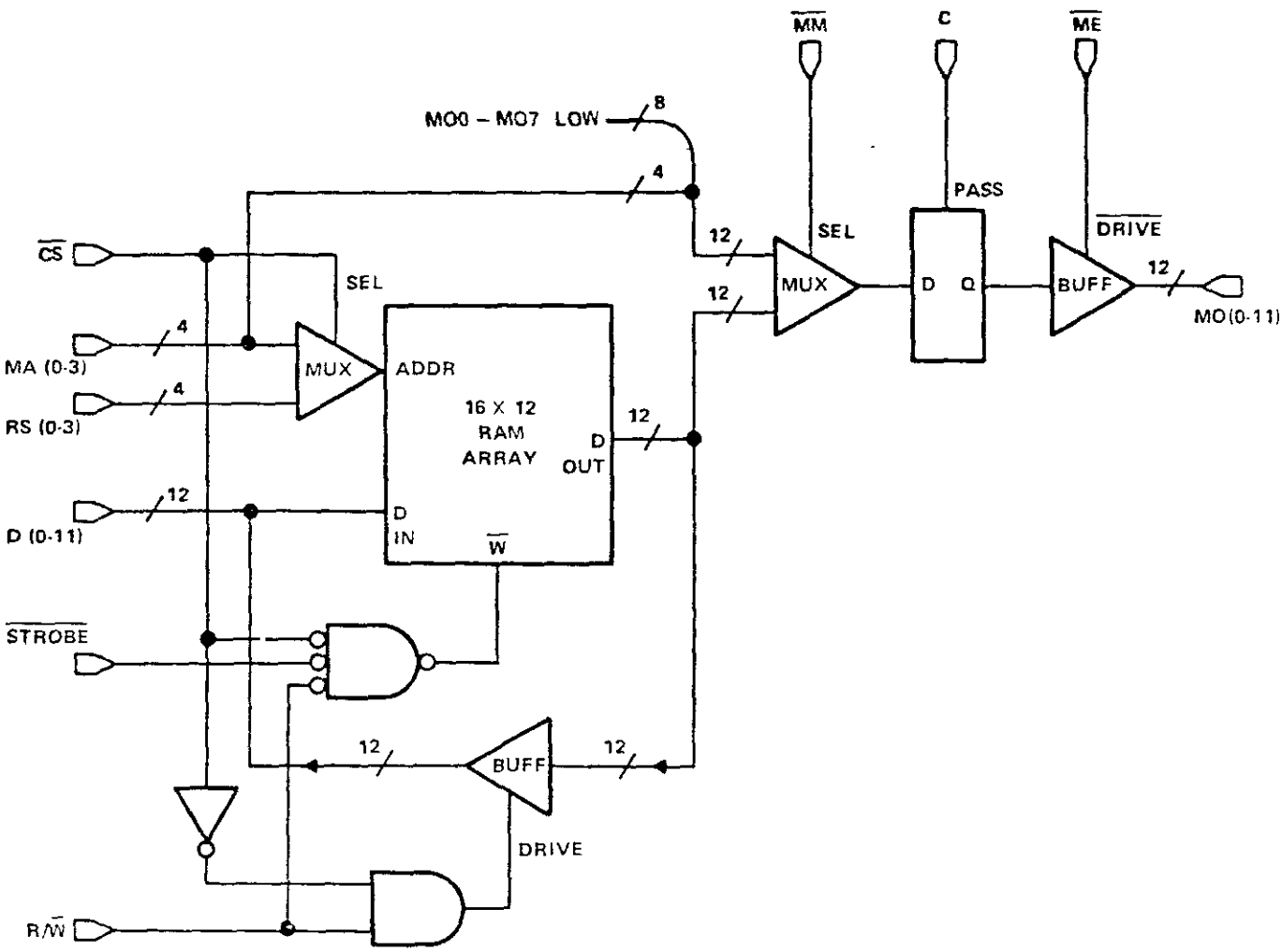


Figure 2. Logic Diagram of the Memory Mapper 'LS610

Table I. Device Comparison

Device	Map Outputs Latched	Map Output Type
SN54/74LS610	Yes	3-State
SN54/74LS611	Yes	Open-collector
SN54/74LS612	No	3-State
SN54/74LS613	No	Open-collector

READ Mode

The contents of one of the sixteen 12-bit registers is read from the mapper via the D0-D11 I/O ports. As in the WRITE mode, the mapper register is selected by the address on the RS0-RS3 inputs. Again chip select ($\overline{CS}$) should be low, while the R/$\overline{W}$ should be kept high.

MAP Mode

The contents of one of the sixteen 12-bit memory mapper registers is outputted to the system address bus via the MO0-MO11 outputs. The address on MA0-MA3 selects the mapper register and is usually the four MSBs of the microprocessor address word. The chip select ($\overline{CS}$) must be inactive (high), the map mode ($\overline{MM}$) control and the map enable ($\overline{ME}$) must both be active (low). The n–4 LSBs, where n equals the microprocessor address bit length, of the microprocessor address bus will be transferred directly to memory from the microprocessor, while the remaining 12 MSBs of the system address bus will be driven onto the bus by the memory mapper.

Table II. Pin Functions

Pin	Pin Name	Functional Description
7-12 29-34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0-RS3 when $\overline{CS}$ is low. Mode controlled by R/$\overline{W}$. (D0 corresponds to MO0 and is the most significant bit.)
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations. (RS3 is the least significant bit.)
6	R/$\overline{W}$	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	$\overline{STROBE}$	Strobe input used to enter data into the selected map register during I/O operations.
4	$\overline{CS}$	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode ($\overline{MM}$ low and $\overline{CS}$ high). (MA3 is the least significant bit.)
14-19 22-27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8-MO11 and low levels on MO0-MO7. (MO11 is the least significant bit.)
13	$\overline{MM}$	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the four bits present on the map address inputs are passed to the map outputs.
21	$\overline{ME}$	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 and 'LS611 (no internal connection for 'LS612 and 'LS613). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	V_{CC}, GND	Power supply (5 V) and network ground (substrate) pins.

Table III. Modes of Operation

MAPPER INPUTS	I/O		MAP	PASS
	WRITE (LOAD)	READ (VERIFY)		
$\overline{CS}$	Active (Low)	Active (Low)	Inactive (High)	Inactive (High)
$\overline{STROBE}$	Active (Low)	Don't Care	Don't Care	Don't Care
R/$\overline{W}$	Low	High	Don't Care	Don't Care
$\overline{MM}$	Don't Care	Don't Care	Active (Low)	Inactive (High)
$\overline{ME}$	Inactive (High)	Inactive (High)	Active	Active
RS0-RS3	Address of Selected Register	Address of Selected Register	Don't Care	Don't Care
MA0-MA3	Don't Care	Don't Care	Address of Selected Register	Address of Selected Register
MO0-MO11	High Impedance	High Impedance	Valid Address	Valid Address
D0-D11	Register contents to be loaded (input)	Register contents to be read (output)	Input Mode	Input Mode

PASS Mode

The four LSBs (MO8-MO11) of the memory mapper address bus (MO0-MO11) will be the same as the address on the MA0-MA3 input bus, while the remaining eight MSBs of the memory mapper address bus will all be low. The chip select ($\overline{CS}$) and the map mode ($\overline{MM}$) should both the inactive (high); map enable ($\overline{ME}$) should be active. In other words, the address on the system address bus will be the same as the address outputted by the microprocessor, and the memory mapper becomes transparent to the system.

SYSTEMS INTEGRATION

The flexibility of the memory mapper is such that it can be used with microprocessors that have either an 8-bit or a 16-bit data bus. In order to use the memory mapper to its fullest potential (i.e., expand the address bus by eight bits) with an 8-bit microprocessor, the 12-bit page address must be multiplexed into the mapper via the 8-bit data bus. This means that the time it normally takes to load or read the memory mapper will be at least doubled and extra external circuitry will be necessary. If the requirement of the system is such that the address bus needs to be increased by only four bits, then there is no need for multiplexing in the page address. Of course this means that the address bus is expanded to only 20 bits resulting in a 1-megabyte addressing capability. Next in this report, we will look at two 8-bit systems utilizing the 'LS612 memory mapper.

TMS9995-Based System

Figure 3 shows a TMS9995-based system using the 'LS612 to expand the address bus by four bits. The TMS9995 is an 8-bit microprocessor with a 16-bit address bus. This system employs the Programmable System Interface (TMS9901) to control the operation of the mapper. The control of the mapper is software programmable via the I/O ports of the TMS9901. Since the mapper registers are viewed as part of the logical memory space, an address decode (AD0) of the 12 MSBs is gated with a CRU bit to select the mapper for a READ or WRITE operation. The specific mapper register is then selected by the four LSBs of the microprocessor address bus (A15-A12) via the RS0-RS3 inputs of the mapper. Table IV shows the state of the three control signals P0, P1 and AD0 and the corresponding mode of operation of the mapper. When placed in the I/O mode, the READ or WRITE operation is then controlled by memory signals from the microprocessor (i.e., $\overline{WE}$/CRUCLK, $\overline{MEMEN}$, and $\overline{DB\ IN}$). On POWER-UP and RESET, the I/O ports of the '9901 are put into the input mode. The pull-up resistors R1 and R2 will ensure the mapper is placed in the pass mode during POWER-UP and RESET. The resultant address bus is 20 bits wide, and SA19 is the LSB.

Z-80-Based System

Figure 4 shows another 8-bit (Z-80-based) system using the TI memory mapper. In this case, the control of the mapper is implemented by two flip-flops feeding $\overline{MM}$ and $\overline{CS}$. These flip-flops are programmed by the Z-80 and are addressed by the data bus, D0-D1. Table V shows the necessary states of D0 and D1 to set the mapper in its proper mode of operation. Again during POWER-UP or RESET, the flip-flops are both cleared by $\overline{RST}$, which is supplied by the system and which puts the mapper in the pass mode.

Table IV. TMS9900/'LS610 Control Signals

MEMORY MAPPER MODE OF OPERATION	CONTROL SIGNALS		
	P1	P0	AD0
MAP	L	H	L
PASS	H	H	L
I/O	H	L	L

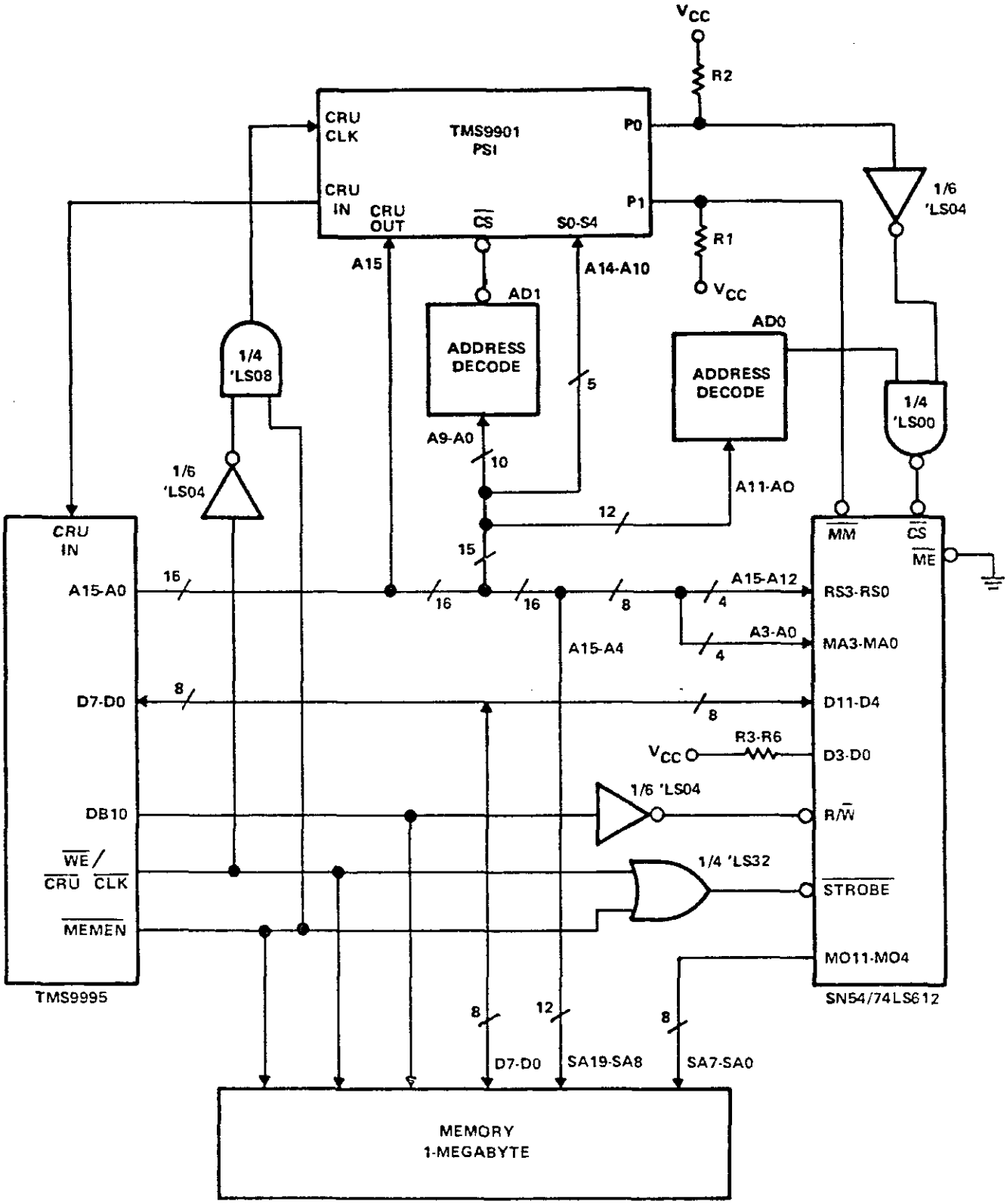


Figure 3. TMS9995 with Memory Mapper

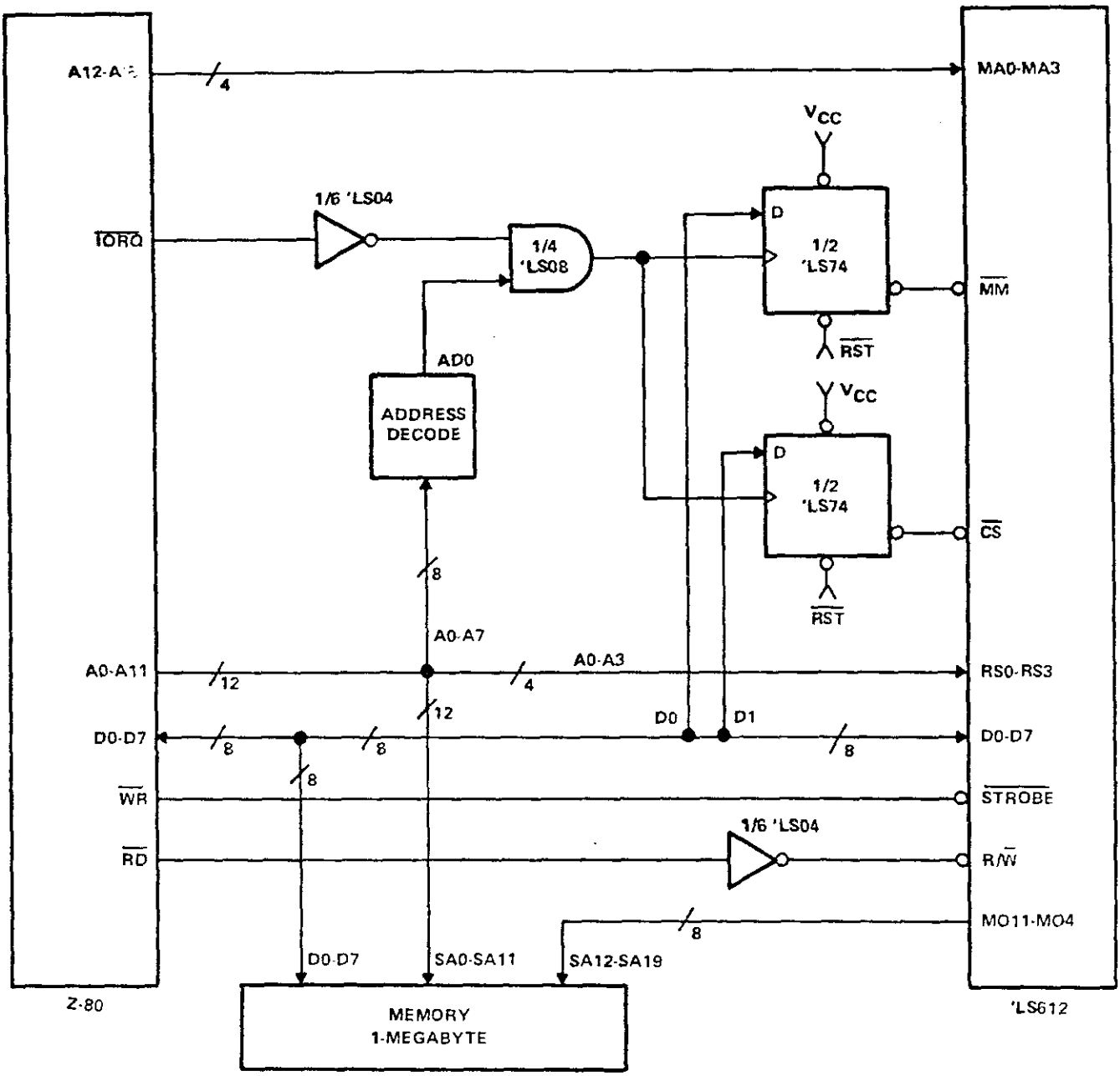


Figure 4. Z-80 with Memory Mapper

Table V. Z-80/LS'610 Control Signals

CONTROL SIGNALS			MEMORY MAPPER
D0	D1	(AD0) $\overline{IORQ}$	MODE OF OPERATION
L	L	↑	PASS
H	L	↑	MAP
L	H	↑	I/O

TMS9900-Based System

One of the limitations of using an 8-bit microprocessor with the memory mapper, without multiplexing the page address, is that the address bus can only be expanded four bits. In a 16-bit system, one based on a 16-bit microprocessor like the TMS9900, no extra circuitry is necessary to load the mapper with the full 12-bit address. Figure 5 shows a TMS9900 with an SN54/74LS612 for memory mapping. The control of the mapper is implemented in the same fashion as the system using the TMS9995 mentioned previously in the report. The resultant addressing capability is eight megawords. These TI microprocessors have set aside address space for RESET, XOP and INTERRUPT VECTORS, which are addressed when the microprocessor performs a context switch. During a context switch, the microprocessor must be able to address these locations which are part of the logical address (i.e., locations that are capable of being addressed by the microprocessor independently). One method, besides placing the mapper into the pass mode, is to load the memory mapper register whose 4-bit address is O_H with the address of the first page of physical memory. This, like the pass mode, will effectively make the memory mapper appear to be transparent.

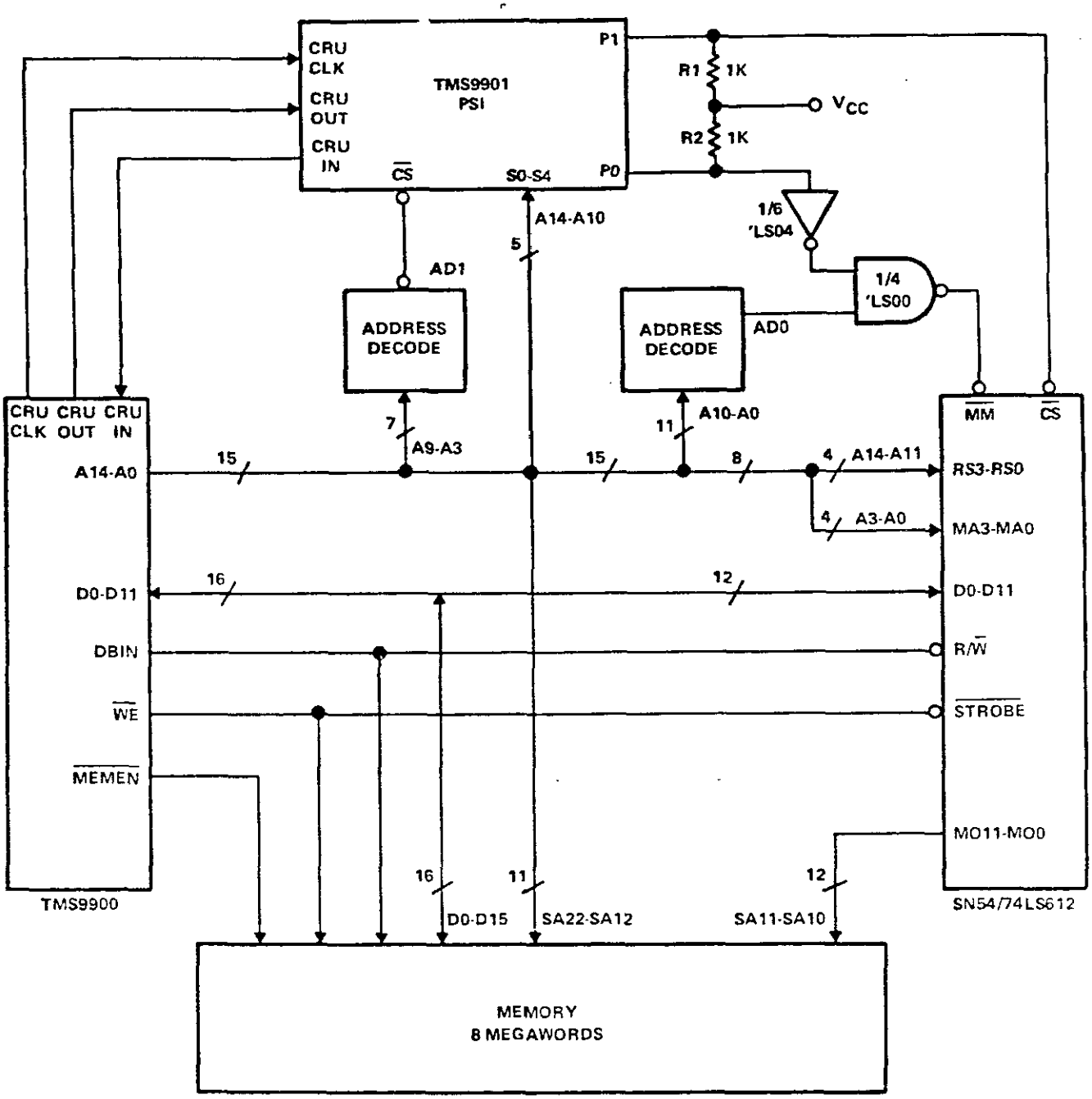


Figure 5. TMS9900 with Memory Mapper

Another point worth noting is that in all three of the previously mentioned systems, the $\overline{ME}$ input was always connected to ground. This caused the mapper address buffers to be enabled during all modes of operation of the mapper. This is only a problem during the I/O mode where, when loading the mapper register, other memory locations are also being written into. The method used to avoid destroying data already in memory was to put the mapper into the pass mode during the I/O operation. This was accomplished simply by pulling $\overline{MM}$ input high, thus making the system address equal to the microprocessor address.

Multimapper Systems

In a system employing a single memory mapper, the maximum active addressing capability is only 16 pages. If increased addressing capabilities are needed, the mapper must be reloaded. To avoid this procedure, another mapper may be added to the system. This will not increase the overall addressing capability of the system, but it will double the amount of active pages and will also afford twice the active addressing capability. Even though the control of two mappers is a little more detailed than the control of one, the same basic methods employed in the systems with one mapper can be used here.

TIMING

The subject of how the mapper affects the critical timing parameters of the memory READ/WRITE cycles and what changes, if any, are needed to accommodate the mapper, have not been discussed in this report. First, looking at the I/O mode of operation where the mapper registers are either loaded or read from, it is seen that the mapper registers can be regarded as standard common I/O, static RAMs, with maximum access times (RS to valid MO, T_A = 25°C, C_L = 50 pF, V_{CC} = 5 V) of 75 ns. Once the I/O mode is set ($\overline{CS}$ = low), the only two signals necessary to read or write into the mapper are $\overline{STROBE}$ and R/$\overline{W}$. As shown in the previously mentioned system, these signals were supplied directly from the microprocessor with no wait states necessary to perform either function. This will be the case with most microprocessors.

In the MAP and PASS mode, the main concern is the maximum access time (MA to MO). This access time is specified at a maximum of 70 ns, which, depending on the timing of the microprocessor and the memory used, may or may not cause any problems. In the Z-80-based system, no wait states were introduced by the mapper because the memory control signals become active 95 ns after the microprocessor address bus became valid. This gives the address bus sufficient time to settle down.

In conclusion, it can be said that for most microprocessors and memory available at the time of this writing, the operation of the mapper does not adversely affect the memory cycle timing and is flexible enough to be used with almost all microprocessors.

SUMMARY

The possible uses of the memory mapper and the various techniques that can be employed to control its operation are numerous and only some examples were shown in this report. Some of the other possible applications of the mapper include: (1) achieving system addressing capability greater than 16 megabytes is accomplished by reducing the number of mapper registers used by a factor of 2, thus increasing the size of each page by the same factor of 2 without affecting the total amount of pages; (2) being used in systems employing DMA; (3) memory protection which can be accomplished by sacrificing one or two bits of the page address, and gating these bits with the memory control signals.

Another technique that may be employed in controlling the modes of operation of the mapper is to use PROMs.

WESTERN DIGITAL
C O R P O R A T I O N

WD279X-02 Floppy Disk Formatter/Controller Family

FEATURES

- ON-CHIP PLL DATA SEPARATOR
- ON-CHIP WRITE PRECOMPENSATION LOGIC
- SINGLE +5V SUPPLY
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 (FM)
  - IBM 34 (MFM)
- AUTOMATIC SEEK WITH VERIFY
- MULTIPLE SECTOR READ/WRITE
- TTL COMPATIBLE
- PROGRAMMABLE CONTROL
  - SELECTABLE TRACK-TO-TRACK ACCESS
  - HEAD LOAD TIMING
- SOFTWARE COMPATIBLE WITH THE FD179X SERIES
- SOFT SECTOR FORMAT COMPATIBILITY

APPLICATIONS

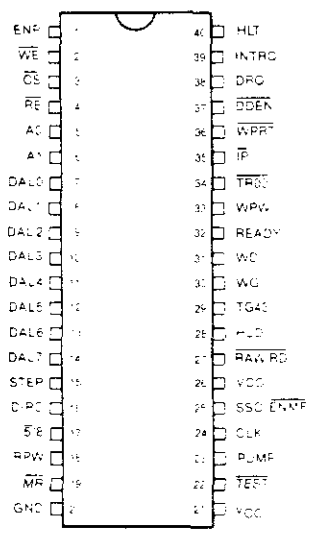
8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER

The WD279X Family are MOS/LSI devices which perform the functions of a Floppy Disk Controller/Formatter. Software compatible with its predecessor, the FD179X, the device also contains a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic.

When operating in Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

The WD279X is fabricated in NMOS silicon gate technology and available in a 40 pin dual-in-line ceramic or plastic package.

FEATURES	2791	2793	2795	2797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Side Select Out			X	X
Internal CLK Divide	X	X		



PIN DESIGNATION

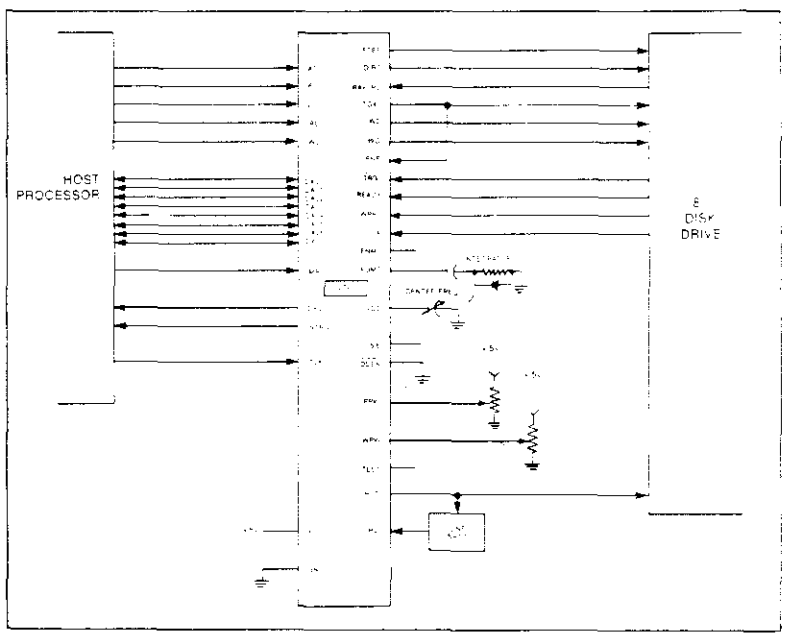


Figure 1.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	ENABLE PRECOMP	ENP	A Logic high on this input enables write precompensation to be performed on the Write Data output.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, *HEX 01 is loaded into sector register.*
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5, 6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit bi-directional bus used for transfer of commands, status, and data. These lines are inverted (active low) on WD2791 and WD2795.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference. 2 MHz ± 1% for 8" drives, 1 MHz ± 1% for mini-floppies.
38	DATA REQUEST	DRQ	This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR.
39	INTERRUPT REQUEST	INTRQ	This output is set at the completion of any command *and is reset when the Status register is read or* the Command register is written to.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	5¼," 8" SELECT	$\overline{5/8}$	This input selects the internal VCO frequency for use with 5¼" drives or 8" drives.
18	READ PULSE WIDTH	RPW	An external potentiometer tied to this input controls the phase comparator within the data separator.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins.
23	PUMP	PUMP	High-Impedance output signal which is forced high or low to increase/decrease the VCO frequency.
25	ENABLE MINI-FLOPPY (2791, 2793)	$\overline{\text{ENMF}}$	A logic low on this input enables an internal ÷2 of the Master Clock. This allows both 5¼" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a Logic 1.
25	SIDE SELECT OUTPUT (2795, 2797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	VOLTAGE-CONTROLLED OSCILLATOR	VCO	An external capacitor tied to this pin adjusts the VCO center frequency.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	MFM or FM output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE PRECOMP WIDTH	WPW	An external potentiometer tied to this input controls the amount of delay in Write precompensation mode.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the WD279X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the WD279X when the index hole is encountered on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
36	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	$\overline{DDEN}$	This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected.
40	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.

GENERAL DESCRIPTION

The WD279X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The WD279X, which can be considered the end result of both the FD1771 and FD179X designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The WD279X contains all the features of its predecessor the FD179X plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD179X and WD279X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The WD279X is set up to operate on a multiplexed bus with other bus-oriented devices.

The WD279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The 2793 is identical to the 2791 except the DAL lines are TRUE for systems that utilize true data busses.

The 2795/7 has a side select output for controlling double sided drives.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input ($\overline{RAW\ READ}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — *This 8-bit register holds the* command presently being executed. This register should *not be loaded when the device is busy unless the new* command is a force interrupt. The command register can *be loaded from the DAL, but not read onto the DAL.*

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is $G(x) = x^{16} + x^{12} + x^5 + 1$.

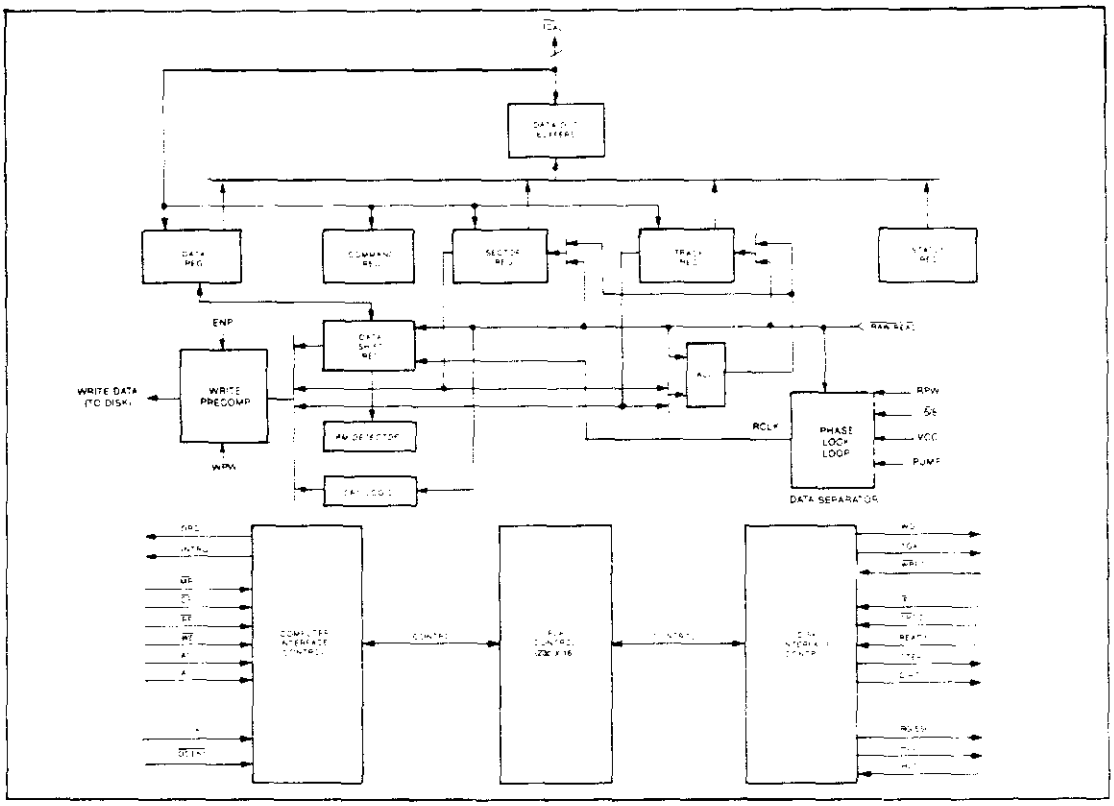
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — *The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID* field.

Timing and Control — *All* computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation — enables write precompensation to be performed on the Write Data output.



WD279X BLOCK DIAGRAM

Data Separator — a high performance Phase-Lock-Loop Data Separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD279X. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD279X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 279X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 5¼" drives.

On the 2791/2793, the $\overline{ENMF}$ input (Pin 25) can be used for controlling both 5¼" and 8" drives with a single 2 MHz clock. When $\overline{ENMF}$ = 0, an internal ÷ 2 of the CLK is performed. When $\overline{ENMF}$ = 1, no divide takes place. This allows the use of a 2 MHz clock for both 5¼" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The $\overline{5/8}$ input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When $\overline{5/8}$ = 0, 5¼" data separation is selected; when 5/8 = 1, 8" drive data separation is selected.

CLOCK (24)	$\overline{ENMF}$ (25)	$\overline{5/8}$ (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	5¼"
1 MHz	1	0	5¼"

Note: All other conditions invalid.

FUNCTIONAL DESCRIPTION

The WD279X-02 is software compatible with the FD179X-02 series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 179X can be transferred to a 279X system without modification.

In addition to the 179X, the 279X contains an internal Data Separator and Write precompensation circuit. The $\overline{TEST}$ (Pin 22) line is used to adjust both data separator and precompensation. When $\overline{TEST}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths to meet drive specifications.

Similarly, Data separation is also adjusted with $\overline{TEST}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (.5 MHz for 8" drives). The VCO Trimming capacitor (Pin 26) is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The $\overline{TEST}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{TEST}$ pin, overriding the pull-up. The $\overline{TEST}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the 179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: ENP, $\overline{5/8}$, $\overline{ENMF}$, $\overline{WPRT}$, $\overline{DDEN}$, HLT, TEST, and $\overline{MR}$.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

* 2795/97 may vary — see command summary.

The number of sectors per track as far as the 279X is concerned can be from 1 to 255 sectors. The number of tracks as far as the 279X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the 279X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the 279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the 279X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 2791, 2793

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

B. Commands for Models: 2795, 2797

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No. 15 MS delay E = 1, 15 MS delay (30 MS for 1 MHz)
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field: 00 / 01 / 10 / 11 L = 0: 256 / 512 / 1024 / 128 L = 1: 128 / 256 / 512 / 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset* I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

Write Precompensation

When operating in Double Density mode ($\overline{DDEN}$ = 0), the 279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{TEST}$ = 0.

Data Separation

The 279X can operate with either an external data separator or its own internal recovery circuits. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.

To program the 279X for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST}$ = 0. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8" Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a Logic 1 for normal operation. Note: To maintain this mode, $\overline{TEST}$ must be held low whenever $\overline{MR}$ is applied.

For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external variable capacitor of 5-60 pf is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 KHz for 8" Double Density). The $\overline{DDEN}$ line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

After adjustments have been made, the $\overline{TEST}$ pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a Filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The Source Impedance for a PUMP UP/DOWN condition is 600/120 ohms, respectively, therefore the change in bias voltage for each pump can be approximated:

$$dV = \frac{dt \, \Delta V}{RC}$$

dt = 250 ns. (set by RPW)
C = 0.1μf
R = R_S + R
ΔV = 2.6 V for PUMP UP
0.9V for PUMP DOWN

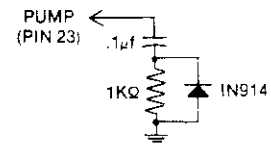
Look up response (T_L) is the transient time for the Loop to lock from center frequency (F_O) to maximum lock range:

$$T_L = 10\% \, F_L \times K_O \times \Delta P$$

Where:
K_O = VCO Conversion Gain = 3.7KHz/mV
F_L = Lock Range = 4.00 MHz
ΔP = Change in Bias for each Pump = 4 mV/PUMP

400 KHz x 3.7 KHz x 4 mV = 27 pumps
27 pumps = 54 μsec = 3.4 Byte times (8" Double Density)

The following Filter Circuit is recommended for 8" FM/MFM:



Since 5¼" Drives operate at exactly one-half the data rate (250 Kb/sec) the above capacitor should be doubled to .2 or .22μf.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0 r_1), which determines the stepping motor rate as defined in Table 3.

A 2μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK R1	CLK R0	2 MHz $\overline{TEST}$ = 1	1 MHz $\overline{TEST}$ = 1
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for

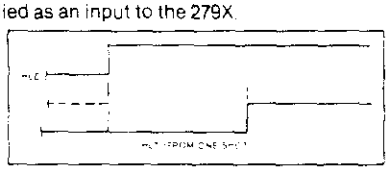
a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The WD279X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the 279X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the 279X which is used for the head engage time. When HLT = 1, the 279X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the 279X.



HEAD LOAD TIMING

When both HLD and HLT are true, the 279X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the 279X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the 279X then waits for HLT to occur.

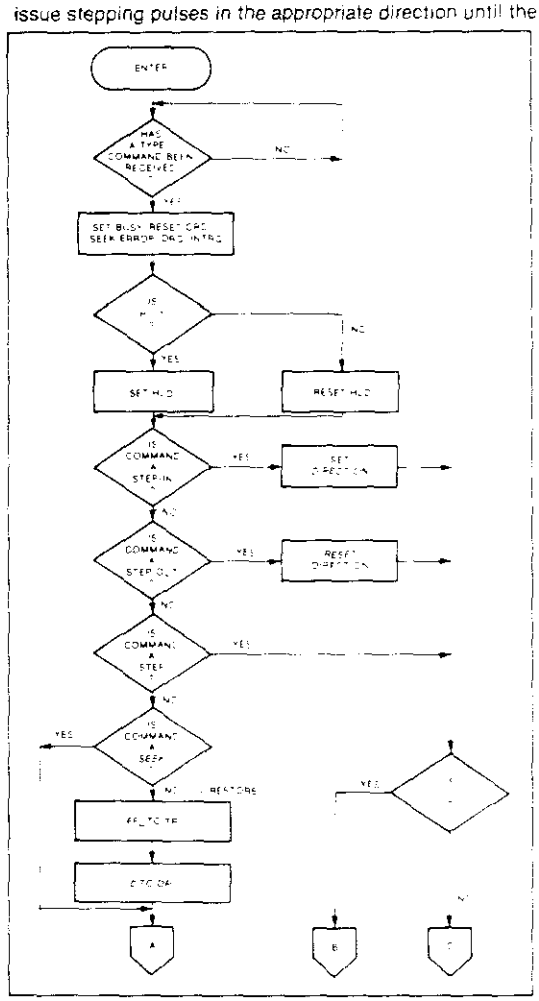
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

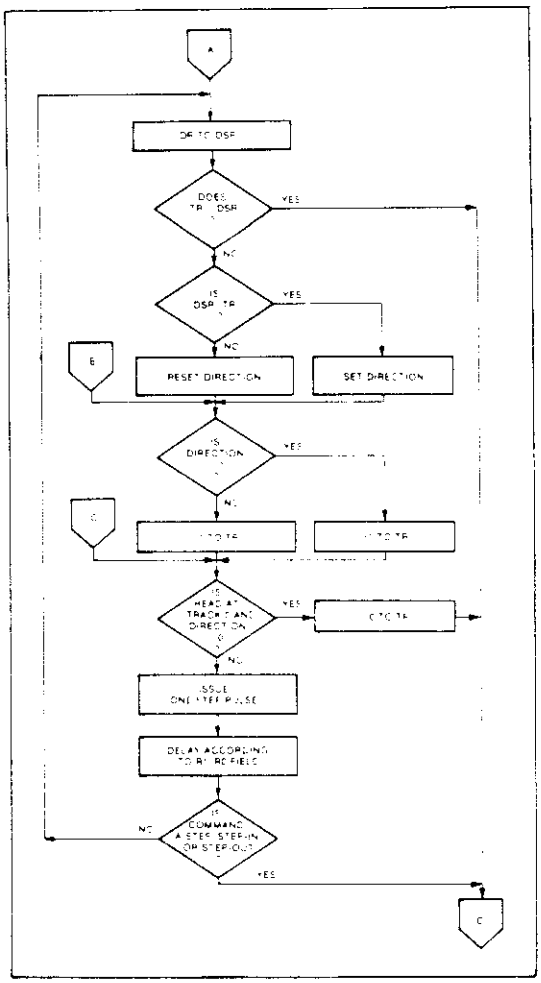
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r1r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the 279X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.

SEEK

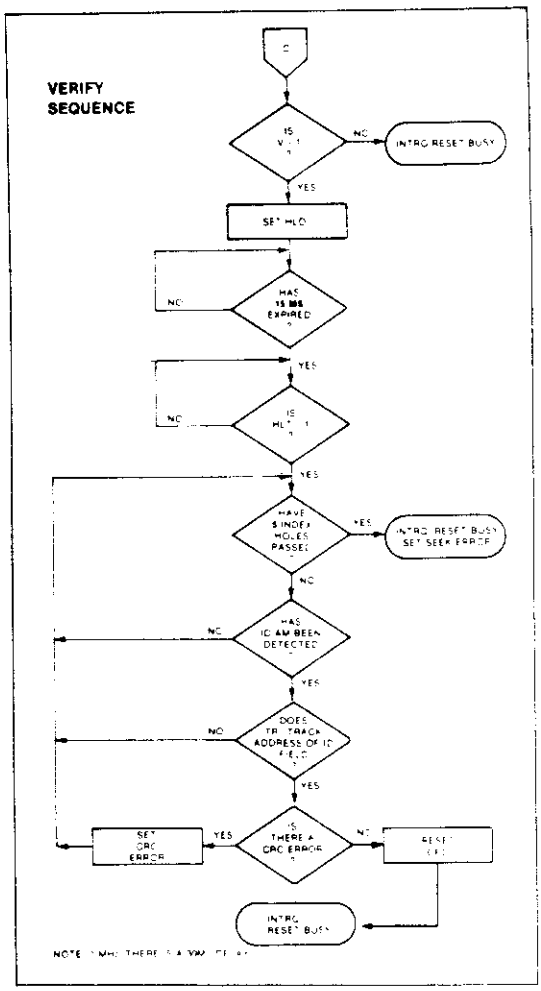
This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the appropriate direction until the



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the 279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 76. If the T flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

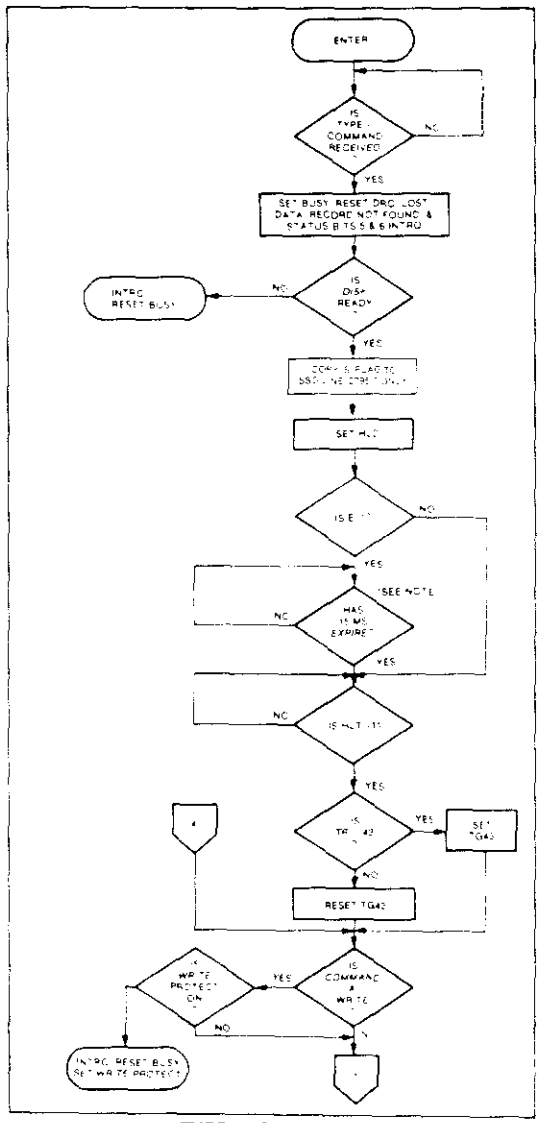
On the 2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

TYPE II COMMANDS

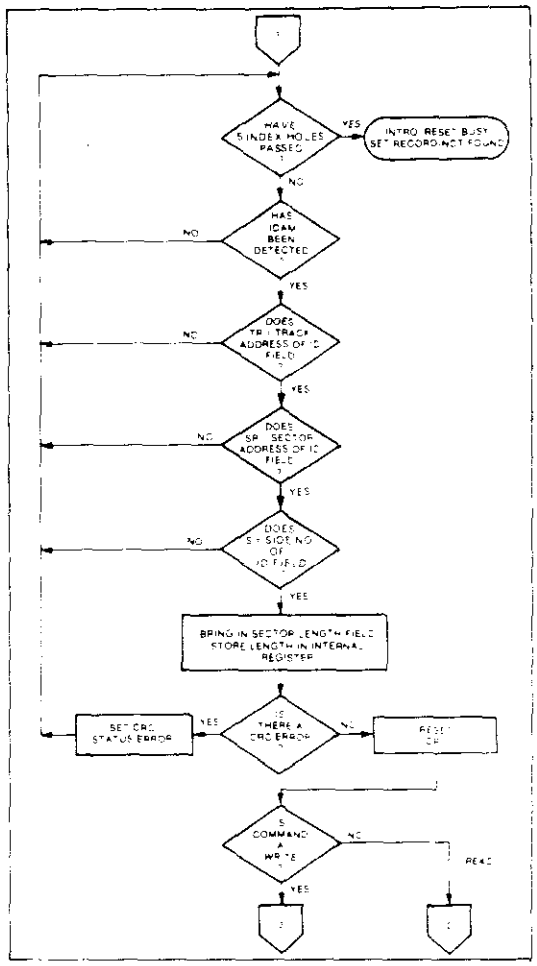
The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the

Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.

When an ID field is located on the disk, the 279X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from



TYPE II COMMAND

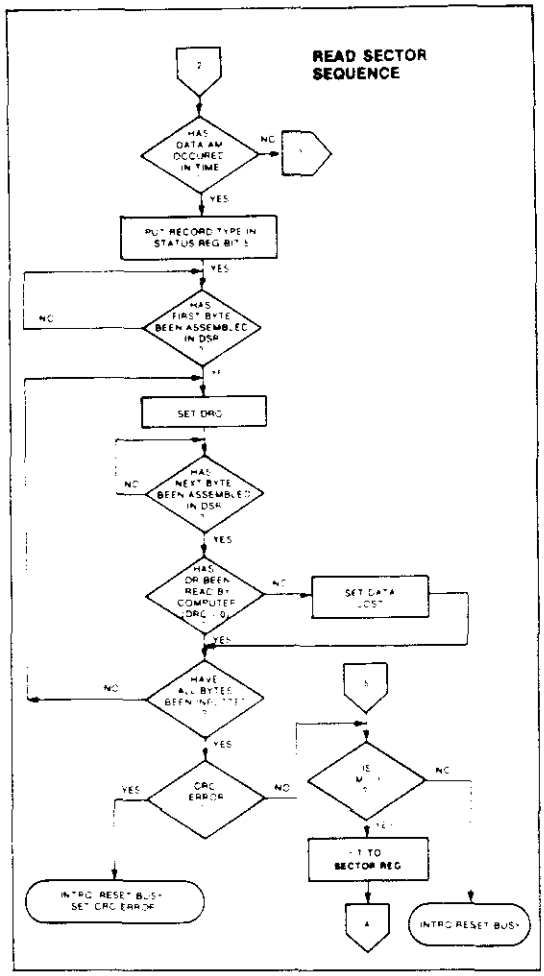


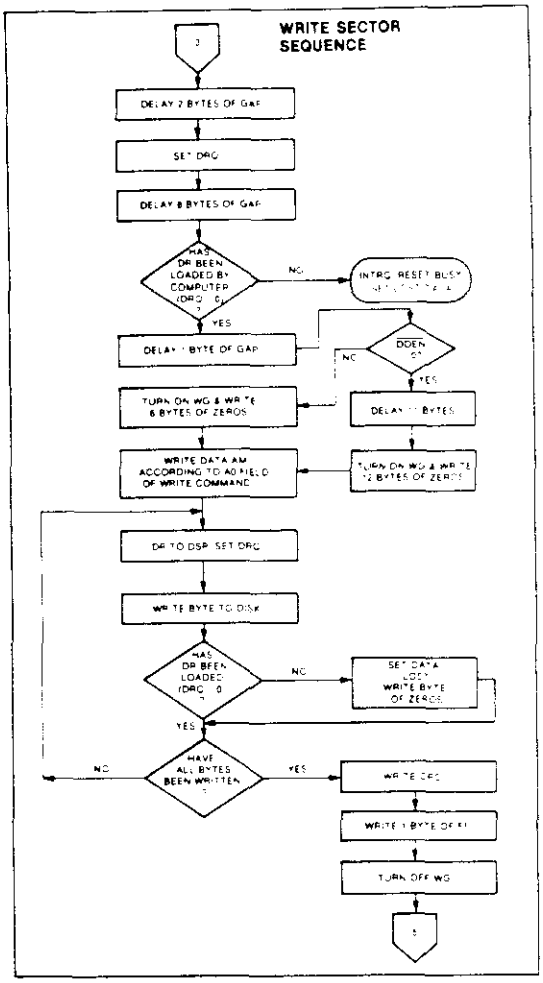
TYPE II COMMAND

depending upon the command. The 279X must find an ID field with a Track number, Sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 4) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 279X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the 279X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds





TYPE II COMMAND

the number available. The 279X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for 2791-93 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the 279X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 2795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The 2795/7 READ SECTOR and WRITE SECTOR com-

TYPE II COMMAND

mands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field search is repeated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred

that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The 279X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a0 field of the command as shown below:

a0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The 279X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one bye of FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

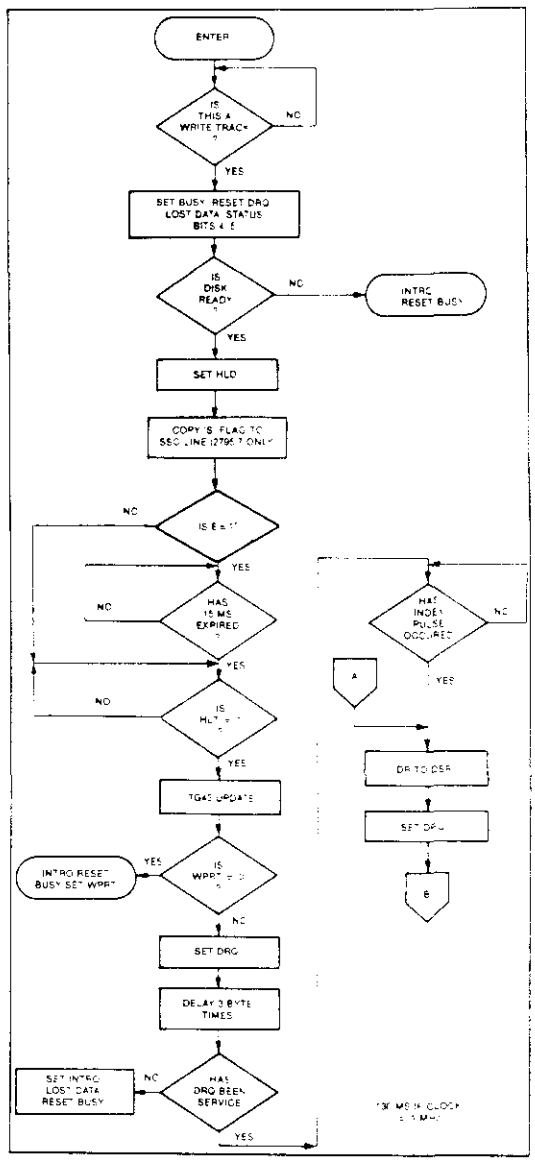
TYPES III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

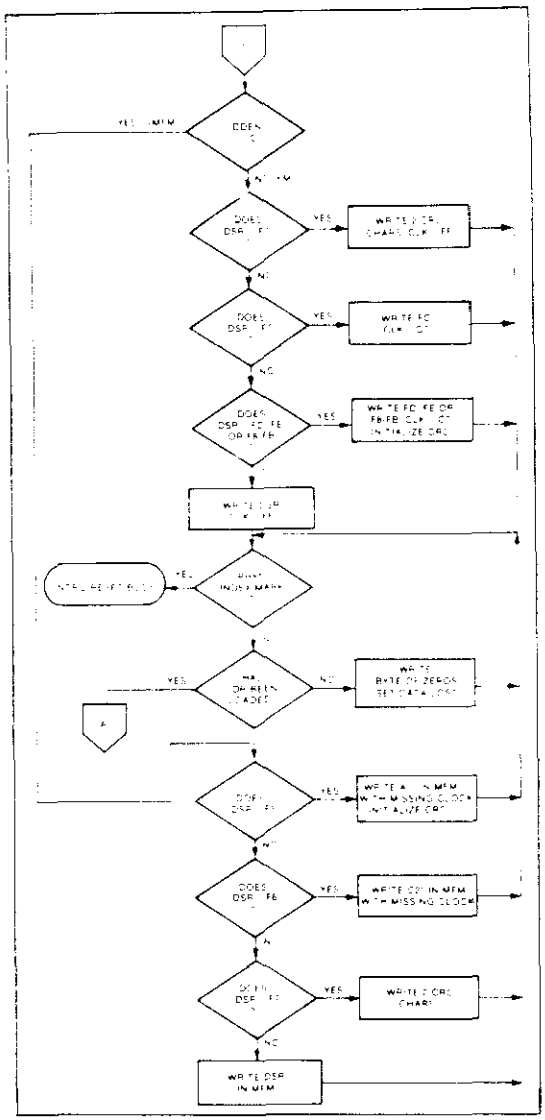
Although the CRC characters are transferred to the computer, the 279X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy Status is reset.



TYPE III COMMAND WRITE TRACK

READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The ac-



TYPE III COMMAND WRITE TRACK

cumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule with the Lost Data status flag being set.

The ID A.M., ID field, ID CRC bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the 279X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	WD279X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	WD279X INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

* Missing clock transition between bits 4 and 5

** Missing clock transition between bits 3 and 4

or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

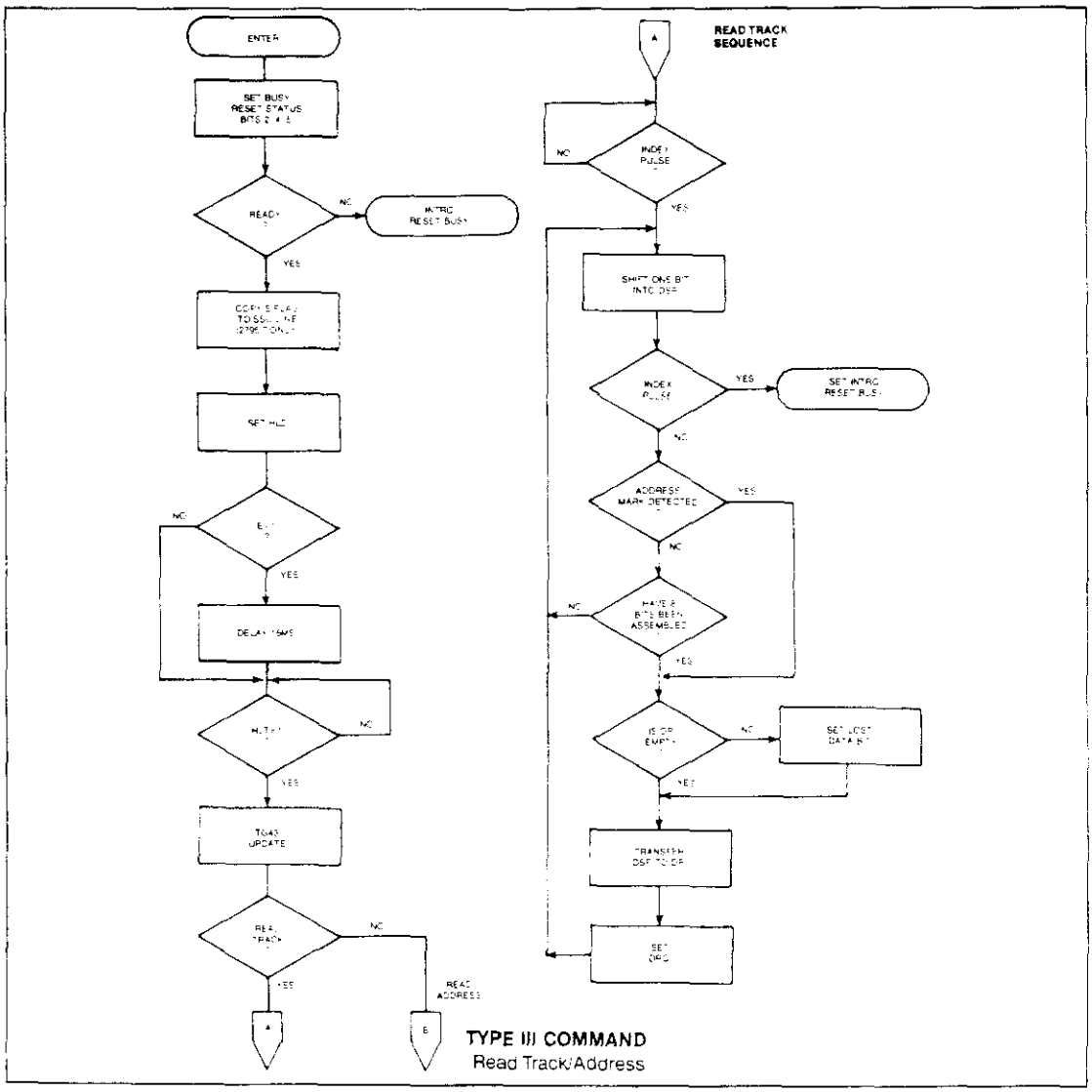
TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate



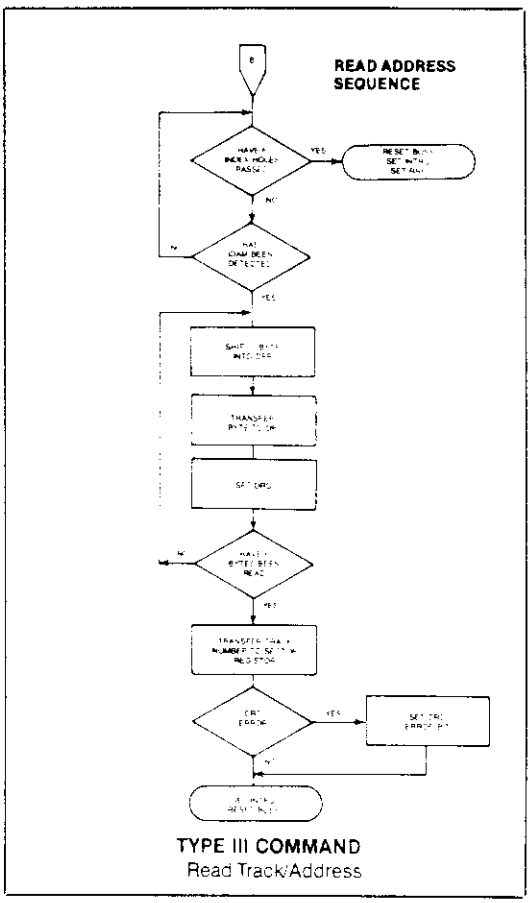
TYPE III COMMAND
Read Track/Address

interrupt condition I_3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.)

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.



TYPE III COMMAND
Read Track/Address

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12μs	6μs
Write to Command Reg.	Read Status Bits 1-7	28μs	14μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)[3]
6	00
1	FC (Index Mark)
1 26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247[2]	FF (or 00)

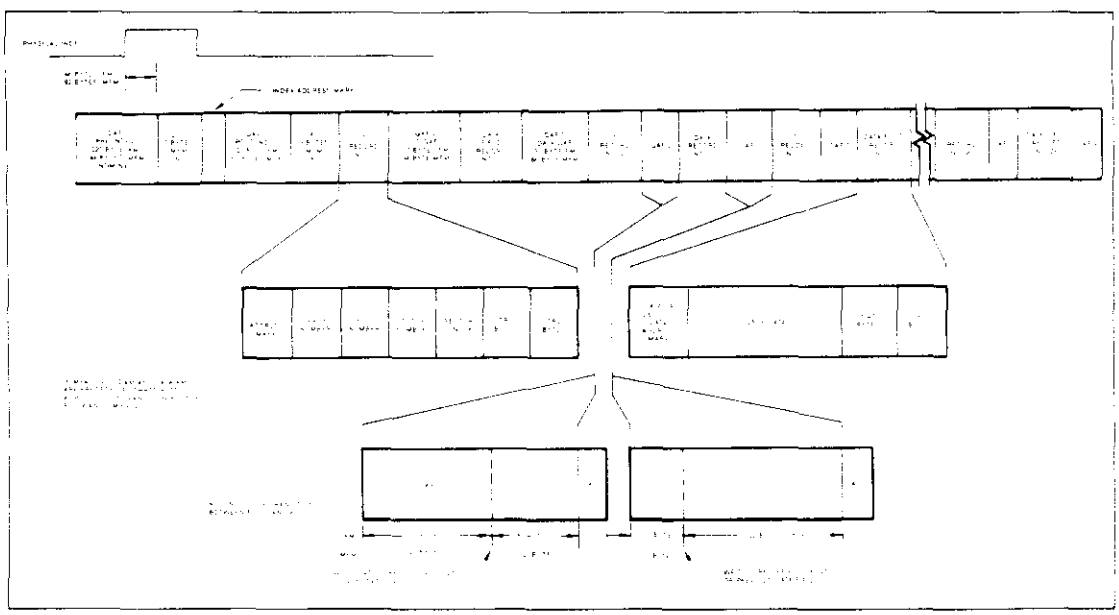
1. Write bracketed field 26 times
2. Continue writing until 279X interrupts out. Approx. 247 bytes.
3. A '00' option is allowed.

IBM SYSTEM 34 FORMAT-256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order for format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
* 50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times
** Continue writing until 279X interrupts out. Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.

2) Gap 2 cannot be varied from the IBM format.

3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the 279X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for 279X operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

* Byte counts must be exact.

** Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage to any input with respect to V_{SS} = +7 to −0.5V
Operating temperature = 0°C to 70°C
Storage temperature = −55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage			10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	$I_O = -100\mu A$
V_{OL}	Output Low Voltage			0.45	V	$I_O = 1.6$ mA
V_{OHP}	Output High PUMP	2.2			V	$I_{OP} = -1.0$ mA
V_{OLP}	Output Low PUMP			0.2	V	$I_{OP} = +1.0$ mA
P_D	Power Dissipation			.75	W	All Outputs Open
R_{PU}	Internal Pull-up*	100		1700	μA	V_{IN} = 0V
I_{CC}	Supply Current		70	150	mA	All Outputs Open

* Internal Pull-up resistors on PINS 1, 17, 19, 22, 36, 37 and 40. Also pin 25 on 2791 and 3.

TIMING CHARACTERISTICS

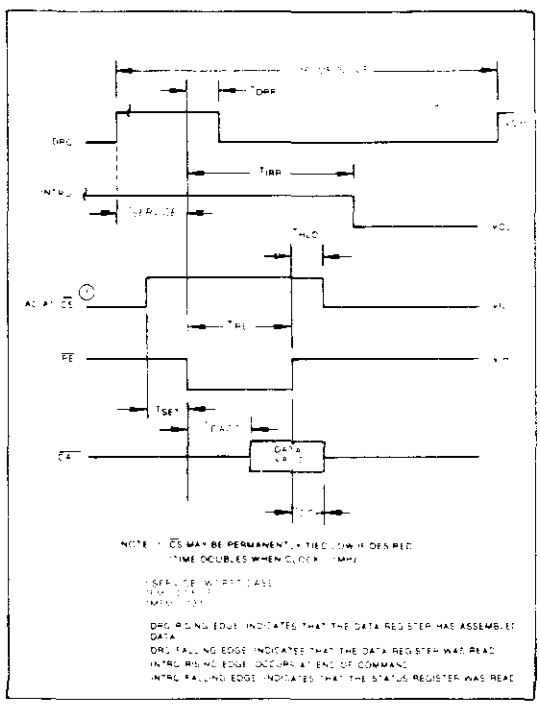
T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING

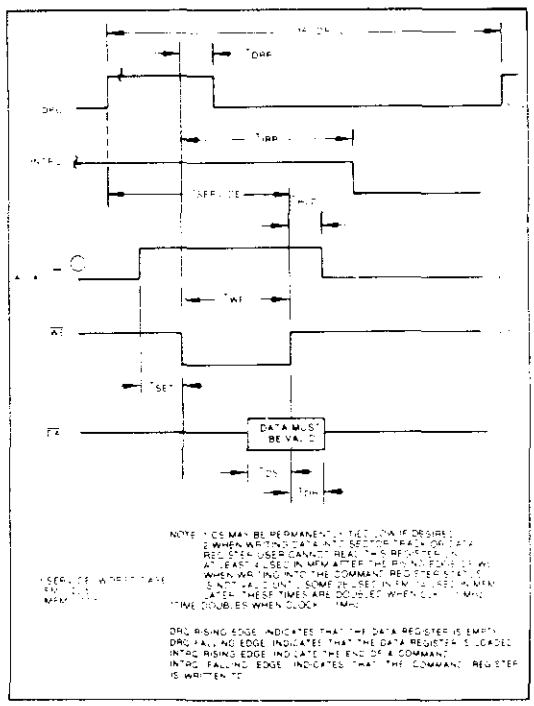
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{RE}$	50			nsec	
T_{HLD}	Hold ADDR & CS from $\overline{RE}$	10			nsec	
T_{RE}	$\overline{RE}$ Pulse Width	200			nsec	C_L = 50 pf
T_{DRR}	DRQ Reset from $\overline{RE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note
T_{DACC}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
T_{DOH}	Data Hold From $\overline{RE}$	20		150	nsec	C_L = 50 pf

WRITE ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{WE}$	50			nsec	
T_{HLD}	Hold ADDR & CS from $\overline{WE}$	10			nsec	
T_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
T_{DRR}	DRQ Reset from $\overline{WE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
T_{DS}	Data Setup to $\overline{WE}$	150			nsec	
T_{DH}	Data Hold from $\overline{WE}$	50			nsec	



READ ENABLE TIMING



WRITE ENABLE TIMING

INPUT DATA TIMING

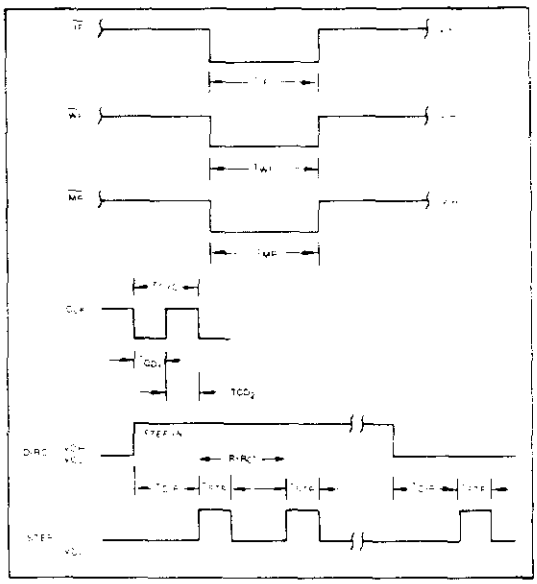
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{PW}	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	
T_{BC}	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz) (NO WRITE PRECOMPENSATION)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{WP}	Write Data Pulse Width	400	500	600	nsec	FM
		200	250	300	nsec	MFM
T_{WG}	Write Gate to Write Data		2		µsec	FM
			1		µsec	MFM
T_{WF}	Write Gate off from WD		2		µsec	FM
			1		µsec	MFM

MISCELLANEOUS TIMING:

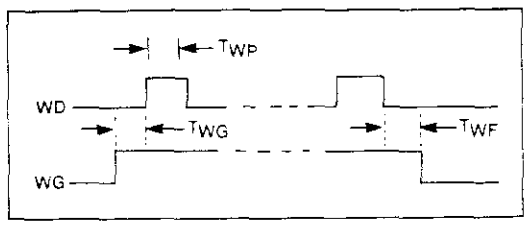
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{CD_1}	Clock Duty (low)	230	250	20000	nsec	
T_{CD_2}	Clock Duty (high)	230	250	20000	nsec	
T_{STP}	Step Pulse Output	2 or 4			µsec	See Note
T_{DIR}	Dir Setup to Step		12		µsec	± CLK ERROR
T_{MR}	Master Reset Pulse Width	50			µsec	
T_{IP}	Index Pulse Width	10			µsec	See Note
RPW	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
	Precomp Adjust.	100		300	nsec	MFM
WPW	Write Data Pulse Width					Precomp = 100 nsec
		200	300	400	nsec	MFM
WPW	Write Data Pulse Width					Precomp = 300 nsec
		600	900	1200	nsec	MFM
VCO	Free Run Voltage Controlled	6.0			MHz	Cext = 0
	Oscillator. Adjustable by ext. capacitor on Pin 26		4.0		MHz	Cext = 35 pf
	Pump Up ± 25%	5.0			MHz	PU = 2.2V Cext = 35 pf
VCO	Pump Down – 25%			3.0	MHz	$\overline{PD}$ = 0.2V Cext = 35 pf
	5% Change V_{CC}	3.8		4.2	MHz	Cext = 35 pf
VCO	T_A = 75°C	3.5			MHz	Cext = 35 pf
Cext	Adjustable external capacitor	20	45	100	pf	VCO = 4.0MHz nom
RCLK	Derived read clock = VCO ÷ 8, 16, 32					VCO = 4.0MHz
			500		KHz	$\overline{DDEN}$ = 0 5/$\overline{8}$ = 1
			250		KHz	$\overline{DDEN}$ = 0 5/$\overline{8}$ = 0
			250		KHz	$\overline{DDEN}$ = 1 5/$\overline{8}$ = 1
			125		KHz	$\overline{DDEN}$ = 1 5/$\overline{8}$ = 0
PU/DON	PU/$\overline{PD}$ time on (pulse width)			250 500	ns ns	MFM FM



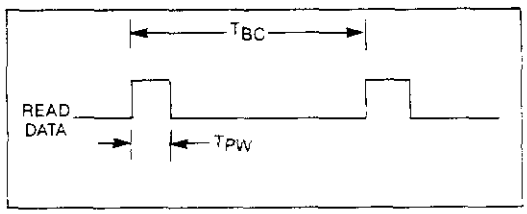
MISCELLANEOUS TIMING

NOTES:

1. Times double when clock = 1 MHz.
2. Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.



WRITE DATA TIMING



READ DATA TIMING

*FROM STEP RATE TABLE

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a Zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

SUMMARY OF ADJUSTMENT PROCEDURE

WRITE PRECOMPENSATION

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19).
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe pulse width on WD (Pin 31).
5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
6) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

DATA SEPARATOR

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19). Insure that 5/8, and $\overline{\text{DDEN}}$ are set properly.
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe Pulse Width on TG43 (Pin 29).
5) Adjust RPW (Pin 18) for 1/8 of the read clock (250ns for 8" DD, 500ns for 5¼" DD, etc.).
6) Observe Frequency on DIRC (Pin 16).
7) Adjust variable capacitor on VCO pin for Data Rate (500 KHz for 8" DD, 250 KHz for 5¼" DD, etc.).
8) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}}$ = 1 whenever a master reset pulse is applied.

Z8400
Z80® CPU Central Processing Unit

Zilog

Product Specification

September 1983

Features

- The instruction set contains 158 instructions. The 78 instructions of the 8080A are included as a subset; 8080A software compatibility is maintained.
- Eight MHz, 6 MHz, 4 MHz and 2.5 MHz clocks for the Z80H, Z80B, Z80A, and Z80 CPU result in rapid instruction execution with consequent high data throughput.
- The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers together with indexed and relative addressing result in the most powerful data handling capabilities in the microcomputer industry.
- The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system. This system may be daisy-chained to allow implementation of a priority interrupt scheme. Little, if any, additional logic is required for daisy-chaining.
- Duplicate sets of both general-purpose and flag registers are provided, easing the design and operation of system software through single-context switching, background-foreground programming, and single-level interrupt processing. In addition, two 16-bit index registers facilitate program processing of tables and arrays.
- There are three modes of high-speed interrupt processing: 8080 similar, non-Z80 peripheral device, and Z80 Family peripheral with or without daisy chain.
- On-chip dynamic memory refresh counter.

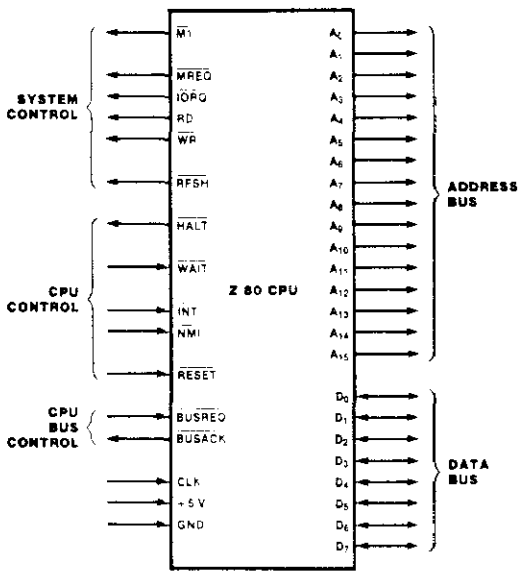


Figure 1. Pin Functions

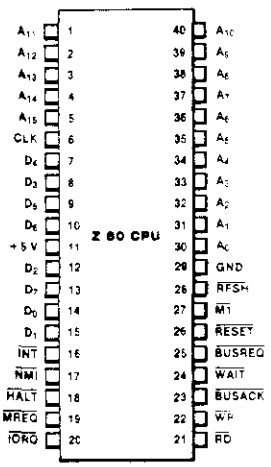


Figure 2. Pin Assignments

General Description

The Z80, Z80A, Z80B, and Z80H CPUs are third-generation single-chip microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second-and third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The Z80 also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5 V power source. All output signals are fully decoded and timed to control standard memory or peripheral circuits, and it is supported by an extensive family of peripheral controllers. The internal block diagram (Figure 3) shows the primary functions of the Z80 processors. Subsequent text provides more detail on the Z80 I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

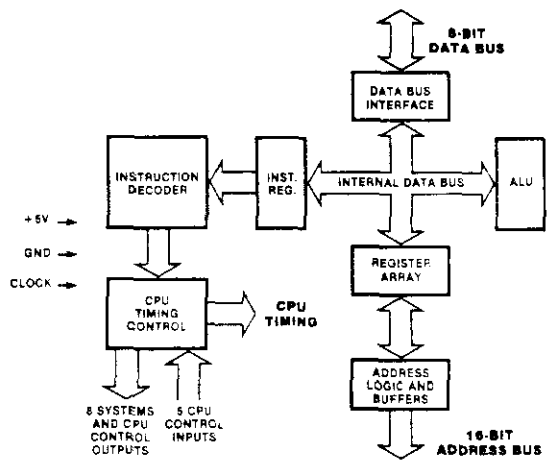


Figure 3. Z80 CPU Block Diagram

Z80 Microprocessor Family

The Zilog Z80 microprocessor is the central element of a comprehensive microprocessor product family. This family works together in most applications with minimum requirements for additional logic, facilitating the design of efficient and cost-effective microcomputer-based systems.

Zilog has designed five components to provide extensive support for the Z80 microprocessor. These are:

- The PIO (Parallel Input/Output) operates in both data-byte I/O transfer mode (with handshaking) and in bit mode (without handshaking). The PIO may be configured to interface with standard parallel peripheral devices such as printers, tape punches, and keyboards.
- The CTC (Counter/Timer Circuit) features four programmable 8-bit counter/timers, each of which has an 8-bit prescaler. Each of the four channels may be configured to operate in either counter or timer mode.
- The DMA (Direct Memory Access) controller provides dual port data transfer operations and the ability to terminate data transfer as a result of a pattern match.
- The SIO (Serial Input/Output) controller offers two channels. It is capable of operating in a variety of programmable modes for both synchronous and asynchronous communication, including Bi-Sync and SDLC.
- The DART (Dual Asynchronous Receiver/Transmitter) device provides low cost asynchronous serial communication. It has two channels and a full modem control interface.

Z80 CPU Registers

Figure 4 shows three groups of registers within the Z80 CPU. The first group consists of duplicate sets of 8-bit registers: a principal set and an alternate set (designated by ' [prime], e.g., A'). Both sets consist of the Accumulator Register, the Flag Register, and six general-purpose registers. Transfer of data between these duplicate sets of registers is accomplished by use of "Exchange" instructions. The result is faster response to interrupts and easy, efficient implementation of such versatile programming techniques as background-foreground data processing. The second set of registers consists of six registers with assigned functions. These are the I (Interrupt Register), the R (Refresh Register), the IX and IY (Index Registers), the SP (Stack Pointer), and the PC (Program Counter). The third group consists of two interrupt status flip-flops, plus an additional pair of flip-flops which assists in identifying the interrupt mode at any particular time. Table 1 provides further information on these registers.

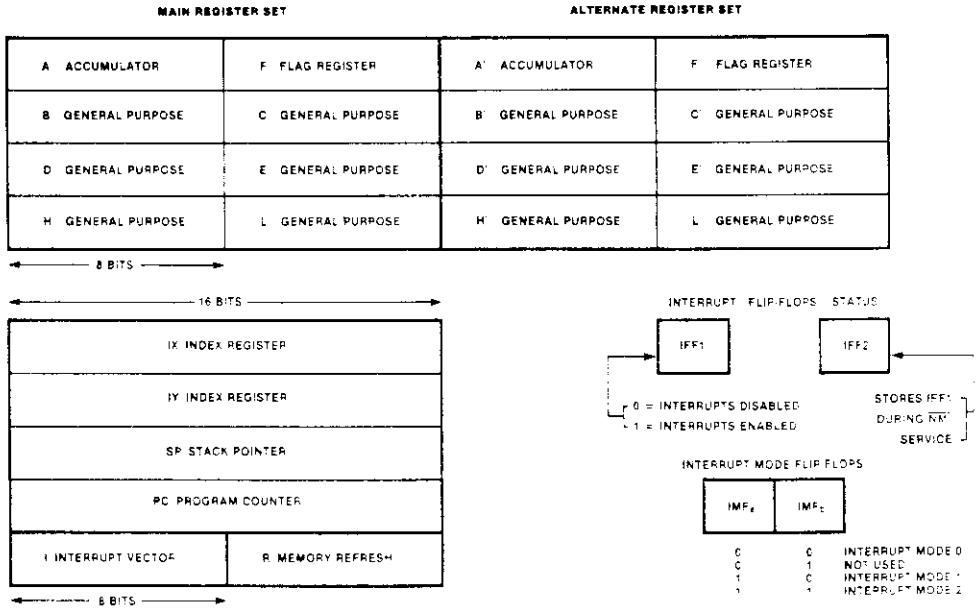


Figure 4. CPU Registers

Z80 CPU Registers (Continued)

Register		Size (Bits)	Remarks
A, A'	Accumulator	8	Stores an operand or the results of an operation.
F, F'	Flags	8	See Instruction Set.
B, B'	General Purpose	8	Can be used separately or as a 16-bit register with C.
C, C'	General Purpose	8	See B, above.
D, D'	General Purpose	8	Can be used separately or as a 16-bit register with E.
E, E'	General Purpose	8	See D, above.
H, H'	General Purpose	8	Can be used separately or as a 16-bit register with L.
L, L'	General Purpose	8	See H, above.
			Note: The (B,C), (D,E), and (H,L) sets are combined as follows: B — High byte C — Low byte D — High byte E — Low byte H — High byte L — Low byte
I	Interrupt Register	8	Stores upper eight bits of memory address for vectored interrupt processing.
R	Refresh Register	8	Provides user-transparent dynamic memory refresh. Lower seven bits are automatically incremented and all eight are placed on the address bus during each instruction fetch cycle refresh time.
IX	Index Register	16	Used for indexed addressing.
IY	Index Register	16	Same as IX, above.
SP	Stack Pointer	16	Holds address of the top of the stack. See Push or Pop in instruction set.
PC	Program Counter	16	Holds address of next instruction.
IFF_1-IFF_2	Interrupt Enable	Flip-Flops	Set or reset to indicate interrupt status (see Figure 4).
IMFa-IMFb	Interrupt Mode	Flip-Flops	Reflect interrupt mode (see Figure 4).

Table 1. Z80 CPU Registers

Interrupts: General Operation

The CPU accepts two interrupt input signals: $\overline{NMI}$ and $\overline{INT}$. The $\overline{NMI}$ is a non-maskable interrupt and has the highest priority. $\overline{INT}$ is a lower priority interrupt and it requires that interrupts be enabled in software in order to operate. $\overline{INT}$ can be connected to multiple peripheral devices in a wired-OR configuration.

The Z80 has a single response mode for interrupt service for the non-maskable interrupt. The maskable interrupt, $\overline{INT}$, has three programmable response modes available. These are:

- Mode 0 — similar to the 8080 microprocessor.
- Mode 1 — Peripheral Interrupt service, for use with non-8080/Z80 systems.
- Mode 2 — a vectored interrupt scheme, usually daisy-chained, for use with Z80 Family and compatible peripheral devices.

The CPU services interrupts by sampling the $\overline{NMI}$ and $\overline{INT}$ signals at the rising edge of the last clock of an instruction. Further interrupt service processing depends upon the type of interrupt that was detected. Details on interrupt responses are shown in the CPU Timing Section.

Interrupts: General Operation (Continued)

Non-Maskable Interrupt ($\overline{NMI}$). The non-maskable interrupt cannot be disabled by program control and therefore will be accepted at all times by the CPU. $\overline{NMI}$ is usually reserved for servicing only the highest priority type interrupts, such as that for orderly shutdown after power failure has been detected. After recognition of the $\overline{NMI}$ signal (providing $\overline{BUSREQ}$ is not active), the CPU jumps to restart location 0066H. Normally, software starting at this address contains the interrupt service routine.

Maskable Interrupt ($\overline{INT}$). Regardless of the interrupt mode set by the user, the Z80 response to a maskable interrupt input follows a common timing cycle. After the interrupt has been detected by the CPU (provided that interrupts are enabled and $\overline{BUSREQ}$ is not active) a special interrupt processing cycle begins. This is a special fetch ($\overline{M1}$) cycle in which $\overline{IORQ}$ becomes active rather than $\overline{MREQ}$, as in normal $\overline{M1}$ cycle. In addition, this special $\overline{M1}$ cycle is automatically extended by two $\overline{WAIT}$ states, to allow for the time required to acknowledge the interrupt request.

Mode 0 Interrupt Operation. This mode is similar to the 8080 microprocessor interrupt service procedures. The interrupting device places an instruction on the data bus. This is normally a Restart instruction, which will initiate a call to the selected one of eight restart locations in page zero of memory. Unlike the 8080, the Z80 CPU responds to the Call instruction with only one interrupt acknowledge cycle followed by two memory read cycles.

Mode 1 Interrupt Operation. Mode 1 operation is very similar to that for the $\overline{NMI}$. The principal difference is that the Mode 1 interrupt has a restart location of 0038H only.

Mode 2 Interrupt Operation. This interrupt mode has been designed to utilize most effectively the capabilities of the Z80 microprocessor and its associated peripheral family. The interrupting peripheral device selects the starting address of the interrupt service routine. It does this by placing an 8-bit vector on the data bus during the interrupt acknowledge cycle. The CPU forms a pointer using this byte as the lower 8-bits and the contents of the I register as the upper 8-bits. This points to an entry in a table of addresses for interrupt service routines. The CPU then jumps to the routine at that address. This flexibility in selecting the interrupt service routine address allows the peripheral device to use several different types of service routines. These routines may be located at any available location in memory. Since the interrupting device supplies the low-order byte of the 2-byte vector, bit 0 (A_0) must be a zero.

Interrupt Priority (Daisy Chaining and Nested Interrupts). The interrupt priority of each peripheral device is determined by its physical location within a daisy-chain configuration. Each device in the chain has an interrupt enable input line (IEI) and an interrupt enable output line (IEO), which is tied to the next lower priority device. The first device in the daisy chain has its IEI input hardwired to a High level. The first device has highest priority, while each succeeding device has a corresponding lower priority. This arrangement permits the CPU to select the highest priority interrupt from several simultaneously interrupting peripherals.

The interrupting device disables its IEO line to the next lower priority peripheral until it has been serviced. After servicing, its IEO line is raised, allowing lower priority peripherals to demand interrupt servicing.

The Z80 CPU will nest (queue) any pending interrupts or interrupts received while a selected peripheral is being serviced.

Interrupt Enable/Disable Operation. Two flip-flops, IFF_1 and IFF_2, referred to in the register description are used to signal the CPU interrupt status. Operation of the two flip-flops is described in Table 2. For more details, refer to the *Z80 CPU Technical Manual* and *Z80 Assembly Language Manual*.

Action	IFF_1	IFF_2	Comments
CPU Reset	0	0	Maskable interrupt $\overline{INT}$ disabled
DI instruction execution	0	0	Maskable interrupt $\overline{INT}$ disabled
EI instruction execution	1	1	Maskable interrupt $\overline{INT}$ enabled
LD A,I instruction execution	•	•	IFF_2 → Parity flag
LD A,R instruction execution	•	•	IFF_2 → Parity flag
Accept $\overline{NMI}$	0	IFF_1	IFF_1 → IFF_2 (Maskable interrupt $\overline{INT}$ disabled)
RETN instruction execution	IFF_2	•	IFF_2 → IFF_1 at completion of an $\overline{NMI}$ service routine.

Table 2. State of Flip-Flops

Instruction Set

The Z80 microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block *move for fast, efficient* data transfers within memory or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the Z80 instruction set and shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. The *Z80 CPU Technical Manual* (03-0029-01) and *Assembly Language Programming Manual* (03-0002-01) contain *significantly more details for programming* use.

The instructions are divided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges, block transfers, and searches
- 8-bit arithmetic and logic operations
- General-purpose arithmetic and CPU control
- 16-bit arithmetic operations
- Rotates and shifts
- Bit set, reset, and test operations
- Jumps
- Calls, returns, and restarts
- Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- Immediate
- Immediate extended
- Modified page zero
- Relative
- Extended
- Indexed
- Register
- Register indirect
- Implied
- Bit

8-Bit Load Group

Mnemonic	Symbolic Operation	Flags S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD r, r'	r ← r'	•	•	X	•	X	•	•	•	01 r r'		1	1	4	r, r' Reg
LD r, n	r ← n	•	•	X	•	X	•	•	•	00 r 110 ← n →		2	2	7	000 B 001 C
LD r, (HL)	r ← (HL)	•	•	X	•	X	•	•	•	01 r 110		1	2	7	010 D 011 E
LD r, (IX+d)	r ← (IX+d)	•	•	X	•	X	•	•	•	11 011 101 01 r 110 ← d →	DD	3	5	19	100 H 101 L 111 A
LD r, (IY+d)	r ← (IY+d)	•	•	X	•	X	•	•	•	11 111 101 01 r 110 ← d →	FD	3	5	19	
LD (HL), r	(HL) ← r	•	•	X	•	X	•	•	•	01 110 r		1	2	7	
LD (IX+d), r	(IX+d) ← r	•	•	X	•	X	•	•	•	11 011 101 01 110 r ← d →	DD	3	5	19	
LD (IY+d), r	(IY+d) ← r	•	•	X	•	X	•	•	•	11 111 101 01 110 r ← d →	FD	3	5	19	
LD (HL), n	(HL) ← n	•	•	X	•	X	•	•	•	00 110 110 ← n →	36	2	3	10	
LD (IX+d), n	(IX+d) ← n	•	•	X	•	X	•	•	•	11 011 101 00 110 110 ← d → ← n →	DD 36	4	5	19	
LD (IY+d), n	(IY+d) ← n	•	•	X	•	X	•	•	•	11 111 101 00 110 110 ← d → ← n →	FD 36	4	5	19	
LD A, (BC)	A ← (BC)	•	•	X	•	X	•	•	•	00 001 010	0A	1	2	7	
LD A, (DE)	A ← (DE)	•	•	X	•	X	•	•	•	00 011 010	1A	1	2	7	
LD A, (nn)	A ← (nn)	•	•	X	•	X	•	•	•	00 111 010 ← n → ← n →	3A	3	4	13	
LD (BC), A	(BC) ← A	•	•	X	•	X	•	•	•	00 000 010	02	1	2	7	
LD (DE), A	(DE) ← A	•	•	X	•	X	•	•	•	00 010 010	12	1	2	7	
LD (nn), A	(nn) ← A	•	•	X	•	X	•	•	•	00 110 010 ← n → ← n →	32	3	4	13	
LD A, I	A ← I	↕	↕	X	↕	X	IFF	0	•	11 101 101 01 010 111	ED 57	2	2	9	
LD A, R	A ← R	↕	↕	X	↕	X	IFF	0	•	11 101 101 01 011 111	ED 5F	2	2	9	
LD I, A	I ← A	•	•	X	•	X	•	•	•	11 101 101 01 000 111	ED 47	2	2	9	
LD R, A	R ← A	•	•	X	•	X	•	•	•	11 101 101 01 001 111	ED 4F	2	2	9	

NOTES: r, r' means any of the registers A, B, C, D, E, H, L.
IFF the contents of the interrupt enable flip-flop (IFF) is copied into the P/V flag.
If an interrupt occurs during execution of this instruction, the P/V flag contains a 0.

16-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd, nn	dd ← nn	•	•	X	•	•	•	00 dd0 001 ← n → ← n →	3	3	10	dd Pair 00 BC 01 DE 10 HL 11 SP
LD IX, nn	IX ← nn	•	•	X	•	•	•	11 011 101 DD 00 100 001 21 ← n → ← n →	4	4	14	
LD IY, nn	IY ← nn	•	•	X	•	•	•	11 111 101 FD 00 100 001 21 ← n → ← n →	4	4	14	
LD HL, (nn)	H ← (nn + 1) L ← (nn)	•	•	X	•	•	•	00 101 010 2A ← n → ← n →	3	5	16	
LD dd, (nn)	dd_H ← (nn + 1) dd_L ← (nn)	•	•	X	•	•	•	11 101 101 ED 01 dd1 011 ← n → ← n →	4	6	20	
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	•	•	X	•	•	•	11 011 101 DD 00 101 010 2A ← n → ← n →	4	6	20	
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	•	•	X	•	•	•	11 111 101 FD 00 101 010 2A ← n → ← n →	4	6	20	
LD (nn), HL	(nn + 1) ← H (nn) ← L	•	•	X	•	•	•	00 100 010 22 ← n → ← n →	3	5	16	
LD (nn), dd	(nn + 1) ← dd_H (nn) ← dd_L	•	•	X	•	•	•	11 101 101 ED 01 dd0 011 ← n → ← n →	4	6	20	
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	•	•	X	•	•	•	11 011 101 DD 00 100 010 22 ← n → ← n →	4	6	20	
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	•	•	X	•	•	•	11 111 101 FD 00 100 010 22 ← n → ← n →	4	6	20	
LD SP, HL	SP ← HL	•	•	X	•	•	•	11 111 001 F9	1	1	6	
LD SP, IX	SP ← IX	•	•	X	•	•	•	11 011 101 DD 11 111 001 F9	2	2	10	
LD SP, IY	SP ← IY	•	•	X	•	•	•	11 111 101 FD 11 111 001 F9	2	2	10	
PUSH qq	(SP - 2) ← qq_L (SP - 1) ← qq_H SP ← SP - 2	•	•	X	•	•	•	11 qq0 101	1	3	11	qq Pair 00 BC 01 DE 10 HL 11 AF
PUSH IX	(SP - 2) ← IX_L (SP - 1) ← IX_H SP ← SP - 2	•	•	X	•	•	•	11 011 101 DD 11 100 101 E5	2	4	15	
PUSH IY	(SP - 2) ← IY_L (SP - 1) ← IY_H SP ← SP - 2	•	•	X	•	•	•	11 111 101 FD 11 100 101 E5	2	4	15	
POP qq	qq_H ← (SP + 1) qq_L ← (SP) SP ← SP + 2	•	•	X	•	•	•	11 qq0 001	1	3	10	
POP IX	IX_H ← (SP + 1) IX_L ← (SP) SP ← SP + 2	•	•	X	•	•	•	11 011 101 DD 11 100 001 E1	2	4	14	
POP IY	IY_H ← (SP + 1) IY_L ← (SP) SP ← SP + 2	•	•	X	•	•	•	11 111 101 FD 11 100 001 E1	2	4	14	

NOTES: qq is any of the register pairs BC, DE, HL, SP.
qq is any of the register pairs AF, BC, DE, HL.
($PAIR_H$) ($PAIR_L$) refer to high order and low order eight bits of the register pair respectively.
e.g. BC_L = C, AF_H = A.

Exchange, Block Transfer, Block Search Groups

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	DE ↔ HL	•	•	X	•	X	•	•	11 101 011 EB	1	1	4	
EX AF, AF'	AF ↔ AF'	•	•	X	•	X	•	•	00 001 000 08	1	1	4	
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	•	•	X	•	X	•	•	11 011 001 D9	1	1	4	Register bank and auxiliary register bank exchange
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	•	•	X	•	X	•	•	11 100 011 E3	1	5	19	
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	•	•	X	•	X	•	•	11 011 101 DD 11 100 011 E3	2	6	23	
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	•	•	X	•	X	•	•	11 111 101 FD 11 100 011 E3	2	6	23	
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC - 1	•	•	X	○	X	0	•	11 101 101 ED 10 100 000 A0	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC - 1 Repeat until BC = 0	•	•	X	○	X	0	•	11 101 101 ED 10 110 000 B0	2 2	5 4	21 16	If BC ≠ 0 If BC = 0

NOTE: ○ = 0 if the result of register decrement is zero; = 1 if the result is non-zero.

Exchange, Block Transfer, Block Search Groups (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	•	•	X	0	X	↕ ①	11 101 101 ED 10 101 000 A8	2	4	16	
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	0	X	0 ②	11 101 101 ED 10 111 000 B8	2 2	5 4	21 16	If BC ≠ 0 If BC = 0
CPI	A − (HL) HL ← HL + 1 BC ← BC − 1	↕	↕ ③	X	↕	X	↕ ①	11 101 101 ED 10 100 001 A1	2	4	16	
CPIR	A − (HL) HL ← HL + 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	↕	↕ ③	X	↕	X	↕ ①	11 101 101 ED 10 110 001 B1	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	↕	↕ ③	X	↕	X	↕ ①	11 101 101 ED 10 101 001 A9	2	4	16	
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	↕	↕ ③	X	↕	X	↕ ①	11 101 101 ED 10 111 001 B9	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)

NOTES: ① P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1
② P/V flag is 0 at completion of instruction only
③ Z flag is 1 if A = (HL), otherwise Z = 0

8-Bit Arithmetic and Logical Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A, r	A ← A + r	↕	↕	X	↕	X	V	0	↕	10 000 r	1	1	4	r: Reg 000: B 001: C 010: D 011: E 100: H 101: L 111: A
ADD A, n	A ← A + n	↕	↕	X	↕	X	V	0	↕	11 000 110 ← n →	2	2	7	
ADD A, (HL)	A ← A + (HL)	↕	↕	X	↕	X	V	0	↕	10 000 110	1	2	7	
ADD A, (IX + d)	A ← A + (IX + d)	↕	↕	X	↕	X	V	0	↕	11 011 101 DD 10 000 110 ← d →	3	5	19	
ADD A, (IY + d)	A ← A + (IY + d)	↕	↕	X	↕	X	V	0	↕	11 111 101 FD 10 000 110 ← d →	3	5	19	
ADC A, s	A ← A + s + CY	↕	↕	X	↕	X	V	0	↕	001				s is any of r, n, (HL), (IX + d), (IY + d), as shown for ADD instructions. The indicated bits replace the 001 in the ADD set above
SUB s	A ← A − s	↕	↕	X	↕	X	V	1	↕	010				
SBC A, s	A ← A − s − CY	↕	↕	X	↕	X	V	1	↕	011				
AND s	A ← A ∧ s	↕	↕	X	1	X	P	0	0	100				
OR s	A ← A ∨ s	↕	↕	X	0	X	P	0	0	110				
XOR s	A ← A ⊕ s	↕	↕	X	0	X	P	0	0	101				
CP s	A − s	↕	↕	X	↕	X	V	1	↕	111				
INC r	r ← r + 1	↕	↕	X	↕	X	V	0	•	00 r 100	1	1	4	
INC (HL)	(HL) ← (HL) + 1	↕	↕	X	↕	X	V	0	•	00 110 100	1	3	11	
INC (IX + d)	(IX + d) ← (IX + d) + 1	↕	↕	X	↕	X	V	0	•	11 011 101 DD 00 110 100 ← d →	3	6	23	
INC (IY + d)	(IY + d) ← (IY + d) + 1	↕	↕	X	↕	X	V	0	•	11 111 101 FD 00 110 100 ← d →	3	6	23	
DEC m	m ← m − 1	↕	↕	X	↕	X	V	1	•	101				m is any of r, (HL), (IX + d), (IY + d), as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode

General-Purpose Arithmetic and CPU Control Groups

Mnemonic	Symbolic Operation	Flags S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
DAA	Converts acc. content into packed BCD following add or subtract with packed BCD operands.	↕	↕	X	↕	P	•	↕	00 100 111 27	1	1	4	Decimal adjust accumulator.
CPL	$A \leftarrow \overline{A}$	•	•	X	1	X	•	1	•	00 101 111 2F	1	1	4	Complement accumulator (one's complement)
NEG	$A \leftarrow 0 - A$	↕	↕	X	↕	X	V	1	↕	11 101 101 ED 01 000 100 44	2	2	8	Negate acc. (two's complement)
CCF	$CY \leftarrow \overline{CY}$	•	•	X	X	X	•	0	↕	00 111 111 3F	1	1	4	Complement carry flag
SCF	CY ← 1	•	•	X	0	X	•	0	1	00 110 111 37	1	1	4	Set carry flag.
NOP	No operation.	•	•	X	•	X	•	•	•	00 000 000 00	1	1	4	
HALT	CPU halted	•	•	X	•	X	•	•	•	01 110 110 76	1	1	4	
DI *	IFF ← 0	•	•	X	•	X	•	•	•	11 110 011 F3	1	1	4	
EI *	IFF ← 1	•	•	X	•	X	•	•	•	11 111 011 FB	1	1	4	
IM 0	Set interrupt mode 0	•	•	X	•	X	•	•	•	11 101 101 ED 01 000 110 46	2	2	8	
IM 1	Set interrupt mode 1	•	•	X	•	X	•	•	•	11 101 101 ED 01 010 110 56	2	2	8	
IM 2	Set interrupt mode 2	•	•	X	•	X	•	•	•	11 101 101 ED 01 011 110 5E	2	2	8	

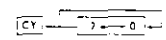
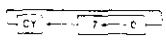
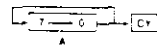
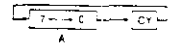
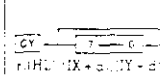
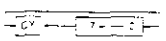
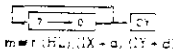
NOTES: IFF indicates the interrupt enable flip-flop.
CY indicates the carry flip-flop.
* indicates interrupts are not sampled at the end of EI or DI.

16-Bit Arithmetic Group

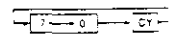
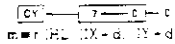
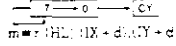
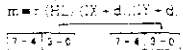
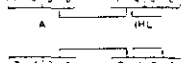
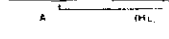
Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD HL, ss	HL ← HL + ss	•	•	X	X	X	•	0	↕	00 ss1 001	1	3	11	ss Reg 00 BC 01 DE 10 HL 11 SP
ADC HL, ss	HL ← HL + ss + CY	↕	↕	X	X	X	V	0	↕	11 101 101 ED 01 ss1 010	2	4	15	
SBC HL, ss	HL ← HL − ss − CY	↕	↕	X	X	X	V	1	↕	11 101 101 ED 01 ss0 010	2	4	15	
ADD IX, pp	IX ← IX + pp	•	•	X	X	X	•	0	↕	11 011 101 DD 00 pp1 001	2	4	15	pp Reg 00 BC 01 DE 10 IX 11 SP
ADD IY, rr	IY ← IY + rr	•	•	X	X	X	•	0	↕	11 111 101 FD 00 rr1 001	2	4	15	rr Reg 00 BC 01 DE 10 IY 11 SP
INC ss	ss ← ss + 1	•	•	X	•	X	•	•	•	00 ss0 011	1	1	6	
INC IX	IX ← IX + 1	•	•	X	•	X	•	•	•	11 011 101 DD 00 100 011 23	2	2	10	
INC IY	IY ← IY + 1	•	•	X	•	X	•	•	•	11 111 101 FD 00 100 011 23	2	2	10	
DEC ss	ss ← ss − 1	•	•	X	•	X	•	•	•	00 ss1 011	1	1	6	
DEC IX	IX ← IX − 1	•	•	X	•	X	•	•	•	11 011 101 DD 00 101 011 2B	2	2	10	
DEC IY	IY ← IY − 1	•	•	X	•	X	•	•	•	11 111 101 FD 00 101 011 2B	2	2	10	

NOTES: ss is any of the register pairs BC, DE, HL, SP.
pp is any of the register pairs BC, DE, IX, SP.
rr is any of the register pairs BC, DE, IY, SP.

Rotate and Shift Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA		•	•	X	0	X	•	0	↕	00 000 111 07	1	1	4	Rotate left circular accumulator
RLA		•	•	X	0	X	•	0	↕	00 010 111 17	1	1	4	Rotate left accumulator
RRCA		•	•	X	0	X	•	0	↕	00 001 111 0F	1	1	4	Rotate right circular accumulator
RRA		•	•	X	0	X	•	0	↕	00 011 111 1F	1	1	4	Rotate right accumulator
RLC r		↕	↕	X	0	X	P	0	↕	11 001 011 CB 00 000 r	2	2	8	Rotate left circular register r
RLC (HL)		↕	↕	X	0	X	P	0	↕	11 001 011 CB 00 000 110	2	4	15	r Reg 000 B 001 C 010 D 011 E 100 H 101 L 111 A
RLC (IX + d)	 r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	11 011 101 DD 11 001 011 CB — d — 00 000 110	4	6	23	
RLC (IY + d)		↕	↕	X	0	X	P	0	↕	11 111 101 FD 11 001 011 CB — d — 00 000 110	4	6	23	
RL m	 m ≡ r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	00 010 r				Instruction format and states are as shown for RLC s. To form new opcode replace 000 of RLC s with shown code
RRC m	 m ≡ r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	00 001 r				

Rotate and Shift Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RR m	 m ≡ r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	CB 00 011				
SLA m	 m ≡ r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	CB 00 100				
SRA m	 m ≡ r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	CB 00 101				
SRL m	 m ≡ r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	CB 00 111				
RLD		↕	↕	X	0	X	P	0	•	ED 01 101 111	6F	2	5	18	Rotate digit left and right between the accumulator and location (HL). The content of the upper half of the accumulator is unaffected.
RRD		↕	↕	X	0	X	P	0	•	ED 01 100 111	67	2	5	18	

Bit Set, Reset and Test Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
BIT b, r	$Z \leftarrow \overline{r_b}$	X	↕	X	1	X	X	0	•	CB 01 b r		2	2	8	r: 000 B, 001 C, 010 D, 011 E, 100 H, 101 L, 111 A. b: Bit Tested: 000 0, 001 1, 010 2, 011 3, 100 4, 101 5, 110 6, 111 7
BIT b, (HL)	$Z \leftarrow \overline{(HL)_b}$	X	↕	X	1	X	X	0	•	CB 01 b 110		2	3	12	
BIT b, (IX + d)	$Z \leftarrow \overline{(IX + d)_b}$	X	↕	X	1	X	X	0	•	DD CB d 01 b 110		4	5	20	
BIT b, (IY + d)	$Z \leftarrow \overline{(IY + d)_b}$	X	↕	X	1	X	X	0	•	FD CB d 01 b 110		4	5	20	
SET b, r	$r_b \leftarrow 1$	•	•	X	•	X	•	•	•	CB 11 b r		2	2	8	
SET b, (HL)	$(HL)_b \leftarrow 1$	•	•	X	•	X	•	•	•	CB 11 b 110		2	4	15	
SET b, (IX + d)	$(IX + d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	DD CB d 11 b 110		4	6	23	
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	FD CB d 11 b 110		4	6	23	
RES b, m	$m_b \leftarrow 0$ m ≡ r, (HL), (IX + d), (IY + d)	•	•	X	•	X	•	•	•	10					To form new opcode replace 11 of SET b, s with 10. Flags and time states for SET instruction.

NOTES: The notation m_b indicates bit b (0 to 7) of location m.

Jump Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP nn	PC ← nn	•	•	X	•	X	•	•	•	11 000 011 ← n → ← n →	C3	3	3	10	
JP cc, nn	If condition cc is true PC ← nn, otherwise continue	•	•	X	•	X	•	•	•	11 cc 010 ← n → ← n →		3	3	10	cc: 000 NZ, nonzero; 001 Z, zero; 010 NC, non-carry; 011 C, carry; 100 PO, parity odd; 101 PE, parity even; 110 P, sign positive; 111 M, sign negative
JR e	PC ← PC + e	•	•	X	•	X	•	•	•	00 011 000 ← e − 2 →	18	2	3	12	
JR C, e	If C = 0, continue If C = 1, PC ← PC + e	•	•	X	•	X	•	•	•	00 111 000 ← e − 2 →	38	2 2	2 3	7 12	If condition not met If condition is met
JR NC, e	If C = 1, continue If C = 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 110 000 ← e − 2 →	30	2 2	2 3	7 12	If condition not met If condition is met
JR Z, e	If Z = 0, continue If Z = 1, PC ← PC + e	•	•	X	•	X	•	•	•	00 101 000 ← e − 2 →	28	2 2	2 3	7 12	If condition not met If condition is met
JR NZ, e	If Z = 1, continue If Z = 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 100 000 ← e − 2 →	20	2 2	2 3	7 12	If condition not met If condition is met
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	11 101 001	E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	11 011 101 11 101 001	DD E9	2	2	8	

Jump Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11 111 101 FD 11 101 001 E9	2	2	8	
DJNZ e	B ← B − 1 If B = 0 continue If B ≠ 0 PC ← PC + e	•	•	X	•	X	•	•	•	00 010 000 10 ← e − 2 →	2 2	2 3	8 13	If B = 0. If B ≠ 0

NOTES: *e represents the extension in the relative addressing mode.*
e is a signed two's complement number in the range <−126, +129>.
e − 2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e.

Call and Return Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	•	•	X	•	X	•	•	•	11 001 101 CD ← n → ← n →	3	5	17	
CALL cc, nn	If condition cc is false continue otherwise same as CALL nn	•	•	X	•	X	•	•	•	11 cc 100 ← n → ← n →	3 3	3 5	10 17	If cc is false. If cc is true.
RET	PC_L ← (SP) PC_H ← (SP + 1)	•	•	X	•	X	•	•	•	11 001 001 C9	1	3	10	
RET cc	If condition cc is false continue otherwise same as RET	•	•	X	•	X	•	•	•	11 cc 000	1 1	1 3	5 11	If cc is false If cc is true.
RETI	Return from interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 001 101 4D	2	4	14	
RETN	Return from *non maskable* interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 000 101 45	2	4	14	
RST p	(SP − 1) ← PC_H (SP − 2) ← PC_L PC_H ← 0 PC_L ← p	•	•	X	•	X	•	•	•	11 t 111	1	3	11	t p 000 00H 001 08H 010 10H 011 18H 100 20H 101 28H 110 30H 111 38H

cc: Condition
000 NZ non-zero
001 Z zero
010 NC non-carry
011 C carry
100 PO parity odd
101 PE parity even
110 P *sign positive*
111 M sign negative

NOTE: *(RETN loads IFF_2 → IFF_1)*

Input and Output Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
IN A, (n)	A ← (n)	•	•	X	•	X	•	•	•	11 011 011 DB ← n →	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
IN r, (C)	r ← (C) if r ≠ 110 only the flags will be affected	‡	‡	X	‡	X	P	‡	•	11 101 101 ED 01 r 000	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INI	(HL) ← (C) B ← B − 1 HL ← HL + 1	X	‡	X	X	X	X	‡	X	11 101 101 ED 10 100 010 A2	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INIR	(HL) ← (C) B ← B − 1 HL ← HL + 1 Repeat until B = 0	X	1	X	X	X	X	‡	X	11 101 101 ED 10 110 010 B2	2 2	5 (If B ≠ 0) 4 (If B = 0)	21 16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
IND	(HL) ← (C) B ← B − 1 HL ← HL − 1	X	‡	X	X	X	X	‡	X	11 101 101 ED 10 101 010 AA	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INDR	(HL) ← (C) B ← B − 1 HL ← HL − 1 Repeat until B ≠ 0	X	1	X	X	X	X	‡	X	11 101 101 ED 10 111 010 BA	2 2	5 (If B ≠ 0) 4 (If B = 0)	21 16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OUT (n), A	(n) ← A	•	•	X	•	X	•	•	•	11 010 011 D3 ← n →	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
OUT (C), r	(C) ← r	•	•	X	•	X	•	•	•	11 101 101 ED 01 r 001	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	X	1	X	X	X	X	‡	X	11 101 101 ED 10 100 011 A3	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 Repeat until B = 0	X	1	X	X	X	X	‡	X	11 101 101 ED 10 110 011 B3	2 2	5 (If B ≠ 0) 4 (If B = 0)	21 16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	X	‡	X	X	X	X	‡	X	11 101 101 ED 10 101 011 AB	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}

NOTE: (1) If the result of B − 1 is zero the Z flag is set, otherwise it is reset.
(2) If the result of B − 1 is not zero, the PC is decremented by two and the instruction is repeated. Interrupts are recognized after each data transfer.

Input and Output Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 Repeat until B = 0	X	?	X	X	X	X	11 101 101 ED 10 111 011	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to A_0 − A_7 B to A_8 − A_{15}

NOTE: ? Flag is set upon instruction completion only.

Summary of Flag Operation

Instruction	D_7 S	Z		H		P/V	N	D_0 C	Comments
ADD A, s; ADC A, s	↕	↕	X	↕	X	V	0	↕	8-bit add or add with carry
SUB s; SBC A, s; CP s; NEG	↕	↕	X	↕	X	V	1	↕	8-bit subtract, subtract with carry, compare and negate accumulator.
AND s	↕	↕	X	1	X	P	0	0	Logical operations.
OR s; XOR s	↕	↕	X	0	X	P	0	0	
INC s	↕	↕	X	↕	X	V	0	•	8-bit increment.
DEC s	↕	↕	X	↕	X	V	1	•	8-bit decrement.
ADD DD, ss	•	•	X	X	X	•	0	↕	16-bit add.
ADC HL, ss	↕	↕	X	X	X	V	0	↕	16-bit add with carry.
SBC HL, ss	↕	↕	X	X	X	V	1	↕	16-bit subtract with carry.
RLA; RLCA; RRA; RRCA	•	•	X	0	X	•	0	↕	Rotate accumulator.
RL m; RLC m; RR m; RRC m; SLA m; SRA m; SRL m	↕	↕	X	0	X	P	0	↕	Rotate and shift locations.
RLD; RRD	↕	↕	X	0	X	P	0	•	Rotate digit left and right.
DAA	↕	↕	X	↕	X	P	•	↕	Decimal adjust accumulator.
CPL	•	•	X	1	X	•	1	•	Complement accumulator.
SCF	•	•	X	0	X	•	0	1	Set carry.
CCF	•	•	X	X	X	•	0	↕	Complement carry.
IN r, (C)	↕	↕	X	0	X	P	0	•	Input register indirect.
INI; IND; OUTI; OUTD	X	↕	X	X	X	X	1	•	Block input and output. Z = 0 if B ≠ 0 otherwise Z = 1.
INIR; INDR; OTIR; OTDR	X	1	X	X	X	X	1	•	
LDI; LDD	X	X	X	0	X	↕	0	•	Block transfer instructions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LDIR; LDDR	X	X	X	0	X	0	0	•	
CPI; CPIR; CPD; CPDR	X	↕	X	X	X	↕	1	•	Block search instructions. Z = 1 if A = (HL), otherwise Z = 0. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LD A, I; LD A, R	↕	↕	X	0	X	IFF	0	•	The content of the interrupt enable flip-flop (IFF) is copied into the P/V flag.
BIT b, s	X	↕	X	1	X	X	0	•	The state of bit b of location s is copied into the Z flag.

Symbolic Notation

Symbol	Operation
S	Sign flag. S = 1 if the MSB of the result is 1.
Z	Zero flag. Z = 1 if the result of the operation is 0.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V = 1 if the result of the operation is even. P/V = 0 if result is odd. If P/V holds overflow, P/V = 1 if the result of the operation produced an overflow.
H	Half-carry flag. H = 1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.
N	Add/Subtract flag. N = 1 if the previous operation was a subtract.
H & N	H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.
C	Carry/Link flag. C = 1 if the operation produced a carry from the MSB of the operand or result.

Symbol	Operation
↕	The flag is affected according to the result of the operation.
•	The flag is unchanged by the operation.
0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a "don't care."
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
ii	Any one of the two index registers IX or IY.
R	Refresh counter.
n	8-bit value in range < 0, 255 >.
nn	16-bit value in range < 0, 65535 >.

Pin Descriptions

A_0-A_{15}. *Address Bus* (output, active High, 3-state). A_0-A_{15} form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

$\overline{BUSACK}$. *Bus Acknowledge* (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ have entered their high-impedance states. The external circuitry can now control these lines.

$\overline{BUSREQ}$. *Bus Request* (input, active Low). Bus Request has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle. $\overline{BUSREQ}$ forces the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, RD, and WR to go to a high-impedance state so that other devices can control these lines. $\overline{BUSREQ}$ is normally wire-ORed and requires an external pullup for these applications. Extended $\overline{BUSREQ}$ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

D_0-D_7. *Data Bus* (input/output, active High, 3-state). D_0-D_7 constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

$\overline{HALT}$. *Halt State* (output, active Low). $\overline{HALT}$ indicates that the CPU has executed a Halt instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

$\overline{INT}$. *Interrupt Request* (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. $\overline{INT}$ is normally wire-ORed and requires an external pullup for these applications.

$\overline{IORQ}$. *Input/Output Request* (output, active Low, 3-state). $\overline{IORQ}$ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. $\overline{IORQ}$ is also generated concurrently with $\overline{M1}$ during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

$\overline{M1}$. *Machine Cycle One* (output, active Low). $\overline{M1}$, together with $\overline{MREQ}$, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. M1, together with IORQ, indicates an interrupt acknowledge cycle.

$\overline{MREQ}$. *Memory Request* (output, active Low, 3-state). $\overline{MREQ}$ indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{NMI}$. *Non-Maskable Interrupt* (input, negative edge-triggered). $\overline{NMI}$ has a higher priority than $\overline{INT}$. $\overline{NMI}$ is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

$\overline{RD}$. *Read* (output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{RESET}$. *Reset* (input, active Low). $\overline{RESET}$ initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that $\overline{RESET}$ must be active for a minimum of three full clock cycles before the reset operation is complete.

$\overline{RFSH}$. *Refresh* (output, active Low). $\overline{RFSH}$, together with $\overline{MREQ}$, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

$\overline{WAIT}$. *Wait* (input, active Low). $\overline{WAIT}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended $\overline{WAIT}$ periods can prevent the CPU from refreshing dynamic memory properly.

$\overline{WR}$. *Write* (output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

CPU Timing

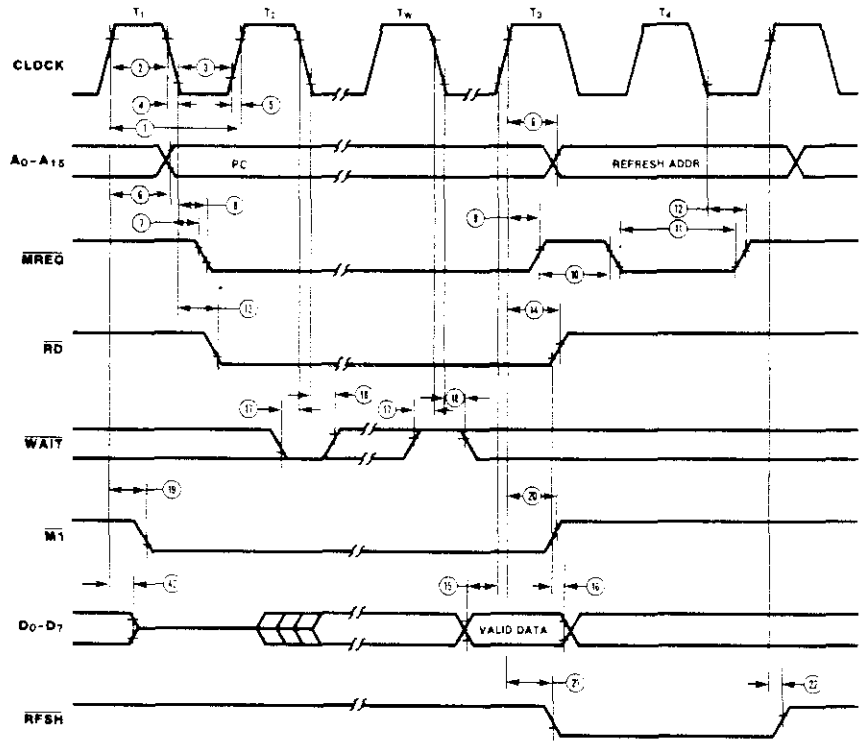
The Z80 CPU executes instructions by proceeding through a specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a T time or cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Instruction Opcode Fetch. The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 5). Approximately one-half clock cycle later, $\overline{MREQ}$ goes active. When active, $\overline{RD}$ indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the $\overline{WAIT}$ input with the falling edge of clock state T_2. During clock states T_3 and T_4 of an $\overline{M1}$ cycle dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction. When the Refresh Control signal becomes active, refreshing of dynamic memory can take place.



NOTE: T_W-Wait cycle added when necessary for slow ancillary devices.

Figure 5. Instruction Opcode Fetch

CPU Timing (Continued)

Memory Read or Write Cycles. Figure 6 shows the timing of memory read or write cycles other than an opcode fetch ($\overline{M1}$) cycle. The $\overline{MREQ}$ and $\overline{RD}$ signals function exactly as in the fetch cycle. In a memory write cycle, $\overline{MREQ}$ also becomes active when the address bus is stable. The $\overline{WR}$ line is active when the data bus is stable, so that it can be used directly as an R/$\overline{W}$ pulse to most semiconductor memories.

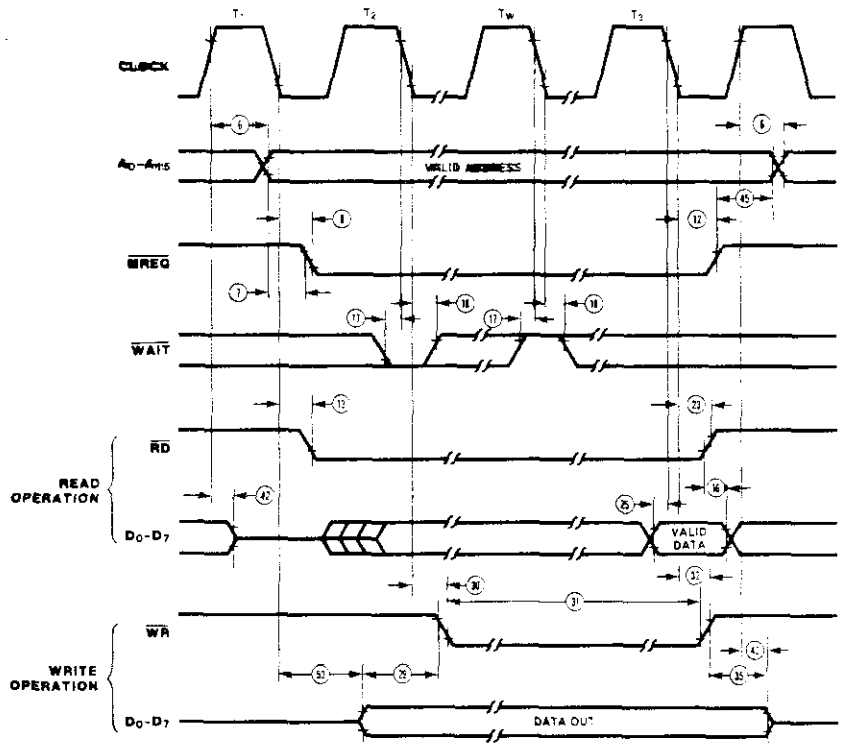
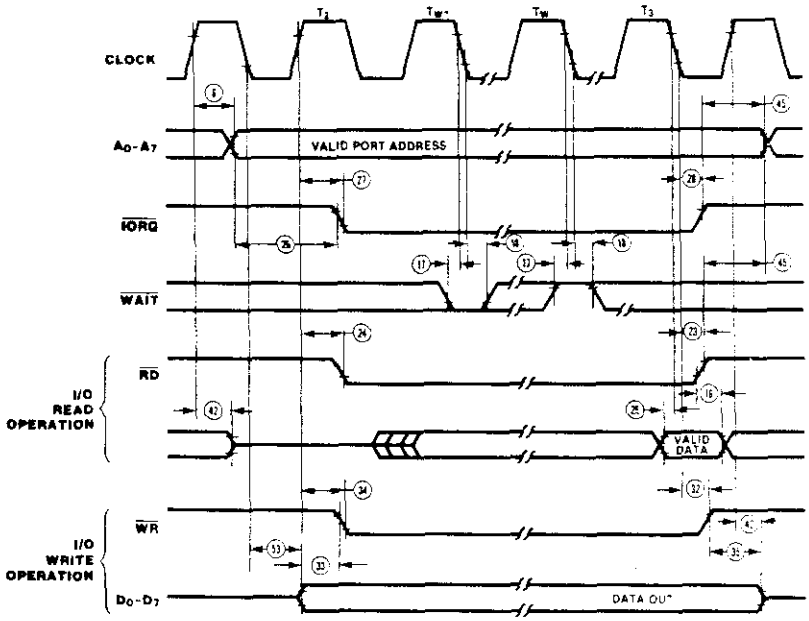


Figure 6. Memory Read or Write Cycles

CPU Timing (Continued)

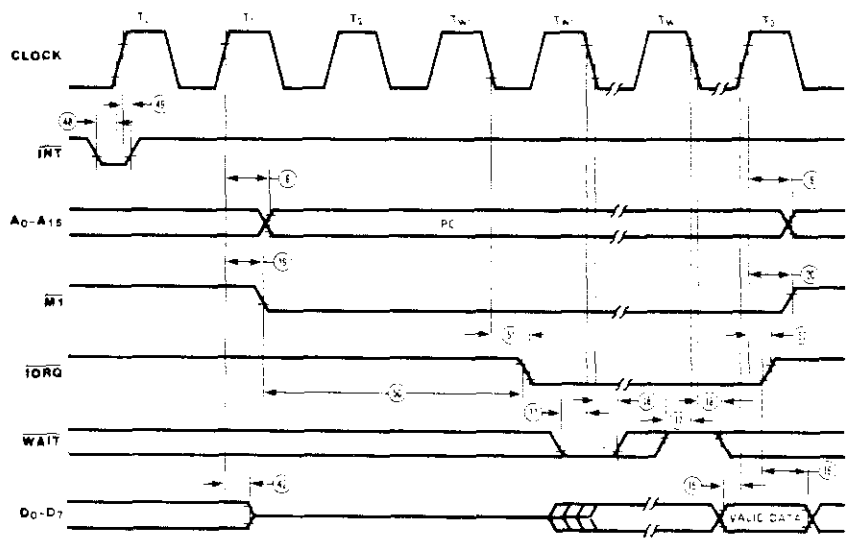
Input or Output Cycles. Figure 7 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state (T_W). This extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.



NOTE: T_W* = One Wait cycle automatically inserted by CPU.

Figure 7. Input or Output Cycles

Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 8). When an interrupt is accepted, a special $\overline{M1}$ cycle is generated. During this $\overline{M1}$ cycle, $\overline{IORQ}$ becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.

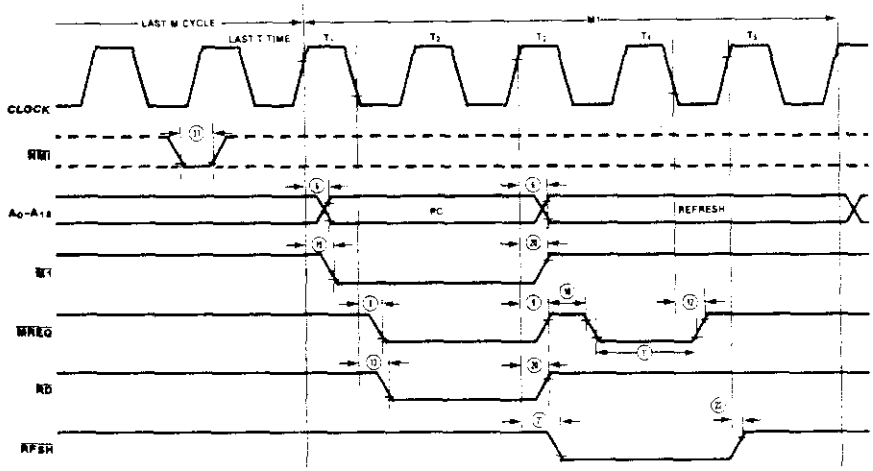


NOTE: 1. T_L = Last state of previous instruction. 2) Two Wait cycles automatically inserted by CPU(*).

Figure 8. Interrupt Request/Acknowledge Cycle

CPU Timing (Continued)

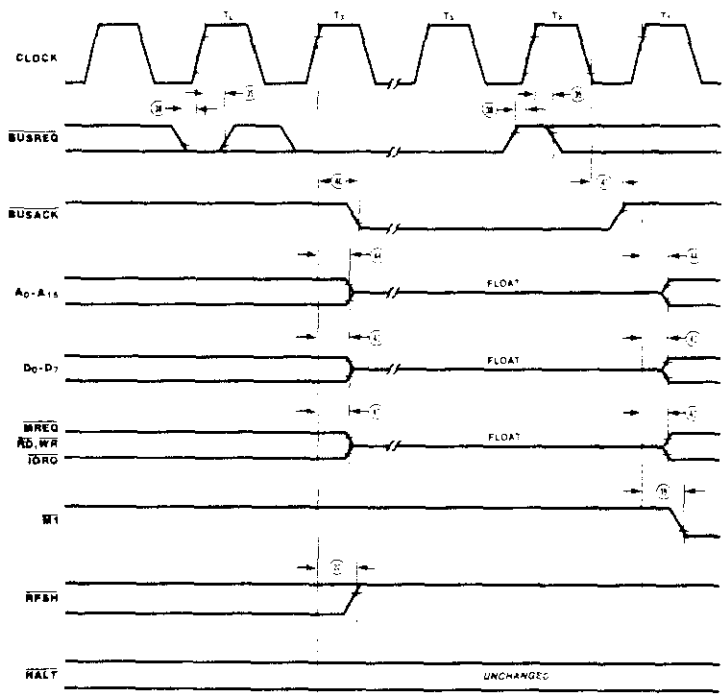
Non-Maskable Interrupt Request Cycle. $\overline{NMI}$ is sampled at the same time as the maskable interrupt input $\overline{INT}$ but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal instruction fetch except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the $\overline{NMI}$ service routine located at address 0066H (Figure 9).



*Although $\overline{NMI}$ is an asynchronous input to guarantee its being recognized on the following machine cycle, $\overline{NMI}$'s falling edge must occur no later than the rising edge of the clock cycle preceding T_{LAST}.

Figure 9. Non-Maskable Interrupt Request Operation

Bus Request/Acknowledge Cycle. The CPU samples $\overline{BUSREQ}$ with the rising edge of the last clock period of any machine cycle (Figure 10). If $\overline{BUSREQ}$ is active, the CPU sets its address, data, and $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ lines to a high-impedance state with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.

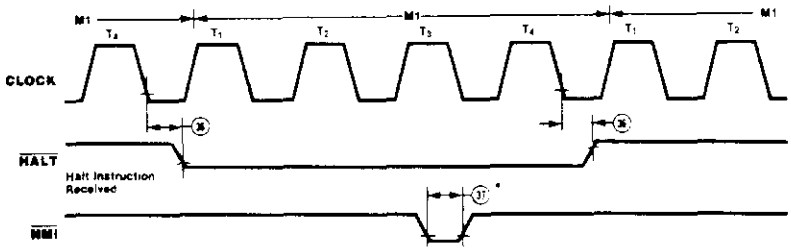


NOTE: T_L = Last state of any M cycle. T_X = An arbitrary clock cycle used by requesting device.

Figure 10. Z-BUS Request/Acknowledge Cycle

CPU Timing (Continued)

Halt Acknowledge Cycle. When the CPU receives a Halt instruction, it executes NOP states until either an $\overline{INT}$ or $\overline{NMI}$ input is received. When in the Halt state, the $\overline{HALT}$ output is active and remains so until an interrupt is received (Figure 11).



NOTE: $\overline{INT}$ will also force a Halt exit.

*See note, Figure 9.

Figure 11. Halt Acknowledge Cycle

Reset Cycle. $\overline{RESET}$ must be active for at least three clock cycles for the CPU to properly accept it. As long as $\overline{RESET}$ remains active, the address and data buses float, and the control outputs are inactive. Once $\overline{RESET}$ goes inactive, three internal T cycles are consumed before the CPU resumes normal processing operation. $\overline{RESET}$ clears the PC register, so the first opcode fetch will be to location 0000 (Figure 12).

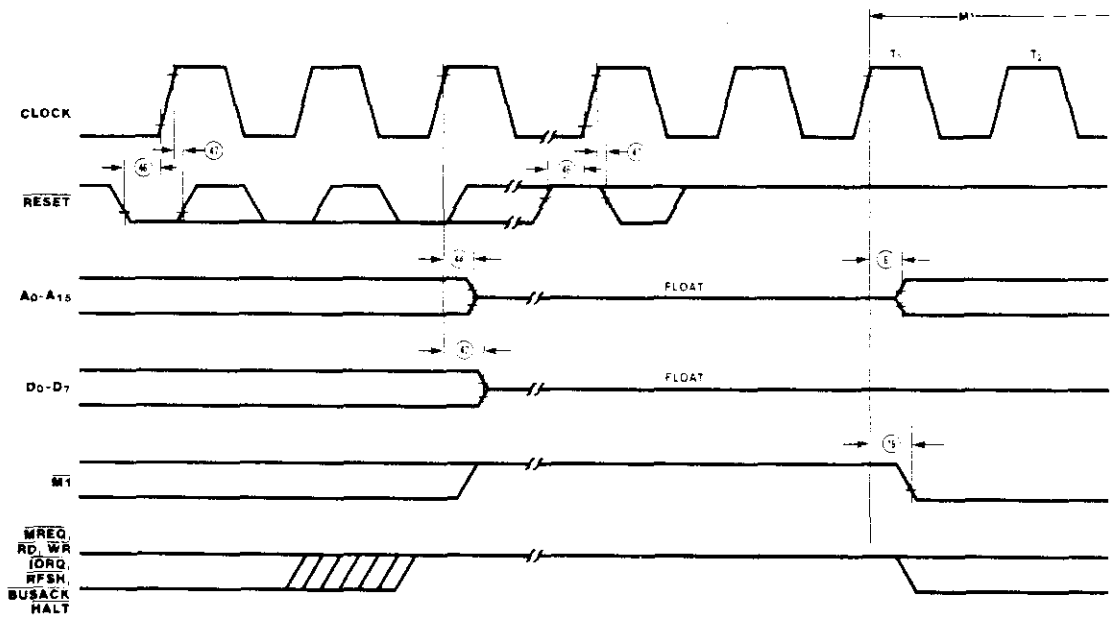


Figure 12. Reset Cycle

AC Characteristics

Number	Symbol	Parameter	Z80 CPU Min	Z80 CPU Max	Z80A CPU Min	Z80A CPU Max	Z80B CPU Min	Z80B CPU Max	Z80H CPU† Min	Z80H CPU† Max
1	TcC	Clock Cycle Time	400*		250*		165*		125*	
2	TwCh	Clock Pulse Width (High)	180*		110*		65*		55*	
3	TwCl	Clock Pulse Width (Low)	180	2000	110	2000	65	2000	55	2000
4	TfC	Clock Fall Time	—	30	—	30	—	20	—	10
5	TrC	Clock Rise Time	—	30	—	30	—	20	—	10
6	TdCr(A)	Clock ↑ to Address Valid Delay	—	145	—	110	—	90	—	80
7	TdA(MREQf)	Address Valid to $\overline{MREQ}$ ↓ Delay	125*	—	65*	—	35*	—	20*	—
8	TdCf(MREQf)	Clock ↓ to $\overline{MREQ}$ ↓ Delay	—	100	—	85	—	70	—	60
9	TdCr(MREQr)	Clock ↑ to $\overline{MREQ}$ ↑ Delay	—	100	—	85	—	70	—	60
10	TwMREQh	$\overline{MREQ}$ Pulse Width (High)	170*		110*		65*		45*	
11	TwMREQl	$\overline{MREQ}$ Pulse Width (Low)	360*	—	220*	—	135*	—	100*	—
12	TdCf(MREQr)	Clock ↓ to $\overline{MREQ}$ ↑ Delay	—	100	—	85	—	70	—	60
13	TdCf(RDf)	Clock ↓ to $\overline{RD}$ ↓ Delay	—	130	—	95	—	80	—	70
14	TdCr(RDr)	Clock ↑ to $\overline{RD}$ ↑ Delay	—	100	—	85	—	70	—	60
15	TsD(Cr)	Data Setup Time to Clock ↑	50		35		30		30	
16	ThD(RDr)	Data Hold Time to $\overline{RD}$ ↑	—	0	—	0	—	0	—	0
17	TsWAIT(Cf)	$\overline{WAIT}$ Setup Time to Clock ↓	70	—	70	—	60	—	50	—
18	ThWAIT(Cf)	$\overline{WAIT}$ Hold Time after Clock ↓	—	0	—	0	—	0	—	0
19	TdCr(M1f)	Clock ↑ to $\overline{M1}$ ↓ Delay	—	130	—	100	—	80	—	70
20	TdCr(M1r)	Clock ↑ to $\overline{M1}$ ↑ Delay	—	130	—	100	—	80	—	70
21	TdCr(RFSHf)	Clock ↑ to $\overline{RFSH}$ ↓ Delay	—	180	—	130	—	110	—	95
22	TdCr(RFSHr)	Clock ↑ to $\overline{RFSH}$ ↑ Delay	—	150	—	120	—	100	—	85
23	TdCf(RDr)	Clock ↓ to $\overline{RD}$ ↑ Delay	—	110	—	85	—	70	—	60
24	TdCr(RDf)	Clock ↑ to $\overline{RD}$ ↓ Delay	—	100	—	85	—	70	—	60
25	TsD(Cf)	Data Setup to Clock ↓ during M_2, M_3, M_4 or M_5 Cycles	60		50		40		30	
26	TdA(IORQf)	Address Stable prior to $\overline{IORQ}$ ↓	320*	—	180*	—	110*	—	75*	—
27	TdCr(IORQf)	Clock ↑ to $\overline{IORQ}$ ↓ Delay	—	90	—	75	—	65	—	55
28	TdCf(IORQr)	Clock ↓ to $\overline{IORQ}$ ↑ Delay	—	110	—	85	—	70	—	60
29	TdD(WRf)	Data Stable prior to $\overline{WR}$ ↓	190*	—	80*	—	25*	—	5*	—
30	TdCf(WRf)	Clock ↓ to $\overline{WR}$ ↓ Delay	—	90	—	80	—	70	—	60
31	TwWR	$\overline{WR}$ Pulse Width	360*	—	220*	—	135*	—	100*	—
32	TdCf(WRr)	Clock ↓ to $\overline{WR}$ ↑ Delay	—	100	—	80	—	70	—	60
33	TdD(WRf)	Data Stable prior to $\overline{WR}$ ↓	20*	—	-10*	—	-55*	—	55*	—
34	TdCr(WRf)	Clock ↑ to $\overline{WR}$ ↓ Delay	—	80	—	65	—	60	—	55
35	TdWRr(D)	Data Stable from $\overline{WR}$ ↑	120*		60*		30*		15*	
36	TdCr(HALT)	Clock ↑ to $\overline{HALT}$ ↑ or ↓	—	300	—	300	—	260	—	225
37	TwNMI	$\overline{NMI}$ Pulse Width	80	—	80	—	70	—	60*	—
38	TsBUSREQ(Cr)	$\overline{BUSREQ}$ Setup Time to Clock ↑	80	—	50	—	50	—	40	—

*For clock periods other than the minimums shown in the table, calculate parameters using the next lowest value in the table on the same line.

† Units in nanoseconds (ns). All timings are preliminary and subject to change.

AC Characteristics (Continued)

Number	Symbol	Parameter	Z80 CPU Min	Z80 CPU Max	Z80A CPU Min	Z80A CPU Max	Z80B CPU Min	Z80B CPU Max	Z80H CPU† Min	Z80H CPU† Max
39	ThBUSREQ(Cr)	$\overline{BUSREQ}$ Hold Time after Clock ↑	0	—	0	—	0	—	0	—
40	TdCr(BUSACKf)	Clock ↑ to $\overline{BUSACK}$ ↓ Delay		120		100		90	—	80
41	TdCf(BUSACKr)	Clock ↓ to $\overline{BUSACK}$ ↑ Delay	—	110	—	100	—	90	—	80
42	TdCr(Dz)	Clock ↑ to Data Float Delay	—	90	—	90	—	80	—	70
43	TdCr(CTz)	Clock ↑ to Control Outputs Float Delay ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$)	—	110	—	80	—	70	—	60
44	TdCr(Az)	Clock ↑ to Address Float Delay	—	110	—	90	—	80	—	70
45	TdCTr(A)	$\overline{MREQ}$ ↑, $\overline{IORQ}$ ↑, $\overline{RD}$ ↑, and $\overline{WR}$ ↑ to Address Hold Time	160*		80*		35*		20*	—
46	TsRESET(Cr)	$\overline{RESET}$ to Clock ↑ Setup Time	90	—	60	—	60	—	45	—
47	ThRESET(Cr)	$\overline{RESET}$ to Clock ↑ Hold Time	—	0	—	0	—	0	—	0
48	TsINTf(Cr)	$\overline{INT}$ to Clock ↑ Setup Time	80	—	80	—	70	—	55	—
49	ThINTr(Cr)	$\overline{INT}$ to Clock ↑ Hold Time	—	0	—	0	—	0	—	0
50	TdM1f(IORQf)	$\overline{M1}$ ↓ to $\overline{IORQ}$ ↓ Delay	920*		565*		365*		270*	—
51	TdCf(IORQf)	Clock ↓ to $\overline{IORQ}$ ↓ Delay	—	110	—	85	—	70	—	60
52	TdCf(IORQr)	Clock ↓ to $\overline{IORQ}$ ↑ Delay	—	100	—	85	—	70	—	60
53	TdCf(D)	Clock ↓ to Data Valid Delay	—	230	—	150	—	130	—	115

*For clock periods other than the minimums shown in the table, calculate parameters using the following expressions. Calculated values above assumed TrC = TfC = 20 ns.
† Units in nanoseconds (ns). All timings are preliminary and subject to change.

Footnotes to AC Characteristics

Number	Symbol	Z80	Z80A	Z80B
1	TcC	TwCh + TwCl + TrC + TfC	TwCh + TwCl + TrC + TfC	TwCh + TwCl + TrC + TfC
2	TwCh	Although static by design, TwCh of greater than 200 μs is not guaranteed	Although static by design, TwCh of greater than 200 μs is not guaranteed	Although static by design, TwCh of greater than 200 μs is not guaranteed
7	TdA(MREQf)	TwCh + TfC − 75	TwCh + TfC − 65	TwCh + TfC − 50
10	TwMREQh	TwCh + TfC − 30	TwCh + TfC − 20	TwCh + TfC − 20
11	TwMREQl	TcC − 40	TcC − 30	TcC − 30
26	TdA(IORQf)	TcC − 80	TcC − 70	TcC − 55
29	TdD(WRf)	TcC − 210	TcC − 170	TcC − 140
31	TwWR	TcC − 40	TcC − 30	TcC − 30
33	TdD(WRf)	TwCl + TrC − 180	TwCl + TrC − 140	TwCl + TrC − 140
35	TdWRr(D)	TwCl + TrC − 80	TwCl + TrC − 70	TwCl + TrC − 55
45	TdCTr(A)	TwCl + TrC − 40	TwCl + TrC − 50	TwCl + TrC − 50
50	TdM1f(IORQf)	2TcC + TwCh + TfC − 80	2TcC + TwCh + TfC − 65	2TcC + TwCh + TfC − 50

AC Test Conditions:
V_{IH} = 2.0 V
V_{IL} = 0.8 V
V_{IHC} = V_{CC} −0.6 V
V_{ILC} = 0.45 V
V_{OH} = 2.0 V
V_{OL} = 0.8 V
FLOAT = ±0.5 V

Absolute Maximum Ratings

Storage Temperature . . . . . -65°C to +150°C
Temperature under Bias . . . . . Specified operating range
Voltages on all inputs and outputs with respect to ground . -0.3 V to +7 V
Power Dissipation . . . . . 1.5 W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

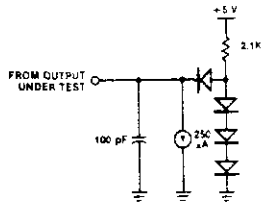
Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0 V). Positive current flows into the referenced pin. Available operating temperature ranges are:

- S* = 0°C to +70°C, +4.75 V ≤ V_{CC} ≤ +5.25 V
- E* = -40°C to +85°C, +4.75 V ≤ V_{CC} ≤ +5.25 V
- M* = -55°C to +125°C, +4.5 V ≤ V_{CC} ≤ +5.5 V

*See Ordering Information section for package temperature range and product number.

All ac parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for address and control lines.



DC Characteristics

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-.6	V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 1.8 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -250 μA
I_{CC}	Power Supply Current				
	Z80		150[1]	mA	
	Z80A		200[2]	mA	
	Z80B		200	mA	
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to V_{CC}
I_{LL}	3-State Output Leakage Current in Float	-10	10[3]	μA	V_{OUT} = 0.4 to V_{CC}

1. For military grade parts I_{CC} is 200 mA.
2. Typical rate for Z80A is 80 mA.
3. A_{15}-A_0, D_7-D_0, MREQ, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$.

Capacitance

Symbol	Parameter	Min	Max	Unit	Note
C_{CLOCK}	Clock Capacitance		35	pF	Unmeasured pins returned to ground
C_{IN}	Input Capacitance		5	pF	
C_{OUT}	Output Capacitance		10	pF	

T_A = 25°C, f = 1 MHz

Ordering Information

Product Number	Package/ Temp	Speed	Description	Product Number	Package/ Temp	Speed	Description
Z8400	CE	2.5 MHz	Z80 CPU (40-pin)	Z8400A	CMB	4.0 MHz	Z80A CPU (40-pin
Z8400	CM	2.5 MHz	Same as above	Z8400A	CS	4.0 MHz	Same as above
Z8400	CMB	2.5 MHz	Same as above	Z8400A	DE	4.0 MHz	Same as above
Z8400	CS	2.5 MHz	Same as above	Z8400A	DS	4.0 MHz	Same as above
Z8400	DE	2.5 MHz	Same as above	Z8400A	PE	4.0 MHz	Same as above
Z8400	DS	2.5 MHz	Same as above	Z8400A	PS	4.0 MHz	Same as above
Z8400	PE	2.5 MHz	Same as above	Z8400B	CS	6.0 MHz	Z80B CPU (40-pin
Z8400	PS	2.5 MHz	Same as above	Z8400B	DS	6.0 MHz	Same as above
Z8400A	CE	4.0 MHz	Z80A CPU (40-pin)	Z8400B	PS	6.0 MHz	Same as above
Z8400A	CM	4.0 MHz	Same as above				

*NOTES: C = Ceramic, D = Cerdip, P = Plastic; E = -40°C to +85°C, M = -55°C to +125°C, MB = -55°C to +125°C with MIL-STD-883 Class B processing, S = 0°C to +70°C

Z8420
Z80® PIO Parallel Input/Output Controller

Zilog

Product Specification

September 1983

Features

- Provides a direct interface between Z-80 microcomputer systems and peripheral devices.
- Both ports have interrupt-driven handshake for fast response.
- Four programmable operating modes: byte input, byte output, byte input/output (Port A only), and bit input/output.
- Programmable interrupts on peripheral status conditions.
- Standard Z-80 Family bus-request and prioritized interrupt-request daisy chains implemented without external logic.
- The eight Port B outputs can drive Darlington transistors (1.5 mA at 1.5 V).

General Description

The Z-80 PIO Parallel I/O Circuit is a programmable, dual-port device that provides a TTL-compatible interface between peripheral devices and the Z-80 CPU. The CPU configures the Z-80 PIO to interface with a wide range of peripheral devices with no other external logic. Typical peripheral devices that are compatible with the Z-80 PIO include most keyboards, paper tape readers and punches, printers, PROM programmers, etc.

One characteristic of the Z-80 peripheral controllers that separates them from other interface controllers is that all data transfer between the peripheral device and the CPU is accomplished under interrupt control. Thus, the interrupt logic of the PIO permits full use of the efficient interrupt capabilities of the Z-80 CPU during I/O transfers. All logic necessary to implement a fully nested interrupt structure is included in the PIO.

Another feature of the PIO is the ability to interrupt the CPU upon occurrence of specified status conditions in the peripheral device. For example, the PIO can be programmed to interrupt if any specified peripheral alarm conditions should occur. This interrupt capability reduces the time the processor must spend in polling peripheral status.

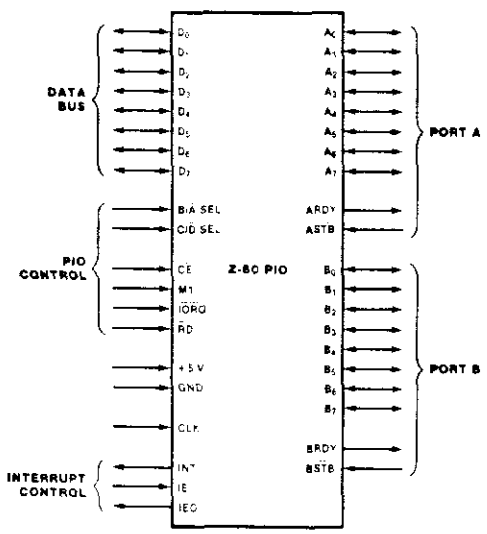


Figure 1. Pin Functions

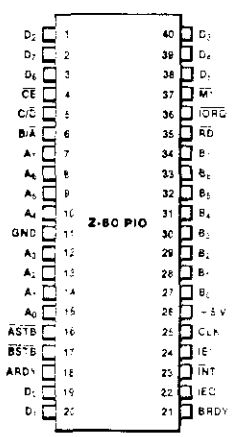


Figure 2. Pin Assignments

General Description (Continued)

The Z-80 PIO interfaces to peripherals via two independent general-purpose I/O ports, designated Port A and Port B. Each port has eight data bits and two handshake signals, Ready and Strobe, which control data transfer. The Ready output indicates to the peripheral that the port is ready for a data transfer. Strobe is an input from the peripheral that indicates when a data transfer has occurred.

Operating Modes. The Z-80 PIO ports can be programmed to operate in four modes: byte output (Mode 0), byte input (Mode 1), byte input/output (Mode 2) and bit input/output (Mode 3).

In Mode 0, either Port A or Port B can be programmed to output data. Both ports have output registers that are individually addressed by the CPU; data can be written to either port at any time. When data is written to a port, an active Ready output indicates to the external device that data is available at the associated port and is ready for transfer to the external device. After the data transfer, the external device responds with an active Strobe input, which generates an interrupt, if enabled.

In Mode 1, either Port A or Port B can be configured in the input mode. Each port has an input register addressed by the CPU. When the CPU reads data from a port, the PIO sets the Ready signal, which is detected by the external device. The external device then places data on the I/O lines and strobes the I/O port, which latches the data into the Port Input Register, resets Ready, and triggers the Interrupt Request, if enabled. The CPU can read the input data at any time, which again sets Ready.

Mode 2 is bidirectional and uses Port A, plus the interrupts and handshake signals from both ports. Port B must be set to Mode 3 and masked off. In operation, Port A is used for both data input and output. Output operation is similar to Mode 0 except that data is allowed out onto the Port A bus only when $\overline{ASTB}$ is Low. For input, operation is similar to Mode 1, except that the data input uses the Port B handshake signals and the Port B interrupt (if enabled).

Both ports can be used in Mode 3. In this mode, the individual bits are defined as either input or output bits. This provides up to eight separate, individually defined bits for each port. During operation, Ready and Strobe are not used. Instead, an interrupt is generated if the condition of one input changes, or if all inputs change. The requirements for generating an interrupt are defined during the programming operation; the active level is specified as either High or Low, and the logic condition is specified as either one input active (OR) or all inputs active (AND). For example, if the port is programmed for active Low inputs and the logic function is AND, then all inputs at the specified port must go Low to generate an interrupt.

Data outputs are controlled by the CPU and can be written or changed at any time.

- Individual bits can be masked off.
- The handshake signals are not used in Mode 3; Ready is held Low, and Strobe is disabled.
- When using the Z-80 PIO interrupts, the Z-80 CPU interrupt mode must be set to Mode 2.

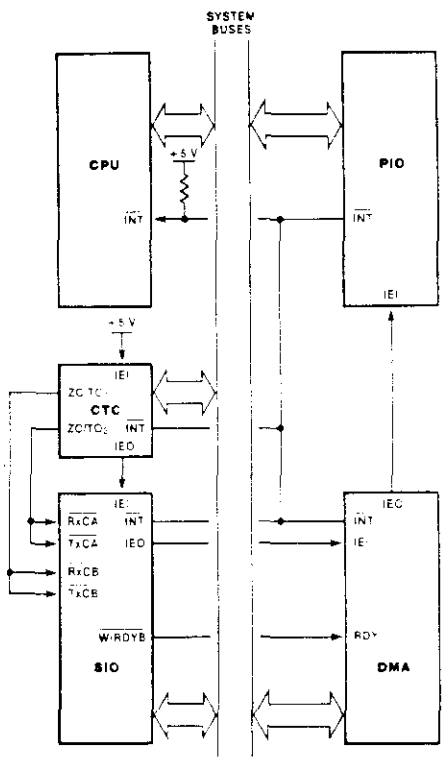


Figure 3. PIO in a Typical Z80 Family Environment

Internal Structure

The internal structure of the Z-80 PIO consists of a Z-80 CPU bus interface, internal control logic, Port A I/O logic, Port B I/O logic, and interrupt control logic (Figure 4). The CPU bus interface logic allows the Z-80 PIO to interface directly to the Z-80 CPU with no other external logic. The internal control logic synchronizes the CPU data bus to the peripheral device interfaces (Port A and Port B). The two I/O ports (A and B) are virtually identical and are used to interface directly to peripheral devices.

Port Logic. Each port contains separate input and output registers, handshake control logic, and the control registers shown in Figure 5. All data transfers between the peripheral unit and the CPU use the data input and output registers. The handshake logic associated with each port controls the data transfers through the input and the output registers. The mode control register (two bits) selects one of the four programmable operating modes.

The control mode (Mode 3) uses the remaining registers. The input/output control register specifies which of the eight data bits in the port are to be outputs and enables these bits; the remaining bits are inputs. The mask register and the mask control register control Mode 3 interrupt conditions. The mask register specifies which of the bits in the port are active and which are masked or inactive.

The mask control register specifies two conditions: first, whether the active state of the input bits is High or Low, and second, whether an interrupt is generated when any *one* unmasked input bit is active (OR condition) or if the interrupt is generated when *all* unmasked input bits are active (AND condition).

Interrupt Control Logic. The interrupt control logic section handles all CPU interrupt protocol for nested-priority interrupt structures. Any device's physical location in a daisy-chain configuration determines its priority. Two lines (IEI and IEO) are provided in each PIO to form this daisy chain. The device closest to the CPU has the highest priority. Within a PIO, Port A interrupts have higher priority than those of Port B. In the byte input, byte output, or bidirectional modes, an interrupt can be generated whenever the peripheral requests a new byte transfer. In the bit control mode, an interrupt can be generated when the peripheral status matches a programmed value. The PIO provides for complete control of nested interrupts. That is, lower priority devices may not interrupt higher priority devices that have not had their interrupt service routines completed by the CPU. Higher priority devices may interrupt the servicing of lower priority devices.

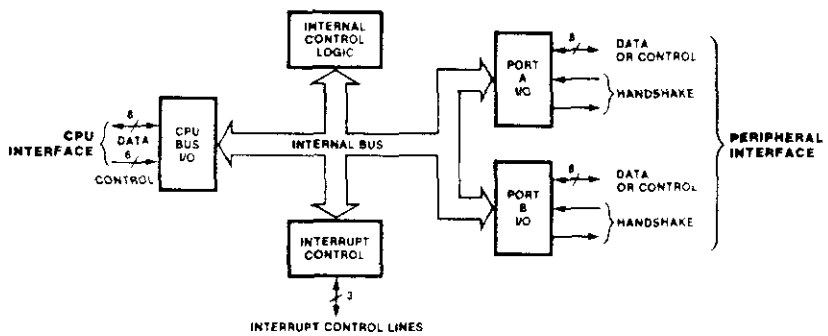


Figure 4. Block Diagram

Internal Structure (Continued)

If the CPU (in interrupt Mode 2) accepts an interrupt, the interrupting device must provide an 8-bit interrupt vector for the CPU. This vector forms a pointer to a location in memory where the address of the interrupt service routine is located. The 8-bit vector from the interrupting device forms the least significant *eight bits of the indirect pointer while the* I Register in the CPU provides the most significant eight bits of the pointer. Each port (A and B) has an independent interrupt vector. The least significant bit of the vector is automatically set to 0 within the PIO because the pointer must point to two adjacent memory locations for a complete 16-bit address.

Unlike the other Z-80 peripherals, the PIO does not enable interrupts immediately after programming. It waits until $\overline{M1}$ goes Low (e.g., during an opcode fetch). This condition is unimportant in the Z-80 environment but might not be if another type of CPU is used.

The PIO decodes the RETI (Return From Interrupt) instruction directly from the CPU data bus so that each PIO in the system knows at all times whether it is being serviced by the CPU interrupt service routine. No other communication with the CPU is required.

CPU Bus I/O Logic. The CPU bus interface logic interfaces the Z-80 PIO directly to the Z-80 CPU, so no external logic is necessary. For large systems, however, address decoders and/or buffers may be necessary.

Internal Control Logic. This logic receives the control words for each port during programming and, in turn, controls the operating functions of the Z-80 PIO. The control logic synchronizes the port operations, controls the port mode, port addressing, selects the read/write function, and issues appropriate commands to the ports and the interrupt logic. The Z-80 PIO does not receive a write input from the CPU; instead, the $\overline{RD}$, $\overline{CE}$, C/$\overline{D}$ and $\overline{IORQ}$ signals generate the write input internally.

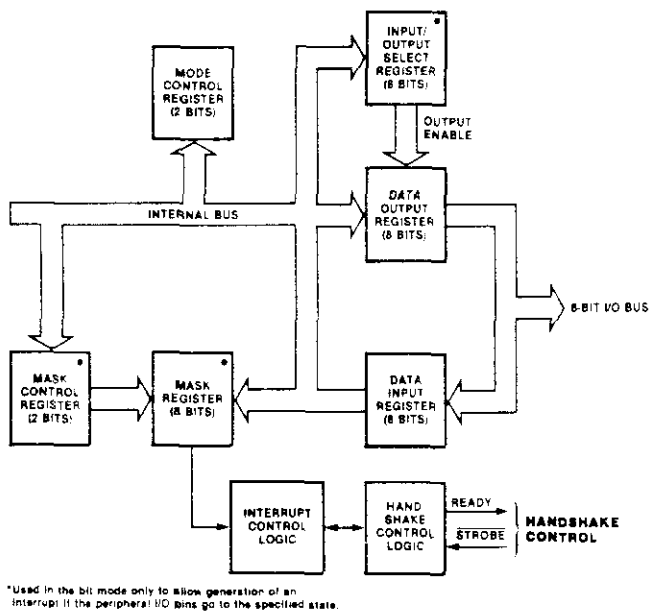


Figure 5. Typical Port I/O Block Diagram

Programming

Mode 0, 1, or 2. *(Byte Input, Output, or Bidirectional).* Programming a port for Mode 0, 1, or 2 requires two words per port. These words are:

A Mode Control Word. Selects the port operating mode (Figure 6). This word may be written any time.

An Interrupt Vector. The Z-80 PIO is designed for use with the Z-80 CPU in interrupt Mode 2 (Figure 7). When interrupts are enabled, the PIO must provide an interrupt vector.

Mode 3. *(Bit Input/Output).* Programming a port for Mode 3 operation requires a control word, a vector (if interrupts are enabled), and three additional words, described as follows:

I/O Register Control. When Mode 3 is selected, the mode control word must be followed by another control word that sets the I/O control register, which in turn defines which port lines are inputs and which are outputs (Figure 8).

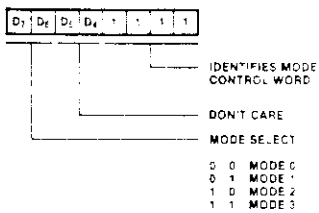


Figure 6. Mode Control Word

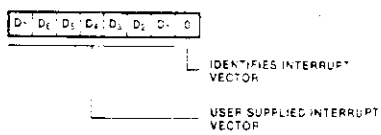


Figure 7. Interrupt Vector Word

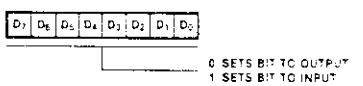


Figure 8. I/O Register Control Word

Interrupt Control Word. In Mode 3, handshake is not used. Interrupts are generated as a logic function of the input signal levels. The interrupt control word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered), and OR (if any one of the input bits changes to the active level, an interrupt is triggered). Bit D_6 sets the logic function, as shown in Figure 9. The active level of the input bits can be set either High or Low. The active level is controlled by Bit D_5.

Mask Control Word. This word sets the mask control register, allowing any unused bits to be masked off. If any bits are to be masked, then D_4 must be set. When D_4 is set, the next word written to the port must be a mask control word (Figure 10).

Interrupt Disable. There is one other control word which can be used to enable or disable a port interrupt. It can be used without changing the rest of the interrupt control word (Figure 11).

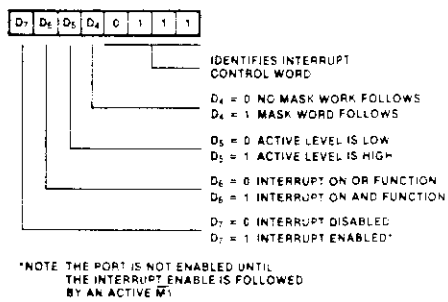


Figure 9. Interrupt Control Word

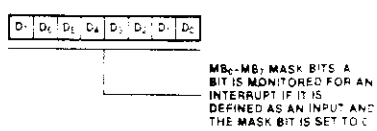


Figure 10. Mask Control Word

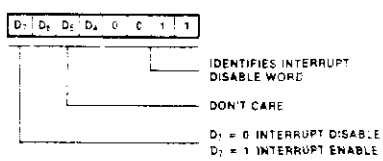


Figure 11. Interrupt Disable Word

Pin Description

A_0-A_7. *Port A Bus* (bidirectional, 3-state). This 8-bit bus transfers data, status, or control information between Port A of the PIO and a peripheral device. A_0 is the least significant bit of the Port A data bus.

ARDY. *Register A Ready* (output, active High). The meaning of this signal depends on the mode of operation selected for Port A as follows:

Output Mode. This signal goes active to indicate that the Port A output register has been loaded and the peripheral data bus is stable and ready for transfer to the peripheral device.

Input Mode. This signal is active when the Port A input register is empty and ready to accept data from the peripheral device.

Bidirectional Mode. This signal is active when data is available in the Port A output register for transfer to the peripheral device. *In this mode, data is not placed on the* Port A data bus, unless $\overline{ASTB}$ is active.

Control Mode. This signal is disabled and forced to a Low state.

$\overline{ASTB}$. *Port A Strobe Pulse From Peripheral Device* (input, active Low). The meaning of this signal depends on the mode of operation selected for Port A as follows:

Output Mode. The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the PIO.

Input Mode. The strobe is issued by the peripheral to load data from the peripheral into the Port A input register. Data is loaded into the PIO when this signal is active.

Bidirectional Mode. When this signal is active, data from the Port A output register is gated onto the Port A bidirectional data bus. The positive edge of the strobe acknowledges the receipt of the data.

Control Mode. The strobe is inhibited internally.

B_0-B_7. *Port B Bus* (bidirectional, 3-state). This 8-bit bus transfers data, status, or control information between Port B and a peripheral device. The Port B data bus can supply 1.5 mA at 1.5 V to drive Darlington transistors. B_0 is the least significant bit of the bus.

B/$\overline{A}$. *Port B Or A Select* (input, High = B). This pin defines which port is accessed during a data transfer between the CPU and the PIO. A Low on this pin selects Port A; a High selects Port B. Often address bit A_0 from the CPU is used for this selection function.

BRDY. *Register B Ready* (output, active High). This signal is similar to ARDY, except that in the Port A bidirectional mode this signal is High when the Port A input register is empty and ready to accept data from the peripheral device.

$\overline{BSTB}$. *Port B Strobe Pulse From Peripheral Device* (input, active Low). This signal is similar to $\overline{ASTB}$, except that in the Port A bidirectional mode this signal strobes data from the peripheral device into the Port A input register.

C/$\overline{D}$. *Control Or Data Select* (input, High = C). This pin defines the type of data transfer to be performed between the CPU and the PIO. A High on this pin during a CPU write to the PIO causes the Z-80 data bus to be interpreted as a *command* for the port selected by the B/$\overline{A}$ Select line. A Low on this pin means that the Z-80 data bus is being used to transfer data between the CPU and the PIO. Often address bit A_1 from the CPU is used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low on this pin enables the PIO to accept command or data inputs from the CPU during a write cycle or to transmit data to the CPU during a read cycle. This signal is generally decoded from four I/O port numbers for Ports A and B, data, and control.

CLK. *System Clock* (input). The Z-80 PIO uses the standard single-phase Z-80 system clock.

D_0-D_7. *Z-80 CPU Data Bus* (bidirectional, 3-state). This bus is used to transfer all data and commands between the Z-80 CPU and the Z-80 PIO. D_0 is the least significant bit.

IEI. *Interrupt Enable In* (input, active High). This signal is used to form a priority-interrupt daisy chain when more than one interrupt-driven device is being used. A High level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). The IEO signal is the other signal required to form a daisy chain priority scheme. It is High only if IEI is High and the CPU is not servicing an interrupt from this PIO. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When $\overline{INT}$ is active the Z-80 PIO is requesting an interrupt from the Z-80 CPU.

$\overline{IORQ}$. *Input/Output Request* (input from Z-80 CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{RD}$ to transfer commands and data between the Z-80 CPU and the Z-80 PIO. When $\overline{CE}$, $\overline{RD}$, and $\overline{IORQ}$ are active, the port addressed by B/$\overline{A}$ transfers data to the CPU (a read operation). Conversely, when $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is not, the port addressed by B/$\overline{A}$ is written into from the CPU with either data or control information, as specified by C/$\overline{D}$. Also, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt; the interrupting port automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

Pin Description (Continued)

$\overline{M1}$. *Machine Cycle* (input from CPU, active Low). This signal is used as a sync pulse to control several internal PIO operations. When both the $\overline{M1}$ and $\overline{RD}$ signals are active, the Z-80 CPU is fetching an instruction from memory. Conversely, when both $\overline{M1}$ and $\overline{IORQ}$ are active, the CPU is acknowledging an interrupt. In addition, $\overline{M1}$ has two other functions within the Z-80 PIO: it synchronizes the PIO interrupt logic; when $\overline{M1}$ occurs without an active $\overline{RD}$ or $\overline{IORQ}$ signal, the PIO is reset.

$\overline{RD}$. *Read Cycle Status* (input from Z-80 CPU, active Low). If $\overline{RD}$ is active, or an I/O operation is in progress, $\overline{RD}$ is used with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{IORQ}$ to transfer data from the Z-80 PIO to the Z-80 CPU.

Timing

The following timing diagrams show typical timing in a Z-80 CPU environment. For more precise specifications refer to the composite ac timing diagram.

Write Cycle. Figure 12 illustrates the timing for programming the Z-80 PIO or for writing data to one of its ports. No Wait states are allowed for writing to the PIO other than the automatically inserted T_{WA}. The PIO does not receive a specific write signal; it internally generates its own from the lack of an active $\overline{RD}$ signal.

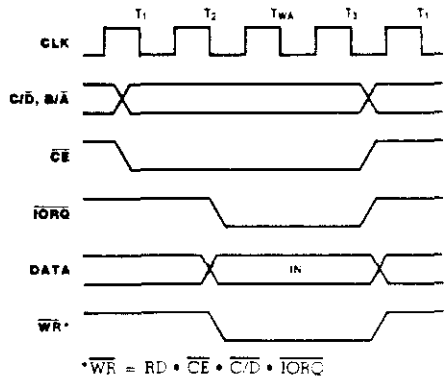


Figure 12. Write Cycle Timing

Read Cycle. Figure 13 illustrates the timing for reading the data input from an external device to one of the Z-80 PIO ports. No Wait states are allowed for reading the PIO other than the automatically inserted T_{WA}.

Output Mode (Mode 0). An output cycle (Figure 14) is always started by the execution of an output instruction by the CPU. The $\overline{WR}$* pulse from the CPU latches the data from the CPU data bus into the selected port's output register. The $\overline{WR}$* pulse sets the Ready flag after a Low-going edge of CLK, indicating data is available. Ready stays active until the positive edge of the strobe line is received, indicating that data was taken by the peripheral. The positive edge of the strobe pulse generates an $\overline{INT}$ if the interrupt enable flip-flop has been set and if this device has the highest priority.

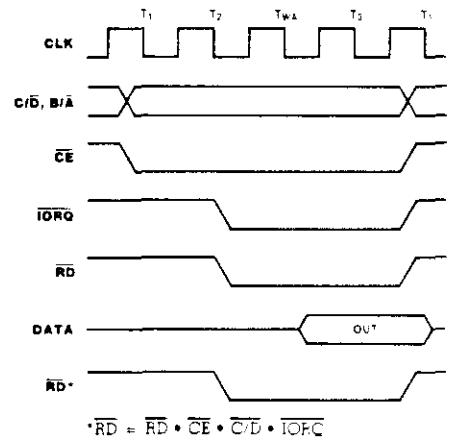


Figure 13. Read Cycle Timing

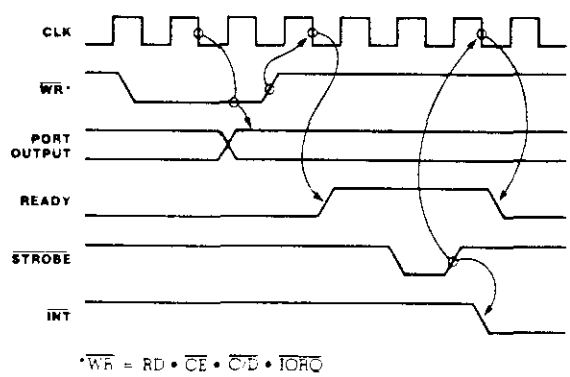


Figure 14. Mode 0 Output Timing

Timing (Continued)

Input Mode (Mode 1). When $\overline{\text{STROBE}}$ goes Low, data is loaded into the selected port input register (Figure 15). The next rising edge of strobe activates $\overline{\text{INT}}$, if Interrupt Enable is set and this is the highest-priority requesting device. The following falling edge of CLK resets Ready to an inactive state, indicating that the input register is full and cannot accept any more data until the CPU completes a read. When a read is complete, the positive edge of $\overline{\text{RD}}$ sets Ready at the next Low-going transition of CLK. At this time new data can be loaded into the PIO.

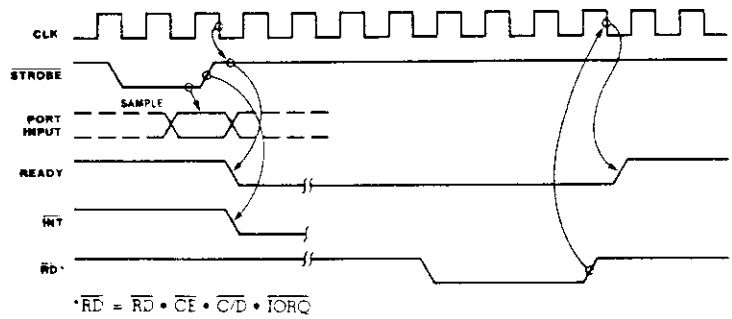


Figure 15. Mode 1 Input Timing

Bidirectional Mode (Mode 2). This is a combination of Modes 0 and 1 using all four handshake lines and the eight Port A I/O lines (Figure 16). Port B must be set to the bit mode and its inputs must be masked. The Port A handshake lines are used for output control and the Port B lines are used for input control. If interrupts occur, Port A's vector will be used during port output and Port B's will be used during port input. Data is allowed out onto the Port A bus only when $\overline{\text{ASTB}}$ is Low. The rising edge of this strobe can be used to latch the data into the peripheral.

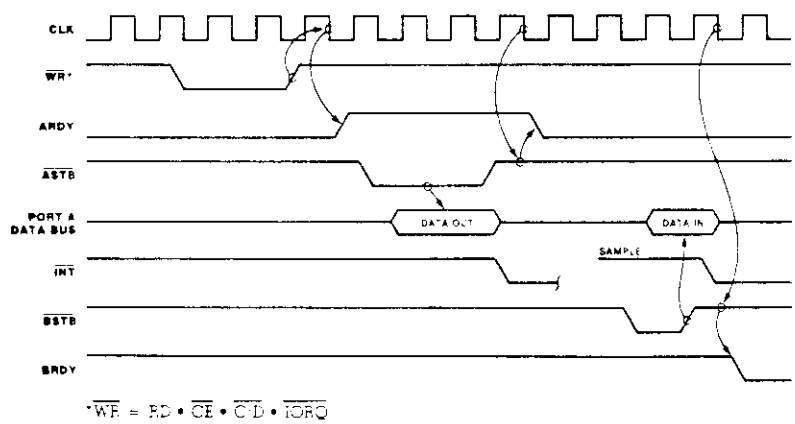


Figure 16. Mode 2 Bidirectional Timing

Timing (Continued)

Bit Mode (Mode 3). The bit mode does not utilize the handshake signals, and a normal port write or port read can be executed at any time. When writing, the data is latched into the output registers with the same timing as the output mode (Figure 17).

When reading the PIO, the data returned to the CPU is composed of output register data from those port data lines assigned as outputs and input register data from those port data lines assigned as inputs. The input register contains data that was present immediately prior to the falling edge of $\overline{RD}$. An interrupt is generated if interrupts from the port are enabled and the data on the port data lines satisfy the logical equation defined by the 8-bit mask and 2-bit mask control registers. However, if Port A is programmed in bidirectional mode, Port B does not issue an interrupt in bit mode and must therefore be polled.

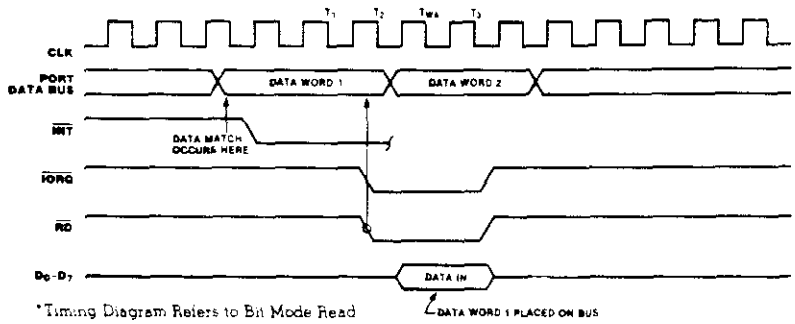


Figure 17. Mode 3 Bit Mode Timing

Interrupt Acknowledge Timing. During $\overline{M1}$ time, peripheral controllers are inhibited from changing their interrupt enable status, permitting the Interrupt Enable signal to ripple through the daisy chain. The peripheral with IEI High and IEO Low during $\overline{INTACK}$ places a preprogrammed 8-bit interrupt vector on the data bus at this time (Figure 18). IEO is held Low until a Return From Interrupt (RETI) instruction is executed by the CPU while IEI is High. The 2-byte RETI instruction is decoded internally by the PIO for this purpose.

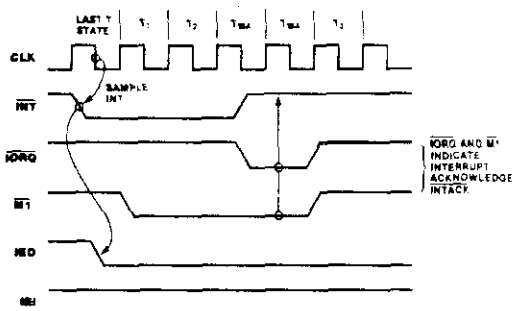


Figure 18. Interrupt Acknowledge Timing

Return From Interrupt Cycle. If a Z-80 peripheral has no interrupt pending and is not under service, then its IEO = IEI. If it has an interrupt under service (i.e., it has already interrupted and received an interrupt acknowledge) then its IEO is always Low, inhibiting lower priority devices from interrupting. If it has an interrupt pending which has not yet been acknowledged, IEO is Low unless an "ED" is decoded as the first byte of a 2-byte opcode (Figure 19). In this case, IEO goes High until the next opcode byte is decoded, whereupon it goes Low again. If the second byte of the opcode was a "4D," then the opcode was an RETI instruction.

After an "ED" opcode is decoded, only the peripheral device which has interrupted and is currently under service has its IEI High and its IEO Low. This device is the highest-priority device in the daisy chain that has received an interrupt acknowledge. All other peripherals have IEI = IEO. If the next opcode byte decoded is "4D," this peripheral device resets its "interrupt under service" condition.

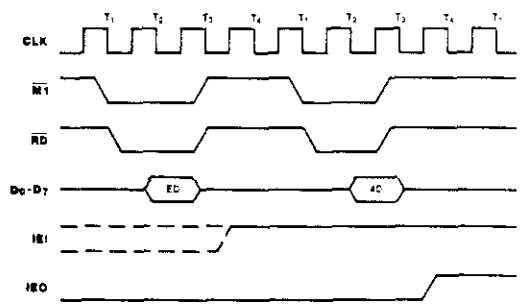
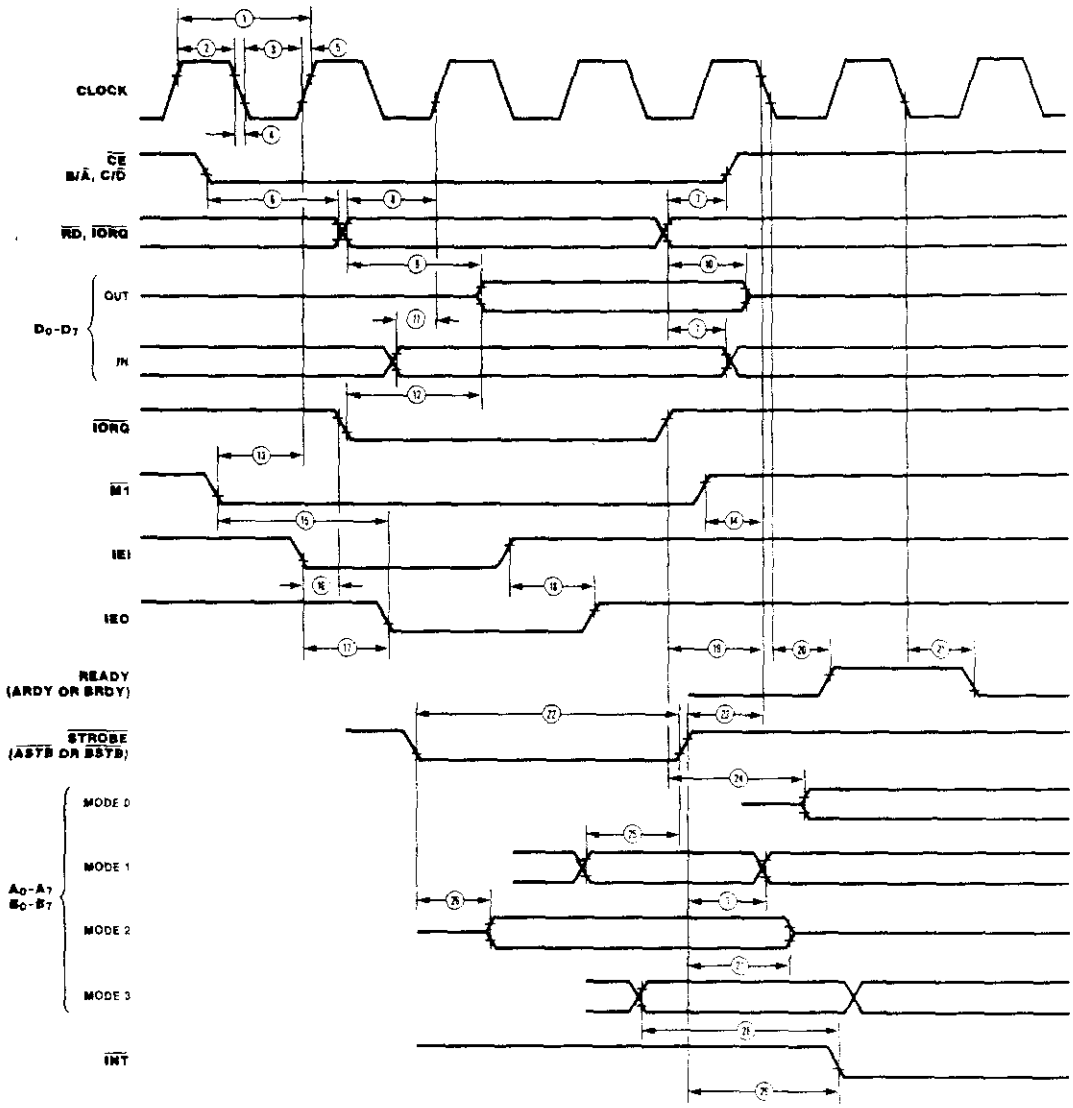


Figure 19. Return From Interrupt

AC Characteristics



Number	Symbol	Parameter	Z-80 PIO Min (ns)	Z-80 PIO Max (ns)	Z-80A PIO Min (ns)	Z-80A PIO Max (ns)	Z-80B PIO[9] Min (ns)	Z-80B PIO[9] Max (ns)	Comment
1	TcC	Clock Cycle Time	400	[1]	250	[1]	165	[1]	
2	TwCh	Clock Width (High)	170	2000	105	2000	65	2000	
3	TwCl	Clock Width (Low)	170	2000	105	2000	65	2000	
4	TfC	Clock Fall Time		30		30		20	
5	TrC	Clock Rise Time		30		30		20	
6	TsCS(RI)	$\overline{CE}$, B/$\overline{A}$, C/$\overline{D}$ to $\overline{RD}$, $\overline{IORQ}$ ↓ Setup Time	50		50		50		[6]
7	Th	Any Hold Times for Specified Setup Time	0		0		0	0	
8	TsRI(C)	$\overline{RD}$, $\overline{IORQ}$ to Clock ↑ Setup Time	115		115		70		
9	TdRI(DO)	$\overline{RD}$, $\overline{IORQ}$ ↓ to Data Out Delay		430		380		300	[2]
10	TdRI(DOs)	$\overline{RD}$, $\overline{IORQ}$ ↑ to Data Out Float Delay		160		110		70	
11	TsDI(C)	Data In to Clock ↑ Setup Time	50		50		40		CL = 50 pF
12	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTACK Cycle)		340		160		120	[3]
13	TsM1(Cr)	$\overline{M1}$ ↓ to Clock ↑ Setup Time	210		90		70		
14	TsM1(Cf)	$\overline{M1}$ ↓ to Clock ↓ Setup Time (M1 Cycle)	0		0		0		[8]
15	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (Interrupt Immediately Preceding $\overline{M1}$ ↓)		300		190		100	[5, 7]
16	TsIEI(IO)	IEI to $\overline{IORQ}$ ↓ Setup Time (INTACK Cycle)	140		140		100		[7]
17	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		190		130		120	[5], CL = 50 pF
18	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED Decode)		210		160		160	[5]
19	TcIO(C)	$\overline{IORQ}$ ↑ to Clock ↓ Setup Time (To Activate READY on Next Clock Cycle)	220		200		170		
20	TdC(RDYr)	Clock ↓ to READY ↑ Delay		200		190		170	[5], CL = 50 pF
21	TdC(RDYf)	Clock ↓ to READY ↓ Delay		150		140		120	[5]
22	TwSTB	$\overline{STROBE}$ Pulse Width	150		150		120		[4]
23	TsSTB(C)	$\overline{STROBE}$ ↑ to Clock ↓ Setup Time (To Activate READY on Next Clock Cycle)	220		220		150		[5]
24	TdIO(PD)	$\overline{IORQ}$ ↑ to PORT DATA Stable Delay (Mode 0)		200		180		160	[5]
25	TsPD(STB)	PORT DATA to $\overline{STROBE}$ ↑ Setup Time (Mode 1)	260		230		190		
26	TdSTB(PD)	$\overline{STROBE}$ ↓ to PORT DATA Stable (Mode 2)		230		210		180	[5]
27	TdSTB(PDr)	$\overline{STROBE}$ ↑ to PORT DATA Float Delay (Mode 2)		200		180		160	CL = 50 pF
28	TdPD(INT)	PORT DATA Match to $\overline{INT}$ ↓ Delay (Mode 3)		540		490		430	
29	TdSTB(INT)	$\overline{STROBE}$ ↑ to $\overline{INT}$ ↓ Delay		490		440		350	

NOTES:
[1] TcC = TwCh + TwCl + TrC + TfC
[2] Increase TdRI(DO) by 10 ns for each 50 pF increase in load up to 200 pF max.
[3] Increase TdIO(DOI) by 10 ns for each 50 pF increase in loading up to 200 pF max.
[4] For Mode 2: TwSTB > TsPD(STB)
[5] Increase these values by 2 ns for each 10 pF increase in loading up to 100 pF max.
[6] TsCS(RI) may be reduced. However, the time subtracted from TsCS(RI) will be added to TdRI(DO).
[7] 2.5 TcC > (N-2)TdIEI(IEOr) + TdM1(IEO) + TsIEI(IO) + TTL Buffer Delay, if any.
[8] $\overline{M1}$ must be active for a minimum of two clock cycles to reset the PIO.
[9] Z80B PIO numbers are preliminary and subject to change.

Absolute Maximum Ratings

Voltages on all inputs and outputs with respect to GND . . . . . -0.3 V to +7.0 V

Operating Ambient Temperature . . . . . As Specified in Ordering Information

Storage Temperature . . . . . -65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

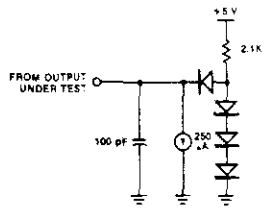
Test Conditions

The characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND (0 V). Positive current flows into the referenced pin. Available operating temperature ranges are:

- S* = 0°C to +70°C, $+4.75\ V \le V_{CC} \le +5.25\ V$
- E* = −40°C to +85°C, $+4.75\ V \le V_{CC} \le +5.25\ V$
- M* = −55°C to +125°C, $+4.5\ V \le V_{CC} \le +5.5\ V$

*See Ordering Information section for package temperature range and product number.

All ac parameters assume a load capacitance of 100 pF max.



DC Characteristics

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	+0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-0.6	V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	-0.3	+0.8	V	
V_{IH}	Input High Voltage	+2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	+2.4		V	I_{OH} = -250 µA
I_{LI}	Input Leakage Current		±10.0	µA	V_{IN} = 0 to V_{CC}
I_{LO}	3-State Output Leakage Current in Float		±10.0	µA	V_{OUT} = 0.4 V to V_{CC}
I_{CC}	Power Supply Current		100.0	mA	V_{CC} = 1.5 V
I_{OHD}	Darlington Drive Current	-1.5		mA	R_{EXT} = 390 Ω

Over specified temperature and voltage range.

Capacitance

Symbol	Parameter	Min	Max	Unit	Test Condition
C	Clock Capacitance		10	pF	Unmeasured pins returned to ground
C_{IN}	Input Capacitance		5	pF	
C_{OUT}	Output Capacitance		10	pF	

Over specified temperature range; f = 1MHz.

Ordering Information

Product Number	Package/ Temp	Speed	Description	Product Number	Package/ Temp	Speed	Description
Z8420	CE	2.5 MHz	Z80 PIO (40-pin)	Z8420A	CMB	4.0 MHz	Z80A PIO (40-pin)
Z8420	CM	2.5 MHz	Same as above	Z8420A	CS	4.0 MHz	Same as above
Z8420	CMB	2.5 MHz	Same as above	Z8420A	DE	4.0 MHz	Same as above
Z8420	CS	2.5 MHz	Same as above	Z8420A	DS	4.0 MHz	Same as above
Z8420	DE	2.5 MHz	Same as above	Z8420A	PE	4.0 MHz	Same as above
Z8420	DS	2.5 MHz	Same as above	Z8420A	PS	4.0 MHz	Same as above
Z8420	PE	4.0 MHz	Same as above	Z8420B	CS	6.0 MHz	Same as above
Z8420	PS	4.0 MHz	Same as above	Z8420B	DS	6.0 MHz	Same as above
Z8420A	CE	4.0 MHz	Z80A PIO (40-pin)	Z8420B	PS	6.0 MHz	Same as above
Z8420A	CM	4.0 MHz	Same as above				

*NOTES: C = Ceramic, D = Cerdip, P = Plastic, E = -40°C to +85°C, M = -55°C to +125°C, MB = 55°C to +125°C with MIL-STD-883 Class B processing, S = 0°C to +70°C.

Z8440
Z80® SIO Serial Input/Output Controller

Zilog

Product Specification

September 1983

Features

- Two independent full-duplex channels, with separate control and status lines for modems or other devices.
- Data rates of 0 to 500K bits/second in the x1 clock mode with a 2.5 MHz clock (Z-80 SIO), or 0 to 800K bits/second with a 4.0 MHz clock (Z-80A SIO).
- Asynchronous protocols: everything necessary for complete messages in 5, 6, 7 or 8 bits/character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.
- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/checking, sync character and zero insertion/deletion, abort generation/detection and flag insertion.
- Receiver data registers quadruply buffered, transmitter registers doubly buffered.
- Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

General Description

The Z-80 SIO Serial Input/Output Controller is a dual-channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications.

The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Moreover, it does this on two fully-independent channels, with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU or DMA

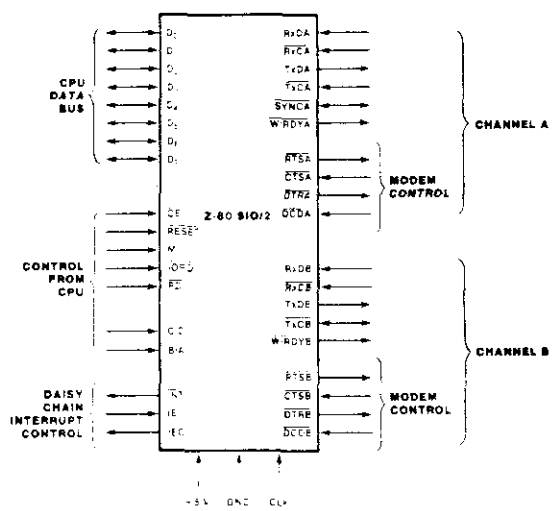


Figure 1. Z-80 SIO/2 Pin Functions

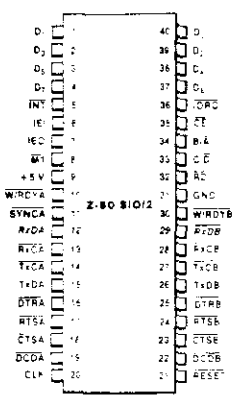


Figure 2. Z-80 SIO/2 Pin Assignments

General Description (Continued)

control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast (or slow) peripheral devices. While designed primarily as a member of the Z-80 family, its versatility makes it well suited to many other CPUs.

The Z-80 SIO is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic or ceramic DIP. It uses a single +5 V power supply and the standard Z-80 family single-phase clock.

Pin Description

Figures 1 through 6 illustrate the three pin configurations (bonding options) available in the SIO. The constraints of a 40-pin package make it impossible to bring out the Receive Clock ($\overline{RxC}$), Transmit Clock ($\overline{TxC}$), Data Terminal Ready ($\overline{DTR}$) and Sync ($\overline{SYNC}$) signals for both channels. Therefore, either Channel B lacks a signal or two signals are bonded together in the three bonding options offered:

- Z-80 SIO/2 lacks $\overline{SYNCB}$
- Z-80 SIO/1 lacks $\overline{DTRB}$
- Z-80 SIO/0 has all four signals, but $\overline{TxCB}$ and $\overline{RxCB}$ are bonded together

The first bonding option above (SIO/2) is the preferred version for most applications. The pin descriptions are as follows:

B/$\overline{A}$. *Channel A Or B Select* (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit A_0 from the CPU is often used for the selection function.

C/$\overline{D}$. *Control Or Data Select* (input, High selects Control). This input defines the type of information transfer performed between the CPU and the SIO. A High at this input during a CPU write to the SIO causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A Low at C/$\overline{D}$ means that the information on the data bus is data. Address bit A_1 is often used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low level at this input enables the SIO to accept command or data input from the CPU during a write cycle or to transmit data to the CPU during a read cycle.

CLK. *System Clock* (input). The SIO uses the standard Z-80 System Clock to synchronize internal signals. This is a single-phase clock.

$\overline{CTSA}$, $\overline{CTSB}$. *Clear To Send* (inputs, active Low). When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these inputs and interrupts the CPU on both logic level transitions. The Schmitt-trigger buffering does not guarantee a specified noise-level margin.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). The system data bus transfers data and commands between the CPU and the Z-80 SIO. D_0 is the least significant bit.

$\overline{DCDA}$, $\overline{DCDB}$. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if the SIO is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these pins and interrupts the CPU on both logic level transitions. Schmitt-trigger buffer-

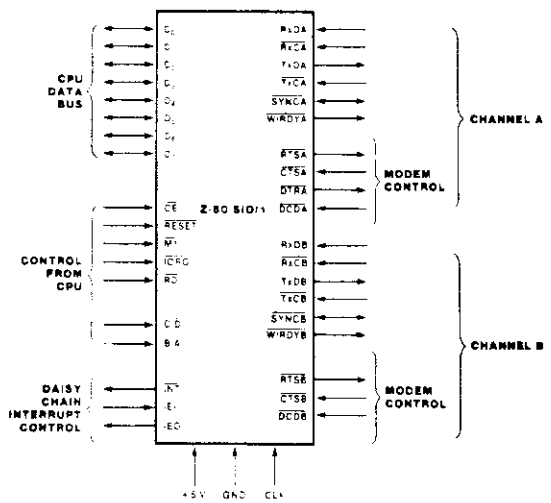


Figure 3. Z-80 SIO/1 Pin Functions

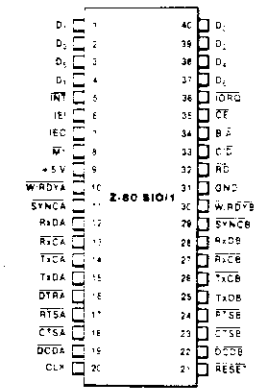


Figure 4. Z-80 SIO/1 Pin Assignments

Pin Description (Continued)

ing does not guarantee a specific noise-level margin.

$\overline{DTRA}$, $\overline{DTRB}$. *Data Terminal Ready* (outputs, active Low). These outputs follow the state programmed into Z-80 SIO. They can also be programmed as general-purpose outputs.

In the Z-80 SIO/1 bonding option, $\overline{DTRB}$ is omitted.

IEI. *Interrupt Enable In* (input, active High). This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this SIO. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When the SIO is requesting an interrupt, it pulls $\overline{INT}$ Low.

$\overline{IORQ}$. *Input/Output Request* (input from CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$ and $\overline{RD}$ to transfer commands and data between the CPU and the SIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are all active, the channel selected by B/$\overline{A}$ transfers data to the CPU (a read operation). When $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is inactive, the channel selected by B/$\overline{A}$ is written to by the CPU with either data or control information as specified by C/$\overline{D}$. If $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt and the SIO automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{M1}$. *Machine Cycle* (input from Z-80 CPU, active Low). When $\overline{M1}$ is active and $\overline{RD}$ is also active, the Z-80 CPU is fetching an instruction from memory; when $\overline{M1}$ is active while $\overline{IORQ}$ is active, the SIO accepts $\overline{M1}$ and $\overline{IORQ}$ as an interrupt acknowledge if the SIO is the highest priority device that has interrupted the Z-80 CPU.

$\overline{RxCA}$, $\overline{RxCB}$. *Receiver Clocks* (inputs). Receive data is sampled on the rising edge of $\overline{RxC}$. The Receive Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. These clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation. Both inputs are Schmitt-trigger buffered (no noise level margin is specified).

In the Z-80 SIO/0 bonding option, $\overline{RxCB}$ is bonded together with $\overline{TxCB}$.

$\overline{RD}$. *Read Cycle Status* (input from CPU, active Low). If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with B/$\overline{A}$, $\overline{CE}$ and $\overline{IORQ}$ to transfer data from the SIO to the CPU.

RxDA, RxDB. *Receive Data* (inputs, active High). Serial data at TTL levels.

$\overline{RESET}$. *Reset* (input, active Low). A Low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls High and disables all interrupts. The control registers must be

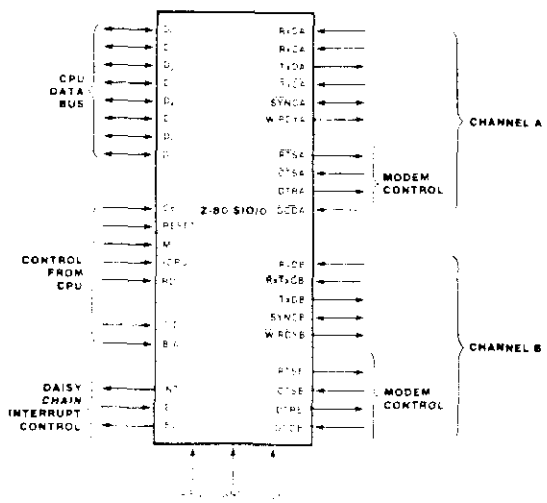


Figure 5. Z-80 SIO/0 Pin Functions

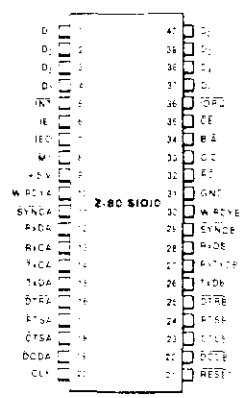


Figure 6. Z-80 SIO/0 Pin Assignments

Pin Description (Continued)

rewritten after the SIO is reset and before data is transmitted or received.

$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$. *Request To Send* (outputs, active Low). When the RTS bit in Write Register 5 (Figure 14) is set, the $\overline{\text{RTS}}$ output goes Low. When the RTS bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{\text{RTS}}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$. *Synchronization* (inputs/outputs, active Low). These pins can act either as inputs or outputs. In the asynchronous receive mode, they are inputs similar to $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0 (Figure 13), but have no other function. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{\text{SYNC}}$ must be driven Low on the second rising edge of $\overline{\text{RxC}}$ after that rising edge of $\overline{\text{RxC}}$ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{\text{SYNC}}$ input. Once $\overline{\text{SYNC}}$ is forced Low, it should be kept Low until the CPU informs the external synchronization detect logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{\text{RxC}}$ that immediately precedes the falling edge of $\overline{\text{SYNC}}$ in the External Sync mode.

In the internal synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock ($\overline{\text{RxC}}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.

In the Z-80 SIO/2 bonding option, $\overline{\text{SYNCB}}$ is omitted.

$\overline{\text{TxCA}}$, $\overline{\text{TxCB}}$. *Transmitter Clocks* (inputs). In asynchronous modes, the Transmitter Clocks may be 1, 16, 32 or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise level margin is specified). Transmitter Clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation.

In the Z-80 SIO/0 bonding option, $\overline{\text{TxCB}}$ is bonded together with $\overline{\text{RxCB}}$.

TxDA, TxDB. *Transmit Data* (outputs, active High). Serial data at TTL levels. TxD changes from the falling edge of $\overline{\text{TxC}}$.

$\overline{\text{W/RDYA}}$, $\overline{\text{W/RDYB}}$. *Wait/Ready A, Wait Ready B* (outputs, open drain when programmed for Wait function, driven High and Low when programmed for Ready function). These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the SIO data rate. The reset state is open drain.

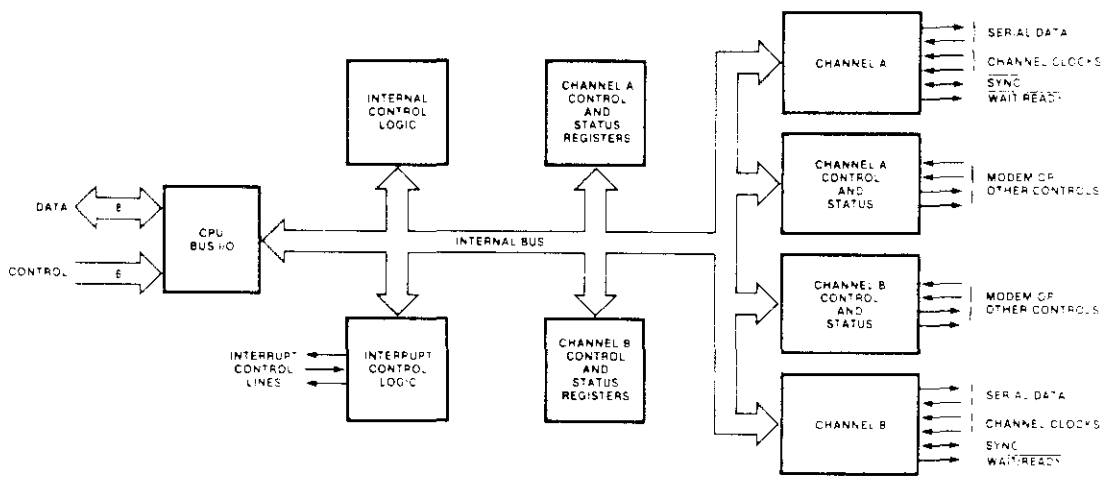


Figure 7. Block Diagram

Functional Description

The functional capabilities of the Z-80 SIO can be described from two different points of view: as a data communications device, it transmits and receives serial data in a wide variety of data-communication protocols; as a Z-80 family peripheral, it interacts with the Z-80 CPU and other peripheral circuits, sharing the data, address and control buses, as well as being a part of the Z-80 interrupt structure. As a peripheral to other microprocessors, the SIO offers valuable features such as non-vectored interrupts, polling and simple handshake capability.

Figure 8 illustrates the conventional devices that the SIO replaces.

The first part of the following discussion covers SIO data-communication capabilities; the second part describes interactions between the CPU and the SIO.

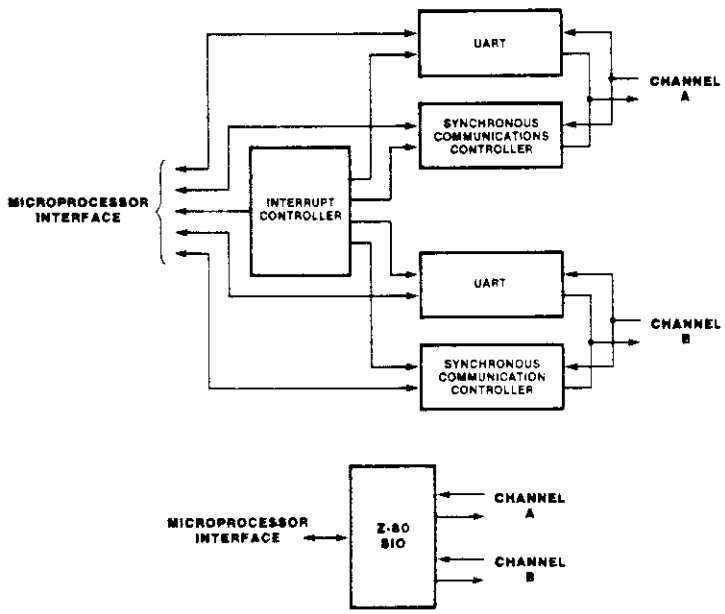


Figure 8. Conventional Devices Replaced by the Z-80 SIO

Data Communication Capabilities

The SIO provides two independent full-duplex channels that can be programmed for use in any common asynchronous or synchronous data-communication protocol. Figure 9 illustrates some of these protocols. The following is a short description of them. A more detailed explanation of these modes can be found in the *Z-80 SIO Technical Manual*.

Asynchronous Modes. Transmission and reception can be done independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in Figure 5). If the Low does not persist—as in the case of a transient—the character assembly process is not started.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occurred. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids interpreting a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit is begun.

The SIO does not require symmetric transmit and receive clock signals—a feature that allows it to be used with a Z-80 CTC or many other clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32 or 1/64 of the clock rate supplied to the receive and transmit clock inputs.

In asynchronous modes, the $\overline{\text{SYNC}}$ pin may be programmed as an input that can be used for functions such as monitoring a ring indicator.

Synchronous Modes. The SIO supports both byte-oriented and bit-oriented synchronous communication.

Synchronous byte-oriented protocols can be handled in several modes that allow character synchronization with an 8-bit sync character (Monosync), any 16-bit sync pattern (Bisync) or with an external sync signal. Leading sync

Data Communication Capabilities (Continued)

characters can be removed without interrupting the CPU.

Five-, six- or seven-bit sync characters are detected with 8- or 16-bit patterns in the SIO by overlapping the larger pattern across multiple in-coming sync characters, as shown in Figure 10.

CRC checking for synchronous byte-oriented modes is delayed by one character time so the CPU may disable CRC checking on specific characters. This permits implementation of protocols such as IBM Bisync.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. In all non-SDLC modes, the CRC generator is initialized to 0's; in SDLC modes, it is initialized to 1's. The SIO can be used for interfacing to peripherals such as hard-sectored floppy disk, but it cannot generate or check CRC for IBM-compatible soft-sectored disks. The SIO also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows very high-speed transmissions under DMA control with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 8- or 16-bit sync characters regardless of the programmed character length.

The SIO supports synchronous bit-oriented protocols such as SDLC and HDLC by performing automatic flag sending, zero insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message the SIO automatically transmits the CRC and trailing flag when the transmit buffer becomes empty. If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. One to eight bits per character can be sent, which allows reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically synchronizes on the leading flag of a frame in SDLC or HDLC, and provides a synchronization signal on the $\overline{SYNC}$ pin; an interrupt can also be programmed. The receiver can be programmed to search for frames addressed by a single byte to only a specified user-selected address or to a global broadcast address. In this mode, frames that do not match either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For transmitting data, an interrupt on the first received character or on every character can be selected. The receiver automatically deletes all zeroes inserted by the transmitter during character assembly. It also calculates and automatically checks the CRC to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers.

The SIO can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SIO can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SIO then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received.

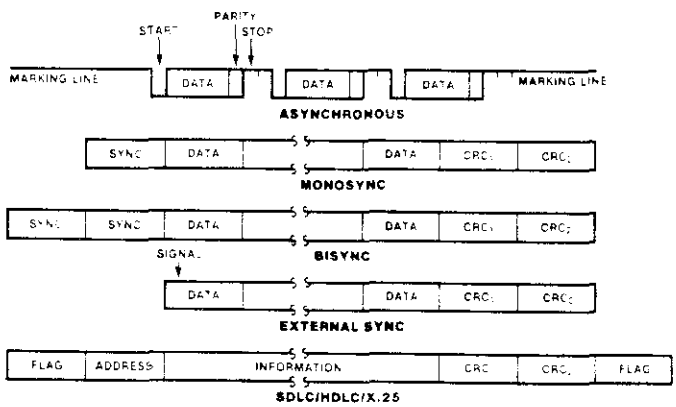


Figure 9. Some Z-80 SIO Protocols

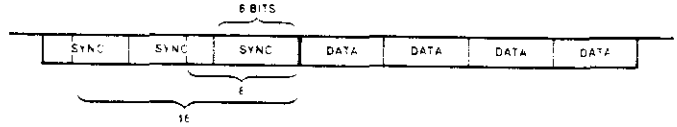


Figure 10. Six-Bit Sync Character Recognition

I/O Interface Capabilities

The SIO offers the choice of polling, interrupt (vectored or non-vectored) and block-transfer modes to transfer data, status and control information to and from the CPU. The block-transfer mode can also be implemented under DMA control.

Polling. Two status registers are updated at appropriate times for each function being performed (for example, CRC error-status valid at the end of a message). When the CPU is operated in a polling fashion, one of the SIO's two status registers is used to indicate whether the SIO has some data or needs some data. Depending on the contents of this register, the CPU will either write data, read data, or just go on. Two bits in the register indicate that a data transfer is needed. In addition, error and other conditions are indicated. The second status register (special receive conditions) does not have to be read in a polling sequence, until a character has been received. All interrupt modes are disabled when operating the device in a polled environment.

Interrupts. The SIO has an elaborate interrupt scheme to provide fast interrupt service in real-time applications. A control register and a status register in Channel B contain the interrupt vector. When programmed to do so, the SIO can modify three bits of the interrupt vector in the status register so that it points directly to one of eight interrupt service routines in memory, thereby servicing conditions in both channels and eliminating most of the needs for a status-analysis routine.

Transmit interrupts, receive interrupts and external/status interrupts are the main sources of interrupts. Each interrupt source is enabled under program control, with Channel A having a higher priority than Channel B, and with receive, transmit and external/status interrupts prioritized in that order within each channel. When the transmit interrupt is enabled, the CPU is interrupted by the transmit buffer becoming empty. (This implies that the transmitter must have had a data character written into it so it can become empty.) The receiver can interrupt the CPU in one of two ways:

- Interrupt on first received character
- Interrupt on all received characters

Interrupt-on-first-received-character is typically used with the block-transfer mode. Interrupt-on-all-received-characters has the option of modifying the interrupt vector in the event of a parity error. Both of these interrupt modes will also interrupt under special receive conditions on a character or message basis (end-of-frame interrupt in SDLC, for example). This means that the special-receive condition can cause an interrupt only if the interrupt-on-first-received-character or interrupt-on-all-received-characters mode is selected. In interrupt-on-first-received-character, an interrupt can occur from special-receive conditions (except parity error) after the first-received-character interrupt (example: receive-overrun interrupt).

The main function of the external/status interrupt is to monitor the signal transitions of the Clear To Send ($\overline{CTS}$), Data Carrier Detect ($\overline{DCD}$) and Synchronization ($\overline{SYNC}$) pins (Figures 1 through 6). In addition, an external/status interrupt is also caused by a CRC-sending condition or by the detection of a break sequence (asynchronous mode) or abort sequence (SDLC mode) in the data stream. The interrupt caused by the break/abort sequence allows the SIO to interrupt when the break/abort sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the break/abort condition in external logic.

I/O Interface Capabilities (Continued)

In a Z-80 CPU environment (Figure 11), SIO interrupt vectoring is "automatic": the SIO passes its internally-modifiable 8-bit interrupt vector to the CPU, which adds an additional 8 bits from its interrupt-vector (I) register to form the memory address of the interrupt-routine table. This table contains the address of the beginning of the interrupt routine itself. The process entails an indirect transfer of CPU control to the interrupt routine, so that the next instruction executed after an interrupt acknowledge by the CPU is the first instruction of the interrupt routine itself.

CPU/DMA Block Transfer. The SIO's block-transfer mode accommodates both CPU block transfers and DMA controllers (Z-80 DMA or other designs). The block-transfer mode uses the Wait/Ready output signal, which is selected with three bits in an internal control register. The Wait/Ready output signal can be programmed as a $\overline{WAIT}$ line in the CPU block-transfer mode or as a $\overline{READY}$ line in the DMA block-transfer mode.

To a DMA controller, the SIO $\overline{READY}$ output indicates that the SIO is ready to transfer data to or from memory. To the CPU, the $\overline{WAIT}$ output indicates that the SIO is not ready to transfer data, thereby requesting the CPU to extend the I/O cycle.

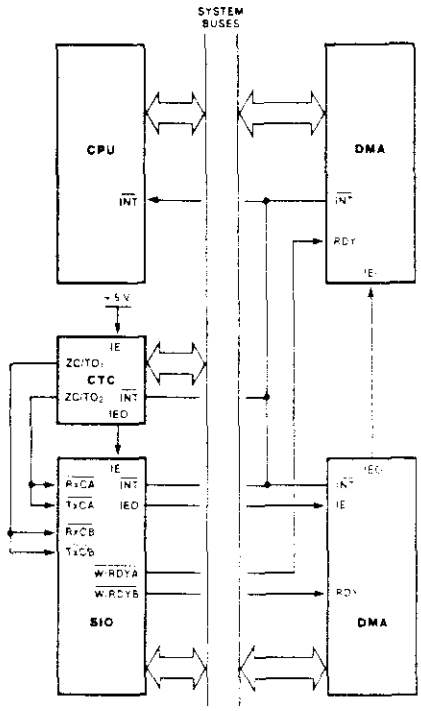


Figure 11. Typical Z-80 Environment

Internal Structure

The internal structure of the device includes a Z-80 CPU interface, internal control and interrupt logic, and two full-duplex channels. Each channel contains its own set of control and status (write and read) registers, and control and status logic that provides the interface to modems or other external devices.

The registers for each channel are designated as follows:

WR0-WR7 — Write Registers 0 through 7
RR0-RR2 — Read Registers 0 through 2

The register group includes five 8-bit control registers, two sync-character registers and two status registers. The interrupt vector is written into an additional 8-bit register (Write Register 2) in Channel B that may be read through another 8-bit register (Read Register 2) in Channel B. The bit assignment and functional grouping of each register is configured to simplify and organize the programming process. Table 1 lists the functions assigned to each read or write register.

Read Register Functions	
RR0	Transmit/Receive buffer status, interrupt status and external status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only)

Write Register Functions	
WR0	Register pointers, CRC initialize, initialization commands for the various modes, etc.
WR1	Transmit/Receive interrupt and data transfer mode definition.
WR2	Interrupt vector (Channel B only)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Sync character or SDLC address field
WR7	Sync character or SDLC flag

Internal Structure (Continued)

The logic for both channels provides formats, synchronization and validation for data transferred to and from the channel interface. The modem control inputs, Clear To Send ($\overline{CTS}$) and Data Carrier Detect ($\overline{DCD}$), are monitored by the external control and status logic under program control. All external control-and-status-logic signals are general-purpose in nature and can be used for functions other than modem control.

Data Path. The transmit and receive data path illustrated for Channel A in Figure 12 is identical for both channels. The receiver has three 8-bit buffer registers in a *FIFO* arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode and—in asynchronous modes—the character length.

The transmitter has an 8-bit transmit data buffer register that is loaded from the internal data bus, and a 20-bit transmit shift register that can be loaded from the sync-character *buffers or from the transmit data register*. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the Transmit Data output (TxD).

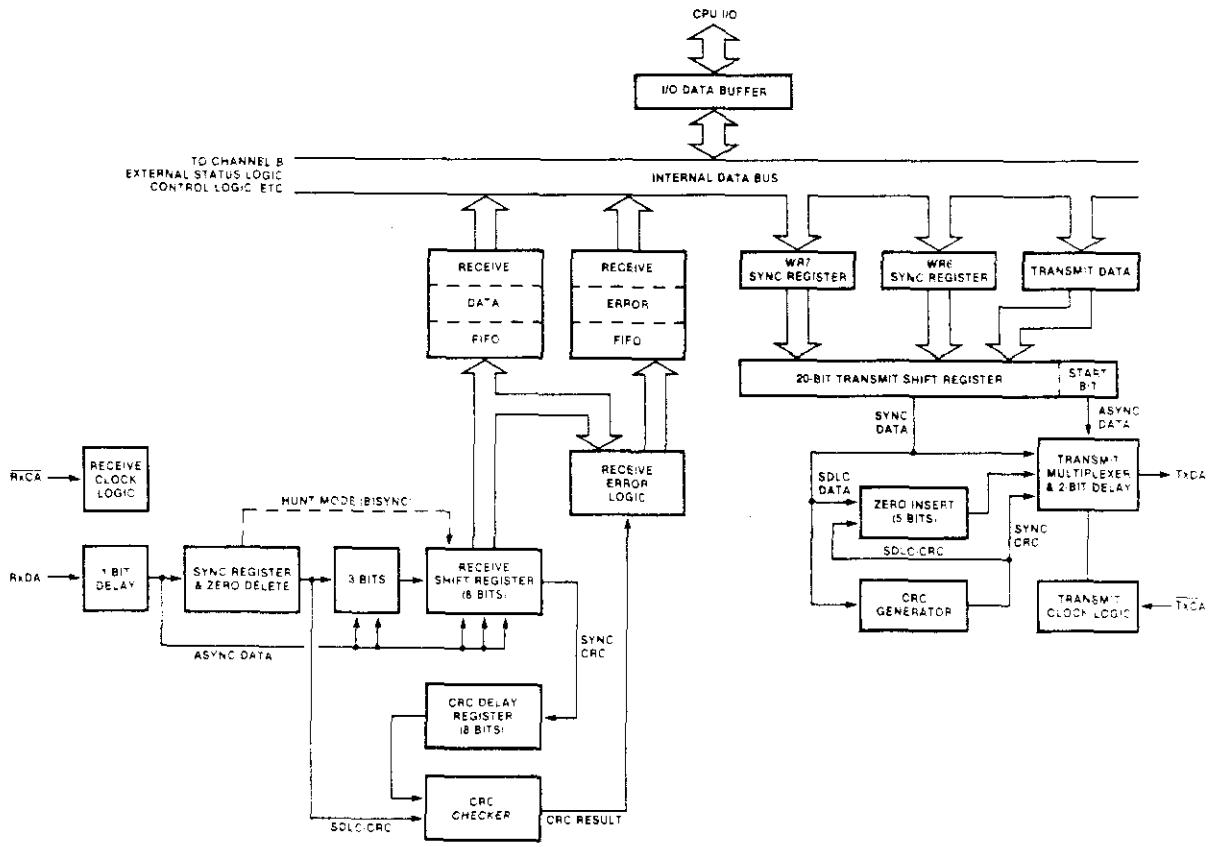


Figure 12. Transmit and Receive Data Path (Channel A)

Programming

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first; then the interrupt mode; and finally, receiver or transmitter enable.

Both channels contain registers that must be programmed via the system program prior to operation. The channel-select input (B/$\overline{A}$) and the control/data input (C/$\overline{D}$) are the command-structure addressing controls, and are normally controlled by the CPU address bus. Figures 15 and 16 illustrate the timing relationships for programming the write registers and transferring data and status.

Read Registers. The SIO contains three read registers for Channel B and two read registers for Channel A (RR0-RR2 in Figure 13) that can be read to obtain the status information; RR2 contains the internally-modifiable interrupt vector and is only in the Channel B register set. The status information includes error conditions, interrupt vector and standard communications-interface signals.

To read the contents of a selected read register other than RR0, the system program must first write the pointer byte to WR0 in exactly the same way as a write register operation. Then, by executing a read instruction, the contents of the addressed read register can be read by the CPU.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates that a Special Receive Condition interrupt has occurred, all the appropriate error bits can be read from a single register (RR1).

Write Registers. The SIO contains eight write registers for Channel B and seven write registers for Channel A (WR0-WR7 in Figure 14) that are programmed separately to configure the functional personality of the channels; WR2 contains the interrupt vector for both channels and is only in the Channel B register set. With the exception of WR0, programming the write registers requires two bytes. The first byte is to WR0 and contains three bits (D_0-D_2) that point to the selected register; the second byte is the actual control word that is written into the register to configure the SIO.

WR0 is a special case in that all of the basic commands can be written to it with a single byte. Reset (internal or external) initializes the pointer bits D_0-D_2 to point to WR0. This implies that a channel reset must not be combined with the pointing to any register.

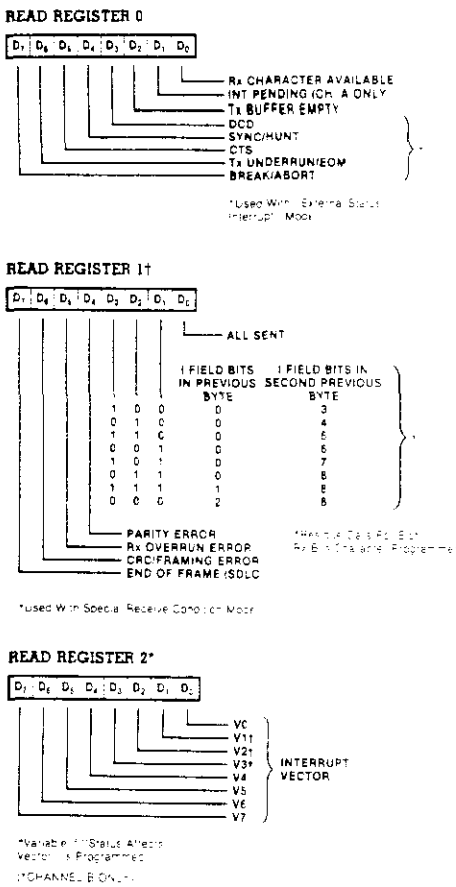


Figure 13. Read Register Bit Functions

Programming (Continued)

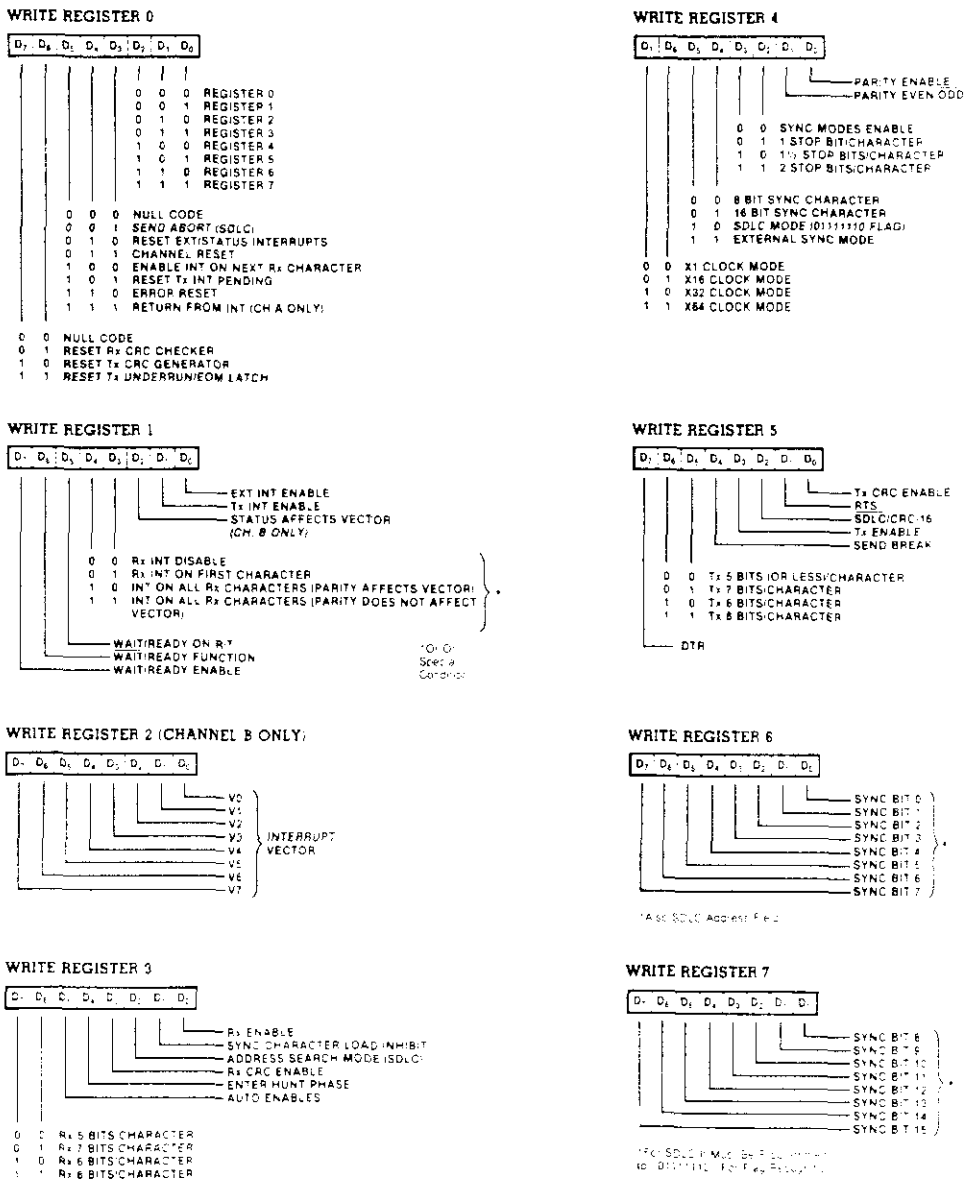


Figure 14. Write Register Bit Functions

Timing

The SIO must have the same clock as the CPU (same phase and frequency relationship, not necessarily the same driver).

Read Cycle. The timing signals generated by a Z-80 CPU input instruction to read a data or status byte from the SIO are illustrated in Figure 15.

Write Cycle. Figure 16 illustrates the timing and data signals generated by a Z-80 CPU output instruction to write a data or control byte into the SIO.

Interrupt-Acknowledge Cycle. After receiving an interrupt-request signal from an SIO ($\overline{INT}$ pulled Low), the Z-80 CPU sends an interrupt-acknowledge sequence ($\overline{M1}$ Low, and $\overline{IORQ}$ Low a few cycles later) as in Figure 17.

The SIO contains an internal daisy-chained interrupt structure for prioritizing nested interrupts for the various functions of its two channels, and this structure can be used within an external user-defined daisy chain that prioritizes several peripheral circuits.

The IEI of the highest-priority device is terminated High. A device that has an interrupt pending or under service forces its IEO Low. For devices with no interrupt pending or under service, IEO = IEI.

To insure stable conditions in the daisy chain, all interrupt status signals are prevented from changing while $\overline{M1}$ is Low. When $\overline{IORQ}$ is Low, the highest priority interrupt requestor (the one with IEI High) places its interrupt vector on the data bus and sets its internal interrupt-under-service latch.

Return From Interrupt Cycle. Figure 18 illustrates the return from interrupt cycle. Normally, the Z-80 CPU issues a RETI (Return From Interrupt) instruction at the end of an interrupt service routine. RETI is a 2-byte opcode (ED-4D) that resets the interrupt-under-service latch in the SIO to terminate the interrupt that has just been processed. This is accomplished by manipulating the daisy chain in the following way.

The normal daisy-chain operation can be used to detect a pending interrupt; however, it cannot distinguish between an interrupt under service and a pending unacknowledged interrupt of a higher priority. Whenever "ED" is decoded, the daisy chain is modified by forcing High the IEO of any interrupt that has not yet been acknowledged. Thus the daisy chain identifies the device presently under service as the only one with an IEI High and an IEO Low. If the next opcode byte is "4D," the interrupt-under-service latch is reset.

The ripple time of the interrupt daisy chain (both the High-to-Low and the Low-to-High transitions) limits the number of devices that can be placed in the daisy chain. Ripple time can be improved with carry-look-ahead, or by extending the interrupt-acknowledge cycle. For further information about techniques for increasing the number of daisy-chained devices, refer to the *Z-80 CPU Product Specification*.

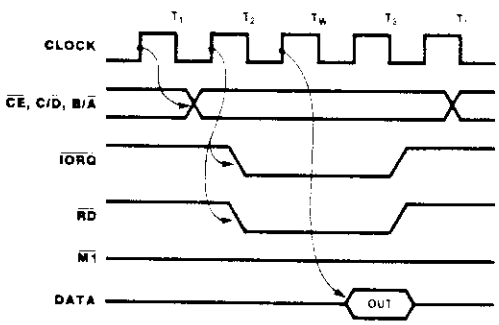


Figure 15. Read Cycle

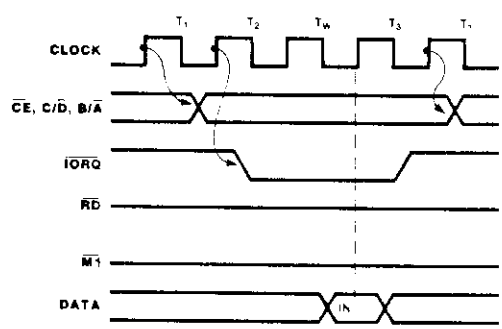


Figure 16. Write Cycle

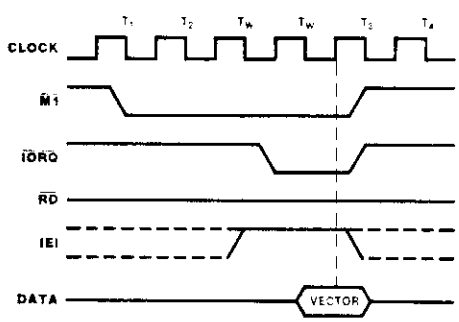


Figure 17. Interrupt Acknowledge Cycle

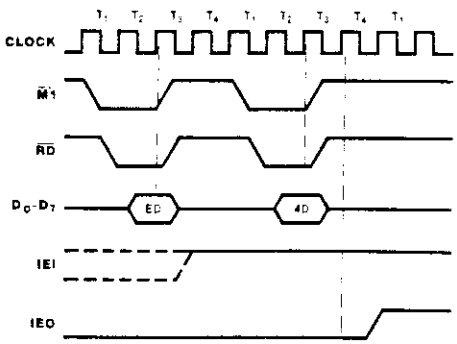


Figure 18. Return from Interrupt Cycle

Absolute Maximum Ratings

Voltages on all inputs and outputs with respect to GND . . . . . -0.3 V to +7.0 V

Operating Ambient Temperature . . . . . As Specified in Ordering Information

Storage Temperature . . . . . -65°C to +150°C

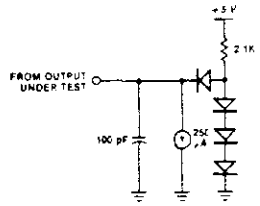
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Test Conditions

The characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND (0 V). Positive current flows into the referenced pin. Available operating temperature ranges are:

- S* = 0°C to +70°C, +4.75 V ≤ V_{CC} ≤ +5.25 V
- E* = −40°C to +85°C, +4.75 V ≤ V_{CC} ≤ +5.25 V
- M* = −55°C to +125°C, +4.5 V ≤ V_{CC} ≤ +5.5 V

*See Ordering Information section for package temperature range and product number.



The product number for each operating temperature range can be found in the ordering information included in the product specification (see 1982/83 Zilog Data Book, document number 00-2034-02).

DC Characteristics

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	−0.3	+0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC} − 0.6	V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	+2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	+2.4		V	I_{OH} = −250 μA
I_{LI}	Input Leakage Current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LO}	3-State Output Leakage Current in Float		±10	μA	V_{OUT} = 0.4 V to V_{CC}
I_{LSY}	$\overline{SYNC}$ Pin Leakage Current		+10/−40	μA	0 < V_{IN} < V_{CC}
I_{CC}	Power Supply Current		30	mA	

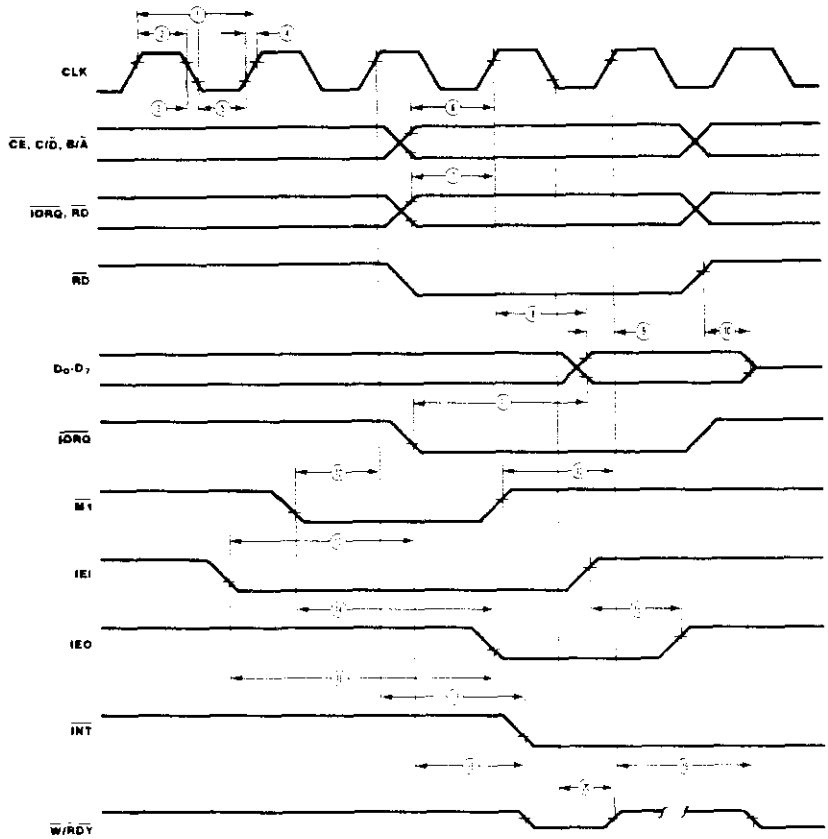
Over specified temperature and voltage ranges.

Capacitance

Symbol	Parameter	Min	Max	Unit	Test Condition
C	Clock Capacitance		40	pF	Unmeasured
C_{IN}	Input Capacitance		5	pF	pins returned
C_{OUT}	Output Capacitance		10	pF	to ground

Over specified temperature range; f = 1 MHz.

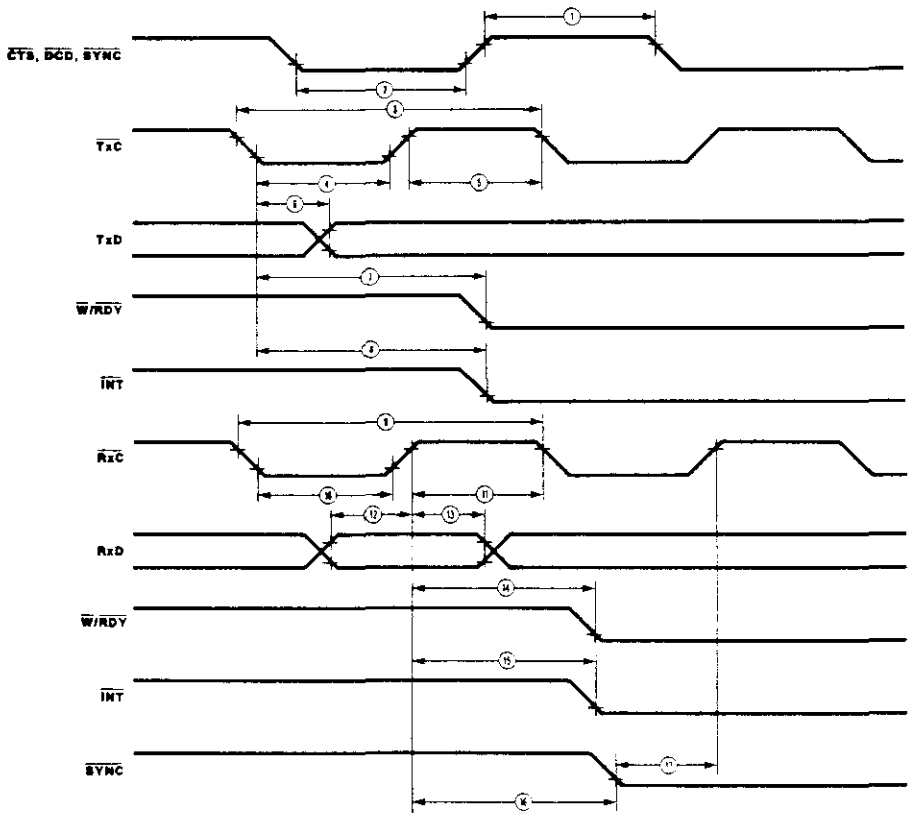
AC Electrical Characteristics



Number	Symbol	Parameter	Z-80 SIO Min	Z-80 SIO Max	Z-80A SIO Min	Z-80A SIO Max	Z-80B SIO*† Min	Z-80B SIO*† Max
1	TcC	Clock Cycle Time	400	4000	250	4000	165	4000
2	TwCh	Clock Width (High)	170	2000	105	2000	70	2000
3	TfC	Clock Fall Time		30		30		15
4	TrC	Clock Rise Time		30		30		15
5	TwCl	Clock Width (Low)	170	2000	105	2000	70	2000
6	TsAD(C)	CE, C/D, B/A to Clock ↑ Setup Time	160		145		60	
7	TsCS(C)	IORQ, RD to Clock ↑ Setup Time	240		135		60	
8	TdC(DO)	Clock ↓ to Data Out Delay		240		220		150
9	TsDI(C)	Data In to Clock ↑ Setup (Write or M1 Cycle)	50		50		30	
10	TdRD(DOz)	RD ↑ to Data Out Float Delay		230		130		90
11	TdIO(DO)	IORQ ↓ to Data Out Delay (INTACK Cycle)		340		160		100
12	TsM1(C)	M1 to Clock ↑ Setup Time	210		90		75	
13	TsIEI(IO)	IEI to IORQ ↓ Setup Time (INTACK Cycle)	200		140		120	
14	TdM1(IEO)	M1 ↓ to IEO ↓ Delay (interrupt before M1)		300		190		160
15	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED decode)		150		100		70
16	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		150		100		70
17	TdC(INT)	Clock ↑ to INT ↓ Delay		200		200		150
18	TdIO(W/RWf)	IORQ ↓ or CE ↓ to W/RDY ↓ Delay Wait Mode)		300		210		170
19	TdC(W/RR)	Clock ↑ to W/RDY ↓ Delay (Ready Mode)		120		120		100
20	TdC(W/RWz)	Clock ↓ to W/RDY Float Delay (Wait Mode)		130		130		110
21	Th	Any unspecified Hold when Setup is specified	0		0		0	

* Z-80 SIO timings are preliminary and subject to change.
† Units in nanoseconds (ns).

AC Electrical Characteristics (Continued)



Number	Symbol	Parameter	Z-80 SIO Min	Z-80 SIO Max	Z-80A SIO Min	Z-80A SIO Max	Z-80B SIO[1] Min	Z-80B SIO[1] Max	Notes†
1	TwPh	Pulse Width (High)	200		200		200		2
2	TwPl	Pulse Width (Low)	200		200		200		2
3	TcTxC	$\overline{TxC}$ Cycle Time	400	∞	400	∞	330	∞	2
4	TwTxCl	$\overline{TxC}$ Width (Low)	180	∞	180	∞	100	∞	2
5	TwTxCh	$\overline{TxC}$ Width (High)	180	∞	180	∞	100	∞	2
6	TdTxC(TxD)	$\overline{TxC}$ ↓ to TxD Delay (x1 Mode)		400		300		220	2
7	TdTxC(W/RRI)	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	5	9	5	9	5	9	3
8	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5	9	5	9	5	9	3
9	TcRxC	$\overline{RxC}$ Cycle Time	400	∞	400	∞	330	∞	2
10	TwRxCl	$\overline{RxC}$ Width (Low)	180	∞	180	∞	100	∞	2
11	TwRxCh	$\overline{RxC}$ Width (High)	180	∞	180	∞	100	∞	2
12	TsRxD(RxC)	RxD to $\overline{RxC}$ ↑ Setup Time (x1 Mode)	0		0		0		2
13	ThRxD(RxC)	RxC ↑ to RxD Hold Time (x1 Mode)	140		140		100		2
14	TdRxC(W/RRI)	$\overline{RxC}$ ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	10	13	10	13	10	13	3
15	TdRxC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ Delay	10	13	10	13	10	13	3
16	TdRxC(SYNC)	RxC ↑ to $\overline{SYNC}$ ↓ Delay (Output Modes)	4	7	4	7	4	7	3
17	TsSYNC(RxC)	$\overline{SYNC}$ ↓ to $\overline{RxC}$ ↑ Setup (External Sync Modes)	-100		-100		-100		2

NOTES:
1. In all modes the System Clock rate must be at least five times the maximum data rate.
2. Z-80B SIO timings are preliminary and subject to change.
2. Units in nanoseconds (ns).
3. Units equal to System Clock Periods.

Ordering Information

Product Number	Package/ Temp	Speed	Description
Z8440	CE,CM	2.5 MHz	Z80 SIO/0 (40-pin)
Z8440	CMB,CS	2.5 MHz	Same as above
Z8440	DE,DS	2.5 MHz	Same as above
Z8440	PE,PS	2.5 MHz	Same as above
Z8440A	CE,CM	4.0 MHz	Z80A SIO/0 (40-pin)
Z8440A	CMB,CS	4.0 MHz	Same as above
Z8440A	DE,DS	4.0 MHz	Same as above
Z8440A	PE,PS	4.0 MHz	Same as above
Z8440B	CS	6.0 MHz	Z80B SIO/0 (40-pin)
Z8440B	DS	6.0 MHz	Same as above
Z8440B	PS	6.0 MHz	Same as above
Z8441	CE,CM	2.5 MHz	Z80 SIO/1 (40-pin)
Z8441	CMB,CS	2.5 MHz	Same as above
Z8441	DE,DS	2.5 MHz	Same as above
Z8441	PE,PS	2.5 MHz	Same as above
Z8441A	CE,CM	4.0 MHz	Z80A SIO/1 (40-pin)
Z8441A	CMB,CS	4.0 MHz	Same as above
Z8441A	DE,DS	4.0 MHz	Z80B SIO/1 (40-pin)
Z8441A	PE,PS	4.0 MHz	Same as above
Z8441B	CS	6.0 MHz	Z80B SIO/1 (40-pin)
Z8441B	DS	6.0 MHz	Same as above
Z8441B	PS	6.0 MHz	Same as above
Z8442	CE,CM	2.5 MHz	Z80 SIO/2 (40-pin)
Z8442	CMB,CS	2.5 MHz	Same as above
Z8442	DE,DS	2.5 MHz	Same as above
Z8442	PE,PS	2.5 MHz	Same as above
Z8442A	CE,CM	4.0 MHz	Z80A SIO/2 (40-pin)
Z8442A	CMB,CS	4.0 MHz	Same as above
Z8442A	DE,DS	4.0 MHz	Same as above
Z8442A	PE,PS	4.0 MHz	Same as above
Z8442B	CS	6.0 MHz	Z80B SIO/2 (40-pin)
Z8442B	DS	6.0 MHz	Same as above
Z8442B	PS	6.0 MHz	Same as above

*NOTES: C = Ceramic, D = Cerdip, P = Plastic, E = -40°C to +85°C, M = -55°C to +125°C, MB = -55°C to +125°C with MIL-STD-883 with Class B processing, S = 0°C to +70°C.