

SOPHISTICATED 256K MEMORY

256KMB-100 From Intercontinental Micro Systems

SOPHISTICATED? PROVE IT.

Read the features, the specs, the description and find out about our 256K memory, personality boards and CPU. We're betting you'll like what you see.

- IEEE S100 bus, spec 696.1/D2. The 256KMB-100 is compatible with most IEEE S100 board products now on the market.
- Linear addressable to 2 megabytes.
- 222 nano-second access time, maximum, 160 nano-seconds, typical.
- 295 nano-second read-write time, minimum.
- Bank selectable in 16K increments. Any combination of 16K banks is possible—4 64K users, 8 32K users, 16 16K users or any other combinations.
- I/O port address bank selection.
- Configures for phantom deselection.
- Parity error detection, visual and/or interrupts.
- Can accommodate IEEE, 8080™, Z-80™, Alpha Micro timing.
- Bank selection compatible with CROMIX™

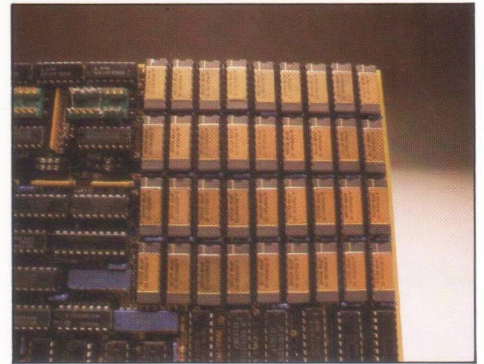
CP/M 2.2™, MP/M™, Alpha Micro, and other major systems.

- Fully compatible with our CPZ-48000 single board CPU.

FEATURES DON'T MAKE A BOARD GREAT, OVERALL PERFORMANCE DOES.

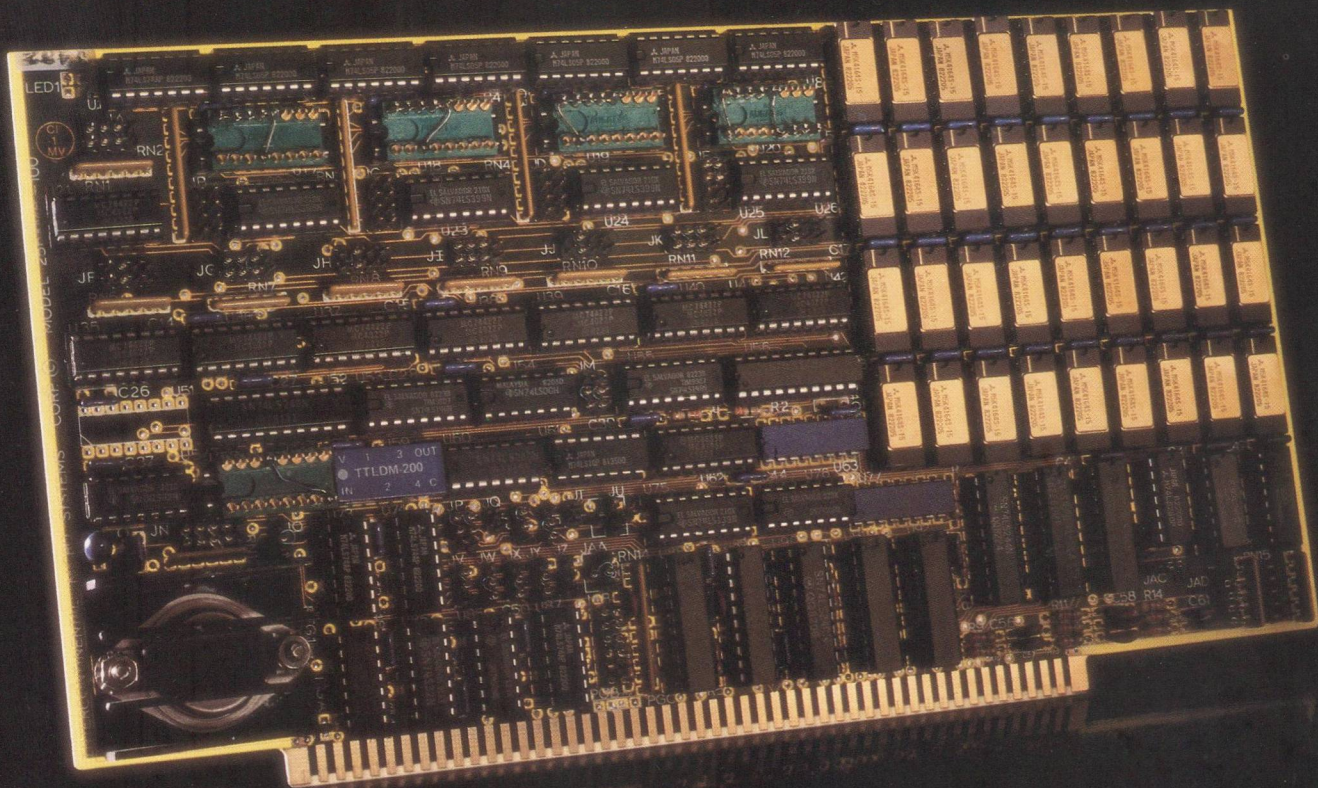
The 256KMB™ uses the 4164S-150 64K x 1 bit dynamic RAM chip giving the user 225 nano-second (max) access time with simple, reliable Z80 or 8080 refresh capability. The board may be operated as a bank selectable or linear addressable memory.

Each bank may reside at addresses within a 64 Kbyte address space starting at location 0000H, 4000H, 8000H or C000H as set by jumper options. One or more banks may reside in the same address space. Each bank is individually enabled or disabled at system reset time, depending on jumper option settings. Each bank is selectable through open collector data BUS drivers via 20 pin dip headers to allow complete flexibility in implementing bank selection methods compatible with Cromemco (open-collector OR-ties to select banks simultane-

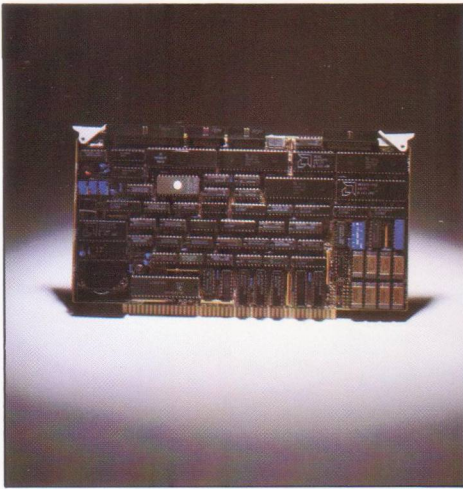


ously) or Alpha-Micro (banks selected in direct correspondence with active data bits). Each bank may be "phantomed" (disabled when the S100 BUS signal phantom goes active) or may be configured to disregard phantom.

Up to 2 megabytes of linear address memory may be configured. The beginning address may commence at any 64 Kbyte boundary as specified by the user.



Performance Specifications



A window deselection within the 64 Kbyte address space may be specified via headers. The window may take any size from 4K to 64 Kbytes and resides at 4 Kbyte boundaries. The starting and ending address of deselection are specified through headers. Parity error detection is provided. A light emitting diode gives visual error indications and the user may connect the error signal to MNI (Pin 12) or ERROR (Pin 98) of the S100 BUS. Refresh is accomplished with minimal circuitry thus providing greater reliability. The 256KMB is ideal for operation as a turbo disk file cache also known as memory disk or RAM disk. Operating the CPZ-48000 Central Processor Unit with Turbo-Disk™ and memory-to-memory transfers under direct memory access (DMA) control, block move transfers are enhanced by a factor of 3 over Z80™ block moves.

Fast and flexible. The 256 KMB-100 from Intercontinental Micro Systems.

SOUNDS GOOD. BUT WHAT'S RAM DISK, PARITY ERROR DETECTION AND WINDOW DESELECTION?

RAM Disk: RAM that emulates disk memory, speeds file access and throughput by up to 300%.

Parity Error Detection: Memory failures automatically result in error signal.

Window Deselection: Defines upper and lower boundaries in 4K increments for dedication to off-board memory devices. Allows off-board device to appear in corresponding address space.

HOW USING OUR WHOLE PRODUCT LINE WILL HELP YOU

The CPZ-48000 CPU and 256KMB-100 from Intercontinental Micro Systems give you the perfect team for the most demanding of tasks—Multi-user/multi-tasking, RAM disk or single user functions.

PERSONALITY PLUS

With our CPZ-48000 and 256KMB-100 you can get a complete line of personality boards that will provide easy interface for all kinds of peripherals—printers, floppies, modems, winchesters—you name it. Best of all they're small and won't take up any S100 bus space.

The simple, black and white proof—the 256KMB-100 is the highest performance 256K, S100 Bus Memory available today.

BUS INTERFACE... IEEE 696.1/D2

MICROPROCESSOR COMPATIBILITY... Any Z80 or 8080 board micro processor operating up to 4MHz

WAIT STATES... None required

MEMORY CAPACITY... 262,144 bytes (256 Kbytes)

MEMORY ACCESS TIME... 225 Nano-seconds (max)

READ/WRITE CYCLE TIME... 295 Nano-seconds (min)

BANK SELECTION... Banks set or reset through I/O Port Commands. I/O Port Address Assignment selectable through jumper options

Configurations...

16—16 Kbyte banks

8—32 Kbyte banks

4—64 Kbyte banks

or any combination of 16 Kbyte banks; e.g., 5—48 Kbyte banks and 1—16 Kbyte bank

Reset... Each Bank separately enabled or disabled through jumper options

Phantom... All banks disabled with phantom or configured to disregard phantom with jumper option

Address Allocation... Each bank assignable to location 0000H, 4000H, 8000H, or C000H through jumper options.

I/O Port Assignments...

| A7 | A6 | A5 | A4 | A3 | A1 | A0 | Function |
|----|----|----|----|----|----|----|--------------------|
| X | X | X | X | X | 0 | 0 | Bank Select 0H-7H |
| X | X | X | X | X | 0 | 1 | Bank Select 8H-FH |
| X | X | X | X | X | 1 | 0 | Clear Parity Error |
| X | X | X | X | X | 1 | 1 | Undefined |

LINEAR ADDRESSING... Configurable as 8 pages of 256 Kbytes each for a contiguous memory spanning an address of 000000H to 1FFFFFFH for a total of 2,097,152 bytes (2 megabytes)

WINDOW DESELECTION... 4K to 64 Kbytes of deselection on 4 Kbyte boundaries as defined by jumper options.

POWER REQUIREMENTS

Voltagess... +8V DC @ 1.5 A (max.)

Power... 12W (max)

OPERATING ENVIRONMENT

Temperature... 0 to 45 Degrees Celsius

Relative Humidity... 0 to 95%

CONSTRUCTION

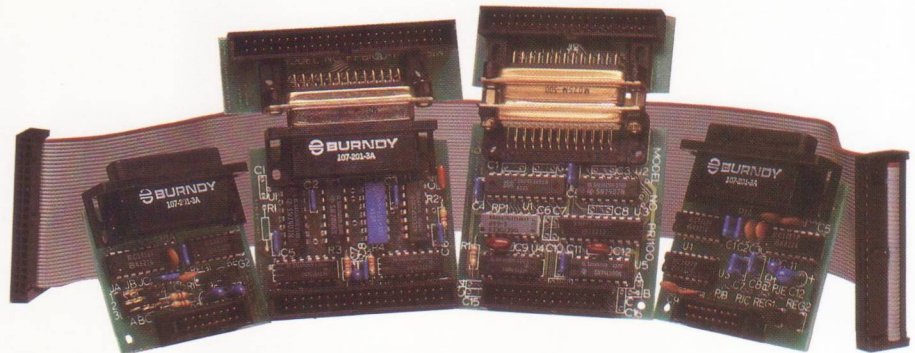
Circuit Board... Four Layer Glass Epoxy; Soldermask over copper. All IC's in sockets

TESTING... Tested and Burned-In

WARRANTY... One Year Warranty (Parts and Labor)

CALL

Call today, we'd love to help you with your memory application problems.



TM CP/M and MP/M are trademarks of DIGITAL RESEARCH
CROMIX is a trademark of CROMEMCO
Z80 is a trademark of ZILOG, INC.
Turbo-Disk is a trademark of Intercontinental Micro Systems, Corp.





256 KMB-100 RAM MEMORY BOARD

The 256KMB is a 256K RAM MEMORY BOARD designed to comply with the IEEE 696.1/D2 S-100 BUS standard. It is a very versatile memory board that is compatible with most S-100 compatible SBC's. It can be interfaced with most Z80's, 8080's and 8085's. It also conforms to IEEE, Z80, 8080 and Alpha-Micro timing standards.

The 256KMB can be addressed three different ways:

- LINEAR ADDRESSABLE:** The MEMORY MANAGEMENT UNIT (MMU) available on ICM's CPZ-48000 SBC expands the CPZ's address bus from the standard 16 bits to a full 24 bit address bus. This allows the CPZ to linearly address 2 MBYTES of memory instead of the usual 64 KBytes all other 8 bit CPU's can address. This addressing capability is equal to or better than any 16 bit CPU on the market. EIGHT KMB256's can be stacked on the bus to take full advantage of this extended memory addressing capability.
- TURBODISK (RAM DISK):** The TURBODISK capabilities of ICM's CPZ can be fully utilized with the 256KMB. No other SBC on the market offers a TURBODISK capability. Turbodisk allows the 256KMB memory board to emulate disk memory. Using TURBODISK in combination with DIRECT MEMORY ACCESS (DMA) increases file access and throughput by 300%. This technique results in the fastest method of storing and retrieving data known.
- BANK SELECTABLE:** This very flexible addressing technique can be used under Cromix, MP/M, CP/M2.2, or ALPHA-MICRO. It is adaptable to any I/O addressing scheme and the user can select any I/O port address. It can support Multi-users in any combination of 16K increments: 4-64K users, 8-32K users, 16-16K users, etc.

PHANTOM DESELECTION expands memory capabilities by allowing other devices (such as PROM, EPROM, ROM, VIDEO MAPPED I/O, etc) to be addressed on the same address space.

WINDOW DESELECTION allows substitution of other memory mapped devices on the same address space. WINDOW DESELECTION is in 4 KBYTE sectors and can be programmed via SOFTWARE with ICM's CPZ-48000, or via hardware headers with other SBC's.

PARITY ERROR NOTIFICATION is immediate and automatic. The 256KMB offers three types of notification: (1) a visual indicator is provided via an on-board LED; (2) an automatic CPU interrupt signal is generated; and (3) an error signal can be sent on the S-100 BUS error pin.