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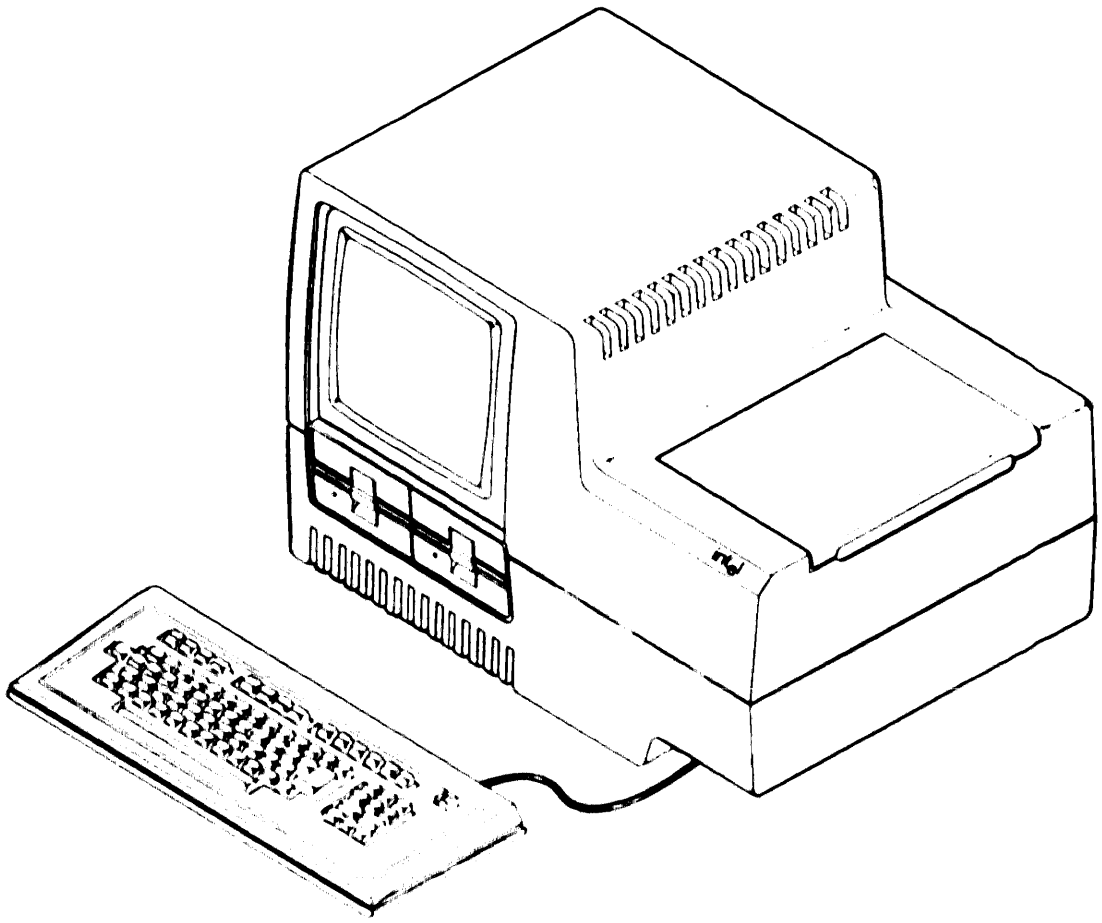
INTELLEC SERIES IV
INSTALLATION AND CHECKOUT
MANUAL



Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 121757-002

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INSTALLATION AND CHECKOUT
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iATC	int$_e$lBOS	iSDM	Promware
I²ICE	Intelevision	iSXM	Ripplemode
ICE	int$_e$ligent Identifier	Library Manager	RMX/80
iCS	int$_e$ligent Programming	MCS	RUPI
iDBP	Intellec	Megachassis	SYSTEM 2000
			UPI

and the combination of ICE, iCS, iRMX, iSBC, iSBX, or MCS and a numerical suffix.

REV.	REVISION HISTORY	DATE
001	Original Release per ECO #54415.	04/83
002	056 Memory Board Configuration Change per ECO #54735.	07/83

PREFACE

This manual is intended for use by the design engineer, programmer, or technician who will install and maintain the Intellec Series IV Microcomputer Development System. The manual is divided into five chapters and one appendix as follows:

- Chapter 1, General information, provides a physical and functional description and relevant specifications for the system.
- Chapter 2, Installation, provides information for pre installation requirements, and installation of the standard system.
- Chapter 3, System Operation and Verification, describes and provides procedures for the power-up and confidence tests that verify system performance.
- Chapter 4, Installing Options, provides information for installing optional boards in the system to fit a variety of configurations.
- Chapter 5, Service Information, contains basic troubleshooting information and instructions on how to obtain service and repair assistance.
- Appendix A, Confidence Test Commands, describes and provides examples for use of the confidence test commands.

Information for installing external disk drives for use with the Series IV Development System is contained in the *External Peripheral Chassis Installation and Checkout Manual,* Order Number 121766.

Additional information on the system and a list of users manuals are provided in the *Intellec Series IV Microcomputer Development System Product Overview,* Order Number 121752.

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FIGURES

CHAPTER 1
GENERAL DESCRIPTION

1.1 Introduction

This chapter provides a basic introduction to the physical and functional characteristics of the Series IV Development System (hereafter referred to as the Series IV or just the system). It contains a physical and functional description of the system and its major subassemblies, and a summary of the physical, functional and environmental specifications. It also includes information on available options, typical system configurations and power supply loading.

1.2 Physical Description

The physical system consists of two major assemblies: the mainframe and the keyboard (see Figure 1-1).

1.2.1 Mainframe

The mainframe contains a CRT subsystem, a 5¼-inch Winchester Disk Drive and a 5¼-inch floppy disk drive or dual 5¼-inch floppy disk drives, a multiple-output power supply, an auxiliary 5 volt power supply, a 10-slot card cage and three cooling fans. These subassemblies are contained in a high-impact structurally strengthened plastic enclosure. A rear panel on the enclosure contains the system RESET switch, the

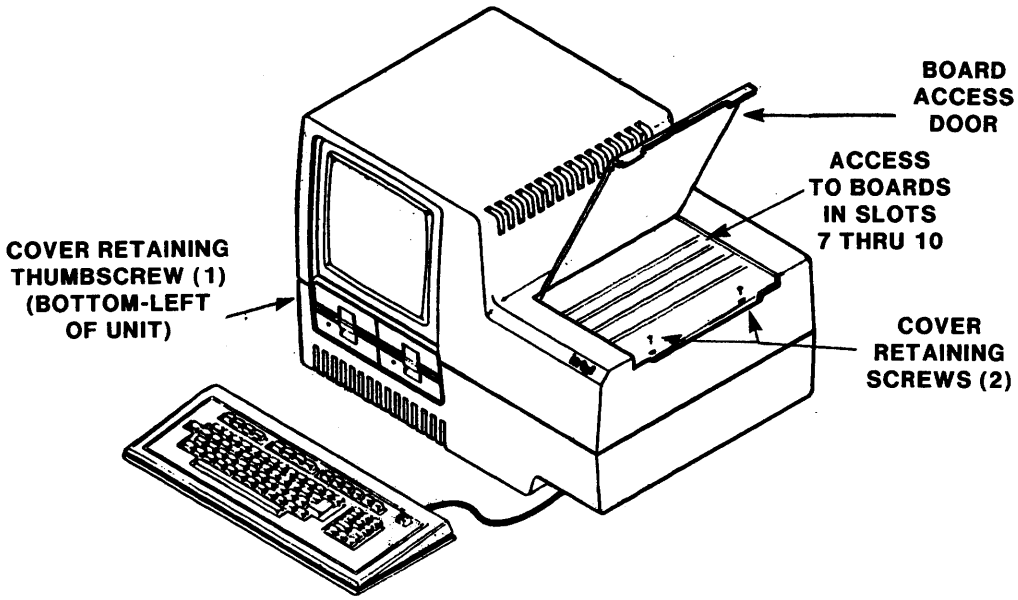


Figure 1-1. Intellec Series IV Development System

configuration switches, a line printer connector and two serial channel connectors. (See Figure 1-2).

1.2.2 Card Cage

The card cage includes a 10-slot motherboard that uses Multibus backplane architecture. This architecture enables more than one bus master, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. For standard configurations: card slots 1 & 2 (nearest the CRT) will contain a Central Processor I/O board (CPIO) and an ISIS Execution Unit (IEU); slot 4 contains an iSBC-056 (256-Kbyte) Memory board. Optional configurations add a Slave Processor Unit (SPU) in the third slot. Whatever the configuration, the first three slots will accommodate 12-inch by 12-inch (30.48 by 30.48 centimeters) boards that are covered by an RFI shield (see Figure 1-3).

The remaining seven slots accommodate 6.75-inch by 12-inch (18.63 by 30.48 centimeters) boards and are used to accommodate options such as expansion memory boards, controller boards for peripheral disk drives, network communication boards, and In-Circuit Emulator (ICE) boards. Four of these slots are accessible through a

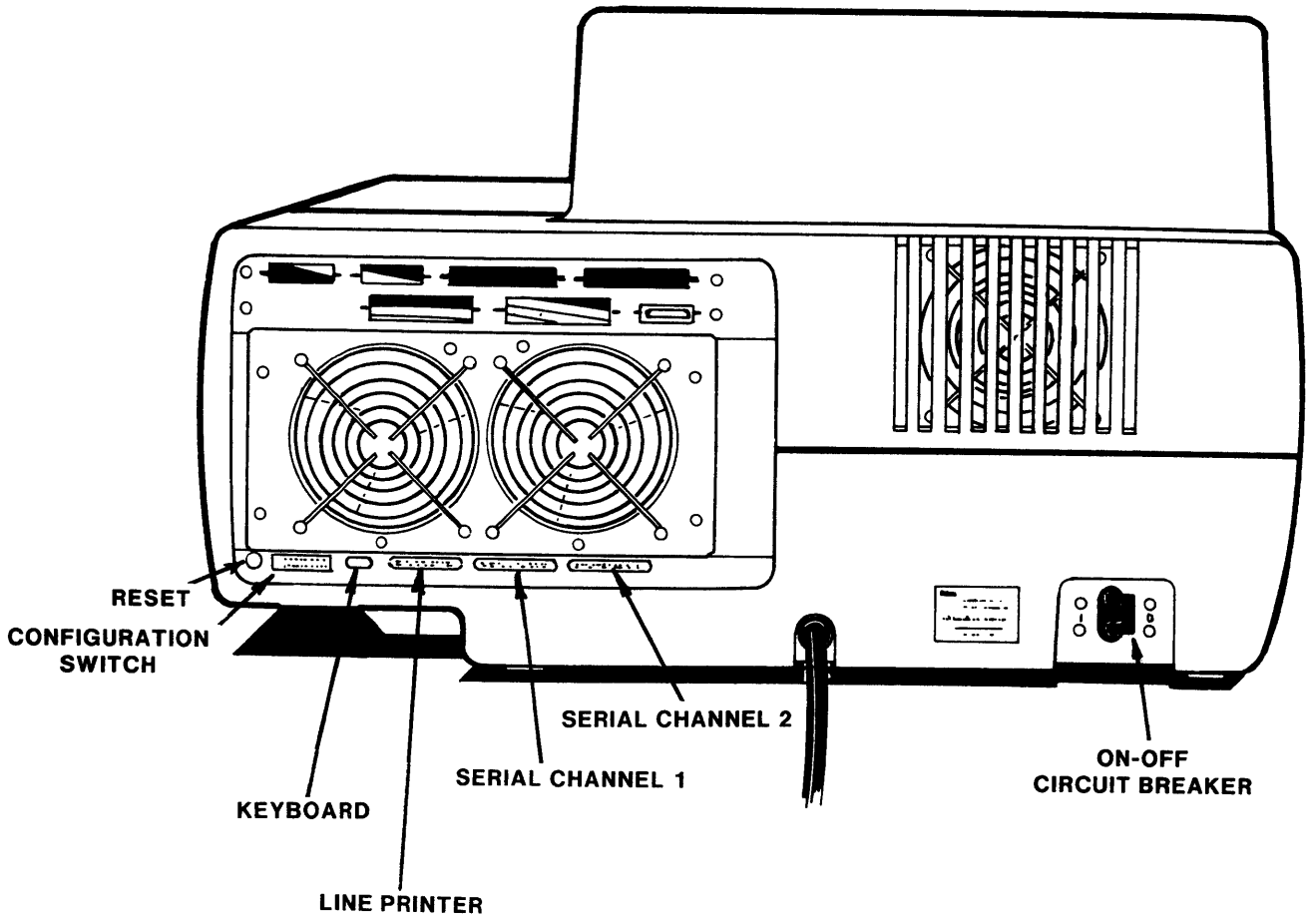


Figure 1-2. Series IV, Rear View

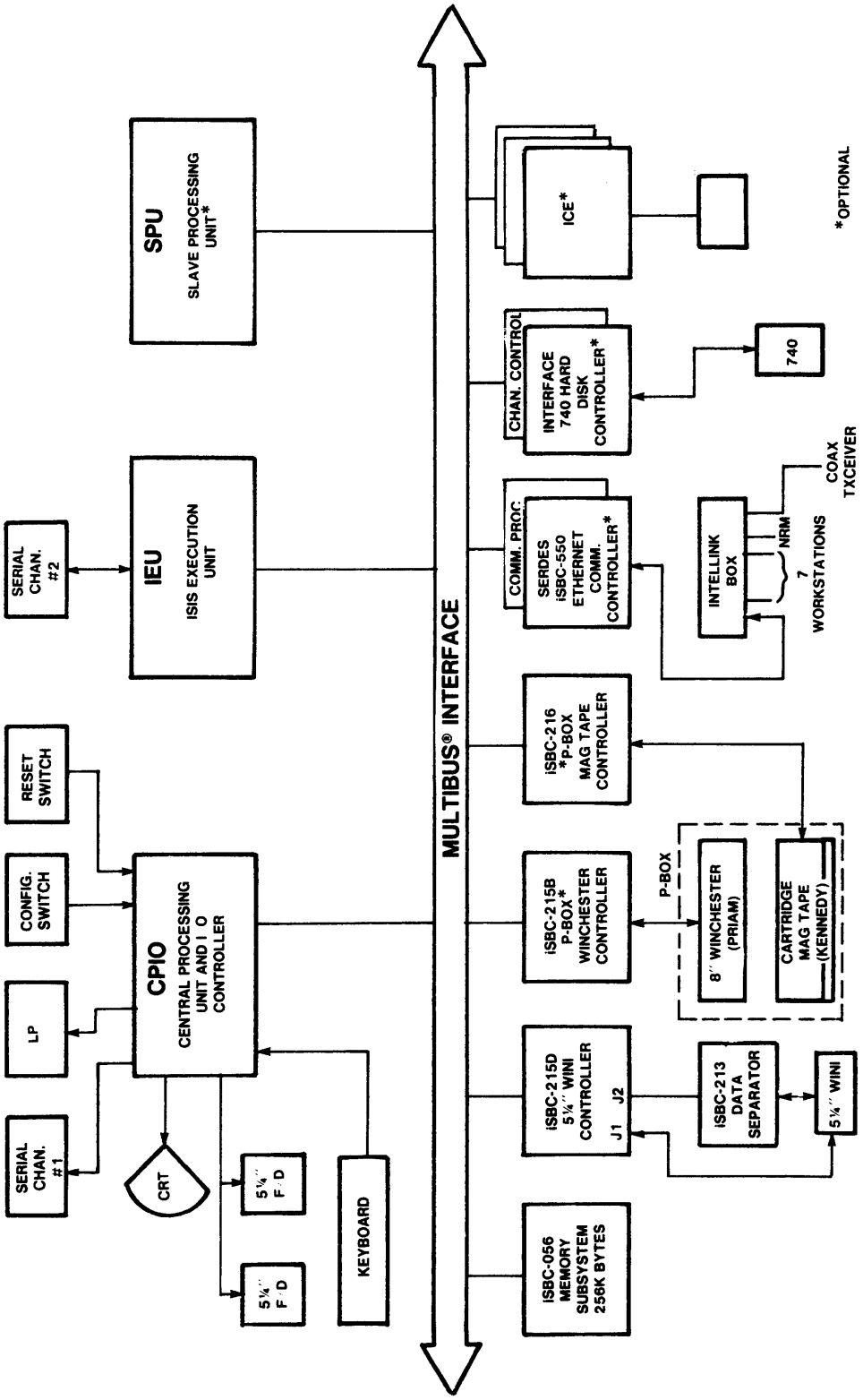


Figure 1-3. Series IV, Functional Block Diagram

hinged door over the top of the card cage and the other three may be accessed only by removing the top cover of the system.

In addition to the backplane connectors, the motherboard houses the system power distribution and I/O connectors. This includes connectors for power to the floppy and Winchester disk drives, floppy and Winchester I/O, power for CRT, input power from the multiple-output power supply, two serial I/O channels, a line printer channel and the keyboard.

1.3 Functional Description

The Series IV is a microcomputer development system that can be used in a standalone or network environment. This manual deals mainly with the standalone installation where the system is used as a free-standing, self-contained, data input and display computer. Various applications of the system can be enhanced and new applications added by installing options such as expansion memory and peripheral devices.

A functional block diagram of the Series IV system is shown in Figure 1-3. The function of its major modules is described in the following paragraphs.

1.3.1 Multiple-Output Power Supply

The multiple-output power supply provides the main dc power for the system. This switching type power supply receives input of 110-volts, 60Hz or 220-volts, 50Hz through a power circuit breaker switch and a line filter. For 110-volt operation, the circuit breaker is rated at 15 amperes; for 220-volt operation, 10 amperes.

The power supply provides five dc outputs as follows:

+5.1 V	+ 1% at	45.0 amperes maximum
+12.0 V	+ 5% at	1.1 amperes maximum
+12.0 V	+ 5% at	4.6 amperes maximum
−12.0 V	+ 5% at	2.0 amperes maximum
−10.0 V	+ 5% at	.5 amperes maximum

1.3.2 Auxiliary Power Supply

The auxiliary power supply provides a voltage-controlled current source for parallel operation with the multiple-output power supply. This single-output switching power supply receives the same ac input power as the multiple output power supply. The auxiliary power supply output is connected in parallel with the 5-volt output from the multiple-output power supply so that the output voltage level remains the same, but the output current level is increased. Output from the auxiliary power supply alone is 5.1 volts dc + 1% at 27 amperes maximum. The multiple-output and auxiliary supplies connected in parallel produce up to 72 amperes of current at 5 volts.

1.3.3 Cooling Fans

The system employs three fans to provide cooling by circulating air over the power supplies and the card cage. When fully configured, the system can dissipate 2500

BTU per hour (725 watts) during operation. To allow for adequate cooling, the system positioning or surroundings must not prevent the natural flow of air. The card cage access door on top of the system must also remain closed then the system is turned on. The exhaust fans are located on the rear of the system and are connected so that they run when ac power is applied.

1.3.4 Keyboard

The keyboard provides the operator interface for entering data and control commands to the system (see Figure 1-3). This keyboard employs a standard typewriter key arrangement with additional keys for computer operation. The additional keys include an 11-key edit pad on the right, eight programmable function keys across the top that work with the CRT menu display, five additional function keys that are user defined and a BREAK key. The BREAK key allows the user to regain control of the system.

Circuits contained on the keyboard provide buffering for up to eight sequential keystrokes, and 24 additional buffers are provided by software. The CPIO board processes all keyboard input.

1.3.5 CRT Subsystem

The CRT subsystem provides a 12-inch raster scan-type monitor display with a 15.5KHz horizontal scan. The display is 80 characters wide, and is divided by software into two partitions. An upper 25 partition provides a scrolling feature so that, when the partition is full, new data is entered on the bottom line. Previous data then moves up and the top line is lost from the display. Data cannot be scrolled backwards. The lower 2 line partition is fixed and not influenced by the scrolling partition. This fixed partition is controlled by software to provide a menu for system operation. The menu works with the eight function keys (soft keys) across the top of the keyboard. There is no visual separation between the upper and lower partitions.

Characters in either partition can be displayed, through software control, with the following attributes: Overline (not underline), reverse video, blink and highlight. The cursor appears as a non-blinking reverse video rectangle, occupying the position where the next character will appear. As each new character is displayed, the cursor moves one position to the right until the 80th character is entered. The cursor does not wrap-around, but remains in the last position on top of the last character displayed. The cursor will not appear if it is in the same location as an attribute character.

Pressing the keyboard RETURN key causes the cursor to move to the first character position at the left of the display and also to move downward to the next line. Pressing the keyboard LINE FEED key also moves the cursor down one line , but the cursor remains in the same horizontal position. If the cursor is on the last line of the scrolling partition, pressing the RETURN or LINE FEED keys causes all characters in the partition to move up one line; the top line is then lost and the bottom line is blank.

A normal display is light characters on a dark background, and reverse video is dark characters on a light background. There is no background separation between character lines.

1.3.6 Floppy Disk Drive

The system contains either two 5¼-inch floppy disk drives or one 5¼-inch Winchester drive and one 5¼-inch floppy drive. The double-sided, double-density floppy diskettes

with 80 tracks per side, provide 638K of formatted storage. The soft sectored floppy drive records in Modified Frequency Modulation (MFM) with FM track 0 side 0.

Diskettes are inserted and removed through the front of the disk drives. A latch on the front of the disk drives is lifted (opened) to insert or remove diskettes, and when a diskette is inserted, the latch is pressed down (closed) to lock the diskette on the spindle and position (load) the read and write heads. Do not apply or remove power to or from the system when diskettes are in the drives. Drive 0 is normally the drive on the right-hand side and drive 1 is normally on the left-hand side.

The 5¼-inch (mini-floppy) diskettes are normally write enabled so that data can be transferred to the diskette. To prevent writing over existing files, a tab must be installed over the write enable slot on the side of the diskette . Always insert diskettes with the label facing upward, the write enable slot to the left, and the read/write slot to the back of the drive.

1.3.7 Winchester Disk Drive (Option)

A Winchester disk drive optionally replaces the left-hand floppy disk drive. This 10 Mbyte (formatted storage) drive records MFM. This drive, which spins at 3600 RPM has 2 double-sided, metal oxide coated platters. Four heads access the platters and transfer data at 5 Mbytes/sec. The Winchester does not need to be unlocked for regular operation. The heads are protected automatically at "Power-on and Power-off".

1.3.8 Central Processor and I/O

The Central Processor and I/O (CPIO) board interfaces the following I/O devices:

- Keyboard
- CRT Monitor
- Floppy Disk Drives
- Line Printer (Centronix parallel type)
- Serial Channel 1 (RS232 and CCITT Rec V24)

This single board computer also provides a 5MHz co-processor cluster that contains an 8088 microprocessor, an 8089 I/O processor, 64K of two-ported RAM, up to 32K of PROM/ROM, an interrupt subsystem with three 8259A programmable interrupt controllers, and a general purpose timer with an 8253 programmable interval timer. Since the CPIO is a bus master (able to control access to the Multibus backplane) in a system that can use more than one bus master, an on-board 8289A bus arbiter resolves bus access conflict. The CPIO also supports the functions performed by the IEU board.

1.3.9 ISIS Execution Unit

The ISIS Execution Unit (IEU) board, a standard feature in system configurations, supports ISIS operating system application environments. This allows the system to provide a compatible code execution environment for previous users o f the ISIS operating system. The IEU board also supports a serial I/O channel (Channel 2) that is compatible with the RS232 specification and CCITT Recommendation V24.

The CPU for the IEU board, a 5 MHz 8085A microprocessor, is supported by 64K of two-ported RAM, an interrupt subsystem with two 8259A programmable interrupt controllers, and a general purpose timer with an 8253 programmable interval timer. To support its operational environment, the IEU board depends upon the assistance from the CPIO board.

1.3.10 SPU Unit (Option)

The Slave Processor Unit (SPU), a single board computer that can be added to the system, provides greater computing power. The board provides an 8086 microprocessor, operating at 8MHz. The processors are supported with 128K of two-ported RAM and up to 64K of PROM/ROM, an interrupt system with two 8259A programmable interrupt controllers, and a general purpose timer with an 8253 programmable interrupt timer. Since the SPU can also function as a bus master, an on-board 8289 bus arbiter resolves bus conflicts with other bus masters.

The SPU also contains an 8206 Error Detection and Correction Unit (ECC) that works with the on-board RAM. This ECC provides greater memory system reliability by detecting and correcting all single-bit errors and detecting all double-bit and most multiple-bit errors.

1.4 System Configuration

The system configuration depends upon the boards contained in the card cage, the combination of disk drives and whether the system is used as standalone or as a communication network workstation. The standard configuration for a standalone system provides a CPIO board, an iSBC 056 memory board and an IEU board. By adding boards, the system can accommodate a variety of applications. Computing power for the standard system is increased by adding an SPU board. In addition to the 12-inch by 12-inch boards, the remaining seven slots in the card cage can contain expansion memory boards, network communications boards, disk drive controller boards and In-Circuit Emulator (ICE) boards. Table 1-1 lists typical system configurations and indicates required and optional boards that make up a particular system configuration.

The Series IV software (operating system) is designed to operate within a one megabyte boundary. There is therefore a limit to the amount of functional RAM that can be added to the system. Before adding additional RAM, calculate existing system memory and install optional memory not to exceed one megabyte total system memory. Figure 1-4 shows system memory allocation before adding optional memory. Optional memory may be added to the Series IV, above page 6 (6000:FFFF) on the standard system and above page 9 (9000:FFFF), with the iMDX-434 option. The IEU board must occupy the top-most page of memory (See Figure 1-4). Memory may be added to the system, provided the IEU is not pushed above page D (D000:FFFF).

Where external Winchester drives are used, they are contained in an external Peripheral Chassis. For installation and information on the Peripheral Chassis and the associated controller board, refer to Appendix D.

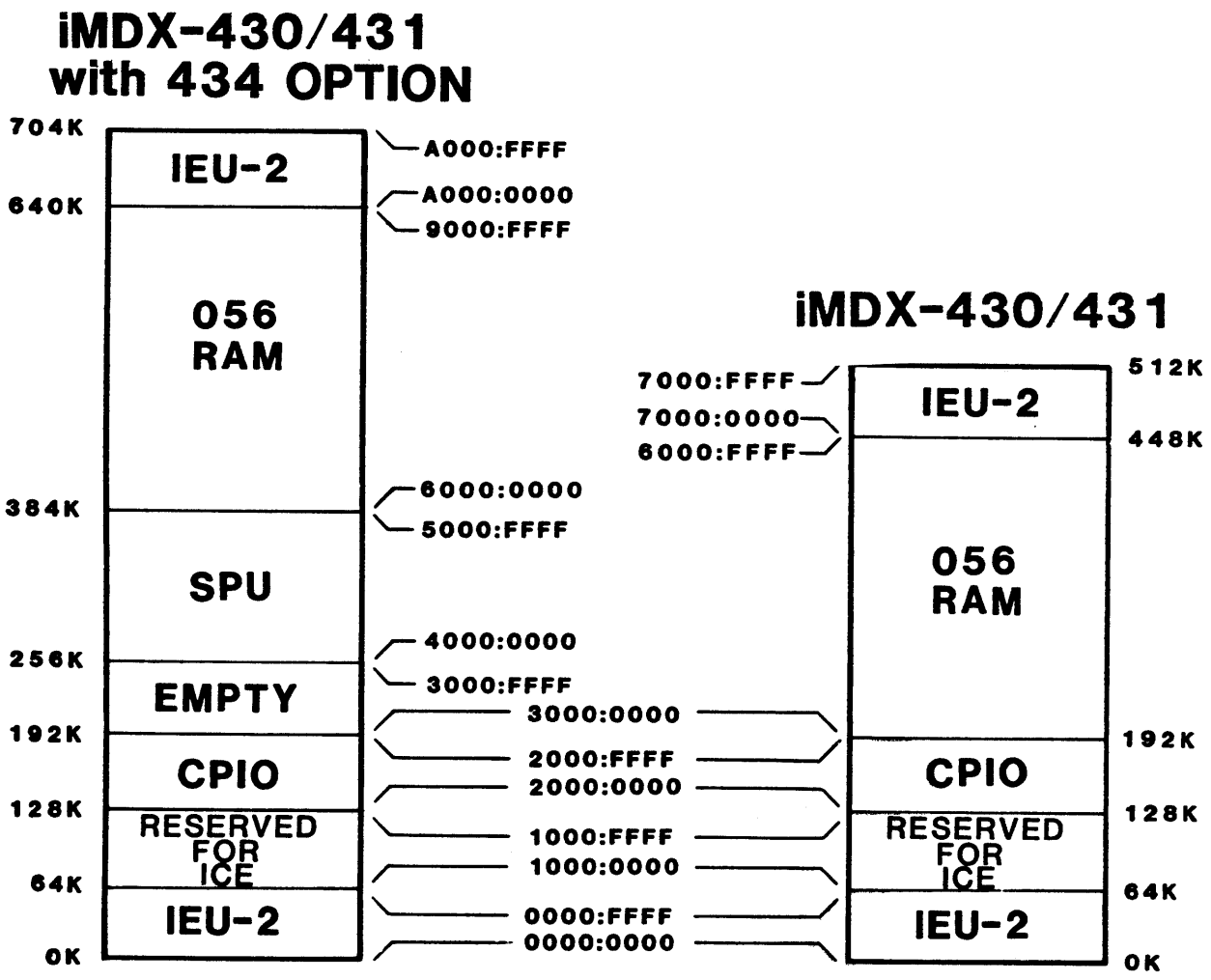


Figure 1-4. Series IV, System Memory Allocation

Some configurations of options may not be possible due to excessive current drain on the system power supplies. Refer to Tables 1-3 and 1-4 and verify that the power usage of the selected configuration does not exceed total power supply current output.

1.5 System Bus Architecture

The system bus architecture is designed such that the SPU, IEU and the CPIO all have their unique local memory and yet all can access the Multibus interface. The CPIO and the SPU can also access any Multibus memory. However, the IEU, because of the limited 16-bit addressing, can not address any other memory outside it's own local 64K. It can, however, address system I/O.

The memory is dual-port access, in that it is local memory to the resident CPU(s) and system memory to the other boards (except the IEU) CPUs. The address lines are multiplexed between local and Multibus interface access.

1.6 System Memory Allocation

The system memory is referenced by multiple processors on the CPIO board (8088) and the optional SPU board (8086). The 8088 and 8086 microprocessors will both address one megabyte (20-bit addressing). All three processors, address the majority of memory at common addresses. Since the 8085 does not have segment registers, any address it passes as data to and from the CPIO board will have an implied segment address the same as the 8088, For compatability with existing 8085 resident applications that communicate with the Multibus backplane, IEU memory is aliased at address 0K thru 63K. This is apparent only to the 8085 processor.

Actually, a small portion of common memory is reserved and can not be shared. The lowest 1K is reserved for interrupt vectors and the top 16K (992 to 1024K) of CPIO and SPU on board memory is the PROM (ROM) memory for each board. Expansion memory must be contiguous to both the CPIO and SPU processors. Refer to Figure 1-4.

1.7 Specifications

Table 1-2 lists the relevant specifications for the system. Additional power supply information is provided in Tables 1-3 and 1-4 for standard system and optional board current demands.

Table 1-1. Series IV, Typical Systems Configurations

System	Description
iMDX430	• CPIO Processor • IEU ISIS Processor • iSBC056 RAM Board (256 KB) • 2 - 5¼″ Floppy Disk Drives
iMDX431	• CPIO Processor • IEU ISIS Processor • iSBC056 RAM Board (256KB) • iSBC215D 5¼″ Winchester Controller • 5¼″ Winchester Drive and iSBC213 Data Separator (under Winchester drive) • 5¼″ Floppy Disk Drive
Options	**Description**
Extended Processing	iMDX434 Upgrade kit (SPU Processor and software)
Workstation	iMDX456 Upgrade Kit (Ethernet Communications to the NDS-2 Network)
Peripheral Chassis	• 35 MB Winchester Drive and iSBC215B Controller
Hard Disk	Model 740/743 and iSBC206 Controller
8″ Floppy Disk Drive	Such as Intel 720 (User Supplied) for COPY only
ICE	In Circuit Emulator board and board sets may be added by the user

Table 1-2. Series IV, Development System Specifications

Physical Characteristics	
Mainframe	Width: 26.5 in. (67.31cm) Height: 16.5 in. (41.91cm) Depth: 18.5 in. (46.99cm) Weight: 66 lbs. (29.24kg)
Keyboard	Width: 20.0 in. (50.8cm) Height: 3.0 in. (7.62cm) Depth: 8.0 in. (20.32cm) Weight: 7.0 lbs.(3.17kg)
AC Input Power Requirements	
Standard: Optional:	8.5A @ 85/170 Vac 4.25A @ 170/264 Vac 47 to 64 Hz
Environmental Characteristics	
Operating Temperature: Relative Humidity:	50° to 104° F (0° to 40° C) 5% to 90% without condensation
Power Supply Characteristics	
Available Outputs:	+5.1 ±1% (2), +12 ±5% (2), -12 ± 5%, -10 ± 5%
Current Capacity:	Refer to Table 1-3
Integral Floppy Disk Drive Characteristics	
Number of Drives:	One or Two
Drive Type:	5¼″, double-sided, double-density
Tracks per side:	80
Sector Size:	512 bytes
Storage Capacity:	638 Kbytes formatted
Media Type:	Dysan 204/2D or equivalent (certified)
Rotational Speed:	300 rpm ± 1.5%
Recording Mode:	MFM (Modified Frequency Modulation) FM (Track 0)
Data Transfer Rate:	250K bits per second
Access Time:	10 ms maximum
Head Settling Time:	15.0 ms maximum
Power-up Delay:	0.5 seconds maximum
Integral Winchester Disk Drive Characteristics	
Rotational Speed:	3600 rpm ± 0.1%
Storage Capacity:	12.76 Megabytes unformatted
Cylinders:	306
Tracks:	1224
Sector Size:	512 bytes
Power-up Time:	30 sec.
Head Settling Time:	15 ms.
Track Access:	3 ms.
Data Transfer Rate:	5 Mbits/sec.
R/W Heads:	4
Disks:	2
Encoding Method:	MFM
Display Characteristics	
CRT Screen Size:	12 inches (30.48 cm) measured diagonally
Display Color:	Green (P42 phosphor)
Display Size:	6″ × 8.25″ both ±.125 @ 12VDC 15.24cm × 20.95cm both ±.3cm @ 12VDC
Character Size:	6 x 9 pixels (8 x 12 template)
Characters per Line:	80
Number of Lines:	25
Display Partitions (software):	Two:Bottom two lines non-scrolling

Table 1-2. Series IV, Development System Specifications (Cont'd.)

Display Modes:	Five:Normal video, intensified video overline (not underline), reverse video and blink
Horizontal Scan Frequency:	19.61KHz
Vertical Scan Frequency:	60Hz 110Vac; 50Hz 220Vac
Horizontal Blanking/Retrace Time:	11 micro Sec.
Vertical Blanking/Retrace Time:	1.22ms (60Hz) or 2.45ms (50Hz)
Keyboard Characteristics	
Buffer Size:	Eight Characters
Mode:	Asynchronous
Baud Rate:	300
Scan:	Each key sensed every 12.5 ms max.
Data Transfer:	Bit serial; 10-bit frame; 1 start bit 1 stop bit, and 8 data bits
Card Cage Characteristics	
Number of Slots:	10
Card Size:	Three 12″ x 12′;′ (30.48cm x 30.48cm) and seven 6.75″ x 12″ (18.63 x 30.48cm)
Architecture:	Multibus backplane (IEEE Standard P796 compatible)
Bus Priority Slots:	Priority 1 thru 10 fixed, non-rotating (see Figure 4-1)
CPIO Board Characteristics	
Board Size:	12″ x 12″ (30.48 x 30.48cm)
Processor:	8088 and 8089 co-processor cluster operating at 5MHz
RAM:	64KB two-ported
PROM/ROM:	32KB
Bus Clock Rate:	9.8304MHz
Interrupt Levels:	System, local master and local slave
Serial Channel (No. 1):	Dedicated to :TI: :TO: at 300 Baud
Line Printer Channel:	Centronics parallel interface
SPU Board Characteristics	
Board Size:	12″ x 12″ (30.48 x 30.48cm)
Processor: 8086 operating at 8MHz	RAM:
128KB two-ported with Error Correction Unit (ECC)	PROM/ROM:
Up to 64KB	Interrupt Levels:
15	
IEU Board Characteristics	
Board Size:	12″ x 12″ (30.48 by 30.48 cm.)
Processor:	8085A
RAM:	64KB two-ported
ROM:	none
Interrupt Types:	Two: system and local
Serial Channel 2:	8253-8251A Programmable Interface
Baud Rate:	64K with Ext. Clock (synchronous)
Type:	RS232 and CCITT Rec. V24 compatible

Table 1-3. Series IV, Standard System Power Supply Loading

	Power Supply Outputs				
Assembly	+5.1Vdc	+12Vdc	+12Vdc	-10Vdc	-12Vdc
Power Supply Capacity (Maximum Amps)					
Multiple-Output Power Supply	45A	5.00A	3.00A	0.50A	2.00A
Auxiliary Power Supply	25A	—	—	—	—
Total Available Current	70A	5.00A	3.00A	0.50A	2.00A
Maximum Current Demand iMDX430 (Amps)					
CRT Display	—	—	1.50A	—	—
Keyboard	0.50A	—	—	—	—
Floppy Disk Drives (2)	1.40A	1.10A	—	—	—
CPIO Board	12.06A	—	0.25A	—	0.10A
IEU Board	6.82A	—	0.50A	—	0.50A
iSBC 056 256K RAM Board	4.80A	0.015A	—	—	—
Total Current Drain	25.58A	1.115A	2.25A	—	0.60A
Available for Options	49.42A	#	0.75A	0.5A	1.40A
Maximum Current Demand iMDX431 (Amps)					
CRT Display	—	—	1.50A	—	—
Keyboard	0.50A	—	—	—	—
Winchester and Floppy Drives	3.50A	2.80A	—	—	—
CPIO Board	12.06A	—	0.25A	—	0.10A
IEU Board	6.82A	—	0.50A	—	0.50A
iSBC 056 256K RAM Board	4.80A	0.015A	—	—	—
Total Current Drain	27.68A	2.815A	2.25A	0.0A	0.60A
Available for Options	47.32A	#	0.75A	0.5A	1.40A

NOTE:

Not Available

For optional device current demand refer to Table 1-4.

Table 1-4. Series IV, Optional Device Maximum Current Demand

	Power Supply			
Assembly	+5.1Vdc	+12Vdc	−10Vdc	−12Vdc
SPU Board	13.2A	0.025A	—	0.023A
iSBC 550 Communication Board Set	9.55A	0.50A	—	—
iSBC 215 Winchester Disk Controller	5.05A	—	—	—
iSBC 218 Streaming Tape Controller	5.05A	—	—	—
@ 206 Hard Disk Controller	8.14A	—	—	—
ICE 41A Emulator Board Set	8.91A	0.07A	—	—
ICE 49 Emulator Board Set	10.72A	0.07A	—	—
ICE 51 Emulator Board Set	15.47A	0.07A	—	—
ICE 85 Emulator Board Set	19.30A	0.07A	—	—
ICE 86 Emulator Board Set	21.43A	0.07A	—	—
ICE 88 Emulator Board Set	19.62A	0.07A	—	—
Multi-ICE (85+85) Emulator Board Sets	38.60A	0.14A	—	—

NOTE:

@ The iSBC 206 Hard Disk Controller is user supplied.

CHAPTER 2
INSTALLATION

2.1 Introduction

This chapter provides pre-installation requirements and the installation procedure used to prepare the system for operation.

2.2 Installation Procedure

Refer to Figure 2-1 for a user guide through the installation procedure. Check off each box as you finish each process.

Assure proper installation and checkout of the Series IV by:

1. Preparing the system site (see Paragraph 2.3).
2. Unpacking the system and inspecting for damage (see Paragraph 2.4).
3. Setting up the system (see Paragraphs 2.5 and 3.1 3.10).
4. Powering up the system (see Paragraph 3.14).
5. Running the Confidence Tests (see Paragraphs 3.15, 3.16 and 3.17).
6. Installing and verifying options (see Chapter 4).
7. Loading the system software (see Paragraph 2.8)

2.3 Site Preparation

The physical characteristics (width, height, depth and weight) of the system are given in Table 1-2. Ensure that the work area (bench, table desk or other structure) accommodates and supports the system mainframe and keyboard. The system requires a height clearance of at least 25.5 inches (65 centimeters).

CAUTION

Allow a minimum clearance of 6 inches (15.25 centimeters) around the system to provide air flow for system cooling. Failure to provide adequate air flow may cause overheating an d damage to sensitive electronic parts.

A three conductor power cable supplies ac line power from the source (power outlet) to the system. The round pin makes a ground connection between any equipment plugged into the ac line for safety. Never use adapters to defeat the safety ground, but have a qualified electrician rewire the electrical system with a safety ground conductor.

2.4 Unpacking Instructions and Inspection

2.4.1 Incoming Inspection

Inspect the exterior of the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is damaged or water stained, request that the carrier's agent be present when the equipment is unpacked. If the

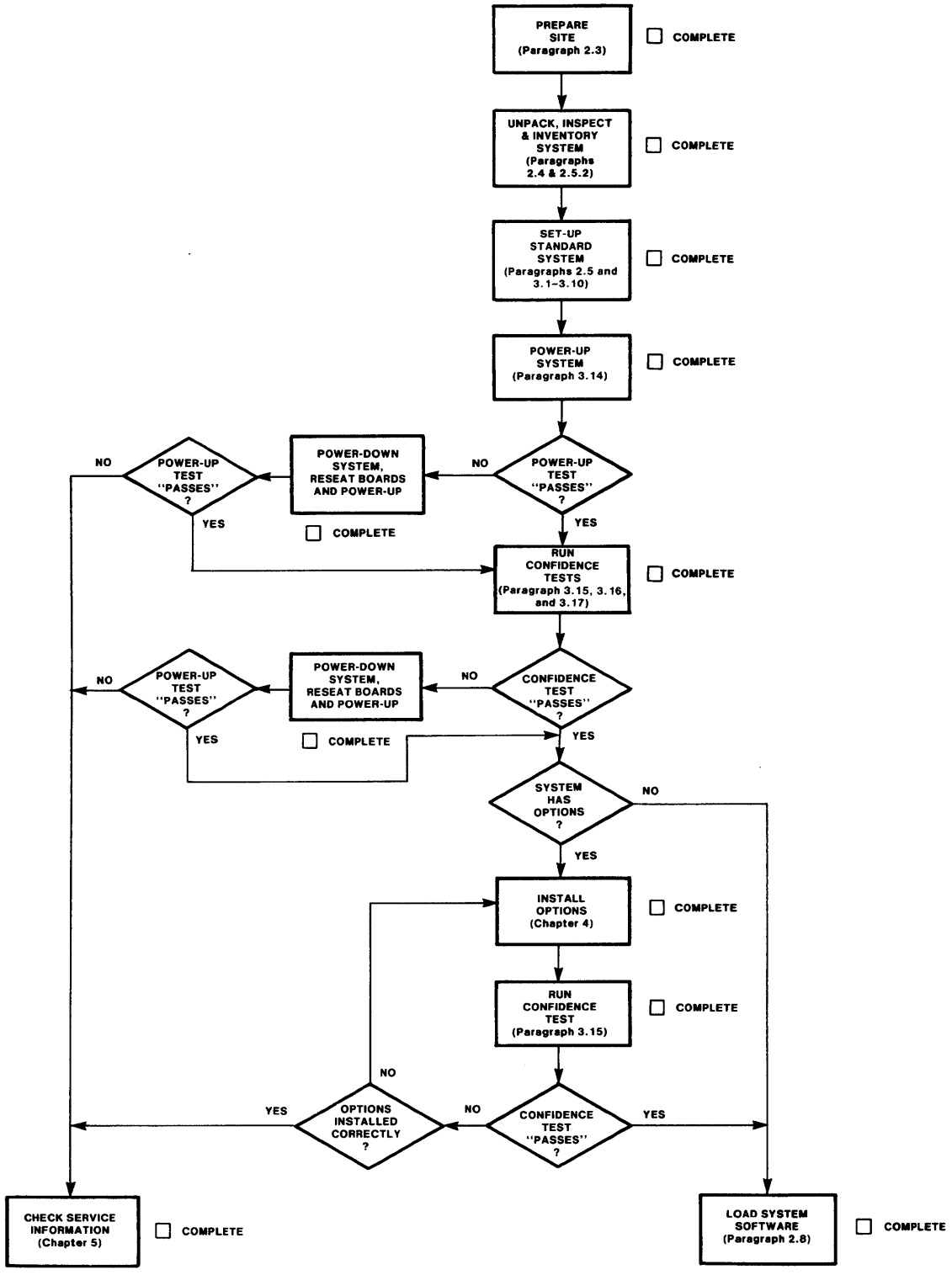


Figure 2-1. Series IV, Installation Procedure

carrier's agent is not present, and the equipment is damaged, keep the carton and packing material for the agents inspection.

For repairs to equipment damaged in shipment, contact Intel Technical Service Center to obtain a Return Authorization Number and further instructions. (Refer to Paragraph 5.5). A purchase order will be required to complete the repair . A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be reshipped.

2.4.2 Unpacking Procedure

Figures 2-2 and 2-3 show the system packed in one of two approved methods (Procedure "A" or "B"). Identify the packing illustration that reflects the method used to pack your system and referring to the illustration, proceed as follows:

WARNING

The packed system weighs approximately 89 pounds (40.37 kilograms). To prevent injury, always use two people to lift or move the system.

1. Remove the accessory kit envelope and set it aside for use when installing options.
2. Lift the keyboard and packing material from the top of the system. Separate the keyboard from the packing material and place the keyboard aside until the mainframe is in place.
3. Use two people to lift the system mainframe onto the work area.
4. Remove the tape used to retain the mainframe top door and disk drive bezel during shipment.
5. Finish the installation by referring to Paragraph 2.5 (System Set-up) and con tinuing through the installation procedure.

Paragraph 2.5 should be followed with the standard configuration of the system (see Table 1-1). After you verify the standard system, install the options. This procedure identifies if you have problems with your system and whether that problem is with the standard configuration or options.

NOTE

The shipping carton contains an accessory kit (part no. 124480) with a download cable and auxiliary connectors. These parts are not used in this pro cedure, but are explained in "Installing Options" (Chapter 4).

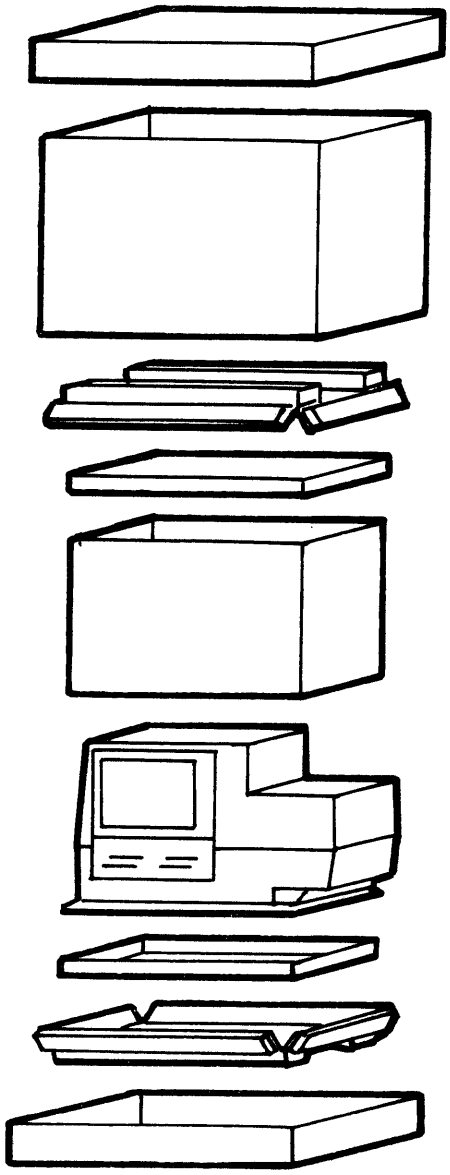


Figure 2-2. Series IV, Unpacking Procedure "A"

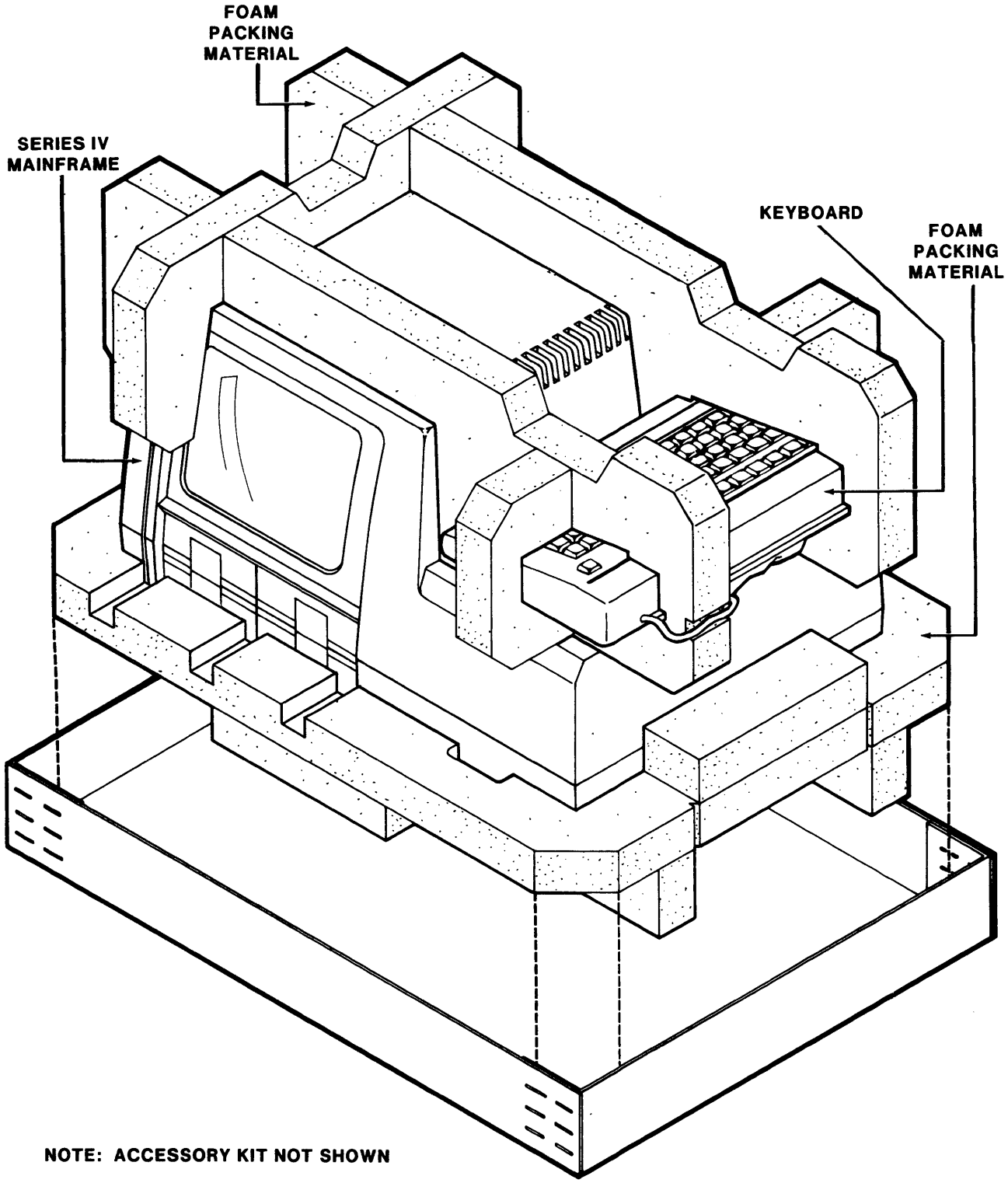


Figure 2-3. Series IV, Unpacking Procedure "B"

WARNING

The unpacked system weighs approximately 70 pounds (31.75 kilograms). To prevent injury, always use two people to lift or move the system.

2.5 System Set-Up

Set-up the system as follows:

1. Connect the plug on the keyboard cable to the mainframe keyboard connector (see Figure 3-1). Fasten the connector to the mainframe with its two captive, slothead screws.
2. Arrange the system in its working position. Usually the keyboard sits in front of the disk drives.
3. After assuring that the circuit is in the "OFF" position, connect the power cord connector to a three-conductor power outlet and turn on the circuit breaker switch.

2.5.1 System Options

Table 1-1 lists all options for the Series IV. Refer to Paragraph 2.5.2 for the board positioning of various system options in the card cage. The approved options to the Series IV are:

- iMDX434 Enhanced Performance Option (customer installable)
- 5¼-inch Winchester in place of the left hand 5¼-inch floppy disk drive.
- External Peripheral Chassis (8″ Winchester Disk Drive)
- 740 Hard Disk
- Network Communications
- In-Circuit Emulation
- Centronics Parallel Type Printer (Customer Supplied)
- 8″ Floppy Disk Drive (ICOPY)
- PROM Programming

2.5.2 System Configuration

Section 1-4, System Configuration, identifies standard and optional boards and peripherals required for each system configuration. Inventory the standard PCBs contained in the system and the optional PCBs sent in separate boxes against the boards required for your system as listed in Table 1-1. Identify the boards by comparing them to the illustrations in Chapters 4.

Notify your Intel sales representative of any shortages.

2.5.3 Board Configuration

The standard iMDX 430/431 system boards are shipped appropriately configured. The addition of the iMDX434 Extended Processing option requires rejumpering the IEU and the iSBC 056 boards. Section 4-10 illustrates this jumper reconfiguration of the PCBs.

The installation of options, other than the SPU and ICE to the Series IV are tech nically complex procedures. These options should be installed by an authorized Intel Customer Service Engineer.

2.5.4 Board Installation

Positioning of the boards in the card cage is critical. Each board must be installed in a unique position for each system configuration. Four boards CPIO, IEU, SPU and iSBC056 occupy permanent positions, slots 1 through 4 (J10–J7), and will not change with optional system configurations. The other optional boards occupy different slots, depending upon the system configuration. Figure 4-2 shows the placement of each board in the card cage for it's respective system configuration.

After determining the proper board locations (Figure 4-2), insert the board into the appropriate slot by lowering it until it touches the connector. After determining that the board is aligned in the PCB guides and meets the connector properly, firmly push the board into the connector until it securely seats. Connect all appropriate external cables, as required, to the seated board.

2.5.5 Peripherals

2.5.5.1 Peripheral Chassis

Appendix D explains the installation and checkout of the Peripheral Chassis (P-Box) option.

2.5.5.2 NRM and 740 Hard Disk Drive

Appendix E explains the installation and checkout of the NRM and the 740 Hard Disk Drive options.

2.5.5.3 Centronics Printer

The Series IV interfaces to a Centronics Parallel Type Printer through the Line Printer connector on the back panel (Figure 1-2). The printer interface table (Table 2-1) defines each printer signal on the Line Printer connector.

This interface requires Cable No. 125705-003. It is suggested that a copy of Centronics Specification No. C332-44 Rev. A, be obtained before attempting an interface of the printer.

2.6 Power-Up Test

Every time the system is turned on or reset, board resident firmware automatically performs a subsystem and board test. This test, although not as thorough as the confidence test, assures the user, with a high degree of confidence, that his system performs correctly. This test is not foolproof and is not a substitute for the Customer Confidence test. The power-up test is described in more detail in Section 3.11.

2.7 Customer Confidence Test

The Customer Confidence Test, the optimum verifier of the system, resides on a separate enclosed diskette. The diskette, titled *Series IV Supplemental Level Diagnostic,* is included as part of the system. This diagnostic test should be performed anytime the system is changed, repaired, moved or when a malfunction is suspected to assure proper operation. The Customer Confidence Test is described in more detail in Section 3.16.

2.8 Loading System Software

The system software may be loaded into the system when the Customer Confidence Test has run error free. Refer to the *Series IV Programmer's and User's Guide,* enclosed in the literature kit, for operating system loading instructions.

Table 2-1. Series IV, Centronics Printer Interface

Pin #	Description	Centronics Signal Name
1	Line Printer Data Bit 0	LPDATA0
2	1	LPDATA1
3	2	LPDATA2
4	3	LPDATA3
5	4	LPDATA4
6	5	LPDATA5
7	6	LPDATA6
8	Line Printer Data Bit 7	LPDATA7
9	Logic Ground	GND
10	Logic Ground	GND
11	Logic Ground	GND
12	Logic Ground	GND
13	Fault	FAULT/
14	Data Strobe	DATA STB/
15	Logic Ground	GND
16	Acknowledge	ACKNLG/

Table 2-1. Series IV, Centronics Printer Interface (Cont'd.)

Pin #	Description	Centronics Signal Name
17	Busy	BUSY
18	Logic Ground	GND
19	Prime (Reset)	PRIME/
20	No Connection	—
21	Logic Ground	GND
22	Select/	SELECT/
23	Logic Ground	GND
24	+ 5 Volts dc*	5VDC
25	Chassis Ground*	CHASSIS GND/

* These wires are not in the cable

/ Active Low Signal

Printer Connection is Centronics Parallel Type

See Centronics Specification C332-44 Rev. A

CHAPTER 3
SYSTEM OPERATION AND VERIFICATION

3.1 Introduction

This chapter contains information about the operators controls, power turn-on, power-up test, and confidence tests. The information in this chapter familiarizes the operator with the system operation and hardware and describes the tests that verify system performance. Power-up tests are performed automatically at power turn-on. The confidence test should be performed during initial system installation, whenever the system configuration is changed by installing options, whenever system malfunctioning is suspected and routinely to verify system performance.

3.2 Operators Controls

The operators primary interface with the system is through the system keyboard, observing the system response displayed on the CRT. There are also several manual controls that control system operation. The following list contains the names and paragraph reference of these manual controls:

1. System Configuration Switches (Paragraph 3-3)
2. Power Circuit Breaker Switch (Paragraph 3-4)
3. Hardware RESET Switch (Paragraph 3-5)
4. CRT Brightness Control (Paragraph 3-7)
5. Drive 0, Drive 1 Latches (Paragraph 3-8)
6. Buzzer (operator programmable) (Paragraph 3-9)

3.3 System Configuration Switches

The system configuration switches (S2-1 thru S2-8), located on the back of the system near the RESET switch (see Figure 3-1) select the power line frequency and the device that contains the boot-up program. Unless the switches are properly set, the system will not boot-up or run correctly. Table 3-1 lists the configuration switch settings and some typical settings are shown in the following examples. In the examples, "0" indicates a switch in the down or OFF position; "1" indicates a switch in the up or ON position; "n" indicates a switch in either position (don't care).

NOTE

Table 3-1 shows the operation of each switch of the eight systems configurations switches. The configuration switches must be set properly for correct system operation.

Table 3-1. Series IV, System Configuration Switch Settings

Switch Numbers								
1	2	3	4	5	6	7	8	
*	n	0	0	0	0	0	0	Skip power-up test and boot system monitor.
*	n	0	0	0	0	1	0	Boot system from integral floppy disk, drive 0.
*	n	0	1	0	0	1	0	Boot system from integral floppy disk, drive 1.
*	n	0	0	0	1	0	0	Boot system from 740 Hard Disk.
*	n	0	0	0	1	1	0	Boot system from external peripheral chassis.
*	n	0	0	1	0	1	0	Boot system from integral Winchester drive.
*	n	0	1	1	0	1	0	Reserved for future configurations.
*	n	0	0	1	1	0	0	Reserved for future configurations.
*	n	0	0	1	1	1	0	Reserved for future configurations.
*	n	0	1	1	1	1	0	Reserved for future configurations.
*	n	#	#	#	#	#	1	Boot workstation from network.
*	n	0	0	1	1	1	1	Reserved (special case)

"0" indicates OFF (down) "1" indicates ON (up) "n" indicates DON'T CARE

NOTES:

Switch 1 (*) selects 50Hz (0) or 60Hz (1). (CRT scan rate only).

Switch 2 (n) is reserved for future configurations.

Switches 3 and 4 select boot device unit addresses.

Switch 5, 6 and 7 select boot device.

Switch 8 selects network communications booting.

= Bit Substitute; i.e., substitute the bit pattern that corresponds to the device from which the Operating System (OS) will be booted by default. (For example, a workstation that uses a 740 hard disk, drive 0 as a defaulted boot device, would require a switch pattern of * n 0 0 0 1 0 1). If network communications are lost, the system will boot to the address of switches 3–7.

1. To select a 60Hz standalone system that boots from the integral floppy disk, drive 0:

1	2	3	4	5	6	7	8	Switch Numbers
1	n	0	0	0	0	1	0	Switch Settings

2. To select a 50Hz standalone system that boots from the integral floppy disk, drive 0:

1	2	3	4	5	6	7	8	Switch Numbers
0	n	0	0	0	0	1	0	Switch Settings

3. To select a 60Hz standalone system that boots from an external peripheral chassis:

1	2	3	4	5	6	7	8	Switch Numbers
1	n	0	0	0	1	1	0	Switch Settings

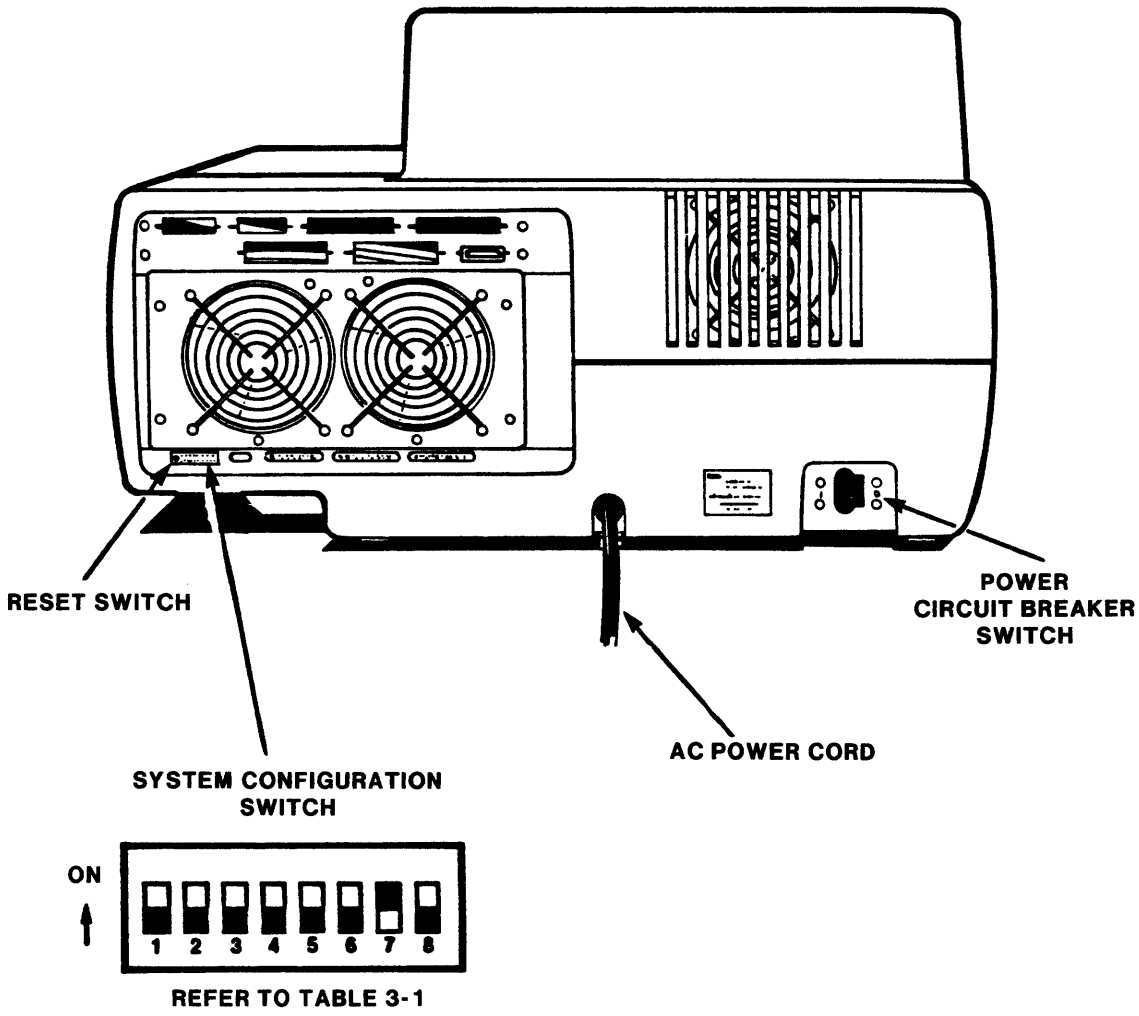


Figure 3-1. Series IV, Systems Control Locations, Rear View

3.4 Power Circuit Breaker Switch

The power circuit breaker switch is located on the back of the system (see Figure 3-1). This switch combines an ON/OFF switch and a circuit breaker for circuit protection against excess current drain. This switch controls application of ac power to the system.

3.5 Hardware Reset Switch

The hardware RESET momentary switch, located on the back of the system (see Figure 3-1), reinitializes the system, to a known set of parameters. The system subsequently reboots, depending upon the configuration and switch settings, and performs the power-up tests.

3.6 Software Restart Key

The RESTART key is reserved for Intel use only.

3.7 CRT Brightness Control

The CRT brightness control, located under the card cage portion of the mainframe and near the front (see Figure 3-2), controls the brightness of the CRT display. The brightness should be adjusted for comfortable viewing, but not so bright as to cause a halo affect on the display.

3.8 Drive 0 and Drive 1 Latches

The integral floppy disk drives have latches and indicators. These latches, located in the front center of the drives, are opened to insert and remove diskettes. The latches are closed, after a diskette is inserted, to lock the diskette in place and enable the drive to respond to program commands. To open a latch, pull outward on the bottom edge, then release. To close a latch, first insert a diskette, with the write enable slot on the left (see Figure 3-3), and then press downward and inward on the latch until it locks in place. An LED indicator, located on the front of each drive, lights when its drive is selected.

3.9 Buzzer

The buzzer provides an audible alarm to the operator when certain programmed functions occur. This audible alarm generally indicates an abnormal condition or a condition that requires the operators attention. The audible alarm alerts the operator that further action is required.

3.10 Power-Up Tests

When ac power is first applied to the system (power-up), or when the hardware RESET switch is pressed, the system automatically performs a self-test (power-up) procedure. The power-up test program is contained in the CPIO board firmware and,

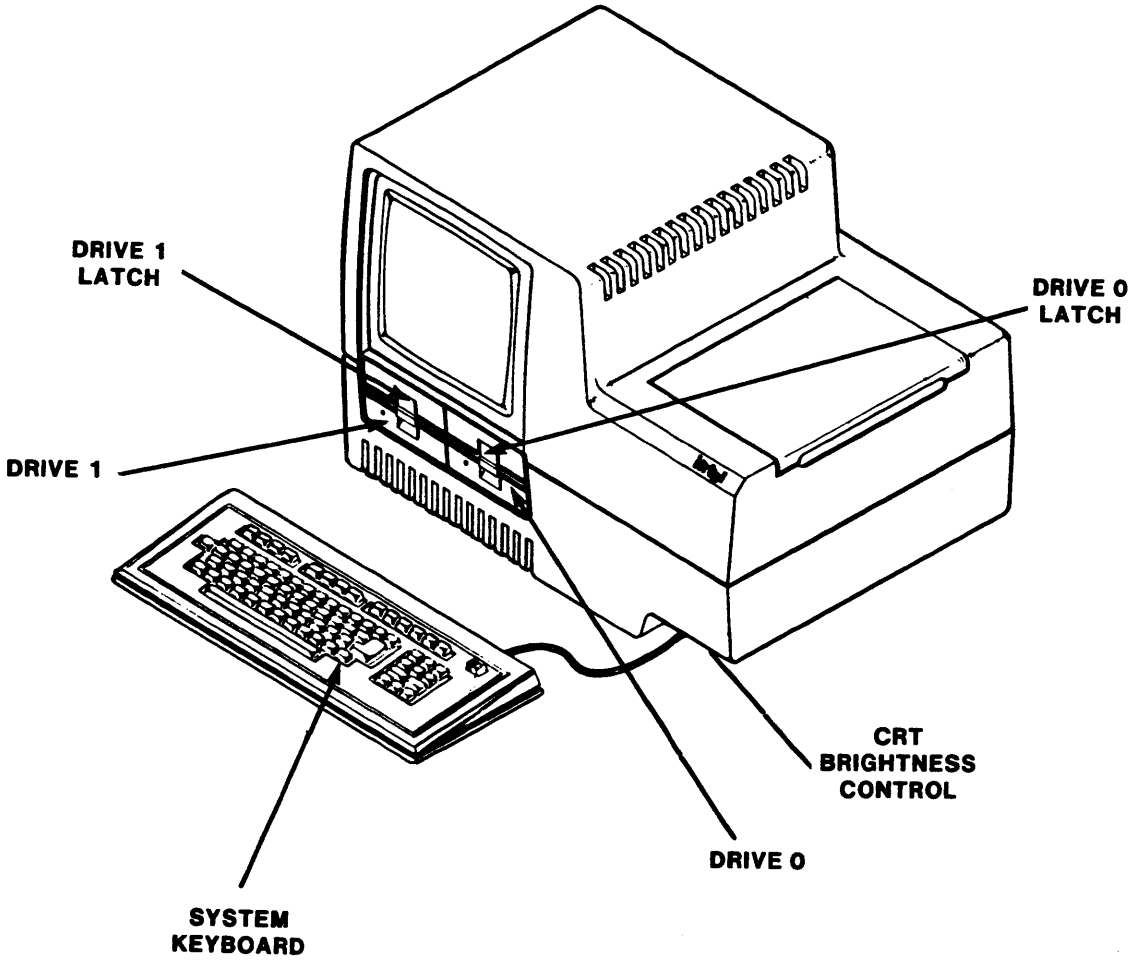
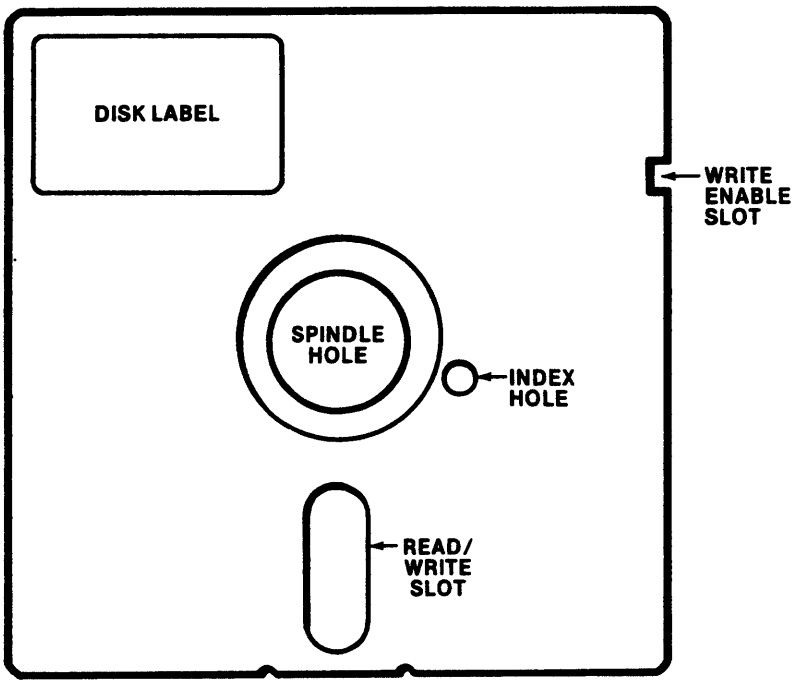


Figure 3-2. Series IV, System Control Locations, Front View



NOTES:

1. **To prevent writing onto a diskette, cover the write enable slot.**
2. **To prevent media damage and subsequent data loss, do not touch the diskette surface in the Read/ Write slot.**

Figure 3-3. Series IV, Floppy Diskette, 5¼-inch

when invoked, executes a go/no-go verification of the CPIO board and keyboard electronics. The test requires approximately 15 seconds to complete. The results are displayed on the CRT. The SPU, if installed, is simultaneously checked by its firmware on power-up. The CPIO obtains the test results and displays them on the CRT.

If an error is detected, the system displays an error code to identify the test that failed (Table 3-2 and 3-3). After displaying the error code, the power-up diagnostics transfers control to the system monitor.

To verify a power-up test failure, press the hardware RESET switch to reinitialize the test. If the failure is repeatable, immediately turn off system power and refer to Chapter 5 for service information.

CAUTION

Do not attempt to operate the system if the power-up test has a repeatable failure. Operating the system may induce errors in programs or damage components.

3.11 CPIO Board Power-Up Test Descriptions

Table 3-2 lists the CPIO board power-up test by test number and provides the test names and a brief description of each test.

3.12 Optional Board Power-Up Tests

Optional boards, such as the SPU board, also perform a firmware-based self-test sequence during power-up. After completing their self-test, and after the CPIO board completes its test, the optional boards report their status to the CPIO board. The CPIO board power-up test reads the information passed from the optional boards and displays the status information on the CRT screen. The optional board status information is displayed in two bytes. The first byte is the optional board identification and the second byte is the number of the test that failed. When no failure occured, the word "PASSED" is displayed and a test number is not displayed.

3.13 Optional SPU Board Power-Up Test Descriptions

Table 3-3 lists the optional SPU board power-up tests by names and a brief description of each test. All numbers used for the tests and in the test descriptions are hexadecimal (H) unless otherwise specified.

3.14 Power-Up Procedures

The power-up procedures describe how to properly apply power to the system and observe performance of the power-up tests. Power-up procedures are performed when the system is initially installed (refer to Chapter 2) to ensure that the system functions properly. This initial power-up should be performed before any optional devices are installed and again after any options are installed to ensure that system performance has not been affected. Finally, power-up procedures are performed whenever power is applied to the system to ensure that the system is set up and initialized properly.

The power-up procedures may vary slightly depending upon the system configuration and application. The following procedure provides the power-up sequence.

To power-up the Series IV:

1. Set the system configuration switches as required to select the ac source frequency, boot device address, boot device and type of system (see Table 3-1). If the selected device does not contain the operating program, or the selected device is not funtional, the system transfers control back to the system monitor.

Table 3-2. Series IV, CPIO Power-up Test

TEST #	TEST NAME	TEST DESCRIPTION
0001H	PROM Checksum	Reads the four PROMs on the CPIO board, computes and verifies the checksum for each PROM.
0002H	Data Bus Ripple	Data is written to a test location in each 16KB memory bank on the CPIO board and data is verified as each data line becomes a logic 1.
0003H	Address Bus Ripple	Writes into CPIO RAM memory while rippling a logic 1 across the address bus. For each test location, the data is read, complemented and read again for verification. Each 16KB memory bank is tested separately.
0004H	CPIO RAM March	Writes a pattern upward through CPIO RAM memory, then complements the pattern and writes the complement downward through memory. After each write, the memory location is read and verified.
0005H	Keyboard Reset	The CPIO board executes a diagnostic test contained in the keyboard firmware. The test includes a RAM/ROM checksum test, FIFO test and matrix short test.
0006H	CRT Subsystem ROM	Executes the CRT programmable interface ROM diagnostic.
0007H	CRT Subsystem RAM	Executes the CRT programmable interface RAM diagnostic.
0008H	CRT Video Counter	Checks the CRT video circuits.
0009H	CPIO 8259A Interrupt	Checks that the programmable interrupt controller mask registers can be read from and written to.
000AH	Line Printer Subsystem	Executes the line printer programmable interface (on the CPIO board) ROM diagnostic.
000BH	Line Printer Subsystem RAM	Executes the line printer programmable interface (on the CPIO board) RAM diagnostic.
000CH	8253 Timer	Checks the counting capability of all three counters on the programmable interval timer and also checks counter 2 interrupt capability.

Before the CPIO finishes its power-up test, it verifies the physical presence of the IEU board.

2. Observe that the ac power cord (Figure 3-2) is properly connected to a three-wire power outlet.

NOTE

If the system has an external Winchester drive, the drive must be powered up and rotating at operating speed before the system power is turned on.

3. Turn ON power circuit breaker switch (back left of system).

NOTE

After power has been removed from the system, the user should not reapply power for 15 seconds.

4. Observe that power is applied to the system (fans running) and the system proceeds through the power-up test. If the system is booting from a floppy disk, the power-up test is controlled by the system monitor. An "Error 3800" message is

normally displayed because the user has boot from a 5¼" floppy drive and a diskette has not yet been inserted in that drive.

(example of "Error 3800" display)

```
SIV BOOT Vx.y
Mini-floppy dr 0
- device failure
Error 3800
Attempt to reboot from: MON88
SERIES IV CPIO MONITOR Vx.y
```

5. Turn on power to any connected peripherals such as line printers or non system disk drives (if applicable).

3.15 Boot Loading the System

The following instructions explain how to boot the system. Before the system boots, it performs a power-up test.

Table 3-3. Series IV, SPU Power-up Test

TEST #	TEST NAME	TEST DESCRIPTION
0001H	PROM Checksum	Generates a checksum of the PROM contents and then verifies that it compares to a stored checksum.
0002H	SPU Data Bus Ripple	The error correction unit is enabled and a logic 1 is rippled across the data bus and verified.
0003H	SPU Address Bus Ripple	The error correction unit is enabled and a pattern is written to all memory locations. The locations are then read and verified, the pattern is complemented, written again and the complemented pattern is then read and verified.
0004H	SPU RAM March	The error correction is enabled and a pattern is written to all locations of the SPU memory. The pattern is then read and verified, complemented, then written, read and verified again.
0005H	ECC Syndrome	Checks operation of the error correction unit by inputting correctable errors and reading and verifying each of the 16 bits.
0006H	Force Uncorrectable Error	Checks operation of the error correction unit by generating a two-bit error and verifying that an uncorrectable error signal results.
0007H	SPU Timer	Checks the counting capability of all three counters on the programmable interval timer.
0008H	SPU FIFO	Writes and verifies 16 different patterns for the FIFO and then repeats the process with the complement patterns.
0009H	SPU Local Interrupt Controller	Generates interrupts and checks that the correct interrupts are issued by the controller.

NOTE

Steps 1 and 2 are applicable only if the system is booting from an integral floppy disk drive.

To boot the Series IV system:

1. Insert a floppy diskette (5¼-inch) that contains the Supplemental Level Diagnostic (confidence test), order number 133511, into the appropriate floppy disk

drive. Normally, drive 0, on the right-hand side, is selected to boot the diagnostic monitor. Always insert the diskette with the write-enable slot on the left and the read/write slot to the back of the drive (refer to Figure 3-3). The system diskette should be write protected by covering over the write-enable slot.

2. Press the RESET switch (back right of system) to reinitialize the system and boot from the integral floppy disk drive. Observe that the system completes the power-up test (approximately 15 seconds), no error messages are displayed and this sign-on message is displayed:

```
SERIES IV Power-Up Diagnostic, Vx.y
SPU PASSED (only if optional SPU board is installed)
IEU PASSED
SIV Boot Vx.y
Mini-floppy dr 0
Series IV Diagnostic Monitor, Vx.y
```

NOTE

If the sign-on message is not displayed, repeat step 2 twice more. If the system still does not sign on, refer to the service information in Chapter 5.

3. Observe that the system sign on message above is displayed, then proceed to the confidence test or system operation as applicable. The confidence test must be performed following initial installation, following any configuration change, when a system malfunction is suspected and routinely to assure proper operation.

3.16 Confidence Test General Information

The confidence test runs under the control of the CPIO board and provides five unique, dynamic subsystem and peripheral tests called:

1. SIVDIA
2. SIVEXT
3. SIVWIN
4. SIVCOM
5. SIV740

The SIVDIA portion of the confidence test exercises the CPIO and SPU boards, while the SIVEXT portion checks the IEU and extra system memory. SIVWIN and SIV740 test the operation of the integral, and peripheral chassis (Winchesters) and the 740 (hard disk) drives respectively. SIVCOM verifies the systems ethernet communication network.

The remaining paragraphs in this chapter provide the confidence tests operating procedures, descriptions, execution times and error messages. Appendix A to this manual describes and gives examples of the Test MONitor (TMON) commands used to interface the confidence test suite.

All supplemental level diagnostics display error codes or error messages to aid in isolating faults to a replaceable subassembly. The primary factors in isolating failures are the failing test numbers and the total system failure symptoms. Failures are typically caused by faulty printed circuit boards/subassemblies or bad connections

between subassemblies (i.e., oxidation on motherboard connectors, loose cable connector, etc.).

3.17 SIVDIA Confidence Test

3.17.1 Initiating the SIVDIA Confidence Test

At the completion of the power-up test, the SIVDIA portion of the confidence test may be initiated by:

1. Inserting a copy of the Series IV Supplemental Level Diagnostic, Order No. 133511, into the floppy disk drive No. 0 and closing the latch and booting the system (Refer to Section 3.15).
2. Typing "Z" and the test name "SIVDIA" into the system.
3. Activating the TMON monitor by typing a GO command "G".
4. Defining test suite parameters and starting the test procedure. (see Appendix A for TMON commands).

NOTE

Operator entries are shown in reverse video and the <cr> indicates pressing the keyboard RETURN key.

NOTE

To exit a diagnostic test and return to the monitor so that another test may be exercised or testing abandoned altogether, type:

*E X I T <cr>

(Example of initiating SIVDIA)

```
Series IV Diagnostic Monitor, Vx.y
>L O A D S I V D I A <cr>
File SIVDIA loaded
>G <cr>
SERIES IV CPIO, SPU DIAGNOSTIC TEST Vx.y
```

5. Enter the following command to execute tests 0000H to 0003H, 0008H, 0009H, 000BH, 000DH–0014H, (if SPU installed) and 0015H:

*T <cr>

The SIVDIA test suit, now loaded into the system, begins testing the CPIO and SPU boards, and finishes after the tests run one time.

As the system exercises each portion the test results are displayed on the CRT. Figure 3-4 shows the display of the CRT screen if all the SIVDIA tests have passed.

3.17.2 SIVDIA Test Descriptions

Table 3-4 describes the function of each test in the SIVEXT test suite.

```
0004H *** IGNORED ***
0005H *** IGNORED ***
0006H *** IGNORED ***
0007H *** IGNORED ***
000AH *** IGNORED ***
000CH *** IGNORED ***
0000H CPIO CPU TEST                                    ''PASSED''
0001H CPIO 8259A INTERRUPT TEST                        ''PASSED''
0002H CPIO SOFTWARE INTERRUPT TEST                     ''PASSED''
0003H CPIO FAILSAFE TIMER TEST                         ''PASSED''
0008H IEU RAM REFRESH TEST                             ''PASSED''
0009H CPIO RAM REFRESH TEST                            ''PASSED''
000BH FLOPPY DISK SEEK TEST                            ''PASSED''
000DH SPU WAKE UP TEST                                 ''PASSED''
000EH SPU CPU TEST                                     ''PASSED''
000FH NORMAL W/R SPU MEMORY TEST                       ''PASSED''
0010H SPU CHECK BITS MEMORY MARCH TEST                 ''PASSED''
0011H SPU MEMORY REFRESH                               ''PASSED''
0012H SPU MEMORY REFRESH ECC OFF                       ''PASSED''
0013H CPIO WAKE UP                                     ''PASSED''
0014H CPIO FIFO                                        ''PASSED''
0015H CPIO 8089 OPERATION TIME-OUT                     ''PASSED''
*
```

Figure 3-4. Series IV, CRT Display of SIVDIA Confidence Test

Table 3-4. Series IV, SIVDIA Test Descriptions

TEST #	TEST NAME	TEST DESCRIPTION
0000H	8088 CPU	The 8088 microprocessor executes a sequence of assembly language instructions to verify its Arithmetic Logic Unit (ALU).
0001H	CPIO 8259A Interrupt	Generates interrupts and verifies the interrupt vectors to test the three CPIO interrupt controllers.
0002H	8088 Software	Generates and verifies all 256 software interrupts.
0003H	Failsafe Timer (88)	Verifies that the onboard failsafe timer generates an acknowledge signal to the CPU within 10ms of an access to a nonexistent memory or I/O location. **NOTE** Before executing test 0004H, install the lineprinter loopback connector, No. 124270, in jack (J20).

Table 3-4. Series IV, SIVDIA Test Descriptions (Cont'd.)

TEST #	TEST NAME	TEST DESCRIPTION
*0004H	Lineprinter Loopback	Invokes the line printer loopback test resident in the line printer subsystem controller (8741A). The line printer loopback connector must be installed on I/O panel connector 20 to execute this test successfully. **NOTE** Before executing test 0005H, install the USART loopback connector, No. 123314, in serial channel 1.
*0005H	USART	Loopback Sets and verifies Request to Send, Clear to Send, Data Terminal Ready, Data set Ready, Transmitted Data and Received Data functions on the CPIO USART (8251).
*0006H	Reserved	Reserved for the 8087 Numeric Processor test that is to be implemented in the future.
*0007H	Keyboard	Enables a full screen display of each character typed. To advance to the next test, type CONTROL-C (press and hold CONTROL key while pressing the C key).
0008H	IEU RAM Refresh	Writes an FFH to all IEU board RAM memory locations, waits 55 seconds, and then checks for changes in data. Next, the same write, wait and check is performed with complement pattern 00H. If a failure occurs, the failed address and expected versus received values are displayed.
0009H	CPIO RAM Refresh	Same as test 0008H except for CPIO board RAM instead of IEU RAM.
*000AH	CPIO Line Printer	**NOTE** Test 000AH times out and reports PASSED when no line printer is attached to the Series IV. Outputs the ASCII character set to the line printer five times. When a printer is attached, actual pass/fail status is based on visual inspection of the printer's output.
000BH	Floppy Disk Seek	Executes a worst case seek sequence to verify the diskette drive sub system. The user is prompted, on the first pass only, to select the floppy disk drive to be tested.
*000CH	Floppy Disk F/W/R	Formats, writes, and reads random diskette checks to exercise the diskette drive subsystem. The user is prompted, on the first pass only, to insert a blank diskette into the drive before executing this test.
		NOTE Tests 000DH through 0012H verify the optional SPU board. These tests are performed only if an optional SPU board is installed in the system.
000DH	SPU Wake Up	Verifies communication from the CPIO board to the SPU board 8086 microprocessor.
000EH	SPU CPU	The 8086 microprocessor executes a sequence of assembly language instructions to verify that the processor is functioning properly.

Table 3-4. Series IV, SIVDIA Test Descriptions (Cont'd.)

TEST #	TEST NAME	TEST DESCRIPTION
000FH	Normal W/R SPU RAM	Initializes on-board RAM with 00H, verifies the data, writes FFH to RAM, and again verifies the data.
0010H	SPU Check-bits RAM March	Verifies integrity of check RAM by filling check RAM with alternating ones and zeros, verifying the pattern, complementing the pattern, and verifying the new pattern.
0011H	SPU Memory Refresh	Writes data pattern to RAM, waits, and verifies the data pattern.
0012H	SPU RAM March (ECC off)	Writes a data pattern to RAM with Error Correction Unit (ECC) disabled. Verfies the pattern, complements it, and verfies the new pattern.
0013H	CPIO Wake Up	Verifies communication from the SPU board to the CPIO board 8088 microprocessor.
0014H	CPIO FIFO	Checks the CPIO board FIFO control port protocol from the SPU board 8086 microprocessor.
0015H	CPIO 8089 Operation Time-out	This test checks the 8089 Operation Time-out circuit on the CPIO board.

* Ignored at test initialization.

3.17.3 SIVDIA Test Execution Times

Approximate execution times for individual tests or groups of tests are listed in Table 3-5.

Table 3-5. Series IV, SIVDIA Test Execution Time

Test No.	Execution Time
0 to 3	1 second (Combined)
4	ignored
5	ignored
6	ignored
7	ignored
8	15 seconds
9	20 seconds
A	ignored
B	3 minutes
C	ignored
D to F	2 seconds (Combined)

Table 3-5. Series IV, SIVDIA Test Execution Time (Cont'd.)

Test No.	Execution Time
10	10 seconds
11	18 seconds
12	18 seconds
13 to 15	2 seconds (Combined)

3.18 SIVEXT Confidence Test

3.18.1 Initiating the SIVEXT Confidence Test

At the completion of the power-up test, the SIVEXT portion of the confidence test may be initiated by:

1. Inserting a copy of the Series IV Supplemental Level Diagnostic, Order No. 133511, into the floppy disk drive No. 0 and closing the latch and pressing the RESET switch. (Refer to Section 3.15.)
2. Typing "Z" and the test name into the system.
3. Activating the TMON monitor by typing a GO command "G".
4. Defining test suite parameters and starting test procedure. (See Appendix A for TMON commands).

NOTE

Operator entries are shown in reverse video and the <cr> indicates pressing the keyboard RETURN key.

NOTE

To exit a diagnostic test and return to the monitor so that another test may be exercised or testing abandoned altogether, type:

*E X I T <cr>

(Example of initiating SIVEXT)

```
Series IV Diagnostic Monitor x.y
>Z SIVEXT<cr>
File SIVEXT loaded
>G<cr>
SERIES IV IEU, EXTRA RAM DIAGNOSTIC TEST X.Y
```

5. Type the following command to execute tests 0000H - 000CH:

*T<cr>

The SIVEXT test suite, now loaded into the system, begins testing the IEU and extra memory boards, and because of the TEST<cr>, command finishes after the tests run one time.

As the tests exercise the system, the results are displayed on the CRT. Figure 3-5 shows the display of the CRT screen after all the SIVEXT tests have passed.

3.18.2 SIVEXT Test Descriptions

Table 3-6 describes the function of each individual test in the SIVEXT test suite.

```
0007H *** IGNORED ***
000DH *** IGNORED ***
000EH *** IGNORED ***
0000H 8085 RESET                                    ''PASSED''
0001H 8085 CPU                                      ''PASSED''
0002H FIFO CONTROL PORT                             ''PASSED''
0003H IEU 8259A INTERRUPT                           ''PASSED''
0004H FAILSAFE TIMER                                ''PASSED''
0005H TIMER COUNT                                   ''PASSED''
0006H IEU CONTROL PORT                              ''PASSED''
0008H EXTRA RAM DATA BUS RIPPLE                     ''PASSED''
0009H EXTRA RAM ADDRESS BUS RIPPLE                  ''PASSED''
000AH EXTRA RAM MARCH                               ''PASSED''
000BH EXTRA RAM REFRESH                             ''PASSED''
000CH EXTRA RAM ADDRESS                             ''PASSED''
```

Figure 3-5. Series IV, CRT Display of SIVEXT Confidence Test

Table 3-6. Series IV, SIVEXT Test Descriptions

TEST #	TEST NAME	TEST DESCRIPTION
0000H	8085 Reset	Verifies that a RESET disables the IEU board 8085 microprocessor **NOTE** Do not run IEU tests if test 0001H fails.
0001H	8085 CPU	Executes the IEU 8085 microprocessor instruction set and verifies the results. Software interrupts are also tested.
0002H	FIFO Control Port	Checks the IEU board FIFO control port protocol from the CPIO board 8088 microprocessor. FIFO interrupts are also verified.
0003H	IEU 8259A Interrupt	Checks the Multibus interrupts that invoke the IEU 8259A interrupt controller chip. 0004H Failsafe Timer Verifies that the IEU board failsafe timer will time out when it attempts to read a nonexistant I/O port. The program will automatically seek an unused I/O port.
0005H	Timer Count	Synchronizes and compares the values of the three IEU board counters through 1900 values ranging from 0000H to FFFFH. Verifies generation of the interrupt level 2 is also verified when counter 2 reaches its terminal count.
0006H	IEU Control Port	Verifies the following operations of the IEU board bus public control port: Overide (OVRD) Interrupt Interrupt Enable SLAVE LOCK **NOTE** Before executing test 0007H, install the USART loopback connector in Serial Channel 2.

Table 3-6. Series IV, SIVEXT Test Descriptions (Cont'd.)

TEST #	TEST NAME	TEST DESCRIPTION
0007H	USART Loopback	Sets and then verifies the following signals on the IEU USART (8251A): Request to Send, Clear to Send, Data Terminal Ready, Data Set Ready, Transmitted Data and Received Data.
0008H	Extra RAM Data Bus Ripple	A logic 1 is rippled across the data bus and data is written into a test location and verified for each 16KB of memory specified.
0009H	Extra RAM Address Bus Ripple	A 55H is written into RAM while a logic 1 is rippled across the address bus. Data is then read, complemented and read again for verification at each location.
000AH	Extra RAM March	A background pattern (55H) is marched upward through the specified mamory, complemented, marched downward; each time verifying the complemented pattern.
000BH	Extra RAM Refresh	A background pattern (FFH) is written to all locations and, after a 40 second wait, all locations are checked for changes in data. The procedure is then repeated with the complement (00H) pattern.
000CH	Extra RAM Address	The integrity of both low byte and high byte addressing is checked to locate any RAM addressing problems, such as dual addressing on writes.
000DH*	Extra RAM Walk	Each memory bank is tested separately by writing a background pattern (00H) in all locations. An FFH pattern is then written into each location one at a time. As each location is written, the previous location is complemented, and the background data is read to verify data is unchanged. This test is initially ignored and a RECOGNIZE command must be issued before it is performed.
000EH*	Extra RAM Galpat	A pattern of ones and zeros is galloped (written) through each memory bank to check for pattern sensitivity and access problems. This test is initially ignored and a RECOGNIZE command must be issued before it is performed.

* Ignored at test initialization.

3.18.3 SIVEXT Test Execution Times

Table 3-7 shows the approximate execution time of each test in the SIVEXT test suite.

Table 3-7. Series IV, SIVEXT Test Execution Time

Test No.	Execution Time
0 to 6	2 seconds (Combined)
7	ignored
8 to 9	seconds (Combined)
B	40 seconds
C	1 second
D	when recognized (12 hours)
E	when recognized (36 hours)

3.19 SIVWIN Confidence Test

The SIVWIN test suite verifies proper operation of the winchester disk controller board and the peripheral chassis or integral winchester disk drives. The user configures and controls the test through an initialization menu and TMON test commands. The peripheral chassis and integral disk drives are tested separately by choosing either the 8-inch (peripheral), or 5¼-inch (integral) drive in the SIVWIN confidence test menu.

A menu of questions, displayed at test initialization, allows the user to configure the test suite to match the hardware configuration. Individual tests are initialized as either ignored or recognized depending on how the user answers the questions. The menu, and the responses to the questions are described and illustrated in the paragraphs that follow. The test program determines the next question to ask by examining the answer given to the previous questions. The user enters identification values or gives yes/no answers in response to the questions. Identification values consist of one or more decimal digits. Affirmative responses to the yes/no questions are an upper case "Y" or a lower case "y." Negative responses to the yes/no questions are an upper case "N", a lower case "n", or a carriage return.

Answer the menu of questions shown in Paragraphs 3.19.1 and 3.19.2 as follows:

1. Enter correct number to "TYPE OF UNIT BEING TESTED" to select the proper drive.
2. Enter 3 to "TYPE OF SYSTEM", to select the Series IV system environment.
3. Answer YES to "IS UNIT 0 BEING TESTED" to test the first drive in the peripheral attachment.
4. Answer NO to "IS UNIT BACKED UP" question to prohibit execution of tests 15, 16, and 17. Tests 15 and 16 are both destructive tests that require an hour or more to execute. These tests should only be run when you suspect a platter to be defective. Test 17 is a utility routine that formats all selected drives.

NOTE

Tests 15, 16, and/or 17 will not run unless the data on the Winchester drive is backed up.

5. Answer YES to "DO YOU WANT TO USE THE INITIALIZATION DEFAULTS" to select the default test parameter values. Do not respond NO. A NO response is reserved for use by Intel Repair Center personnel.
6. Answer the question, "IS UNIT 1 BEING TESTED" according to system configuration (one or two drives). Answer NO, as the two drive option is not yet available.

7. Answer NO to the last two questions testing drive UNIT 2 and UNIT 3. These drives are not supported in the current Series IV release.
8. Answer YES to DO YOU WANT TO USE THE INITIALIZATION DEFAULTS to select the default test parameter values. Do not respond NO. A NO response is reserved for use by Repair Center personnel.
9. Answer the question, "IS UNIT 1 BEING TESTED" according to system configuration (one or two drives). Answer NO, as the two drive option is not yet available.
10. Answer NO to the last two questions testing drive UNIT 2 and UNIT 3. These drives are not supported in the Series IV release.

NOTE

If an error has been made in a response, the user can back through the menu a question at a time by entering a B on the keyboard. Once a <cr> has been entered for the last question, IS UNIT 3 BEING TESTED, the backup option no longer exists.

3.19.1 Initiating the Integral Winchester SIVWIN Confidence Test

Follow the step-by-step procedures in this paragraph when executing the SIVWIN test suite. Because the system has one drive, tests B, E, 10, 15, 16, and 17 are ignored at initialization. Tests 15, 16, and 17 cannot be run if the drive is not backed up (UNIT BACKED UP question in the initialization menu) and are not recognized.

Load the SIVWIN integral winchester test suite into system memory by:

1. Inserting a copy of the Series IV Supplemental Level Diagnostic, Order No. 133511, into the floppy disk drive No. 0 and closing the latch and pressing the RESET switch (refer to Section 3.15).
2. Typing "Z" and the test name into the system.
3. Activating the TMON monitor by typing a GO command "G".

NOTE

To exit a diagnostic test and return to the monitor so that another test may be exercised or testing abandoned altogether, type:

```
*EXIT<cr>
```

(Example of initiating SIVWIN)

```
Series IV Diagnostic Monitor x.y.
>Z SIVWIN<cr>
File SIVWIN loaded (takes approximately 40
sec.)
>G<cr>
```

Winchester Subsystem Supplemental Test for the Intellec Series IV Development System, Version x.y

4. Type the appropriate response (reverse video) and press the carriage return key <cr> as shown below.

```
TYPE OF UNIT BEING TESTED?
0 = 8 INCH WINCHESTER  1 = 5 1/4-INCH WINCHESTER
- ENTER NUMBER *0<cr>
Which type of system?
```

```
  0 = TPS    1 = DBP    2 = NRM    3 = S-IV
*<cr>
 ALL INITIALIZE NUMBERS MUST BE DECIMAL
IS UNIT 0 BEING TESTED (Y or N) *<cr>
 IS THIS UNIT BACKED UP (Y or N) *<cr>
  DO YOU WANT TO USE THE INITIALIZATION DEFAULTS (Y or
N) *<cr>
    IS UNIT 1 BEING TESTED (Y or N) *<cr>
    IS UNIT 2 BEING TESTED (Y or N) *<cr>
    IS UNIT 3 BEING TESTED (Y or N) *<cr>
    THIS COULD TAKE 1 MINUTE
    PASS
    MDS/VERSION x.y
    CANNOT READ DEFECT INFORMATION
    *
```

5. Enter the following command to execute tests 0000H 000AH and 000FH - 0014H:

   *<cr>

6. The CRT at the SIV will display the messages shown in Figure 3-6 when all tests pass.

3.19.2 Initiating the Peripheral Chassis SIVWIN Confidence Test

The following step-by-step procedures should be used in executing the SIVWIN test suite. Because the system has one drive, tests B, E, 10, 15, 16, and 17 are ignored at initialization. Tests 15, 16, and 17 cannot be run if the drive is not backed up (UNIT BACKED UP question in the initialization menu) and are not recognized. Load the SIVWIN integral winchester test suite into system memory by:

1. Inserting a copy of the Series IV Supplemental Level Diagnostic, Order No. 133511, into the floppy disk drive No. 0 and closing the latch and pressing the RESET switch (refer to Section 3.15).
2. Typing "Z" and the test name into the system.
3. Activating the TMON monitor by typing a GO command "G".

NOTE

To exit a diagnostic test and return to the monitor so that another test may be exercised or testing abandoned altogether, type:

*<cr>

(Example of initiating SIVWIN)

```
Series IV Diagnostic Monitor x.y.
><cr>
File SIVWIN loaded (takes approximately 40 sec.)
><cr>
```

Winchester Subsystem Supplemental Test for the Intellec Series IV Development System, Version x.y

4. Type the appropriate response (reverse video) and press the carriage return key <cr> as shown below.

```
000BH  *** IGNORED ***
000EH  *** IGNORED ***
0015H  *** IGNORED ***
0016H  *** IGNORED ***
0017H  *** IGNORED ***
0000H  RESET TEST                                    ''PASSED''
0001H  TRANSFER STATUS                               ''PASSED''
0002H  BUFFER I/O TEST                               ''PASSED''
0003H  ROM CHECKSUM TEST                             ''PASSED''
0004H  RAM WINDOW TEST                               ''PASSED''
0005H  RAM ADDRESS TEST                              ''PASSED''
0006H  FORMAT TEST                                   ''PASSED''
0007H  MICRO-DIAGNOSTICS                             ''PASSED''
0008H  SEEK/VERIFY TEST                              ''PASSED''
0009H  WORST CASE SEEK TEST                          ''PASSED''
000AH  WRITE/READ TEST                               ''PASSED''
000CH  PLATTER/HEAD SELECTION TEST                   ''PASSED''
000DH  SECTOR SELECTION TEST                         ''PASSED''
000FH  TRACK VERIFY TEST                             ''PASSED''
0010H  PLATTER VERIFY TEST                           ''PASSED''
0011H  ALTERNATE TRACK TEST                          ''PASSED''
0012H  ZERO FILL TEST                                ''PASSED''
0013H  DATA OVERRUN TEST                             ''PASSED''
0014H  AUTO-INCREMENT TEST                           ''PASSED''
*
```

Figure 3-6. Series IV, SIVWIN Confidence Test Display

```
TYPE OF UNIT BEING TESTED?
0 = 8 INCH WINCHESTER  1 = 5 1/4 INCH WINCHESTER
- ENTER NUMBER *<cr>
Which type of system?
  0 = TPS   1 = DBP   2 = NRM   3 = S-IV
*<cr>
 ALL INITIALIZE NUMBERS MUST BE DECIMAL
IS UNIT 0 BEING TESTED (Y or N) *<cr>
 IS THIS UNIT BACKED UP (Y or N) *<cr>
DO YOU WANT TO USE THE INITIALIZATION DEFAULTS (Y or N)
*<cr>
 IS UNIT 1 BEING TESTED (Y or N) *<cr>
 IS UNIT 2 BEING TESTED (Y or N) *<cr>
 IS UNIT 3 BEING TESTED (Y or N) *<cr>
 THIS COULD TAKE 1 MINUTE
 PASS
 MDS/VERSION x.y
 CANNOT READ DEFECT INFORMATION
 *
```

5. Enter the following command to execute tests 0H AH and FH-14H:

   *T < c r >

6. The CRT at the SIV will display the messages shown in Figure 3-6 when all tests pass.xm

3.19.3 SIVWIN Test Descriptions

Table 3-8 describes the function of each individual test contained in the SIVWIN test suite.

Table 3-8. Series IV, SIVWIN Test Descriptions

TEST #	TEST NAME	TEST DESCRIPTION
0000H	Reset	Resets the controller and initializes the Winchester Disk controller.
0001H	Transfer Status	Checks communication lines between controller and drive by enabling the transfer error status function.
0002H	Buffer I/O	Verifies the transfer of data between the controller and CPIO memory.
0003H	ROM Checksum	Checks the controller ROM by running the on-board ROM checksum test.
0004H	RAM Window	Checks 2KB bytes of controller on board RAM by walking ones and then zeros through memory.
0005H	RAM Address	Verifies RAM address lines.
0006H	Format	Formats and verifies diagnostic tracks on the Winchester drive.
0007H	Micro-Diagnostics	Executes on-board ROM-based diagnostics to verify fundamental controller-drive functions.
0008H	Seek/Verify	Checks seek and verify functions by reading the first sector on the first and last tracks of each surface.
0009H	Worst Case Seek	Checks seek and verify functions by executing a worst case seek sequence.
000AH	Write/Read	Verifies write and read functions by writing/reading the diagnostic tracks.
000BH*	Drive Selection	Verifies controller access of each drive when more than one drive is operating.
000CH	Platter/Head Selection	Verifies that each platter and head can be accessed individually.
000DH	Sector Selection	Verifies that each sector of a diagnostic track can be written, read and verified.
000EH*	Overlap Seek	Verifies correct controller overlap control on more than one disk drive.
000FH	Track Verify	Verifies data fields on a pre determined number of tracks.
0010H	Platter Verify	Verifies data fields on all drive tracks.
0011H	Alternate Track	Checks alternate track capability by assigning and accessing an alternate diagnostic track.
0012H	Zero Fill	Verifies controller ability to fill partial sectors with zeroes on a diagnostic track.

Table 3-8. Series IV, SIVWIN Test Description (Cont'd.)

TEST #	TEST NAME	TEST DESCRIPTION
0013H	Data Overrun	Reads the area immediately following partial sectors on a diagnostic track to determine if extra (overrun) data is being written.
0014H	Auto-Increment	Verifies controller ability to increment to the next sector, head, or cylinder automatically. **NOTE** You must spell out the answer Y-E-S, if the system disk is backed up in order to run tests 0015H to 0017H.
0015H*	Write/Read/Compare	Writes the worst case data pattern (6DB6H) to all drive sectors and verifies the pattern. Writes the complement pattern (9249H) and verifies that pattern.
0016H*	Write All/Read/Compare	Writes a random data pattern to all drive sectors, then reads and compares the data with the original patterns.
0017H*	Format Entire Drive(s)	This utility formats all attached drives. All sectors are formatted as data sectors. An interleave factor of four is used. This differs from the operating system "FORMAT" command.

* Ignored at test initialization.

3.19.4 SIVWIN Test Execution Times

Approximate execution times for individual tests or groups of tests are shown in Table 3-9.

Table 3-9. Series IV, SIVWIN Test Execution Time

Test No.	One Drive
0 to 8	12 seconds (combined)
9	2 minutes 57 seconds
A	7 seconds
B*	Ignored
C and D	3 seconds (combined)
E*	Ignored
F	7 seconds
10	2 minutes 54 seconds
11 to 14	5 seconds (combined)
15	52 minutes
16	1 hour 27 minutes
17**	3 minutes 42 seconds

* Ignored unless more than one drive is present and selected for testing.

** Not a test; a utility routine that formats all selected drives.

3.20 SIVCOM Standalone Confidence Test

When initiated, the SIVCOM confidence test verifies the operation of the optional iSBC 550 ethernet communications board set. The following paragraphs familiarize the user with the actual operation of the SIVCOM confidence test.

3.20.1 Initiating the SIVCOM Confidence Test

The following procedures offer step-by-step instructions for initializing and running the SIVCOM test suite in the single station test mode:

1. Verify that the Intellink and iSBC 550 Ethernet Communications Board set (option) has been installed and power has been applied. Contact you Intel representative for this option information.
2. Insert a copy of the Series IV Supplemental Level Diagnostic, Order No. 133511, into the floppy disk drive No. 0, closing the latch and pressing the "RESET" switch (refer to Section 3.15).
3. Type "Z" and the test name "SIVCOM" into the system.
4. Activate the TMON monitor by typing a GO command "G".
5. Define test suite parameters and starting the test procedure. (see Appendix A for TMON commands).

NOTE

Operator entries are shown in reverse video and the <cr> indicates pressing the keyboard RETURN key.

NOTE

To exit a diagnostic test and return to the monitor so that another test may be exercised or testing abandoned altogether, type:

*[illegible]<cr>

(Example of initiating SIVCOM)

```
Series IV Diagnostic Monitor, x.y
>[illegible]<cr>
File SIVCOM loaded
<[illegible]<cr>
iSBC-550 Ethernet Controller 8086-Based Diagnos-
tic, Vx.y

*[illegible]<cr>
0001H *** IGNORED ***
001EH *** IGNORED ***
001FH *** IGNORED ***
0020H *** IGNORED ***
0021H *** IGNORED ***
0022H *** IGNORED ***
0023H *** IGNORED ***
0024H *** IGNORED ***
0025H *** IGNORED ***
0026H *** IGNORED ***
0027H *** IGNORED ***
```

```
0028H *** IGNORED ***
0029H *** IGNORED ***
0000H Processor Wake-up Ports
0000H Processor Wake-up Ports                    ''PASSED''
0002H Processor Hardware Reset
0002H Processor Hardware Reset                   ''PASSED''
0003H Processor Multibus Data Ripple
0003H Processor Multibus Data Ripple             ''PASSED''
0004H Processor Multibus Address Ripple
0004H Processor Multibus Address Ripple          ''PASSED''
0005H Processor Firmware Verify
0005H Processor Firmware Verify                  ''PASSED''
0006H Processor/Host Bus Arbitration
0006H Processor/Host Bus Arbitration             ''PASSED''
0007H Processor DRAM Data Ripple
0007H Processor DRAM Data Ripple                 ''PASSED''
0008H Processor 8202 DRAM Bank Select
0008H Processor 8202 DRAM Bank Select            ''PASSED''
0009H Processor 8202 DRAM Refresh
0009H Processor 8202 DRAM Refresh                ''PASSED''
000AH Processor DRAM March Test
000AH Processor DRAM March Test                  ''PASSED''
000BH Processor SRAM Data Ripple
000BH Processor SRAM Data Ripple                 ''PASSED''
000CH Processor SRAM March Test
000CH Processor SRAM March Test                  ''PASSED''
000DH PROCESSOR SYS/LOC Memory Access
000DH PROCESSOR SYS/LOC Memory Access            ''PASSED''
000EH Processor 8255A
000EH Processor 8255A                            ''PASSED''
000FH Processor 8253
000FH Processor 8253                             ''PASSED''
0010H Processor 8237
0010H Processor 8237                             ''PASSED''
0011H Processor 8237/SRAM Addressing
0011H Processor 8237/SRAM Addressing             ''PASSED''
0012H Processor 88/8237 SRAM Contention
0012H Processor 88/8237 SRAM Contention          ''PASSED''
0013H Processor 8259/RCV Request Latch
0013H Processor 8259/RCV Request Latch           ''PASSED''
0014H SerDes Transmit Enable
0014H SerDes Transmit Enable                     ''PASSED''
0015H SerDes Transmit Sequencing
0015H SerDes Transmit Sequencing                 ''PASSED''
0016H SerDes Internal Carrier Sense
0016H SerDes Internal Carrier Sense              ''PASSED''
0017H SerDes Ethernet Address PROM
0017H SerDes Ethernet Address PROM               ''PASSED''
0018H SerDes Promiscuous Receive
0018H SerDes Promiscuous Receive                 ''PASSED''
0019H SerDes Non-Promiscuous Receive
0019H SerDes Non-Promiscuous Receive             ''PASSED''
001AH SerDes Transmit Long Packet
001AH SerDes Transmit Long Packet                ''PASSED''
001BH SerDes Interpacket Spacing
001BH SerDes Interpacket Spacing                 ''PASSED''
001CH SerDes Receive CRC Circuit
001CH SerDes Receive CRC Circuit                 ''PASSED''
001DH SerDes External Transmit Loopback
001DH SerDes External Transmit Loopback          ''PASSED''
```

3.20.2 SIVCOM Test Descriptions

Table 3-10 identifies each SIVCOM test and describes its operation.

Table 3-10. Series IV, SIVCOM Test Descriptions

TEST #	TEST NAME	TEST DESCRIPTION
0000H	Processor Wake-up Ports	Verifies that processor board responds to wakeup command from host.
0001H*	Processor Multibus Interrupt	Verifies ability of the processor board to generate level 6 (INT6/) system interrupt. Host responds to interrupt by resetting processor board interrupt latch.
0002H	Processor Hardware Reset	Verifies that interrupt latch, Multibus I/O latch, 8237 DMA Controller, and 8255A Programmable Peripheral Interface are reset by Select Reset (SEL RESET) command.
0003H	Processor Multibus Data Ripple	Verifies integrity of the Multibus data drivers.
0004H	Processor Multibus Address Ripple	Verifies ability to access system memory.
0005H	Processor Firmware Verify	Verifies integrity of 8Kbytes of ROM by executing a checksum test.
0006H	Processor/Host Bus Arbitration	Verifies ability to arbitrate, gain control, and release control of the Multibus interface (system bus).
0007H	Processor DRAM Data Ripple	Verifies ability to read/write its 16KB Dynamic RAM Memory.
0008H	Processor 8202A DRAM Bank Select	Verifies ability of 8202A Dynamic RAM Controller to differentiate between DRAM addresses and Multibus I/O port addresses.
0009H	Processor 8202A DRAM Refresh	Verifies ability of 8202A to refresh 16KB Dynamic RAM Memory.
000AH	Processor DRAM March	Tests all 16KB of Dynamic RAM Memory by executing standard march algorithm.
000BH	Processor SRAM Data Ripple	Verifies integrity of DMA bus data lines by writing to and reading from Static RAM Memory.
000CH	Processor SRAM March	Tests all 8KB of Static RAM Memory by executing standard march algorithm.
000DH	Processor SYS/LOC	Verifies ability of processor board to access lower 2KB (00000 007FFH) in on-board DRAM and in system RAM.
000EH	Processor 8255A	Verifies ability of 8255A Programmable Peripheral Interface to latch Port B and Port C data.
000FH	Processor 8253	Verifies ability of all three 8253 Programmable Interval Timer counters to count down and to interrupt the 8088 CPU on reaching terminal count; also verifies "on the-fly" count values while waiting for terminal count.

Table 3-10. Series IV, SIVCOM Test Descriptions (Cont'd.)

TEST #	TEST NAME	TEST DESCRIPTION
0010H	Processor 8237	Verifies ability of all four 8237 DMA Controller channels to (1) read/write Base and Current Address registers, (2) read/write Base and Current Word Count registers, (3) increment/ decrement Current Address register, (4) increment Current Word Count register, and (5) autoinitialize Current Address and Word Count registers.
0011H	Processor8237/SRAM Addressing	Verifies ability of 8237 DMA Controller to access all 8KB of SRAM memory.
0012H	Processor 88/8237 SRAM Contention	Verifies ability of 8088 CPU and SRAM Contention 8237 DMA Controller to resolve arbitration of DMA bus and to access SRAM memory.
0013H	Processor 8259/RCV Request Latch	Verifies ability of the three DMA receive channels and one transmit channel to generate interrupt requests via the 8259A Programmable Interrupt Controller. SerDes board is cleared following each interrupt.
0014H	SerDes Transmit Enables	Verifies that Transmit Start Enable (TXSRT) command initiates SerDes board transmit startup sequence and that SerDes board sets Enable Transmit Data (ENABLE TXD) status bit.
0015H	SerDes Transmit Sequencing	Verifies that the SerDes board clears Enable Transmit Data (ENABLE TXD) status bit after transmit shutdown.
0016H	SerDes Internal Carrier Sense	In both the Read Address and Carrier Sense Verify SerDes modes, verifies that SerDes board generates Carrier Sense (CS) Signal.
0017H	SerDes Ethernet Address PROM	Verifies integrity of SerDes board Address PROM.
0018H	SerDes Promiscuous Receive	Verifies ability of SerDes board to receive broadcast and self addressed packets that contain good CRC data when SerDes board Promiscuous Receive bit is set.
0019H	SerDes Non-	In Verify SerDes mode, with Promiscuous Receive control bit cleared, verifies ability of SerDes board to (1) receive broadcast packets, (2) receive self-addressed packets, and (3) reject all other packets.
001AH	SerDes Transmit	Verifies that SerDes board sets Transmit Time Out (TXTO) status bit when packet exceeds maximum length. Also verifies that SerDes board does not set TXTO status bit when maximum length packet is transmitted.
001BH	SerDes Interpacket	In Verify SerDes modes, verifies that SerDes board enforces interpacket gap requirement.

Table 3-10. Series IV, SIVCOM Test Descriptions (Cont'd.)

TEST #	TEST NAME	TEST DESCRIPTION
001CH	SerDes Receive CRC	In Verify SerDes mode, verifies ability of SerDes board to transmit and receive data packets that contain bad CRC data and report CRC errors to processor board.
001DH	SerDes External Receive Loopback	Demonstrates send and receive capabilities by transmitting two self-addressed packets that contain random data via an external loopback path provided by the Intellink chassis or a transceiver.

* Ignored at test initialization.

3.20.3 SIVCOM Execution Times

The approximate execution times of the SIVCOM Confidence individual or groups of tests are listed in Table 3-11.

Table 3-11. Series IV, SIVCOM Test

Test #	Execution Time
0	15 seconds
2	15 seconds
3 - 5	2 seconds
6	4 seconds
7 - 12	2 seconds
13	6 seconds
14 - 19	1 second
1A	8 seconds
1B	1 second
1C	45 seconds
1D	1 second

3.21 SIV740 Confidence Test

The SIV740 test suite verifies proper operation of the Model 740 Hard Disk Controller boards and the disk drive. The diagnostic test is divided into three test sequences; 740 controller self tests, the drive tests, and the error detection tests.

3.21.1 SIV740 Test Execution

All TMON commands may be used with the SIV740 test suite. Appendix A provides command descriptions, syntax, and example entries for TMON commands. The user may also use utility and test subroutines to execute specific drive functions. These utility and test subroutines are described in the Model 740/743 Hard Disk System Test Field Service Manual. Below are step-by-step instructions for executing the drive test sequence of the SIV740 test suite:

1. Insert a copy of the Series IV Supplemental Level Diagnostic, Order No. 133511, into the floppy disk drive No. 0, close the latch and press the "RESET" switch (refer to Section 3.15).
2. Type "Z" and the test name "SIV740" into the system.

3. Activate the TMON monitor by typing a GO command "G".
4. Define test suite parameters and start the test procedure. (see Appendix A for TMON commands).

NOTE

Operator entries are shown in reverse video and the <cr> indicates pressing the keyboard RETURN key.

Check that the 740 Hard Disk "READY" (up to speed) light is lite before proceeding with the SIV740 Confidence Test.

NOTE

To exit a diagnostic test and return to the monitor so that another test may be exercised or testing abandoned altogether, type:

*EXIT<cr>

(Example of initiating SIV740)

```
Series IV Diagnostic Monitor, x.y
>ZSiv740<cr>
File SIV740 loaded
>G<cr>
SIV 740 TEST x.y
enter platter id's:*
```

The SIV740 test suite, now loaded into the system.

5. Entering platter identification numbers selects the drive test sequence and the platters to be tested. The zero character (0) selects the first drive unit; the one character (1) selects the second drive unit. For example, enter the following character to test both platters of the first drive unit:

   *0<cr>

6. Type 0R<cr> to test the removable disk or type 0F<cr> to test the fixed disk drive. Type 1<cr> to test the second drive unit; type 0 1<cr> to test both drive units. The terminal displays the following message:
   make sure all drives and platters selected are ready and not write protected
   *
7. Press the START/STOP switch on the drive unit(s) to be tested and ensure the "READY" light is on.
8. Start the test by typing:

   *T<cr>

The terminal displays the following messages when all tests pass:

```
0001H *** IGNORED ***
0002H *** IGNORED ***
0009H *** IGNORED ***
000BH *** IGNORED ***
000DH *** IGNORED ***
000EH *** IGNORED ***
000FH *** IGNORED ***
0010H *** IGNORED ***
0011H *** IGNORED ***
0012H *** IGNORED ***
0013H *** IGNORED ***
```

```
0000H Controller Status Test

controller status test

controller base word = 68H

mds-240/740 firmware level = 02H

0000H Controller Status Test                    ''PASSED''
nop test
0003H NOP Test                                  ''PASSED''
recalibrate test
0004H Recalibrate Test                          ''PASSED''
seek test
0005H Seek Test                                 ''PASSED''
drive selection test
0006H Drive Selection Test                      ''PASSED''
platter/surface selection test
0007H Platter/Surface Selection Test            ''PASSED''
sector selection test
0008H Sector Selection Test                     ''PASSED''
track verify test
0009H Track Verify Test                         ''PASSED''
drive switches test
000AH Drive Switches Test

write protect drive 0T, fixed platter
write enable all other platters
type cr when write protected
```

9. Write protect the specified platter (drive unit control switches) and press the terminal RETURN key. The test provides additional messages to test the remaining combinations of switch positions. After the sequence of switch tests is complete, the display continues:

NOTE

Check the 740 Hard Disk "READY" light and make sure it is lite (up to speed) before proceeding with the SIV740 test.

```
000AH Drive Switches Test                       ''PASSED''
memory addressing test
000CH Memory Addressing Test                    ''PASSED''
```

10. Test 14 then displays the error tables. A prompt message is displayed to allow the operator to clear the error tables.

11. Press the return key. The terminal displays the command prompt (*) to indicate that the program is at the TMON command level.

3.21.2 SIV740 Test Descriptions

The test descriptions of SIV740 in Table 3-12 explain the operation of the test as it exercises the 740 logic.

Table 3-12. Series IV, SIV740 Test Descriptions

TEST #	TEST NAME	TEST DESCRIPTION
0000H	Controller Status	Verifies basic controller commands and displays controller ID values.
		Controller Self Tests
0001H*	Self Diagnostic	Reserved for Intel Service Personnel.
0002H*	20 Bit Self	Reserved for Intel Service Personnel.
		Drive Test Sequence
0003H	NOP	Verifies handshaking ability of controller by executing NOOP function.
0004H	Recalibrate	Verifies ability to recalibrate drive by seeking track 407, then back to track 0.
0005H	Seek	Verifies ability to seek to preselected tracks.
0006H	Drive Selection	Verifies that controller can access each drive separately when more than one drive is connected to the controller.
0007H	Platter/Surface Selection	Verifies that each platter and head can be addressed individually.
0008H	Sector Selection Test	Verifies that each sector of a track can be addressed individually.
0009H*	Track Verify	Verifies all sectors of data on preselected tracks.
000AH	Drive Switches Test	Verifies that controller can detect status changes caused by drive READY and WRITE PROTECT switches. The user is prompted to make several changes to the switches during test.
000BH	Overlap Seek Test	Verifies ability to perform concurrent seeks on multiple drives. This test is ignored when the user tests one drive.
000CH	Memory Addressing	Verifies ability of controller to access system RAM memory during data transfers between the system and the disk.
000DH*	Format Track	Initializes specific tracks by writing all address marks, gaps, and data fields to verify format ability of drive. The selected tracks also ensure that tracks can be addresses individually.
000EH*	Track Selection	Verifies ability to individually address disk tracks.
000FH*	Cartridge Defect	Formats and verifies all disk tracks. This test, when run before test 10H causes the test to execute faster.
0010H*	Long Data Transfer	Writes, reads, verifies, and compares data on all tracks, surfaces, and platters. Tracks are accessed in a psuedo-random order from a fixed table in memory. Controller differentiates between recoverable (successful retries) and non-recoverable errors (unsuccessful retries) and alternates between 16-bit and 20 bit addressing when accessing system memory.
0011H*	Reserved	Reserved for future use.

Table 3-12. Series IV, SIV740 Test Descriptions (Cont'd.)

TEST #	TEST NAME	TEST DESCRIPTION
0012H	Verify Platter	Verifies surface integrity of selected platters without destroying user data. The test displays a decimal digit for each track verified (the sequence 0-9 is repeated 40 times).
		Error Detection Test Sequence
0013H*	Error Detection	This test is reserved for Intel Service Personnel.
		Utility Routine
0014H*	Display Error	This utility routine displays two error tables (one for each drive test sequence) and allows the user to clear the tables.

* Ignored at test initialization.

Tests 000DH to 0013H are ignored at test initialization because they destroy data. Test 000BH is ignored when only one drive unit is selected for testing.

3.21.3 SIV740 Test Execution Times

Approximate execution times for individual SIV740 tests or series of tests are listed in Table 3.13.

Table 3-13. Series IV, SIV740 Test Execution Times

Test No.	Execution Time
0	2 seconds
3 to 9	24 seconds (Combined)
*A	65 seconds (Minimum)
**B	60 seconds (Maximum)
C	3 seconds
D	27 seconds
E	17 seconds
F	6 minutes 45 seconds
10	6 minutes 47 seconds
11	Ignored
12	5 minutes 12 seconds

* User must configure drive unit control switches during test.

** Ignored when only one drive unit is selected for testing.

Times shown assume the following:

- Testing both platters of one drive unit (two drive units for test 000BH)
- TMON debug switch set (=1) to enable error messages
- All tests pass

CHAPTER 4
INSTALLING OPTIONS

4.1 Introduction

This chapter provides information on installing options. The information consists of priority resolution, instructions for installing optional printed wiring assemblies (boards) and peripherals, and other information for configuring the system to fit a variety of applications. Before performing the instructions in this chapter, install and test the system as described in Chapters 2 and 3.

4.2 Card Cage Layout

Many of the options available for the system require installation of boards to be connected to a common bus (Multibus backplane). These card slots are referenced from 1 thru 10 beginning at the slot closest to the CRT and going outward toward the right-hand side of the system. The backplane connectors (J1–J10) are numbered in the opposite direction (see Figure 4-1). Slots 7 thru 10 are accessible through the door on top of the system. To install boards in slots 4 thru 6, the cover must be removed from the system. To install boards in slots 1 thru 3, an internal cover must be removed also.

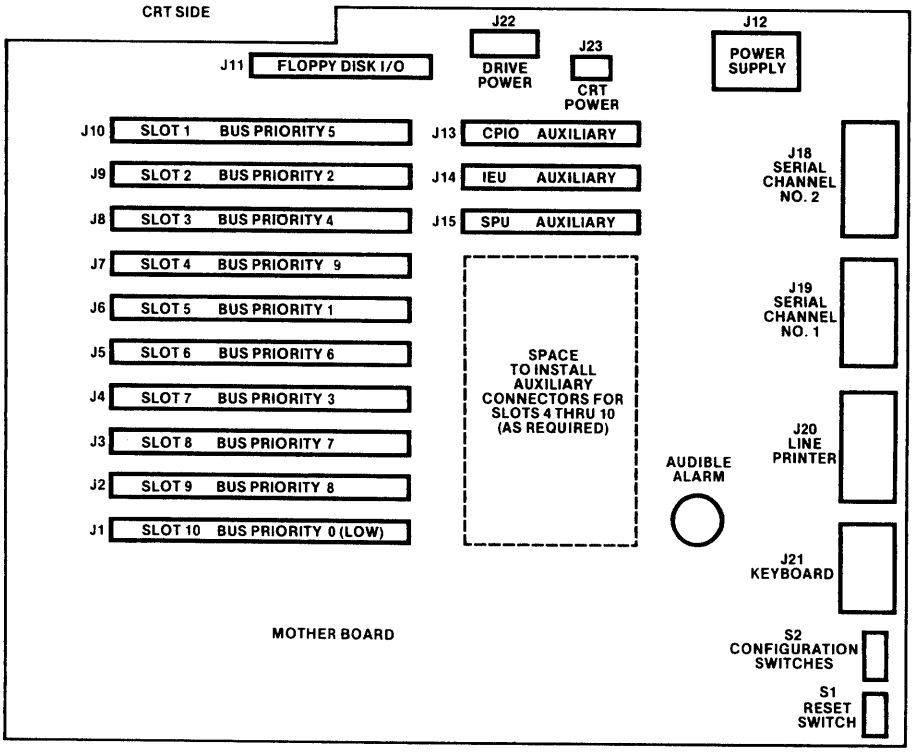


Figure 4-1. Series IV, Backplane Connectors and Slot Assignments

Connectors J13 thru J15 are auxiliary connectors that mate with the P2 connector of the boards installed in slots 1 thru 3 respectively. Space is provided for using auxiliary connectors, if they are required, on the boards installed in slots 4 thru 10. Auxiliary connectors are usually used for communication between boards that are installed in two and three board sets, such as the In-Circuit Emulator (ICE) products. Auxiliary connector assemblies with two and three connectors are supplied with the system accessory kit.

4.3 Backplane Bus Priority

Boards installed in the system backplane access the backplane bus on a priority basis depending upon their card slot location. In general, boards or board sets used for mass storage and (disk) controllers require the highest priority slots. Lower priority slots are normally assigned to peripherals that access the bus less frequently. Usually only one board in the board set will request service through the backplane bus, while other boards in the set may not affect the priority structure. Add-on memory boards do not request bus service and can be inserted in any slot without changing the existing priorities. The priorities assigned to each slot are listed in Table 4-1 and Figure 4-1.

Table 4-1. Series IV, Bus Priority Assignments

Bus Priority	Slot Number	Backplane Connector Designation
9 (Highest)	4	J7
8	9	J2
7	8	J3
6	6	J5
5	1	J10, J13
4	3	J8, J15
3	7	J4
2	2	J9, J14
1	5	J6
0 (Lowest)	10	J1

4.4 Installing Optional Boards

The priorities of various optional boards of the basic system are shown in Figure 4-2. Before installing options determine the exact board placement. Optional boards are installed in the mainframe card cage using the applicable procedures given in Paragraphs 4.5 thru 4.9. Before an optional board is installed, determine what applicable procedures must be performed as follows:

If the ICE, Model 740/743, iSBC550 and iMDX720 options are installed, the ICE Controller board must be installed in the highest priority slot.

1. What is the relative priority for the board to be installed? Refer to Figure 4-2.
2. Is an auxiliary connector required? Refer to Paragraph 4.5.

Priority	Slot	Jack	Board	Configuration Options								
5	1	J10	CPIO									
2	2	J9	IEU									
4	3	J8	SPU*									
9	4	J7	056									
1	5	J6		215D	550 or 740	215D	215D	215B	215B	215D	215D	215D
6	6	J5		550 or 740	550 or 740	215B	215B	216	216	215B	215B	215B
3	7	J4		550 or 740	ICE	550 or 740	550	550 or 740	ICE	216	216	216
7	8	J3		ICE	ICE	550 or 740	550	550 or 740	ICE	550 or 740	ICE	Open
8	9	J2		ICE	ICE	ICE	740	ICE or 720	ICE	550 or 740	ICE	740 or 720
0	10	J1		ICE	ICE	ICE	740	ICE or 720	ICE	Open	ICE	740 or 720
*If present												

Figure 4-2. Series IV, Optional Board Placement

3. Does installation require an internal cable assembly to connect between a top-edge connector on the board and an external device? Refer to Paragraph 4.7.
4. What slot or slots will be used to install the board or board set? To install boards in slots 4 thru 10, refer to Paragraph 4.8; boards in slots 1 thru 3 (CPIO, IEU and SPU) refer to Paragraph 4.9.

CAUTION

DO NOT remove, install, connect or disconnect any board or cable assembly while development system power is on. Performing these operations with power on may cause damage to connectors and other components.

4.5 Auxiliary Connector Installation

Auxiliary connectors consist usually of two or three edge connector sockets mounted on a printed wiring assembly. They are used to provide interconnections (interface) between the P2 connectors in board sets that contain two or three boards. The ICE-85 and ICE-86 are typical options with two or three board sets that require auxiliary connectors.

One auxiliary connector with two sockets (dual-auxiliary connector) and one auxiliary connector with three sockets (triple-auxiliary connector) are shipped with the system. These connectors are also usually shipped with options that require them. To ensure proper spacing between connectors, use only auxiliary connectors with the following part numbers:

Dual-Auxiliary Connector, part number 1000515-01
Triple-Auxiliary Connector, part number 1001854-01

The auxiliary connectors can not be installed permanently in the card cage and must be connected to the board set first and the board set then inserted, as a unit, into the appropriate slots in the card cage.

4.6 Top Cover Removal and Reinstallation

It is not always necessary to remove the top cover from the system to install boards. Card cage slots 7 thru 10 are accessible through the board access door (see Figure 4-3). To install boards into card cage slots 1 thru 6 the top cover must be removed.

WARNING

High voltage is present in the mainframe chassis. DO NOT attempt to connect power or operate the system with the cover removed. DO NOT attempt to override the safety interlock switch. DO NOT come in contact with the CRT anode connection. Failure to observe these precautions may result in serious injury.

To remove the top cover from the system, proceed as follows:

1. Turn off system power at the power circuit breaker switch and disconnect the ac power cable from the power receptacle to prevent accidental power turn on.

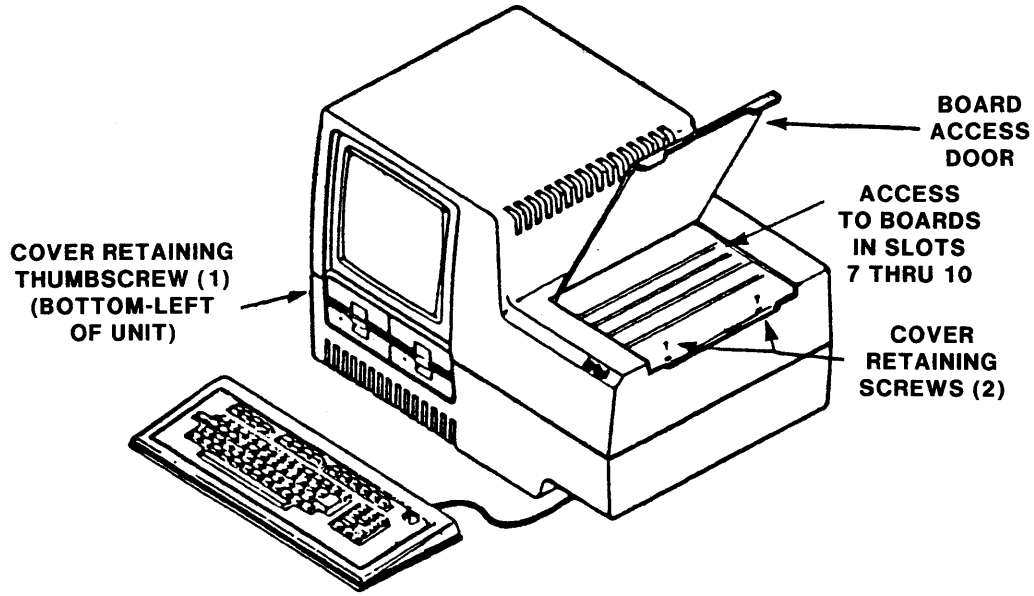


Figure 4-3. Series IV, Mainframe Board Access Door Opened

2. Loosen the cover retaining thumbscrew until it is completely free from the top cover (see Figure 4-3). The thumbscrew remains captive in the base.
3. Lift the board access door and loosen the two cover retaining screws until the screws are completely free from the base (see Figure 4-3). The cover retaining screws remain captive in the cover.

WARNING

While handling the cover or working inside the system chassis, use extreme care not to strike the CRT neck or base. Striking the CRT neck or base could cause the CRT to implode and may cause injury, death and damage in the immediate area.

4. Close the board access door and then lift straight up on the top cover until the top cover completly clears the card cage and CRT. Set the cover aside so that the work area is kept clear.
5. Reinstall the cover before resuming operation by reversing the procedure in steps 1 thru 4.

4.7 Internal Cable Assembly Installation

An internal cable assembly must be installed for boards that interface through their top-edge connector with an external device. The cable assembly and its mounting hardware are usually shipped with the board or board set that requires the external connection. Connectors at one end of the cable assemblies are mounted in the utility connector slots on the back panel (see Figure 4-4). Install any ground wires from the cable assemblies to the threaded inserts, provided on the back panel, with appropriate

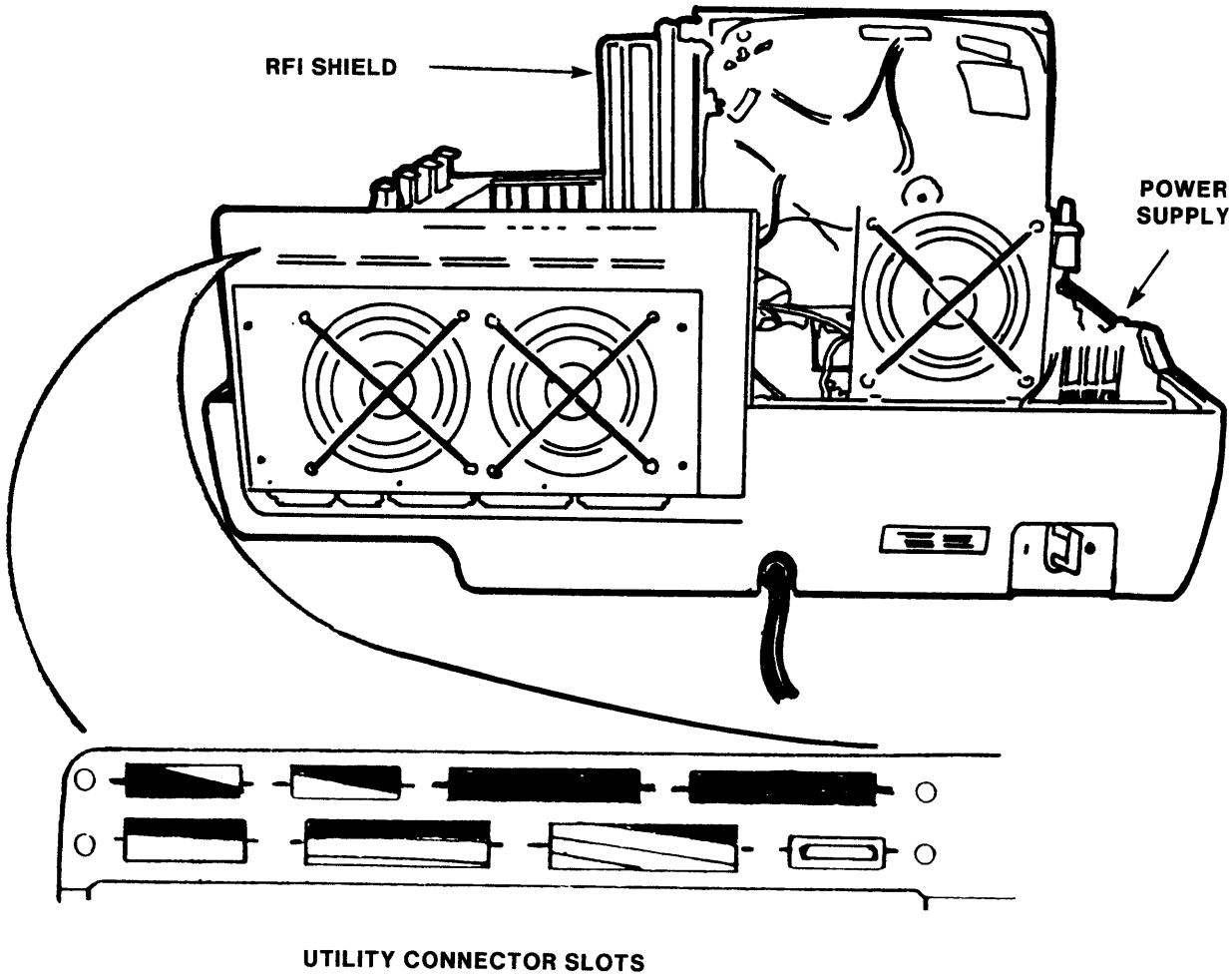


Figure 4-4. Series IV, Mainframe with Cover Removed

hardware. The other end of the cable assemblies have connectors that mate with top edge connectors on the associated boards. The mainframe top cover must be removed in order to gain access to the utility connector slots (refer to Paragraph 4.6). After the cable assembly and board installation are complete, an external cable assembly is connected between the utility connectors and the external device to complete the interface.

NOTE

ICE products use flat cable assemblies to interconnect the top-edge connectors and external buffer boxes. These flat cable assemblies are routed through the slot under the board access door and not through the utility connectors.

4.8. Installing Boards in Slots 4 thru 10

Card cage slots 4 thru 10 accept 7 × 12 inch (17.8 × 30.5 centimeter) Multibus interface compatable boards. Four of these slots (7 thru 10) are accessible through

the board access door (see Figure 4-3) and are usually reserved for boards that may be changed occasionally or that require easy access. Typical options that may be installed in slots 7 thru 10 are ICE and mass storage (disk) controllers (slot 8 has the second highest priority).

When installing ICE boards, route the flat cables from the top edge connectors of the boards through the access door. A slot in the access door has been provided to accomodate these cables.

Slots 4 thru 6 are accessible only when the mainframe top cover is removed, and usually contain boards that are more permanently installed, such as expansion memory boards and data communication board sets.

Depending upon the option being installed, an auxiliary connector and internal cable assembly may be required. Information for installing these assemblies is provided in Paragraphs 4.5 and 4.7.

NOTE

Before installing any boards in the card cage, determine where each board fits in the priority structure (refer to Paragraph 4.3).

Install boards in slots 4 thru 10 by:

1. Turning off system power at the power circuit breaker switch and disconnecting the ac power cable from the receptacle to prevent accidental power turn-on.
2. Lifting the board access door (see Figure 4-3) to gain access to card cage slots 7 thru 10, or remove the top cover (refer to Paragraph 4.6) as required.
3. Checking the board, or board set, to be installed determining proper jumper locations and switch settings. The necessary information for setting board configuration is usually provided with the manuals or other data shipped with the board. Configuration jumper locations for commonly used boards are given in Paragraph 4.10.
4. Installing an auxiliary connector (refer to Paragraph 4.5) and an internal cable assembly (refer to Paragraph 4.7), as required. Install the auxiliary connector on the board set (see Figure 4-5).
5. Installing the board, or board set, in the card cage, making sure that the board edges line up in the card cage guide slots (see Figure 4-4). When boards are lined up and resting on the backplane bus connectors, press down firmly on the lifters at the top corners of the boards until the P1 edge connectors (see Figure 4-5) are seated in the bus connectors.
6. Reinstalling the mainframe top cover (refer to Paragraph 4.6) and closing the board access door.
7. Connecting the ac power cable to a three-conductor power outlet and performing the test procedures given in Chapter 3, making sure system operation has not been affected. The test procedures check optional memory boards, but some ignored test(s) must be recognized to check other optional boards installed in slots 4 thru 10.

4.9 Installing CPIO, IEU and iMDX 434 SPU Boards

The CPIO, IEU and the optional iMDX 434 SPU boards are installed in card cage slots 1, 2 and 3 respectively. Slots 1 thru 3 are accessible only when the top cover is removed from the mainframe and the Radio Frequency Interferance (RFI) shield is removed from the card cage (see Figure 4-4). Slots 1 thru 3 accept 12 × 12 inch

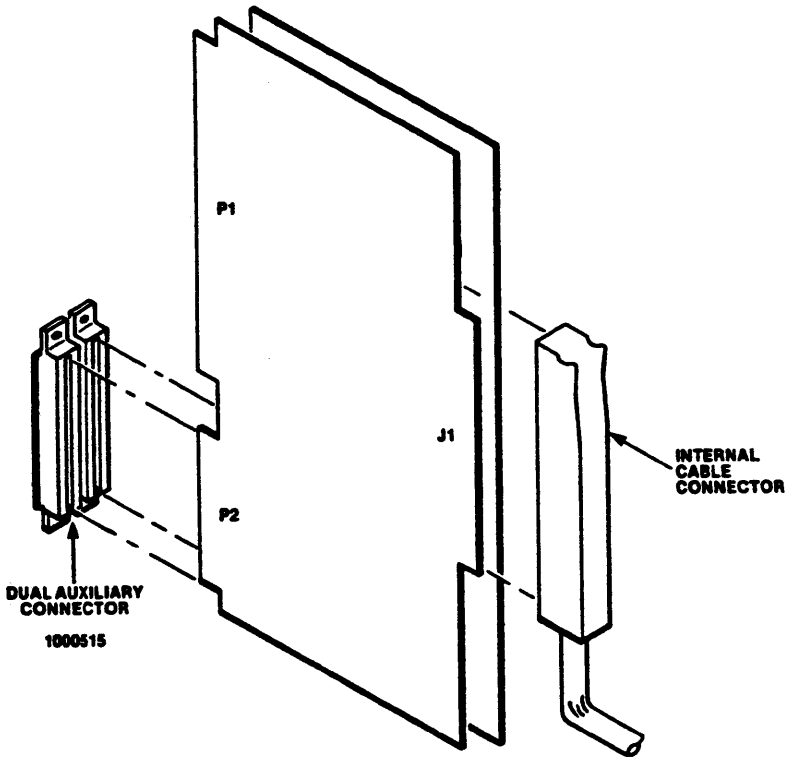


Figure 4-5. Series IV, Auxiliary Connector Installed on a Two-Board Set

(30.5 × 30.5 centimeter) boards that are dedicated to system operation. The layout for these three slots is shown in Figure 4-1 and listed in Table 4-2.

Table 4-2. Series IV, Slot 1, 2 and 3 Layout

Card Slot	Board Name	Board Mnemonic	Bus Connector	Auxiliary Connector	I/O Connector
1	Central Processor and I/O	CPIO	J10	J13	J11, J19 J20, J21
2	ISIS Execution Unit	IEU	J9	J14	J18
3	Enhanced Performance Option	SPU	J8	J15	—

The CPIO and IEU boards are currently installed in the mainframe when the unit is shipped from the factory. The optional SPU board is shipped in a separate box and must be installed by the user. To install and remove these boards:

1. Turn off system power at the power circuit breaker switch and disconnect the ac power cable from the power receptacle to prevent accidental power turn on.
2. Remove the top cover as described in Paragraph 4.6.
3. Loosen the five screws on top of the RFI shield (see 1 of Figure 4-6). Do not remove the screws. These top screws may remain in the card cage frame.

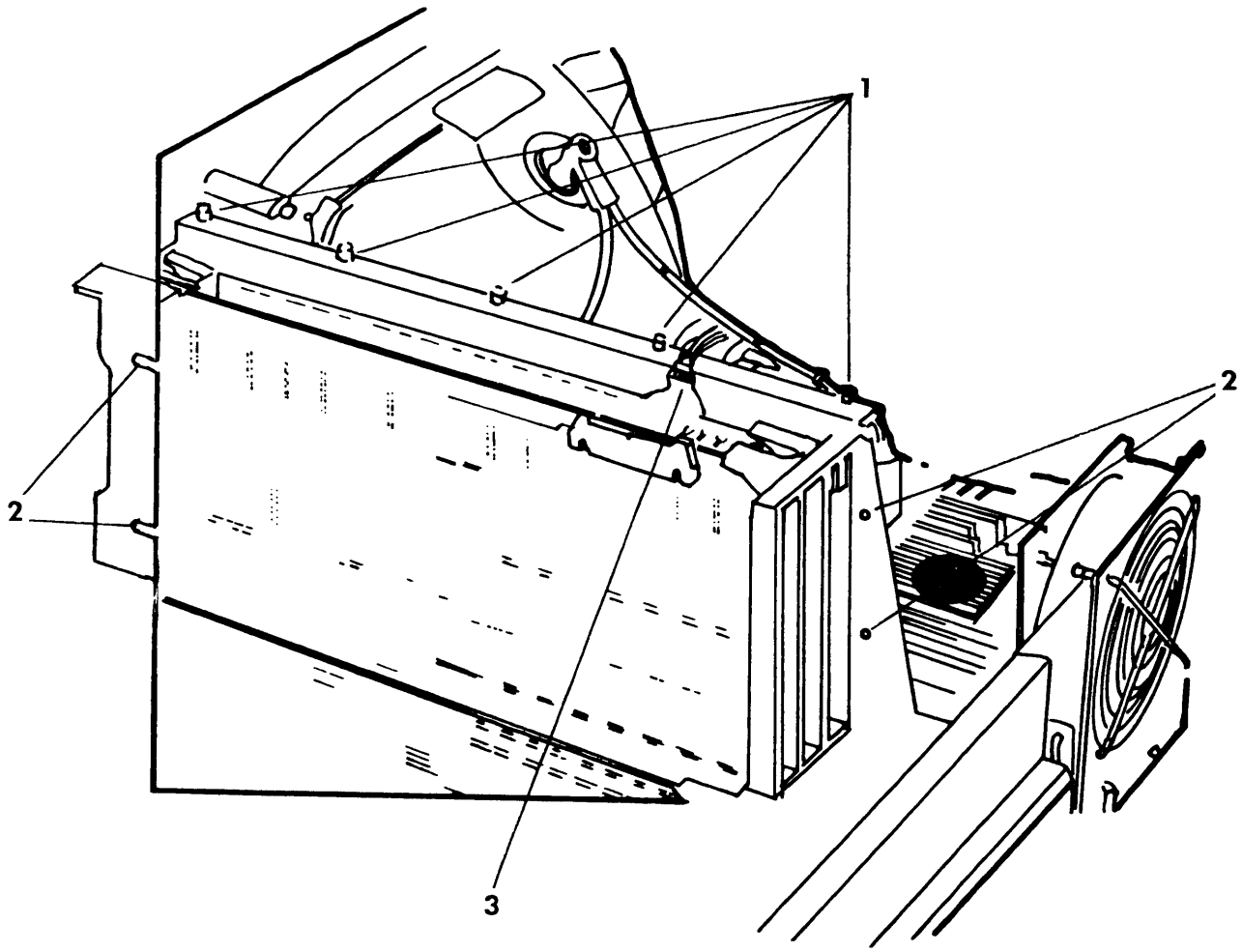


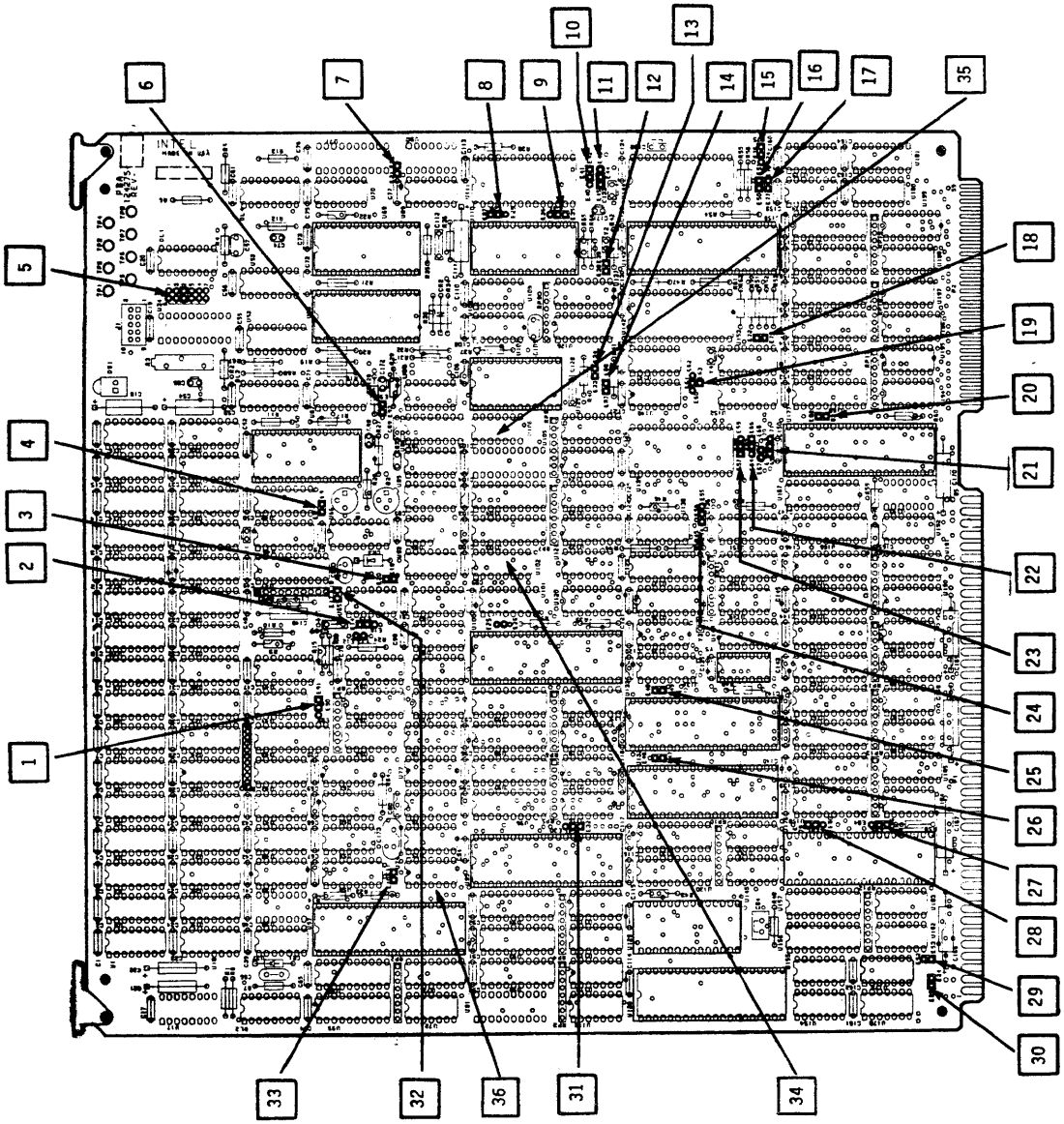
Figure 4-6. Series IV, Mainframe with Cover and RFI Shield Removed

4. Loosen the four captive screws on the side of the RFI shield (see 2 of Figure 4-6). These side screws (two in front and two in back) remain captive in the RFI shield.
5. Slide the RFI shield out from under the top screws and set the RFI shield aside to keep the work area clear.

NOTE

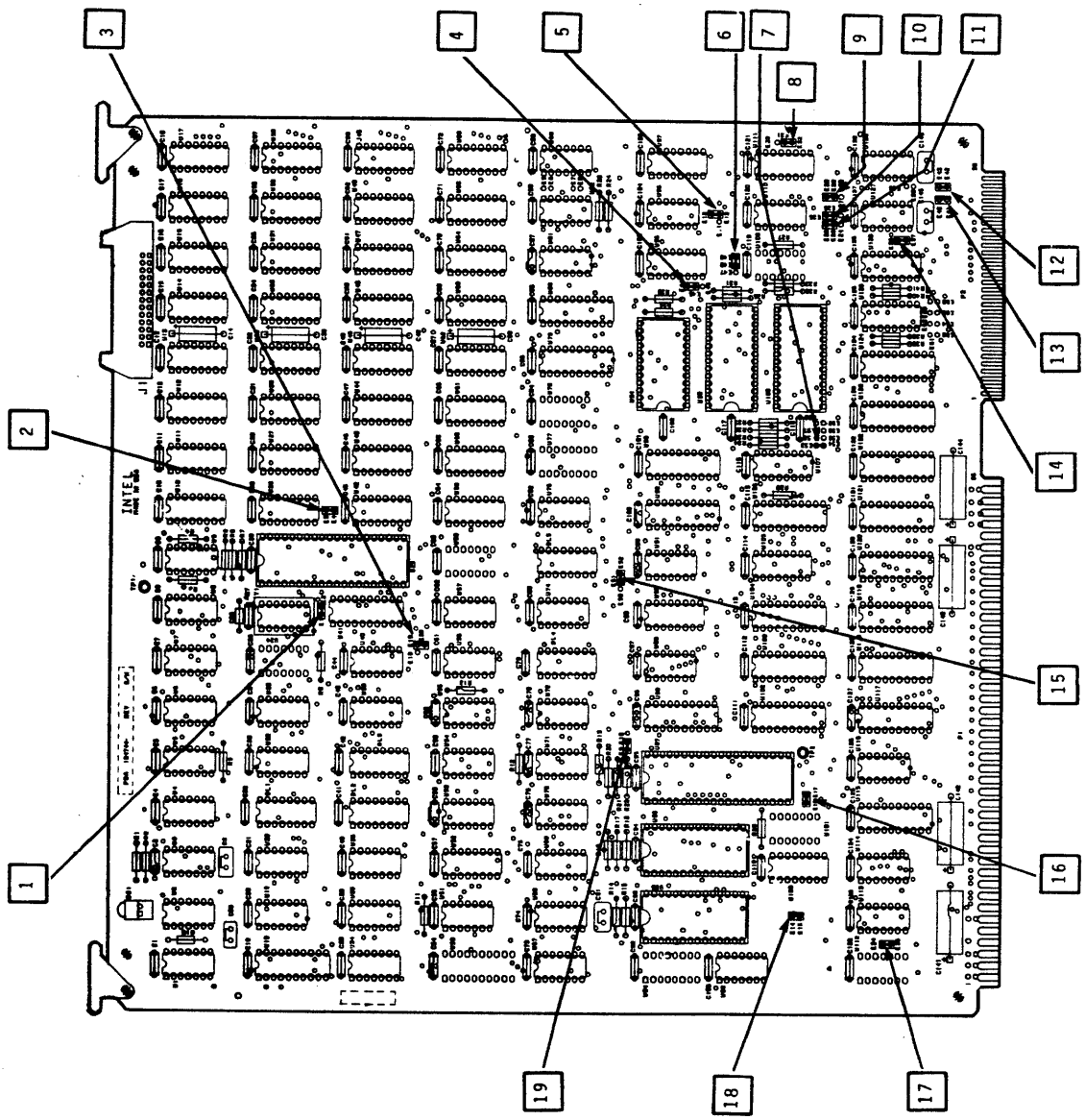
The CRT is connected to J1 on the top of the CPIO board. J1 is the only top edge connector used in slots 1 thru 3.

6. Check the configuration jumpers and switch settings on each board to be installed. The configuration jumper locations and switch settings for the CPIO, IEU, SPU and iSBC 056 boards are given in Paragraph 4.10 and Figures 4-7 thru 4-10.
7. Install the board in the correct card cage slot (see Figure 4-1), making sure that the board edges line up in the appropriate card cage guide slots (see Figure 4-4). When the board is lined up and resting on the backplane bus connector, press down firmly on the lifters at the top corners of the board until the bottom edge connectors are seated in the backplane connectors.



Jumper Connection	Location
E2 - E6	5
E8 - E9	4
E10 - E11	33
E14 - E15	2
E17 - E18	32
E19 - E20	3
E21 - E22	7
E23 - E24	30
E27 - E28	8
E31 - E32	31
E33 - E34	13
E35 - E37	9
E38 - E39	12
E41 - E42	10
E44 - E45	11
E46 - E47	26
E48 - E49	25
E50 - E51	16
E52 - E53	29
E54 - E56	24
E57 - E58	23
E61 - E63	19
E65 - E66	22
E69 - E70	21
E72 - E73	18
E75 - E76	15
E77 - E78	17
E79 - E81	28
E82 - E83	20
E85 - E86	27
E87 - E88	14
E90 - E91	1
E92 - E93	6
E95 - E96	34
E97 - E98	34
E99 - E100	35
E102 - E103	36

Figure 4-7. Series IV, CPIO Board Jumper Configurations



Jumper Connection	Location
E1 - E2	1
E3 - E4	2
E9 - E10	19
E11 - E13	5
E14 - E15	18
E16 - E17	16
E19 - E20	3
E22 - E23	11
E25 - E26	10
E28 - E29	9
E31 - E33	8
E34 - E35	17
E36 - E37	14
E40 - **	13
E41 - **	12
E44 - E45	4
E48 - E49	6
E51 - E52	15
E55 - E56*	7

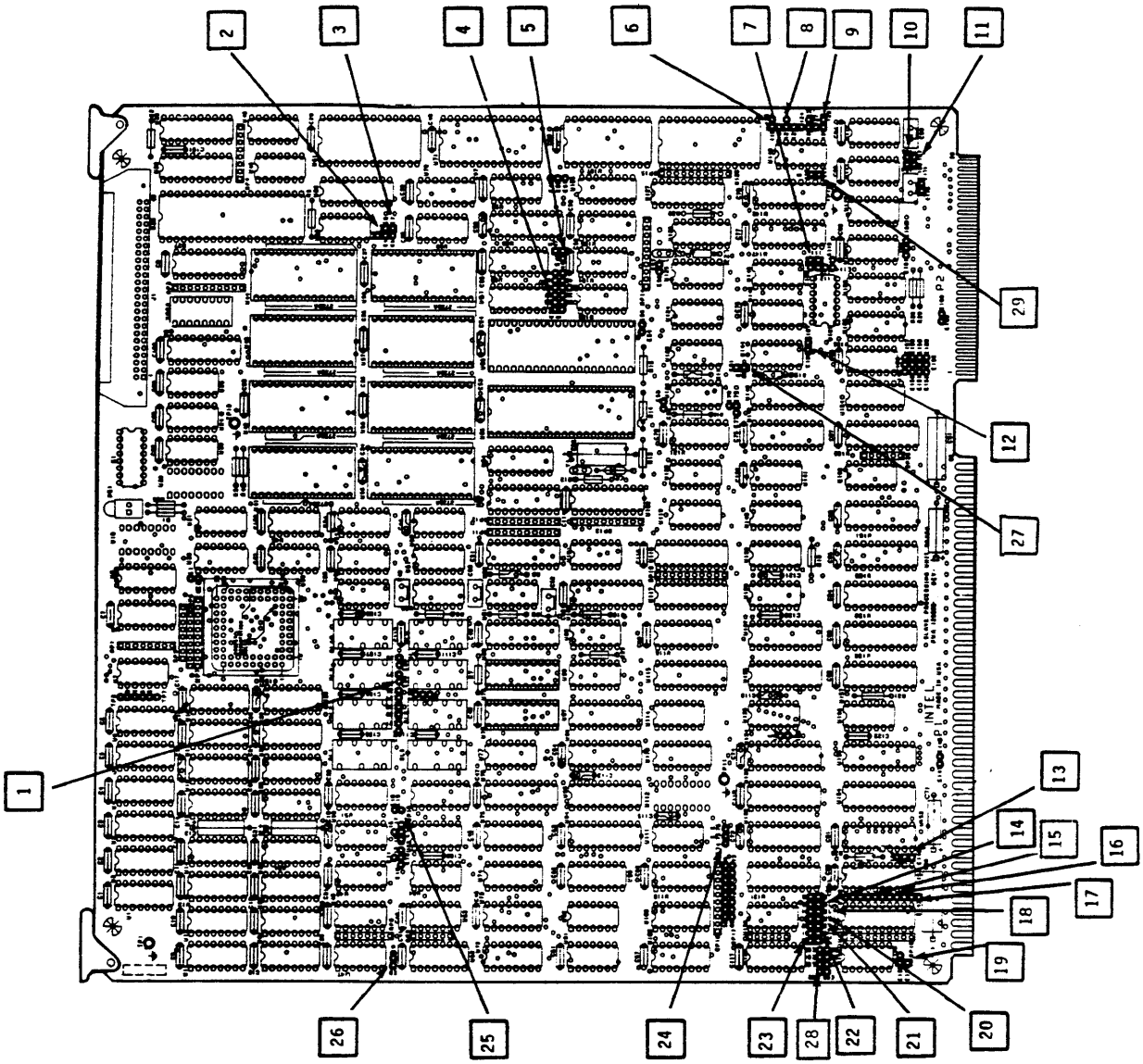
*WITH SPU OPTION THIS JUMPER MOVES TO E53 - E54 AND ADD A JUMPER AT E59 - E60.

**PB 124743-001
E40 - E42
E41 - E43

**PB 124743-002
E40 - E43
E41 - E42

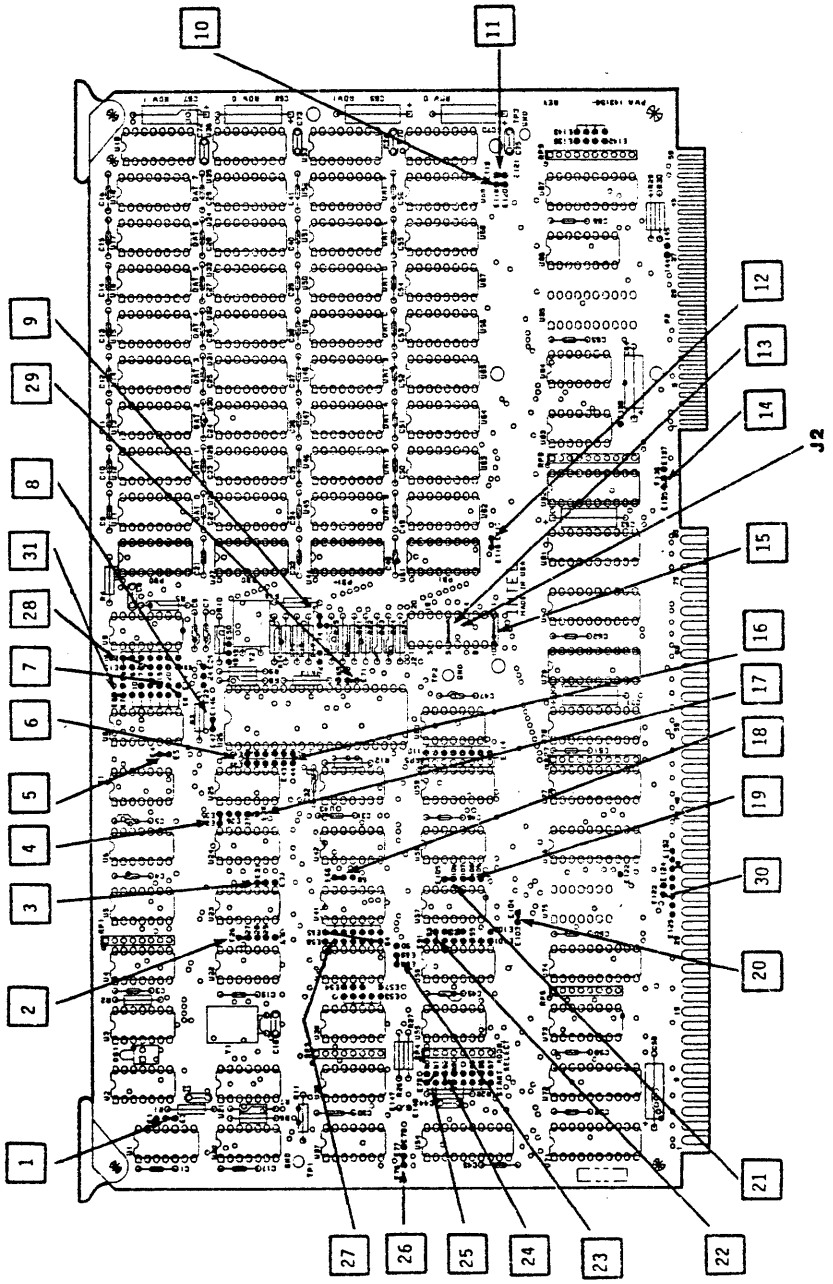
WIRE-WRAP CONNECTIONS

Figure 4-8. Series IV, IEU Board Jumper Configurations



Jumper Connection	Location
E4 - E5	2
E6 - E7	3
E8 - E9	26
E14 - E15	25
E22 - E23	1
E35 - E36	4
E47 - E48	5
E75 - E76	24
E80 - E81	27
E84 - E88	28
E90 - E97	23
E92 - E99	22
E93 - E100	21
E94 - E101	20
E95 - E102	18
E96 - E103	14
E106 - E107	12
E109 - E111	7
E116 - E117	29
E118 - E120	6
E121 - E123	8
E125 - E126	9
E128 - E129	9
E130 - E131	19
E135 - E136	15
E139 - E138	16
E141 - E142	17
E145 - E146	13
E164 - E166	10
E165 - E167	11
E170 - E171	11

Figure 4-9. Series IV, SPU Board Jumper Configurations



Jumper Connection	Location
E2 - E3	1
E4 - E5	5
E6 - E7	31
E9 - E13	7
E15 - E22	28
E18 - E22	28
E23 - E24	7
E26 - E27	2
E31 - E32	3
E34 - E35	4
E37 - E38	17
E39 - E45	6
E44 - E46	16
E51 - E52*	32
E47 - E146	8
E64 - E65	27
E66 - E67	18
E70 - E71***	29
E76 - E77	26
E79 - E83**	25
E79 - E82	24
E88 - E89	23
E92 - E93	22
E94 - E95	22
E97 - E98	22
E101 - E102	20
E103 - E104	20
E105 - E106	21
E107 - E108	19
E116 - E117	12
E118 - E120	10
E119 - E121	11
E123 - E127	30
E135 - E136***	14

*JUMPER ONLY ON P.B. #143514

**WITH SPU OPTION THIS JUMPER MOVES TO E79 - E81

***FOR BOARD #143156-059 ONLY. REMOVE: E135 - E136, E70 - E71 ADD: E69 - E70

Figure 4-10. Series IV, 056 RAM Board Jumper Configurations

8. Connect the CRT cable to J1 on the CPIO board (see 3 of Figure 4-6).
9. Slide the RFI shield into place under the flat washers of the five top screws.
10. Tighten the four side captive screws on the RFI shield and then tighten the five top screws.
11. Reinstall the mainframe top cover (refer to Paragraph 4.6).
12. Connect the ac power cable to a three-conductor power outlet and perform the test procedures given in Chapter 3 making sure that the system operation has not been affected.

4.10 Plug-On Jumper Options

Printed wiring assemblies (boards), to be installed in the mainframe card cage, require that plug-on jumper locations be verified to establish the proper configuration. Standard system boards are usually supplied with the plug-on jumpers installed in default locations and only verification of their installation is required. In some cases, (such as the SPU option), an optional configuration is required and jumpers must be adjusted to satisfy requirements. Six extra jumpers are provided in the auxiliary kit.

For most optional boards, plug-on jumper locations are given in a technical manual provided with the board. For some of the more common options, and the standard boards, plug-on jumper locations are given in Figures 4-6 thru 4-10. The jumper locations for all boards should be checked and verified before the boards are installed in the mainframe card cage.

4.11 Down-Load Cable

A down-load cable is provided as part of the system accessory kit. The cable is used to down-load programs from external 8-inch floppy diskettes to the internal 5¼-inch floppy diskettes. The external disk drive must be controlled by a Series I (Model 800), Series II or Series III development system that has an external I/O connector available.

CAUTION

Before connecting or disconnecting the down-load cable, be sure that power to both systems is shut off. Failure to shut off power may result in damage to the cable or connector.

To connect the down-load cable, first shut off power to both systems, then locate the serial I/O channel connectors on both systems. Connect one end of the down-load cable to the Series IV serial I/O channel No. 1 (J19) and connect the other end of the cable to the Series I or Series II serial I/O connector. Reapply power to both systems.

To down-load programs after the cable is connected, first issue a Series I or Series II command to transfer the programs from the 8-inch floppy through the serial channel to the external device (Series IV memory). Then, issue the command to transfer the program from the Series IV memory to the 5¼-inch diskette. Refer to the Series IV Programmers and Users Guide (part of system literature package) for complete information on the commands required to transfer data.

When the program down-loading operation is complete, shut off power to both systems and disconnect the down-load cable.

4.12 Connecting Optional Peripherals

Three 25-pin D-type connectors are provided on the system back panel for connecting peripheral devices. The three connectors are hard wired to the motherboard and the controller circuits are contained on the CPIO and IEU boards. Optional peripheral devices are connected to the system with user supplied cables. One end of the cables must have a connector that mates with the system connectors. The mating connectors are Amphenol Part Number 205208-1 or equivalent.

The system provides connectors for one line printer channel (J20) and two serial channels (J19 and J18). The Line Printer Channel and Serial Channel 1 (J19) are controlled by circuits on the CPIO board. Serial Channel 2 (J18) is cont rolled by circuits on the IEU board. Table 4-3 provides signal names and functions, connector pin assignments and circuit loading characteristics for the Line Printer Channel.

The two serial channels are fully compatible with both the EIA Standard RS-232-C and the International Telegraph and Telephone Consultive Committee (CCITT) Recommendation V.24 (see Table 4-4). For this manual, Data-Terminal Equipment (DTE) is defined as the Series IV system and the Data Circuit-Terminating Equipment or Data Comminication Equipment (DCE) is defined as the external peripheral device that connects to the system. Signal outputs are defined as going from the system to the external device and signal inputs are defined as going from the external device to the system. The term "signal element", as specified in the description Transmitter Signal Element Timing is defined as a binary data bit. The signal voltage levels are as follows:

1. The marking of OFF condition is more negative than −3Vdc.
2. The spacing or ON condition is more positive than +3Vdc.
3. The area between −3Vdc and +3Vdc is an unspecified transition region.
4. All voltage levels are given with respect to signal ground.

Circuit loading characteristics for both serial channels are defined by the specific ation for the output and input drivers, SN75188 and SN75189. These drivers are designed to meet all requirements of the EIA RS-232-C specification. Table 4-5 provides connector pin assignments and signal identifications, names and descriptions for both serial channels.

CAUTION

Shut off system power before connecting or disconnecting peripheral cables. Failure to shut off power when connecting or disconnecting cables may cause damage to the connectors or sensitive electronic parts.
Extreme care should be taken NOT to plug a line printer cable into a serial channel connector. Safeguards have been installed but, damage could still occur.

Table 4-3. Line Printer Connector J20 Pin Assignments

Pin No.	Signal	Function	Current Drive		Current Load		Termination in Ohms
			Low (I_{OL})	High (I_{OH})	Low (I_{IL})	High (I_{IH})	
1	LPDATA0	Output Data Bit 0 **NOTE** For pins 1-8, high is a binary 1 and low is a binary 0. The coding format is ASCII for characters and control functions.	24mA	−15mA	—	—	—
2	LPDATA1	Output Data Bit 1	24mA	−15mA	—	—	—
3	LPDATA2	Output Data Bit 2	24mA	−15mA	—	—	—
4	LPDATA3	Output Data Bit 3	24mA	−15mA	—	—	—
5	LPDATA4	Output Data Bit 4	24mA	−15mA	—	—	—
6	LPDATA5	Output Data Bit 5	24mA	−15mA	—	—	—
7	LPDATA6	Output Data Bit 6	24mA	−15mA	—	—	—
8	LPDATA7	Output Data Bit 7	24mA	−15mA	—	—	—
9–12	GND	Logic Ground					
13	FAULT/	Printer Error. A low (binary 0) indicates a condition such as paper empty, deselect, or platen open.	—	—	−.02mA	.02mA	470
14	DATASTB/	Data Strobe. A low to high transition clocks data from the controller to the printer.	24mA	−15mA	—	—	—
15	GND	Logic Ground					
16	ACKNLG/	Data Acknowledge. A low to high transition indicates that the current character was received or the current instruction was implemented.	—	—	−.02mA	.02mA	470
17	BUSY	Printer Busy. A high (binary 1) indicates the printer is not ready to receive new characters.	—	—	−.02mA	.02mA	470
18	GND	Logic Ground					
19	PRIME/	Printer Reset. A low to high transition resets the printer logic.	24mA	−15mA	—	—	—
20	N/C	No Connection					
21	GND	Logic Ground					
22	SELECT	Printer Select. A high (binary 1) indicates the printer switch is closed, the printer is loaded with paper, and the platen is closed.	—	—	−.02mA	.02mA	470
23	GND	Logic Ground					
24	+5Vdc	Power for logic circuits					
25	GROUND	Chassis Ground					

Table 4-4. Serial Channels 1 (J19) and 2 (J18) Pin Assignments

Pin No.	RS-232-C Circuit	C.C.I.T.T. Equivalent	Signal Name	Signal Description
1	AA	101	CHASSIS GROUND	Protective Ground.
2	BA	103	TRANSMITTED DATA (Data Output)	Data on this pin are normally transmitted to an external device. The line can be jumpered to configure either serial channel as a transmitter or receiver, and also to provide loop back capability.
3	BB	104	RECEIVED DATA (Data Input)	Data on this pin are normally received from an external device. The line can be jumpered to configure either serial channel as a receiver or a transmitter, and also to provide loop back capability.
4	CA	105	REQUEST TO SEND (Control Output)	A high level (ON condition) indicates data is ready to transmit. Data is not transmitted until a CLEAR TO SEND is received.
5	CB	106	CLEAR TO SEND (Control Input)	A high level (ON condition) indicates that the external device is ready to receive transmitted data. The CCITT recommendation calls this signal READY FOR SENDING. Jumper options on both serial channels allow the system to accept external clear-to-send (CTS) signals or to provide internal (self-generating) CTS signals. For Serial Channel 1, the CTS signal can be controlled by the program (software).
6	CC	107	DATA SET READY (Control Input)	A high level (ON condition) indicates that the external device is connected and ready to communicate with the system.
7	AB	102	LOGIC GROUND	Signal Ground (Common Return).
8	CF	109	RECEIVED LINE SIGNAL DETECTOR (Control Input)	This line can be activated by a jumper or Serial Channel 1 only. If activated, a high level (ON condition) indicates that no signal is being received or the received signal is unsuitable for demodulation.
9, 10	—	—	No Connection	Reserved for data set testing.
11	—	126	SELECT TRANSMIT FREQUENCY (Control Output for CCITT only)	This signal selects one of two transmit frequencies. A low level (OFF condition) selects the lower frequency and a high level (ON condition) selects the higher frequency. The signal is programmable for serial channel 1 and jumper selectable (normally low) for Serial Channel 2.
12	SCF	122	No Connection	Not Used.
13	SCB	121	No Connection	Not Used.
14	SBA	118	No Connection	Not Used.
15	DB	114	TRANSMIT CLOCK IN (Clock Input)	This Transmitter Signal Element Timing signal is jumper selectable to be received from the external device or an internal clock source. For Serial Channel 1 it is normally jumpered to accept the external clock, and for Serial Channel 2 it is normally jumpered to accept the internal clock. In either case, a low to high level transition (OFF to ON condition) causes data to be output on the TRANSMITTED DATA LINE.
16	SBB	119	No Connection	Not Used.

Table 4-4. Serial Channels 1 (J19) and 2 (J18) Pin Assignments (Cont'd.)

Pin No.	RS-232-C Circuit	C.C.I.T.T. Equivalent	Signal Name	Signal Description
17	DD	115	RECEIVE CLOCK (Clock Input for Synchronous Operation)	This Receiver Signal Element Timing signal is jumper selectable to be received from the external device or an internal clock source. For Serial Channel 1 it is normally jumpered to accept the external clock, and for Serial Channel 2 it is normally jumpered to accept the internal clock. In either case, a high to low level transition (ON to OFF condition) nominally marks the center of each data bit on the RECEIVED DATA line.
18	—	—	No Connection	Unassigned.
19	SCA	120	No Connection	Not Used.
20	CD	108.2	DATA TERMINAL READY (Control Output)	A high level (ON condition) indicates the system is ready to transmit or receive data. A jumper in this line allows it to be active or inactive (unjumpered). Normally Serial Channel 1 is active and Serial Channel 2 is inactive.
21	CG	110	No Connection	Not Used.
22	CE	125	No Connection	Not Used.
23	CH	111	DATA SIGNALLING RATE SELECTOR (Control Output)	This signal selects one of two data signalling rates for a dual-rate modem. A high level (ON condition) selects the higher of the two rates, and a low level (OFF condition) selects the lower of the two rates. The signal is programmable for serial channel 1 and is jumper selectable (normally low) for Serial Channel 2.
24	DA	113	TRANSMIT CLOCK OUT (Clock Output for Synchronous Operation)	This Transmitter Signal Element Timing signal is provided by an internal clock for Serial Channel 1, and for Serial Channel 2 may be provided either internally or externally depending upon the jumper for TRANSMIT CLOCK IN. On this line, a high to low transition (ON to OFF condition) nominally marks the center of each data bit on the TRANSMITTED DATA line.
25	—	—	+12Vdc	Load not to exceed 50mA.

CHAPTER 5
SERVICE INFORMATION

5.1 Introduction

This chapter provides basic troubleshooting information and instructions on how to obtain service and repair assistance.

5.2 Basic Troubleshooting

When the mainframe is powered up, ac power is routed through the line filter and power circuit breaker switch to the main (multi-output) power supply, 5 Vdc auxiliary power supply and the three cooling fans. Within 20 seconds, the system will normally complete the power-up test and display the sign-on message. Completion of the power-up test indicates that most of the system is operational. Following initial installation, installation of an option or when a malfunction is suspected, the confidence test is performed to provide more thorough testing and to test circuits that were not tested by the power-up test. If the system should fail to boot up properly, or if any of the tests should fail, refer to the troubleshooting guide in Table 5-1.

To use Table 5-1, first locate the symptom (first column) that most closely defines the error or malfunction. Then read across the table to see what the possible cause or causes could be and what corrective action is required. After performing the corrective actions, restore the system to its operating configuration (top cover in place, etc.) and repeat the failed tests. If the test continues to fail, request assistance from Intel Customer Service (refer to Paragraph 5.4).

If power-up tests that check memory (on board RAM) should fail, the system will display an error message that contains a location number.

For example:
```
FAILED TEST #4
LOCATION EC5A
```

The location number indicates the memory address where the failure occurred. This is useful information in determining the cause of failure. If assistance from Intel Customer Service is subsequently requested, be sure to include the location information in the trouble report.

Table 5-1. Series IV, Troubleshooting Guide

Symptom	Probable Cause	Corrective Action
Fans not running at power up.	No ac at power outlet.	Check power outlet for proper voltage connection.
	Circuit breaker.	1. Turn circuit breaker off then on again. 2. If circuit breaker was tripped and trips a second time, disconnect the ac power cord and request assistance from Intel Customer Service (refer to Paragraph 5 4).

Table 5-1. Series IV, Troubleshooting Guide (Cont'd.)

Symptom	Probable Cause	Corrective Action
	Loose connections at power supply terminal TB1.	1. Turn circuit breaker off and unplug ac cord. 2. Remove top cover (refer to paragraph 4.6). 3. Check connections to TB1 on the power supply behind the CRT (see Figure 4-4).
Failed power-up	CPIO failure. Board jumpers missing or in wrong place.	1. Remove and reinstall test. CPIO board (refer to paragraph 4.9). 2. Check jumpers on CPIO board. 3. If problem remains, request assistance from Intel Customer Service (refer to Paragraph 5.4).
Failed optional board (such as SPU) power-up.	Loose Connection between optional board and motherboard.	1. Reseat board that failed by removing and reinstalling to Paragraph 4.9). 2. If problem continues, contact the Intel Service Representative.
System will neither boot from diskette nor run confidence test.	Configuration switch settings.	Check configuration switches (refer to Paragraph 3.3).
	Loose cable connection.	1. Turn off circuit breaker and unplug ac cord. 2. Remove top cover (refer to Paragraph 4-6). 3. Check floppy disk cable connections J11 and J22 (see Figures 5-1 and 4-1). 4. Reseat CPIO board by removing and reinstalling (refer to Paragraph 4.9).
CRT Blank.	CRT failure.	1. Turn off circuit breaker and remove ac cord from wall socket. 2. Remove top cover (refer to Paragraph 4-6). 3. Check video cable that connects between the motherboard (J23) and the video circuit board and the CPIO board top edge connector (see Figure 5-1). 4. Reseat the CPIO board by removing and reinstalling (refer to Paragraph 4-9).
	Brightness Control	Adjust the brightness control.
Failed 0000H to 0003H of SIVDIA	CPIO board failure.	1. Reseat CPIO board by removing and reinstalling (refer to Paragraph 4-9). 2. Check CPIO jumpers (see Figure 4-7).
Failed Confidence Test 0007H of SIVDIA.	Keyboard failure.	Check keyboard connection to the mainframe.

Table 5-1. Series IV, Troubleshooting Guide (Cont'd.)

Symptom	Probable Cause	Corrective Action
Failed Confidence Test 0008H of SIVDIA.	IEU board failure.	Reseat IEU by removing and reinstalling (refer to Paragraph 4-9).
Failed Confidence Test 0009H of SIVDIA.	CPIO board failure.	Reseat CPIO by removing and reinstalling (refer to Paragraph 4-9).
Failed Confidence Test 000Ah of SIVDIA.	Line printer failure.	1. Check line printer for ac power connection, power switch on and printer operation (refer to printer manual). 2. Check line printer cable connection to the mainframe (J20). 3. Reseat the CPIO board by removing and reinstalling (refer to Paragraph 4-9). 4. Check CPIO board jumpers (see Figure 4-7).
Failed Confidence Test 000BH & 000CH of SIVDIA.	Floppy disk or disk drive failure.	1. Turn off circuit breaker and unplug ac cord. 2. Remove top cover (refer to Paragraph 4-6). 3. Check floppy disk cable connections J11 and J22 (see Figures 5-1 & 4-1). 4. Check that drive being tested has a formatted blank diskette inserted.
Failed Confidence Test 0015H.	CPIO board failure.	Reseat the CPIO board by removing and reinstalling (refer to Paragraph 4-9).
Failed a Confidence Test between 0000H and 000CH of SIVDIA.	Loose connection between IEU board and motherboard.	1. Reseat the IEU board by removing and reinstalling (refer to Paragraph 4-9). 2. Check IEU board jumpers (see Figure 4-8).
Failed a Confidence Test between 0000H and 0007H of SIVEXT.	Expansion (extra) memory failure.	1. Remove the failing memory board (refer to Paragraph 4-8). 2. Check failing memory board for proper jumper configuration (see Figure 4-10). 3. Reinstall and retest memory board.
Failed a Confidence Test between 000DH and 0014H of SIVDIA.	SPU board failure.	1. Reseat the SPU board by removing and reinstalling (refer to Paragraph 4-9). 2. Check SPU board jumpers (see Figure 4-9).

5.3 Preventive Maintenance

The mainframe and keyboard require the same care and maintenance given to an electronic computer terminal equipment. To maintain the equipment properly, perform the following steps routinely in manufacturing environments:

1. Clean the outside of the mainframe cabinet and keyboard with any high quality (non-solvent, non abrasive) office cleaner such as 3M Desk and Office Cleaner,

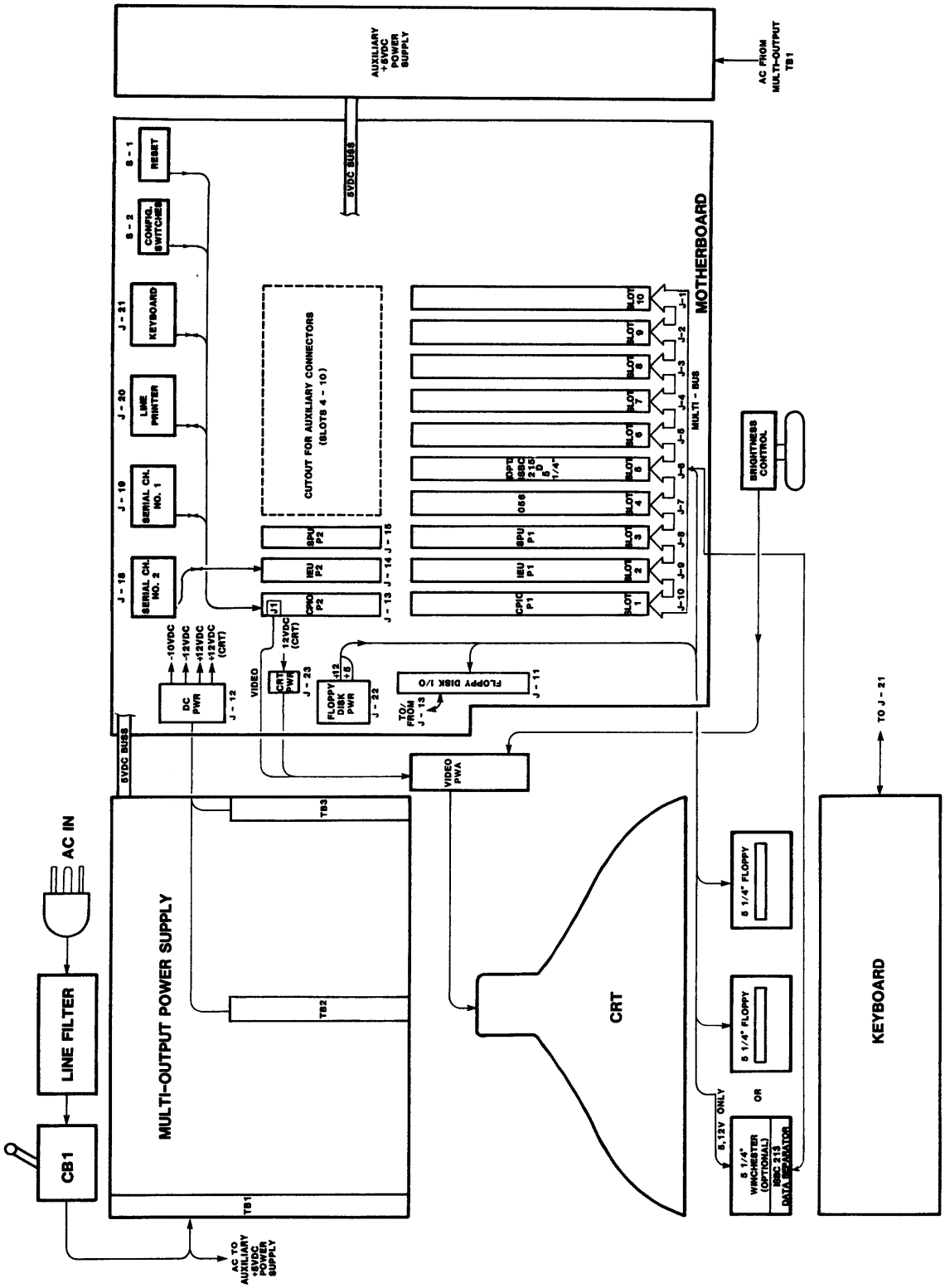


Figure 5-1. Series IV, Mainframe Internal Connections

Catalog No. 573 or equivalent and a soft, lint-free cloth. Use cleaners sparingly. Always apply cleaners to the cloth first and then wipe equipment.

DO NOT allow cleaners to enter mainframe or keyboard openings or get into the disk drives. If cleaners get on printed circuit boards or in the disk drive, short circuits or serious damage could occur.

2. Clean the CRT screen with any high quality, non abrasive glass cleaner, such as Windex and a soft, lint-free cloth. Use cleaner sparingly. Always apply cleaner to the cloth first and then wipe the screen.
3. Check around the equipment to maintain proper air circulation for cooling (refer to Paragraph 2.3).
4. Perform the Confidence Test to ensure that all circuits are functioning (refer to Paragraphs 3.16 to 3.21).

5.4 Service and Repair Assistance

The best service for your Intel product will be provided by an Intel Customer Engineer. These trained professionals provide prompt, efficient on-site installation, preventive maintenance or corrective maintenance services that will keep your equipment in the best possible operating condition.

Your Intel Customer Engineer can provide the service you need through a prepaid service contract on an hourly charge basis. For further information, contact your local Intel office.

When it is impossible for you to use the services of an Intel Customer Engineer or when Intel service is not available in your local area, you can contact the Intel Service Center directly at one of the following numbers:

Telephone:

From Alaska, Arizona or Hawaii call:
(1-602) 869-4600

From all other U. S. locations call toll free:
(1-800) 528-0595

TWX: 910-951-1330

NOTE

Customers outside of the Continental United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

5.5 Reshipment

Never return equipment to Intel for service or repair before you contact an Intel Customer Engineer or the Intel Service Center.

If return of your equipment is necessary, you will be given a Repair Authorization Number, shipping instructions and other important information that will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment or if the product is out of warranty, a purchase order is necessary in order for the Intel Service Center to make the repair.

CAUTION

Before shipping the system: recalibrate the heads by running the diagnostic test SIVDIA, Floppy Disk Seek Test 000BH. If possible protect the heads by inserting the original floppy drive head protector (cardboard insert), into the drive. Close the latch.

When preparing the product for shipment to the Service Center, use the original factory packaging material if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Gap SD-240, manufactured by the Sealed Air Corporation, Hawthorne, NJ (or equivalent) and enclose a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling and ship it to the address specified by the Intel Service Center.

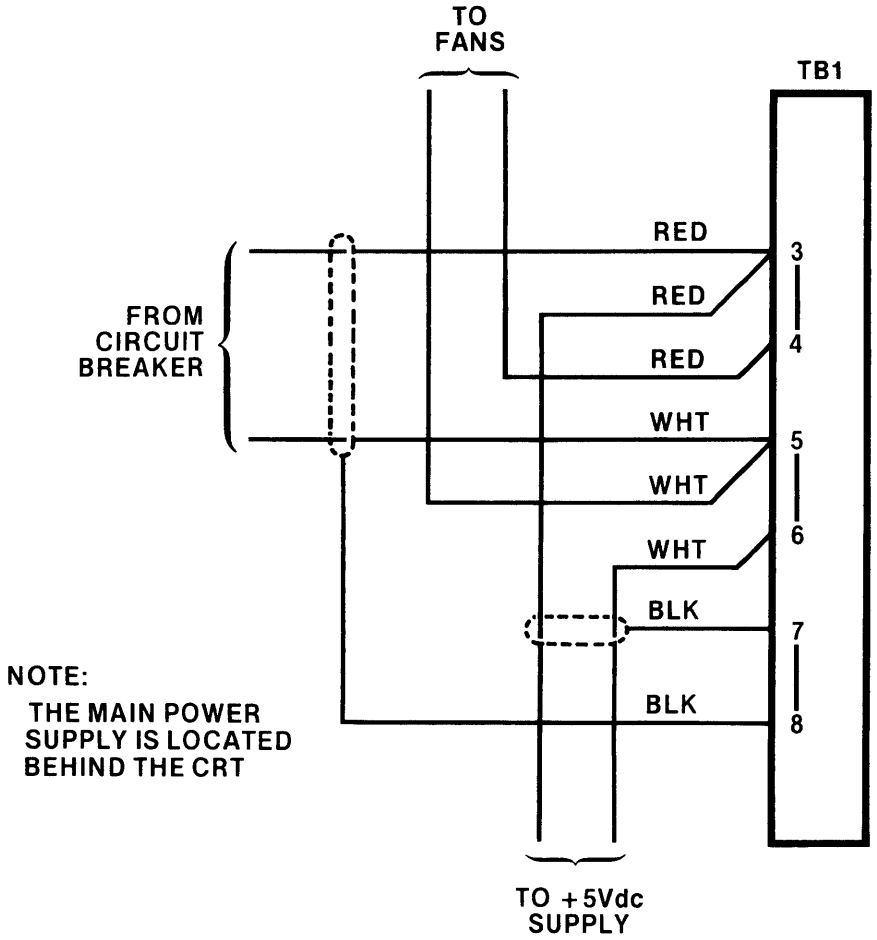


Figure 5-2. Series IV, AC Power Connections on the Main Power Supply

APPENDIX A
TEST MONITOR COMMAND DESCRIPTIONS

A.1 Introduction

This chapter explains the Test MONitor (TMON) commands of the DETMON syntax. TMON is the interface software between the user and the diagnostics. TMON provides a test suite, not a debug environment.

Each TMON command is described, shown with proper syntax and demonstrated with examples as actually used.

The TMON commands are:

CLEAR
DESCRIBE
EXIT
IGNORE
RECOGNIZE
SUMMARY
TEST

A.2 Console Interface

The console interface supports the standard ISIS console commands. This section contains a table (Table A-1) of keyboard control special action characters. These commands provide the CE with error correction, display and I/O control between the keyboard and the monitor.

The symbol "^" preceeding a term, means that the "CNTL" key must be held down before the term key is pushed.

A.3 TMON Definitions

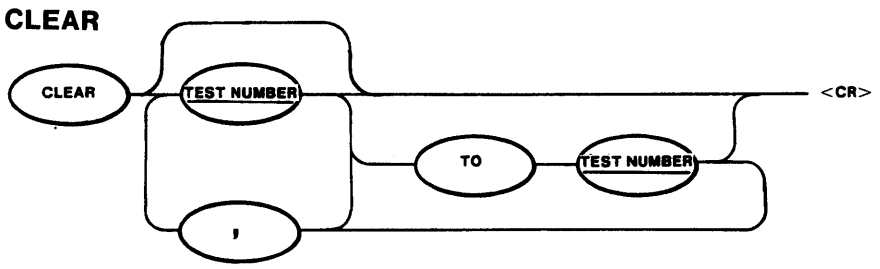
This section contains a one page definition of each command in the TMON test suite. Each page contains a flowchart of the actual key-in language, examples of use, a description of what the command actually does and pertinent error message information.

Table A-1. Series IV, Console Control Commands
CONSOLE CONTROL COMMANDS

SYMBOL	DEFINITION	DESCRIPTION
RUBOUT		Delete the previous character
^Z	CONTROL Z	End of file
^X	CONTROL X	Delete the entire input line
^R	CONTROL R	Echo and correct the input line
^P	CONTROL P	Input next character literally
^C	CONTROL C	Delete input line and abort command instruction
<cr>	CARRIAGE RETURN	End of line
LF	LINE FEED	End of line
^S	CONTROL S	Pause the display of the output
^Q	CONTROL Q	Resume the display of the output

CLEAR

Syntax:



Examples:

*CLEAR<cr>

or

*CLE<cr>

or

*CLEAR 10<cr>

Description:

Clear purges the test summary table. The summary indicates the number of times the diagnostic(s) has been executed and how many times each test failed. This command destroys the old results.

Error Message:

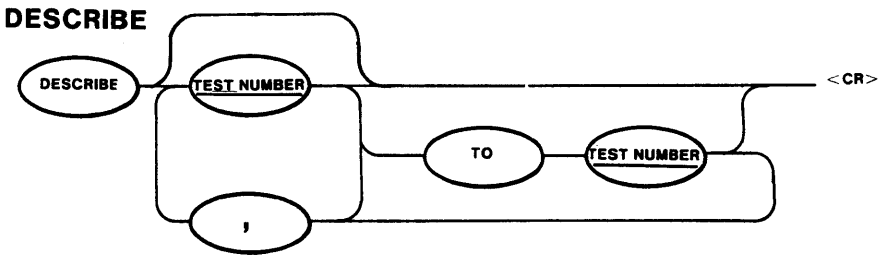
TEST OUT OF RANGE

The command specified a test outside the range of the test description table.

(*) DETMON curser, signals the user that development system will accept input from the keyboard.

DESCRIBE

Syntax:



Examples:

*DES<cr>

or

*DESCRIBE 0,1,2<cr>

or

*DESCRIBE 1 TO 20<cr>

Description:

DESCRIBE displays the name and operational status of the test programs incor porated in the diagnostic, and flags unavailable tests as "IGNORED". The names of the tests indicate that portion of the circuitry being tested. This command describes all test if no particular test(s) is specified.

Error Message:

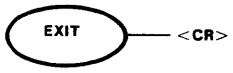
TEST OUT OF RANGE

A specified test exceeds the top range of the test description table.

EXIT

Syntax:

EXIT



Example:

*EXIT<cr>

Description:

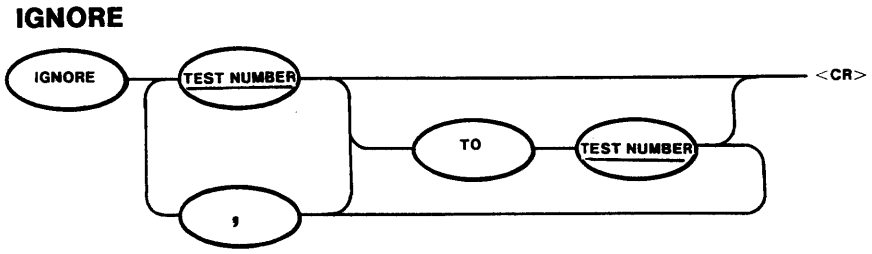
This command transfers control from TMON back to the Software Diagnostic Monitor, indicated by the prompt ">". Once under the control of the Software Diagnostic Monitor, another test suite can be loaded or a directory of the test suite names can be displayed.

Error Message:

None

IGNORE

Syntax:



Examples:

```
*IGNORE 2,4,12 TO 17<cr>
```

Description:

Ignore disables any undesired test in the test descriptor table. The ignored test will not be tested. The "RECOGNIZE" command enables those tests previously ignored (see RECOGNIZE test.).

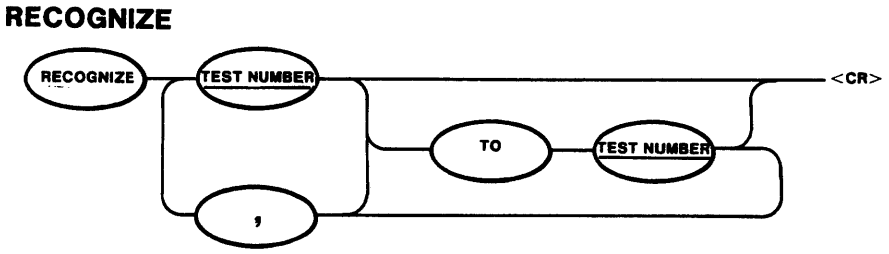
Error Message:

```
TEST OUT OF RANGE
```

A test has been specified which exceeds the top range of the test description table.

RECOGNIZE

Syntax:



Examples:

```
*REC 2,4,6 TO 8<cr>
*REC<cr>
```

Description:

This command enables tests previously ignored (see IGNORE). REC enables all tests unless a range is specified, and than enables only those tests specified.

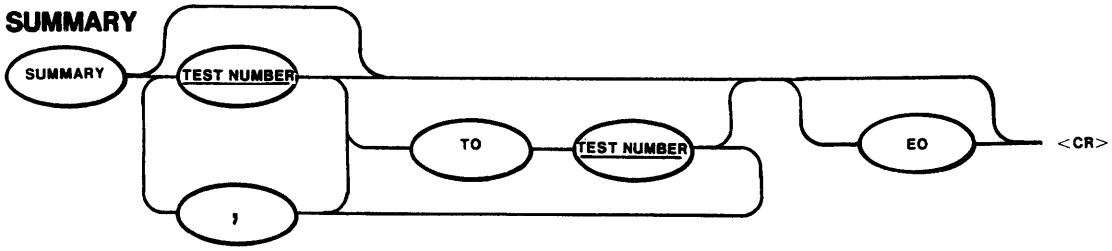
Error Message:

```
TEST OUT OF RANGE
```

A test has been specified which is greater than the index of the last test in the test description table.

SUMMARY

Syntax:



Examples:

```
*SUMMARY EO<cr>
0001H FOO TEST          0000H PASSED 0003 FAILED <***

*SUM *<cr>
0001H FOO TEST          0000H PASSED 0003 FAILED <***
```

Description:

This command displays and labels both ignored and active tests. For active tests, the log indicates the number and name of the test, followed by the number of times it was tested and the number of passes and failures. Ignored tests are labeled "IGNORED".

The error only (EO) in the syntax will cause the summary to display only those tests that have failed.

Error Message:

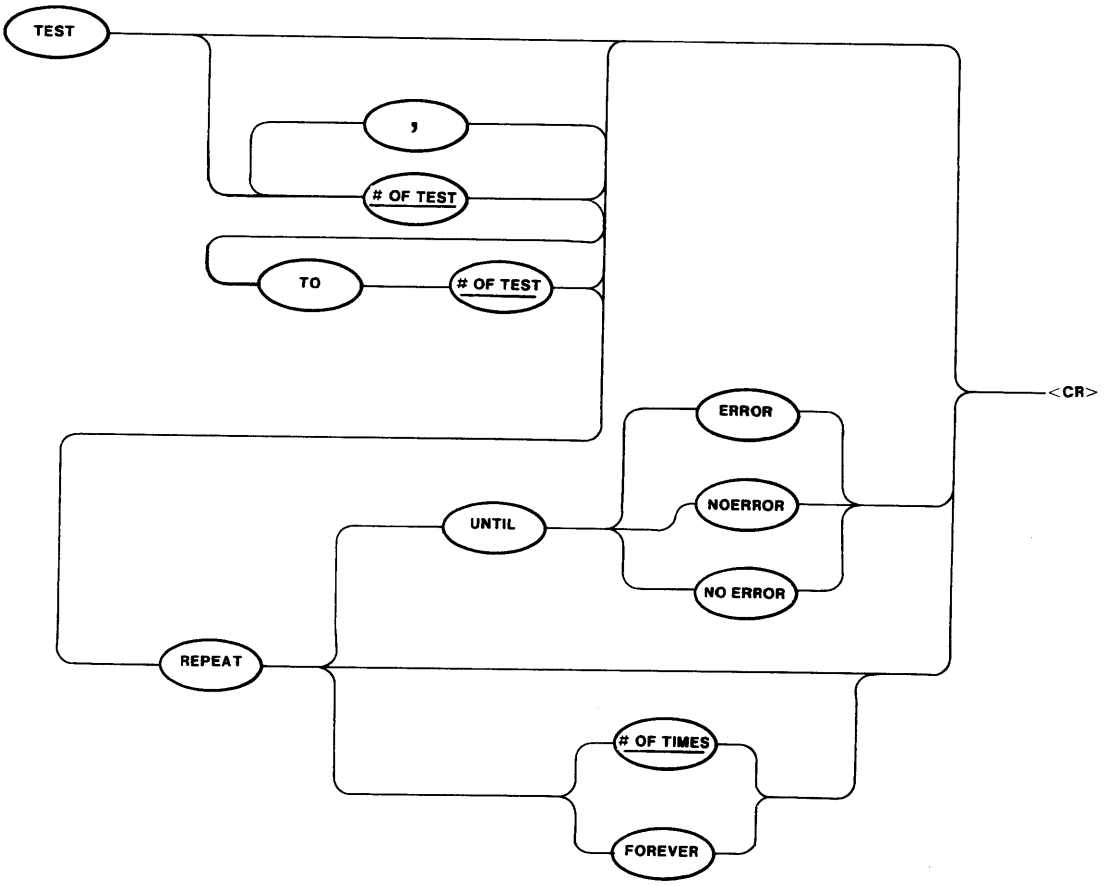
```
TEST OUT OF RANGE
```

A test exceeding the top range of the test description table has been specified.

TEST

Syntax:

TEST



Examples:

*T <cr>
(The condition of all non-ignored tests are displayed. All non-ignored tests are tested.)

*T 1,3 TO 40 REP FOR<cr>
(Tests 1 and 3 to 40 are displayed until interrupted by user.)

*T 12 REP ON ERROR<cr>
(The results of Test 12 are displayed as long as it fails.)

*T REPEAT 500T<cr>
(The execution of all non-ignored tests, tested according to the TEST command sequence, 500 times, is displayed.)

Description:

The test command initiates the test sequence and displays the name of the test(s) executed and the results of that testing. Tests may be activated by the "RECOGNIZE" and deactivated by the "'IGNORE" command. Ignored tests are not tested. The "DESCRIBE" command displays the status of the tests.

The test range entered by the user, determines which active tests are executed.

Error Message:

TEST OUT OF RANGE

A test has been specified which exceeds the top range of the test description table.

A.4 TMON Error Message

TMON displays an error message whenever the desired TMON command addresses a location outside the user defined limits. The error message intepretation is:

```
TEST OUT OF RANGE
```

A test has been specified which is greater than the last test indicated in the test description table. This error message is associated with the IGNORE, CLEAR, RECOGNIZE, SUMMARY, TEST, and DESCRIBE commands.

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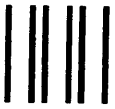

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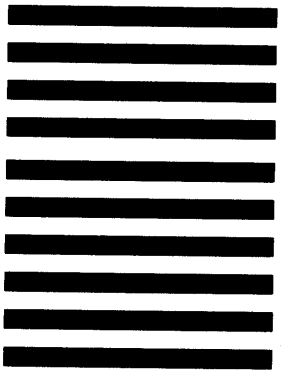

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