T A B L E O F C O N T E N T S

KLEEMAN
16 ANNING WAY,
NEW INN YARD
LONDON, ENGLAND

INDUSTRIAL MICRO SYSTEMS, INC.

CP/M 2.2 IMPLEMENTATION GUIDE

For the Series 8000 and Series 5000 systems

including the CMD hard disk sub-system

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Manufacturing:
2800 Lockheed Way
Carson City, Nevada 89701

Sales and Engineering:
628 N. Eckhoff Street
Orange, California 92668

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1.0 CP/M 2.2 IMPLEMENTATION

The Industrial Micro Systems implementation of CP/M 2.2 for the Series 5000 and Series 8000 includes the support of a CMD hard disk sub-system and extended accessing capabilities for double-density and double-sided diskettes.

1.1 Floppy disk based systems

The Series 8000 will support these three diskette formats:

Single-density, single-sided (IBM 3740)
Double-density, single-sided
Double-density, double-sided (see note below)

A single-density, double-sided 8" format is not supported because it essentially has the same storage capacity as the double-density, single-sided format.

The Series 5000 version will support two diskette formats:

Double-density, single-sided
Double-density, double-sided (see note below)

Note: The system must contain double-sided drives to support the double-sided format.

A single-density 5" format is not supported.

In floppy disk based CP/M systems, the operating system is designed to reside on the first two tracks of a double-density diskette. The diskette may be double-sided also.

The storage and directory capacities for the Series 8000 and Series 5000 diskette formats are:

diskette format	total storage	directory entries	min. block size
SERIES 8000			
single-density	243 kb	64	1 kb
double-density	486 kb	128	2 kb
double-sided	972 kb	256	4 kb
SERIES 5000			
double-density	152 kb	64	1 kb
double-sided	304 kb	64	2 kb

The BIOS automatically determines the diskette format in its first access to a drive. If after accessing a drive, it is desired to change the diskette format in that drive, a warm boot (Control C) must be executed. For example, if a single-density diskette was first accessed in a drive, and it was desired to replace that diskette with a double-density formatted diskette, a warm boot would be required. If a double-density, double-sided diskette was first accessed in a

double-sided drive, and it was desired to change the media to double-density, single-sided, a warm boot would be necessary.

In the Series 8000 system, for double-density and double-sided formats, there are differences in structure of the directories between Industrial Micro Systems' CP/M 1.4 and CP/M 2.2. Under CP/M 2.2, a directory entry can control multiple 16K extents, which reduces directory searching and speeds up the system. Single-density formats are fully compatible in directory structure between CP/M 1.4 and 2.2 and can be read or written on the system using either version of CP/M.

There is a point regarding CP/M 2.2 which needs to be communicated and well understood by the user. That is, for double-density files created under CP/M 1.4 that are greater than 16K bytes in length, the DIR command will yield two directory listings for these files and four listings in the case of double-sided files. These files are not directly compatible for operation under CPM 2.2 due to differences in the directory structures. A utility program, TRANS14, has been written and is included on the diskette. This program will be discussed in more detail later; however, in summary, TRANS14 allows one disk drive in the system to be selected for reading and writing using the CP/M 1.4 directory structure.

In the Series 5000 system, double-sided capabilities were not supported with CP/M 1.4. The directory structure of single-sided diskettes created under CP/M 1.4 is fully compatible with CP/M 2.2, therefore there will be no 1.4-to-2.2 incompatibilities for the Series 5000.

PIP and STAT have both changed for CP/M 2.2 and care should be taken to use the new version with CP/M 2.2.

Caution should be exercised with the use of programs that call BIOS directly for disk operations. Information about the BIOS jump table as well as the BIOS source listing are contained in this document and will aid in tailoring these programs to run on the system.

The double-density formats in both the Series 8000 and 5000 use physical 256 byte sectors which are blocked and deblocked through the BIOS to support reading and writing of 128 byte logical sectors. A 256 byte buffer for these double-density sectors is maintained in the BIOS area of the system. Care should be taken to insure that records written to this buffer are updated on the diskette. Open files must be closed before a diskette may be removed! This is accomplished by always closing files in application programs prior to returning to a point where a diskette may be removed or by returning control to CP/M by executing a warm boot (Control C).

The IMS CP/M contains a modification of BDOS for the handling of errors and provides extensive read/write error messages. When a permanent disk error is encountered, BIOS will print its error message followed by a BDOS prompt. Typing a return will ignore the error and continue, while typing a Control C will warm boot the system and leave drive A selected. If an attempt is made to access a drive which is not physically present on the system or during the first access to a drive, the BIOS finds the drive not reading or cannot determine the format of the diskette inserted, a BDOS select error prompt is printed on the console. Typing any key will perform a warm boot and leave drive A selected. Once the BIOS has made the first access to a drive and the format of the diskette is successfully found, further access to this drive with the diskette removed will produce a "DRIVE x NOT READY" error message to be printed on the console (where x is the drive number 0 to 3 corresponding to the CP/M devices A to D). If the diskette is re-inserted, the BIOS automatically senses the drive becoming ready again and continues with its accessing without any user interaction at the console. Typing any key will perform a warm boot and leave drive A selected.

Parity error detection for the IMS Model 460 64k dynamic memory board has been implemented with the new release of the BIOS. When a parity error is detected, all of memory is

re-initialized and the Model 460 parity error is reset, the current console activity is interrupted and this message is printed on the console:

PARITY ERROR, IGNORE?

If a "Y" response is typed, the interrupted program will continue where it was stopped, and if any other response is typed, a system warm boot is performed. Note that if the parity error occurred within the BIOS portion of the system a warm boot may not be sufficient to fully restore the system. A cold boot, however, will reload the entire operating system.

1.2 CMD Hard disk based systems

A CMD hard disk sub-system may be added to either the Series 8000 system or the Series 5000 system, thus creating a hard disk based operating system designed to reside on the removable cartridge in the CMD drive. The CMD drives are referred to by their unformatted storage capacities (32, 64, and 96 megabytes). All CMD drives contain one removable cartridge with an unformatted storage of 16 megabytes (referred to as cartridge from here on), plus fixed unformatted storage of 16, 48, or 80 megabytes (referred to as fixed from here on). The cartridge is referred to as Volume 0 and the fixed as Volume 1 by the drive manufacturer.

In CMD hard disk based CP/M systems, multiple CP/M logical devices are used to describe the entire drive. Device A and B are always the cartridge while the fixed is defined as device C through device L. Each CMD drive's storage capacity is based on the size of the drive in unformatted megabytes.

The BIOS for the CMD hard disk based system is upward compatible with floppy disk format for the floppy based system. All diskette formats and a total of four drives are supported by the BIOS. The four floppy disk devices directly follow the hard disk devices with each drive size. After initial system loading and execution, a driver initialization is performed to determine the size of the hard disk and set the CMD and floppy devices. As a convenience, the range of CMD and floppy devices are printed on the console along with the sign-on message. The CP/M logical device assignment based on drive size is as follows:

The CMD hard disk controller and drive use a 512 byte sector format which is blocked and deblocked similar to double-density floppy disks. The buffer for the CMD sector is located on the controller so system memory need not be used. Reading and writing to this buffer is done by DMA through a channel on the floppy disk controller board (either the Model 400 or 430). All the same rules apply here as they do in double-density floppy based systems for insuring the buffer has been updated on the disk.

Caution should be used when changing CMD cartridges. To be safe, cold boot the system whenever a new cartridge is inserted, or at least be double sure to type a Control "C".

The CP/M logical device assignment based on drive size is as follows:

CMD drive size	cartridge	fixed	floppy drives
32 megabyte	A and B	C and D	E thru H
64 megabyte	A and B	C thru H	I thru L
96 megabyte	A and B	C thru L	M thru P

Due to the sub-division of the CMD drive as to CP/M logical devices, CMD device capacities vary in size as shown by this table:

CMD device	total storage	directory entries	min. block size
A	6560 kb	512	8 kb
C,E,G,I & K	6576 kb	512	8 kb
B,D,F,H,J & L	6592 kb	512	8 kb

The same control for BDOS and BIOS error messages as described in the floppy based system apply in the CMD hard disk based system.

2.0 CP/M START-UP PROCEDURES

2.1 Floppy based CP/M system start-up

The initial start-up of the Series 8000 or Series 5000 floppy based systems consists of the following:

1. Connect any 9600 baud CRT terminal, which requires no special hand-shaking, to the channel 1 serial port.

2. Apply power to the system and the CRT.

3. Insert a double-density CP/M 2.2 diskette in Drive A (the left-most drive). The diskette should be inserted with the label facing right and entering the disk drive last.

4. Close the door of the drive.

5. Loading of the system should begin immediately with the drive activity light on and the sound of the head loading onto the diskette.

   For CP/M 2.2 the standard IPL EPROM included in Series 8000 and 5000 systems does not prompt for the system load (See Appendix C). The system should sign on with:

   ```
   Industrial Micro Systems
   32K CP/M vers 2.2 of 80Mar12
   Series 8000    (or Series 5000)
   ```

If the message doesn't appear, before proceeding, perform the following checks:

1. Verify the terminal cable for standard 3-wire (transmit, receive, and ground) configuration.

2. Make certain that connectors are secure at the terminal and mainframe.

3. Verify CRT compatibility and mode selects through reference to the BIOS listing for word format on the serial port.

4. If the system has had board removals or shuffling in the card cage, make certain that the I/O Board to DB-25 connector cable is in place and that UART0 signals are going to Channel 1.

5. Verify the shunting of the IMS400 (or IMS430) vector interrupt. (See Appendix A)

Now retry the Power-on IPL procedures as described above. If no drive activity occurs, then you may have a double-sided diskette mounted in a single-sided drive or internal hardware failure. If there is drive activity but the head unloads within one second, then one of the following problems may exist:

1. The diskette in Drive A is a single-density diskette.

2. The diskette in Drive A does not contain CP/M on the system tracks.

3. A disk read error occurred in loading the CP/M system.

Series 8000 floppy disk based CP/M systems are supplied on a double-density, single-sided diskette which will load and run on either single-sided drive systems or double-sided drive systems. The standard system diskette is configured to leave the IPL ROM pre-set drive step rate of 6 ms unchanged. In systems with double-sided drives, the step rate should be increased to 3 ms to quiet the noise down from the drive during steps. Read about the program CPMPAT.COM in the Utility Programs section and patch your CP/M relocator file to increase the drive step rate after system execution.

2.2 CMD hard disk based CP/M start-up

Since all software pertaining to the CMD hard disk is supplied on a double-density Series 8000 or 5000 compatible floppy diskette, it is necessary to perform drive initialization procedures that format, build a CMD based system and write the system onto the cartridge. Your CMD hard disk sub-system diskette contains all the programs and files needed to accomplish this. Begin first by reading this entire document and bringing up the floppy based CP/M system, for this system is used to initialize CMD drives and provide back-up in case of hard disk failure. Once this is done, you may insert the Model 490 CMD hard disk controller into the system, if not already there, and connect the cables to the drive. Turn power on the drive, place the cartridge into the drive, and press the start button on the front panel. A list of steps for initialization of the CMD drive follows:

1. Use the CMD hard disk formatting program (explained in System Utilities section below) to format all devices on the CMD drive. Each device will take roughly 10 minutes to format.

2. Use the CMD hard disk based CP/M relocator (MOVCPMHD explained in System Utilities section below) to build the largest possible system that will fit in your memory configuration. Leave the memory image of the system in the TPA and DO NOT run any program that may overwrite this image.

3. Use the IMSHDGEN utility program (explained in System Utilities section below) to write the memory image of the system in the TPA to the CMD cartridge.

4. There are two ways to perform the IPL of the CMD hard disk based operating system. The first is to run the supplied HDBOOT utility program from your floppy based CP/M system, which will load and execute the CP/M system on the CMD cartridge. Secondly, if you have been supplied with the latest revision of the IPL rom (see Appendix C), you may use this rom to boot the system directly from the CMD cartridge by pressing system reset on the front panel or performing a power on sequence. Note: When using the IPL ROM, make sure that a diskette is not inserted in floppy drive 0 or the IPL ROM will attempt to load a system from this floppy drive.

5. Depending upon the size of your CMD drive, floppy devices will begin at E, I, or M. This is printed on the console when CMD based system is up and running. Once you know where the floppy devices are, use PIP to transfer files from floppy diskettes to the CMD devices.

The CMD hard disk based CP/M system initialization has now been completed. To initialize a new CMD cartridge, only format CMD devices A and B of Step 1, then perform Steps 2 through 5 to write a system to the cartridge.

The standard distribution of the CMD hard disk based CP/M system relocator (MOVCPMHD.COM) assumes a drive step rate of 6 ms for single-sided drives. If your system has been supplied with double-sided drives, use the Utility Program CPMPAT.COM (see System Utility Programs section) to patch the relocator to set the floppy disk drive step rate to 3 ms after system execution.

3.0 SYSTEM UTILITY PROGRAMS

This section explains the use of utility programs supplied with the system in addition to the Digital Research transient programs which are covered in the CP/M 2.2 System Features and Utilities Manual provided by Digital Research. Most of these additional programs are unique to this system and will not run on other manufacturers' implementation of CP/M 2.2. The sources for some of these utilities are provided on or with the system diskette and are compatible with Digital Research's "MAC" macro assembler.

3.1 General purpose utility programs

These programs are designed for use with both the floppy based CP/M system and the CMD hard disk based CP/M system.

3.1.0 BAUD.COM - Set printer baud rate

The BAUD program will temporarily set the printer port to a new baud rate specified in the command line when BAUD is loaded at the command level of CP/M. BAUD will only accept the rates 110,150,300,600,1200,4800, and 9600 unless the rate is preceeded by an "@" character, in which case any rate between 110 and 9600 may be specified. Rates other than the checked values may not be precise, due to the base input frequency of the divider that generates baud rates for the uarts. The new baud rate on the printer port will continue until BAUD is run again or the IPL (cold boot) brings the entire system in again. Warm boots will not affect the printer baud rate.

3.1.1 MEMTEST.COM - Memory test utility

This utililty will perform a one pass test on system memory beginning at the end of the program in the TPA (approximately 300H) to the beginning of BIOS. No parameters are needed when the program is invoked at the command level of CP/M 2.2. Once loaded, MEMTEST will begin testing, and after one complete pass a reboot of the system is performed. Errors are displayed with the memory address first, followed by the byte MEMTEST wrote at that location and the byte which was read back. In the case of multiple memory errors, Control-S may be used to stop the display and examine the error. The console is checked for the Control-C break character.

3.1.2 TRANS14.COM - Translate CP/M 1.4 double-density

TRANS14 is a self-relocating program that, when initialized, will force the 1.4 directory structure on one selected drive on the system. The drive is specified at program run time by using any valid drive name (i.e. A:, B:, C:) other than the currently logged in drive. If an attempt is made to make the current drive 1.4 compatible, a "drive name error" is printed on the console. Once a drive is set for 1.4 compatibility, double-density 1.4 diskettes may be accessed with any of the system utilities or application programs.

TRANS14 locates itself right below the CCP in memory and changes the BDOS entry jump at location 5 to point to itself, which will prevent programs which use this jump to find the top of memory from overwriting TRANS14. When this module is installed, it will trap warm boots and print out the message:

(Trans 14 active)
(Drive n: is set for 1.4 compatibility)

Where n stands for the drive specified when TRANS14 was run. The warm boot is then allowed to proceed, so diskettes may be changed without the need to run TRANS14 again. If TRANS14 is run while the module is active in memory, it will clear itself from memory and all drives will again be the 2.2 directory structure. After clearing, the message:

Trans14 cleared, system restored

will be printed on the console. TRANS14.ASM is the source to this program. It is provided for reference only because the files needed to generate the relocating version are not present.

3.1.3 CPMPAT.COM - Patch utility for MOVCPM.COM

CPMPAT allows the user to make limited modifications to the operating system without the necessity of going through a second level generation of the system (explained in the section below). Based on interaction by CPMPAT into the BIOS portion of the operating system, the user can examine and alter the default drive step rate, console and list device baud rates, and enable or disable handshaking with the list device port. CPMPAT informs the user of the current patch it is set up to perform, displays the various options allowed at this level with the current value present, and prompts for a new value. Typing a <RET> only to any input request causes no change to take place. Furthermore, the last prompt issued asks if all previously made changes are correct and typing a "Y" answer will update the CP/M relocator with the new changes.

By the nature of the CPMPAT program, it may only patch CP/M relocators with the new revision of the BIOS. It will check for a valid BIOS and print a TABLE ERROR message if the BIOS is not the new revision. Additional information about this table is in the source of the BIOS. To invoke CPMPAT at the command level of CP/M, use the format:

A>cpmpat movcpm?

where "movcpm?" should be the file name of the relocator COM file that the CPMPAT program will operate with. It is suggested that an original of the issued relocator be put in safe keeping somewhere and operating should be done on a back-up copy of that file.

For systems with the hard disk subsystem, CPMPAT may be used on the relocator for that operating system (usually called MOVCPMHD.COM).

Note that CPMPAT only changes the BIOS contained in the CP/M relocator program and not the system on tracks 0 and 1 or the current system in memory. Therefore, once the relocator has been changed, to integrate these changes into the system, a first level system generation needs to be performed (See section below). CPMPAT.ASM is the source file for this program.

3.2 Floppy based system utility programs

These programs all contain driver level software for the IMS Model 400 and Model 430 disk controllers. They are effective for system level housekeeping, diskette back-ups, or media validation. The source files for these programs contain a conditional assembly switch "MINI" that when set TRUE will generate the Series 5000 (IMS430 5" controller) version or when set FALSE will generate the Series 8000 (IMS400 8" controller) version.

Although the current release of the BIOS for CP/M 2.2 floppy based systems uses interrupts to recover from disk related routines, all the internal drivers within these utilities disable processor interrupts immediately and use polling to recover from disk related routines. When they exit

back to CP/M via the warm boot entry point at 0, processor interrupts are re-enabled by the first disk command.

3.2.0 FORMAT.COM - Diskette Formatting Utility

This program is used to initialize the sector format of a diskette to be used with the IMS CP/M 2.2 system. It should be used on new diskettes to insure their compatibility with the system and may be used to reformat crashed diskettes which cause errors in reading or writing. This program destroys all data on the diskette, so proper care should be taken in recovering the data on crashed diskettes.

There are two versions of the Industrial Micro Systems CP/M 2.2 FORMAT program: one for the Series 8000 formats, and one for the Series 5000 formats. The following tables describe the formatting for all densities and diskette types:

8" DISKETTE FORMATTING

	Single-sided	**Double-sided**
Single-density	77 Tracks 26 Sectors/Track 128 Bytes/Sector	——
Double-density	77 Tracks 26 Sectors/Track 256 Bytes/Sector	2 Sides 77 Tracks/Side 26 Sectors/Track 256 Bytes/Sector

5" DISKETTE FORMATTING

	Single-sided	**Double-sided**
Double-density	40 Tracks 16 Sectors/Track 256 Bytes/Sector	2 Sides 40 Tracks/Side 16 Sectors/Track 256 Bytes/Sector

Both versions first prompt for a drive name (A through D), and the diskette should be inserted into the drive it is to be formatted in. The Series 8000 will issue a density prompt here if a single-sided diskette was inserted. The Series 5000 version will issue a side prompt here if the system has double-sided drives. Both versions issue a last chance prompt, then proceed formatting. During the format process, each track is read after it is formatted to verify the media. The keyboard is checked for a Control-C break character.

The following is an example of executing FORMAT on a Series 8000 with the diskette to be formatted in Drive B.

```
A>format

Industrial Micro Systems
8" Disk format program version 2.0

Type disk (A-D) to format or return to reboot B
Single or Double density (S/D)? D
Format will destroy all data on disk B
Press RETURN to continue or CONTROL-C to abort <RET>
```

After the function is complete, FORMAT will again issue the drive name prompt and RETURN may be typed to reboot CP/M. FORMAT will discontinue formatting on any type of error and return to the drive name prompt. Drive A is always selected after the warm boot. FORMAT.ASM is the source file for this program.

3.2.1 COPY.COM - Diskette Copy Utility

COPY is used to make a track for track direct copy of one diskette to another. The diskettes must be of the same format or COPY will print a format error on the console and warm boot the system. COPY accepts three copying commands, ALL, DATA, or SYSTEM: "COPY ALL" copies the entire disk (tracks 0-76 for the Series 8000 and tracks 0-39 for the Series 5000). "COPY DATA" copies the data and directory from tracks 2-76 for the Series 8000 and tracks 2-39 for the Series 5000. "COPY SYSTEM" will transfer the first two tracks of the diskette which contains the CP/M 2.2 operating system. Source and Destination drives (A thru D) may be specified after the copy command in the format, Destination=Source, or COPY will default to the source on drive A and the destination on drive B. COPY defaults to a read after write verification unless the command line is followed by a "/" character to switch this mode off.

COPY is initiated at the command level of CP/M with the form:

COPY command [Destination=Source] [/]

([ ] = optional)

COPY loads and reprints the source and destination drive, followed by a last chance prompt which accepts a Control-C to reboot CP/M. At this time the diskettes involved in the COPY may be placed into the source and destination drives and RETURN should be used to start the COPY. Any pair of like format diskettes may be placed into the drives even if a drive was previously set for a different format.

Any errors which occur during transfer are printed on the console with the message "IGNORE?". If a "Y" is typed, COPY will continue with the copy. If any other key is typed, COPY will abort and reboot CP/M. The keyboard is checked for the Control-C break character. After the transfer is complete, a prompt to reboot CP/M is issued with the option of repeating the exact type of copy command again, same format or new. COPY.ASM is the source file for this program.

3.2.2 DSKTEST.COM - Drive/Media Verification Utility

DKSTEST is used to verify the readability of every sector on the diskette. DSKTEST does not write and is non-destructive to the diskette. It is entirely self prompting and requires only the name "DSKTEST" to be typed at the command level of CP/M. There is also an optional long seek testing mode in which a seek to the last track is performed before tracks 0-middle are read, and a seek to track 0 is performed before tracks middle-last are read. If an unreadable sector is encountered, the disk error message is printed first, then the physical track, head (if double-sided), and sector location the error was found. DSKTEST has a built-in sector reading interlace of 2 (or every other sector) so the entire track can be read in two revolutions of the diskette. The console is checked for the Control-C break character during testing. DSKTEST.ASM is the source file for this program.

3.2.3 IMSGEN.COM - Sysgen for the IMS CP/M

IMSGEN is functionally identical to Digital Research's SYSGEN program with the added capabilities for handling the IMS double-density formats. With this program, systems may be brought into memory from double-density, single- or double-sided formats and then written out to any format diskette. Single-density diskettes are a special case in that only a partial system can be written onto the operating system tracks. This may be done to allow a single-density

diskette to be placed in drive A after the initial system load from a double-density diskette, but only warm boots are allowed after this. The IPL must always be done from a double-density diskette. IMSGEN.ASM is the source file for this program.

3.3 CMD hard disk based utility programs

These utility programs all contain driver type software for the IMS Model 490 CMD hard disk controller. They are used for formatting the drive, booting CP/M systems from the drive and testing the CMD hard disk sub-system.

Although the current release of the BIOS for CP/M 2.2 CMD hard disk based systems uses interrupts to recover from the CMD controller routines, these utility programs disable processor interrupts immediately and use polling to recover from CMD controller routines. After the program exits to CP/M via the warm boot entry point at location 0, processor interrupts are re-enabled by the first disk command.

3.3.0 FMT490.COM - CMD Drive Formatter

FMT490 is the main formatter for the CMD hard disk based CP/M system. The IMS Model 490 CMD controller is a hard sectored controller. Therefore, an 8 byte header is maintained at the beginning of each physical 512 byte sector, making the total number of bytes read or written from the drive 520. This program must be run to initialize the header and data area of each sector on the drive. When the CMD drive is brought up for the first time, all CMD devices on the drive must be formatted. After that when using new cartridges, only CMD devices A and B need be formatted.

CP/M 2.2 supports a logical storage device with a maximum of 8 megabytes. Since the CMD cartridge and each surface of the fixed media have roughly 13 megabytes of storage capacity, multiple CP/M devices must be defined over the CMD drive. The cartridge, with its single surface, was chosen to contain the CP/M operating system on track 0 and CP/M logical devices A and B. The fixed media starting with its surface 1 contains pairs of CP/M logical devices beginning with C and D, and, depending upon the size of the CMD drive, it may extend up to CP/M logical device L. This will always leave room for at least four floppy disk CP/M devices.

The CP/M device allocation area for all possible devices on a CMD drive is as follows:

CP/M device	media	head	surface	tracks
A	cart	0	*	0 thru 410
B	cart	0	*	411 thru 822
C	fixed	0	1	0 thru 410
D	fixed	0	1	411 thru 822
(32 megabyte drive ends here)				
E	fixed	1	2	0 thru 410
F	fixed	1	2	411 thru 822
G	fixed	2	3	0 thru 410
H	fixed	2	3	411 thru 822
(64 megabyte drive ends here)				
I	fixed	3	4	0 thru 410
J	fixed	3	4	411 thru 822
K	fixed	4	5	0 thru 410
L	fixed	4	5	411 thru 822
(96 megabyte drive ends here)				

*Surface identifiers are used with the fixed media only.

When FMT490 is run, it first determines the size of the CMD drive, printing on the console the CP/M devices on the cartridge and the CP/M devices on the fixed storage. The user is then asked if a list of instructions are to be printed on the console. FMT490 will then prompt for a CP/M device to format. Note that in the event that a portion of the CMD drive's area becomes unformatted or unreadable due to CRC or SEEK errors, only one device portion of the drive need be reformatted with this program. After input of a CP/M device to format, the area on the CMD drive where that device is defined is printed for reference purposes used later in prompting for known bad tracks on the drive. A last chance prompt to continue with the format operation is issued and a "Y" should be typed to continue, or an "N" to return to the device prompt. Formatting will take approximately 10 minutes per device during which any bad tracks found by the formatter are printed at the console. After the CP/M device has been formatted, the user will be prompted to input known bad tracks that were not detected by the format operation. The CMD drive manufacturer should supply a list of bad tracks on the fixed media. This list will refer to the bad track by track and surface number. The surface number is printed by the program with the device allocation area information. Note that the bad track input prompt is also given when formatting the cartridge, but normal cartridges should not contain any bad tracks. Terminate the input of bad tracks to the formatter by typing Return only.

If bad tracks were found by the program or input by the user, FMT490 will create a pseudo directory entry on that device to mark the bad spot(s) as pre-allocated data blocks to the operating system. In the normal operation of the CP/M, these blocks appear pre-allocated to a file and the system will not attempt to write new data into these blocks.

FMT490 will abort the format operation on these errors:

1. CMD drive I/O errors (except READ): Errors in writing, seeking, or selecting heads are defined as I/O errors.

2. A bad directory track: Due to the nature of this method of dealing with bad tracks, the directory track cannot be bad itself. The directory track input by the user is also considered an error.

3. A bad system track: This pertains to the cartridge only.

4. Number of bad tracks exceeds 128: If you have a drive with 128 bad tracks out of the total number of tracks per device (approximately 410), then that drive should be retired.

During device formatting, FMT490 monitors the console for the Control-C break character, which when typed, will cause the program to prompt the user to verify that the program really should be aborted. Typing a "Y" to this prompt will continue with the formatting. Note that impatient users may use this to verify that FMT490 is still running and the system has not really crashed.

Due to the destructive nature of any formatting program, FMT490 should be used with great caution. FMT490.ASM is the source file of this program.

3.3.1 HDTEST.COM - CMD hard disk test utility

This is a screen oriented test utility for both the IMS490 controller and the CMD drive. This test and verify type program is in a pre-release state and may contain some bugs. Further documentation in the form of an appendix will be available later but for the time being the program can be run and the internal help menu can be viewed by typing "HELP" to the command prompt. Caution: Do not use the formatting capabilities of this test utility, for the routines do not flag tracks and create the pseudo directory entry as FMT490 does.

The terminal dependent routines have been grouped together in one area of the program and may be altered with the use of a terminal dependent area source file (HDTDA) and patch procedure, or the source of the test may be changed and re-assembled.

To change the terminal dependent routines in HDTEST, re-assemble the file HDTDA.ASM for your terminal drivers and integrate into HDTEST by the following steps:

```
A>ddt hdtest.com                ; initiate DDT
DDT VERS 2.2
NEXT PC
3800 0100
-ihdtda.hex                     ; initialize DDT's FCB
-r                              ; overlay new drivers
NEXT PC
3800 0000
-g0                             ; exit DDT

A>save 55 hdtest.com            ; save new test
```

HDTEST.ASM is the source file of this program and HDT.LIB is a macro library needed to assemble this program.

3.3.2 HDBOOT.COM - CMD hard disk based CPM boot loader

This is a secondary initial program loader for the CMD hard disk CP/M system. HDBOOT was written to be used in two useful ways. Assuming that a CMD cartridge has been formatted and a CP/M system has been written onto the first track, HDBOOT may be run directly from the floppy disk based CP/M system as a transient program to load and execute the hard disk based CP/M system on the CMD cartridge. This is useful for running the system the first time. HDBOOT may also be written to the first two tracks of a floppy diskette in the same way that a CP/M system is. This means that when a diskette prepared in this manner is booted from a floppy only IPL rom, this secondary hard disk loader is read and executed instead of a floppy based CP/M system. The hard disk loader will then load and execute the hard disk CP/M system from the CMD cartridge. Note that the current release of the IPL ROM contains a loader for the CMD based CP/M system so using HDBOOT on the system track of a floppy would be redundant.

To write the HDBOOT program to the first two tracks of a double-density floppy diskette in drive B while running under a floppy based CP/M system, perform the following steps:

```
A>ddt hdboot.com                ;use DDT to bring HDBOOT into TPA
DDT VERS 2.2
NEXT PC
2000 0100
-g0

A>imsgen                        ;now bring in IMSGEN

IMS 8" sysgen version 2.0
Type source drive name (or return to skip)
Type destination drive name (or return to reboot) B
Destination on B, type Return to continue
Double-density function complete
Type destination drive name (or return to reboot)
```

Now by placing this prepared diskette in drive A and pressing RESET on the front panel, the hard disk CP/M system can be executed directly. HDBOOT.ASM is the source file of this program.

3.3.3 IMSHDGEN.COM

This is a combined GETSYS and PUTSYS program used to write a relocated operating system built by MOVCPMHD in the TPA to the hard disk. It can also be used to read the operating system from the hard disk and place it into the TPA so it can be saved as a file and altered. IMSHDGEN doesn't require parameters when invoked at the CP/M command level, but will prompt the user to read or write the system.

Examples:

To build and write a 64K CP/M system to the disk using both MOVCPMED and IMSHDGEN:

```
A>movcpmhd 64 *                    ;build a 64K system & leave in TPA

CONSTRUCTING 64K CP/M vers 2.2
FOR A HARD DISK SYSTEM
READY FOR "IMSHDGEN" OR
"SAVE 44 CPMHD64.COM"

A>imshdgen                         ;run directly after MOVCPMHD

IMS Hard Disk Sysgen vers 2.0
Load system from Hard Disk (Y/N)? N
Write system to Hard Disk (Y/N)? Y
Function complete
Write system to Hard Disk (Y/N)? N
```

To read the system from the hard disk and write it to a file named TEST.SYS:

```
A>imshdgen

IMS Hard Disk Sysgen vers 2.0
Load system from Hard Disk (Y/N)? Y
Function complete
Write system to Hard Disk (Y/N)? N

A>save 44 test.sys
```

IMSHDGEN.ASM is the source file of this program.

4.0 THE BIOS

This section deals with the current version of the BIOS released with systems and dated JUNE of 1980. BIOS.ASM is the source distributed with all Series 8000 and Series 5000 systems. IODEF.LIB is the macro library used by the BIOS when assembled with CP/M "MAC" macro assembler. A basic understanding of the responsibility of the BIOS, as outlined by Digital Research's CP/M 2.2 Alteration Guide, is assumed. The NEC uPD765 document will aid in understanding the absolute floppy disk I/O routines, and the write-ups on the IMS Model 340 (8080 CPU) or Model 440 (I/O Board) will aid in understanding console and list related routines. If your system is supplied with the CMD hard disk sub-system, the write-up on the IMS Model 490 CMD controller will be useful. The following information deals with the standard dealer. Dealers may have, previous to the end user's delivery, altered the BIOS, e.g. custom printer and/or console drivers, so information about possible changes should be checked with your dealer.

The new release of the BIOS for the IMS systems contains new ideas in handling floppy disk routines, the CMD hard disk sub-system routines, and more convenient methods for limited customization of the CP/M relocator.

One source file is used now for the BIOS with conditional assembly switches in the beginning of the source to create one of four versions of the system. The main BIOS conditionals are HDSK, MINI, AUTO, and RELBIOS.

The RELBIOS switch is used mainly in house at IMS to originate the BIOS at the address necessary to integrate it with the CP/M relocator. For second level system generation, this switch must be set FALSE in order for the MSIZE equate to originate the BIOS at the proper address.

The AUTO switch may be set true with second level generations of the system only to produce and originate the data/code needed for the CCP to automatically execute a single command line directly after the initial program load. The standard and most rational command to use is: A>SUBMIT INIT, which requires that only SUBMIT.COM and a submit file INIT.SUB be present on the system device A. This way, by controlling what is in the submit file, multiple as well as single commands can be executed after system loading.

The MINI switch controls the generation of the code for the floppy disk controller routines. With MINI set FALSE, code for the IMS Model 400 8" controller (Series 8000) will be generated. If MINI is set TRUE, IMS Model 430 5" controller (Series 5000) routines will be generated. Be sure during second level system generations that this switch is set for the proper system.

The HDSK switch controls the generation of the CMD hard disk controller routines. With HDSK set FALSE, Series 5000 or 8000 floppy based CP/M routines are generated, else when HDSK is set TRUE, Series 5000 or 8000 CMD hard disk based CP/M routines are generated. Of course, this switch may only be used if your system has been supplied with the CMD hard disk sub-system.

With this single source of the BIOS and the conditional switches properly set, BIOS routines for these four systems may be generated:

HDKS	MINI	GENERATED BIOS ROUTINES
false	false	Series 8000 floppy based CP/M
false	true	Series 5000 floppy based CP/M
true	false	Series 8000 CMD hard disk based CP/M
true	true	Series 5000 CMD hard disk based CP/M

Interrupts for all the disk controllers Models 400, 430, and 490 are used to recover from disk routines in the new BIOS release. This prevents a previous problem of unserviced drive ready line change interrupts from stacking internally in the uPD765 FDC used on both the Model 400 and 430 controllers. See Appendix A for proper shunting of the interrupt vector strips on these controllers.

The new BIOS release now contains a limited configurating table at the end of the jump table which is used by a driver initializing routine to perform console and list device baud rate setting, as well as minor patching to the list driver routine for handshaking and changing the floppy drive step rates used.

The IMS Model 460 64K dynamic memory board with parity is now supported by the BIOS. The Model 460 should be set for I/O address 0 and respond to this address by the I/O enable shunt for proper reset of parity errors. See Appendix A for interrupt shunting of this board. When parity errors occur, memory is re-initialized and the parity error is cleared. The console is broken and the message "PARITY ERROR, IGNORE?" is printed on the console. If a "Y" response is typed, the interrupted program is continued and if any other response is typed, the BIOS performs a warm boot. Note that if the parity error occurred in the BIOS portion of the system, a warm boot may not be sufficient to fully recover from the error. A cold boot could be performed in this case.

The rest of this section is split into three parts defined as floppy disk based CP/M systems, CMD hard disk base CP/M systems, and console and list devices common to both systems.

4.1 Console and list device routines

The IMS Model 340 (8080 CPU) has two serial ports incorporated on the board. The base address of ports is fixed at 10 hex. Channel one serial is assigned the default console device, which is assumed to be a 9600 baud CRT terminal. Channel two serial is assigned the default list device, which operates at 300 baud. No special device handshaking is used with either serial port. The IMS Model 450 (Z80 CPU) is used in conjunction with the Model 440 (I/O board) which has two serial ports that are software compatible with the Model 340. In addition, this board has a 24 bit parallel device (8255) assigned to ports directly above the serial ports. The standard system does not use this parallel device and contains no code for it. The Model 440 can be assigned different base addresses in 16 address increments. For the standard system, its assigned 10 hex as the base address to be compatible with the Model 340 serial ports. In effect, this means the system software is independent of whether the 8080 CPU or Z80 CPU is used. Both serial ports have software selectable baud rates through the use of a programmable interval timer (8253). They are initially set for 9600 and 300 baud by the cold boot ROM even though there is no console interaction before initial system load. The ROM sets up these default values to remain compatible with previous CP/M 1.4 releases. Also the counter values set by the ROM assume that the optional on-board (IMS440) oscillator for 19.2kb operation is not present.

The CP/M 2.2 BIOS, however, performs re-initialization of the uarts in its driver initialization, setting new baud rates for the standard oscillator or the optional 19.2kb oscillator. See CPMPAT.COM in the System Utility Program section.

4.2 Floppy disk based CP/M BIOS

The Model 400 and 430 (8" and 5" disk controllers) are set up with their base address etched into the board at 80 hex. This base can be moved in 16 address increments but is not recommended to avoid incompatibility with disk controller dependent utility programs and the IPL ROM.

Floppy disk controller interrupts should be shunted to vector 5 on the bus for proper operation (see Appendix A). A jump to the interrupt handler is maintained at both restart 5 and 6 for compatibility with the Model 340 8080-I/O board.

4.2.0 Series 8000

Single-density diskettes may be used as the common mode for recovering files written on other CP/M systems. See the section on FORMAT.COM for detailed sector formatting. When BIOS is in the single-density mode, reading and writing is done immediately from and to the disk, into and out of the preset DMA address. The standard sector interlace defined by Digital Research is used.

When BIOS is in the double-density mode, reading and writing are done from an internally maintained 256 byte buffer. Each read call from BDOS causes half of this buffer (128 bytes) to be transferred to the current DMA address. Each write call brings 128 bytes from the DMA address into this buffer. Double-sided diskettes are handled with this same buffering, but consider the track on side two of the diskette to be just an extension of the same track on side one. The second side is formatted the same way as the first. Each 256 byte physical sector on the diskette represents two 128 byte logical records for BDOS. The double-density mode does not use a sector interlace table; instead, the SECTRAN subroutine in BIOS contains math to determine the interlace.

The 8" disk parameter blocks used for CP/M look like this:

	single-density	**double-density**	**double-density double-sided**
SPT	26	52	104
BSH	3	4	5
BLM	0111B	01111B	011111B
EXM	0	1	3
DSM	242	242	242
DRM	63	127	255
AL0	0C0H	0C0H	0C0H
AL1	0	0	0
CKS	16	32	64
OFF	2	2	2

4.2.1 Series 5000

The Series 5000 BIOS now supports a double-sided, double-density format that follows the same accessing convention as the Series 8000. Both 5000 formats are double-density, with 256 bytes per sector, 16 sectors per track, and 40 tracks per side. The BDOS interface is handled the same as with the Series 8000.

The 5" disk parameter blocks used in CP/M look like this:

	double-density	**double-density double-sided**
SPT	32	64
BSH	3	4
BLM	0111B	01111B
EXM	0	1
DSM	151	151
DRM	63	63
AL0	0C0H	080H
AL1	0	0
CKS	16	16
OFF	2	2

4.3 CMD hard disk based CP/M BIOS

The model 490 CMD hard disk controller is set up with a base address of 90 hex etched into the board. This base can be moved in 8 address increments but is not recommended to avoid incompatibility with hard disk related utility programs and the IPL ROM. Hard disk controller interrupts should be shunted for vector 5 on the bus for proper operation (see Appendix A). A jump to the interrupt handler is maintained at both restart 5 and 6 to be compatible with the Model 340 8080-I/O board.

The Series 8000 and 5000 CMD hard disk based CP/M BIOS are functionally identical except for the type of floppy disk they support. The CMD devices are always the first CP/M logical devices and the floppies are the next four open CP/M devices. Warm boots are always from the cartridge or CP/M device A.

The CMD controller and drive use a sector size of 512 bytes with an additional 8 bytes at the beginning of the sector for a header. The header contains information like select code, cylinder number, sector number, and an optional CRC word. The CMD controller contains hardware for automatic and transparent maintenance of CRC so the optional software CRC is not used. The CMD sector buffer is located on the controller so system memory need not be wasted. Reading and writing of this buffer is done via DMA through channel 2 of the floppy disk controller based at 80 hex (the Model 400 or 430).

The CMD devices have disk parameter blocks as follows:

	A	**C,E,G,I,K**	**B,D,F,H,J,L**
SPT	128	128	128
BSH	6	6	6
BLM	0111111B	0111111B	0111111B
EXM	3	3	3
DSM	819	821	823
DRM	511	511	511
AL0	0C0H	0C0H	0C0H
AL1	0	0	0
CKS	0	0	0
OFF	1	0	411

Note that the directory check vector size (CKS) is zero for all CMD devices including the removable cartridge. This means that the directory integrity of the cartridge devices could be lost if a cartridge was switched without performing either a cold or a warm boot of the system.

5.0 FIRST LEVEL SYSTEM GENERATION

First level system generations in an IMS system are done to change the memory size of the operating system, re-define the baud rates of either the console or the list device, switch to the optional on-board 19.2kb oscillator, change the step rate of the floppy disk drives, and do limited configuring of the list driver for handshaking.

First level system generations involve the use of the CP/M relocator program MOVCPM.COM (or MOVCPMHD.COM in CMD hard disk based systems). The IMS versions of these relocators are functionally identical to the MOVCPM relocator described by Digital Research in their Introduction to CP/M Features and Facilities. The minimum memory size which any CP/M system may be generated for is 20K.

Changes to the IMS system as described above can be accomplished swiftly with the use of the utility program CPMPAT.COM, written to access and/or change the driver configuring table contained in the BIOS. See the System Utility Program section on CPMPAT.

5.1 Floppy based systems

Once the CP/M relocator has been patched for proper operation on the target system, run MOVCPM to build, and leave in the TPA, a system of the proper memory size. Immediately after running the relocator, use the system utility IMSGEN.COM to write the new operating system on the first two tracks of a diskette (usually a back-up diskette for testing). Cold boot from this diskette using the IPL ROM and verify proper operation, then use IMSGEN once again to write the system onto all packs that contain a system.

Because of the implementation of MOVCPM, all system diskettes are supplied with 32k CP/M systems. If your system is configured with more than 32k, a few simple steps will generate a system for your memory size. Before proceeding any further, back the system diskette up using "COPY ALL" and place the master diskette somewhere safe, only to be used as a last recovery source. Cold boot from the back-up diskette and type in the command:

```
A>MOVCPM * *
```

This will relocate the largest possible CP/M system that will fit in your current memory configuration and leave it in the TPA for IMSGEN. After the CCP prompt returns, type in the command:

```
A>IMSGEN
```

This will load the IMS system generation program which will in turn prompt you for a source drive or return to skip. Type a return to this prompt because the system is already in memory, and IMSGEN will prompt you for the destination drive. Type in "A" and write the system onto the back-up system diskette. Now reset the computer to start the IPL again, and the system will sign on with the new size CP/M system.

5.2 CMD hard disk based systems

The procedure for first level generations of the CMD hard disk based systems are the same as with the floppy based system with the exception of the system generation utility. Once the

system is in the TPA, use the utility IMSHDGEN.COM (see System Utility Program section) to write the system onto the first track of the cartridge.

As with the floppy based system, the maximum sized CP/M system can be built easily by these steps:

```
A>MOVCPMHD * *
```

This will build the largest possible CMD hard disk based CP/M system that will fit in your current memory configuration and leave it in the TPA ready for IMSHDGEN.

Next type:

```
A>IMSHDGEN
```

IMSHDGEN will load and prompt to type "Y" to load the current system on the cartridge or type "N" to skip. Skip this part with an "N" and then you will be prompted to write the system in the TPA onto the cartridge. Type a "Y" here and the system will be written and program should return with "Function complete" and the same write system prompt. Type an "N" here to return to the operating system. Note that if you are currently performing a system generation while operating under the CMD hard disk, and a CP/M system of a different size was written to the cartridge, the warm boot performed by IMSHDGEN to return to the operating system is invalid. In this case cold boot the system to regain control.

6.0 SECOND LEVEL SYSTEM GENERATION

This section is designed as a guide for generating your own custom BIOS for use on the IMS systems. A basic understanding of the operation of the BIOS is given in Digital Research's CP/M 2.2 System Alteration Guide and this manual should be reviewed before continuing. A second level system generation is necessary if you wish to alter the routines in the BIOS in any way. A back-up diskette of some kind should be used to write the newly constructed system to, after which the altered system can be tested and then ultimately written to all diskettes containing systems. Before altering the BIOS, please consult the section in this document on the BIOS. It may be helpful in customizing your own version, as well as for tailoring user written programs that call BIOS directly for disk operations. This section is not necessary for simply increasing memory size or duplicating your current system on another diskette. Tools provided for this are "MOVCPM", "COPY SYSTEM" and "IMSGEN" which are covered in the previous system utility section. A second boot loader known as SBOOT is not needed with the IMS system because the IPL ROM handles the entire load of the system.

Note that performing a second level system generation defeats the CP/M relocator for further first level system generations due to the altered BIOS routines. The patching of the relocator with CPMPAT is also defeated, so the driver configurating table after the jump table in the BIOS should be changed for the proper system configuration.

Second level system generation is generally the same in concept for all versions of the IMS system, but differences in the systems will be pointed out where need be.

The common files needed in any second level generation are:

```
BIOS.ASM                    ; BIOS source file
IODEF.LIB                   ; BIOS macro library file
ED.COM or VUE.COM           ; Program editor
MAC.COM                     ; CP/M macro assembler
DDT.COM or SID.COM          ; Debugger
```

Files needed for floppy based systems are:

```
MOVCPM.COM                  ; CP/M relocator
IMSGEN.COM                  ; System generation utility
```

Files needed for CMD hard disk based systems are:

```
MOVCPMHD.COM                ; CP/M relocator
IMSHDGEN.COM                ; System generation utility
```

STEP #1: RE-ASSEMBLY OF THE BIOS

Using the CP/M editor "ED", "PolyVue/80" or other text editor, edit the MSIZE equate in BIOS to reflect the exact new memory size. This equate is the rounded memory size in kilobytes. Make sure that the RELBIOS switch is set FALSE. Now using MAC.COM, re-assemble BIOS to produce a .HEX file on the disk. The end address of the assembly cannot be greater than the top of RAM memory. Do not attempt to use LOAD.COM once the "HEX" file is generated.

STEP #2: RELOCATING CP/M 2.2 SYSTEM

Use the CP/M relocator to build a system for the target memory size and save this on the disk as a file:

```
A>MOVCPM xx *        ; for floppy based systems

        - or -

A>MOVCPMHD xx *      ; for CMD based systems

          . .
          . .
          . . . . .instructs MOVCPM.COM to leave system in TPA area
          .
          . . . . . new memory size rounded in kilobytes
```

Follow the instructions given by the relocator for saving the memory image on disk in a file CPMxx.COM where xx will be the target memory size.

STEP #3 OVERLAYING THE CUSTOM BIOS

The new task is to overlay your custom BIOS on top of the new CPM 2.2 system. This is done with the aid of CP/M debugger "DDT". Issue the command:

```
A>DDT CPMxx.COM                ; xx is the target system size
```

DDT will load the new CP/M 2.2 system into the TPA and issue its own sub-system prompt "-". Type in the next instruction to DDT:

```
-IBIOS.HEX
```

This initializes DDT's file control block for the new BIOS file. The next part of this step is to read in the re-assembled custom BIOS with the proper offset to place it in memory over the old BIOS. Offsets differ with every memory size. Some standard offsets are listed below but any offset may be computed by subtracting the absolute address of BIOS from 1F80 hex. This computation must either be done in hex or converted to hex for use with DDT.

Example: In a 64k CP/M system:

The 8000 BIOS will begin at F400 hex.
1F80 hex - F400 hex = 2B80 hex (offset for DDT).

The 5000 BIOS will begin at F600 hex.
1F80 hex - F600 hex = 2980 hex (offset for DDT).

Common memory sizes can be looked up in the following table:

	Floppy Based Systems		CMD Based Systems
memory size	series 8000	series 5000	both 8000 and 5000
32K	AB80	A980	B380
36K	9B80	9980	A380
40K	8B80	8980	9380
44K	7B80	7980	8380
48K	6B80	6980	7380
52K	5B80	5980	6380
56K	4B80	4980	5380
60K	3B80	3980	4380
64K	2B80	2980	3380

Once the offset is known, issue this next DDT command to read DBIOS.HEX (or MBIOS.HEX) into memory.

-Rxxxx (where "xxxx" is the offset required)

At this point the new CP/M 2.2 system has been constructed in memory and is ready to be written out to your new diskette, so be sure you have a new diskette formatted or one ready to accept the system, and leave the DDT program by typing:

-G0

STEP #4: WRITING NEW SYSTEM TO DISK

After leaving the DDT program, no other transient program except the system generation program IMSGEN.COM (or IMSHDGEN.COM in CMD based systems) may be loaded due to the newly constructed system still contained in memory. Type the next command in:

A>IMSGEN ; for floppy based systems

- or -

A>IMSHDGEN ; for CMD based systems

This loads the IMS system generation program which then issues a prompt to load the system into memory or return to skip. Type a return to skip system loading since our new system is already in memory. You will then be prompted to write the system from memory to the disk. For IMSGEN, type a destination drive name and then return to write the system, and for IMSHDGEN, type a "Y" to write the system to the cartridge.

Cold boot the system to load and execute the new system. Verify proper operation of customized routines, and in the case of the floppy based systems, write systems to all diskettes to be used in drive A.

APPENDIX A
CP/M and MP/M Interrupt Vector Shunting

FLOPPY DISK CONTROLLERS:

IMS400 (8" controller) and IMS430 (5")
Location (JB) on the board is the interrupt selection strip. Shunt the pins labeled "5" only and no others.

HARD DISK CONTROLLER:

IMS490 (CMD controller)
Location (JD) on the board is the interrupt selection strip. Shunt the pins labeled "5" only and no others.

64K DYNAMIC MEMORY:

IMS460
Location (JG) on the board is the interrupt selection strip. Shunt the pins labeled "2" only and no others. Also for software to reset the parity error detection logic, the I/O enable shunt (JE) must be on and the board address set for 0 (all shunts on the JC strip).

The following shunts are only mandatory for MP/M operation, but will not alter CP/M operation if done.

I/O BOARDS:

IMS440 (2-serial, 24-bit parallel)
Location (JJ) on the board is the interrupt selection strip for relative time clock interrupts. Shunt the pins labeled "7" only and no others. Locations (JK and JL) on the board are the interrupt selection strips for uart receive and transmit status. Shunt the pins labeled "6" only on both strips and no others.

IMS480 (4-line serial)
Locations (JC, JD, JE and JF) on the board are the interrupt selection strips for each of the uarts respectively. Shunt the pins labeled "5" only on all strips and no others.

ADDITIONAL 64K DYNAMIC MEMORY:

IMS460
If memory bank zero in an MP/M system is a dynamic board, the shunting of this board is identical to the CP/M shunting described above. The convention for additional MP/M memory banks using the IMS460 is that each board I/O address follows the last, and additional boards are placed in the "BANK" mode (JE) with a shunt. Enable I/O with (JB) on these boards also but do not shunt any parity interrupt vectors at location (JG).

APPENDIX B
Processor Port Assignments

ADDRESS (HEX)	ASSIGNMENT
00 - 0F	Memory management (bank switching ports): Consult operating system for breakdown.
10 - 1F	IMS440 I/O board: CP/M - MP/M default console and list device, MP/M relative time clock.
20 - 3F	IMS480 4-line I/O board: Reserved for MP/M additional consoles.
40 - 4F	IMS440 I/O board: Reserved for MP/M additional consoles.
50 - 5F	**FREE**
60 - 7F	IMS480 4-line I/O board: Reserved for MP/M additional serial ports, Modems, aux list devices, etc.
80 - 8F	IMS400 / IMS430 floppy disk controllers: Includes 8257 DMA device with four channels.
90 - 97	IMS490 hard disk controller #1: Default controller in hard disk subsystem. DMA provided through FDC at base 80H.
98 - 9F	IMS490 hard disk controller #2: Expansion controller (reserved).
A0 - BF	** FREE **
C0 - CF	IMS400 / IMS430 floppy disk controllers: Optional expansion for 8 floppy drives of either type or dual 8" and 5" systems.
DO - FF	** FREE **

APPENDIX C
Initial Program Loader (IPL)

16-bit checksum = 7297 Hex)

The new release of the IPL ROM was initiated to support the CMD hard disk sub-system. Like previous IPL ROMS, the new one loads the entire CP/M operating system into memory and jumps to the BOOT entry point in the BIOS jump table. Now, one IPL ROM is responsible for loading all Industrial Micro Systems diskette formats:

SERIES 8000 FORMATS:

CP/M 1.4 double-density
CP/M 1.4 double-density, double-sided
CP/M 2.2 double-density
CP/M 2.2 double-density, double-sided
CP/M 2.2 CMD hard disk sub-system

SERIES 5000 FORMATS

CP/M 1.4 double-density
CP/M 2.2 double-density
CP/M 2.2 double-density, double-sided
CP/M 2.2 CMD hard disk sub-system

The origin of this ROM in all systems is 0 and the board in which the ROM is located (either the Model 340 or 440) should be shunted to enable the ROM automatically after power-on or system reset.

A summary of the steps in with the IPL ROM goes through to load a CP/M system after a power-on or system reset is as follows:

1. All of memory is moved into the ACC register then back to memory. This step will initialize a 64K dynamic memory board if present and also copy the contents of the ROM into system memory beginning at 0. Note that only the first 1K of memory is altered by this action. Directly following the move, the ROM is disabled and the program begins execution from RAM memory.

2. The standard baud rates for the uarts are programmed for compatibility with the CP/M 1.4 release. Note that the IPL program does not require any interaction with the console to load the system.

3. The CMD hard disk controller is initialized and tested for its presence in the system.

4. The default step rate for 8" floppy disks is programmed.

5. The IPL program then waits in a loop for either the CMD hard disk drive to become ready (if present) or floppy disk drive 0 to become ready. If the CMD drive becomes ready, the program proceeds to step 6. If floppy drive 0 becomes ready, the program proceeds to step 7.

6. The CMD drive is tested for a valid CP/M system. If CP/M is not present on the CMD drive, the program goes back to step 5. If the CP/M system is preset on the drive, the starting address is determined and the system is loaded and executed.

7. The disk is tested for a mini floppy for determining load addresses for CP/M and to increase the step rate for mini floppy drives.

8. The disk is then tested for a valid CP/M operating system. If CP/M is not found on the disk, the program goes back to step 5. If CP/M is present on the disk, it is tested for CP/M 1.4 for determining load and execution addresses.

9. CP/M is loaded from the disk and executed.

IPL.ASM is the source for the ROM and is supplied on or with the system diskette with every system. Normally the origin of the IPL is at 0, but a conditional exists for testing the IPL if new code was added. Set TRUE, the origin of the IPL is moved to 100 hex and then may be loaded as a .COM file and executed directly from CP/M.

INDUSTRIAL MICRO SYSTEMS

MODELS 450 & 440

Z80 PROCESSOR & I/O BOARDS

****

GENERAL

The Model 450 Processor and the 440 I/O Boards are the Central Processing Unit (CPU) of the Industrial Micro Systems Series 5000 and 8000 Computer Systems. The Model 450 provides control and the 440 provides timing, and I/O interfacing for the system.

Control is accomplished by the NEC Z-80 LSI (Large Scale Integration) Micro Processor device. This is a fully Parallel, 8-bit, Bi-Directional, Bus Oriented Processing Unit with a 16-bit address capability, allowing up to 64 Kbytes of directly addressable memory. the Z-80 has a 1 USEC instruction cycle time.

Timing is provided by the 8253 Programmable Interval Timer (PIT). The PIT is a Timer/Counter and functions as a general-purpose, multi-mode timing element that generates accurate time delays under software control.

The 6402 Universal Asynchronous Receiver/Transmitter (UART) interfaces the Z-80 Microprocessor to an Asynchronous Serial Data Channel. The UART converts input serial data to parallel data to be acted upon by the system. Output data is converted from parallel to serial to be placed on the RS-232 PORT.

The 8255 Programmable Peripheral Interface Circuit interfaces to Z-80 Microprocessor to three 8-bit parallel ports. These are located at the 50 pin I/O connector at the top of the 440 card. Each line is TTL buffered and has provision for termination network.

The Model 450 processor consists of a single Printed Circuit Board that nominally occupies the first slot (Slot 0) of 12 slots in the Series 5000 or 8000 Computer Systems. It interfaces with the rest of the system through the address, data, and control lines of the S-100 Bus System.

The 450 Processor board consists of the following functional divisions (See Figure 1).

- 8-bit Microprocessor Device (CPU)
- Priority Vectored Interrupt Circuitry

The 440 I/O Board consists of the following functions:

- 1024 by 8-bit ultraviolet Erasable Programmable Read-Only-Memory
- Programmable Interval Timer/Real Time Clock
- Two Universal Asynchronous Receiver/Transmitters (UART's)
- RS-232 Interface Logic
- Three 8-bit parallel ports

SPECIFICATIONS

. Word Size: Address	16 bits
Data	8 bits
. On-Board ROM:	1 Kbyte
. Directly Addressable Memory:	64Kbytes
. Clock Frequency:	4 MHz
. I/O Ports (Serial):	2
. 8 Bit Parallel Ports:	3
. Baud Rate:	75 to 9600 Baud
. PCB Dimensions:	5.25" x 10" (13.3 cm x 25.4 cm)
. Power Requirements:	440 +16 @ 60 ma +8 @ 500 ma -16 @ 40 ma 450 +8 @ 700 ma

Z-80 MICROPROCESSOR

The Z-80 Processor is a Bi-Directional, Bus-Oriented, 8-bit Parallel LSI device with a 16-bit address capability, allowing up to 64 Kbytes of directly addressable memory. The Z-80 contains six 8-bit, general purpose working registers and an accumlator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The Z-80 has an external stack feature wherein any portion of memory may be used as a last-in/first-out stack to store/retrieve the contents of the accumulator, flags, program counter, and all of the six general-purpose registers. The 16-bit stack pointer contains the address of the next available location in the external memory. The program counter is a 16-bit register that contains the program address. The flag register contains six bits of condition code information which indicate the results of the ALU (Arithmetic Logic Unit) operation; Negative (N), Zero (Z), Overflow (V), Carry from Bit 7 (C), and Half-Carry from Bit 3 (H). These are used as testable conditions for the conditional branch instructions. This stack feature allows the ability to provide priority vectored interrupts.

The minimum instruction time for the Z-80 Microprocessor is 1 usec. Separate 16-bit address and 8-bit bi-directional data lines are used to facilitate easy interface to memory and I/O.

Memory and I/O interface control signals may be used to suspend processor operation and force the address and data lines to a high impedance state (Tri-State allowing Direct Memory Access (DMA) and multi-processor operation.

The Z-80 provides 158 variable length instructions (see Z-80 instruction set). In addition to performing basic processing functions, the processor is capable of responding to Real-Time Program Interrupts, Automatic Restart in response to the RESET/Power-On RESET signals, and Direct Memory Access operations.

FIGURE 1 - Z80 CPU BLOCK DIAGRAM

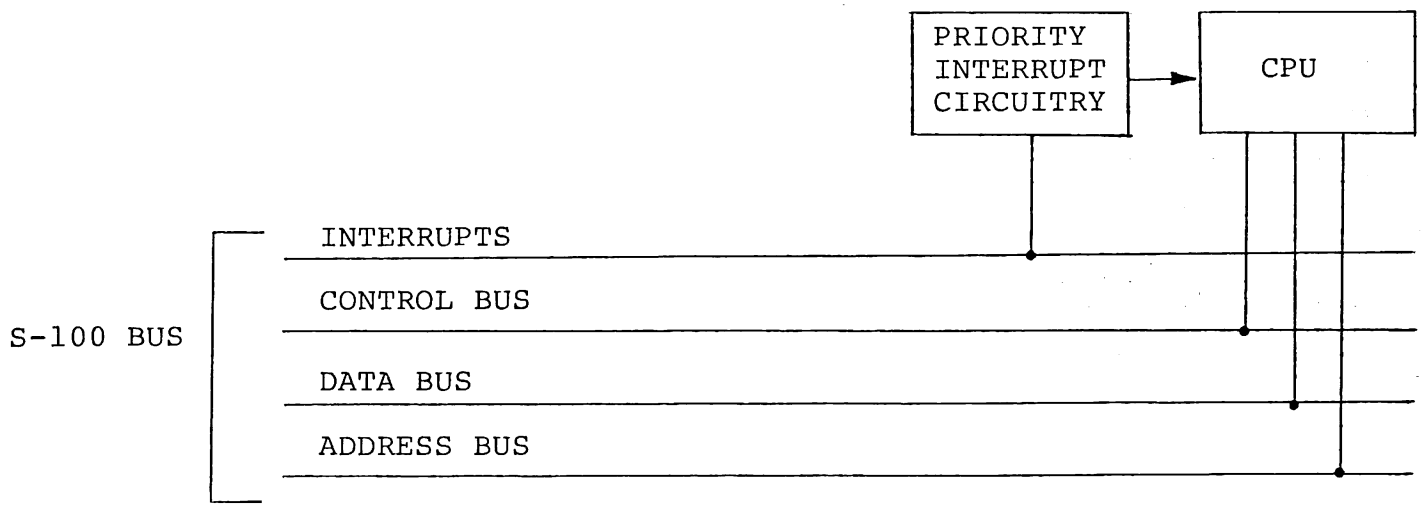
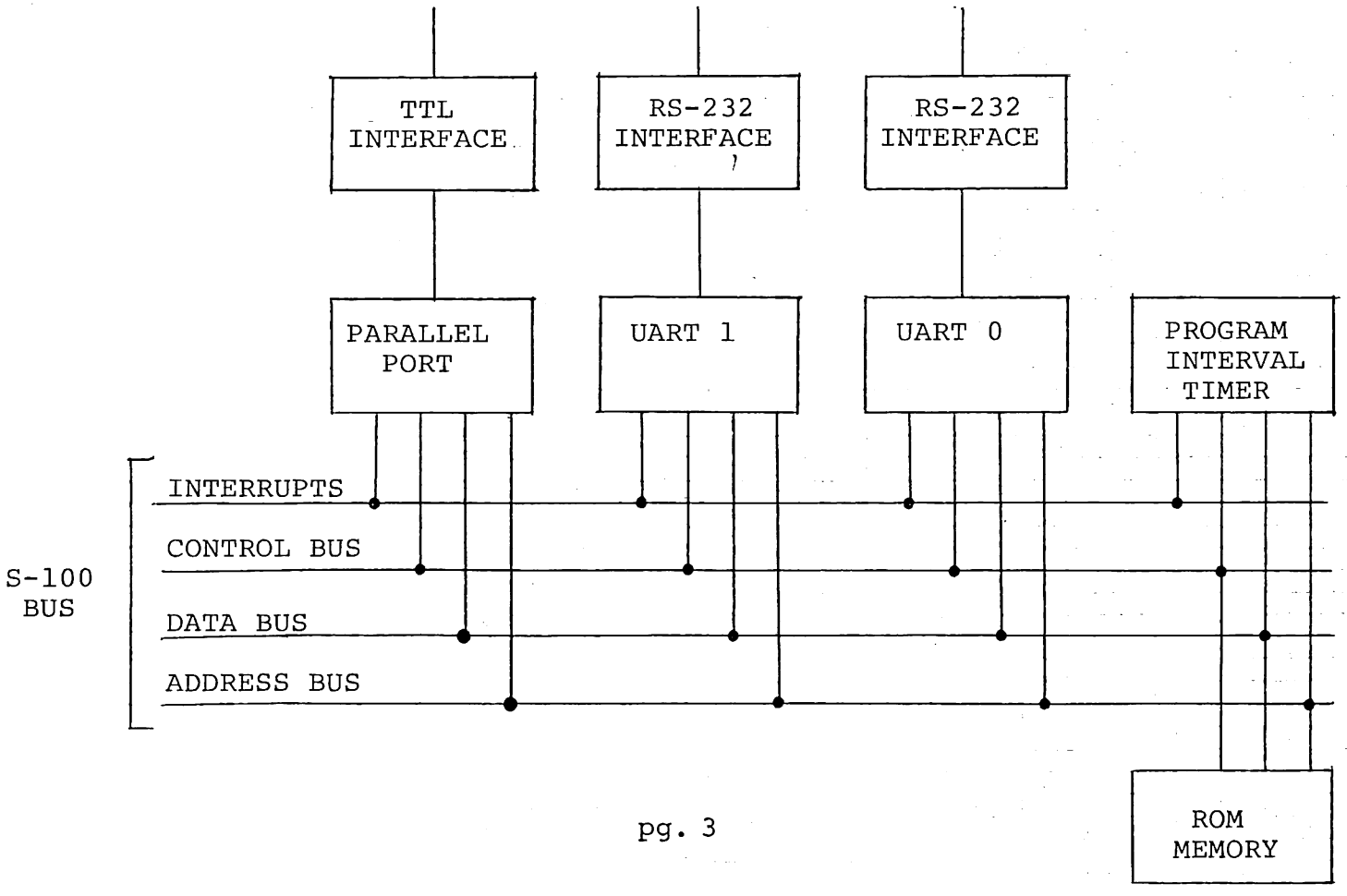


FIGURE 2 - I/O BOARD BLOCK DIAGRAM



440 I/O BOARD

1024 x 8 EPROM (Memory)

The Intel 2708 is a high-speed, bit-erasable, and electrically reprogrammable Read Only Memory (EPROM). It is packaged in a 24-pin, Dual In-Line Package (DIP) with a transparent lid, allowing the user to expose the chip to ultraviolet light and erase the bit pattern. A new pattern can then be written into the device. ROM address space is SHUNT selectable. The EPROM is used in the 440 Processor to contain the Bootstrap Program or a special monitor.

PROGRAMMABLE INTERVAL TIMER

The Intel 8253 Programmable Interval Timer is a programmable Counter/Timer. It's function is that of a general-purpose, multi-mode timing element that can be treated as an array of I/O ports in the system software.

The 8253 allows the programmer to set up timing loops in the system software so as to generate accurate time delays under software control The user may initialize one of the three counters with the desired quantity and, upon command, count out the delay and interrupt the CPU when it has completed it's tasks. This minimizes software overhead and allows multiple delays that can be easily maintained by assignment of priority levels.

Other Counter/Timer functions provided by the 8253 are:

- Real Time Clock
- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Digital One-Shot

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

The 440 has two on-board Serial I/O Ports. Each port consists of a 6402 UART. The UART is a programmable MOS/LSI device used for interfacing an Asynchronous Serial Communication Line to the parallel data lines of the microprocessor.

The UART is made up of two separate and independent sections:

1. The receiver
2. The transmitter

RECEIVER

The receiver accepts the serial data, converts it to parallel and decodes it. The decode function converts the serial Start, Data, Parity, and Stop bits to parallel information and verifies the proper code transmission by checking parity and the receipt of a valid stop bit.

TRANSMITTER

The transmitter section converts the parallel data into a serial word which contains the data, along with the start, parity, and stop bits.

Both the receiver and transmitter are double-buffered. The UART may be programmed as follows:

1. The word length may be either 5, 6, 7, or 8 bits.
2. Parity generation and checking may be inhibited, and the parity may be odd or even.
3. The number of stop bits may be one or two (1 1/2 when transmitting a 5-bit code).
4. The baud rate may be set from 75 to 9600 baud.

RS-232 VOLTAGE INTERFACE

The two serial ports of the 340 processor go to the system peripherals through industry standard EIA RS-232 Voltage Interfaces.

HARDWARE SUMMARY

The instruction set of the 450 is that of the Z-80 Microprocessor Device. The Processor has a 1 usec instruction cycle time, the ability to provide priority vectored interrupts, and the capability for 256 bi-directional I/O ports.

FUNCTIONAL OVERVIEW (See Figure 1)

The S-100 bus interface consists of three separate sets of lines:

1. Address Lines
2. Data Lines
3. Control Lines

ADDRESS - The 16 address lines (A0-A15) allow each of 65,536 bytes of memory to be uniquely addressed.

The address lines are utilized by either the Microprocessor or a Direct Memory Access (DMA) device, such as the Disk Controller. These lines are decoded by each memory module so that only one memory location is addressed by an exclusive bit pattern.

DATA - The data lines are further sectioned into two sets of lines:

1. Input Data
2. Output Data

The input data lines (DI0-DI7) carry the binary data in parallel from the memory to the 450 Processor.

The output lines (DO0-DO7) carry the binary data in parallel from the 450 Processor to memory.

CONTROL - The remaining bus lines perform various control functions:

1. Timing
2. Synchronization
3. Data Direction
4. Status

TIMING AND SYNCHRONIZATION - These control lines are:

0 CLOCK	PSYNC
0 CLOCK	READY1
CLOCK-	READY2
SMI	WAIT

01 and 02 (phase 1 and phase 2) clocks, along with CLOCK-, are generated by the microprocesor clock circuit and are the main timing signals.

PSYNC, XRDY, and SYNC enable and initialize the clock circuit. The 16 MHz crystal provides the base frequency for the oscillator. From this circuit 02 clock is used by the Microprocessor from control timing.

STATUS - The status signals and the corresponding data bits are as follows:

BIT	STATUS TERM
D0	SMEMR+
D1	SINP+
D2	SMI+
D3	SOUT+
D4	SHLTA+
D5	
D6	SWO-
D7	SINTA+

The eight status lines are placed on the bus by the microprocessor to be selectively used by the memory and I/O boards to obtain information as to the nature of the cycle.

INTERRUPTS - The vectored priority interrupt system consists of eight interrupt lines as follows:

INTERRUPTS	DESCRIPTION
VI0-VI5	User defined
V6	Communication interrupt
V7	RTC interrupt

The interrupts' function is to indicate to the CPU that there are peripheral devices that need to be serviced. When the priority requirements are fulfilled, the CPU goes into the Interrupt Service Routine and responds to the device requesting the interrupt.

PORT CONTROL - Port X8H interrupt mask, request-to-send, and ROM enable bit assignments are as follows:

BIT	DESCRIPTION
0	ROM disabled = 1
1	Real Time Clock interrupt enable =1
2	UART 1 transmit interrupt enable = 1
3	UART 1 receive interrupt enable = 1
4	UART 1 request-to-send
5	UART 0 transmit interrupt enable = 1
6	UART 0 receive interrupt enable = 1
7	UART 0 request-to-send

The Real Time Clock (RTC) interrupt (bit 1) is reset when out X9H is executed.

The ROM Enable/Disable (bit 0) shunt is located on JG 7-8.

UART CONTROL - Control for UART 0 is accomplished by the following line and bit assignments:

BIT	FUNCTION	
Out X0H= Control		
0	Parity Inhibit	
1	Even Parity Enable	
2	Stop Bit Select	
3	Word Length - LSB	
4	Word Length - MSB	
Out X1H= Transmitted Data Out		
Out X0H= Status		
0	Receive Data Ready	
1	Transmit Holding	Register Empty
2	Parity Error	
3	Framing Error	
4	Overrun Error	
7	Clear-To-Send	
In X1H= Received Data In		

Line and bit assignments for UART 1 are as follows:

Out X2H= Control
Out X3H= Transmitted Data Out
In X2H= Status
In X3H= Receive Data In
(Bit assignments are the same as UART 0)

PIT CONTROL - The Programmable Interval Timer provides three independent counters for interrupt timing:

Counter 0	UART 0 Clock
Counter 1	UART 1 Clock
Counter 2	Real Time Clock

Output X7H provides control for the PIT. An output to line (port) X7H must be accomplished before establishing the timing intervals for each counter. The division factor is loaded into each count register to establish the desired frequency output. The base clock frequency is 2MHz. The following values should be output to port X7H for each counter, as follows:

COUNTER	OUTPUT
0	36H
1	76H
2	B6H

To load the count registers, the desired division rate should be output (least significant byte first) for the counter as follows:

COUNTER	OUTPUT
0	Port X4H
1	Port X5H
2	Port X6H

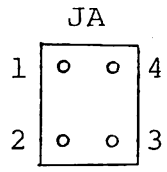
The algorithm for determining the Baud Rate for the UARTs is as follows, using Baud 9600 for the example:

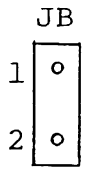
Note that the UART requires an input frequency of 16 times the Baud Rate.

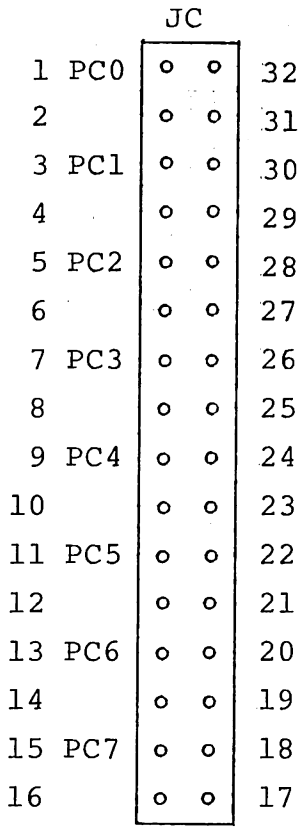
So: Output 36H to port X7, then
Output 0DH to port X4, then
Output 00H to port X4

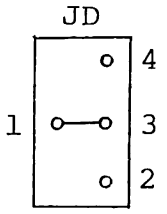
The UART is now set to run at 9600 Baud.

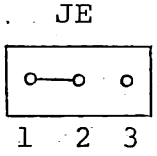
MODEL 440 I/O BOARD SHUNT AND JUMPER OPTIONS

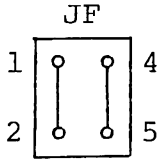












PARALLEL PORT A LOC. 7.5A

No Shunts = Input Mode
Shunt JA 1-2 = Output Mode
Shunt JA 2-3 = Bidirectional Mode

PORT A DRIVER/RECEIVER LOC 8A, 10A

74LS243 Non Inverting
74LS242 Inverting

PORT A TERMINATION OPTIONS LOC. 9A

Open No Termination
Beckman 899-1R1.0K Pull Up Termination
Beckman 899-5-R2201330 Pull Up/Down Term.

PARALLEL PORT B SELECT LOC. 11.5B

No Shunts = Input Mode
Shunt JB 1-2 = Output Mode

PORT B DRIVER/RECEIVER LOC. 10B, 11A

74LS243 Non Inverting
74LS242 Inverting

PORT B TERMINATION OPTIONS LOC. 11B

Open No Termination
Beckman 899-1-R1.0K Pull Up Termination
Beckman 899-5-R2201220 2201330 Pull Up/Dow
Termination

PARALLEL PORT C SELECT LOC. 13.5A

No Shunts = Bit Unused
Shunts = PCX Input Receiver

Shunts = PCX Output Receiver

PORT C DRIVER/RECEIVER LOC. 13A

74LS244 Non Inverting
74LS240 Inverting

PORT C TERMINATION OPTIONS LOC. 12A

Open No Termination
1K Pull Up Termination
2201330 Pull Up/Down Termination

Note: For more detail regarding the programming of the 8255A see the intel Peripheral Design Handbook

MODEL 440 I/O BOARD SHUNT AND JUMPER OPTIONS

JG

1	A15	o o	14
2	A14	o o	13
3	A13	o o	12
4	A12	o o	11
5	A11	o o	10
6	A10	o o	9
7	RE	o o	8

JH

1	o—o	4
2	o o	3

JJ-JN

1	V17	o o	16
2	V16	o o	15
3	V15	o o	14
4	V14	o o	13
5	V13	o o	12
6	V12	o o	11
7	V11	o o	10
8	V10	o o	9

JP

1	A7	o o	8
2	A6	o o	7
3	A5	o o	6
4	A4	o o	5

ROM SELECT LOC. 6.5B

2708 1K x 8 Etch Jumper JD 1-3 VBB = -5
JE 1-2 VDD = +12
JF 1-2 A10
JF 3-4 A11

2716 2K x 8 Cut Etch Jumper
JD 1-3 Add JD 3-4 +5
JE 1-2 JE 2-3 A10
JF 3-4

2732 4K x 8 Cut Etch Jumper
JD 1-2 Add JD 2-3 A11
JE 1-2 JE 2-3 A10
JF 1-2
JF 3-4

ROM ADDRESS SELECT LOC. 9.5C

Shunt Off = 1 Shunt On = 0
(All Shunts Off = ROM Starting Address $FC00_{16}$)
All Shunts On = ROM Starting Address 0000_{16})

RE-ROM ENABLE

Shunt Off ROM Disabled, Shunt On ROM Enabled

TIMER CLOCK OPTION LOC. 2C

Etch Jumper JH 1-4 = External 2Mhz
Cut Etch Jumper JH 1-4 Jumper JH 2-3
Add OSC at 1SD and 74LS161 at 13C
For Internal Timer Clock

INTERRUPT OPTIONS LOC. 2D, 3D

The installing of a shunt will attach the select interrupt level to the function as defined below:

JJ - Real Time Clock Interrupt
JK - Line 0 Transmit/Receive Interrupt
JL - Line 1 Transmit/Receive Interrupt
JM - Parallel Port B Interrupt (PCD $INTR_B$)
JN - Parallel Port A Interrupt (PC3 $INTR_A$)

I/O DEVICE ADDRESS SELECT LOC. 5.5D

Shunt Off = 1 Shunt On = 0
(All Shunts Off = I/O Address $F0\text{-}FF_{16}$)
(All Shunts On = I/O Address $00\text{-}oF_{16}$)

I/O DEVICE ADDRESS

X0	COMM	0	R/W CTRL	-- 6402
X1	COMM	0	R/W DATA	
X2	COMM	1	R/W CTRL	
X3	COMM	1	R/W DATA	
X4	TIMER	0	R/W DATA (BAUD CLOCK X 16 COMM 0)	-- 8253
X5	TIMER	1	R/W DATA (BAUD CLOCK X 16 COMM 1)	
X6	TIMER	2	R/W DATA (RTC)	
X7	TIMER CONTROL WRITE			
X8	INTERRUPT ENABLE/REQUEST TO SEND STRL			
X9	TIMER	2	INTERRUPT RESET (RTC)	
XA				
XB				
XC	PARALLEL PORT A R/W DATA			-- 8255
XD	PARALLEL PORT B R/W DATA			
XE	PARALLEL PORT C R/W DATA			
XF	PARALLEL CONTROL WRITE			

X = SHUNT SELECTED

MODEL 440 I/O BOARD PARALLEL PORT CONNECTOR PIN LISTING

1.	+5VDC	2.	+5VDC
3.	PA7	4.	GND
5.	PA6	6.	GND
7.	PA5	8.	GND
9.	PA4	10.	GND
11.	PA3	12.	GND
13.	PA2	14.	GND
15.	PA1	16.	GND
17.	PA0	18.	GND
19.	PB7	20.	GND
21.	PB6	22.	GND
23.	PB5	24.	GND
25.	PB4	26.	GND
27.	PB3	28.	GND
29.	PB2	30.	GND
31.	PB1	32.	GND
33.	PB0	34.	GND
35.	PC7	36.	GND
37.	PC6	38.	GND
39.	PC5	40.	GND
41.	PC4	42.	GND
43.	PC3	44.	GND
45.	PC2	46.	GND
47.	PC1	48.	GND
49.	PC0	50.	GND

PAX PARALLEL PORT A BITS
PBX PARALLEL PORT B BITS
PCX PARALLEL PORT C BITS

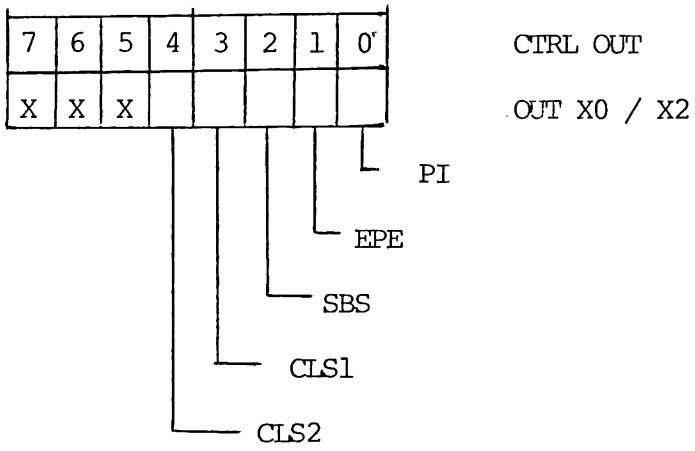
STANDARD ASSIGNMENTS

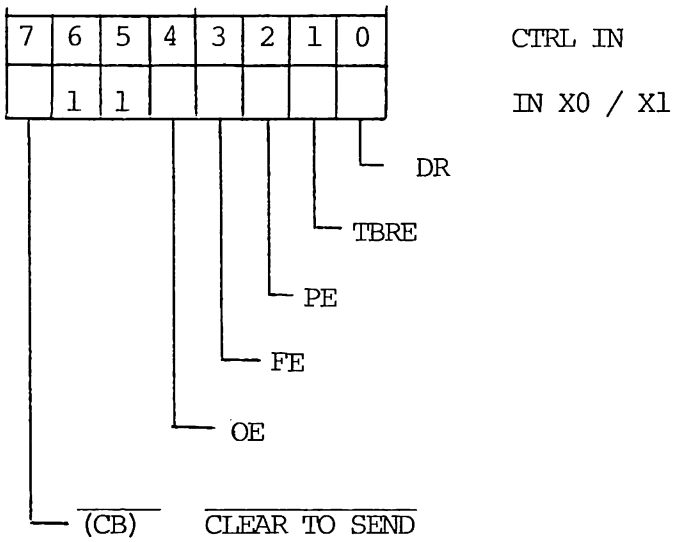
INTERRUPTS

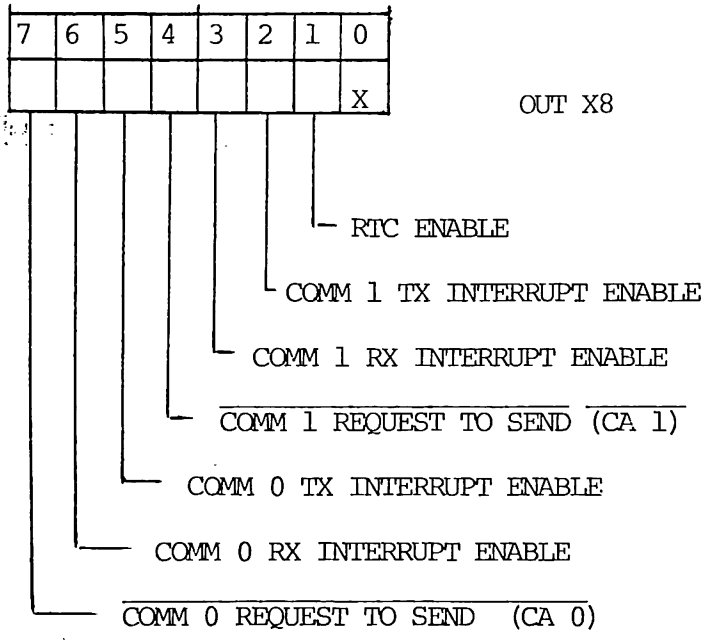
VI0	00	POWER ON
VI1	08	
VI2	10	
VI3	18	PRINTER
VI4	20	EXTERNAL COMMUNICATION
VI5	28	EXTERNAL RTC
VI6	30	COMMUNICATION
VI7	38	RTC

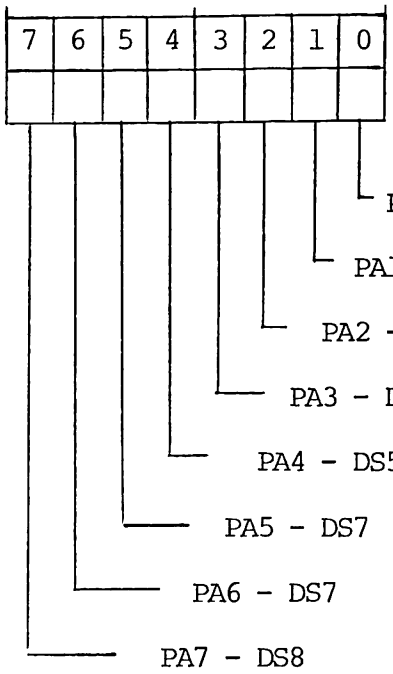
I/O DEVICE ADDRESS

10	COMM 0 R/W CTRL
11	COMM 0 R/W DATA
12	COMM 1 R/W CTRL
13	COMM 1 R/W DATA
14	TIMER 1 R/W
15	TIMER 1 R/W
16	TIMER 2 R/W
17	TIMER CTRL
18	INTERRUPT MASK / CA CTRL

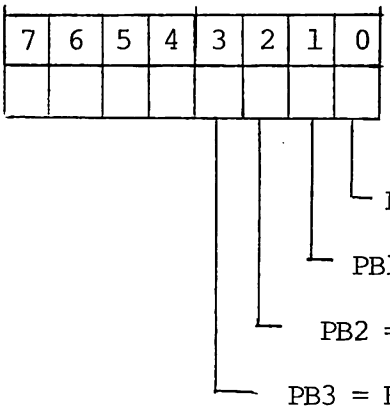

7 6 5 4 3 2 1 0
X X X
CTRL OUT
OUT X0 / X2
PI
EPE
SBS
CLS1
CLS2


7 6 5 4 3 2 1 0
1 1
CTRL IN
IN X0 / X1
DR
TBRE
PE
FE
OE
(CB)
CLEAR TO SEND


7 6 5 4 3 2 1 0
X
OUT X8
RTC ENABLE
COMM 1 TX INTERRUPT ENABLE
COMM 1 RX INTERRUPT ENABLE
COMM 1 REQUEST TO SEND (CA 1)
COMM 0 TX INTERRUPT ENABLE
COMM 0 RX INTERRUPT ENABLE
COMM 0 REQUEST TO SEND (CA 0)



PA PORT OUTPUT MODE 1

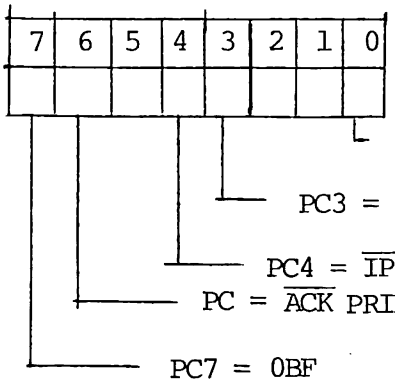


PB PORT INPUT MODE 0

A						2	
7	6	5	4	3	2	1	0
1	0	1	0	0	0	1	0

CONTROL WORD

PORT A OUTPUT MODE 1
PORT B INPUT MODE 0
PORT C UPPER OUTPUT
PORT C LOWER OUTPUT



PC PORT CONTROL

PC0 = $\overline{\text{DSTA}}$ DATA STROBE PULE OUT

PC3 = INTR = VI3 INTERRUPT LOCATION 18 OUT

PC4 = $\overline{\text{IP}}$ INITIALIZE PRINTER OUT

PC = $\overline{\text{ACK}}$ PRINTER ACKNOWLEDGE PULSE / INTE IN/OUT

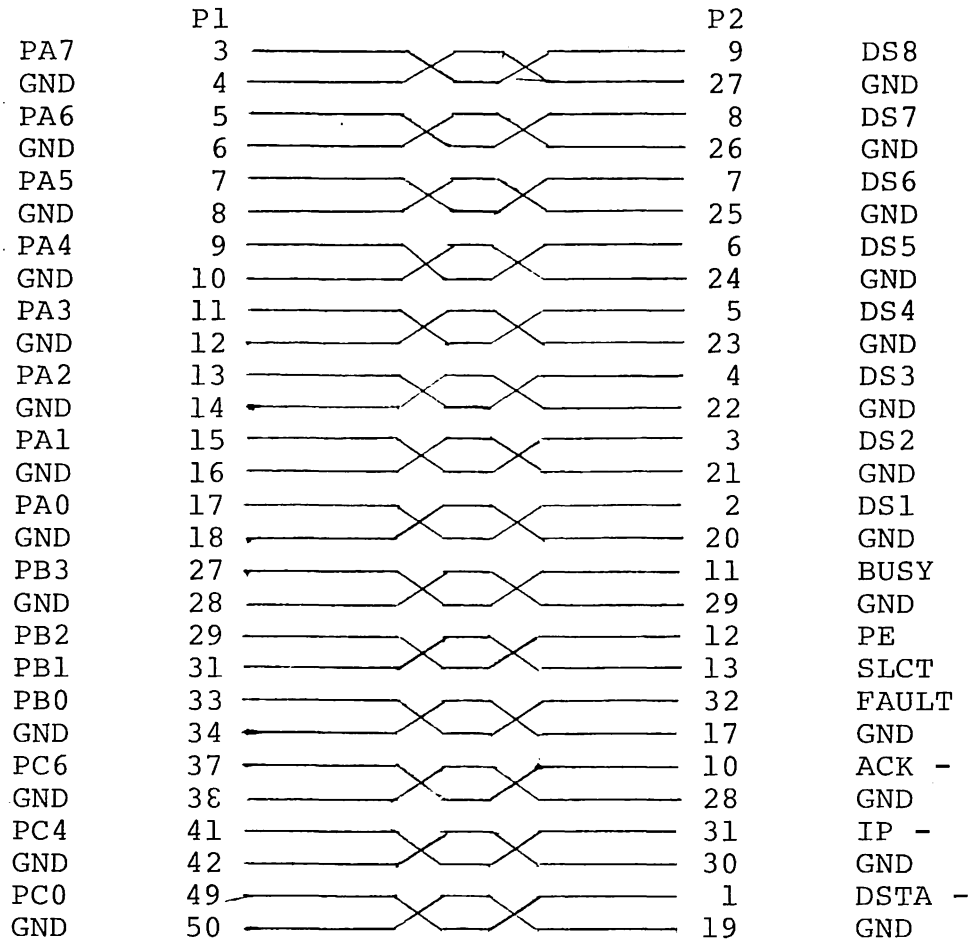
PCX BIT SET/RESET FORMAT FOR CENTRONICS PRINTER

	7	6	5	4	3	2	1	0	
	0				0				
	0	X	X	X	0	0	0	0	CONTROL DEVICE ADDRESS XF
	0	X	X	X	0	0	0	0	RESET PC0 $\overline{DSTA}$
	0				1				
	0	X	X	X	0	0	0	1	SET PC0 $\overline{DSTA}$
	0				8				
	0	X	X	X	1	0	0	0	RESET PC4 $\overline{IP}$
	0				9				
	0	X	X	X	1	0	0	1	SET PC4 $\overline{IP}$
	0				C				
	0	X	X	X	1	1	0	0	RESET PC6 INTE
	0				D				
	0	X	X	X	1	1	0	1	SET PC6 INTE

PCX SHUNTS FOR CENTRONICS PRINTER

1. SHUNT PC3 (INTR) TO INTERRUPT VI3 LOCATION 18 JN 5-12
2. SHUNT PAI TO GND SO PAX = OUTPUT JA 1-4
3. INSTALL 74LS244 FOR PC DRIVER
4. SHUNT PC0 JC 1-2 $\overline{DSTA}$
   JC 31-32
   PC4 JC 9-10 $\overline{IP}$
   JC 23-24
   PC6 JC 13-20 $\overline{ACK}$
   JC 14-19

CENTRONICS PRINTER CABLE



14 TWP
CABLE

HOUSING

AMP 4-87456-6 AMPHENAL CONNECTOR

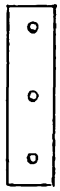
CONTACTS 57-30360

AMP 1-87309-4

MODEL 450 Z80 CPU BOARD

SHUNT AND JUMPER OPTIONS

JA — WAIT STATE SELECT — LOC. 2.5A

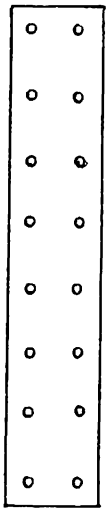


No Shunts = No Memory Wait State

Shunt JA 1-2 = Provides One Wait State

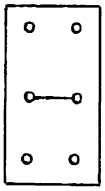
Shunt JA 2-3 = Provides Two Wait States

JB — POWER ON ADDRESS SELECT — LOC. 9.5A



16	A15	Shunt Off = 1 Shunt On = 0
15	A14	(All Shunts Off Power On Address = $FF00_{16}$)
14	A13	(All Shunts On Power On Address = 0000_{16})
13	A12	
12	A11	
11	A10	
10	A 9	
9	A 8	

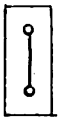
JC — CPU CLOCK SELECT: — LOC. 3.5B



6	
5	4MHZ
4	2MHZ

Cut Etch Jumper to Change CPU Clock

JD — ADDRESS MIRROR SELECT — LOC. 3.5B



Cut Etch Jumper for No Address Mirror

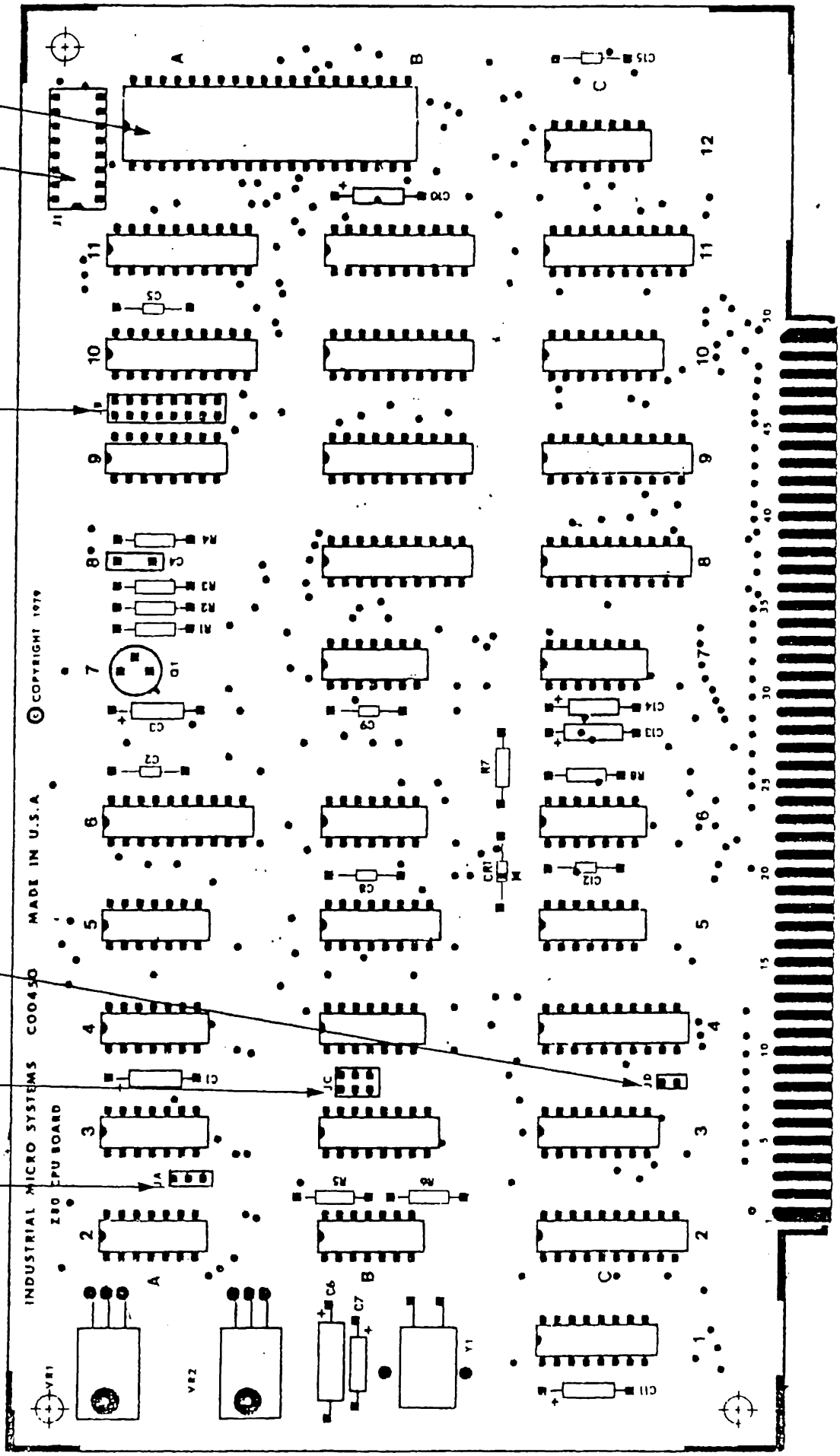
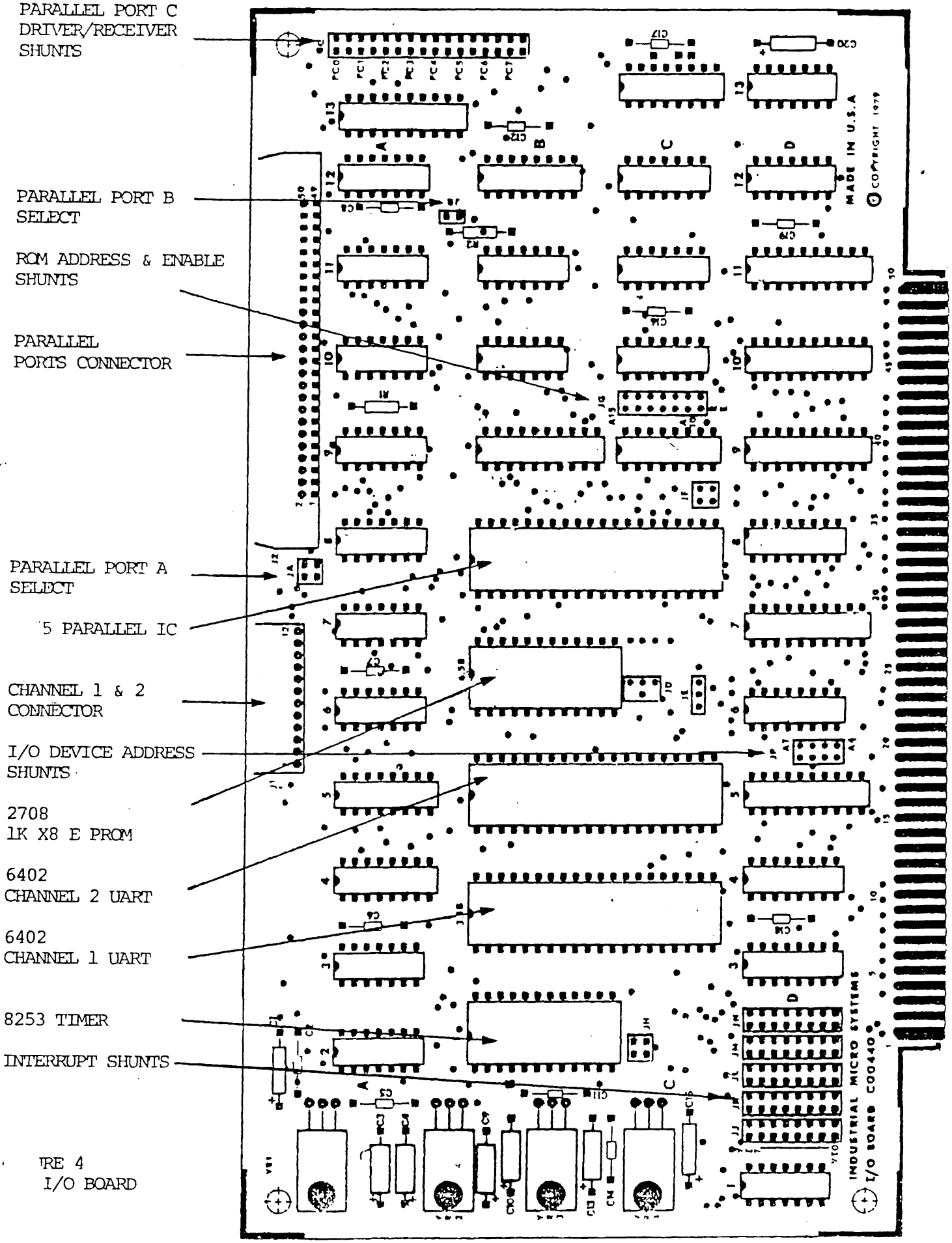
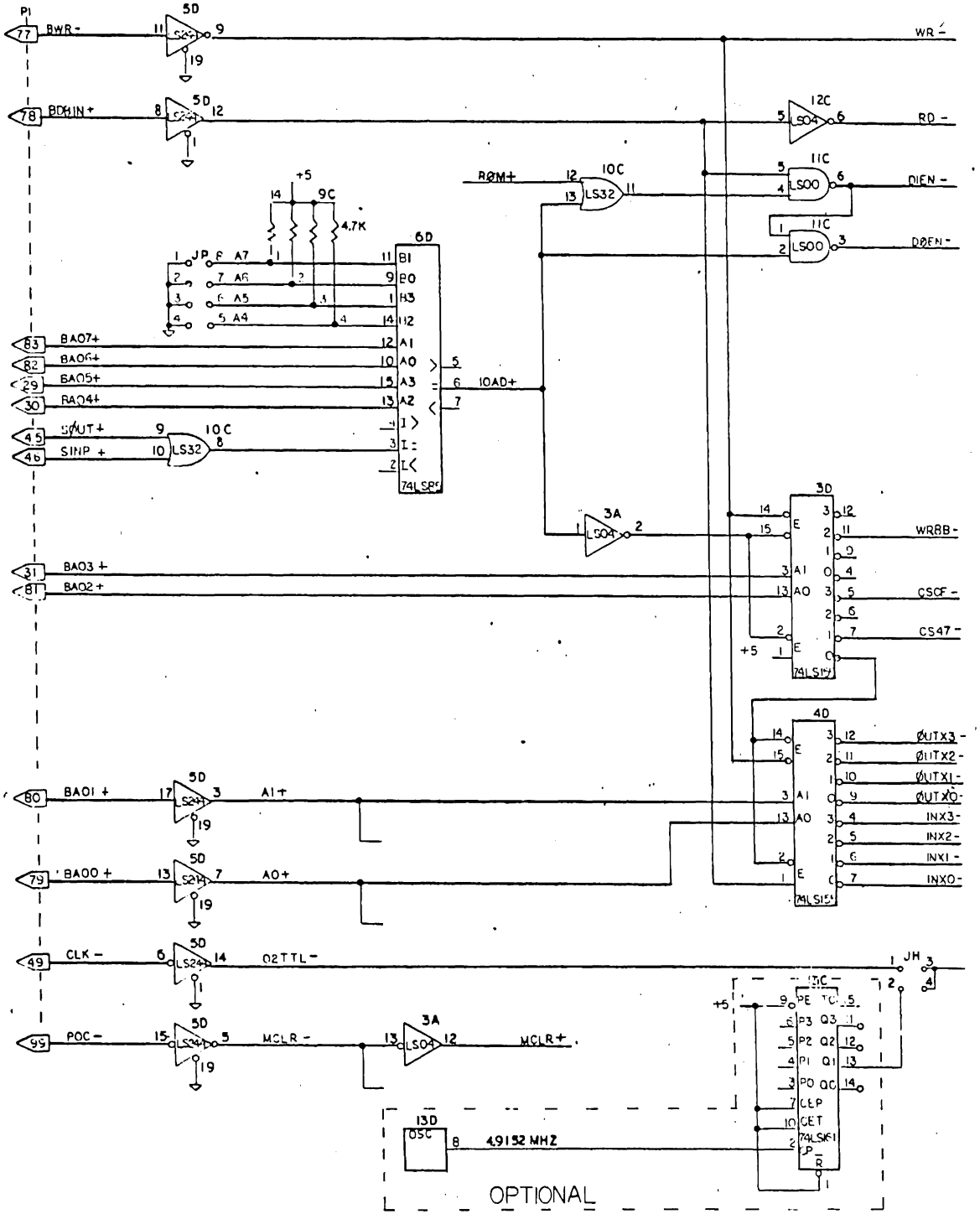


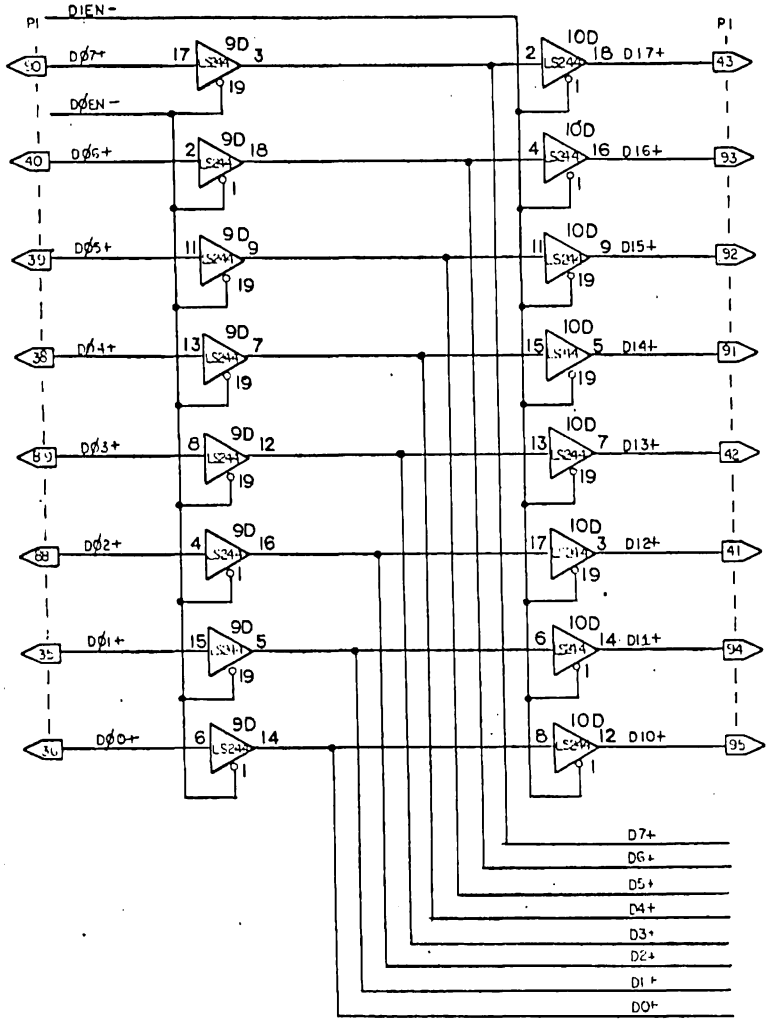
FIGURE 3
450 Z80 CPU BOARD


PARALLEL PORT C DRIVER/RECEIVER SHUNTS
PARALLEL PORT B SELECT
ROM ADDRESS & ENABLE SHUNTS
PARALLEL PORTS CONNECTOR
PARALLEL PORT A SELECT
5 PARALLEL IC
CHANNEL 1 & 2 CONNECTOR
I/O DEVICE ADDRESS SHUNTS
2708 1K X8 E PROM
6402 CHANNEL 2 UART
6402 CHANNEL 1 UART
8253 TIMER
INTERRUPT SHUNTS
MADE IN U.S.A
COPYRIGHT 1979
INDUSTRIAL MICRO SYSTEMS
I/O BOARD C00440

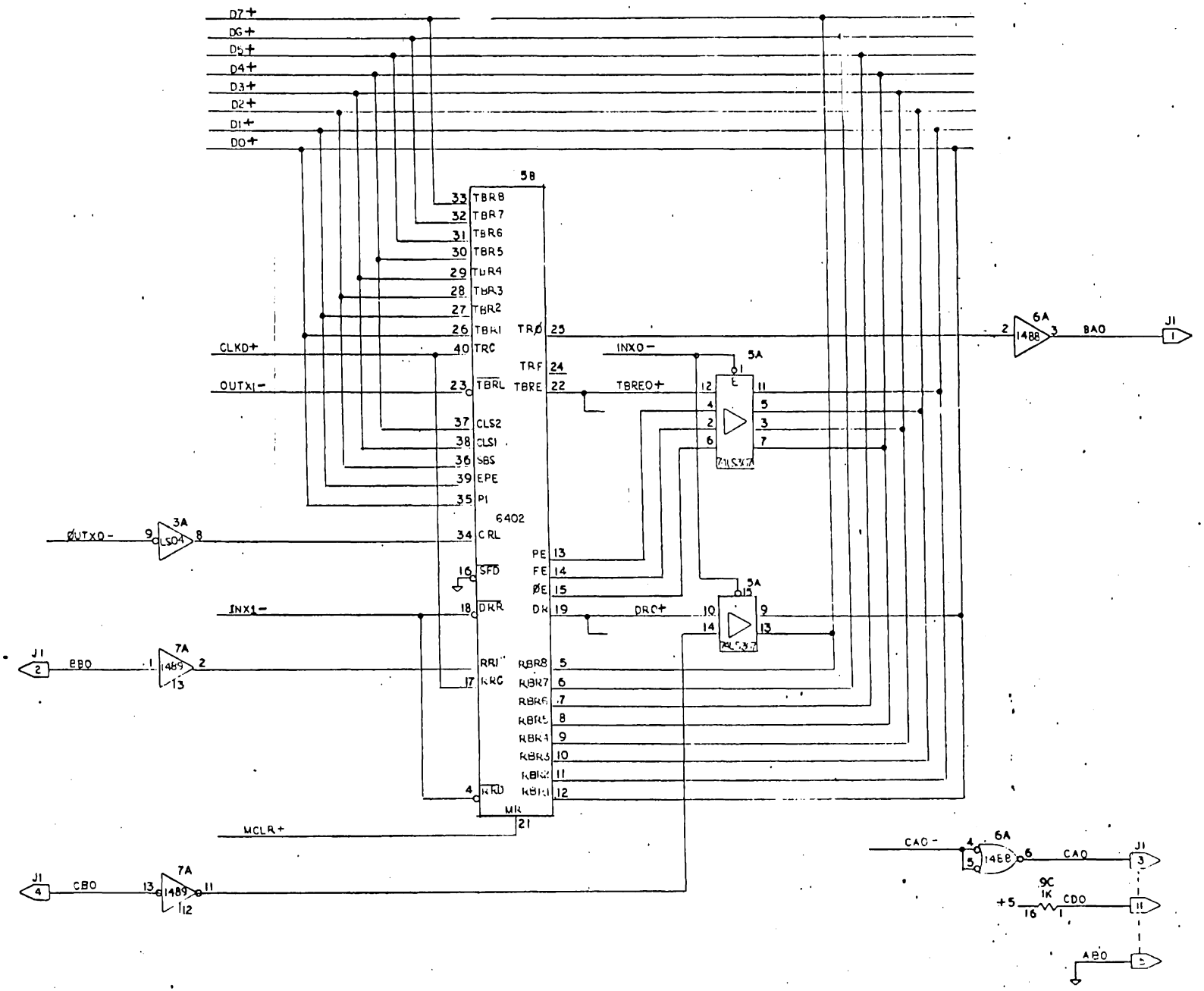
RE 4
I/O BOARD

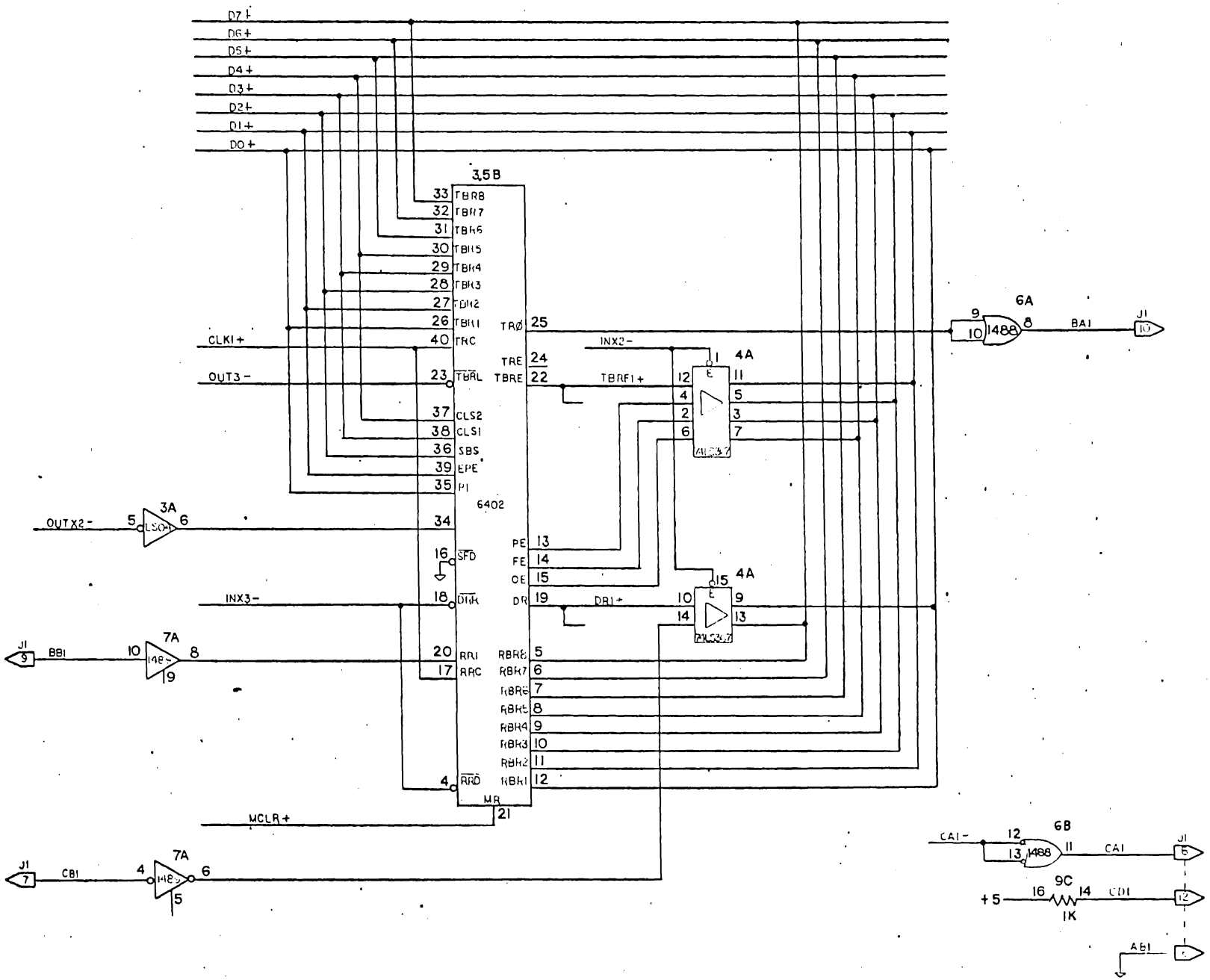


INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED
I/O BOARD		
L00442		DRAWING NUMBER 1 OF 9



INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED
I/O BOARD		
L00442		DRAWING NUMBER 2 OF 9


D7+
D6+
D5+
D4+
D3+
D2+
D1+
D0+
5B
6402
TBR8
TBR7
TBR6
TBR5
TBR4
TBR3
TBR2
TBR1
TRC
TBRL
CLS2
CLS1
SBS
EPE
PI
CRL
SFD
DRR
RRI
RRC
RRD
MR
TRØ
TRF
TBRE
PE
FE
ØE
DR
RBR8
RBR7
RBR6
RBR5
RBR4
RBR3
RBR2
RBR1
CLKD+
OUTXI-
ØUTXO-
INXI-
MCLR+
INXO-
TBREO+
DRC+
J1
EBO
CBO
BAO
CAO
CDO
ABO
3A
5A
6A
7A
9C
1488
1489
LS04
LS367
1K
+5
6402
VCC 1
GND 3
1488
VCC -14 -+12
VEL -1 --12
GND -7
INDUSTRIAL MICRO SYSTEMS
SCALE:
APPROVED BY:
DRAWN BY
DATE: 4-12-79
REVISED
I/O BOARD
LC0442
DRAWING NUMBER
3 OF 9



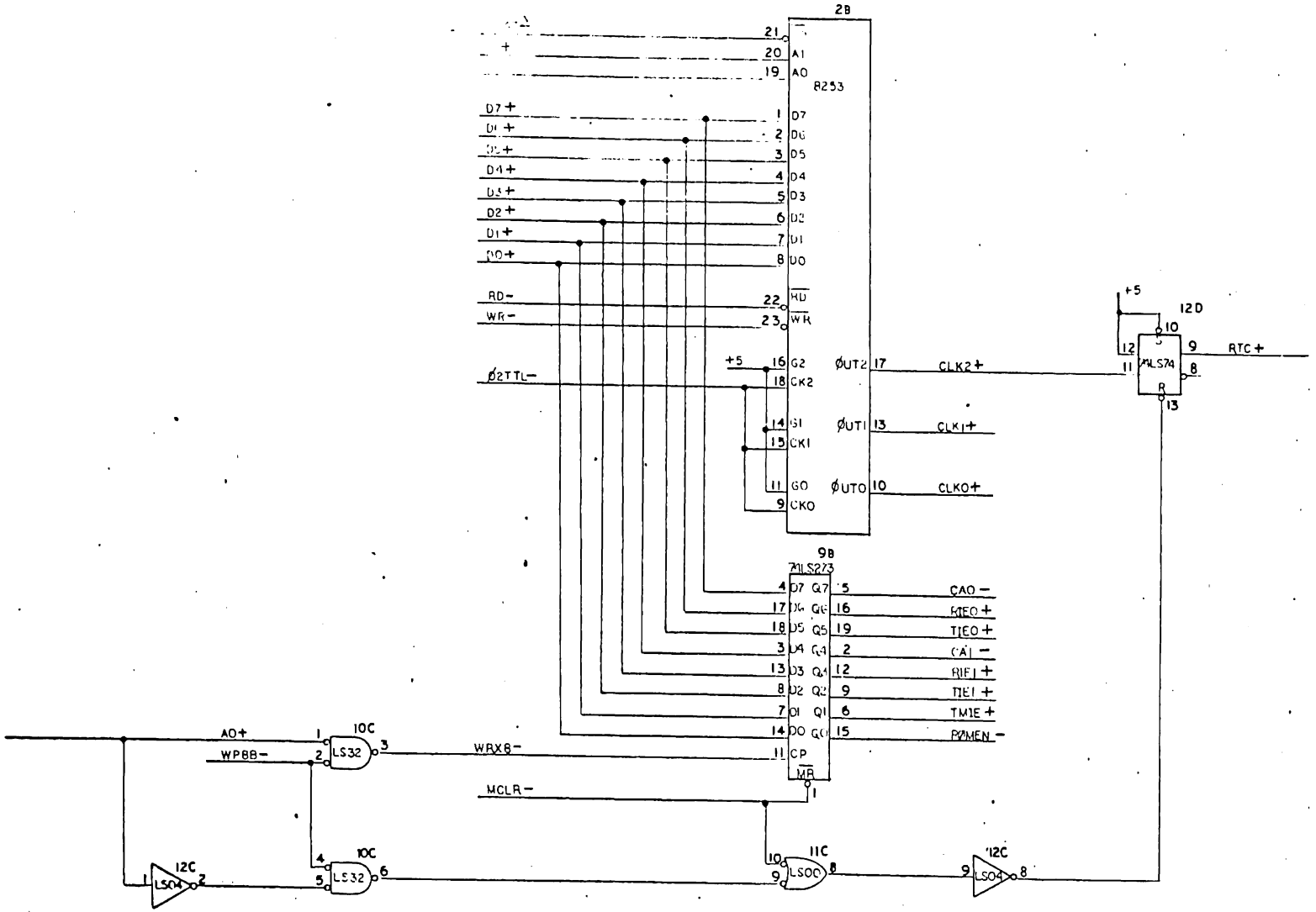
INDUSTRIAL MICRO SYSTEMS

SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED

I/O BOARD

L00442

DRAWING NUMBER 1 9



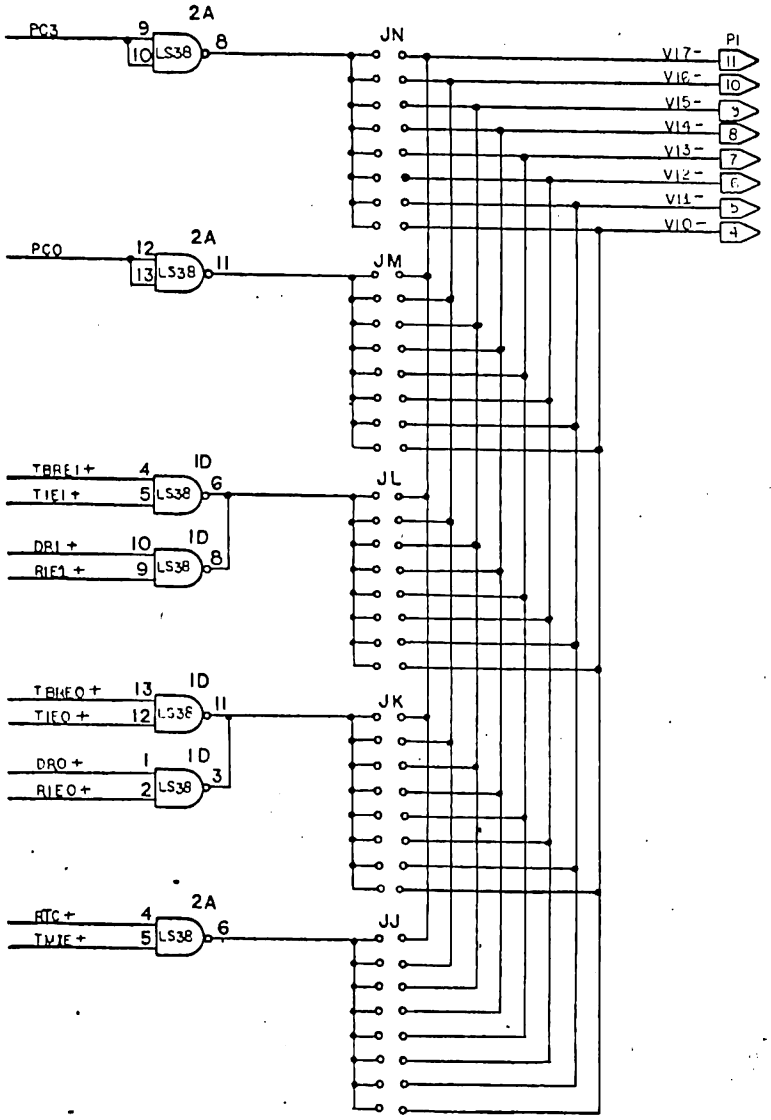
INDUSTRIAL MICRO SYSTEMS

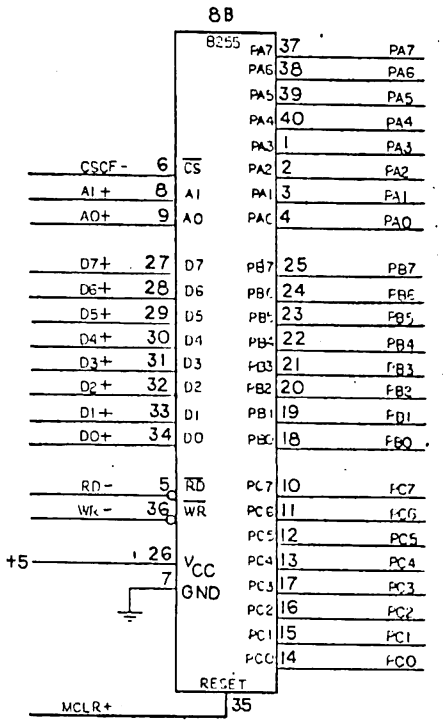
SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED

I/O BOARD

LOC442

DRAWING NUMBER 5-9





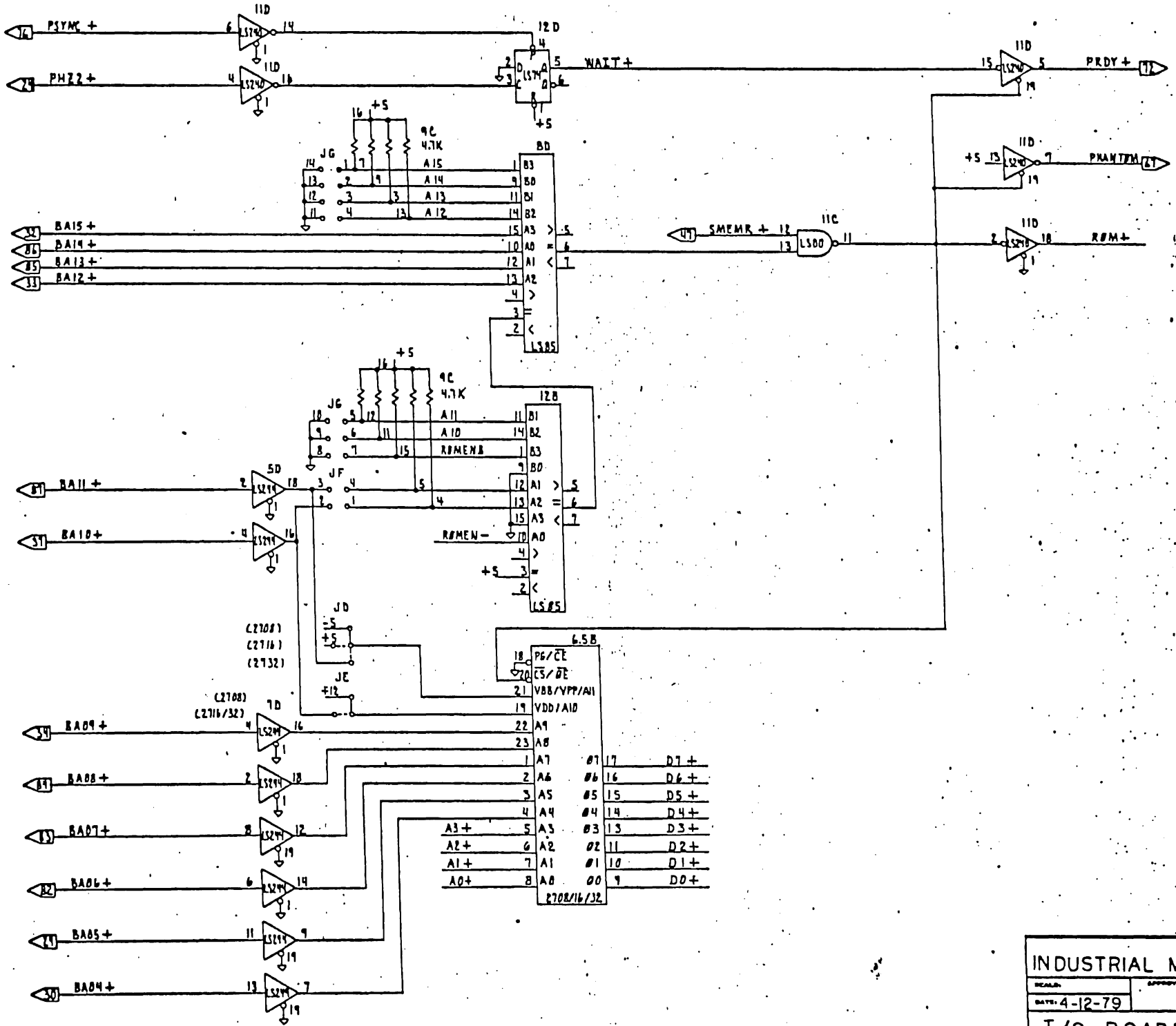
INDUSTRIAL MICRO SYSTEMS

SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED

I/O BOARD

L00442

DRAWING NUMBER 6 OF 9

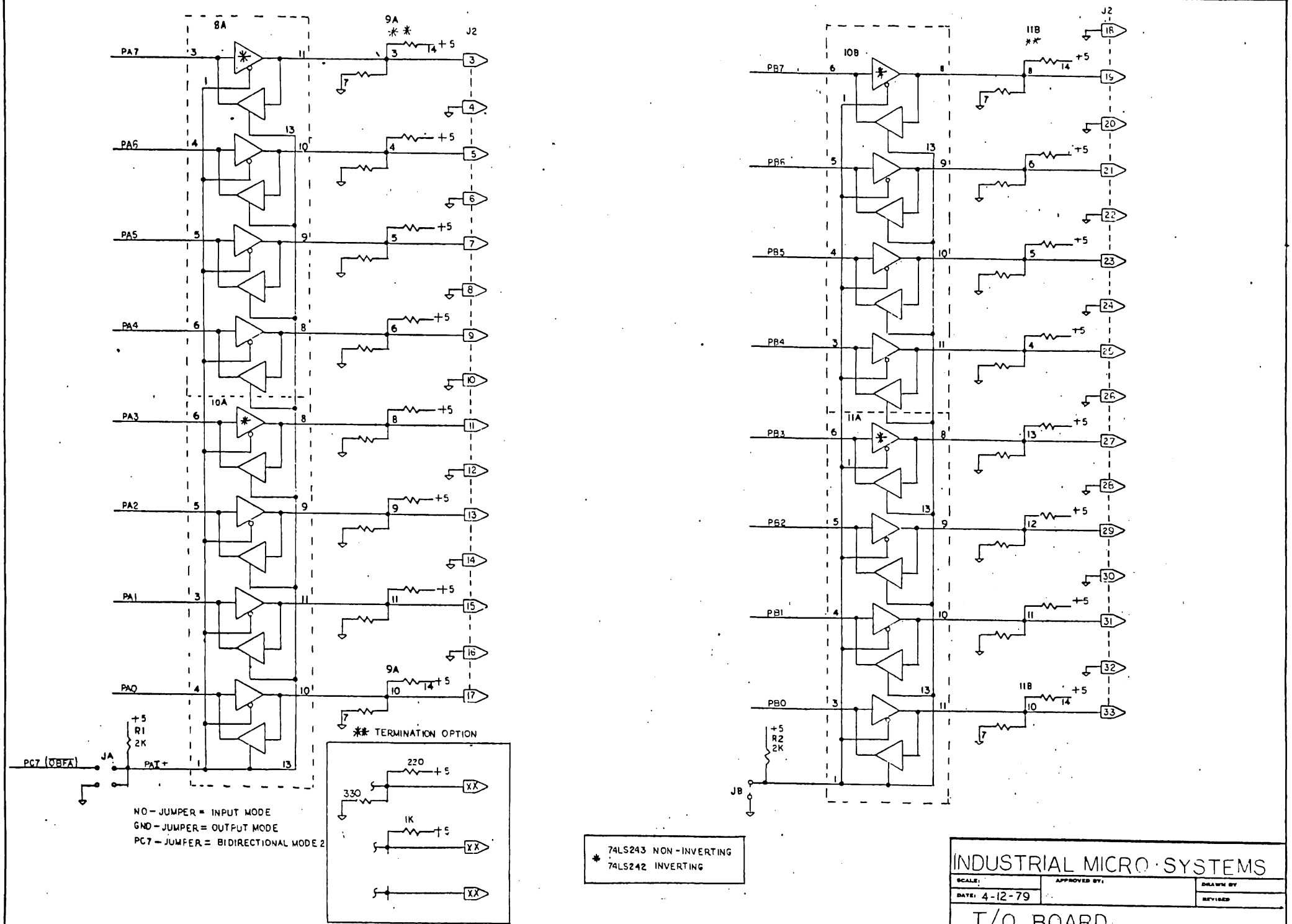


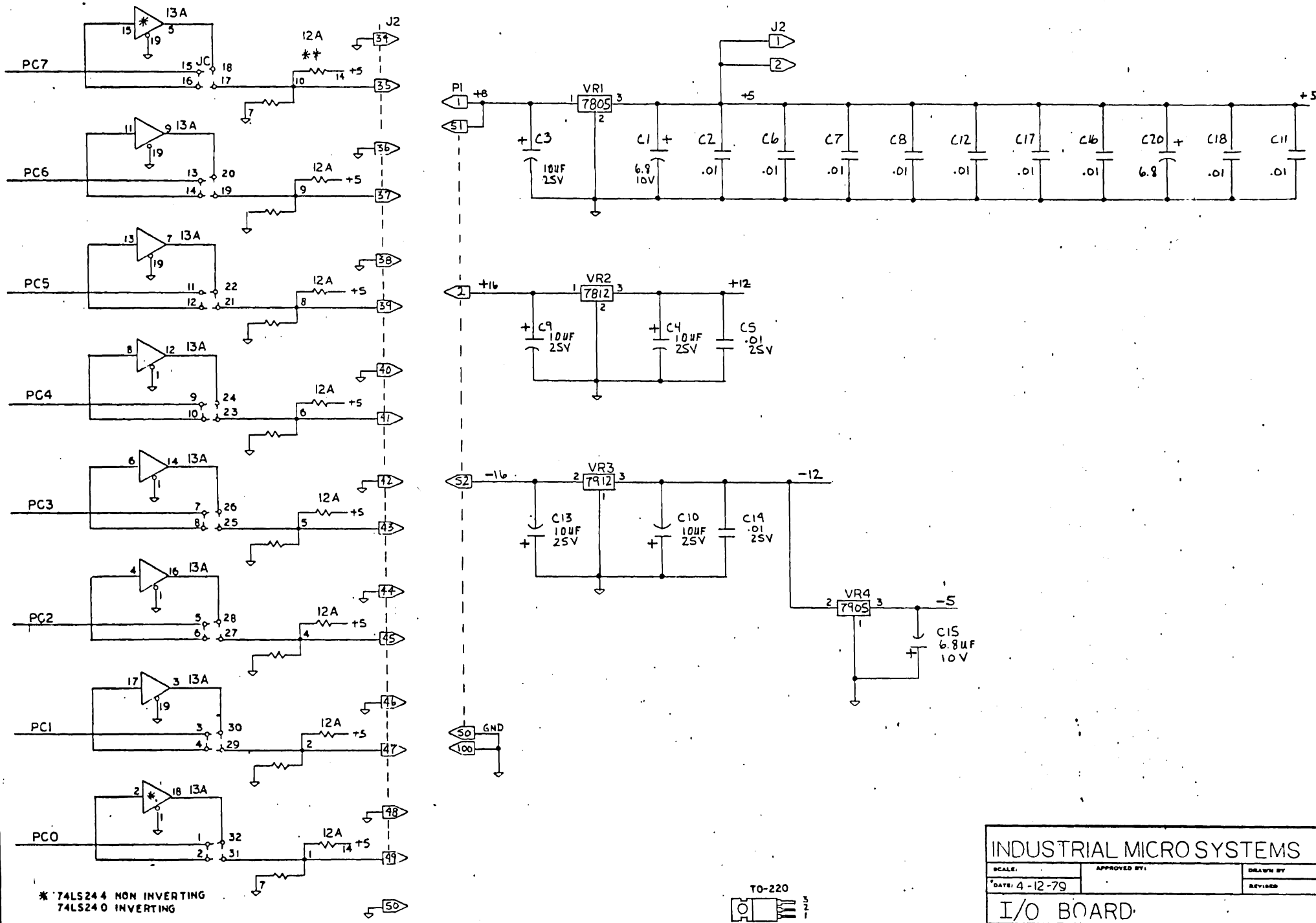
INDUSTRIAL MICRO SYSTEMS

SCALE:	APPROVED BY:	DRAWN BY:
DATE: 4-12-79		REVISION:

I/O BOARD

L00443


8A
9A
J2
PA7
PA6
PA5
PA4
10A
PA3
PA2
PA1
PA0
+5
R1
2K
PC7 (OBFA)
JA
PA I+
NO - JUMPER = INPUT MODE
GND - JUMPER = OUTPUT MODE
PC7 - JUMPER = BIDIRECTIONAL MODE 2
** TERMINATION OPTION
220
330
1K
XX
11B
10B
11A
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
R2
2K
JB
* 74LS243 NON-INVERTING
74LS242 INVERTING
INDUSTRIAL MICRO·SYSTEMS
SCALE:
APPROVED BY:
DRAWN BY
DATE: 4-12-79
REVISED
I/O BOARD
L00442
DRAWING NUMBER
8 OF 9



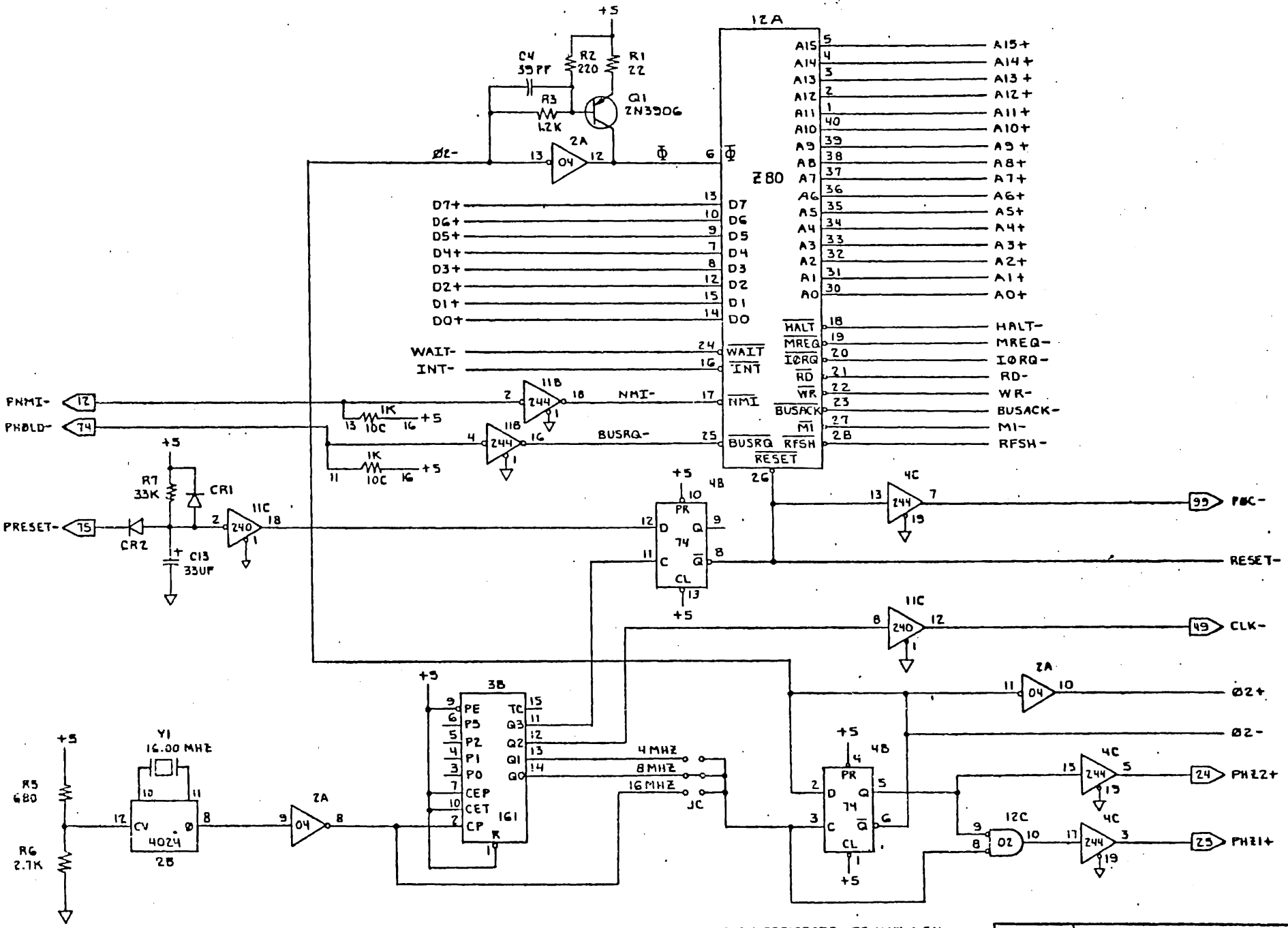
INDUSTRIAL MICRO SYSTEMS

SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED

I/O BOARD

L00442

DRAWING NUMBER 9 OF 9



1. All resistors are 1/4W ± 5%
2. All diodes are silicon switching

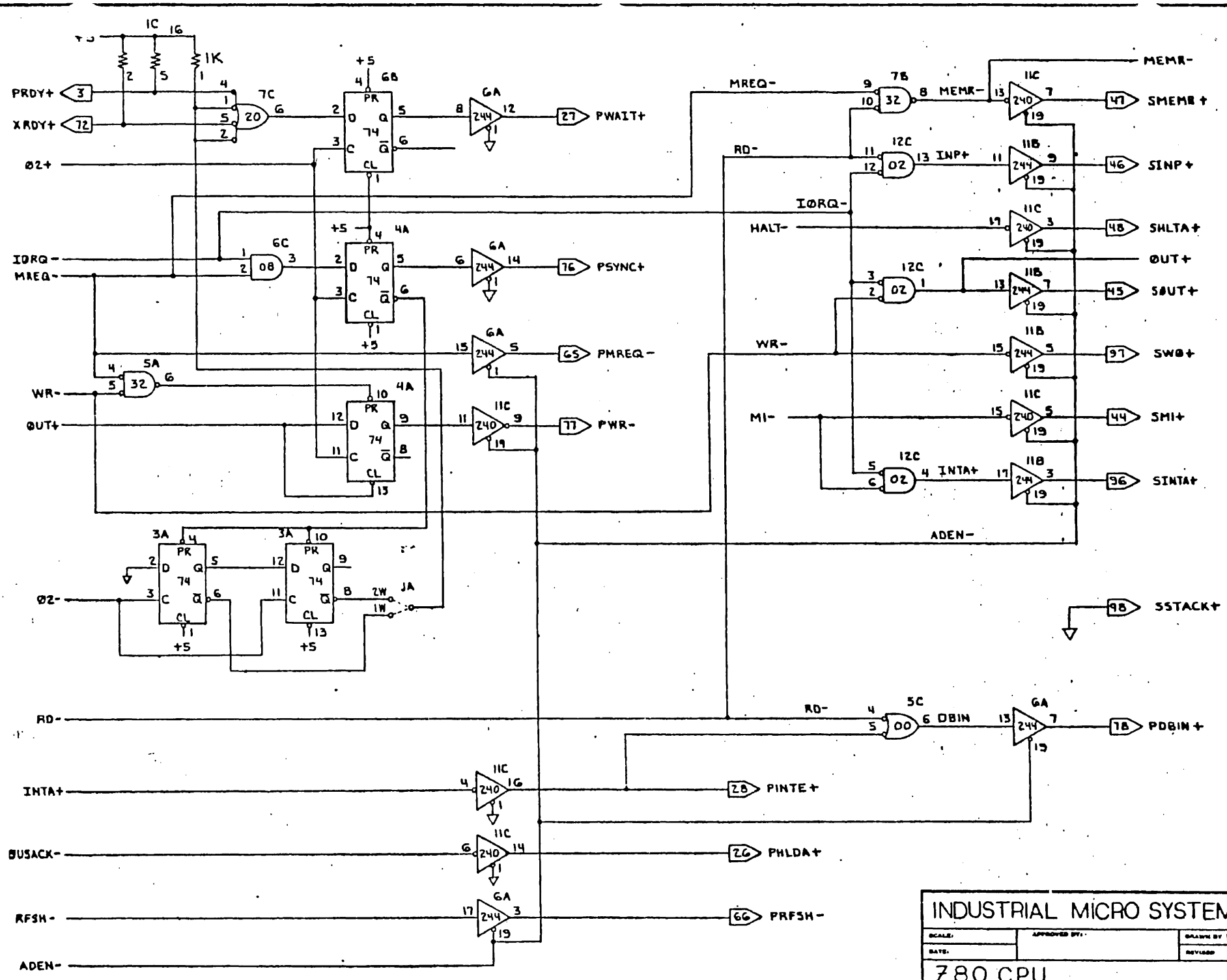
INDUSTRIAL MICRO SYSTEMS

SCALE:	APPROVED BY:	DRAWN BY RJV
DATE:		REVISED

Z80 CPU

L00450.

SHT 1 OF 4



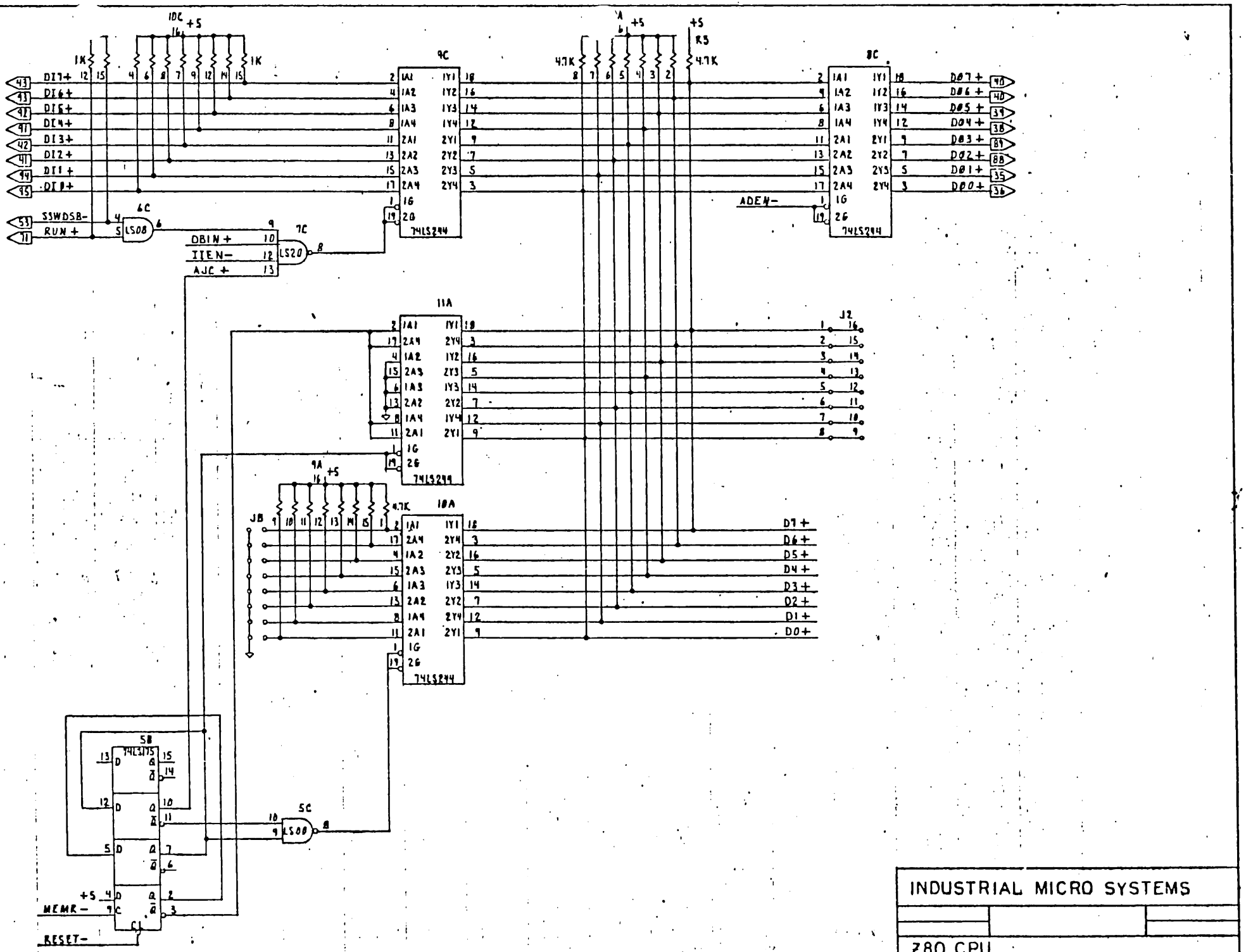
INDUSTRIAL MICRO SYSTEMS

SCALE:	APPROVED BY:	DRAWN BY RJV
DATE:		REVISED

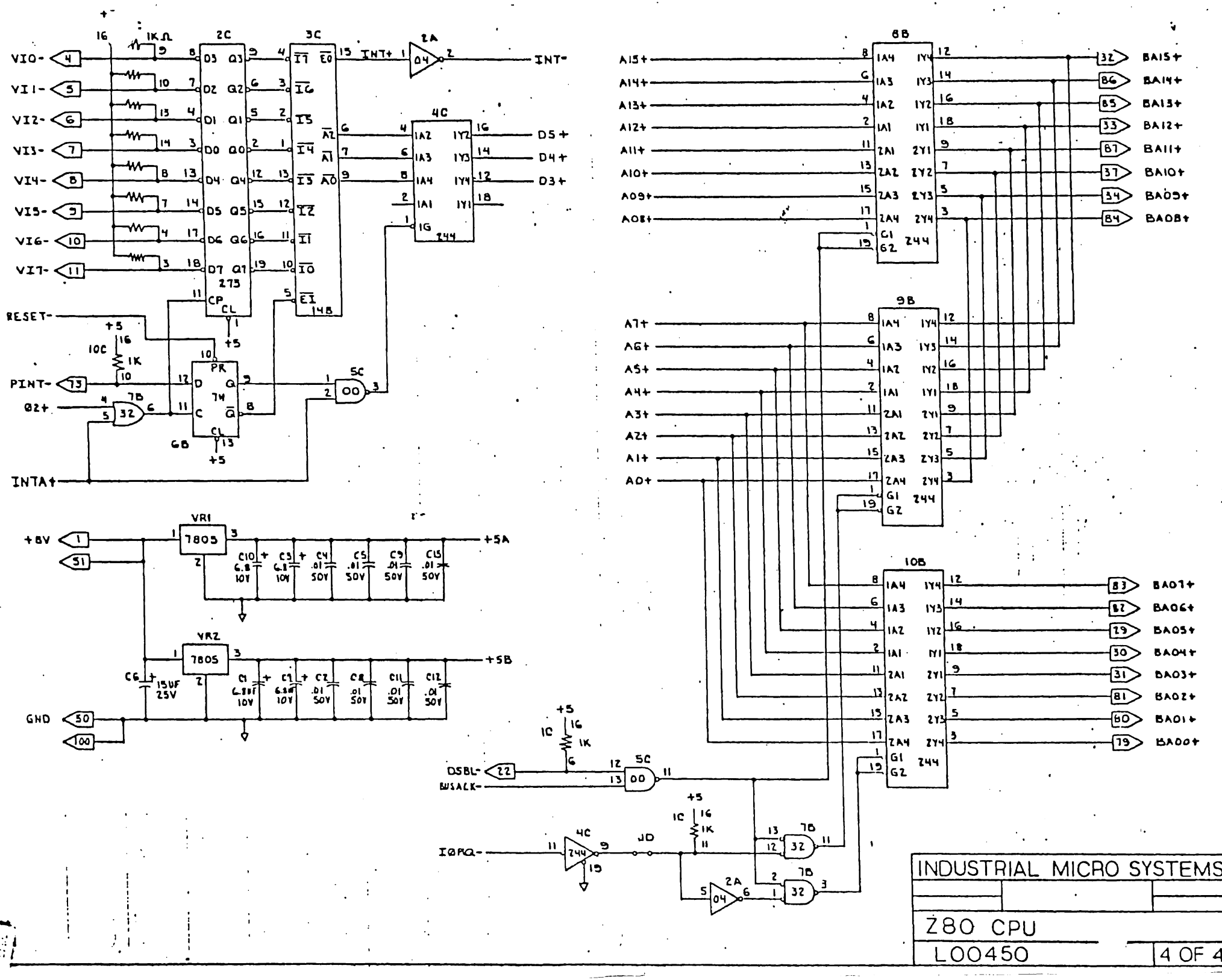
Z80 CPU

L00450

DRAWING NUMBER 2 OF 4



INDUSTRIAL MICRO SYSTEMS		
Z80 CPU		
L00450		3 OF 4



INDUSTRIAL MICRO SYSTEMS	
Z80 CPU	
L00450	4 OF 4

INDUSTRIAL MICRO SYSTEMS, INC.

MODELS 400/430

FLOPPY DISK CONTROLLER BOARDS

****

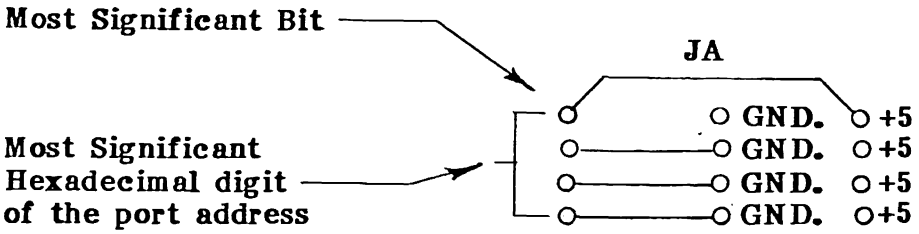
The Industrial Micro System Model 400 and 430 Floppy Disk Controllers for use with 8" and 5-1/4" Floppy Drive, are described in the following paragraphs.

The 400 and 430 are based on the NEC uPD765 Floppy Disk Controller chip providing Single and Double Density and Single and Double Sided operatin. An on-board 8257 provides DMA operation. Either board can control up to four Floppy Disk Drives.

The Model 400 and 430 boards are used in the Industrial Micro Systems Series 8000 and 5000 systems, respectively.

INPUT/OUTPUT PORT ADDRESS RANGE SELECTION

The Model 400/430 boards are etched for the use of Input/Output ports 80H through 8FH. This is accomplished at JA near the center of the board. The twelve termination points of JA are as shown in the diagram below:



If it is necessary to change the port address for the board, cuts and jumpers in the JA block will be required.

80H through 88H - These ports are used by the 8257 programmable DMA controller on the board. (See the attached write-up on the DMA controller chip for more detail).

80H -	Channel 0	DMA Register
81H -	Channel 0	Terminal Count Register
82H -	Channel 1	DMA Register
83H -	Channel 1	Terminal Count Register

	84H -	Channel 2 DMA Register	) will be reserved for
	85H -	Channel 2 Terminal Count Register	) hard disk controller
	86H -	Channel 3 DMA Register	) will be reserved for
	87H -	Channel 3 Terminal Count Register	) 2nd hard disk controller
	88H -	DMA Status and Commands	
	89H -	NOT USED	
IN	8AH -	NOT USED	

OUT 8AH - Drive select port. Data bits 0 and 1 binary weighted select one of four disk drives. All subsequent status and commands will pertain to the selected drive. These bits are latched on the board.

IN 8BH - NOT USED

OUT 8BH - Precisely the same significance as OUT 8AH described above.

IN 8CH - Board status port. This port provides status information on the drive select, 765 interrupt and drive select delay functions as follows:

DATA BIT 0 - A logical one indicates that a 765 interrupt has occurred.

DATA BIT 1 & 2 - Binary weighted to provide the infiormation on the drive 1,2, or 3 is selected.

DATA BITS 3-6 - NOT USED>

DATA BIT 7 - A logical one indicates that the floppy disk drive motors are on and the motor-control time-out is complete. If the motors are off, or the time-out is not complete, this bit will be zero. Reading this port will start the motors and reset the thirty (30) second motor-off time-out to zero. After approximately one second this delay complete bit will be set to a logical one.

OUT 8CH - Board interrupt mask. The data bits will provide information as follows:

DATA BIT 0 - A one in this position will enable a 765 interrupt on the selected vectored interrupt line. A zero disables the interrupt.

DATA BIT 1 - A one in this position enables a delay complete interrupt on the selected vectored interrupt line. Both bit 0 and 1 are latched on the board.

DATA BITS 2-7 - NOT USED

IN 8DH &
OUT 8DH - Precisely the same significance as IN 8CH and OUT 8CH as described above.

8EH &
8FH - These ports are utilized by the 765 Floppy Disk Controller chip as follows. (See attached write-up on the Floppy Controller chip for more detail).

8EH - Floppy Disk Controller main status register.

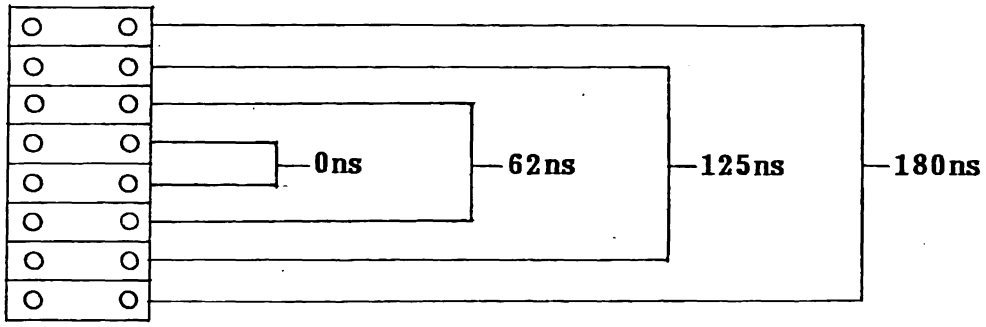
8FH - Disk data register.

VECTORED INTERRUPT JUMPER

The JB area consisting of eight shunt positions (located in the lower left hand portion of the board) is used to select one of the eight Vectored Interrupt levels to be triggered when a Floppy Disk Controller Interrupt or a Delay Complete Interrupt occur depending upon the status of the Interrupt Mask Port (OUT 8CH).

WRITE PRE-COMPENSATION JUMPERS (MODEL 400 ONLY)

The JC shunt block in the upper left hand corner of the Model 400 board is used to select the amount of write pre-comp employed. Two shunts are utilized with pre-comp selection as shown below:



The standard selection is 125 nanoseconds for operation with Shugart or Remex Floppy Disk Drives.

DOUBLE SIDED DRIVE SELECTION SHUNT (MODEL 430 ONLY)

The JC shunt position in the bottom center portion of the 430 board is used to select Single Sided (no shunt) or Double Sided (shunt installed) operation.

Single Sided/Double Sided operation is selected through a drive signal in the 50-pin cable on the Model 400 board.

MOTOR CONTROL SHUNT (MODEL 400 ONLY)

The JD shunt located in the upper right hand corner of the 400 board pertains to the Disk Drive Motor Control. With a shunt installed the Motor Control Option is disabled, and with no shunt Motor Control is enabled. Thus when the shunt is on JD, the Delay Complete Bit (DB7, IN 8CH) is always TRUE.

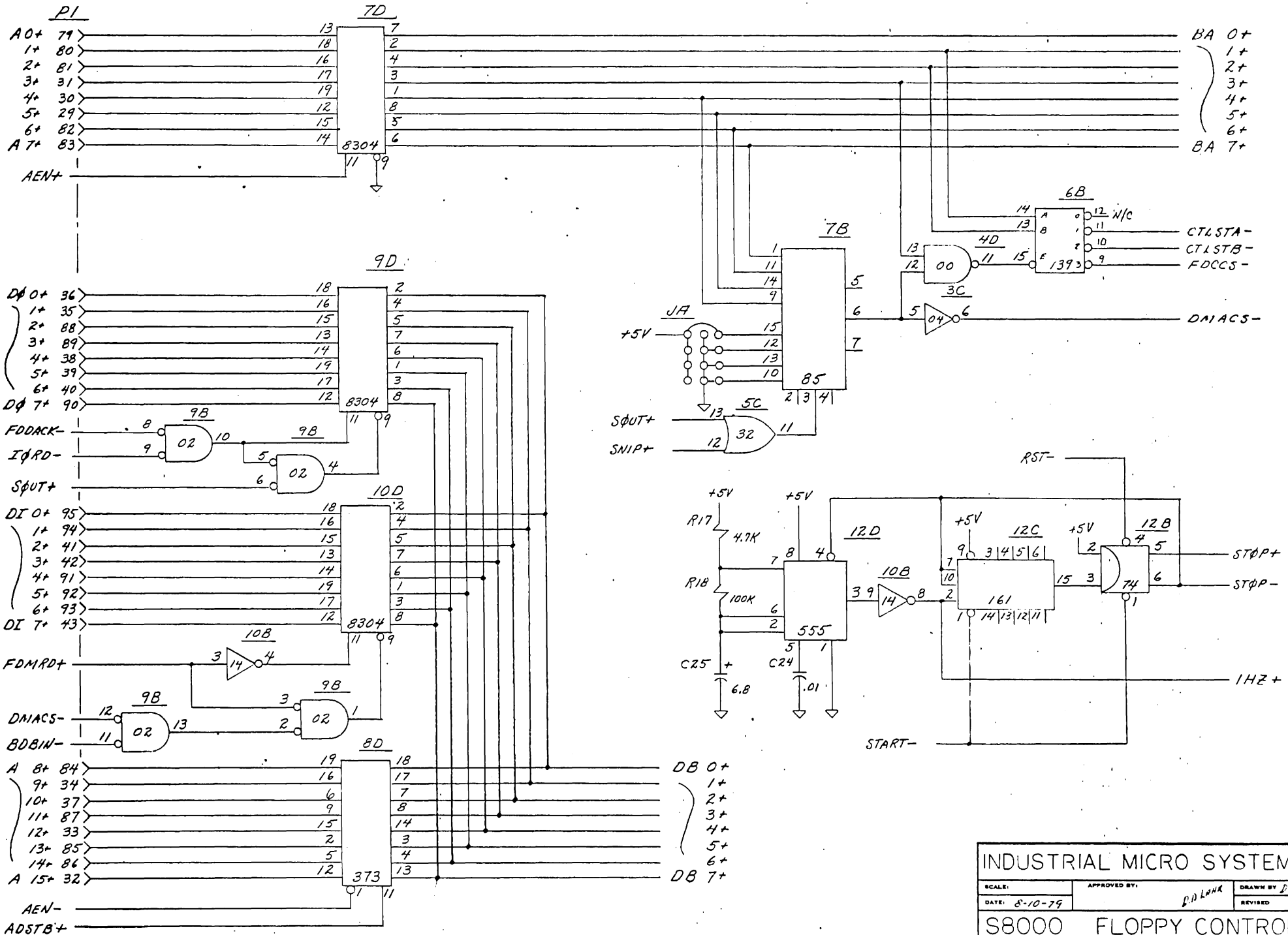
RIBBON CABLE PIN ASSIGNMENTS

The ribbon cable pin assignments for the Model 400 and Model 430 (J1 connector) are Shugart compatible as listed below:

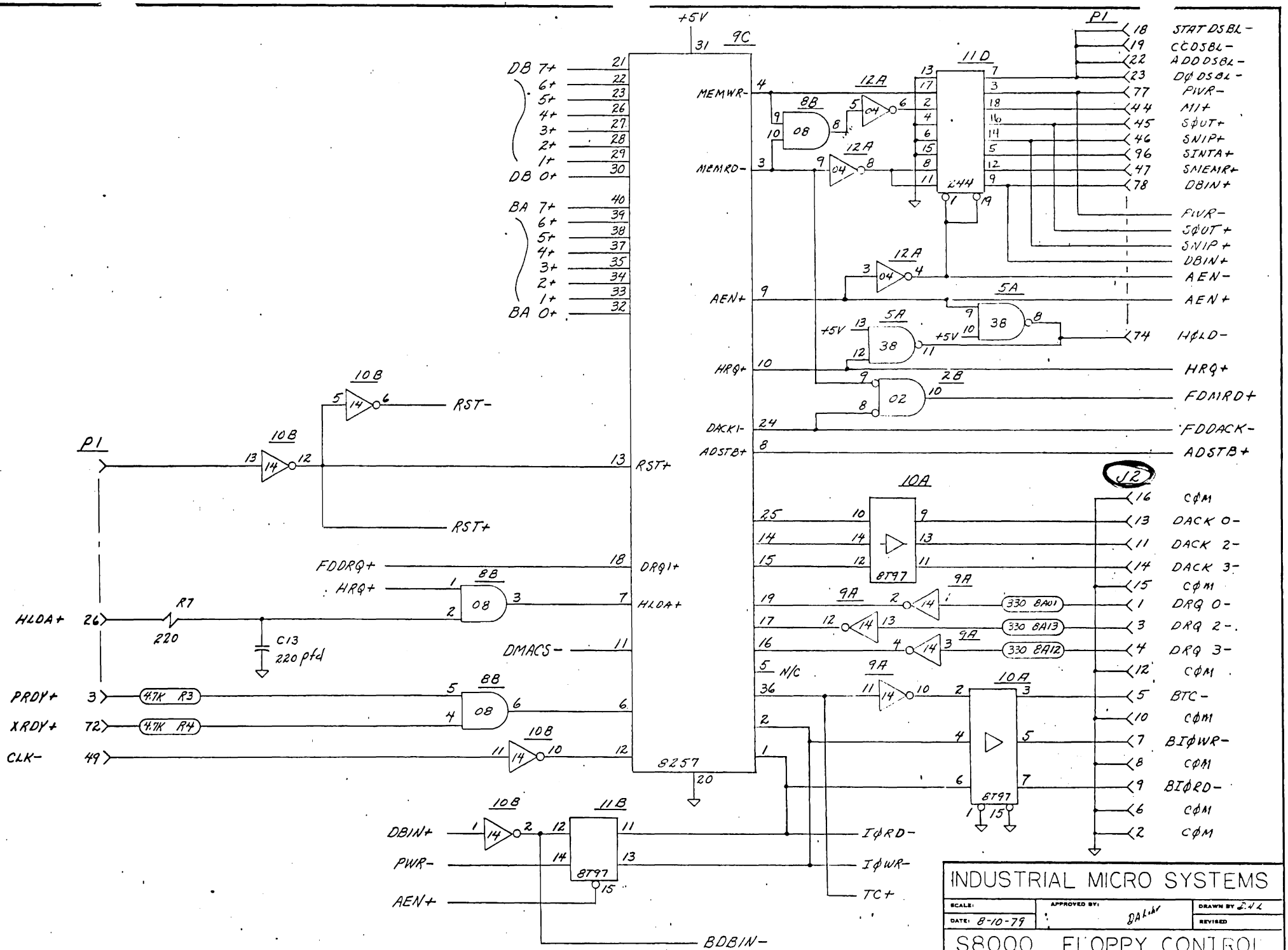
PIN	MODEL 400 (50 PIN)	MODEL 430 (34 PIN)
2	LOWCUR	SPARE
4	-	IN USE
6	-	SEL 4
8	-	INDX
10	2SIDE	SEL 1
12	DSCHG	SEL 2
14	SDE1	SEL 3
16	-	MON
18	HDLOAD	IN
20	INDX	STP
22	RDY	WDAT
24	-	WGAT
26	SEL 1	TRACK0
28	SEL 2	WPROT
30	SEL 3	RDATA
32	SEL 4	SDE1
34	IN	SEPDAT
36	STP	-
38	WDAT	-
40	WGAT	-
42	TRACK0	-
44	WPROT	-
46	RDATA	-
48	-	-
50	-	-
ALL ODD	GROUND	GROUND

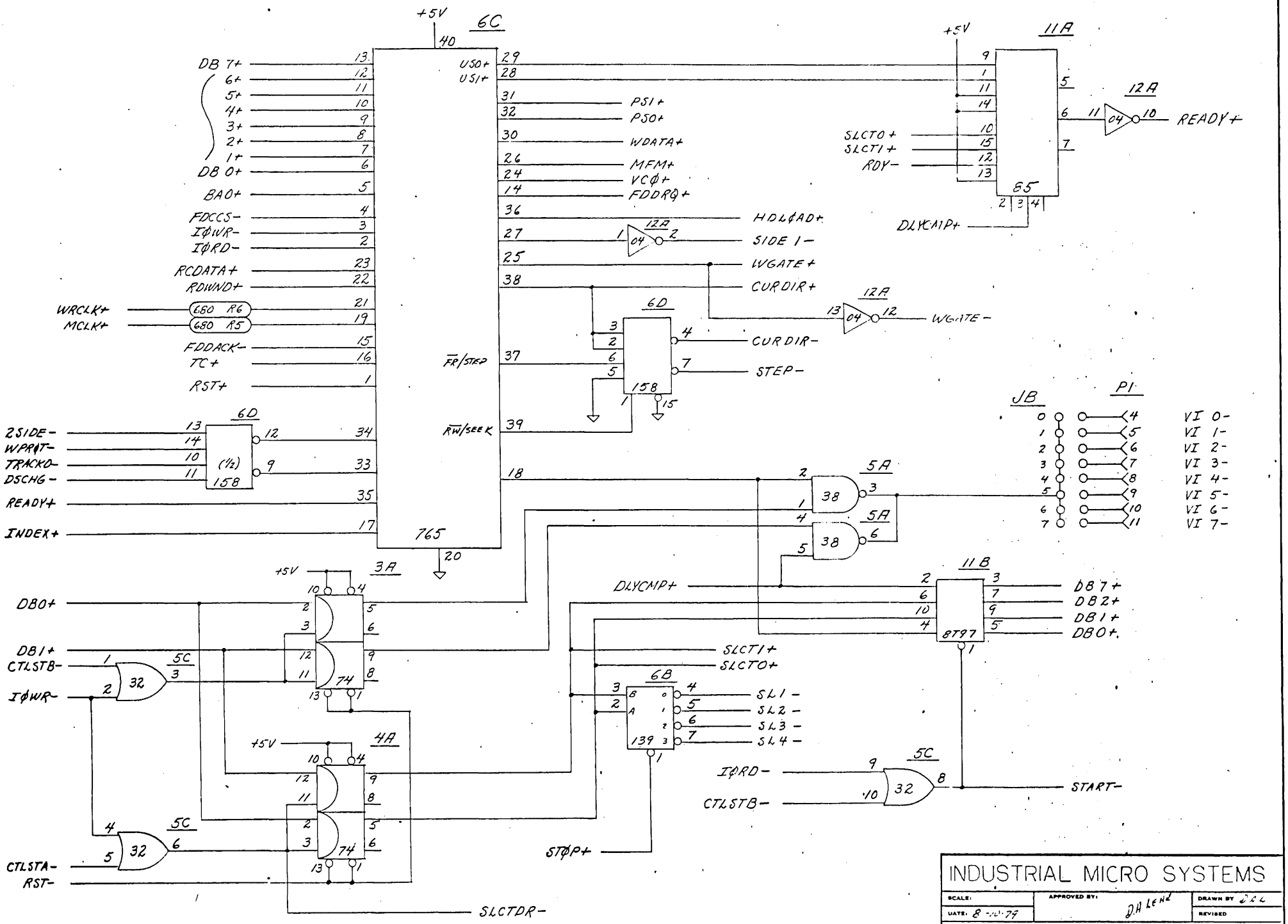
MOTOR CONTROL RELAY (MODEL 400 ONLY)

The connector at J3 in the upper left hand corner of the Model 400 board is to provide control to the solid-state relay used for the Motor Control Option.

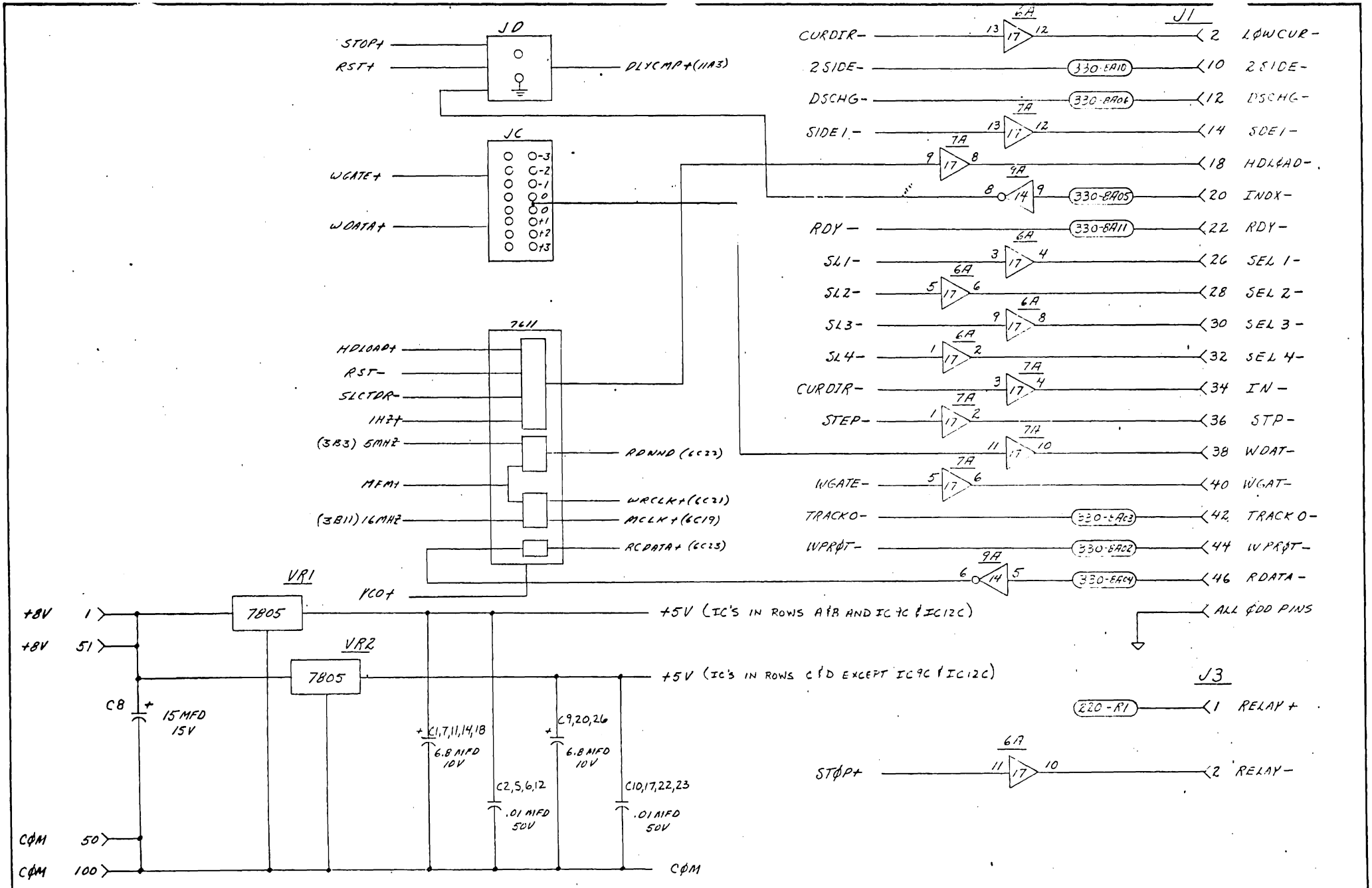


INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY: D.D LOHR	DRAWN BY D.A.L
DATE: 8-10-79		REVISED
S8000 FLOPPY CONTROL		
L00401		DRAWING NUMBER 1 OF 4


+5V
9C
31
DB 7+
6+
5+
4+
3+
2+
1+
DB 0+
21
22
23
26
27
28
29
30
BA 7+
6+
5+
4+
3+
2+
1+
BA 0+
40
39
38
37
35
34
33
32
MEMWR-
MEMRD-
AEN+
HRQ+
DACK1-
ADSTB+
4
3
9
10
24
8
12A
11D
8B
5A
2B
10A
9A
10B
P1
18 STAT DSBL-
19 CCDSBL-
22 ADDDSBL-
23 DØDSBL-
77 PIVR-
44 MII+
45 SØUT+
46 SNIP+
96 SINTA+
47 SNIEMR+
78 DBIN+
PIVR-
SØUT+
SNIP+
DBIN+
AEN-
AEN+
74 IHØLD-
HRQ+
FDMIRD+
FDDACK-
ADSTB+
J2
16 CØM
13 DACK 0-
11 DACK 2-
14 DACK 3-
15 CØM
1 DRQ 0-
3 DRQ 2-
4 DRQ 3-
12 CØM
5 BTC-
10 CØM
7 BIØWR-
8 CØM
9 BIØRD-
6 CØM
2 CØM
RST-
RST+
RST+
FDDRQ+
HRQ+
HLDA+
DMACS-
PRDY+
XRDY+
CLK-
DBIN+
PWR-
AEN+
BDBIN-
I/OWR-
TC+
R7
220
C13
220 pfd
4.7K R3
4.7K R4
330 8A01
330 8A13
330 8A12
DRQ1+
HLDA+
8257
20
N/C
I/ORD-
8T97
INDUSTRIAL MICRO SYSTEMS
SCALE:
APPROVED BY:
DRAWN BY
DATE: 8-10-79
REVISED
S8000 FLOPPY CONTROL
L00401
DRAWING NUMBER
2 OF 4



INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY: D.H LEHR	DRAWN BY JLL
DATE: 8-21-79		REVISED
S8000 FLOPPY CONTROL		
L00401		DRAWING NUMBER 3 OF 4



INDUSTRIAL MICRO SYSTEMS			
SCALE:	APPROVED BY:	DRAWN BY:	
DATE: 8-20-79		REVISED	
8800 FLOPPY CONTROL			
L00401		DRAWING NUMBER	4 OF 4

INDUSTRIAL MICRO SYSTEMS INC.

MODEL 501

16K STATIC RAM MEMORY BOARD

****

The 501 board is fully static and fully buffered and uses 2114 type memory I.C.'s. The boards are supplied fully tested and burned-in at 70 degrees C. under diagnostic test to insure reliable operations.

FEATURES

1. Memory Management - On board Memory Management system.

2. ROM Compatibility - Logic provided to de-activate a portion of memory if ROM is used. A "Phantom Line" is also provided for systems using this feature.

3. Front Panel Independent - Logic provided for compatibility with or without front panels. No front panel modifications are required.

OPTION SELECTION

All option jacks are clearly labeled. With the connector edge of the board toward the viewer, the jacks are located on the right edge and bottom edge of the board. Options are selected by placing shunts (provided) on the jacks. Spare shunts may be left on the board for future use in the event that changes are made in the selected options.

MEMORY ADDRESS SELECTION

The 501 memory is addressed as two independent 8K memories and two shunts must be placed on the (8K MEM ADD) jacks to define the starting address of each 8K section. One shunt must be placed from the center row to the top row and the other from the center row to the bottom row. There are eight positions for each shunt corresponding to the eight 8K memory blocks in a 64K system.

SHUNT POSITION	8K MEMORY BLOCK	SHUNT POSITION	8K MEMORY BLOCK
0	0000 - 1FFF	4	8000 - 9FFF
1	2000 - 3FFF	5	A000 - BFFF
2	4000 - 5FFF	6	C000 - DFFF
3	6000 - 7FFF	7	E000 - FFFF

FRONT PANEL OPTION

A single shunt must be placed on the front panel option jack (J2) located to the left of the memory address jack. Two positions are possible, the PWR position for use with systems not having front panels and the MWR position for systems with front panels. When in the PWR position, the memory write strobe is derived from the "Processor Write" signal (Pin 77 on the Bus). When in the MWR position, the "Memory Write" signal (Pin 68 on the Bus) is used to generate a write strobe.

Caution - On some systems not having front panels, the processor board generates a "Memory Write" signal and in this case, the MWR position should be used.

MEMORY MANAGEMENT OPTIONS

Memory Management provides a powerful tool to expand the working RAM memory to greater than 64K bytes. Theoretically, the memory may be expanded to 4096K bytes (i.e., 4,194,304 bytes, large enough?). Memory Management can be used on systems of less than 64K. Fundamentally, this system provides a means of having more than one memory with the same addressing.

Each memory board may be mapped "ON" or "OFF" via an output command to a user selected address. Bit 0 of the output word is used to enable or disable the board. A "one" bit enables the board, a "zero" disables the board. The user may interrogate the status of the board by doing an input from the same address. Again, bit 0 of the input word indicates the status; "one" indicates enabled, zero indicates disabled.

MEMORY MANAGEMENT I/O ADDRESSING

Four jacks are located along the bottom of the board. Starting from the left, they are labeled ADDR 7-6, ADDR 5-4, ADDR 3-2, and ADDR 1-0. Each of these jacks is labeled 0, 1, 2, 3, with the "3" position at the top and the "0" position at the bottom.
The I/O address is selected by placing the shunts horizonally on the jacks to make up the desired I/O address. For example, if we wanted to define I/O address 7E, this would correspond to the following:

ADDR 7-6 = 1
ADDR 5-4 = 3
ADDR 3-2 = 3
ADDR 1-0 = 2

I/O address 00 is configured by placing shunts on jacks 0000, and I/O address FF is configured by placing shunts on jacks 3333.

To disable this feature, that is, to configure the board so that no I/O address is decoded, simply remove any one shunt. When shipped the I/O address shunt on the ADDR 1-0 jack is stored on the SP of jack J5 disabling the Memory Management I/O address.

MEMORY MANAGEMENT INITIALIZE OPTION

When power is first applied or after "RESET", more than one board located at the same address could be mistakenly enabled. To control this situation, the leftmost two positions of the J1 jack are used to determine whether the board is initially selected "ON" or "OFF".

Placing the shunt on the leftmost position, labeled "OFF", causes the board to be initialized off. Conversely, placing the shunt on the "ON" position causes the board to be initialized on.

As shipped, the board is selected ON and must be ON unless Memory Management is used.

ROM COMPATIBILITY OPTIONS

On systems using ROM's, the RAM memory with corresponding addressing must be deselected when operating in ROM. Two systems are currently popular -

A. "Bootstrap" ROM's used to initially load the memory and not used thereafter.

B. "Dedicated" ROM's which permanently use some portion of the addressable 64K.

Some "Bootstrap" ROM's have been implemented using a "Phantom Line" (Pin 67 on the S-100 Bus). When the ROM is active, the "Phantom Line" is held low by the ROM and provides a signal which is used to deselect RAM memory.

"Dedicated" ROM's could, but often do not provide a Phantom Line Signal. In this case, that portion of the RAM memory corresponding to the ROM memory must be permanently disabled. The 501 board is compatible with either "Bootstrap" or "Dedicated" ROMs.

PHANTOM LINE OPTION

Located on the right edge of the board, directly below the MEM ADD jack, is jack J1. Placing a shunt on the "PH" position, (second from the right), enables the Phantom Line Option. The rightmost position labeled "SP" for spare is provided for storing the shunt if the Phantom Line Option is not used.

DEDICATED ROM OPTION

Jacks J4 and J5 are used to disable the portion of the memory board which conflicts with DEDICATED ROMS. The user may disable from 1 to 15K bytes of memory in 1K increments starting from either end of the memory addressing or you may disable a 1K block of memory anywhere within the memory.

Jack J5 has four positions, labeled 0, 1, 2, and SP. The first three are used to select whether disabling is to be done from the top (high addresses), the center (1K block), or the bottom (low addresses), respectively. The SP position is a spare position for shunt storage.

Jack J4 has four positions, labeled, 8, 4, 2, 1. Their positions are used to select either the amount of memory to be disabled or the location of a 1K block within the memory to be disabled depending upon the jack J5 shunt position.
As shipped, the board is configured to use all of memory with nothing disabled. The following table shows how to position the shunts to disable any portion of memory.

J4					J5		
8 -	4 -	2 -	1	(HEX)	SHUNT ON "0"	SHUNT ON "1"	SHUNT ON "2"
X	X	X	X	F	0444-3FFF	0000-3FFF	NONE
X	X	X	0	E	0800-3FFF	0400-07FF	0000-03FF
X	X	0	X	D	0C00-3FFF	0800-0BFF	0000-07FF
X	X	0	0	C	1000-3FFF	0C00-0FFF	0000-0BFF
X	0	X	X	B	1400-3FFF	1000-13FF	0000-0FFF
X	0	X	0	A	1800-3FFF	1400-17FF	0000-13FF
X	0	0	X	9	1C00-3FFF	1800-1BFF	0000-17FF
X	0	0	0	8	2000-3FFF	1C00-1FFF	0000-1BFF
0	X	X	X	7	2400-3FFF	2000-23FF	0000-1FFF
0	X	X	0	6	2800-3FFF	2400-27FF	0000-23FF
0	X	0	X	5	2C00-3FFF	2800-2BFF	0000-27FF
0	X	0	0	4	3000-3FFF	2C00-2FFF	0000-2BFF
0	0	X	X	3	3400-3FFF	3000-33FF	0000-2FFF
0	0	X	0	2	3800-3FFF	3400-37FF	0000-33FF
0	0	0	X	1	3C00-3FFF	3800-3BFF	0000-37FF
0	0	0	0	0	NONE	3C00-3FFF	0000-3BFF

X = SHUNT ON 0 = SHUNT OFF

Addresses shown are for the first 16k portion of RAM. For the second 16K portion, add hex '4000' to addresses, for the third 16K portion add hex '8000', and for the fourth 16K portion add hex 'C000' to addresses.

POWER ON CLEAR OPTION

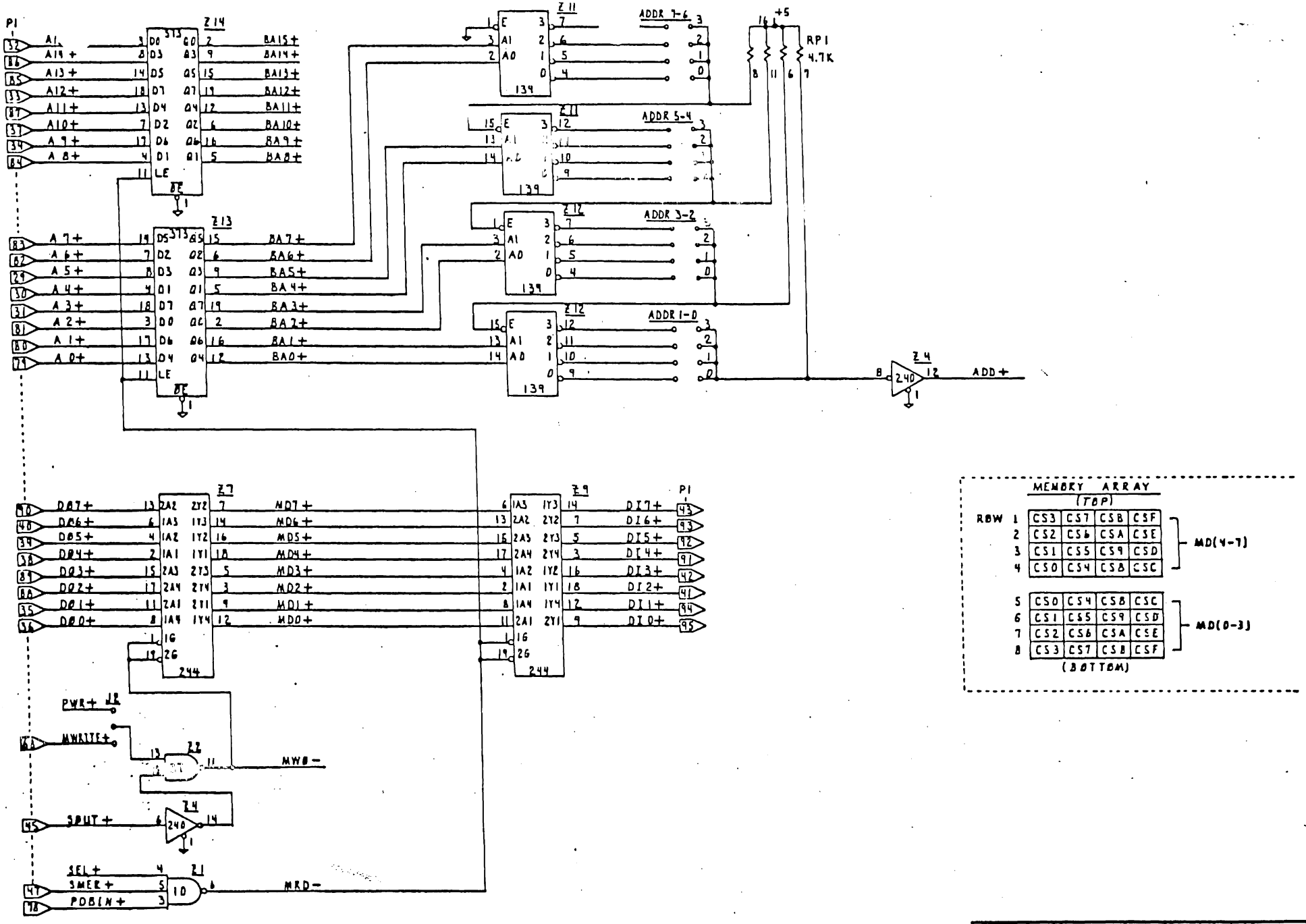
If it is desired to disable the "Power On Clear" signal and initalize only with the "Reset" signal, the vertical trace between the leftmost two pads of J3 should be cut. J3 is located to the left of J5.

Normally, no changes are needed or desired on J3.

SUMMARY

Now that you have read this description, we recommend strongly that all of your users read it completely before using the board and retain it for future reference. We hope that the added features of this board will provide the user with the flexibility and power he wants without undue complexity.

The 501 board has been carefully designed and uses the best of components, including a U.L. listed Printed Circuit Board and glass encapsulated de-coupling capacitors. The board is built and tested to Industrial standards and can be expected to provide long trouble free service.

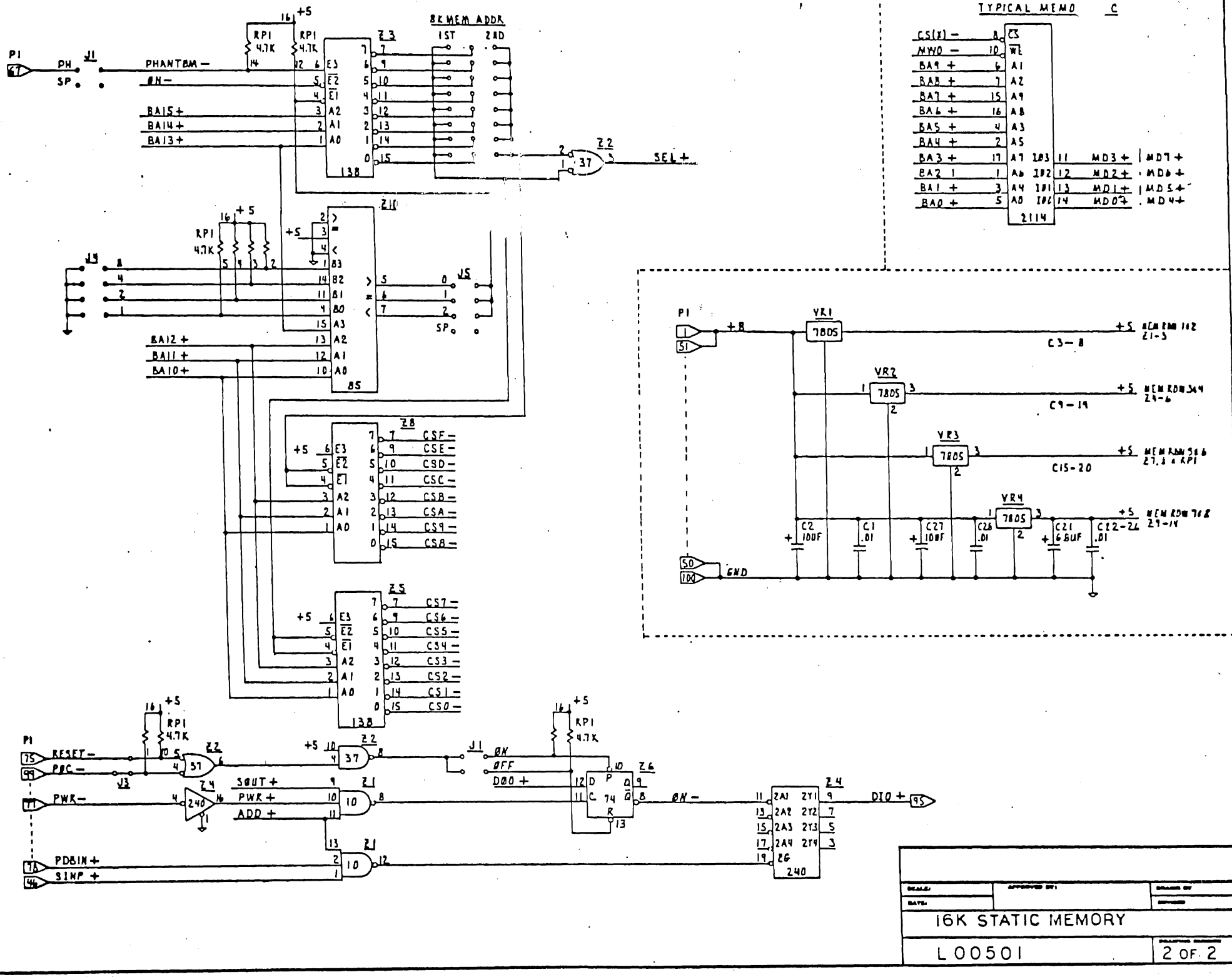


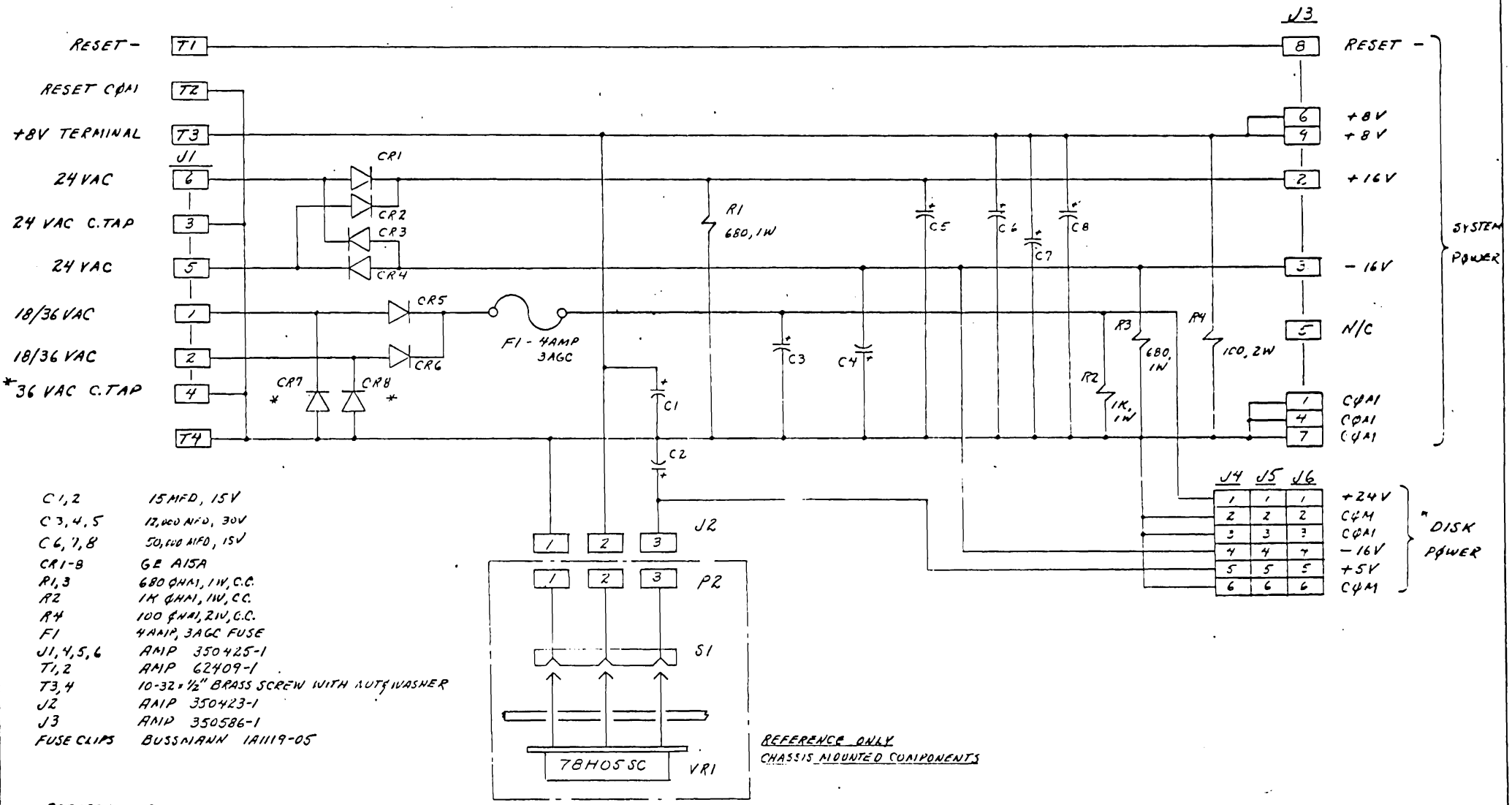
				DRAWN BY GDE
	DATE 12-10-79			

16K STATIC MEMORY

L00501

1 OF 2


TYPICAL MEMO C
8K MEM ADDR
1ST
2ND
PHANTOM –
ON –
BA15 +
BA14 +
BA13 +
BA12 +
BA11 +
BA10 +
SEL +
RPI 4.7K
+5
P1
J1
PH
SP
Z3
Z2
Z10
Z8
Z5
Z4
Z1
Z6
138
85
37
240
74
10
CS(X) –
MWO –
BA9 +
BA8 +
BA7 +
BA6 +
BA5 +
BA4 +
BA3 +
BA2 +
BA1 +
BA0 +
2114
MD3 +
MD2 +
MD1 +
MD0 +
MD7 +
MD6 +
MD5 +
MD4 +
VR1
VR2
VR3
VR4
7805
+8
GND
C3 – 8
C9 – 19
C15 – 20
C2 100UF
C1 .01
C27 100UF
C26 .01
C21 6.8UF
C22 – 24 .01
RESET –
PBC –
PWR –
PWR +
SOUT +
ADD +
PDBIN +
SINP +
ON
OFF
DOO +
DIO +
ON –
V3
16K STATIC MEMORY
L 00501
2 OF 2



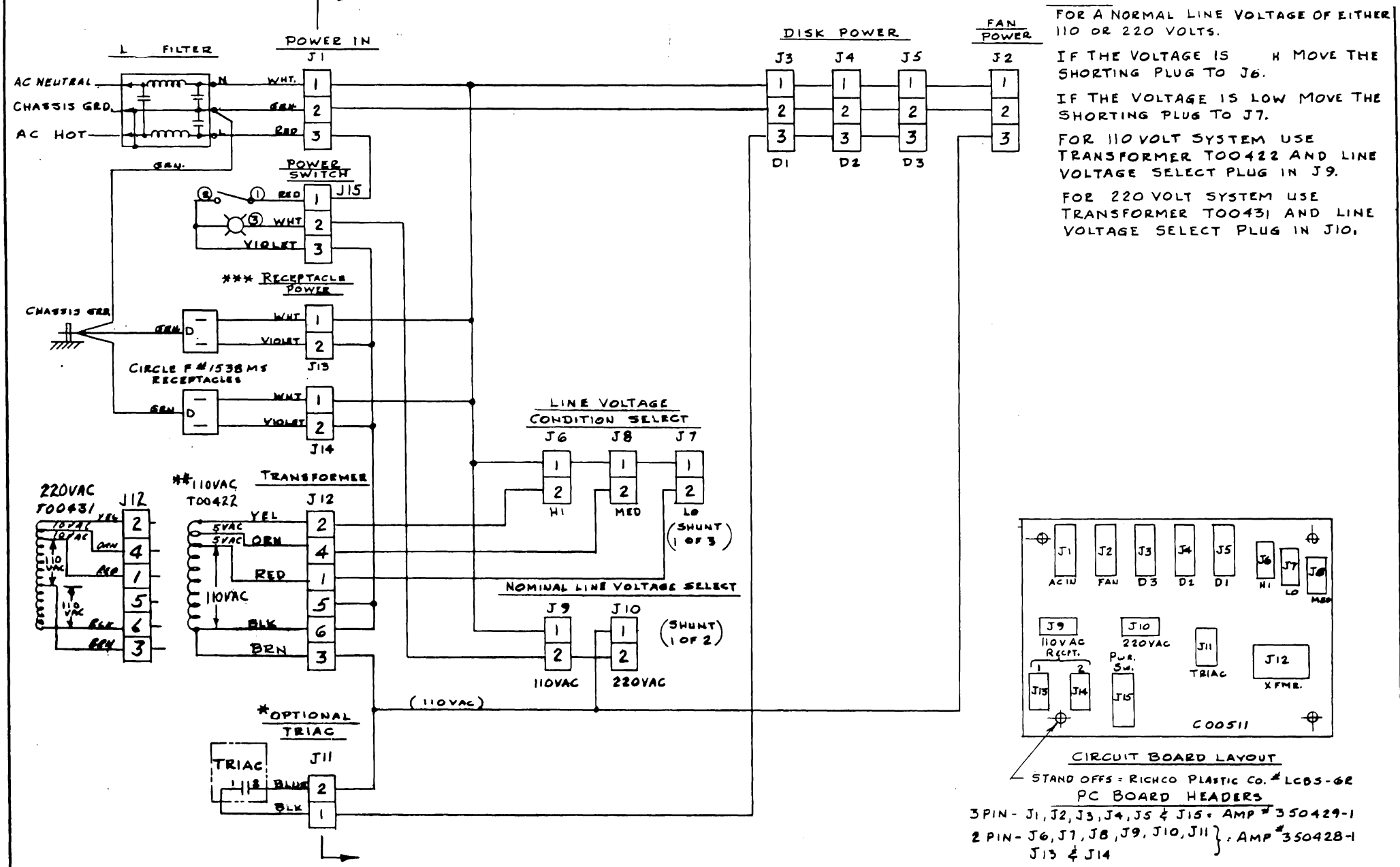
C1,2	15 MFD, 15V
C3,4,5	12,000 MFD, 30V
C6,7,8	50,000 MFD, 15V
CR1-8	GE A15A
R1,3	680 ØHM, 1W, C.C.
R2	1K ØHM, 1W, C.C.
R4	100 ØHM, 2W, C.C.
F1	4 AMP, 3AGC FUSE
J1,4,5,6	AMP 350425-1
T1,2	AMP 62409-1
T3,4	10-32 x ½" BRASS SCREW WITH NUT & WASHER
J2	AMP 350423-1
J3	AMP 350586-1
FUSE CLIPS	BUSSMANN 1A1119-05

REFERENCE ONLY

P2	AMP 1-480303-0
P2 CONTACT	AMP 60619-1 OR 61117-1 IN STRIP FORM
S1	ROBINSON NUGENT MP-3452-T
VR1	78H05SC (FSC)

* NOTE:
CR7 & CR8 NOT USED WITH CENTER TAPPED WINDING.

INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY: D.A. Lowe 4-13-79	DRAWN BY D.A. Lowe
DATE: 3-30-79		REVISED
SYSTEM 8000 POWER SUPPLY		
L00420		1 OF 1



FOR A NORMAL LINE VOLTAGE OF EITHER 110 OR 220 VOLTS.

IF THE VOLTAGE IS H MOVE THE SHORTING PLUG TO J6.

IF THE VOLTAGE IS LOW MOVE THE SHORTING PLUG TO J7.

FOR 110 VOLT SYSTEM USE TRANSFORMER T00422 AND LINE VOLTAGE SELECT PLUG IN J9.

FOR 220 VOLT SYSTEM USE TRANSFORMER T00431 AND LINE VOLTAGE SELECT PLUG IN J10.

CIRCUIT BOARD LAYOUT

STAND OFFS = RICHCO PLASTIC CO. # LCBS-6R

PC BOARD HEADERS

3 PIN - J1, J2, J3, J4, J5 & J15 = AMP # 350429-1

2 PIN - J6, J7, J8, J9, J10, J11, J13 & J14 } = AMP # 350428-1

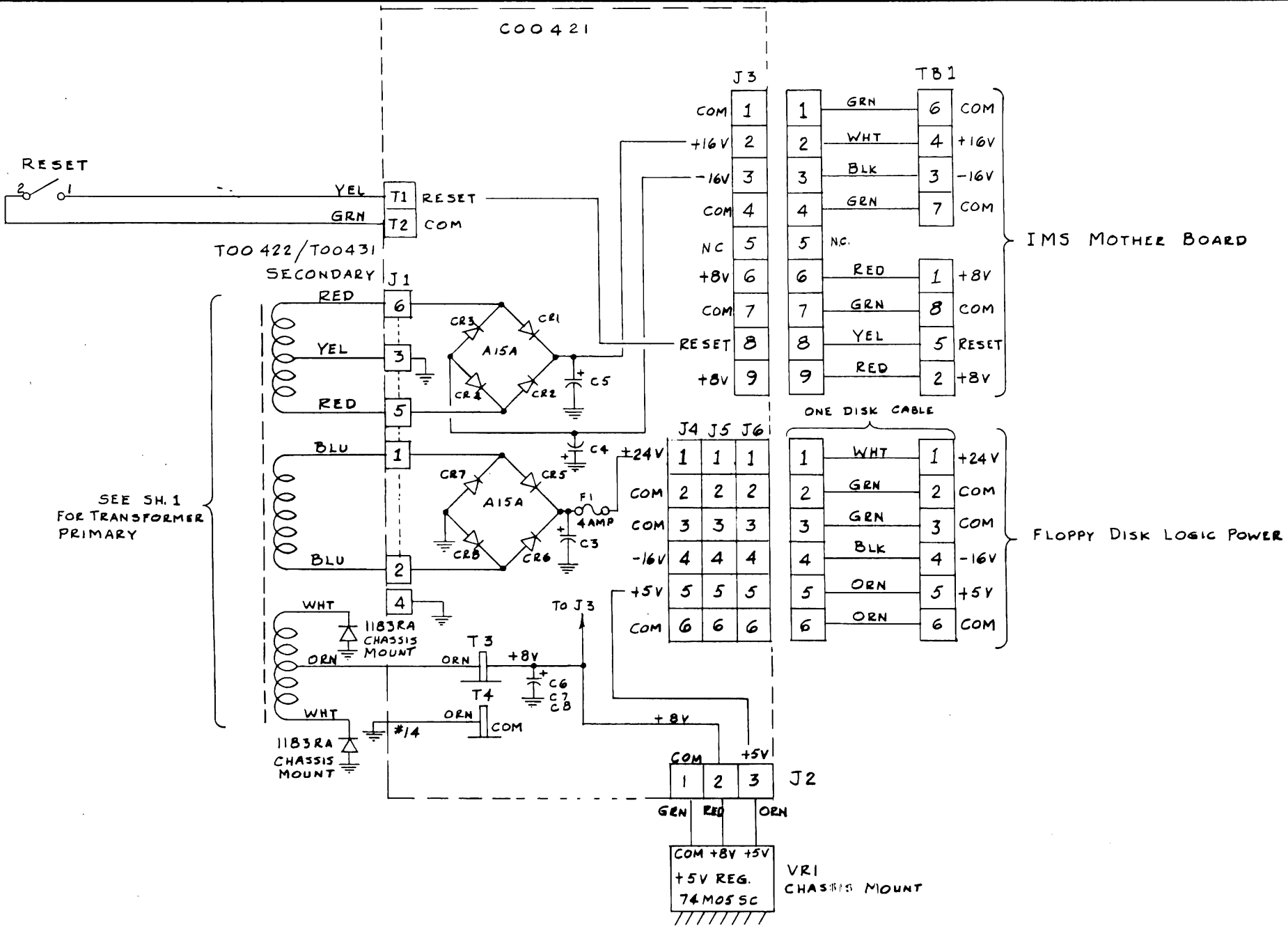
6 PIN - J12 = AMP # 350431-1

* J11 MUST BE SHUNTED IF TRIAC OPTION IS NOT USED.

** ON 110VOLT TRANSFORMER, BRN. & BLK. LEADS ARE INTERNALLY CONNECTED.

*** AC RECEPTACLES USED ON 110VAC ONLY.

INDUSTRIAL MICRO SYSTEMS		
SCALE: ~	APPROVED BY:	DRAWN BY R D W
DATE: 12-18-79		REVISED 8-7-80
AC PWR. DISTRIBUTION BOARD		SYSTEM 8000
W00511		SHEET OF 2



INDUSTRIAL MICRO SYSTEMS		
SCALE: ~	APPROVED BY:	DRAWN BY EDW
DATE: 8-7-80		REVISED
POWER SUPPLY CHASSIS		SYSTEM 8000
W00511		DRAWING NUMBER SH 2 OF 2

APPENDIX M

ASCII Character Codes

ASCII Code	Character	ASCII Code	Character	ASCII Code	Character
000	NUL	043	+	086	V
001	SOH	044	,	087	W
002	STX	045	-	088	X
003	ETX	046	.	089	Y
004	EOT	047	/	090	Z
005	ENQ	048	0	091	[
006	ACK	049	1	092	\
007	BEL	050	2	093	]
008	BS	051	3	094	^
009	HT	052	4	095	_
010	LF	053	5	096	`
011	VT	054	6	097	a
012	FF	055	7	098	b
013	CR	056	8	099	c
014	SO	057	9	100	d
015	SI	058	:	101	e
016	DLE	059	;	102	f
017	DC1	060	<	103	g
018	DC2	061	=	104	h
019	DC3	062	>	105	i
020	DC4	063	?	106	j
021	NAK	064	@	107	k
022	SYN	065	A	108	l
023	ETB	066	B	109	m
024	CAN	067	C	110	n
025	EM	068	D	111	o
026	SUB	069	E	112	p
027	ESCAPE	070	F	113	q
028	FS	071	G	114	r
029	GS	072	H	115	s
030	RS	073	I	116	t
031	US	074	J	117	u
032	SPACE	075	K	118	v
033	!	076	L	119	w
034	"	077	M	120	x
035	#	078	N	121	y
036	$	079	O	122	z
037	%	080	P	123	{
038	&	081	Q	124	|
039	'	082	R	125	}
040	(	083	S	126	~
041	)	084	T	127	DEL
042	*	085	U		

ASCII codes are in decimal
LF=Line Feed, FF=Form Feed, CR=Carriage Return, DEL=Rubout