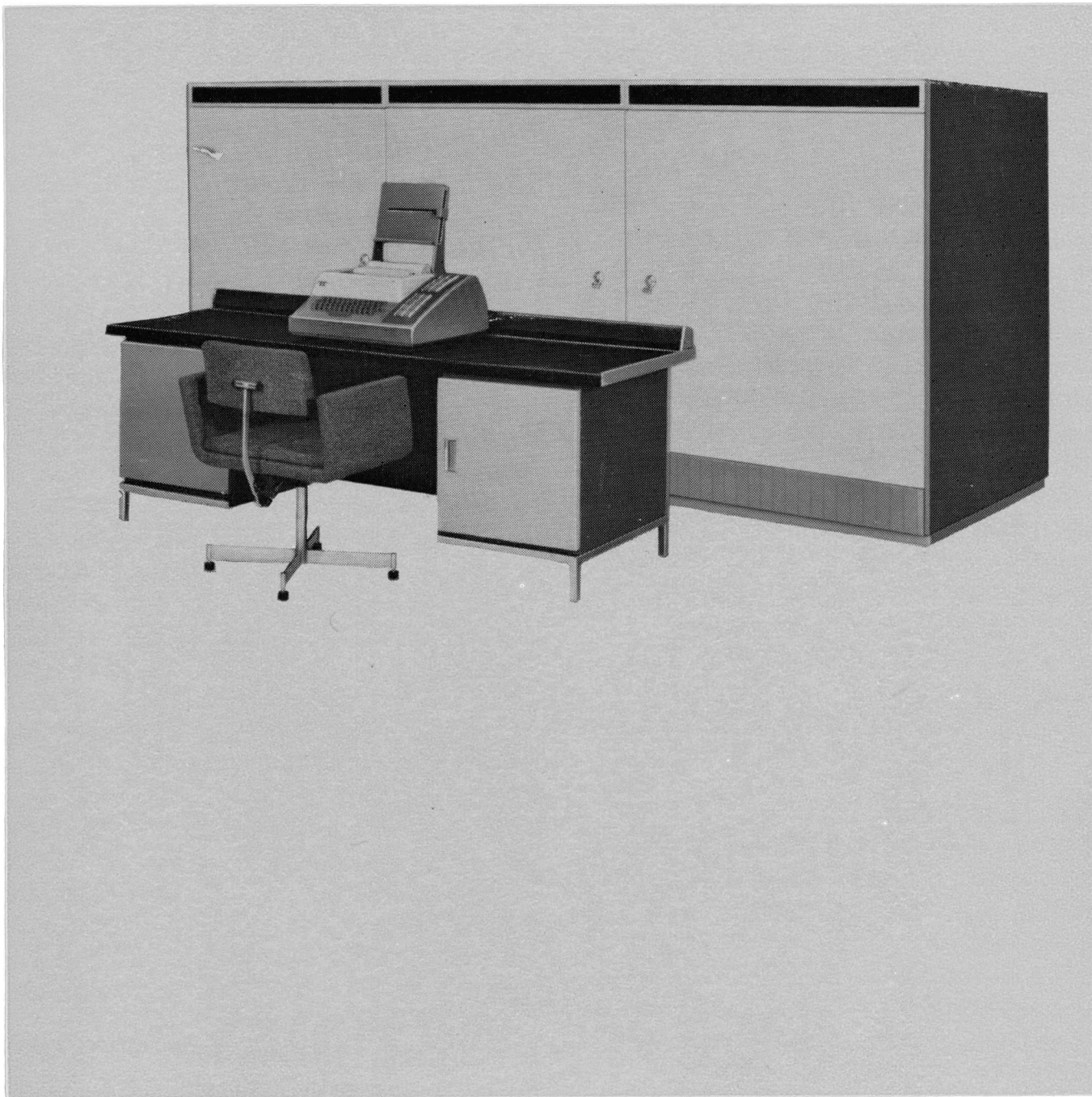# I.C.T 1900 SERIES

CENTRAL PROCESSORS
1906
1907

DESCRIPTION

The I.C.T 1906 is the largest in the 1900 series of compatible Central Processors providing throughput up to three times that of the I.C.T 1904 and high speed storage capacity up to 262,144 words of 24 bits. It is a multi-purpose digital processor to which a wide range of input, output, storage and communications devices can be attached.

The system is designed to allow easy growth from the smaller systems in the range. Thus, all programs written for smaller I.C.T 1900 systems will work unchanged and with increased efficiency on I.C.T 1906. Similarly a 1904 Central Processor can be replaced on site by 1906 without peripheral redundancy. Most peripheral units are attached via I.C.T Standard Interface and are therefore interchangeable with all systems in the range.

Alternatively a 1907 processor can be specified to provide autonomous floating point facilities. Very high calculating speeds are thus available, the performance of a 1907 processor being three times that of the 1905.

■ Multi-programming under automatic control of Executive

■ Processor time automatically allocated for maximum productivity

■ Simultaneous operation of peripheral devices

■ Up to four million characters per second transfer rate

■ Programming compatibility throughout the 1900 series

■ Reservation system prevents inter-program interference

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Multi-programming
The processor incorporates facilities for multi-programming whereby a number of programs may be run concurrently. Up to sixteen programs may be run at once with no risk of mutual interference. This multi-programming system is entirely automatic, and the programmer does not have to consider it when writing his programs. If he so desires, the programmer may incorporate into a main program up to three sub-programs which will then participate independently in the automatic multi-programming system, concurrently with the other main programs in the system.

Executive
Executive is the name given to a program which when the computer is in normal use, is always present in the core store, and which controls all other programs that are in the system at any time. The main functions performed by Executive are:
1. Interpretation and execution of the Operator's commands to the system, and provision of information for the operator concerning normal program running incidents, and peripheral devices that need attention.
2. Allocation of the time of the central processor among the programs in the system according to given priorities so as to achieve maximum utilization of the central processor and of the peripheral devices.
3. Allocation of peripheral devices to programs that are entered into the system, and the control of data transfer to and from peripheral devices.
4. Monitoring of program and peripheral device performance.

Operation
Systems utilizing 1906 and 1907 processors are controlled by means of messages entered by the operator on a typewriter directly connected to the processor. In addition, pre-punched messages may be entered via a card reader or paper-tape reader. Executive takes the actions requested, and when necessary will type out messages for the information or action of the operator. This provides a printed record of the sequence of operational events. Facilities are also available for automatically sequencing jobs.

High Speed Store
A 1906/7 Processor may be supplied with a core store of from 32,768 to 262,144 words in modules of 32,768 words. The store in an initial installation may later be expanded on site up to the maximum when required. Two core store speeds are available. The cycle time of the first varies from 1.1 micro-seconds for a 32,768 word system to an average of 1.25 micro-seconds for a 262,144 word system. The second varies similarly from 2.1 to 2.25 micro-seconds. All store operations are subjected to a parity check. Two words are accessed in parallel thus improving the performance of double-word operations.

Store Reservation
Each program is allotted an appropriate area within the core store. While executing program instructions the central processor is allowed to use only those parts of the store which are reserved for that program. Whenever the Executive causes the central processor to start obeying a different program the reservation settings are changed to those appropriate for that program. Thus each program, including those under test, is prevented from interfering with any others that may be running in the machine.

Peripheral Transfer
All transfers of data to or from peripheral devices are carried out by program entries to Executive, which has direct control of all devices. Before initiating the transfer, Executive checks that the store locations requested are within the area reserved for the program that issued the request. Once initiated the transfers proceed autonomously so that any number of transfers may be in progress simultaneously.
The central processor is caused to 'hesitate' when necessary to allow a single character or word to be transferred between the core store and the peripheral units. The central processor time required for hesitations depends on the speed of the main store and the type of peripheral (fast or slow).
The following figures relate to storage with an average cycle time of 1.25 micro-seconds. The figures in brackets relate to 2.25 micro-seconds storage. For slow peripherals such as buffered printers and card and paper tape equipment, the hesitation time averages 3.125 (5.125) micro-seconds per character while for fast peripherals such as magnetic tape and other types of backing storage the hesitation time varies between 1.25 (2.25) and 3.75 (6.75) micro-seconds per word with an average of 2 (3) micro-seconds per word, or less if more than one Store Access Control is fitted. A Store Access Control provides access to memory for up to eight high speed peripheral channels. Several Store Access Controls can be provided if required.
Internal processing therefore proceeds at a slightly reduced rate while peripheral transfers are in progress. Completion of a transfer causes a signal to the Executive and any program held waiting for that transfer is allowed to proceed.
Transfers which fail accuracy checks are automatically repeated a pre-determined number of times before operator intervention is requested, if the peripheral devices permit automatic re-positioning of the medium e.g. magnetic tape decks or card punches. On other devices a failure is notified to the operator immediately.

Word Length
The processor normally operates with words of 24 binary digits. Such a word can be used to represent:-

one instruction

four alpha-numeric characters

a decimal integer in the range —8,388,608 to +8,388,607

a decimal fraction in the range —1.0 to +0.9999999 with accuracy approximately equivalent to seven decimal digits

Two words together may represent a double-precision number having an

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accuracy equivalent to over thirteen decimal digits, or a floating-point number.

A number of separate data items may be packed into a word or group of words, and instructions are available to address single characters in the store.

Registers
Eight high speed registers are available for use as the program's accumulators and can be used for arithmetic and counting. Three of these accumulators may be further used for indexing. These registers are used by the current program and, when the computer switches via Executive to a new program, are unloaded into the first eight core store locations assigned to that program. The contents of the first eight core store locations of the program with the highest priority which is able to proceed are then loaded into the high speed registers.

The loss of time involved in loading and unloading these registers between program switches is negligible compared to the increased speed resulting from the availability of high speed registers, since most instructions carry a reference to a core store location and an accumulator.

The 1906 processor implements its floating-point instructions in the main arithmetic unit at a speed approximately five times that of a 1904. A 1907 processor provides even higher performance, as floating point operations are performed in a separate arithmetic unit.

Instruction Code
The comprehensive instruction repertoire contains arithmetic, transfer, logical and shifting operations, including multiplication, division, and literal operand facilities. There are special provisions for multiple-length arithmetic, conversions between decimal and binary forms of numbers, floating-point and character handling.

Input/Out Channels
Peripheral devices are connected to the central processor by means of Input/Output Channels which are located in the processor cabinet. A wide range of peripheral devices to Standard Interface can be attached to the same type of Channel. A Channel can handle a Control or Multiplexor device which can itself handle a number of devices.

The processor contains eighteen channels for slow devices, e.g. punched card or punched paper tape. Channels for individual or grouped fast devices e.g. magnetic tape or discs may be incorporated as required.

SPECIFICATION SUMMARY

Data unit 24-bit word

Store size 32,768 to 262,144 words in modules of 32,768 words

Store cycle time 32,768 words 1.1 or 2.1 micro-seconds to 262,144 words 1.25 or 2.25 micro-seconds

Multi-processing Sixteen programs each with three sub-programs may operate concurrently

Accumulators Eight high speed registers for the current program

Index registers Three of the eight high speed registers

Arithmetic Binary (instructions include decimal conversion)

*Addition times** Add to Accumulator—2.5 or 4.5 micro-seconds: add to Store 3.125 or 5.125 micro-seconds

Multiplication times 11.25 micro-seconds average (at one micro-second cycle time)

Input/output channels Slow: 18. Fast: as many as required

Input/output rate (six-bit characters) —total: up to four million characters per second

Peripheral simultaneity Full processor hesitation:—
Slow devices: minimum 2.825 or 4.825, maximum 3.425 or 5.425, average 3.125 or 5.125 micro-seconds per character
Fast devices: minimum 1.1 or 2.1, maximum 4.2 or 7.2, average 2.0 or 3.0 micro-seconds per word with single store access control

*Alternative times depend on selected core store cycle time.

Floating-point Arithmetic
Both 1906 and 1907 Processors can carry out floating-point arithmetic. In the case of the 1906 floating-point instructions are carried out in the main arithmetic unit.

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A 1907 Central Processor has all the facilities and characteristics of a 1906, plus a Floating-Point Arithmetic Unit which is autonomous. The Central Processor can continue obeying other instructions 2.5 microseconds after a floating-point instruction has been initiated. There is a lockout which causes the Central Processor to wait if another floating-point instruction is encountered while the Floating-Point Unit is still busy. The Unit includes a 47-bit floating-point accumulator, and an exponent overflow indicator. The number representation is:

    Argument   37 bits plus sign
    Exponent   8 bits plus sign

The arithmetic functions may be rounded or unrounded and standardized or unstandardized at the discretion of the user.

Typical times in micro-seconds for the floating-point instructions are:

	1.25 micro-second cycle time
Add/Subtract	2.75
Multiply	7.75
Divide	16.75
Load/store	2.5

This specification is subject to modification