P.V. JERMY

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TECHNICAL SPECIFICATION OF THE I.C.T. STANDARD INTERFACE FOR PERIPHERAL DEVICES

This specification has been prepared by the Specifications Project of Engineering Division, Stevenage. The document has been approved by the Managers of Computer Systems Division, and Peripherals Division, Stevenage, Planning Division, Putney; Planning Division, Bracknell; and Computer Equipment Group, West Gorton.

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I.C.T STANDARD INTERFACE SPECIFICATION

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Sheet 1

Control Sheet

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PART I

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1.0 INTRODUCTION

1.1 SCOPE

This document defines the Standard Interface to be used by I.C.T. peripherals and processors.

However it is not possible for a peripheral designer to design his equipment to this specification alone. It is necessary that the designers of the processor to which connection is desired to be made be consulted so that data width and preferred mode of operation be catered for. Similarly processor designers should consult peripheral on individual peculiarities of the peripherals it is desired to be used in the complete system.

The range of peripherals which may be connected by this interface is as follows:

Type 1	Single channel, single mechanism
Type 2	Single channel, multi mechanism
Type 3	Multi channel, multi mechanism
Type 4	Data exchange
Type 5	Single channel, multi address

The suffix A or B following the type number denotes the timing characteristics of the peripheral.

A type will operate according to the timing rules currently described in this specification and will have the 'F' line at logic 0.

B type will operate according to faster timing rules to be defined later and will have the 'F' line at logic 1.

1.2 DEFINITIONS

The following definitions are given to define the application of the terms 'CHANNEL' and 'MECHANISM' in this specification.

1.2.1 Data Block

A block of data on the interface is a group of characters associated as follows:

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1.2.1 Cont/d.

(i) They are transferred as the result of one command.

(ii) One block identifier is necessary and sufficient for a central processor to transfer each character to or from the correct memory location.

(iii) One block is associated with one 'TERMINATED' signal which defines its end.

1.2.2 Simultaneous Operation

If two or more data blocks are transferred over the interface such that there can exist a time when both data block transfers have been INITIATED and neither has been TERMINATED, then the transfers are SIMULTANEOUS.

1.2.3 Channel

An interface which carries one data block transfer, i.e. an INITIATED data block which is TERMINATED before a subsequent data block can exist, is a SINGLE CHANNEL interface.

An interface which carries up to N simultaneous data block transfers is an N-channel interface. In particular if N is greater than one, it is a MULTI-CHANNEL interface. As a corollary it follows that on an N-channel interface at least N distinct identifiers are required which could be used to address N buffer areas in store.

1.2.4 Mechanism

A single device handling a medium on which data is recorded or is to be recorded, is a MECHANISM.

A channel which may be switched (in between data blocks) to different MECHANISMS is a MULTI-MECHANISM CHANNEL.

The case of such a switch in the middle of a data block is not allowed for under this heading, but must use more than one CHANNEL. An interface with more than one MULTI-MECHANISM CHANNEL is a MULTI-MECHANISM, MULTI-CHANNEL INTERFACE.

In addition, some further terms are used in this document, which are defined as follows:

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1.2.5 Peripheral

A device consisting of one or more mechanism associated with one control unit connected to a processor.

1.2.6 Irreversible

A condition which has changed due to the application of a control signal and remains in the new state after the control signal disappears.

1.2.7 Ducked

A condition which has changed due to the application of a control signal but will return to the original state after the control signal disappears.

1.2.8 Status

Status is usually a bit significant coding of the current state of a peripheral. However coding of more than one bit may occur in exceptional circumstances. Changes in the state may be signalled to the central processor where appropriate (See 3-9).

1.2.9 Unset

A condition which has ceased to exist due to the application of a control signal said to be "unset".

1.2.10 Reset

A condition which has been set again in another state is said to be "reset". This term is used for status which may in general exist in one of three states. See 7-1 and 7-3 for further remarks.

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2.0 LINES ACROSS THE INTERFACE

2.1 Types 1, 4 and 5 peripherals.

	Minimum mandatory subset	Permissible Extensions
Processor to peripheral		
Do	6 lines, 2^0 through 2^5	3 lines 2^6 2^7 + parity 2^8
A	1 line	NIL
T	1 line	NIL
C	1 line	NIL
No	NIL	1 line
L	NIL	1 line
G	1 line	NIL
Ho	1 line	NIL
Peripheral to processor		
Di	6 lines, 2^0 through 2^5	3 lines 2^6 2^7 + parity 2^8
F	1 line	NIL
R	1 line	NIL
B	1 line	NIL
J	1 line	NIL
Ni	NIL	1 line
Hi	1 line	NIL
Z	3 lines	NIL
Total - 25		9

Note: A Type peripherals will have F=0 (present timing rules)
B Type peripherals will have F=1 (fast timing rules)
rules

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2.2 Type 2 and 3 peripherals

Minimum mandatory subset		Permissible Extensions
25 lines listed in 2.1		6 lines (as listed in 2.1 except L and Ni, No)
No	1	NIL
Ni	1	NIL
L	1	NIL
Totals	- 28	6

Giving a grand total with extensions of 34

Note: A Type peripherals will have F=0 (present timing rules)
B Type peripherals will have F=1 (fast timing rules)

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3.0 FUNCTION OF LINES ACROSS THE INTERFACE

The function of each line will be described in general terms, followed by the mandatory or permissible aspects of the function.

3.1 Do - Data Out.

These lines can be used to transmit either a data character including odd parity, a control character, or a mechanism or channel identifier.

A convention is adopted whereby 2^0 signifies the lines which is equivalent to the least significant binary bit. The mandatory lines are 2^0 through 2^5. The use of the parity line (2^8) is optional. Peripherals and processors which include the line must provide a means for ignoring parity errors across the interface. Parity, if used, must be odd parity. Types 2 and 3 peripherals must accept identifiers from Do.

An extension to 7 or 8 bit characters, using lines 2^6, 2^7 is permissible only for those peripherals whose natural character width exceeds 6 bits, e.g. 7 hole paper tape, 8 bit magnetic tape. Individual agreed specifications should be consulted regarding the number of lines to be used.

3.2 A - Peripheral Addressed.

This is one line which, when in the logic 1 state, indicates that the interface is active. It exercises over-riding control, such that if A is not present, peripherals must ignore a character on the Do lines ignore C, T, L, No lines and maintain all the Di lines at logic zero.

The use of A is mandatory, If A is present peripherals must continuously present the appropriate character onto the Di lines, and peripherals must be prepared to accept a character from Do when the strobe pulse arrives.

The processor may join the A line to a common bus. (see 10-5)

The conditions under which A is raised to effect a single character transfer are described under the timing rules section, and figure 2.

No extension of A is permissible.

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3.3 T - Strobe

This is one line used to control transfers in conjunction with line A. It is used to make irreversible changes in the control logic in the peripheral.

The use of T is mandatory.

Processors may join the T line to a common bus (see 10-5).

No extension of T is permissible.

3.4 C - Transfer Control

This is one line which, when in the logic 1 state indicates that the character on Do is a control character.

The use of C is mandatory. The processor may join the C line to a common bus. (see 10-5)

No extension of C is permissible.

3.5 No - Identification control out.

This is one line which, when in the logic 1 state indicates:

(i) When A C = 1 1, the character on Do is a control identifier (e.g. a mechanism or channel address).

(ii) When A C = 1 0, the peripheral should place on Di the data identifier of a data character for which an 'R' request has been sent.

No is optional for type 5 peripherals. It is mandatory for types 2 and 3 peripherals. It is not used for types 1 and 4.

No extension of No is permissible.

3.6 L - Limit

This is one line used to conclude a data block transfer in conjunction with A, T and C.

The L line is optional.

If C = 0, No = 0, coincident with L, the last character of a block of data is being transmitted.

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L - Limit (Cont/d.)

In any other situation L indicates that the last character has been transferred of the block identified by the identifier being transmitted or last transmitted to the peripheral. The peripherals will suppress the R line for the appropriate channel and will proceed as follows:

If the ERROR status is already set, it will remain set.

If not set, it will take either action (a) or (b) below, following the transmission of any character read from or written onto the medium after the receipt of L.

Either (a) if the detection of errors has no significance as to the validity of data already transferred will cease to record further errors.

or: (b) if further checks are performed which may effect the validity of the data transferred will continue to record further errors. The point at which termination occurs must be specified in the individual peripheral agreed specifications.

The next READ or WRITE control code to the relevant channel will unset the error status.

No extension of L is permissible.

3.7 Di - Data In

These lines can be used to transmit either a data character including odd parity, a status character or a mechanism or channel identifier. A convention is adopted whereby 2^0 signifies the line which is equivalent to the least significant binary bit. The mandatory lines are 2^0 through 2^5. The use of the parity line (2^8) is optional. Parity, if used, must be odd parity. Type 2 and 3 peripherals must give a data identifier on Di as appropriate.

An extension to 7 or 8 bit characters using lines 2^6, 2^7 is permissible only for those peripherals whose natural character width exceeds 6 bits, e.g. 7 hole paper tape, 8 bit magnetic tape. Peripherals and processors presently designed to use 6 bit characters will continue in this mode.

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3.8 R - Request data transfer

This is one line used in one of two ways.

The use of R is mandatory.

In the case of a read only device, or when a read/write device is in the reading states, the line is used to indicate that a character of data is available for transfer to the central processor. In the case of a write only peripheral device, or when a read/write device is in the writing state, the line is used to indicate that the device requires a data character to be transferred from the processor. The state of R has a special relationship to the speed at which data transfers may be made across the interface. This is dealt with in detail in the section concerning timing.

No extension is permissible.

3.9 B - Interrupt

This is one line used to indicate certain status changes. Such status changes will always be available to the central processor and the B line may not change for any cause other than a status change. Details of how status will affect the B line are given in Fig. 4. and Fig. 4A.

3.10 J - Direction of transfer

This is one line used by the peripheral in conjunction with the 'R' request indicating whether the request is for an input or output data character.

The use of J is mandatory, no extensions are permissible.

J = 0 = output character (WRITE)

J = 1 = input character (READ)

3.11 Ni - Identification control in

This is one line which, the logic 1 state indicates that there has been a change in the identifier associated with data transfers. Ni is optional for Type 5 peripherals. It is mandatory for types 2 and 3 peripherals. It is not used for Types 1 and 4. No extension of Ni is permissible

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3-12 F - Fast transfer

This is one line which, when in the logic 1 state, indicates that transfers from this peripheral are controlled by faster timing rules (These rules are defined in part II of this specification.)
The use of F is mandatory, no extension is permissible.

3-13 Hi - Power present at the peripheral, information on Di is valid.

Hi is one line from the peripheral to the processor which must obey the following rules:

1. When the two wires comprising the Hi line pair are short circuited by the peripheral this indicates that all power supplies at the peripheral are within their specified limits.

2. Further, when Hi is short circuited, valid signals appear on Di, Ni, J, R, B, F in response to processor commands.

Hi is mandatory, no extensions are permissible.

3.14 Ho - Power present at the processor, information on Do is valid
Ho is one line from the processor to the peripheral which must obey the following rules:

1. When the two wires comprising the Ho line pair are short circuited by the processor this indicates that all power supplies at the processor are within their specified limits.

2. Further when Ho is short circuited, valid signals appear on Do, No, A, T, C, L.

Ho is mandatory, no extensions are permissible.

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This is one line from the processor to the peripheral. The peripheral must be so designed that a logic level pulse of 100 uSec. duration is sufficient to cause a general reset.

3.15.1 If a general reset occurs when the peripheral is operable and an order is not being executed, the peripheral must enter the STOPPED 2 State, and B interrupts be inhibited.

3.15.2 If a general reset occurs when an order is being executed, R interrupts must be immediately inhibited. This may result in the rejection of any associated media (e.g. cards). The peripheral must eventually enter the STOPPED 2 state, and a B interrupt is then permissible.

3.16 Z - Ground

Z consists of 3 lines used for the 0 volt connection between the processor and the peripheral.

3.17 Identifiers.

These are characters appearing on Do or Di and indicate mechanism or channel addresses.

The specific assignment of identifiers to mechanism or channel addresses will be given in individual peripheral specifications.

Identifiers are divided into two classes, control identifiers and data identifiers.

Control identifiers are given on Do by the processor, and precede control commands, in order to identify the command with a particular channel or mechanism.

Data identifiers are <u>always</u> given on Di by the peripheral in response to A C T No = 1 0 X 1 from the processor to indicate the channel address of a data character to be transferred.

The Ni line is used by the peripheral to indicate that a <u>change</u> has occurred in the data identifier. Ni arises in conjunction with the

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3.17 Cont'd..

data service request R and the data direction indicator J, and is unset either when:

(i) A C T No Ni = 1 0 1 1 1 or:

(ii) After the processor gives T for transfer of the first data character associated with the new identifier and before the next R interrupt occurs.

Ni will not arise with R and J, if the data character to be transferred is associated with the same data identifier as the previous character.

Processors will normally ask for data identifiers in response to R interrupts. If a data identifier request is made at other times, using T, this may cause Ni to unset prematurely and, therefore, invalidate the state of this line.

For further information on the use on identifiers, the Code of Practice document to the Standard interface may be consulted.

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4.0 CONTROL CONDITIONS AT THE INTERFACE.

4.1 Steady state conditions

This section describes the 'steady state' control conditions i.e. it is written as if there were zero delay between the cause and effect conditions on the interface. Timing considerations are dealt with in the next section.

The actual control conditions are listed in Fig. 2. It can be seen that the central processor has control of the data lines in both directions, since the Di lines may only be used subject to the conditions on the lines A, T, C and No.

The following definitions are assumed:

(i) Logic 1 is that signal on a line which can be unambiguously recognised as a logic 1 by any allowed receiver working within its specified tolerance. Actual values are given in section 8.

(ii) Logic 0 is similarly specified.

The highway is, in general, controlled by the state of the A and T lines as follows:

(i) A is used to address the peripheral, so that if A = 0 the peripheral should ignore the information on lines T, C, L, Do and No, (but not G or Ho). It should also maintain zeroes on Di.

(ii) The condition A T = 1 0 is used to allow the peripheral to put non-zero information on Di in response to the information on C, No and Do. However, under this condition the peripheral may <u>not</u> make irreversible changes within itself as a result of the information on C, Do and No.

For example:

The peripheral may send status, but not reset it.
It may send a data character, but not change it.
It may send a data identifier.
It may not accept a data character.
It may not accept a command control character, or a control identifier, although it should signify its ability to do so.

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4.1 Cont/d.

(iii) The condition A T = 1 1 is used to allow the peripheral to make irreversible changes as a result of the information on C, L, Do and No. It may also use the Di highway.

For example:

It may accept a command control character.

It may accept a control identifier.

It may assume that the data character or data identifier it has been sending has now been accepted by the central processor and can therefore be 'thrown away'.

It may accept a data character.

It may reset status.

4.2 Reading Data.

Assuming that the peripheral has a data character available for transfer to the central processor, and the peripheral is being serviced in time (i.e. the data is not lost because the data medium has moved to a new character) the data character should not alter during the period when A T C = 1 0 0. The control condition A T C = 1 1 0 signifies to the peripheral that the data character has been transferred to the central processor and that the data character may be changed at any times from the beginning of the condition A T C = 1 1 0.

4.3 Writing data.

Assuming that the processor has a data character available for transfer to the peripheral. The central processor should not allow this to alter during the time when A T C = 1 1 0.

4.4. Status.

The status character responses under the conditions A T C = 1 0 1 and A T C = 1 1 1 are dealt with separately under 'STATUS' (Refer to section 7 and Fig.4.)

4.5 Command control codes.

This is similar to the writing data case, except that C = 1

12 4.6 Control Identifiers - processor to peripheral.

This is similar to the writing data case, except that C = 1, No = 1.

4.7 Data Identifiers - peripheral to processor.

This is similar to the reading case except that C = 0, No = 1.

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5.0 TIMING RULES

5.1 General

The timing rules for the interface are defined only for the position of the interface at X in Figure 1. i.e. at the physical boundary of the peripheral. For this purpose any connecting cables and the propogation delays arising therefrom are regarded as part of the central processor.

5.1.1 Peripheral turn around time.

When the peripheral changes the information on Di as a result of a change in the state of the lines A, T, C, L, Do, No then the delay between the change becoming steady and the correct response on Di becoming steady will be between the limits

MINIMUM DELAY 0 nSec.
MAXIMUM DELAY 750 nSec. (F = 0)

In the case of reading data transfers a character will be steady on Di within the limits above and further, when R is not ducked (see 5.2.2.1), subsequent characters will be steady on Di within the limits.

MINIMUM DELAY 0 nSec
MAXIMUM DELAY 1100 nSec (F = 0)

from the leading edge of the T pulse strobing the character just transferred.

Writing peripherals must accept a character from Do with lead and trail times defined in 5.1.2 and 5.1.3 and a T pulse defined in 5.2.1. Further when R is not ducked subsequent characters must be accepted according to 5.2.2.2.

The maximum delay will be less for fast peripherals (When F = 1) This will be defined later.

5.1.2 Leading edge skew.

The lines A, C, L, Do, No must be steady for a minimum time before T can be allowed to change from the logic zero state to the logic one state

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MINIMUM 400 nSec (F = 0)

or MINIMUM to be defined later (F = 1)

NO MAXIMUM

Further, in the case of data interrupts, processors must allow a minimum of 400 nSec (When F = 0) from the leading edge of R for Ni and J to become steady.

The processor must allow for the maximum peripheral turn around time before strobing a status character. Similarly when the direct response to a control command is to be inspected, the processor must hold back the strobe for the maximum peripheral turn around time. The use of the strobe for data is illustrated in Figs. 7, 8, 9 and 10.

5.1.3 Trailing edge skew

Similarly there is specified a minimum time which the lines A, C, L, Do, No, must remain steady after T has returned to the logic zero state.

MINIMUM 400 nSec (F = 0)

or MINIMUM to be defined later (F = 1)

NO MAXIMUM

5.1.4 Transfer of control characters and identifiers.

The rules governing the transfer of single characters under this heading are those given in 5.1.2, 5.1.3 and 5.2.1. In the case of multiple characters (e.g. a control code followed by a qualifier), the minimum time interval in which the peripheral must accept consecutive control characters is 2us.

5.2 Specific functions

5.2.1 Strobe (T)

The duration of T will be

MINIMUM 480 nSec (F = 0)

or MINIMUM to be defined later (F = 1)

MAXIMUM 10 uSec

Further, the minimum interval between the leading edges of successive pulses must be equal to or greater than 2 uSec AND the minimum interval between the trailing edge of one pulse and the leading edge of the next pulse must be equal to or greater than the duration of the pulse just transferred.

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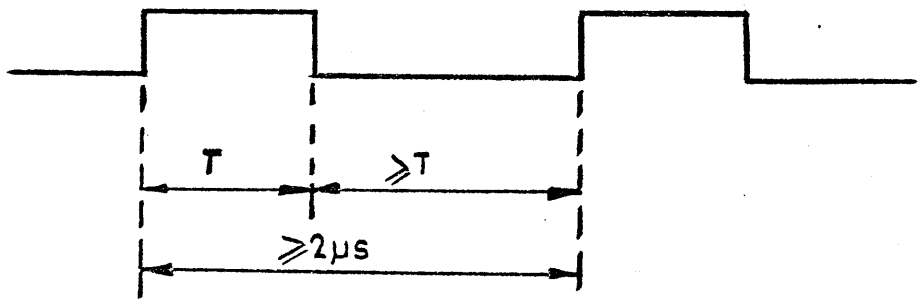
Thus:



5.2.2 Data request (R)

The peripheral will set the R line to logic 1 when it is able to transmit or receive a data character.

The processor will respond by raising the A line to logic 1. The operation of the R line by the peripheral when the A C = 10 condition is detected will depend on the peripheral characteristics and will be as follows:

5.2.2.1 Reading

When F = 0

A peripheral will duck R unless another character can be put on Di in less than 1100 nSec after the leading edge of T and is prepared to accept a T pulse with a minimum duration of 480 nSec. If R does not duck due to the condition previously mentioned, it will continue to remain at logic one until the leading edge of the T pulse strobing the penultimate character of a block, when it will duck within the period 0 - 750 nSec. If A now goes to logic zero, R will go to logic one within the period 0 - 750 nSec. R will be unset by T pulse strobing the final character of a block.

When F = 1

To be defined later.

The timing diagram, fig. 8, illustrates the operation of R, T, J and the characters on Di during a burst mode transfer.

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5.2.2.2 Writing

When F = 0

A peripheral will duck R unless another character can be accepted not later than 2 uSec. after the leading edge of 'T' and is prepared to accept a 'T' pulse of 480 nSec. with lead and trail times of 400 nSec.

When F = 1

To be defined later.

5.2.3.3 Burst mode

Certain restrictions may be placed on the number of characters that may be transferred in burst mode (i.e. when R does not duck) and when this mode is to be used, designers must check the compatibility of processors and peripherals in this respect.

5.2.3 Ni

Ni will occur in conjunction with R and J to indicate that there has been a change in the data identifier. Ni will be steady 400 nSec after the leading edge of R (When F = 0). When ACTNo = 1011, Ni will unset after the leading edge of T between the limits

MIN 0 nSec.

MAX 750 nSec.

The maximum delay will be less for fast peripherals (When F = 1). This will be defined later.

5.2.4 B Interrupt

The peripheral will set the 'B' line to logic 1 when certain status conditions arise. It will be ducked when AC = 11. It will be unset after the leading edge of T between the limits shown below according to the conditions given Fig. 4.

MIN 0 nSec.

MAX 750 nSec.

The maximum delay will be less for fast peripherals (When F = 1). This will be defined later.

5.2.5 Direction of data transfer (J)

J will occur in conjunction with R and will indicate whether the data character to be transferred is from a reading or to a writing mechanism (J = 0 writing, J = 1 reading) J will be steady 400 nSec. after the leading edge of R (When F = 0).

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5.2.5 Cont/d. Note that where identifiers are given on Di in response to No, J will indicate the direction of the data character which follows. J may change after the leading edge of T given with AC = 10 between the limits.

MIN 0 nSec

MAX 750 nSec

In all cases, J will cease to be valid after R unsets. This must not be confused with R ducking.

5.2.6 L, Limit

5.2.6.1 L will occur in conjunction with A and C and cause the termination of data transfers.

5.2.6.2 The change in the peripheral state due to L will be subject to the presence of T as described in 5.1.2 and 5.1.3.

5.2.6.3 L may arise simultaneously with a data character on Do or Di, in which case it will envelope the T pulse given by the processor for that data character.

5.2.6.4 Alternatively, L may arise when no data transfer is taking place, in which case it is regarded as a control command, with A C T L = 1 1 1 1 and Do = 0 0 0 0 0 0, the actual change in the peripheral being caused by T.

5.2.6.5 In both cases 5.2.6.3 and 5.2.6.4 above, the general rules for leading and trailing edge timing allowance as outlined in 5.1.2 and 5.1.3 apply.

5.2.6.6 In the case of a type 2 or 3 peripheral and additionally where type 4 or 5 peripherals use data identifiers, L given as described in 5.2.6.3 will terminate the data transfers associated with the data channel identified by the last data identifier which was transferred on Di.

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6.0 CODES USED ON THE INTERFACE

6.1 Data Codes

The interface allows a data character width of up to 8 bits + odd parity.

The Do and Di lines are identified by the symbols 2^0, 2^1, 2^2, 2^3, 2^4, 2^5, 2^6, 2^7, 2^8, where 2^0 is the line assigned to the least significant bit of a data character and 2^8 is the odd parity bit.

Peripherals and processors using less than the full complement of bits must assign the lines starting at the 2^0th bit, continuing 2^1, 2^2 ..... 2^7 etc. The parity bit (if used) will always be 2^8.

The relationship between peripheral and processor codes will be specified in other documents.

6.2 Control codes

The lines are similarly identified as indicated above, 6.1.

The codes should be restricted to the first 6 significant bits (i.e. 2^0 ....2^5). Parity is not used.

Figure 3 gives details of the code groups.

6.3 Status codes

The lines are similarly identified as indicated above, 6.1.

The codes should be restricted to the first 6 significant bits (i.e. 2^0 .... 2^5). Parity is not used.

Figure 4 gives details of the status codes.

6.4 Identifiers

The lines are similarly identified as indicated above, 6.1.

Up to 8 bits may be used. Peripherals and processors using less than the full complement of bits must assign the lines starting at the 2^0th bit, continuing 2^1 ..... 2^7 etc.

The parity bit (if used) will always be 2^8.

The identifiers are numbers placed on Do or Di (when No = 1) and are used to indicate a mechanism or channel address.

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6.4 Cont/d.

The precise assignment will be stated in the individual peripheral specification.

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7-0 STATUS CONDITIONS

Information describing the state of the peripheral is sent to the central processor on the Di lines in the form of status characters. These may only be sent in response to control codes of the 'SEND STATUS' group.

The status characters form an open set S_1, S_2, S_3 .....etc. for which there will be corresponding control codes, 'SEND STATUS S_1', 'SEND STATUS S_2' etc. (see Fig. 4-A)

Each status character S_n is coded such that bits $2^0 \ldots 2^4$ each represent a particular status condition and bit 2^5 is used as an 'escape' to indicate that at least one bit of S_{n+1} status is set.

The codes for S_1 and S_2 which have so far been defined are shown in figure 4, together with details of setting, resetting or unsetting. The S_1 set is called Q status, and the S_2 set is called P status.

When a 'SEND STATUS S_n' control character is sent together with A C T = 1 1 0, the peripheral will respond with the S_n status character on Di.

When a 'SEND STATUS S_n' control character is sent together with A C T = 1 1 1 action will be taken as described in the previous paragraph and in addition, the status of the individual statuses will be changed as defined in figure 4.

To avoid 'race' conditions the peripheral unit must be designed so that certain changes which can occur in the status conditions are held back until the condition A C = 1 1 vanishes. These conditions are indicated in figure 4.

Certain selected status conditions can signal their presence to the central processor on the 'B' line (which is a D.C. level and can signal to the central processor independently of the state of A C T).

These are known as 'interrupting' status.

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7.1 Some interrupting status can occupy three states, viz:

UNSET = When the status condition is absent.

SET 1 = when the status condition is present and affecting the B line.

SET 2 = when the status condition is present and not affecting the B line.

The SET 1 state of a status may be unset but be immediately set into the SET 2 state. This is referred to simply as a reset. Thus a reset defines a transition from the SET 1 to the SET 2, or SET 2 to the UNSET state of the status, whereas unset merely means the status ceases to exist in its previous SET state. If the SET 2 state is reset, then the status itself is UNSET i.e. absent.

7.2 Other interrupting status can occupy two states, viz:

UNSET = condition absent

SET 1 = condition present and affecting the B line

7.3 Status which are not interrupting can occupy two states, viz:

UNSET = condition absent

SET 2 = condition present but not affecting the B line

Examples 7.1 see Fig. 4d; 7.2 see Fig. 4a; 7.3 see Fig. 4g.

As the status may only occupy two states, it will be appreciated that the SET 2 state can only be replaced by one other state when unset i.e. the UNSET state. Thus reset and unset must mean the same thing when referring to the SET 2 state or a two state status.

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8.0 ELECTRICAL SPECIFICATION

8.1 Introduction

8.1.1 The objective is to provide a signal path between two equipments, in general, a Central Processor and a Peripheral Unit, for the transmission of a signal unidirectionally from one equipment to the other. The signal is to be interpreted unambiguously by the receiving equipment in the presence of electrical noise due to adjacent signal paths or external causes. In particular, a difference in the nominal earth (zero volt) potentials between the two equipments is to be tolerated.

8.1.2 Each signal path will consist of a transmitter element, an interconnecting cable, and a receiver element designed to match the cable impedance.

8.1.3 The signal transmitted will be at a standard current level, nominally 25mA. 'Logic 1' as referred to in Section 4 of this specification is defined as a particular polarity of current in a specified core of the cable.

8.1.4 Transmitter and receiver elements situated in the Central Processor will, in general, be part of the family of circuit elements peculiar to that Central Processor.

8.1.5 Transmitter and receiver elements situated in the Peripheral Unit will, in general, be part of the family of Standard Peripheral Circuit elements; exceptionally they may be part of a family of circuit elements peculiar to the particular Peripheral Unit.

8.1.6 From the consideration above, and the detailed signal specification it follows that any transmitter element will drive any receiver element irrespective of the circuit element family of which either is a part.

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8.2 Standard Signal

The following definitions and parameters will apply to all signals across the interface except Ho and Hi (see Section 8.3.6).

8.2.1 Signal Level

(a) A 'Logic 1' is a current within the range +17mA to +31mA flowing in Core A of the signal path cable from transmitter to receiver, and a current not greater than ± 1mA flowing in Core B, from transmitter to receiver.

(b) A 'Logic 0' is a current within the range +17mA to +31mA flowing in Core B of the signal path cable from transmitter to receiver, and a current not greater than ±1mA flowing in Core A, from transmitter to receiver.

(c) In (a) and (b) above the usual sign convention is assumed, i.e. that a positive current is a current flow from a potential to a more negative potential.

8.2.2 Signal Timing

A 'logic 1' is timed at the points in the differential current waveform at which the current in Core A exceeds that in Core B by 14mA. A 'Logic 0' is timed at the points in the differential current waveform at which the current in Core B exceeds that in Core A by 14mA.

The logic state will be indeterminate during the transition periods, i.e. when the differential current is less than 14mA.

8.2.3 Signal Terminations

The centre tap of the termination resistance of the cable shall be returned to a supply having a potential within the limits of -9 to -7 volts with respect to the receiver earth, and able to deliver at least 31mA for each transmitter connected.

8.3 Transmitter and Receiver Elements

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8.3.1 The transmitter shall be able to transmit the standard signal along the specified cable when component values, power supply lines and ambient conditions in the transmitting equipment are at their worst tolerance and when a maximum difference of ± 4 volts exist between the nominal earth (zero volt) potentials of the two equipments.
The design of the transmitter must also allow, by providing additional voltage rating or by other means, for any ringing induced in the cable by out of balance currents from the transmitter.
As a guide to the amount of ringing which may be present, a simulated worst case test shows the ringing as a 2.2 volts source in series with 12,000 ohms between the transmitter outputs and zero volts.

8.3.2 The receiver shall be able to receive the standard signal and interpret it unambiguously when component values, power supply lines and ambient conditions in the receiving equipment are at their worst tolerance, when a maximum difference of ± 4 volts exist between the nominal earth (zero volt) potentials of the equipments and in addition there is a maximum out of balance noise current of ± 2mA induced in either core of the twin cable.

8.3.3 The transmitter and receiver elements will provide any level translation or polarity inversion required to match the standard signal to the logic level and polarity required in the particular equipment in which they are situated.

8.3.4 For Line G, referred to in Section 3.15, the transmitter may be a simple D.C. current source, provided that the standard signal specification is met in respect of all parameters.

8.3.5 Note that for the correct operation of a transmitter/receiver pair it is essential to provide a D.C. connection between the zero volt lines in the two equipments (see Section 8.5.4)

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8.3.6 Power present Lines Ho, Hi

For these lines the transmitter will consist of a pair of relay contacts electrically isolated from the equipment in which the relay is situated and unique for every Ho/Hi.
A logic '1' exists when the contacts are closed, a logic '0' when the contacts are open.
The current passed through these contacts must not exceed 400mA D.C. and the supply from which this current is derived must not exceed 35v D.C.
The receiver may be any circuit which does not cause the above current and voltage limits to be exceeded.
The connection between the pins in the fixed plug and the relay contacts will be in twisted pair.

8.4 Transmission Cable

8.4.1 The multi-way transmission cable will consist of 37 twin cables of which up to 34 are required. The Multi-way cable will have an overall screen.

8.4.2 Each twin cable will have a nominal characteristic impedance of 93 ohms and, at 50 Mc/s, a nominal delay of 1.5 nS/ft.
The detailed electrical specification is given below:

TEST	CONDITION	LIMITS		
		Min.	Max.	Units.
High Voltage	1Kv RMS for 5min	-	-	-
Insulation resistance	500v D.C.	750,000	-	Megohms for 100ft
Conductor resistance	D.C. at 20°C	-	2.8	Ohm/100 ft.
Spark test	2Kv RMS	-	-	-
Capacitance	1000 c/s	15	18	pF/ft
Characteristic impedance	50 Mc/s	89	99	Ohms
Velocity ratio	50 Mc/s			
Attenuation constant	50 Mc/s	-	9.0	-
Cross talk attenuation	50 Mc/s	25	-	db down for 100 yards.

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8.5 Cable Connections

8.5.1 Each core of the cable will be allocated to a specified pin of the plug and socket at the Peripheral Unit as listed in 9.4.1.

8.5.2 The connections between the transmitter or receiver elements and the sockets in the equipment in which they are situated shall be in twin cable similar to that specified for the transmission cable.

8.5.3 Three twin cables are allocated to the Z (zero volt) line. The Z line will be connected to the zero volt system of the Central Processor at a point adjacent to the transmitter and receiver elements.

8.5.4 The Z line may or may not be directly connected to the zero volt system of the Peripheral Equipment. This will be defined in the overall specification for the particular system and may be different for different Peripherals in the one system, and for the same Peripheral in different systems. If the Z line is not directly connected then an alternative low impedance D.C. path must be provided between the zero volt systems of the Processor and Peripheral Equipment.

8.5.5 In view of the alternative connections given in 8.5.4. above, it is desirable to make provision for protecting the transmitter and receiver elements against possible damage due to mains leakage when either the interface cable or the mains cable to the Peripheral Equipment is unplugged while the equipment is operating. This may be achieved by connecting a resistor or suitably designed inductor having a D.C. resistance not greater than 1,000 ohms between the zero volt system of the Peripheral Equipment and either:

(a) The earthed frame of the Peripheral Equipment in the case where the Z line is directly connected to the zero volt system of the Peripheral Equipment.

(b) The Z line, in the case where the Z line is not directly connected to the zero volt system of the Peripheral Equip-

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8.5.5 Cont/d.

ment and the necessary zero volt connection between the units is made externally to the interface cable.
The frame of the Peripheral Equipment will be earthed.

8.5.6 The cable overall screen will be connected to the machine frame at the Central Processor end only.

8.5.7 Some twin cables may be unused because they are allocated as 'spare', or for use on types 2, 3, 4 and 5 peripherals, or for use on an 8 bit data interface.
The unused lines should be treated as follows:-

8.5.7.1 At the Peripheral:
Any pair of pins on the fixed plug which is allocated to a receiver input (i.e. at the receiving end of any OUT line) but to which no receiver is in fact connected, should be joined together with a 91 ohm CS10 resistor. This resistor will terminate the twisted pair constituting an interface line and will be isolated from OV or any power supply rail.
The 'spare' lines should be terminated with a 91 ohm CS10 resistor and isolated from OV or any power supply rail.
Any pair of pins allocated to a transmitter output but to which no transmitter is connected, will be left open circuit.

8.5.7.2 At the Central Processor:
When they are unused, the Ni or J lines should be terminated by a 91 ohm CS10 resistor. This resistor will terminate the twisted pair constituting an interface line, and will be isolated from OV or any power supply rail. The lines Di 2^6, Di 2^7, Di 2^8 and F, when unused will be left open circuit. The 'spare' lines will be left open circuit.
Any pair of pins allocated to a transmitter output but to which no transmitter is connected, will be left open circuit.

8.6 Disconnection of Cable

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8.6.1 If the cable is not connected, all outputs from transmitters and inputs to receivers will, in general, be indeterminate.

8.6.2 Disconnecting the cable while power is present is not recommended as general practice. Exceptionally this may be done, but the Central Processor system will usually require that Line Hi is set to Logic 0 (as referred to in para. 8.3.6) before the cable is disconnected. This may be achieved by operation of a manual switch in the Peripheral Unit, or by other means.

9.0 PHYSICAL SPECIFICATION

9.1 Introduction

9.1.1 The objective is to specify the method of connecting transmission cables to a Peripheral Device which has the I.C.T. Standard Interface.
The Interface is defined as lying between the fixed plug on the Peripheral, and the Free socket on the transmission cable from the Central Processor. Both the Free socket and the transmission cable are considered to be part of the Central Processor. This specification, however, gives guidance in their design, in that the cables would generally be connected to the Central Processor by connectors of the same type as those used at the peripheral end.

9.1.2 Requirements
The requirements exist, therefore, for the provision of terminations for a 37 pair R.F. cable, the cable conforming to the electrical requirements laid down in Section 8.4 of this specification.

9.2 Transmission Cable I.C.T. Part No. 958474 (Computer Equipment No. 1548 - 491)

9.2.1 Physical Properties
The transmission cable has the following physical properties.

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9.2.1 Cont/d.

Specification:

37 pair Radio Frequency cable having 7/.0076" Plain Copper Wire Conductors, Polythene insulated to .040" ± .001" dia. Two such cores twisted to form a pair, 37 pairs laid up, two laps polythene taped, braided with .0076" tinned copper wires and PVC sheathed. black. .045" radial thickness.

Overall Diameter .636" ± .020".

Colour Code.

The colour code for the polythene insulation of the pairs of conductors is as follows:

Centre Pair

Black	White

1st Layer

Black	Blue
Black	Orange
Black	Green
Black	Brown
Black	Grey
Black	Red

2nd Layer

White	Blue
White	Orange
White	Green
White	Brown
White	Grey
White	Red
White	Yellow
White	Violet
Blue	Orange
Blue	Green
Blue	Brown
Blue	Grey

3rd Layer

Orange	Green
Orange	Brown
Orange	Grey

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9.2.1 Cont/d.

Orange	Red
Orange	Yellow
Orange	Violet
Green	Brown
Green	Grey
Green	Red
Green	Yellow
Green	Violet

3rd Layer

Brown	Grey
Brown	Red
Brown	Yellow
Brown	Violet
Grey	Red
Grey	Yellow
Grey	Violet

This cable is obtainable from Messrs. British Insulated Callenders Cables Ltd., under their Specification No RPC. 3239B.

9.3 Connector

9.3.1 General Description

The connector used should be a 75-way cable mounting socket and panel mounting plug with an overall cable clamp.

9.3.2 Connector Details.

The connector specified is a 75 way version of the BICC-Burndy Ltd., type MS HYFEN with size 22 (.040 dia) pins. This connector will be made up with parts to BICC-Burndy reference as follows:-

a) Cable Mounting Parts

ITEM	QTY.	BICC REF.	I.C.T. PT. NO.
Contact (Socket)	75	RC22W-BID29	889571
Moulding and Hood Assy.	1	MS75P-B157	5005491
Guide Socket.	4	MS14P-BIP3	889566

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9.3.2 Cont/d.

b) Panel Mounting Items.

ITEM	QTY.	BICC REF.	I.C.T. PT. NO.
Contact (Pin)	75	RM22W-BID29	889570
Receptacle	1	MS75R-B7T	889568
Guide Pin	4	MS34P-BIP12	889567

NOTE:

In addition to the above items, a pin extraction tool will be required, BICC ref. RX20/10 and a Hand Crimping Tool BICC ref. M10S-1 with die set S-10 and locator SL14.

9.4 Cable/Connector Terminations.

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9.4.1 Termination Details

The transmission cable will be terminated as detailed below:

Twisted Pair	Pin No. & Terminating Wire Colour				Wire Function	Code
Colours	CORE A		CORE B			
	Pin	Colour	Pin	Colour		
White/Blue	1	White	4	Blue	Data Out	$Do2^0$
White/Orange	2	White	5	Orange	Data Out	$Do2^1$
White/Green	3	White	7	Green	Data Out	$Do2^2$
White/Brown	8	White	12	Brown	Data Out	$Do2^3$
White/Grey	10	White	13	Grey	Data Out	$Do2^4$
White/Red	11	White	14	Red	Data Out	$Do2^5$
Grey/Violet	15	Grey	18	Violet	Data Out	$Do2^8$
Brown/Grey	16	Brown	20	Grey	Data Out	$Do2^6$
Brown/Red	17	Brown	21	Red	Transfer Control	C
Brown/Violet	22	Brown	25	Violet	Device addressed	A
Orange/Violet	23	Orange	26	Violet	Data Out	$Do2^7$
Green/Brown	24	Green	27	Brown	Data In	$Di2^6$
Green/Grey	28	Green	31	Grey	Data In	$Di2^7$
Green/Red	29	Green	32	Red	Limit	L
Brown/Yellow	30	Brown	33	Yellow	Identifier In	Ni
Black/Blue	34	Black	37	Blue	Timing Signal	T
Black/Orange	35	Black	38	Orange	General Reset	G
Black/Green	36	Black	39	Green	Power Present at Processor.	Ho
Black/Brown	40	Black	43	Brown	Data In	$Di2^0$
Black/Grey	41	Black	44	Grey	Data In	$Di2^1$
Black/Red	42	Black	45	Red	Data In	$Di2^2$
Grey/Red	46	Grey	49	Red	Data In	$Di2^3$
Blue/Orange	47	Blue	50	Orange	Data In	$Di2^4$
Blue/Green	48	Blue	51	Green	Data In	$Di2^5$
Blue/Brown	52	Blue	55	Brown	Data In	$Di2^8$
Blue/Grey	53	Blue	56	Grey	Identifier out	No
White/Yellow	54	White	57	Yellow	Request Data Transfer	R
White/Violet	58	White	62	Violet	Break-in	B
Orange/Green	59	Orange	63	Green	Direction of Transfer	J
Orange/Brown	60	Orange	64	Brown	Fast Transfer	F
Orange/Grey	65	Orange	70	Grey	Spare	
Orange/Red	66	Orange	71	Red	Spare	
Orange/Yellow	67	Orange	72	Yellow	Spare	
Green/Yellow	73	Green	76	Yellow	Power Present at Peripheral	Hi
Green/Violet	74	Green	77	Violet	0 Volt	Z1
Grey/Yellow	75	Grey	78	Yellow	0 Volt	Z2
White/Black	79	White	80	Black	0 Volt	Z3
Screen	82	Screen	-	-	SCREEN	

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12 9.4.2 Method of Assembly

The Piece Parts of the Connectors detailed in Paragraph 9.3.2 should be assembled in accordance with Instructional Drawings as follows:-

ASSEMBLY	I.C.T. PT. NO.
PANEL MOUNTING	5005492
CABLE MOUNTING	5005493

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10-0 USE OF THE INTERFACE

10-1 Multi-Channel/multi mechanism operation (Peripheral types 2 and 3 and possibly 5).

Control identifiers (mechanism or channel addresses), control codes and data characters are multiplexed on Do.
Data identifiers, status and data characters are multiplexed on Di.
The control line C = 1 indicates that the character present or about to be present on Do is a control character or, in conjunction with No, control identifier.
The control conditions A C No = 1 1 1 indicates that the character present, or about to be present on Do is a control identifier.
The control conditions A C No = 1 0 1 indicates that the peripheral will put a data identifier on Di.
Ni is used by the peripheral when an 'R' data transfer request is made to indicate that the data identifier has changed since the last data character was transferred.
The control condition A C No = 1 0 0 indicates that the character present or about to be present on Do or Di is a data character.
For more details of control conditions refer to figure 2.
The status information transmitted on Di is of two types, firstly the status of the peripheral control unit which is given as a 'direct response' to the control condition A C = 1 1.
The direct responses are confined to the indication of three states, i.e. operability, ability to accept a control order, rejection of a control order. Secondly, an open ended group of status is available to indicate the state of both the peripheral control unit and the mechanism. These statuses are given by the peripheral on Di in response to 'SEND STATUS' control codes from the processor. Both types of status may be asked for by the processor at any time by putting up the appropriate control lines and/or control codes. Status and direct responses are dealt with in detail in other sections of this document.
A typical example of a processor implementing a command is as follows:

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10.1.1 Initiation

There are several ways in which initiation of a command may be achieved. Since direct response status is available simply by raising A C = 1 1, a processor may examine this type of status before giving every control code or identifier. The direct response will be available after the peripheral turn around from the steady state of the control conditions, or the leading edge of T, as appropriate.

However, this method is not obligatory, and commands may be given more rapidly by the following method. Assuming a 2 x n magnetic tape system, which ducks R when A arise and has F = 0.

The steps shown in the examples which follow are given as the 'steady state' condition. In practice, the timing rules given in section 5 should, of course, be observed.

1) A C T No = 1 1 1 1 Do = control identifier } Switch mechanism (address given by identifier) to channel n (given by X X X X in control code)

2) A C T No = 1 1 1 0 Do = control code - - - 1 0 X X X X

3) A C T No = 0 0 0 0 (processor leaves this interface)

4) 'B' interrupt from the peripheral.

5) A C T No = 1 1 0 0 Do = control code 'IDENTIFY'

6) After peripheral turn around from the steady state of the control conditions, the interrupting identification will be on Di. Processor stores this to use as a control identification later.

7) A C T No = 1 1 1 1 Do = Control identifier obtained at step (6)

8) A C T No = 1 1 1 0 Do = Control command 'SEND STATUS Q'

9) We will assume that the 2^2, 2^3 and 2^4 bits of the Q status character are set. The 2^3 and 2^4 bits indicate that the control unit of the peripheral may accept and implement immediately a control command. The 2^2 bit indicates that the tape deck addressed is physically capable of responding to control commands

10) A C T No = 1 1 1 0 Do = Control command to be given to connected mechanism.

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10.1.1 Cont/d.

The foregoing is a typical sequence used to initiate a control command. For the purpose of this illustration, we will assume that a 'WRITE' command has been given.

10.1.2 Data Transfer

11) Peripheral interrupts with R J Ni = 1 0 1, processor must allow a minimum of 400 n sec from leading edge of R before examining J Ni.

12) A C T No = 1 0 1 1 Di = Data identifier: Processor accepts identifier. Peripheral must unset Ni after leading edge of T. Peripheral will duck R.

13) R J Ni = 1 0 0

14) A C T No = 1 0 1 0 Do = data character Peripheral accepts data character from processor.

If further data characters from the same data block are to be transmitted. (13) and (14) will be repeated. Ni in this case would be 0.

If a data character of a new block is to be transmitted steps (11) and (12) will occur to identify the new block, followed by steps (13) and (14) as required.

10.1.3 Termination

Either the processor or the peripheral may terminate the command. If the processor terminates, it will do this by raising the limit line 'L' to logic 1 during the transmission of the final data character, or after the final data character has been sent. The peripheral will set the 'TERMINATED' status and give a 'B' interrupt when it has done so. Details are given in the 'Function of lines' section. In those peripherals which it is appropriate to include a counting device, the peripheral may terminate as follows:

15) B interrupt

Processor makes steps (5), (6), (7) followed by:

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10.1.3 16) A C T No = 1 1 0 0 Do = control command 'SEND STATUS Q'
The 2^0 bit of the Q status will indicate 'TERMINATED'.
After the status bits have been examined the processor will send 'T' which will unset or reset the Q status bits.

10.2 Single channel/single mechanism operation (peripheral type 1)
In this case identifiers are not used since the A line is unique to a peripheral and is sufficient identification.
The command sequence is much simplified therefore.

10.2.1 Initiation
This will involve step (10) only, unless status requests are made either before or after.

10.2.2 Data transfer
This involved step (13) (J either 1 or 0 depending whether peripheral is a reading or writing device, Ni not used) and step (14)

10.2.3 Termination
The condition leading to termination is the same as type 2 and 3 peripherals. If the peripheral is terminating itself, the procedure is a B interrupt followed directly by step (16)

10.3 Direct data exchange operation (peripheral type 4)
Refer to section 11.0.

10.4 General
Once a command is given by the processor to a peripheral, and accepted, the functional connection between the two is severed. The next action arises from the peripheral and will be either an 'R' or a 'B' interrupt. The 'R' is a request by the peripheral indicating that it is ready for a data transfer. The processor will service the 'R' request, recognising the appropriate priority of the interrupting peripheral connected by that interface. Whilst 'R' interrupts will usually be dealt with by hardware control, the 'B' interrupt, which has lower priority, will lead to a program interrupt. The response by the processor to a 'B' interrupt will

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10-4 Cont'd be a status request.

Conventionally the Q status is examined first as the bits assigned to this character indicate statuses which are expected during normal operation. The 2^5 bit of Q status is assigned to indicate that there are status bits set in the P_n status groups. Similarly each P status group has an escape bit, thus the P status groups are 'open ended'.

10-5 Bussing

Certain control lines may be joined to a common bus in the processor, providing the processor deals with one interface character at a time.
These are the GACTNoL Do sets. However, it is not possible to bus all these groups; at least A or T must be retained as unique lines to each interface. R, B, Ni, J & F must not be bussed. The data line Di may also be joined to a common bus providing the A lines are unique.

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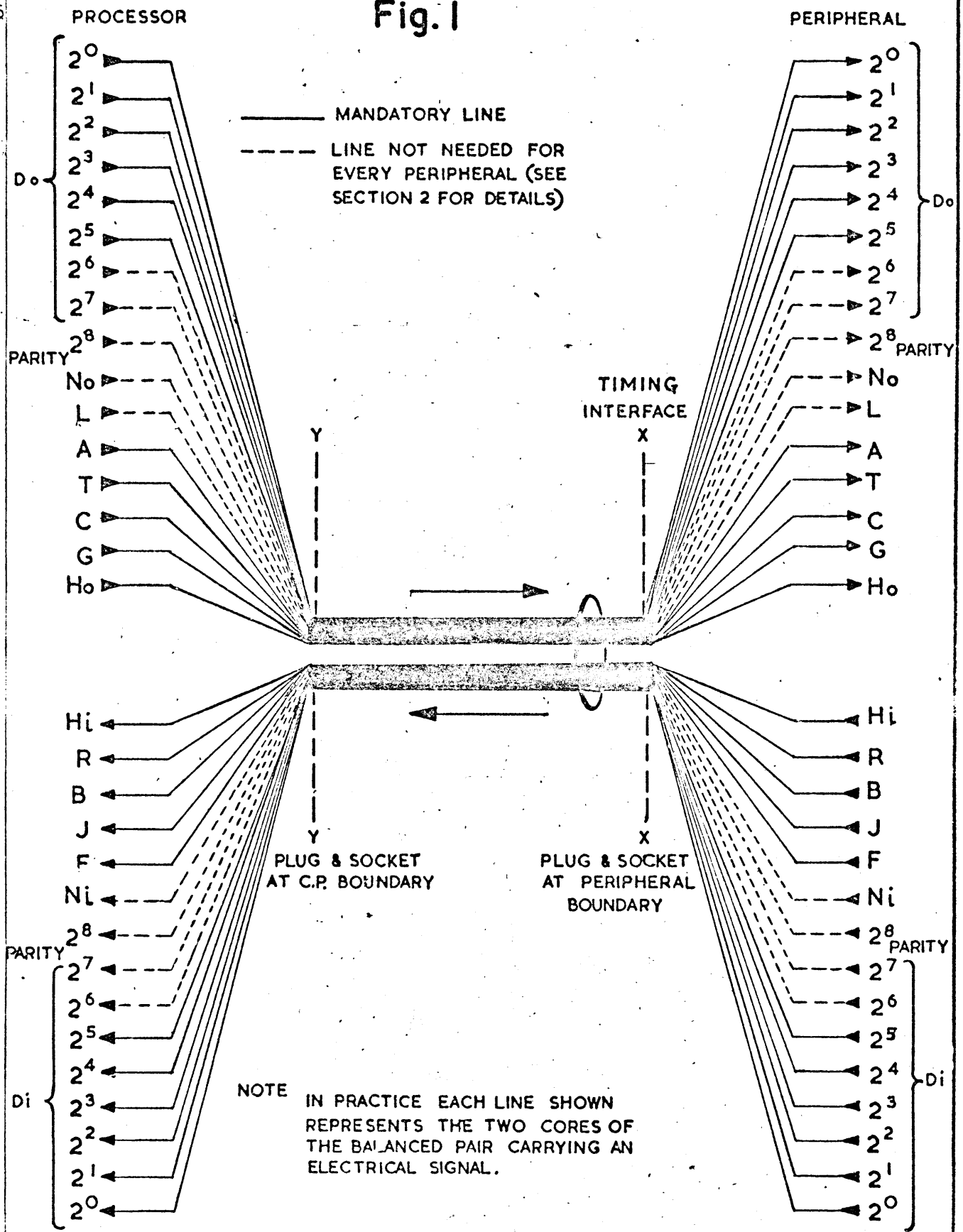
Fig. 1



INTERFACE LINES, Schematic

Fig.2. CONTROL CONDITIONS Note: 'X' means that the lines may have any value.

Ref:	CAUSE				EFFECT		
	A T C No	Do	State of Peripheral	Remarks	Di	Irreversible effects in peripheral	Remarks
a	0 X X X	X	ANY	'A' is the line which activates the peripheral	ALL ZEROES	NONE	When A = 0, the peripheral must ignore all incoming lines except G & Ho, and should maintain all zeros on Di
b	1 0 0 0	X	READING		THE INPUT DATA CHARACTER	NONE	When AC = 10 the 'R' line is subject to special conditions. Refer to 'R' timing
c	1 0 0 0	X	NOT READING		X	NONE	When AC = 10 the 'R' line is subject to special conditions. Refer to 'R' timing.
d	1 0 0 1	X	ANY	Processor is asking for a data identifier in response to an 'R' interrupt	DATA IDENTIFIER	NONE	When AC = 10 the 'R' line is subject to special conditions. Refer to 'R' timing
e	1 1 0 0	X	READING		X	peripheral may remove the input data character. Refer also to 'R' timing	AT = 11 informs the peripheral that the processor has received the input character.
	t	u	v	w	x	y	z

Fig.2 (cont'd)

Ref:	CAUSE					EFFECT	
	A T C No	Do	State of peripheral	Remarks	Di	Irreversible effects in peripheral	Remarks
f	1 1 0 0	The output data character	WRITING		X	Peripheral will accept the output data character Refer also to 'R' timing	AT = 11 informs the peripheral that the character on Do is steady.
g	1 1 0 0	X	READING OR WRITING	A data character has been transferred	X	If the next data character has a new identifier, Ni must be set and the identifier changed before the next 'R' occurs.	When AC = 10, the 'R' line is subject to special conditions. Refer to 'R' timing Processors should not give this control except in response to an 'R'.
h	1 1 0 1	X	ANY	Processor has accepted a data identifier.	X	Peripheral must unset Ni and remove the data identifier.	When AC = 10, the 'R' line is subject to special conditions. Refer to 'R' timing. Processors should not give this control except in response to an 'R'.
	t	u	v	w	x	y	z

Fig.2. (Cont'd)

Ref:	CAUSE				EFFECT			
	A T C No	Do	State of Peripheral	Remarks	Di	Irreversible effects in peripheral	Remarks
i	1 0 1 0	'SEND STATUS' OR IDENTITY	ACTIVE	Processor is asking for status or a control identifier	RELEVANT STATUS CHARACTER, OR CONTROL IDENTIFIER	NONE	When AC = 11 the perepheral should duck 'B' while the condition lasts
j	1 0 1 0	OTHER CONTROL CODES	ACTIVE	The effect is assuming control is valid. The effect for other codes is indeterminate	DIRECT RESPONSE CHARACTER	NONE	When AC = 11 the peripheral should dick 'B' while that condition lasts.
k	1 0 1 1	THE CONTROL IDENTIFIER	ACTIVE		DIRECT RESPONSE CHARACTER	NONE	When AC = 11 the peripheral should duck 'B' while the condition lasts.
l	1 1 1 0	'SEND STATUS' OR 'IDENTIFY'	ACTIVE		RELEVANT STATUS CHARACTER OR CONTROL IDENTIFIER	Peripheral will reset the relevant statuses (If Do = 'SEND STATUS')	(i) When AC = 11 the peripheral should duck 'B' while the condition lasts. (ii) The status character on Di may change due to 'T'.
	t	u	v	w	x	y	z

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Fig;2 Cont'd.

Ref:	CAUSE				EFFECT		
	A C T No	Do	State of Peripheral	Remarks	Di	Irreversible effects in peripheral	Remarks
m	1 1 1 0	OTHER CONTROL CODES	ACTIVE	Assuming control is valid. The effect for other codes is indeterminate.	DIRECT RESPONSE CHARACTER	Peripheral will accept the control if able to do so.	(i) When AC = 11 the peripheral should duck 'B' while the condition lasts. (ii) The direct response character on Di may change to 'T'
n	1 1 1 1	THE CONTROL IDENTIFIER	ACTIVE	Processor is sending a control identifier.	DIRECT RESPONSE CHARACTER	Peripheral will accept the control identifier.	(i) When AC = 11 the Peripheral should duck 'B' while the condition lasts. (ii) AT = 11 informs the peripheral that the control identifier is steady.
	t	u	v	w	x	y	z

NOTE: The peripheral turn around time should be considered when using the 'EFFECT' columns. For instance, the status and direct response characters may not be steady on Di until the expiration of the maximum peripheral turn around time from the steady conditions of A C No Do. Similarly, if the 'T' strobe is sent, Di may change, and may not be steady until the expiration of the maximum peripheral turn around time from the leading edge of 'T'.

For example, in the case A T C No = 1 1 1 0, the original direct response before the arrival of the 'T' strobe cannot be examined unless 'T' is delayed after A C No a time equivalent to the peripheral turn around. A new direct response, due to the peripheral accepting the character from Do may be given after the expiration of the peripheral turn around from the leading edge of 'T'. Individual peripheral specifications should be examined to obtain more information regarding the effect of 'T' and direct responses. The use of the direct response characters by the processor is optional.

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Fig. 3.

CONTROL CODE GROUPS

CONTROL CHARACTER $2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0$	GROUP	DESCRIPTION OF THE GROUP
- - - 0 0 X X X X	0	PERIPHERAL ASSIGNMENT Each peripheral may be allocated its own codes within this group and this code (if used) must be specified in the individual peripheral specification.
- - - 0 1 1 X X X	1	NORMAL CONTROLS This group comprises the normal controls which are common to peripherals. The detailed code is shown in Fig 3-B
- - - 0 1 0 X X X	2	STATUS TESTS This group comprises all the 'SEND STATUS' controls and the 'IDENTIFY' control. The detailed code is shown in Fig 3-C
- - - 1 0 X X X X	3	CONNECTING CONTROLS This is one control, i.e., $2^5 2^4 = 10$, with $2^3 - 2^0$ reserved for channel or mechanism addresses. It is used to establish a connection between mechanisms and channels
- - - 1 1 X X X X	4	ALLOCATED FOR CENTRAL PROCESSOR This group of codes is allocated for central processor use and should have no irreversible effect on the peripheral device.

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Fig. 3-A

PERIPHERAL ASSIGNED CODES. GROUP 0

Guidance as to the codes to be used by peripherals may be obtained from the "Standard Interface Code of Practice" document. Wherever possible, similar functions should use identical codes.

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Fig. 3-B

12 NORMAL CONTROLS, GROUP 1

CONTROL CHARACTER $2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0$	CONTROL NAME	DESCRIPTION
- - - 0 1 1 0 0 1	READ	For reading devices, initiate a data transfer from the peripheral to the processor, otherwise FREE.
- - - 0 1 1 0 1 0	WRITE	For writing devices, initiate a data transfer from the processor to the peripheral, otherwise FREE.
- - - 0 1 1 1 1 0	DISCONNECT	Place the peripheral under operator control where this is applicable, otherwise FREE.
- - - 0 1 1 1 1 1	BOOTSTRAP	Upon receipt of this code a reading peripheral will read in some basic mode starting from some convenient set point on the media such that address and qualifiers need not be sent in addition to the code. This will be mandatory for reading devices.
- - - 0 1 1 X X X (Excepting above)		FREE

Codes when used, will be specified in the individual peripheral agreed specification.

Fig. 3-C

STATUS TESTS, GROUP 2

CONTROL CHARACTER $2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0$	CONTROL NAME	DESCRIPTION OF GROUP
- - - 0 1 0 1 0 0	SEND STATUS P_1	This control causes the peripheral to put the P_1 status character on Di not later than the turn around time defined for the peripheral after the control conditions are steady.
- - - 0 1 0 0 0 0	SEND STATUS Q	As above, except that the Q status character is sent.
- - - 0 1 0 0 0 1	IDENTIFY	As above, except that the control identifier is sent.
- - - 0 1 0 1 1 0 1	SEND STATUS P_2	As above, except that the P_2 status character is sent.

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FIG. 3-D

ADDITIONAL CODES

CONTROL CHARACTER $2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0$	CONTROL NAME	DESCRIPTION
- - - 0 0 0 0 0 0	DO NOTHING	The peripheral must be designed so that this code will cause no irreversible effect.
- - - Y Y X X X X	QUALIFY	Used by some peripherals as a qualifier following a normal command. The code may contain additional information relating to the command. YY may be 10, 01, 00 but not 11. The qualify code all zeroes is allowed, in which case it will not necessarily mean 'DO NOTHING'. Where the qualify code "all zeroes" is meaningful, the peripheral must ensure that when ACL = 111, all zeroes on Do means (in this case) a control code 'DO NOTHING' and the LIMIT operation will be performed.

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Fig. 4. STATUS CHARACTER RESPONSE GIVEN BY PERIPHERAL ON Di LINES IN RESPONSE TO A 'SEND STATUS Q' CONTROL CODE
Where a Q status bit is to be used by a peripheral, it must be used for the status shown below unless marked FREE. Refer to Fig. 4A for reduced facility peripheral status.

STATUS CHARACTER APPEARING ON Di. $2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0$	STATUS NAME	SET 1 STATE		SET 2 STATE		
		SET	UNSET	SET	UNSET	
- - - X X X X X X	TERMINATED	(i) L line raised and processes defined in peripheral agreed spec. completed. (ii) End of Data Block.	SSQ. T or start of next block.	Cannot exist.		
- - - X X X X X X	SEMI-TERMINATED	End of intermediate data block	SSQ.T or start of next intermediate block.	Cannot exist.		*
- - - X X X X X X	FREE	To be defined for each peripheral.				
- - - X X X X X X	STOPPED 1	An appropriate control order as defined in the peripheral agreed spec. will be accepted.	SSQ.T or Causative condition ends.	SSQ.T if previously in SET 1 state	Causative condition ends.	
- - - X X X X X X	STOPPED 2	An appropriate control order will be accepted and implemented immediately. This status should not be set before TERMINATED has been set for the previous data block.	SSQ.T or causative condition ends.	SSQ.T if previously in SET 1 state.	Causative condition ends.	
- - - 0 X X X X X	P_1 STATUS ON	At least one of the P status set.	SSQ.T or causative condition ends.	SSQ.T if previously in SET 1 state.	Causative condition ends.	**

Fig. 4. Cont/d.

Any status may cause a B interrupt depending on the system of which the peripheral is a part. However where a status is arranged to cause a B interrupt, the peripheral must be so designed that the status may be disconnected from the B line if desired. A processor must wait the maximum peripheral turn around time before resetting status with the strobe. Changes in state which would result in a status condition must not be allowed to effect this until the condition AC = 11 vanishes.

References:

* This status is FREE, to be defined in the peripheral agreed specification, for those peripherals that do not use SEMI-TERMINATED

** see Fig. 4-B.

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Fig. 4. STATUS CHARACTER RESPONSE GIVEN BY PERIPHERAL ON Di LINES IN RESPONSE TO A 'SEND STATUS P_1' CONTROL CODE
Where a P_1 status bit is to be used by a peripheral, it must be used for the status shown below unless marked FREE. Refer to Fig. 4-A for reduced facility peripheral status.

STATUS CHARACTER APPEARING ON Di $2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0$	STATUS NAME	SET 1 STATE		SET 2 STATE		
		SET	UNSET	SET	UNSET	
- - - X X X X X 0	INOPERABLE	Peripheral ceases to be operable and becomes unserviceable to the processor.	SSP_1.T or causative condition ends.	SSP_1.T if previously in SET_1 state or if unserviceable due to transition from Hi=0 to Hi=1 condition.	Causative condition ends.	**
- - - X X X X 1 1	WARNING	(i) HOLD button pressed. (ii) WARNING	SSP_1.T or causative condition ends.	SSP_1.T if previously in SET 1 state.	Causative condition ends.	
- - - X X X 1 X 1	ERROR	Parity error Data error	SSP_1.T or next READ or WRITE order.	SSP_1.T if previously in SET_1 state or if no interrupt is required when status is set.	Next READ or WRITE order.	
- - - X X 1 X X 1	ATTENTION	A warning condition not requiring such urgent processor action as WARNING (See individual Peripheral Agreed Specs)	SSP_1.T or causative condition ends.	SSP_1.T if previously in SET 1 state.	Causative condition ends.	*
- - - X 1 X X X 1	FREE	To be defined for each	peripheral.			
- - - 1 X X X X 1	P_2STATUS ON	At least one of the P_2 status contributing is set (See Individual Peripheral Agreed Specs)	SSP_1.T or causative condition ends.	SSP_1.T if previously in SET 1 State.	Causative condition ends.	

References: *This status is FREE, to be defined in the peripheral agreed specification for peripherals that do not use ATTENTION.
**See Fig. 4-B.

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Fig. 4. Cont/d.

Any status may cause a B interrupt depending on the system of which the peripheral is a part. However where a status is arranged to cause a B interrupt, the peripheral must be so designed that the status may be disconnected from the B line if desired. A processor must wait the maximum peripheral turn around time before resetting status with the strobe. Changes in state which would result in a status condition must not be allowed to effect this until the condition AC = 11 vanishes.

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Fig. 4-A STATUS CHARACTER RESPONSE GIVEN BY A REDUCED FACILITY PERIPHERAL TO ANY CODE IN THE STATUS TEST GROUP.
This table shows the subject of Fig.4. to be used by reduced facility peripherals.

STATUS CHARACTER APPEARING ON Di $2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0$	STATUS NAME	SET 1 STATE		SET 2 STATE		
		SET	UNSET	SET	UNSET	
- - - 1 1 X X X X	STOPPED 2	Data transfer completed AND peripheral may accept and implement an appropriate control order immediately.	Any Group 2 code with T or causative condition ends.	(Group2 code).T if previously in SET 1 state.	Causative condition ends.	
- - - 1 X X 1 X X	DATA	Cannot exist		An incident occurs while a control command is being processed which causes data just transferred to be suspect.	Causative condition ends.	
- - - 0 X X X X X	P STATUS ON	Peripheral is inoperable.	Any Group 2 code with T or causative condition ends.	(Group 2 code).T if previously in SET 1 state.	Causative condition ends.	

The peripheral must be designed so that any status may be disconnected from the B line if desired.
A processor must wait the maximum peripheral turn around time before resetting status with the strobe.
Changes in state which would result in a status condition must not be allowed to effect this until the condition AC = 11 vanishes.

GENERATION OF STATUS GROUPS.

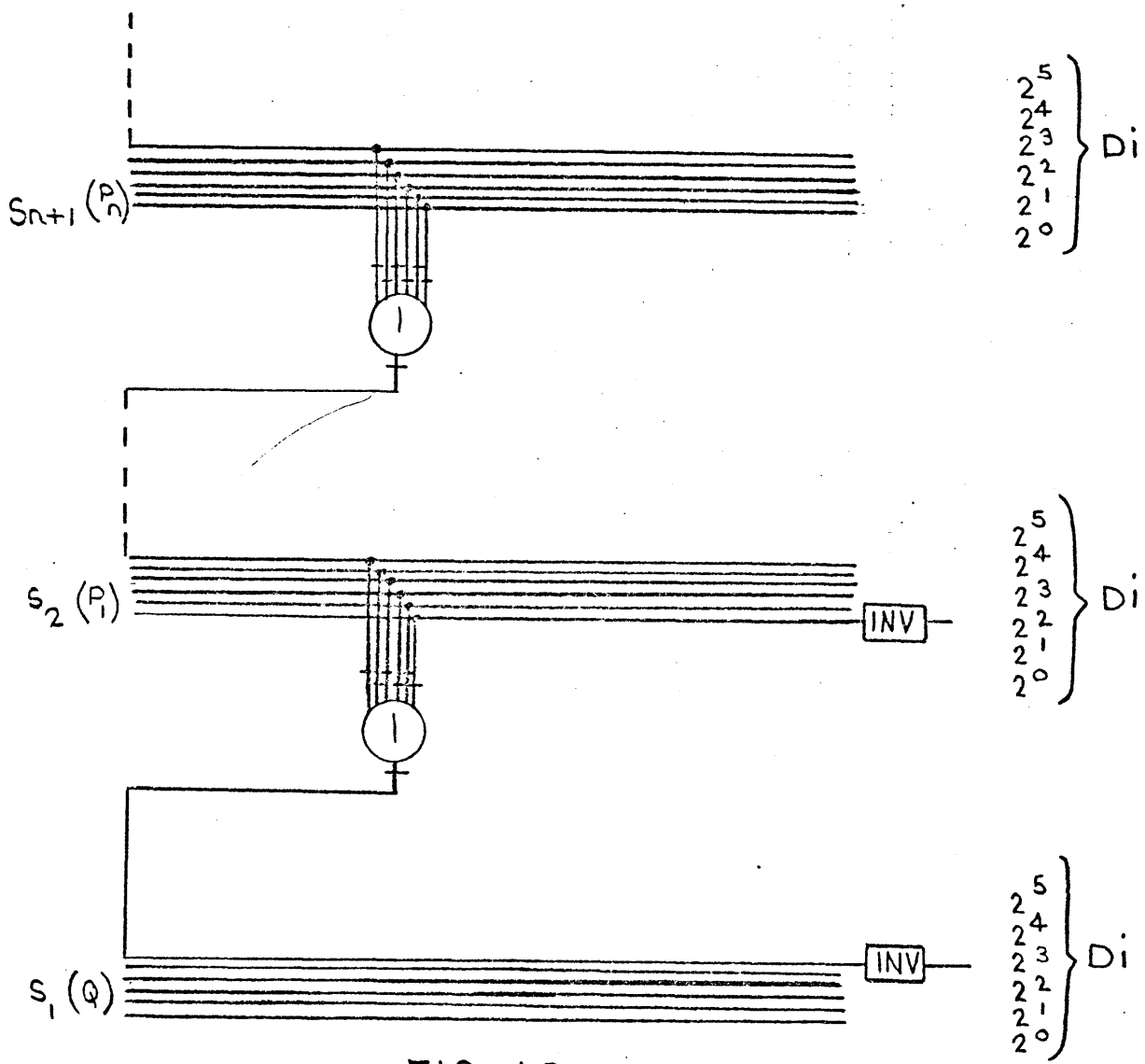

FIG. 4B

At the processor: -
a '0' in $Q2^5$ indicates a P status is on.
a '1' in $P_1 2^5$ indicates a P_{n+1} status is on.
where $n \geqslant 1$

NB. Some status need not set the 2^5 bit (see individual Agreed Specifications).

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Fig. 5. DIRECT RESPONSES

CHARACTER APPEARING ON Di $2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0$	STATUS NAME	TYPICAL CONDITIONS WHICH SET THE STATUS
*- - - X X X X X 0	INOPERABLE	Peripheral inoperable. The control character cannot be accepted until the operator or engineer has removed the condition.
- - - X X X 0 1 1	REJECTED	Peripheral too busy to accept the control character, but in the normal course of events will be able to do so later.
- - - X X X 1 0 1	ACCEPTED	Peripheral will accept the control character and will initiate it when able to do so.

* The 2^0 bit is inverted for transmission.

No additional status will be assigned to the 2^2, 2^1 and 2^0 bits of the response character

The symbol X in the bit position of the character on Di indicates that these bits have no significance in determining the state of the assigned status.

Provision for direct responses will be optional for 'reduced facility peripherals' but will be mandatory for all others. Reference to the individual peripheral agreed specification must be made to determine into which category a peripheral falls.

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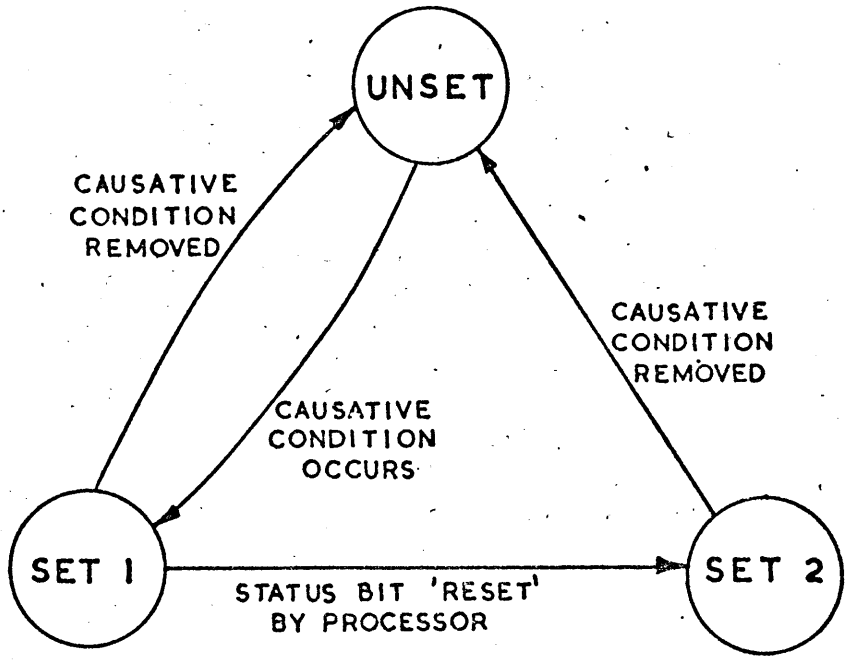
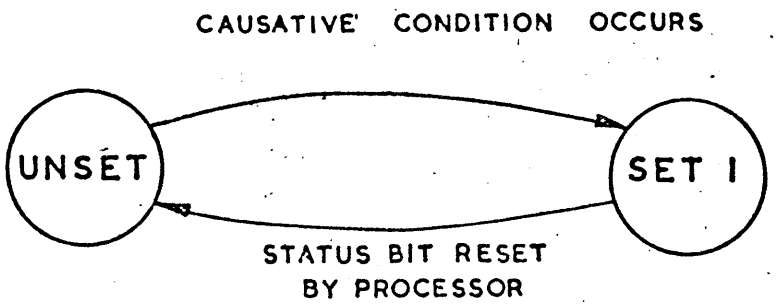
STATE DIAGRAM

Fig. 6

3-STATE STATUSES



2-STATE STATUSES



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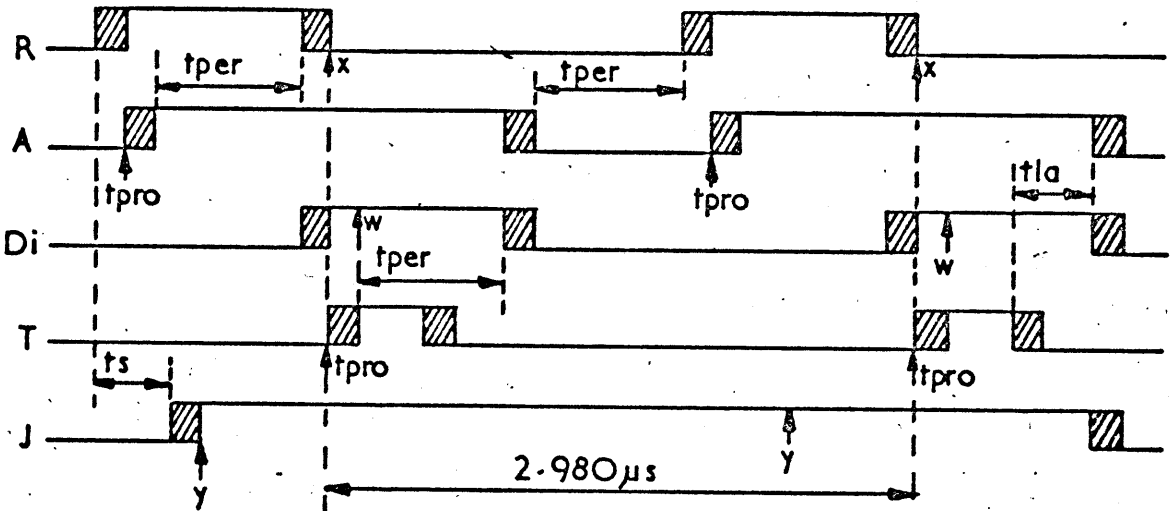
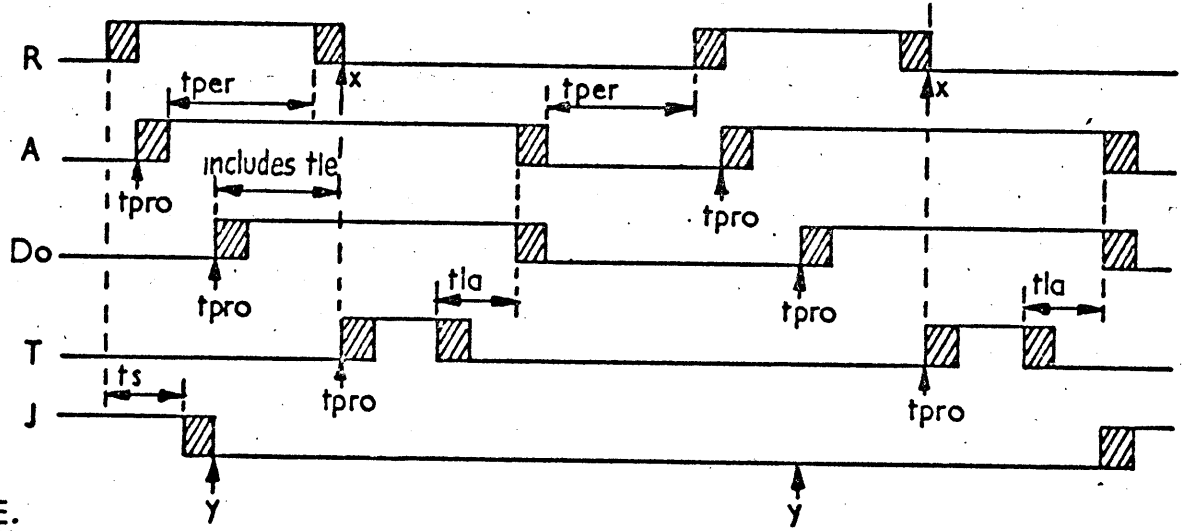
READING



WRITING



SCALE.

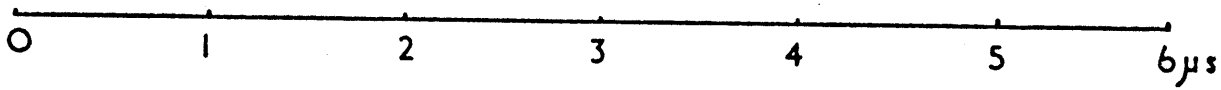


FIG. 7 (See explanatory note over.)

Note on Fig.7.

SIGNAL SEQUENCE WHEN 'R' DUCKS

The illustration shows a Type 1 peripheral timing diagram and assumes a 150ns cable delay (shaded area). Processor turn around times must be added where shown to obtain the true data rate. The maximum peripheral turn around time has been assumed and a 'T' pulse of 480ns.

tper - peripheral turn around time 0 - 750ns

tpro - processor turn around time (assumed zero in these timing diagrams).

ts - time from leading edge of 'R' before 'J' may be examined. 400ns.

tle - leading edge skew 400ns.

tla - trailing edge skew 400ns.

w - 'Di' may change any time after this point

x - 'R' may be examined at processor

NB. 'T' must not be given before this point if processor wishes to check the validity of 'R', but must wait to see if 'R' is going to duck. If 'R' ducks as a result of 'A', processor knows a single character mode transfer is required. If 'R' ducks as a result of 'T', processor knows that penultimate character in a burst mode transfer has been strobed. The position of X assumes a 150ns cable delay.

y - 'J' may be examined at the processor.

'J' may be a fixed level for a unidirectional peripheral.

'J' may change for each character for a bidirectional peripheral

MAXIMUM CHARACTER RATE

(Limiting case excluding processor turn around time).

READING = 336kch/s

WRITING = 336kch/s

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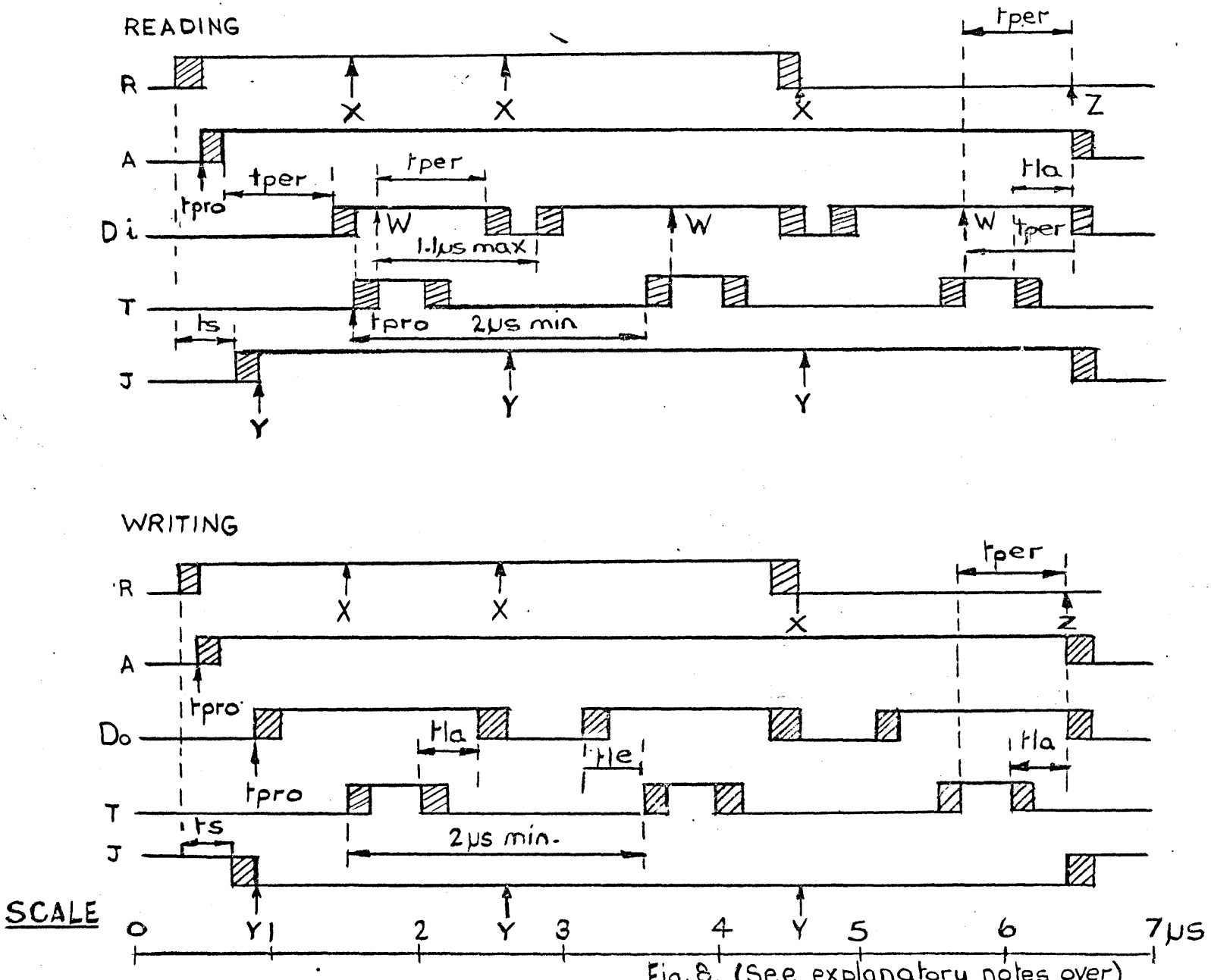

Fig. 8. (See explanatory notes over)

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Note on Fig.8.

SIGNAL SEQUENCE WHEN 'R' DOES NOT DUCK AND 'T' PULSE IS 480ns

The illustration shows a Type 1 peripheral timing diagram and assumes a 150ns cable delay (shaded area). Processor turn around times must be added where shown to obtain the true data rate. The maximum peripheral turn around time has been assumed.
When reading, 'R' does not duck if a new data character can be placed on 'Di' in 1.1us after the leading edge of 'T' unless it is the penultimate character (see 5-2-2-1).
When writing, 'R' does not duck if a character can be accepted from 'Do' in the minimum permitted time after the leading edge of 'T' (see 5-2-2-2).
The minimum interval between the leading edges of successive 'T' pulses is 2us (see 5-2-1).

tper - peripheral turn around time 0 - 750ns.

tpro - processor turn around time (assumed zero in these timing diagrams.)

ts - time from leading edge of 'R' before 'J' may be examined 400ns.

tle - leading edge skew 400ns
NB. the data character on 'Do' must be steady at least tle before the 'T' pulse is sent.

tla - trailing edge skew 400ns.

w - 'Di' may change any time after this point.

x - 'R' may be examined at the processor
NB: 'T' must not be given before this point if processor wishes to check validity of 'R', but must wait to see if 'R' is going to duck. If 'R' ducks as a result of 'A' processor knows a single character mode transfer is required. If 'R' ducks as a result of 'T', processor knows that penultimate character in a burst mode transfer has been strobed. The position of X assumes a 150ns cable delay.

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Y - 'J' may be examined at the processor.

Z - 'R' unsets and 'J' ceases to be valid.

MAXIMUM CHARACTER RATE

READING = 500kch/s (with an allowance of 600ns for processor turn around time.)

WRITING = 500kch/s (with an allowance of 700ns for processor turn around time.)

This diagram is subject to the comment in 5-2-2-3.

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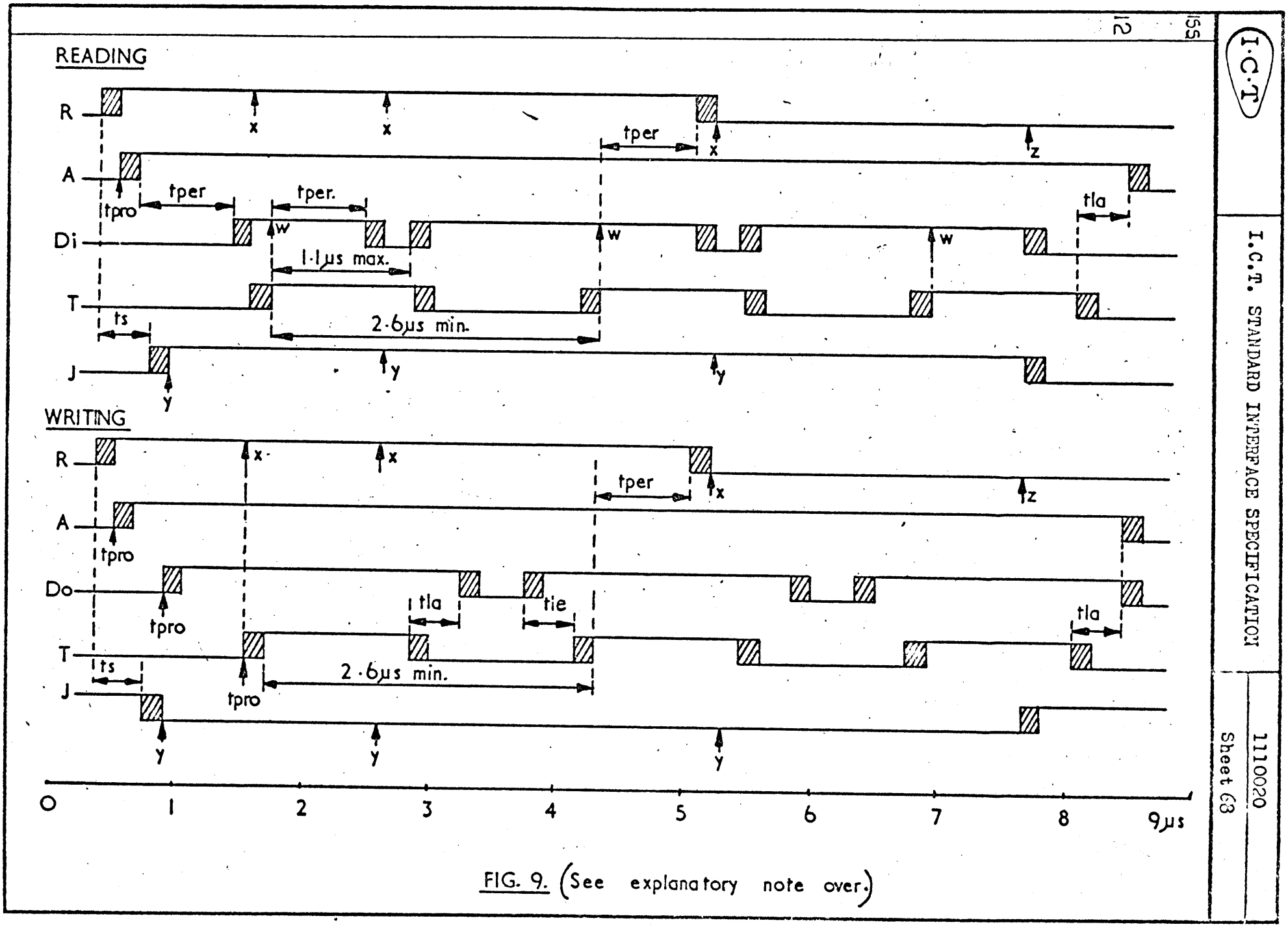

FIG. 9. (See explanatory note over.)

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Note on Fig.9.

SIGNAL SEQUENCE WHEN 'R' DOES NOT DUCK AND 'T' PULSE IS 1-3us.

The illustration shows a Type 1 peripheral timing diagram and assumes a 150ns cable delay (shaded area). Processor turn around times must be added where shown to obtain the true data rate. The maximum peripheral turn around time has been assumed.

When reading,'R' does not duck if a new data character can be placed on Di in 1.1us. after the leading edge of 'T' unless it is the penultimate character (see 5-2-2-1).

When writing, 'R' does not duck if a character can be accepted from 'Do' in the minimum permitted time after the leading edge of 'T' (see 5-2-2-2).

The minimum interval between the leading edges of successive 'T' pulses is 2.6us (see 5-2-1).

tper - peripheral turn around time 0 - 750ns.

tpro - processor turn around time (assumed zero in these timing diagrams).

ts - time from leading edge of 'R' before 'J' may be examined 400ns.

tle - leading edge skew 400ns.
NB. the data character on 'Do' must be steady at least tle before the 'T' pulse is sent.

tla - trailing edge skew 400ns.

w - 'Di' may change any time after this point

x - 'R' may be examined at the processor
NB. 'T' must not be given before this point if processor wishes to check validity of 'R', but must wait to see if 'R' is going to duck. If 'R' ducks, as a result of 'A', processor knows a single character mode transfer is required. If 'R' ducks as a result of 'T', processor knows that penultimate character in a burst mode transfer has been strobed. The position of X assumes a 150ns cable delay.

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Y - 'J' may be examined at the processor.

Z - 'R' unsets and 'J' ceases to be valid.

'J' may be fixed level for a unidirectional peripheral

'J' may change for each character for a bidirectional peripheral

MAXIMUM CHARACTER RATE

READING = 385 kch/s

WRITING = 385 kch/s

This diagram is subject to the comment in 5-2-2-3.

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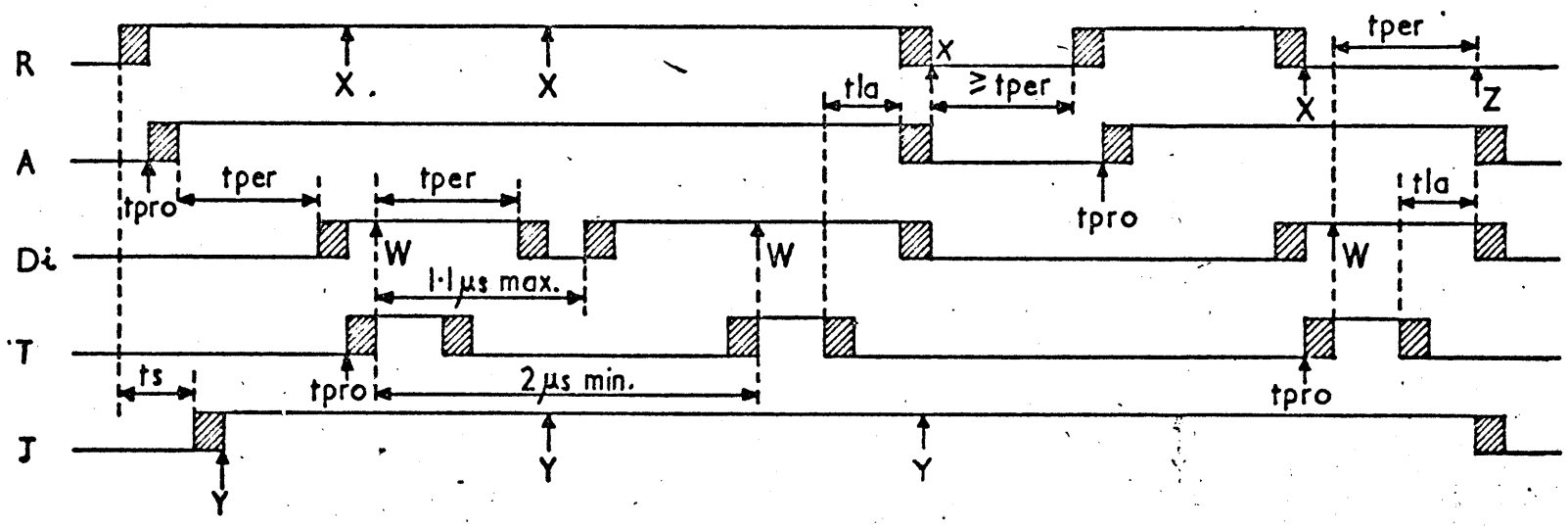
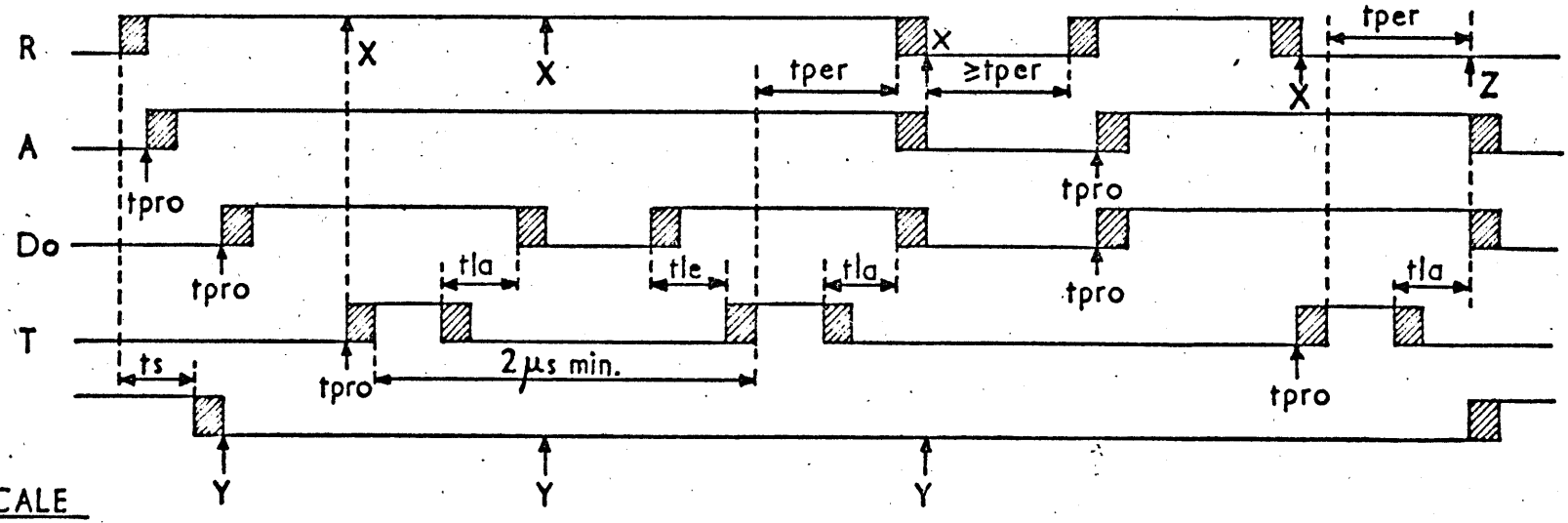
READING



WRITING



SCALE

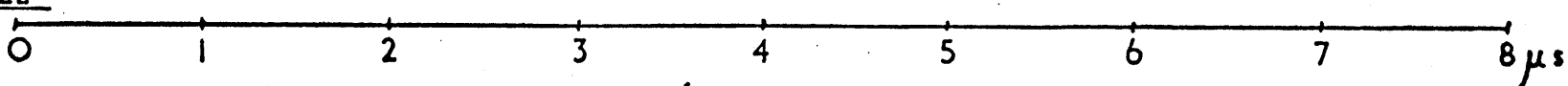


FIG. 10. (see explanatory note over.)

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Note on Fig.10.

SIGNAL SEQUENCE WHEN 'A' DUCKS AFTER THE PENULTIMATE CHARACTER DURING A BURST MODE TRANSFER (480ns 'T' PULSE)

The illustration shows a Type 1 peripheral timing diagram and assumes a 150ns cable delay (shaded area). Processor turn around times must be added where shown to obtain the true data rate. The maximum peripheral turn around time has been assumed.

tper - peripheral turn around time 0 - 750ns.
tpro - processor turn around time (assumed zero)
ts - time from lead edge of 'R' before 'J' may be examined 400ns.
tle - leading edge skew 400ns.
tla - trailing edge skew 400ns.
w - 'Di' may change any time after this point
x - 'R' may be examined at the processor
z - 'R' unsets and 'J' ceases to be valid

READING

'R' ducks tper after the landing edge of the 'T' pulse strobing the penultimate character while 'A' ducks tla after the trailing edge of 'T'. The last character is now transferred according to the normal timing rules.

WRITING

If peripheral requires three data characters it will duck 'R' as in Fig.9. If 'A' also ducks at this point, it will return to logic '1' at the earliest point and the last transfer occurs in the normal way.

'J' may be a fixed level for a unidirectional peripheral
'J' may change for each character for a bidirectional peripheral.

This diagram is subject to the comment in 5-2-2-3.

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11-0 DIRECT DATA EXCHANGE

When two computers are connected together via the I.C.T. Standard Interface for the purpose of data exchange, one of the computers may be regarded as a peripheral of the other, and will have a peripheral type of interface as defined in the main body of specification 1110020. This section assumes such an arrangement and further defines (in the manner of a peripheral specification) the specific function of the lines, the valid control codes, status and other conventions to be adopted for the purpose of data exchange.

11-1 Definition

11-1-1 DATA EXCHANGE is defined in general terms as a method of imparting information contained within one data processing system to another data processing system.
This specification describes a restricted type of data exchange where the cable length is limited to 100ft. and no change or modification of the data format occurs during the transmission.
This form of data exchange will be called DIRECT DATA EXCHANGE.
Where the distance between two data processing systems exceeds 100ft., data exchange will be achieved by other methods, including DATA TRANSMISSION, which may involve a change in the data format using extra intervening equipment.
This arrangement will subsequently be specified.
What follows is applicable only to DIRECT DATA EXCHANGE.

11-1-2 The unit of transmission shall be a character of up to 8 bits plus an optional odd parity bit. The exchange of data shall take place one character at a time and the rules governing initiation, transfer and termination of a block of data characters between the computers shall be according to sections 1 to 9.

11-1-3 One of the two connected computers shall have a peripheral type terminal, which is the interface defined at 'X' in Fig. 1.

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11-2 Initiation

11-2-1 Either of the two computers may initiate a data transfer.

11-2-2 For convenience, the computer with the peripheral type of interface will be referred to as the 'peripheral', and the other computer the 'processor'

11-2-3 The processor may initiate a data transfer to the peripheral by sending the command, 'WRITE'. Data will be transferred using the R request signals given by the peripheral.

11-2-4 The peripheral may initiate a data transfer to the processor by using the 'B interrupt line, to which the processor must respond with 'SEND STATUS Q'.
The peripheral will indicate with the 2^2 Q status bit 'READY' that it wishes to send data.
'READY' is interpreted as "enquiry". The processor must follow with a 'READ' command and data will be transferred using the R request signals given by the peripheral.

11-2-5 / During the preliminary data transfer phase initiated by either side, information will be transmitted appertaining to the main data transfers required. This information will, by convention, comply to an agreed format which will be specified later. It is essential that symmetry is achieved at the lowest level at which program compatibility exists between two computers.

11-3 Control Commands (originated by processor).

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11-3-1 The meaningful control commands which may be given by the processor are:-

		2^5 2^0
'READ'	Control Code	0 1 1 0 0 1
'WRITE'	Control Code	0 1 1 0 1 0
'SEND STATUS Q'	Control Code	0 1 0 0 0 0

11-3-2 Peripheral response to 'READ'or 'WRITE'.
The peripheral will give the following direct responses on Di within 750 n sec of the command being received.

11-3-3 The direct response codes are as follows:

'ACCEPTED'	X X X 1 0 1
'REJECTED'	X X X 0 1 1
'INOPERABLE'	X X X X X 0

11-3-4 The direct response to a 'WRITE' order will be 'ACCEPTED' if 'STOPPED' and not 'READY', otherwise it will be 'REJECTED'. If order is rejected, because 'STOPPED' is not set but 'TERMINATED' is set, the peripheral will cause an internal program interrupt to be generated and prepare to become 'STOPPED'.

11-3-5 / The direct response to a 'READ' order will be 'ACCEPTED' if 'STOPPED' and 'READY', otherwise it will be 'REJECTED'.

11-3-6 The direct response to all commands will be 'INOPERABLE' if the peripheral is inoperable for any reason.

11-3-7 Peripheral response to 'SEND STATUS Q'.
The peripheral will respond within 750 n sec as follows:

	STATE OF PERIPHERAL	Q STATUS CHARACTER 2^5 2^0
(i)	INOPERABLE	0 X X X X X
(ii)	BUSY, OPERABLE	1 X X X X X
(iii)	STOPPED	1 1 1 X X X
(iv)	READY (Enquiry)	1 X X 1 X X
(v)	TERMINATED	1 X X X X 1

11-3-8 Other Control Commands.

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11-3-9 There are no P status conditions specified except 'INOPERABLE', therefore the 2^5 escape bit of the Q status will normally be true indicating no P status present.
If the escape bit becomes false, indicating P status present, a 'SEND STATUS P' request will provoke the correct response, i.e. 0 0 0 0 0 0 'INOPERABLE'.
If a P status request is given when the escape bit is true the P status response will be invalid.

11-3-10 The peripheral response to all other commands is not defined and will be indeterminate.

11-3-11 If the processor continuously sends 'READ' or 'WRITE' following a 'REJECTED' response, the peripheral will, when prepared, accept the control command but will hold back the change in the response from 'REJECTED' to 'ACCEPTED' until A C = 0 0. Further, whilst A C = 1 1, the B interrupt which would normally arise with the 'STOPPED' status will be suppressed.

11-4 Interrupts (originated by peripheral)

11-4-1 A B interrupt will be given by the peripheral when any of 11-3-7 (iii)(iv) or (v) status arise.

/ As mentioned in 11-2-4, the peripheral may initiate data exchange, and will do so by using the 'READY' Q status bit 2^2 as an "enquiry" status. The 'STOPPED 1' and 'STOPPED 2' status are always given if the peripheral is able to accept a control command. This is the case in 11-3-7 (iii)(iv) and (v).
The B interrupt will cease when T is given during 'SEND STATUS Q', following the rules given in para 7-0.

11-5 Status

			2^5 ... 2^0
11-5-1	'INOPERABLE'	P status	X X X X X 0
		Q status	0 X X X X X

Either the 2^5 (escape) bit of the Q status, or the 2^0 bit of the P status will, if false, indicate the inoperable state of the peripheral. There are no other P status conditions.

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11-5-2 'BUSY, OPERABLE Q STATUS 1 0 0 0 0 0

The peripheral is operable, but cannot accept a control command, either because it is busy obeying a previously given command, or is engaged with another program. If any command is attempted during this condition, i.e. A C = 1 1 Do = X X X X X X, the peripheral will reject it. See 11-3-2 regarding 'READ' and 'WRITE' orders; in particular the conditions under which a peripheral program interrupt is caused.

11-5-3 'STOPPED' Q status 1 1 1 X X X

The peripheral is able to accept a valid control command and implement it immediately.

This status would normally occur when initially starting, or when the peripheral places the interface in the prepared state for data exchange.

If 'TERMINATED' is not present there has not been a data transfer immediately prior to the condition arising.

A B interrupt is given.

11-5-4 'READY' (Enquiry) Q status 1 X X 1 X X

The peripheral generates this status when it wishes to initiate data exchange. A B interrupt is given.

The processor must acknowledge this status condition by giving a 'READ' control command, thus enabling the peripheral to transfer the message in the ensuing data flow. As mentioned in 11-2-5, and agreed convention regarding the format of the enquiry message will later be specified.

11-5-5 'TERMINATED' Q status 1 X X X X 1

On completion of data transfer, this status will be given with a B interrupt. The data transfer may be ended by either the processor giving an L signal, or internally by the peripheral. The 'TERMINATED' status will arise in either case.

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11-5-6 Unsetting

The B interrupt will be unset in the usual way when 'T' is given with 'SEND STATUS Q'. The 'STOPPED' status will unset either when the peripheral state changes to 'BUSY' due to internal operations, or when a 'READ' or 'WRITE' command is given.
The 'READY' status will unset when a 'READ' command is given.
The 'TERMINATED' status will unset either when a 'READ' or 'WRITE' command is given, or when 'SEND STATUS Q' is given with T = 1.
Refer also to 11-8-3.

11-5-7 The peripheral may also give a 'READY' status with 11-5-5, in the case where it has a message to transfer applicable to the data just received (e.g. a parity error detected), to which the processor will respond in the normal way with a 'READ' order to enable the message to be transferred. See 11-7.

11-6 Termination

Termination of a block of data may evolve from either processor or peripheral.

11-6-1 Processor

The processor will raise the L line with either A C = 1 0 during data, or A C = 1 1 between data characters.
The peripheral will lower the R line, complete the transfer if a data character is present when L is given and raise the B line, responding to a 'SEND STATUS Q' request from the processor as shown in 11-3-7 (v).

11-6-2 Peripheral

The peripheral will lower the R line, raise the B line and respond to a 'SEND STATUS Q' request from the processor as shown in 11-3-7.

11-7 Parity Checks

11-7-1 Where processors are provided with data checking hardware, errors detected in characters transferred across the interface with a parity bit will be dealt with in the following manner.

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11-7-2 If the error is detected by the peripheral, the data flow will be terminated. The status will be 'TERMINATED', 'STOPPED' and 'READY', indicating to the processor that a 'READ' order is required so that the peripheral may transfer a message applicable to the data transfer which has just occurred.

11-7-3 If the error is detected by the processor, the latter will give a 'G' reset followed by a 'WRITE' command, transferring a message applicable to the data transfer in a similar manner to 11-7-2. The peripheral action following a 'G' reset is detailed in 11-8-3.

11-8 Other Interface Lines

11-8-1 Direction of transfer

The peripheral should indicate the direction of data transfer with the 'J' line in conjunction with 'R'.

11-8-2 Hi - Ho

The peripheral shall provide an Hi line as defined in 3-13. A manual control will be provided which will open circuit Hi and cause the peripheral to assume that Ho is also open circuit. The control is necessary to allow an operator to disconnect the data exchange link when required.
Ho will be provided by the processor as defined in 3-14.

11-8-3 G

The processor will provide a G line as defined in 3-15
The peripheral will implement the following when G is true.

(i) Forget any stored information concerning previously given commands.

(ii) If inoperable , display the 'INOPERABLE' status (see 11-3-7 (i)).

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11-8-4 Z

Z lines will be provided as specified in 8-5-3/4/5.

11-8-5 F

The peripheral will use this line to indicate the relevant timing rules according to 5-2.

11-9 Design

11-9-1 This specification for data exchange does not define the manner in which the foregoing conditions should be implemented, since it is recognized that this is a function of a particular processor design.
However, it must be appreciated that the method of implementation will define the maximum rate at which data exchange takes place.

11-9-2 Whilst the inclusion of certain conditions appertaining to responses to control commands will avoid some 'race' effects (see 11-3-4 and 11-3-5), the designer will have to ensure that if a valid ' WRITE' command given by the processor coincides with a valid 'WRITE' command generated by the peripheral, one or the other will satisfactorily take precedence.

/

* i.e. a 'B' interrupt with 'READY' status at the interface.

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PART II

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FAST DATA TRANSFER FOR TYPE (1B and 2B) PERIPHERALS

PART II OF THIS SPECIFICATION APPLIES ONLY TO THE DATA TRANSFERS OF PERIPHERALS WHICH SET THE 'FAST TRANSFER' (F) LINE TO LOGIC '1'.

CONTROL COMMANDS WILL REMAIN AS SPECIFIED IN THE REVELANT SECTIONS OF PART I OF THIS SPECIFICATION.

12. DEFINITIONS

12.1 A 'Burst' is defined as the transfer of four characters.

12.2 'Burst Mode'

Only one 'Burst' is transferred as the result of a single 'R' line request.

12.3 'Repetitive Burst Mode'

Continuous transfer of more than one 'Burst' can result from a continuous 'R' line request.

For a writing peripheral the transfer of every character can be strobed at the maximum rate of the interface.

For a reading peripheral the transfer of every character must be strobed within ±10% of the 'average' pulse period of the 'S' strobe if successive 'T' strobes arrive within the limits defined in Section (15.9.2.).

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13-0 MODIFIED FUNCTIONS OF LINES ACROSS THE INTERFACE

13.1 'A' - (Peripheral Addressed when F = 0)

Function of the 'A' line during control commands when F = 1:-

The 'A' line is used to address a particular interface as detailed in Section (3.2).

Function of the A line during data transfers when F = 1:-

The 'A' line is not used to address a particular interface but it serves the following function:-

This line is used to obtain advanced information on the ability of a writing peripheral to transfer data in 'Repetitive Burst Mode'.

The 'A' line may be set to logic '1' in response to an 'R' line request, and it may remain in this state while the peripheral is being serviced.

The 'R' line will operate in conjunction with the 'A' line to indicate that 'Repetitive Burst Mode' is possible (See 15.8.4).

Since the 'A' line is not used to address a particular interface there is no significance in the time at which the 'A' line returns to logic '0'.

13.2 'T' - Computer Strobe

This line is used by the processor to control the transfer of data to a writing peripheral.
This line is also used to initiate the transfer of each 'Burst' of four characters from a reading peripheral.
The 'Computer Strobe' must be sent to a particular interface (It must not be sent out on a common bus, since the 'A' line does not address a particular interface during data transfers when F = 1).

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13.3 'S' - Peripheral Strobe

This line is used only by a reading peripheral to control the transfer of a 'Burst' of four characters to the processor when initiated by a 'T' strobe. Every 'Burst' of four 'S' strobes must be generated from one 'T' strobe.
The use of 'S' is mandatory for reading peripherals. No extension of 'S' is permissible.

The physical location of 'S' in the interface cable will be as follows:-

Core A	Pin 65	Orange
Core B	Pin 70	Grey

13.4 'L' - Limit Pulse

This line is used by the processor to terminate the data transfer in progress, but the present 'Burst' of four characters will be completed before termination can take place (see 15.5).

The 'Limit Pulse' must be sent to a particular interface (it must not be sent out on a common bus, since the 'A' line does not address a particular interface during data transfers when F = 1).

13.5 'Di' - Data In

These lines must not be bussed at the processor. (Since the 'A' line does not address a particular interface during data transfers when F = 1).

13.6 'R' - Request Data Transfer

This line is used to indicate the ability of a peripheral to receive or transmit a 'Burst' of four characters.

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14.0 MODE OF OPERATION

14.1 The peripheral will be given a READ/WRITE control command (i.e., C = 1) according to the relevant sections of PART I of this specification.

14.2 Writing Data

After a writing peripheral has been given a WRITE command, it will raise its 'R' line to Logic '1', when it is ready to indicate its ability to accept a 'Burst' of four characters. Data transfers will then take place under the control of the computer strobe 'T'.

14.3 Reading Data

After a reading peripheral has been given a READ command it will raise its 'R' line to Logic '1', when it is ready to indicate its ability to transmit a 'Burst' of four characters. The processor will send one 'T' strobe when it is in a position to accept this burst of characters. The data transfers will then take place under the control of the peripheral strobe 'S'.

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15.0 TIMING RULES

The timing rules for the interface are defined at the plug and socket at the peripheral boundary. For this purpose any connecting cables and propogation delays arising therefrom are regarded as part of the processor.

15.1 Leading edge skew of the Strobes:

15.1.1 Leading edge skew of 'T'

The 'Do' lines must be steady for a specified time before the leading edge of 'T'.

Minimum 115 nS
No Maximum

15.1.2 Leading edge skew of 'S'

The 'Di' lines must be steady for a specified time before the leading edge of 'S'.

Minimum 115 nS

15.2 Strobes

15.2.1 The 'T' strobe will be of a specified duration.

Minimum 100 nS
Maximum 1 uS

15.2.2 The 'S' strobe will be of a specified duration

Minimum 100 nS

15.3 Data Hold

15.3.1 The 'Do' lines must remain steady for a specified time after the leading edge of 'T'.

Minimum 80 nS
No Maximum

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15.3.2 The 'Di' lines must remain steady for a specified time after the leading edge of 'S'.

Minimum 80 nS

15.4 Gap between 'T' strobes

The gap is the time between the lagging edge of one strobe to the leading edge of the next strobe.

Minimum 100 nS
No Maximum

15.4.1 Gap between 'S' strobes

Minimum 100 nS

15.5 'L' - Limit Pulse

The duration of the 'L' pulse will be:-

Minimum 100 nS
No Maximum

The 'Limit Pulse' is used to terminate a data transfer at the end of a 'BURST'. In order to terminate after a particular 'BURST' the leading edge of the 'Limit Pulse' must arrive within the following limits:-

A maximum of 100 nS before the leading edge of either the first 'T' strobe of the present 'Burst' to a writing peripheral, or the initiating 'T' strobe of the present 'Burst' to a reading peripheral.

A maximum of 500 nS after the leading edge of either the first 'T' strobe of the present 'Burst' to a writing peripheral, or the initiating 'T' strobe of the present 'Burst' to a reading peripheral.

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15.6 'Di' - Data In

The 'Di' lines must be steady within a specified time of the Control line (C) changing from Logic '1' to Logic '0'.

No Minimum
Maximum 200 nS

15.7 'C' - Control Line

During data transfers the control line must be held at logic '0' within the specified limits.

A minimum of 115 nS before the leading edge of 'T'.

A minimum of 115 nS after the lagging edge of 'T'.

15.8 Operation of the 'R' Line

15.8.1 The 'R' line must be unset within 200 nS (maximum) of the leading edge of the 'Limit Pulse'.

15.8.2 The 'J' line must be steady for a specified time befcre raising the 'R' line.

Minimum 115 nS
No Maximum

The 'J' line must remain steady until the 'R' line unsets.

15.8.3 Operation of the R line for a Reading Peripheral

The 'R' line will be unset within 200 nS (maximum) of the first 'S' strobe of a 'Burst', unless a further 'Burst' can be transferred in 'Repetitive Burst Mode'.

The 'R' line may be set again at any time during a 'Burst' if the peripheral subsequently becomes ready to transmit a further 'Burst'.

The 'average' repetition frequency of the 'S' strobe will not be less than 2 Mc/s.
In 'Burst Mode' or 'Repetitive Burst Mode' the transfer of every character must be strobed within ±10% of the 'average' pulse period of the 'S' strobe.

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15.8.4 Operation of the 'R' line for a Writing Peripheral

'Burst Mode':-

The 'R' line will duck within 200 nS (maximum) of the 'A' line becoming logic 1 unless a further 'Burst(s)' can be transferred in 'Repetitive Burst Mode'.

'Repetitive Burst Mode' :-

It is necessary to obtain advanced information on the ability of a writing peripheral to operate in 'Repetitive Burst Mode':-

The 'R' line will not duck as a result of 'A' becoming logic 1, but it will duck within 200 nS (maximum) of the leading edge of the second 'T' strobe of the penultimate 'Burst'.

If 'R' is ducked, and the processor subsequently ceases to service the peripheral, then the 'R' line must return to logic '1' within 200 nS (maximum) of the 'A' line going to logic '0'.

The 'R' line will unset within 200 nS (maximum) of the leading edge of the first 'T' strobe of the ultimate 'Burst'.

The 'R' line may be set again at any time during the ultimate 'Burst' if the peripheral subsequently becomes ready to accept a further 'Burst'.

15.9 Operation of a Reading Peripheral

15.9.1 'Burst Mode'

When the 'Burst' has been initiated by a 'T' strobe, the leading edge of the first 'S' strobe must occur within the limits given by the later of the two following conditions:-

1) 200 nS (maximum) after the leading edge of the initiating 'T' strobe.
2) 500 nS (maximum) after the 'R' line has been set to logic '1'.

See Fig.I.

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15.9.2 'Repetitive Burst Mode'

When the first 'Burst' has been initiated by a 'T' strobe, the leading edge of the first 'S' strobe of the first 'Burst' must occur within the limits given by the later of the two following conditions:-

1) 200 nS (maximum) after the leading edge of the initiating 'T' strobe.
2) 500 nS (maximum) after the 'R' line has been set to logic '1'.

See Fig.1.

If the 'R' line has not been unset, then to initiate a further 'Burst' the peripheral must be able to accept a further 'T' strobe after the second 'S' strobe of the present burst. 'Repetitive Burst Mode' operation must be achieved if the leading edge of the 'T' strobe arrives not later than the leading edge of the last 'S' strobe of the present 'Burst'.

15.10 Operation of a Writing Peripheral

15.10.1 'Burst Mode'

The leading edge of the first 'T' strobe of the 'Burst' will not occur earlier than 100 nS after the 'R' line has been set to logic '1'.

15.10.2 'Repetitive Burst Mode'

The leading edge of the first 'T' strobe of the first 'Burst' will not occur earlier than 100 nS after the 'R' line has been set to logic '1'.

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16.0 GENERAL NOTE

If control commands occur during a data transfer, the maximum data transfer rate will be greatly reduced. Consequently the practice of sending control commands during a data transfer should be avoided wherever possible.

Consideration should therefore be given to inhibiting 'B' interrupts from other mechanisms of a multi-mechanism peripheral during data transfers.

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17.0 GUIDE TO PART 1 OF THIS SPECIFICATION WHEN F = 1

The previous sections of this Specification which are not applicable, or need modification for type 1B and 2B peripherals, are detailed below. The remaining sections are valid.

Section	Comments
1.1	Only type 1B and 2B peripherals are defined.
2.1	There is an additional line 'S' from peripheral to processor (see 13.3).
2.2	Ni - Not applicable.
3.2	Not applicable without modification (See 13.1).
3.3	Not applicable without modification (See 13.2)
3.5	Section (ii) not applicable
3.6	Not applicable without modification (See 13.4)
3.8	Not applicable without modification (See 13.6)
3.11	Not applicable
3.17	Applicable with respect to Control Identifiers only
4.1	Only applicable when C = 1
4.2	Not applicable
4.3	Not applicable
4.7	Not applicable
5.1.1 - 5.2.1	Only applicable when C = 1
5.2.2. - 5.2.6	Not applicable
6.4	Not applicable
9.4.1	There is an additional line 'S' (see 13.3)
10. - 10.5	Not applicable
Fig.1	There is an additional line 'S' (see 13.3)
Fig.2	Sections (a) to (h) not applicable
Fig.7 - Fig. 10	Not applicable
11.6.1	Not applicable without modification (see 13.4).

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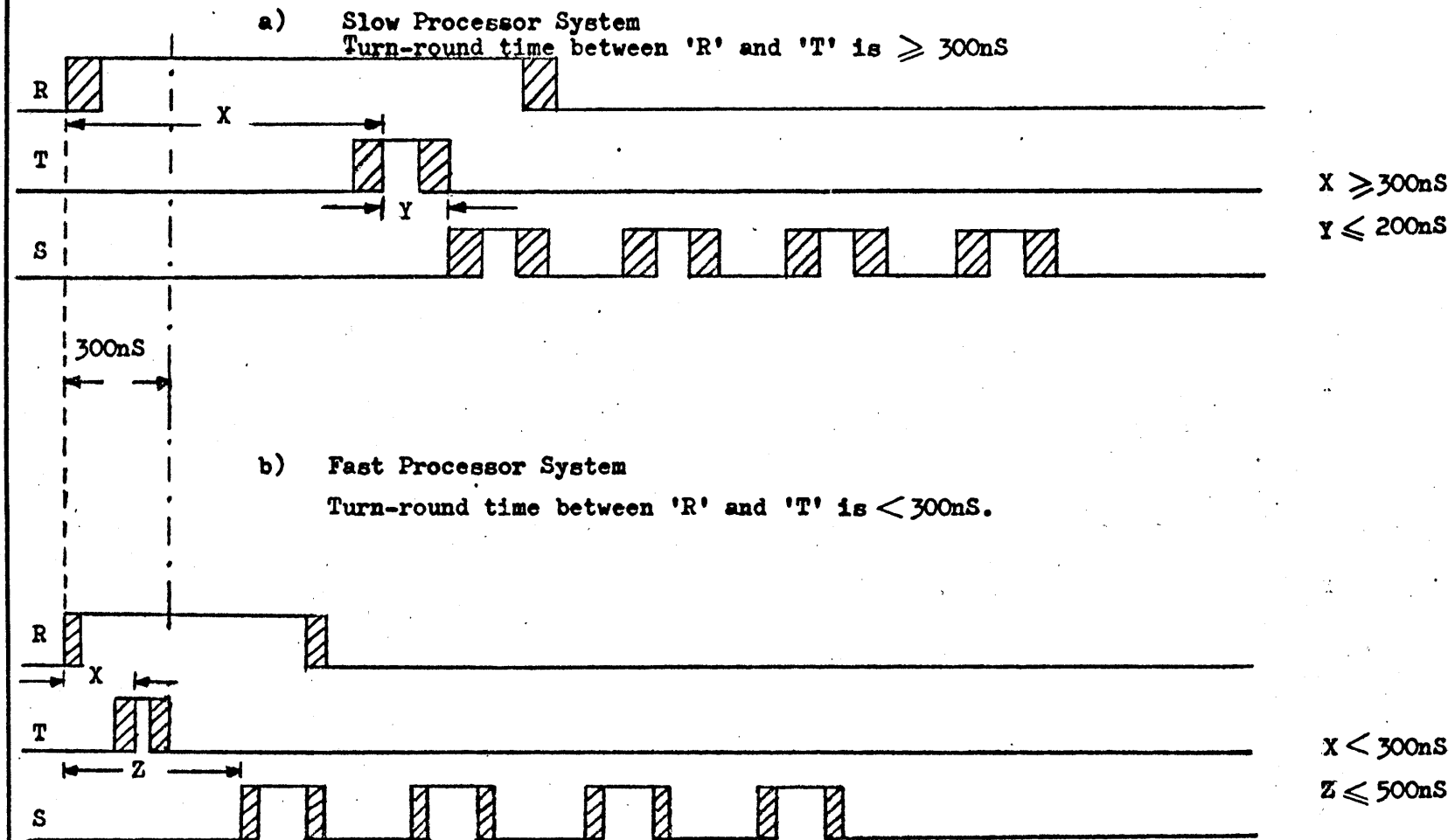
FIG I

INITIATION OF A 'BURST' MODE' READING PERIPHERAL



NOTE: Case a) will normally be applicable, but if a fast processor is connected on a reduced length of cable then the peripheral can delay the arrival of the first 'S' strobe such that it arrives later than 200nS after the 'T' strobe, (see Case b). This extra time can be used by the peripheral to ensure compliance with the requirements of data skew as specified in Section 15.1.2.

SCALE: 0.2 INS = 100 nS

SHADED AREAS = CABLE DELAY

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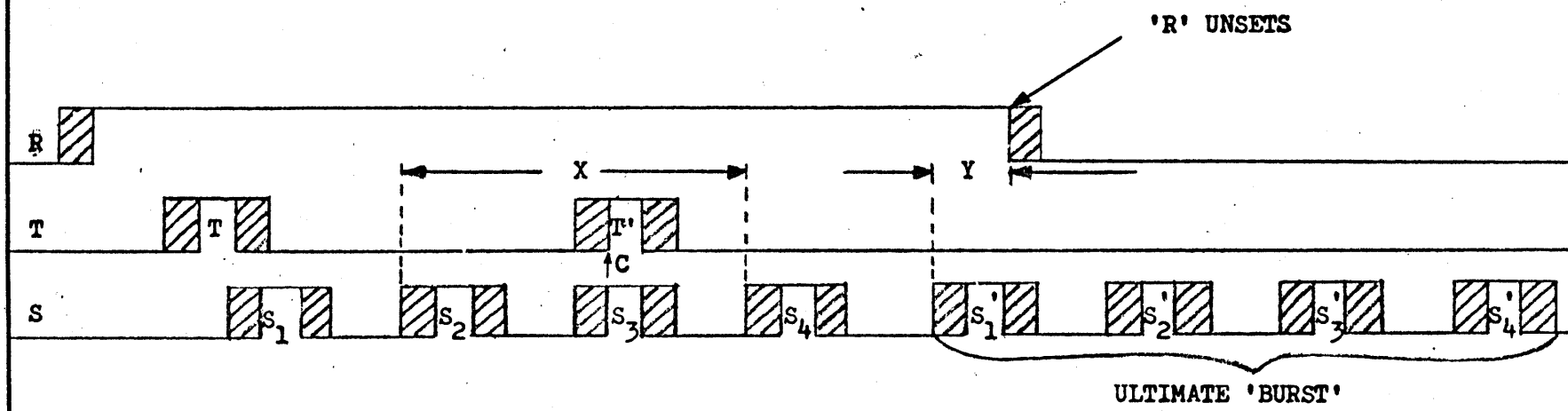
FIG II

READING PERIPHERAL ENDS A 'REPETITIVE BURST MODE' TRANSFER



NOTE:

1) The leading edge of 'T' (C) must arrive within the limits of 'X' if 'Repetitive Burst Mode' is to be achieved.
2) Y $\leqslant$ 200 nS.
3) Every character must be strobed within $\pm$10% of the average pulse period of the 'S' strobe.

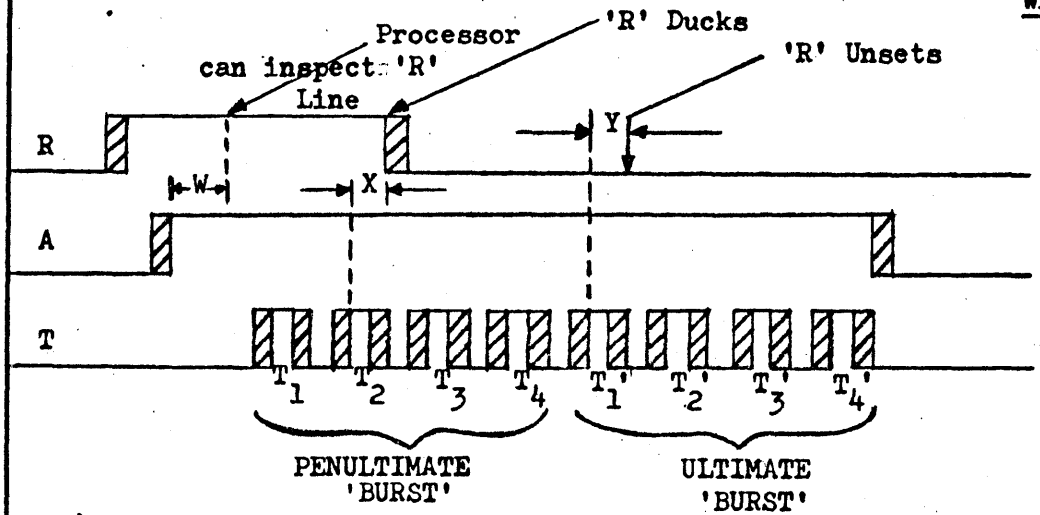
SCALE 0.2 ins. = 100nS

SHADED AREAS = CABLE DELAYS

FIG. III

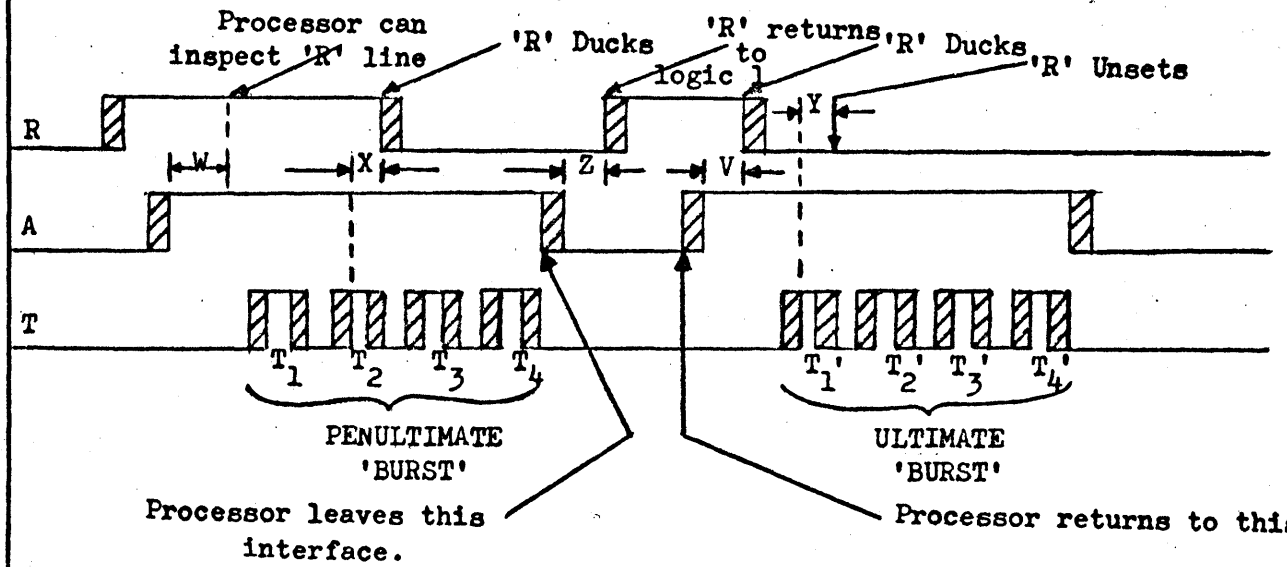
WRITING PERIPHERAL ENDS A 'REPETITIVE BURST MODE' TRANSFER

a) 'A' remains at Logic '1'



Note: 1) 'W' = 200nS + Cable Delay
2) 'X' ≤ 200nS
3) 'Y' ≤ 200nS

b) 'A' reverts to Logic '0'.



Note: 1) 'V' ≤ 200nS
2) 'W' = 200nS + Cable Delay.
3) 'X' ≤ 200nS
4) 'Y' ≤ 200nS
5) 'Z' ≤ 200nS

SCALE 0.1 ins. = 100nS
SHADED AREAS = CABLE DELAYS

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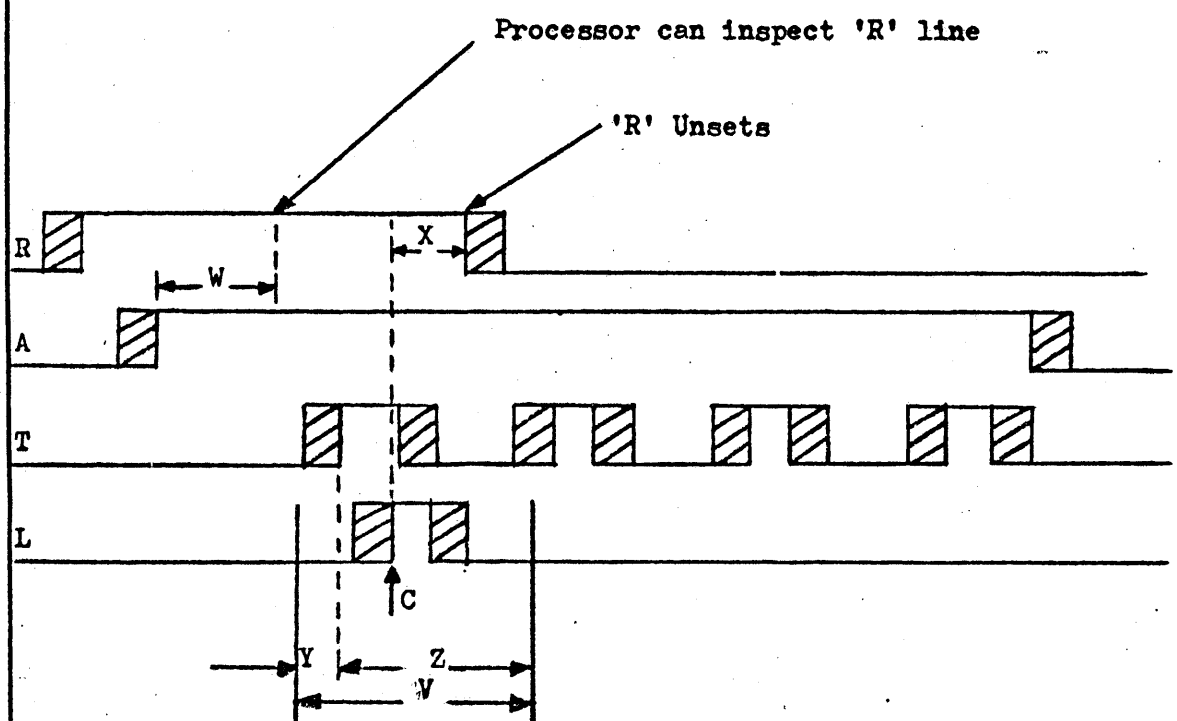
FIG. IV

PROCESSOR TERMINATES THE TRANSFER OF A WRITING PERIPHERAL



Note:

1) 'W' = 200nS + Cable Delay
2) 'X' ⩽ 200nS
3) 'Y' = 100nS
4) 'Z' = 500nS
5) The leading edge of 'L' (C) must arrive within the limits given by 'V' if termination is to occur before a further 'BURST' is requested.
6) The unsetting of 'R' is timed from 'L' not 'T'.

SCALE 0.2 ins. = 100nS

SHADED AREAS = CABLE DELAYS