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Reliability of SiO_2 Gate Dielectric with Semi-Recessed Oxide Isolation

This paper reports the results of a study to minimize defects in the gate oxide and in the single crystal substrate of semi-recessed oxide (Semi-ROX) structures. It is shown that both an increase in oxidation mask thickness and a decrease in wet field oxidation temperature markedly reduce the incidence of low voltage breakdown in the gate oxide. Microscopic studies of samples which exhibited low voltage breakdown showed that the Si_3N_4 oxidation mask had failed to protect the surface of the region in which the gate oxide was grown. Semi-ROX processing also exhibited edge breakdown, most likely due to the Kooi effect (nitrided Si surface). The use of a thicker "pad" oxide and a decrease in the wet field oxide thickness were beneficial in reducing the magnitude of degradation in gate breakdown due to this edge effect.

Introduction

Very large scale integration (VLSI) of circuit components, having linewidths in the micrometer and submicrometer range and yielding chip packing densities of 64K bits, 256K bits, 512K bits, and up, presents severe requirements for some form of isolation. When silicon technology is used, one way in which the isolation of discrete transistors can be achieved is to fabricate integrated circuits (ICs) on a monolithic single crystal of silicon using a combination of p-n junctions, air gaps, and a dielectric insulating material, such as SiO_2. This method of isolation, termed LOCOS (Locally Oxidized Silicon) [1-4] utilizes a patterned Si_3N_4 film as an oxidation barrier to define the active device regions, while a thick film of SiO_2 is thermally grown as the isolation field oxide. The SiO_2 is approximately equally divided above and below the original Si surface, yielding a semi-recessed oxide (Semi-ROX) structure [5]. General advantages of this form of dielectric isolation (DI) are that it minimizes parasitic effects, decreases transistor cell area, and increases performance while reducing cost.

This paper reports an investigation of and efforts to minimize defects in the gate oxide and in the single crystal substrate of Semi-ROX structures. The Semi-ROX isolation process was studied because it is presently used to manufacture high-density polysilicon gate RAM and SAM chips. Specific advantages of this method of DI are:

1. Surface planarity [5].
2. Compatibility with backside ion implantation gettering [6].
3. Ease of processing—one mask level defines both the active and inactive regions, as well as the field ion implantation [1, 6] (used as a "channel stopper").
4. Compatibility with MOSFET and CCD processing in a single isolation process.

Experimental procedures

To study the effects of processing the Semi-ROX isolation layer on the integrity of the active device/gate region, a special mask set was devised to fabricate aluminum gate MOS capacitor test structures. Figure 1 shows a cross-section of these structures, which are similar in concept to those reported by Ohwada, Sakuma, and Ehara [7]. The upper structure in Fig. 1 was designed to investigate isolation edge effects, since the Al electrode overlaps the thick field oxide; the lower structure was designed to investigate only the quality of the thin gate oxide region.

- *Semi-ROX processing*

Table 1 outlines the processing steps used to fabricate the MOS capacitor test structures. Two masking steps are re-

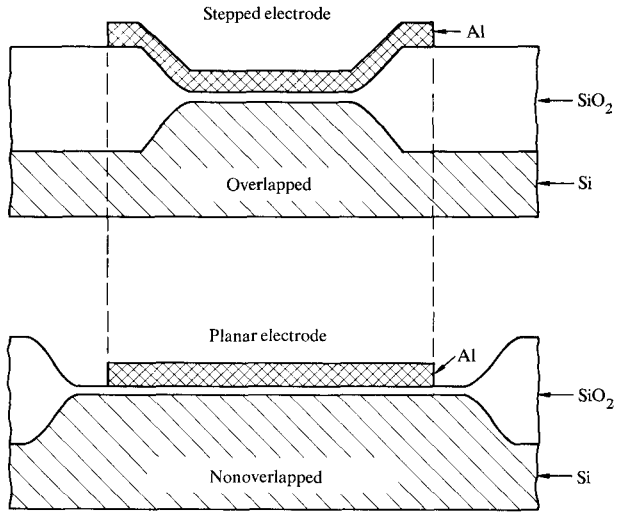

Figure 1 Two types of MOS test structures.

Table 1 Processing steps.

1. Clean wafers
2. Grow SiO_2 pad oxide
3. Deposit Si_3N_4
4. Apply resist (mask 1)
5. Etch Si_3N_4
6. Etch SiO_2 pad/strip resist
7. Clean wafers
8. Grow (DWD) field oxide
9. Strip Si_3N_4
10. Strip SiO_2 pad
11. Clean wafer using modified process
12. Grow SiO_2 gate oxide
13. Deposit Al metal
14. Apply resist (mask 2)
15. Etch Al/strip resist
16. Etch back side
17. Deposit Al back side
18. Anneal with forming gas at 400°C for 20 min

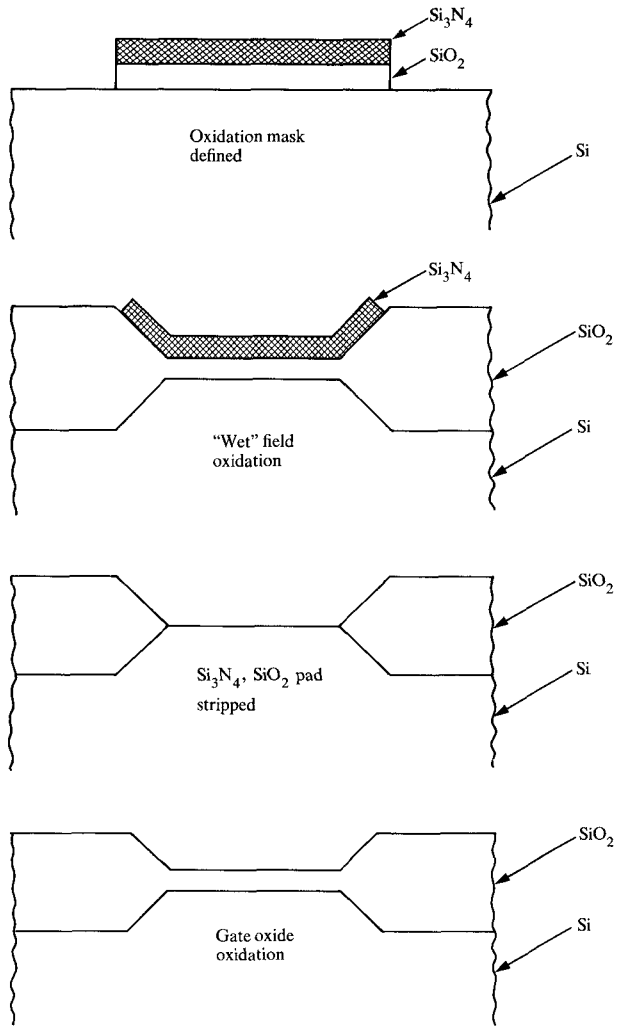

Figure 2 Cross-sectional view of the Semi-ROX process.

quired: The first mask (step 4) defines the nitride oxidation mask (barrier), which in turn defines the Semi-ROX structures, as shown in Fig. 2; the second mask (step 14) delineates the metal electrode patterns shown in Fig. 1.

The starting wafers consisted of high-quality, 57-mm-diameter, chem-mechanically polished, single crystal ⟨100⟩ silicon "float zone" material, which was boron-doped p-type material having 2 Ω-cm resistivity. The initial wafer cleaning step in Table 1 consisted of ultrasonic cleaning in hot peroxide solutions of ammonium hydroxide and hydrochloric acid, followed by a dip etch in concentrated hydrofluoric acid. A modified cleaning step, used later, included all of the previous cleaning solutions except that buffered hydrofluoric acid was used for the dip etch. Doubly distilled, deionized water of 18 MΩ-cm resistivity was used for the wafer rinsing steps. Following each of the cleaning steps, the wafers were spun dry in a centrifuge.

The SiO_2 "pad" oxide and gate oxide were both thermally grown at 1000°C in a dry O_2 ambient with 4.5 percent by volume HCl gas added, followed by annealing at the growth temperature for five minutes in argon to reduce both fixed oxide charge and interface states. The Si_3N_4 films were chemically vapor deposited with an Applied Materials' Model 704 radiant heating system at 800°C using a ratio of NH_3:SiH_4 of 160:1 by volume, with N_2 as a carrier gas. The deposition conditions were similar to those reported by Bassous *et al.* [5]. The Si_3N_4 deposition rate was 15 nm/min. The refractive index of the film was 2.0, and the etch rate in H_3PO_4 at 180°C was about 10 nm/min. Annealing for 10 minutes in nitrogen at

1000°C followed the nitride deposition. Special high-contrast photoresist was used throughout this study for pattern definition. Reactive ion etching with CF_4 was used to etch the nitride films. The field oxide was thermally grown at 1000°C, with 2 percent by volume HCl gas mixed with the O_2 ambient, under dry/wet (steam)/dry (DWD) conditions. Annealing in argon for 15 minutes at 1000°C followed the field oxidation. Then a solution of buffered hydrofluoric acid with a surfactant (glycerine) was used to strip the top layer of oxynitride formed on the nitride film as a result of the field oxidation. The nitride film was then stripped and over-etched in boiling (≈180°C) phosphoric acid.

Next, the pad oxide was stripped and *over-etched* with a solution of buffered hydrofluoric acid and glycerine to *partially* remove any nitridization on the active surface. The modified cleaning step was then used on the wafers just prior to the gate oxide growth of 35.0 nm. The metal electrode films, ≈1 μm thick, were vacuum deposited in a resistance-heated, tantalum boat evaporation system in which high-purity, sodium-free aluminum pellets were used. A hot phosphoric-nitric acid solution [8] (40 parts concentrated H_3PO_4, 3 parts concentrated HNO_3, 5 parts H_2O) was employed to etch the aluminum pattern. The final MOS processing step was annealing with a forming gas at 400°C for 20 minutes to reduce surface states.

• *Electrical measurements*

Dielectric breakdown characteristics [9] of the gate oxides were measured using a voltage ramp technique [10, 11]. Fowler-Nordheim tunneling current measurements were also performed using a log *I versus V* method. For both techniques, a negative voltage was applied to the top aluminum electrode, making it the electron-injecting electrode (cathode), while the silicon substrate was biased positive (anode). Using boron-doped, p-type substrates, the silicon surface near the SiO_2-Si interface was then in accumulation, and the entire applied potential was dropped across the silicon dioxide dielectric.

For the breakdown measurements, the voltage applied was increased with time at a rate of 20 V/s. A *variable* dc trigger circuit which detected current spikes of *typically* ≥50 μA was used to record the "initial" breakdown event [10]. This circuit was fast enough to detect "self-healing" breakdown events [12], in which the potential across the capacitor blows out the defective point or weak spot. The dc trigger current level was varied depending on the area of the thin oxide capacitor under test in accordance with the Fowler-Nordheim tunneling current model. To establish a large statistical data base, automatic data taking and reduction techniques using computers were utilized.

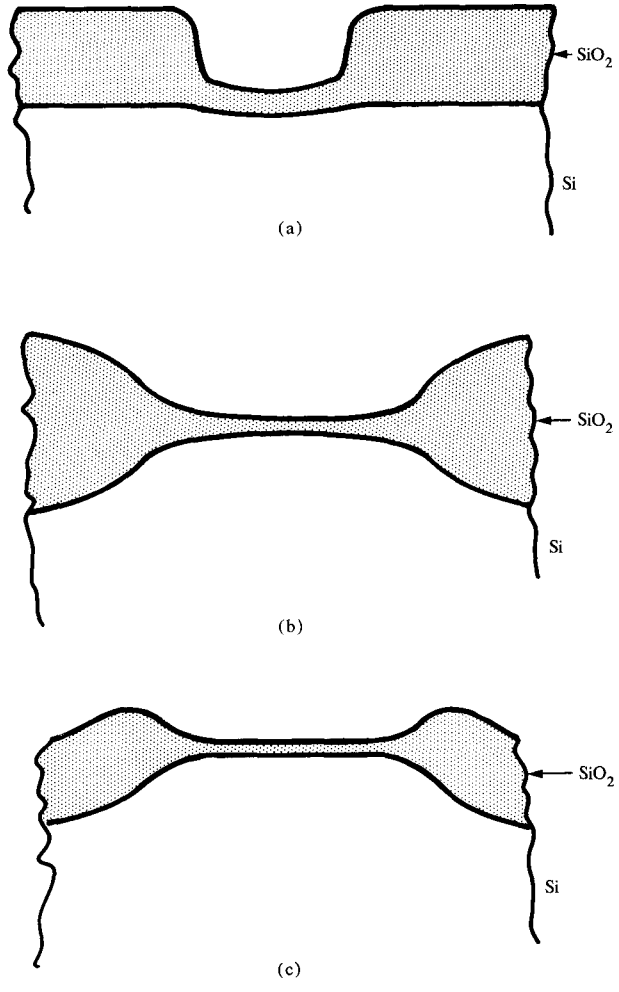

Figure 3 Three types of isolation schemes: (a) conventional (planar), (b) Semi-ROX, and (c) Full-ROX.

Results and discussion

• *Low voltage breakdown*

While monitoring the thin gate oxide breakdown characteristics associated with the Semi-ROX isolation process, we noticed that the gate oxides exhibited a serious shorting problem characterized by a low voltage breakdown, typically at 6-7 volts (1-2 MV/cm). The percent occurrence of the low voltage breakdown scaled with the thin gate oxide area of the individual devices.

This phenomenon was not observed with other isolation schemes, such as "conventional" (planar) and "Full-ROX" [5], illustrated along with Semi-ROX in Fig. 3. Figure 4 summarizes typical thin gate oxide dielectric breakdown characteristics associated with all three isolation

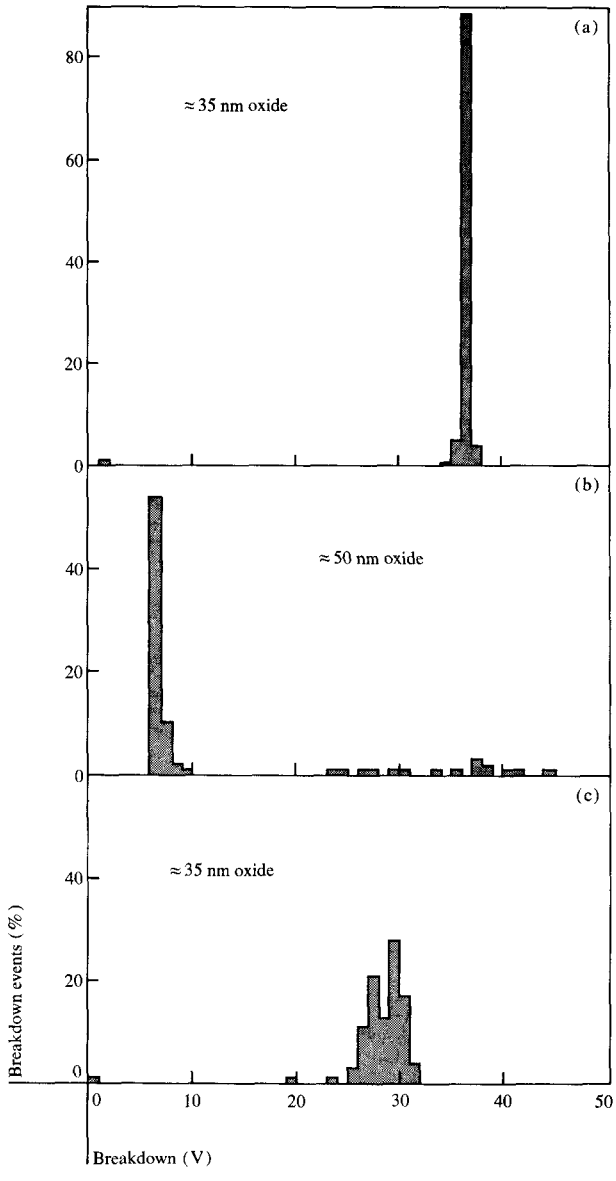

Figure 4 Thin gate dielectric breakdown characteristics associated with (a) the conventional structure, (b) the Semi-ROX structure, and (c) the Full-ROX structure. The area of each capacitor was equal to 0.064 mm^2.

schemes. The ordinate represents the percentage of breakdown events occurring at a given voltage. One hundred capacitors were measured in each histogram. Gate oxides were 4.5 percent HCl and 95.5 percent dry O_2 (mixed by volume) and were grown at 1000°C. (Note that the gate oxide thickness varied for each isolation scheme.) The individual capacitor's area in each case was fixed at 0.064 mm^2. The structure of the capacitors tested was the same as that shown at the top of Fig. 1, except that polysilicon was used as the gate electrode material.

The low voltage, low field breakdown problem associated with Semi-ROX processing was not typical of Full-ROX processing, in which the Si_3N_4 layer (used as the oxidation barrier) was much thicker (200 nm thick, compared to only 30 nm thick). This *preliminary data* led us to suspect a failure of the thinner nitride layer to act as a protective oxidation mask against chemical attack during the growth of the wet field oxide, which was processed at 1000°C.

Subsequent experiments demonstrated that the low voltage breakdown problem could definitely be reduced by employing a thicker nitride layer in Semi-ROX processing. A summary of our *initial findings* is presented in Fig. 5, which shows the average breakdown voltage of the thin gate oxide (approximately 35 nm) *versus* the thickness of the Si_3N_4 layer used as the oxidation barrier in the Semi-ROX process. All other Semi-ROX processing conditions were kept the same, including the 1000°C wet field oxidation. The average breakdown voltage over six wafers (98 points per wafer) plus the standard deviation were plotted for each nitride thickness used in the experiment. The thin planar gate oxide capacitors tested in this experiment were similar to those in the lower part of Fig. 1, with the area of each capacitor equal to 1.0 mm^2. It was clear from these data, even though there was an unusual amount of scatter, that the 100-nm nitride oxidation mask had yielded the best results in terms of the relatively high average gate breakdown voltages and the lack of low voltage (6–7 volts) values in the distribution. The 30-nm nitride samples were the worst, consistent with previous Semi-ROX runs in which a 30-nm nitride layer was also used. With the 300-nm nitride oxidation mask, the gate breakdown averages were slightly degraded, possibly due to a residual stress effect and/or difficulty in etching off the thick nitride layer prior to the gate oxidation. A similar observation was reported recently by Nakajima *et al.* [13].

This experiment was repeated with a simplified matrix using only two nitride thicknesses: the one that appeared to be the best in the previous experiment (the 100-nm nitride layer) and the one that typically appeared to be the worst (the 30-nm nitride layer). Controls, techniques, and monitors on the silicon pilot line were checked to reduce the random variations in the experimental results. The wet field oxidation temperature was again 1000°C, and an HCl-grown dry/wet/dry field oxide of 650 nm was grown. The pad oxide underneath the silicon nitride layer was 30 nm thick. Figure 6 summarizes the dielectric gate breakdown results of this nitride thickness experiment. Note the large preponderance of low field breakdown events around 2 MV/cm (7 volts for a 35-nm-thick gate oxide) for the 30-nm Si_3N_4 sample, while the 100-nm

Si_3N_4 sample showed a distinct absence of this type of gate breakdown. The 100-nm Si_3N_4 group compared favorably with the control sample, which did not undergo recessed oxide processing.

The gate oxide control samples consisted of wafers from the same lot as the others but were only processed from step 11 through step 18 of Table 1. For an exact comparison with the control group, the type of capacitor structure measured in Fig. 6 (to study this area defect problem) was the structure depicted in the lower part of Fig. 1. It was clear from this reproducible experiment that the use of a 100-nm nitride layer in the Semi-ROX process solved the low voltage gate breakdown problem. Furthermore, Semi-ROX processing produced planar gate oxide structures of the same quality as the planar gate oxide control samples.

Physical effects on Semi-ROX wafers

Visual and microscopic inspections were performed on all the wafers as they proceeded along the processing line. After nitride stripping (step 9 of Table 1), wafers that had a 30-nm nitride oxidation mask and were exposed to 1000°C DWD 650-nm field oxidation exhibited evidence of a surface reaction occurring in the active, soon to become gate, area.

In addition, after the pad oxide was stripped (step 10 of Table 1), SEM micrographs were taken of the active Si gate areas prior to gate oxidation. Both microprobe analysis and SEM micrographs confirmed that the Si surface in the active gate area had many pits. The Si surface had obviously been chemically attacked during the oxidation step, and it appeared that the 30-nm nitride oxidation mask was not sufficient to protect the active Si surface. The samples that showed this surface reaction later exhibited poor gate breakdown characteristics. This surface phenomenon was not observed when a 100-nm nitride oxidation mask was employed.

Both values found in the literature [14–16] and ellipsometric measurements made on the samples indicated that about 15 nm of the top surface of the nitride oxidation mask was converted into silicon oxynitride during the field oxidation process. Based on a conversion ratio of 1.5 SiO_2 film formed (actually, 1.64 in the literature [14]) to 1.0 Si_3N_4 consumed, only 20 nm of Si_3N_4 remained as a diffusion barrier in the samples that had 30 nm of nitride originally. Enomoto *et al.* [14] defined a "figure of merit," m, as follows:

$$m = \frac{\text{thickness of oxide grown on base silicon}}{\text{thickness of nitride oxidized}}.$$

Their work indicated that a large m value was obtained when a *wet* field oxidation was performed at *low* temperature. They suggested that at high temperature the Si-N bonds were resistant to breakage only in a *dry* oxygen

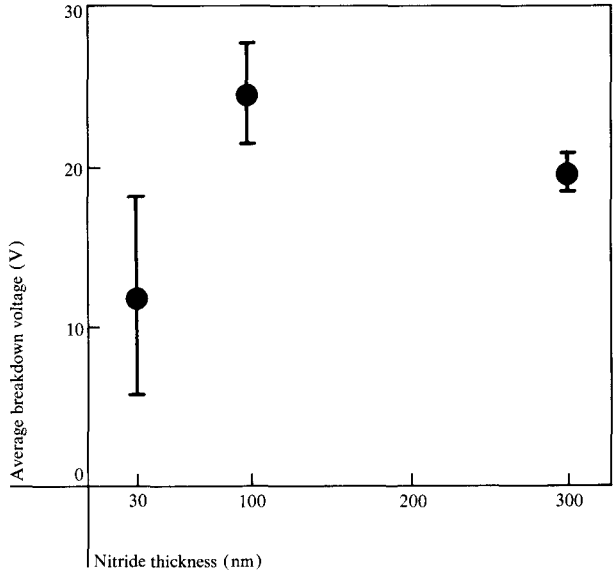

Figure 5 Average gate breakdown voltage *versus* nitride thickness used in Semi-ROX processing. The area of each capacitor was equal to 1.0 mm^2.

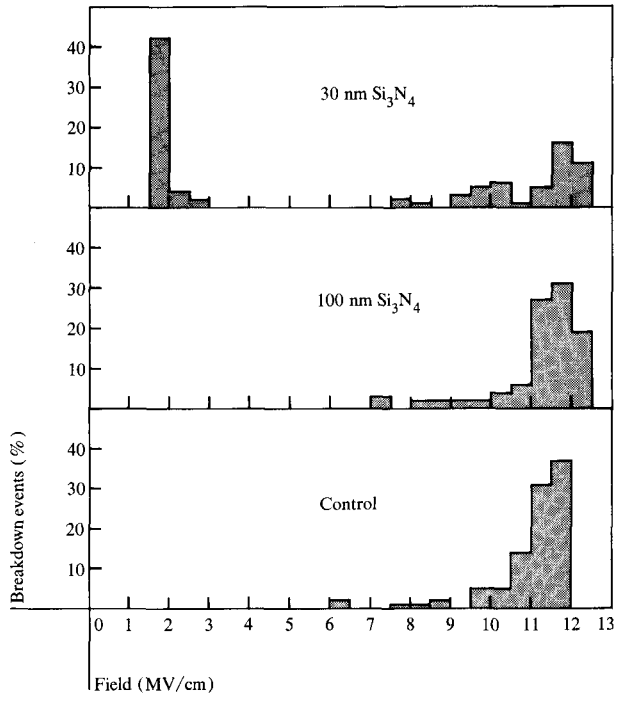

Figure 6 Percentage of breakdown events *versus* the applied field across the oxide. Histograms show the effect of using 30 nm and 100 nm of silicon nitride as an oxidation mask on the integrity of the gate oxide. The area of each capacitor was equal to 0.064 mm^2.

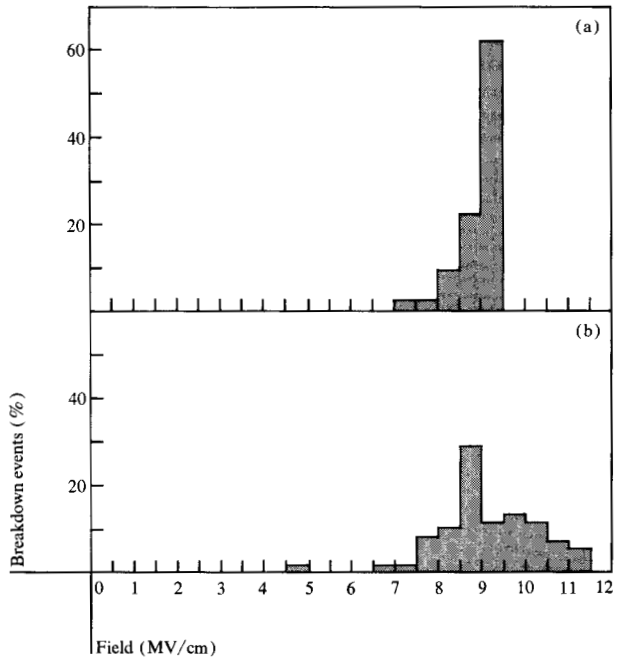

Figure 7 Percentage of breakdown events *versus* applied field across the oxide for stepped electrode capacitor (a) and planar electrode capacitor (b). The thin oxide capacitor area at (a) is 0.21 mm^2 and at (b) is 0.26 mm^2. The data show that the stepped electrode structure exhibits a high field cut-off at 9.5 MV/cm.

Table 2 Semi-ROX blanket experimental results for capacitor with an area of 1.82 mm^2.

950°C oxidation	$\%E_{BD} \leq 2 \times 10^6$ V/cm
30-nm pad/30-nm nitride	2
40-nm pad /100-nm nitride	1
1000°C oxidation	$\%E_{BD} \leq 2 \times 10^6$ V/cm
30-nm pad/30-nm nitride	18
40-nm pad/100-nm nitride	3

ambient, consistent with the findings of Fränz and Langheinrich [17]. Therefore, the entire silicon nitride thickness experiment was repeated with one major change: The *wet* 650-nm field oxidation was performed at approximately 950°C instead of 1000°C. The time needed to grow 650 nm of field oxide was adjusted accordingly. In this experiment a nitride thickness effect was not observed.

Blanket layer experiments

"Blanket layer" experiments were performed which substantiated the previous results. These experiments precluded the need for photolithography and were comparable to the others in indicating an area-related defect problem.

A metal evaporation mask with 1.52-mm-diameter dots was used to define MOS test structures. The dielectric gate breakdown results of these experiments are summarized in Table 2. It shows two variations of oxidation masking layers: (1) a 30-nm pad oxide used in conjunction with a 30-nm nitride layer; (2) a 40-nm pad oxide used in conjunction with a 100-nm nitride layer. At the time of these layer changes, the two wet field oxidation temperatures were 950°C and 1000°C. In Table 2 the percentage of gate oxide breakdowns ≤ 2 MV/cm field are tabulated. The nitride thickness effect was evident with the 1000°C wet field oxidation and not observed with 950°C oxidation. With blanket layer coverage of the wafers, field oxidation was simulated, since no patterns were defined in the pad oxide, nitride layers. The simulation included the appropriate time and temperature necessary to grow 650 nm of field oxide.

Area-related defect problem solutions

To summarize the area-related defect problem, which manifests itself by low voltage, low field gate breakdown, the following solutions have been found: (1) Thickening the Si_3N_4 layer, *e.g.*, from 30 nm to 100 nm; (2) lowering the field oxidation temperature, *e.g.*, from 1000°C to 950°C. Therefore, increased Si_3N_4 thickness is desirable, as well as a lower field oxidation temperature.

In addition, to gain further insight into the nature of the general area chemical surface attack, the following procedures were tried and proved to be successful: (a) reducing the field oxide thickness, *e.g.*, from 650 nm to approximately 350 nm, (b) capping the Si_3N_4 with CVD SiO_2, *e.g.*, 50 nm of CVD SiO_2 on top of 30 nm of Si_3N_4; and (c) stripping the original gate oxide and regrowing it, *e.g.*, stripping a 50-nm SiO_2 layer in buffered HF and regrowing it. Thickening the Si_3N_4 layer to 100 nm proved to be the most desirable when other aspects of Semi-ROX processing, such as reduction of *"bird's beak"* [5, 18], were considered.

Kooi effect and edge breakdown

From reports by Kooi *et al.* [19, 20], one would expect thinning (necking) of the gate oxide near the Semi-ROX boundary because of a nitrided silicon surface. Previous attempts to study this effect in Semi-ROX wafers failed because of a high incidence of low field breakdown events. With the solution of this problem, we have observed edge breakdown in Semi-ROX wafers. Figure 7 shows histograms of breakdown data obtained on capacitors over gate oxide only and on capacitors in which the Al overlapped the field oxide/gate oxide step. The cut-off in the latter case is clearly indicated in the data. Also, physical examination of samples in which self-healing breakdowns occurred (the Al metal is evaporated from

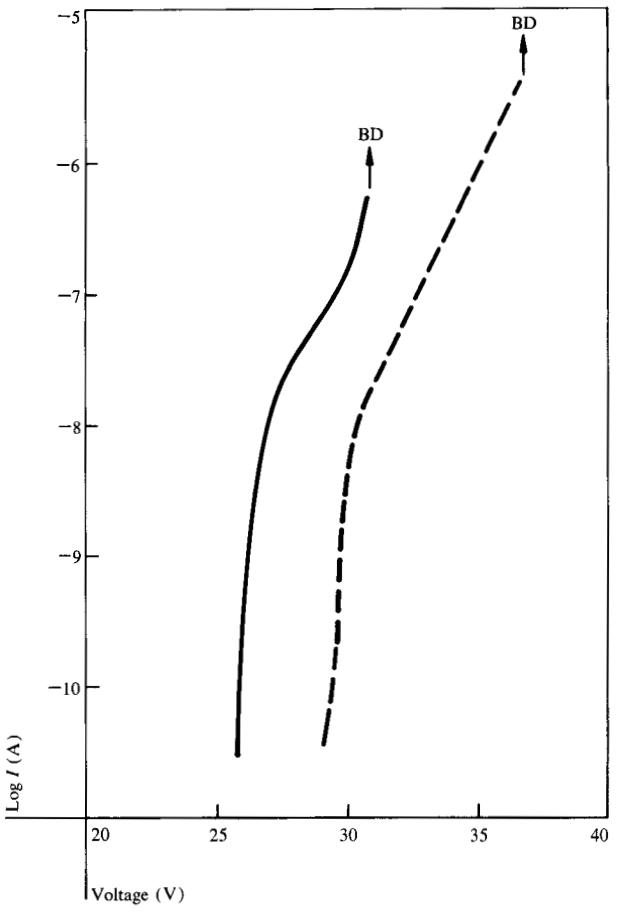

Figure 8 Log of current *versus* applied voltage shown by solid line for the stepped electrode structure (thin oxide capacitor area = 0.21 mm^2) and by the dashed line for the planar electrode (thin oxide capacitor area = 0.26 mm^2) for a 35-nm gate oxide.

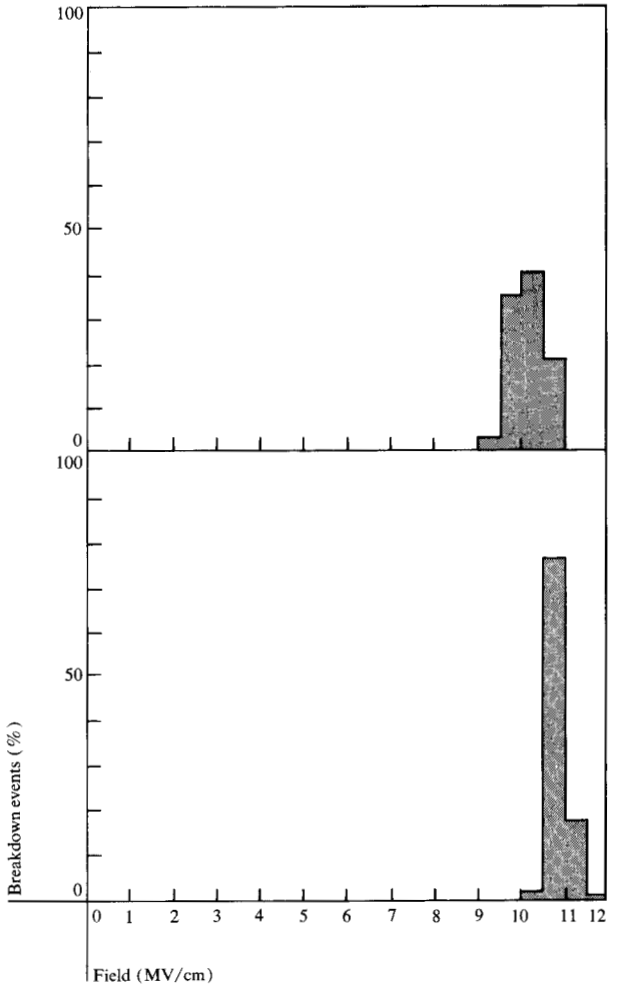

Figure 9 Percentage of gate breakdown events *versus* breakdown field taken on wafers that had 40 nm of pad oxide/100 nm of Si_3N_4 with 650 nm (DWD) of field oxide grown at 1000°C. Comparison is made between the stepped (overlap) structure (top) and the planar electrode (nonoverlap) structure (bottom). Discrete capacitor areas of the thin oxide are 0.041 mm^2 (top) and 0.064 mm^2 (bottom); average breakdown fields $\bar{E}$ = 10.1 MV/cm (top) and 10.8 MV/cm (bottom).

the breakdown area), indicated that edge breakdown was occurring in the overlap capacitors. Additional confirmation of the existence of a thin oxide region was obtained from the *I-V* characteristics of the two types of structures, as shown in Fig. 8. Further confirmation was obtained by observing that the magnitude of edge breakdown was inversely proportional to the pad oxide thickness and directly proportional to the wet field oxide thickness. Both observations were consistent with the mechanism suggested by Kooi. Examples of the above improvements, brought about by increasing the pad oxide thickness and decreasing the wet field oxide thickness, are shown in Figs. 9 and 10, respectively.

Failure mechanisms in gate oxides

The area defect problem may be caused by the mechanisms shown in Fig. 11. Mechanism A shows "H_2O/O_2" diffusing through the nitride layer, through the pad oxide layer, and chemically attacking the active silicon surface. Mechanism B shows "NH_3" diffusing through the remaining nitride layer, through the pad oxide layer, and chemically attacking the active silicon surface. Mechanism AB is a combination of the two, showing a nitridation at the edges of the SiO_2 product. Figure 12 illustrates the Kooi effect at the edge of the Semi-ROX structure, solely for an edge defect problem.

Each failure mechanism must be thought of in the context of the materials aspect of thin films. Thin films, in general, are never free of pinholes or defects. Microsplits, cracks, and edges of inclusions form easy diffusion paths, especially at *high temperature*. Ellipsometric measure-

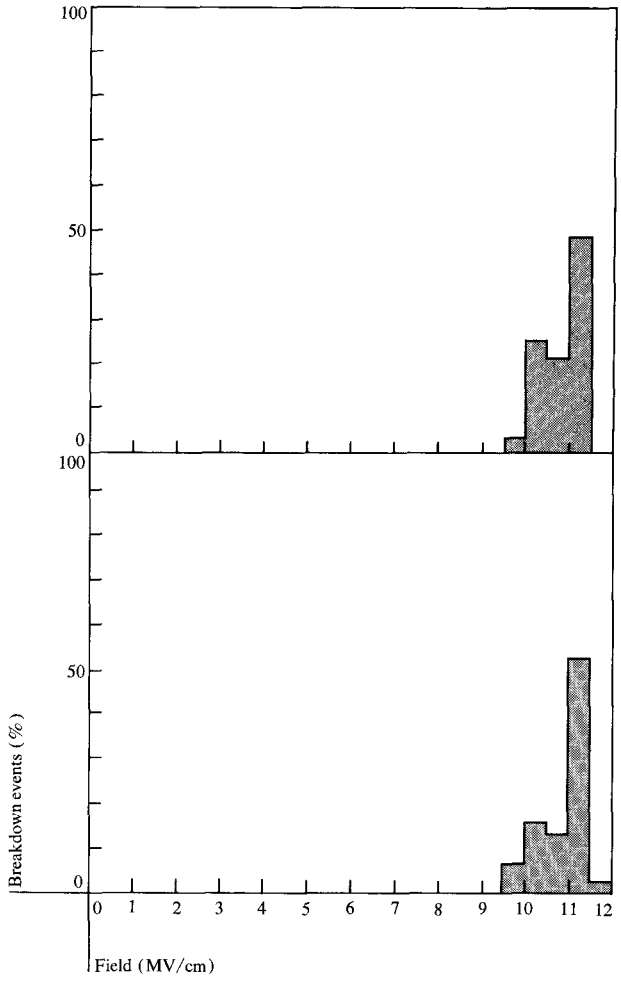

Figure 10 Percentage of gate breakdown events *versus* breakdown field taken on wafers that had 40 nm pad oxide/100 nm Si_3N_4 with 450 nm DWD field oxide grown at 1000°C. Comparison is made between the stepped (overlap) structure (top) and the planar electrode (nonoverlap) structure (bottom). Discrete capacitor areas of the thin oxide are 0.041 mm^2 (top) and 0.064 mm^2 (bottom). Areas given are for the thin gate oxide only. Average breakdown fields $\bar{E}$ = 10.8 MV/cm (top) and 10.9 MV/cm (bottom).

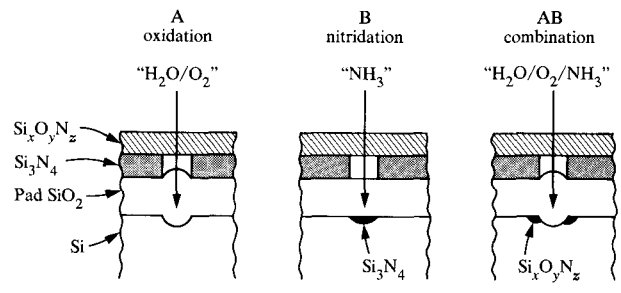

Figure 11 The area defect problem may be caused by these mechanisms.

ments, for example, do not take into account defect-related phenomena, in that thickness readings average over the whole beam. However, breakdown measurements are very sensitive to defects. The silicon areas attacked by a chemical reaction (1) create a nonplanar surface with high field charge injection points; (2) may not oxidize fully, as is the case with a nitrided surface [21]; (3) may form surface asperities which are difficult to clean.

Summary

This study indicates that both an increase in oxidation mask thickness and a decrease in wet field oxidation temperature markedly reduce the incidence of low voltage breakdowns in the gate oxide. Microscopic studies of samples which exhibited low voltage breakdowns showed that the Si_3N_4 oxidation mask had failed to protect the surface region in which the gate oxide was grown. SemiROX processing also exhibited edge breakdown, most likely due to the Kooi effect (nitrided Si surface). The use of a thicker pad oxide and decreasing the wet field oxide thickness were demonstrated to be beneficial in reducing the magnitude of the degradation in gate breakdown due to this edge effect.

Acknowledgments

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References

1. P. Richman, *MOS Field-Effect Transistors and Integrated Circuits*, John Wiley & Sons, Inc., New York, 1973.
2. J. A. Appels, E. Kooi, M. M. Paffen, J. J. H. Schatorje, and W. H. C. G. Verkuylen, "Local Oxidation of Silicon and Its Application in Semiconductor-Device Technology," *Philips Res. Repts.* **25,** 118 (1970).
3. E. Kooi and J. A. Appels, "Selective Oxidation of Silicon and Its Device Applications," *Semiconductor Silicon 1973*, H. R. Huff and R. R. Burgess, Eds., The Electrochemical Society, Princeton, NJ, 1973, p. 860.
4. Anonymous, "LOCOS: A New I.C. Technology," *Microelectronics and Reliability* **10,** 471 (1971).
5. E. Bassous, H. N. Yu, and V. Maniscalo, "Topology of Silicon Structures with Recessed SiO_2," *J. Electrochem. Soc.* **123,** 1729 (1976).
6. W. R. Hunter, L. Ephrath, W. D. Grobman, C. M. Osburn, B. L. Crowder, A. Cramer, and H. E. Luhn, "1 μm MOSFET VLSI Technology: Part V—A Single-Level Polysilicon Technology Using Electron-Beam Lithography," *IEEE Trans. Electron Devices* **ED-26,** 353 (1979).
7. K. Ohwada, K. Sakuma and K. Ehara, "Gate Oxide Defects near the Selectively Oxidized Silicon," *Jpn. J. Appl. Phys.* **17,** 737 (1978).
8. *Handbook of Thin Film Technology*, L. I. Maissel and R. Glang, Eds., McGraw-Hill Book Co., Inc., New York, 1970, pp. 7-36.

9. D. W. Ormond, "Dielectric Breakdown of Silicon Dioxide Thin Film Capacitors Using Polycrystalline Silicon and Aluminum Electrodes," *J. Electrochem. Soc.* **126,** 162 (1979).
10. C. M. Osburn and D. W. Ormond, "Dielectric Breakdown in Silicon Dioxide Films on Silicon, Part I. Measurement and Interpretation," *J. Electrochem. Soc.* **119,** 591 (1972).
11. C. M. Osburn and D. W. Ormond, "Dielectric Breakdown in Silicon Dioxide Films on Silicon, Part II. Influence of Processing and Materials," *J. Electrochem. Soc.* **119,** 597 (1972).
12. N. Klein, "Electrical Breakdown in Solids," *Advances in Electronics and Electron Physics* **26,** 309 (1969).
13. O. Nakajima, N. Shiono, S. Muramoto, and C. Hashimoto, "Defects in a Gate Oxide Grown after the LOCOS Process," *Jpn. J. Appl. Phys.* **18,** 943 (1979).
14. T. Enomoto, R. Ando, H. Morita, and H. Nakayama, "Thermal Oxidation Rate of a Si_3N_4 Film and Its Masking Effect against Oxidation of Silicon," *Jpn. J. Appl. Phys.* **17,** 1049 (1978).
15. S. I. Raider, R. Flitsch, J. A. Aboaf, and W. A. Pliskin, "Surface Oxidation of Silicon Nitride Films," *J. Electrochem. Soc.* **123,** 560 (1976).
16. S. P. Murarka, C. C. Chang, and A. C. Adams, "Thermal Nitridation of Silicon in Ammonia Gas: Composition and Oxidation Resistance of the Resulting Films," *J. Electrochem. Soc.* **126,** 996 (1979).
17. I. Fränz and W. Langheinrich, "Conversion of Silicon Nitride Into Silicon Dioxide Through the Influence of Oxygen," *Solid-State Electron.* **14,** 499 (1971).
18. H. Miyoshi, N. Tsubouchi, and A. Nishimoto, "Selective Oxidation of Silicon in High Pressure Steam," *J. Electrochem. Soc.* **125,** 1824 (1978).
19. E. Kooi, J. G. van Lierop, and J. A. Appels, "Formation of Silicon Nitride at a Si-SiO_2 Interface during Local Oxidation of Silicon and during Heat-Treatment of Oxidized Silicon in NH_3 Gas," *J. Electrochem. Soc.* **123,** 1117 (1976).
20. D. W. Ormond and R. W. Young, "Electrical Confirmation of the Kooi Effect in LOCOS Structures," *Extended Abstr. Electrochem. Soc.* **79-1,** 231 (1979).

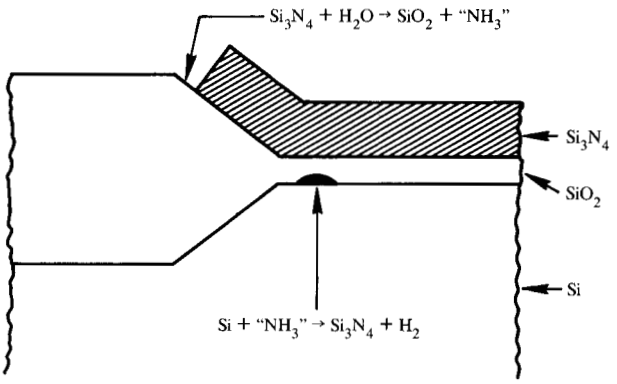

Figure 12 Edge defect problem may be caused by the above mechanism, first proposed by Kooi [19].

21. K. Taniguchi, K. Kurosawa, and Y. Takeuchi, "Analyses of Several Problems of Coplanar Method as Applied to VLSI," *Proceedings of the 15th Symposium on Semiconductors and Integrated Circuits Technology*, Tokyo, Japan, November, 1978.

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