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Metallization Processes in Fabrication of Schottky-barrier FET's*

Abstract: The metallization processes necessary for the production of microwave Schottky-barrier field-effect transistors are described. Since the gate contact is only 1 micrometer wide, the holes and the metallization of the source, drain and gate contacts are produced simultaneously. Then in a subsequent process, the source and drain contacts are converted to ohmic contacts by the evaporation of Au-Sb onto these contacts. Mask alignment is not a problem because the Au-Sb spreads across the surface after suitable heat treatment.

Narrow gate contacts are necessary for a high cutoff frequency of a microwave Schottky-barrier field-effect transistor. Gate contacts only 1 micrometer wide would permit cutoff frequencies above 10 GHz. In order to fabricate such transistors, new optical and metallization processing steps were devised. The optical processing steps have been discussed previously,[1] and the metallization steps will be the subject of this communication.

A rather obvious way of producing a Schottky-barrier FET would start with making source and drain holes in a SiO_2 layer covering a Si wafer (Fig. 1a). In a second step these holes are then filled with a suitable metal alloy (Fig. 1b). In the case of n-type Si, an alloy of Au with a few percent Sb is customary. Subsequently, the wafer is heat-treated, so that alloying of the Au–Sb with the Si in the SiO_2 holes takes place (Fig. 1c). Because of the Sb addition, the source and drain contacts become ohmic. In a final step, a hole for the gate contact is etched between the source and drain contacts (Fig. 1d), followed by a suitable gate metallization step (Fig. 1e). Such a processing-step sequence is feasible as long as the dimensions of the transistor do not become too small, but ordinarily cannot be used for 1-μm gate holes without resorting to electron beam technology.

The main problem arises, in the sequence outlined above, when one tries to make the gate hole in the SiO_2 layer. This is obtained by a photoresist process, followed by an etch process. Because of the rather rough surfaces of the source and drain contacts, and the fact that the very thin photoresist layers required to produce 1-μm-wide holes are obtained by spinning at very high speeds, the thickness of the photoresist between the source and drain contacts tends to be rather inhomogeneous. This leads to irregular, and consequently unusable gate holes.

To circumvent this problem, another sequence of processing steps was introduced, the main feature being the simultaneous fabrication of gate, source and drain contacts. In a second step the source and drain contacts are converted from Schottky-barrier to ohmic contacts.

Device fabrication

In spite of the condition that gate, source and drain holes have to be made simultaneously, several different methods for the production of Schottky-barrier FET's remain possible. After experience was acquired with some of these methods, the following technique was chosen.

A high-resistance Si substrate covered with a thin low-resistance epitaxial layer is oxidized in wet oxygen in the usual manner. Next, the wafer is covered with a thin layer of positive photoresist (AZ 1350) and exposed to light. In contrast to the method of contact masking, the mask containing the source, gate and drain structures is projected by means of a high-quality microscope objective onto the wafer. The mask is simultaneously reduced (25×) so that the final gate width is just 1 micrometer. The distance between the source and drain contacts is 3 micrometers. The photoresist layer is developed as described previously,[1] so that source, drain and gate holes occur in the resist layer and also in the SiO_2 layer after etching in buffered

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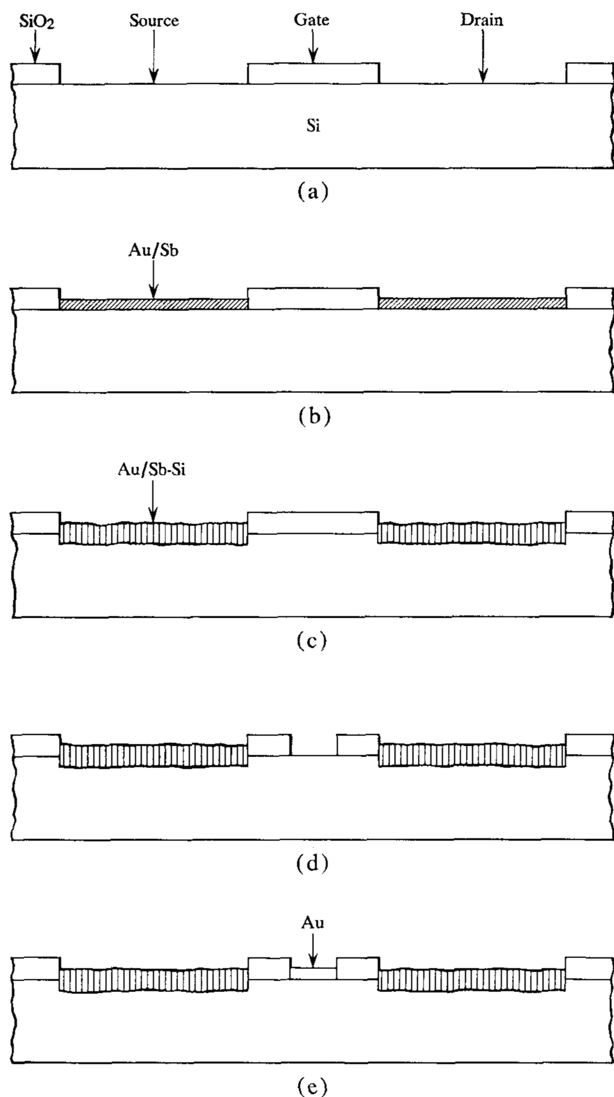

Figure 1 Simplified presentation of a processing step sequence for a Schottky-barrier FET with coarse structures: a) Opening up of source and drain holes in the SiO_2 layer. b) Filling of the holes with Au-Sb. c) Alloying of Au-Sb with Si. d) Opening of gate hole. e) Metallization of gate contact.

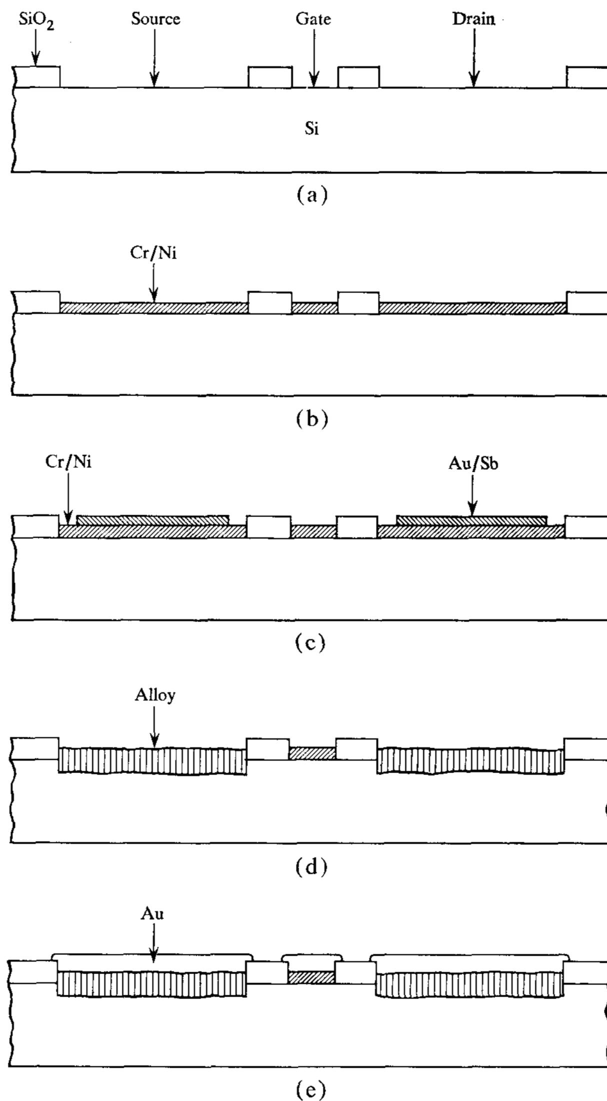

Figure 2 Simplified presentation of new processing step sequence for a Schottky-barrier FET with micrometer structures: a) Opening up the source, drain and gate holes in the SiO_2 layer. b) Metallization of source, drain and gate contacts with Cr-Ni. c) Metallization of source and drain contacts with a Cr-Au/Sb-Cr sandwich with coarse registration. d) Heat treatment during 15 min at 550°C causing surface diffusion, volume diffusion and alloying. e) Gold plating.

etch (Fig. 2a). The final gate hole is 1 micrometer wide and the edges are very satisfactory.

The wafer, which is still covered with nonexposed photoresist, is inserted into a vacuum belljar, and a film sandwich consisting of 50 Å Cr and 150 Å Ni is evaporated. Now the photoresist is stripped off, with the result that only the gate, source and drain holes remain covered with Cr-Ni (Fig. 2b). When measured, it appears that the gate as well as the source and drain contacts are Schottky-barrier diodes. However in order to make a Schottky-barrier FET, it is necessary to convert the source and drain contacts or at least the source contact into ohmic contacts. This is achieved in the following manner.

The wafer is again covered with a photoresist layer. By means of the projection masking technique, holes in the resist are made on top of the source and drain contacts but not on top of the gate contact. A sandwich of 30 Å Cr-300 Å Au-Sb-30 Å Cr is evaporated on top of the wafer, and the resist with the metal on top of it is stripped off. Au-Sb remains on top of only the source and drain

contacts (Fig. 2c). A subsequent heat treatment of 15 min at 550°C in vacuum causes the Au–Sb to diffuse through the previously deposited Cr-Ni layer and to alloy with the underlying Si epitaxial layer (Fig. 2d). The source and drain contacts are now ohmic.

The reason why the Au-Sb film is sandwiched between two thin Cr layers is as follows: When only a single Au–Sb film is evaporated on top of the Cr-Ni film, it appears that, because of the covering of the Cr-Ni with a NiO film, the adhesion of the Au-Sb to the Cr-Ni underlayer is very unsatisfactory. However, an intermediate Cr-film is capable of solving this problem. The second Cr-film is necessary because it appeared that, during the resist stripping process (usually done by rubbing with a Q-tip soaked in a resist solvent) Au-Sb dust was smeared all over the wafer, forming bridges between source and drain contacts. The Cr layer proved to be very effective in preventing these short circuits. Practically all the Au-Sb dust particles can now be removed with the Q-tip. The explanation seems to be that the adhesion between Cr or, in fact, Cr_2O_3 and Au-Sb is very small in contrast to the adhesion between the Au-Sb surfaces and the Au-Sb particles.

For good operation of the Schottky-barrier FET it is necessary that the resistance between the source and drain contact be as low as possible. It seems necessary therefore that the Au-Sb fill the source and drain contacts as well as possible. Especially the contact areas facing the gate contact are critical. To achieve this, good registration between the first and second masking processes is required. In view of the extremely small width of the gate contact and the gate-source and gate-drain distances this registration is very difficult to achieve.

During preliminary experiments it appeared that, even when registration was insufficient, the total surfaces of the source and drain contacts showed alloying.

It was found that upon heat-treatment, the Au-Sb spread across the Cr-Ni layer in the source and drain contacts and then diffused through this Cr-Ni layer to alloy with the Si epitaxial layer. The Au-Sb, however, does not spread across the SiO_2 surface, which makes the above phenomenon so useful.

The metal-spreading process, which will be described in the next section, permits poor registration without the penalty of too high source-drain resistances. It was even observed that when only a small dot of Au-Sb was placed in the source and drain contacts, these contacts were completely alloyed and ohmic after heat-treatment.

Because the metal layers forming the transistor structure are rather thin, in a last step a gold-plating process has to be employed (Fig. 2e). Initially the gold did not adhere too well to the contact surfaces, but after introducing an intermediary Ni-plating bath to improve the contact surfaces, the gold adhered well enough to enable subsequent wire bonding.

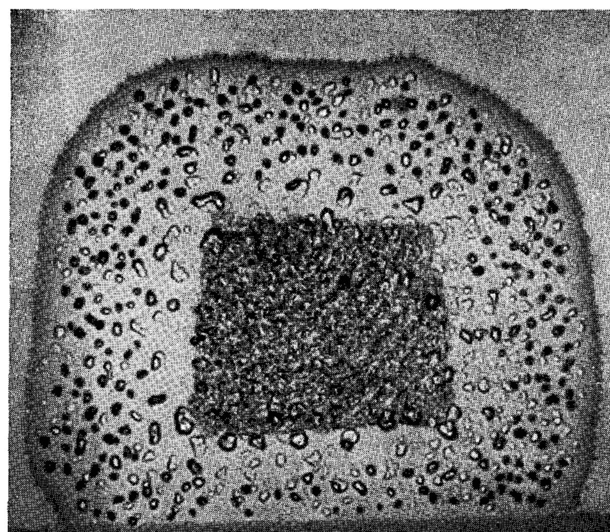

Figure 3 Spreading of AuSb starting from a small evaporated square across a Cr-Ni surface after a heat treatment of 15 min. at 550°C.

Metal spreading

Diffusion in solids can take place in various ways: through the crystal lattice, in grain boundaries and dislocations, and along surfaces.[2] Whereas the first diffusion processes have been rather well studied, surface diffusion is less understood and usually considered as an undesirable effect[3] when the other processes are being investigated. The activation energies related to surface diffusion seem to be lower than in the case of lattice diffusion and are affected by the nature of the surface and its contamination.

In the case of the Schottky-barrier FET, a heat treatment of 15 min at 550°C is sufficient for diffusion of Au-Sb across the Cr-Ni surface, through the Cr-Ni layer, and alloying with Si.

The surface diffusion process is well illustrated by Fig. 3 which shows the spreading of Au-Sb starting from a small evaporated square of Au-Sb. In further experiments, surface diffusion on layers of Cr or Ni was studied. It was observed that surface diffusion of Au-Sb took place across Cr layers but not across Ni layers. For the production of the transistor, a sandwich of 50 Å Cr and 150 Å Ni was deposited. This combination was chosen because the Cr permitted metal spreading, and Ni improved the adhesion of the electroplated Au film at the end of the processing step sequence.

The production of microwave Schottky-barrier FET's has shown that mask-alignment problems can be obviated by means of metal surface diffusion.

It would be worth while to study other systems to see whether mask alignment occurring during the fabrication of other kinds of semiconductor devices especially those with miniature structures, could be simplified.

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