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Semiconductor Crosspoints

Abstract: The design considerations for a semiconductor crosspoint consisting of an SCR-diode-resistor circuit are presented and the fabrication process is briefly reviewed. These crosspoints have an ON-resistance of three to four ohms and a capacitance of approximately three picofarads. They can be interconnected on ceramic modules to form matrix arrays for use in telephone line switching applications.

Introduction

The high performance, excellent reliability, and low cost which semiconductors have demonstrated in computer applications have given impetus to their consideration as crosspoints for communications line switching applications.[1,2] In contrast to previous approaches to the use of semiconductor crosspoints in both time-division and space-division multiplex operation,[3–14] the device described in this paper is an integrated design.

In line switching functions, the crosspoint must have the following properties: (1) Two stable conditions, the ON and OFF states. (2) A high impedance in the OFF state with respect to the impedance in the ON state.

The impedance in the OFF state is generally capacitive; thus the OFF impedance determines the bandwidth of the system. A typical crosspoint figure of merit is the ratio of the OFF impedance to the ON resistance at audio frequencies.

The crosspoint should possess a latch characteristic, i.e., once placed in the ON state the crosspoint should remain ON after the removal of the turn-on signal. Additional considerations for such a switch are

(1) triggering current, i.e., current required to place the switch in the ON state,
(2) holding current, i.e., current required to maintain the switch in the ON state,

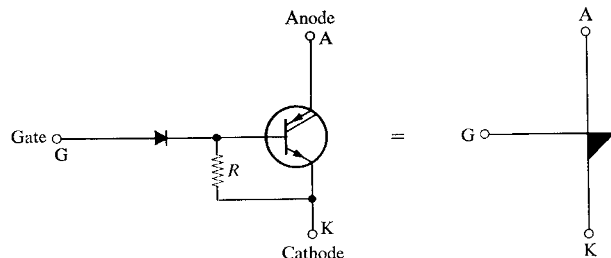

Figure 1 Basic crosspoint.

(3) noise sensitivity,
(4) maximum voltage in the OFF state, and
(5) turn-on and turn-off switching speeds.

Space-division multiplex switching applications generally involve matrix arrangements. The crosspoint must therefore be capable of matrix selection, and the selection circuitry must be isolated from the main signal path.

A silicon controlled rectifier (SCR)-diode-resistor circuit fills these requirements quite well. Such a crosspoint is illustrated in Fig. 1. A positive signal from gate to cathode of approximately two volts is sufficient to switch the SCR from the high-impedance OFF state to the saturated, or low-impedance, ON state. The gate-to-cathode signal may then be removed and the SCR will remain in the ON state provided the anode current is maintained at a level greater than some minimum level of holding current. The switch is turned off by decreasing the anode current below the holding current value. The function of the resistor is to control the trigger current, holding current, and noise sensitivity. The diode is used to provide isolation between

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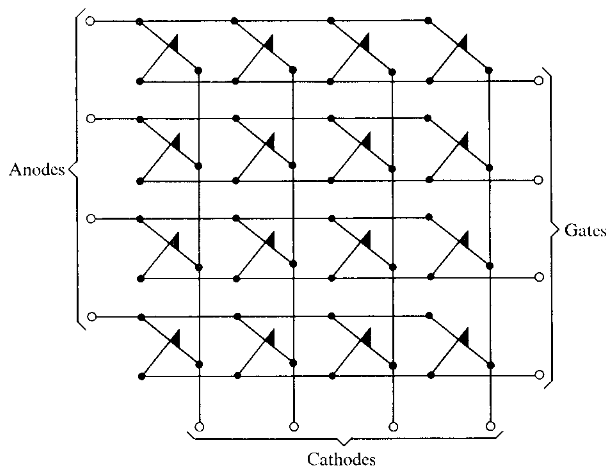


Figure 2 Matrix arrangement of crosspoints.

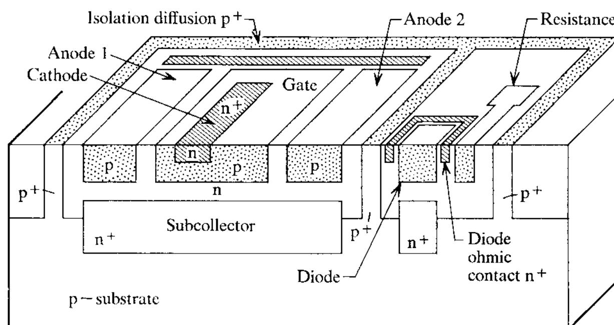


Figure 3 Semiconductor crosspoint with diffused regions but without contact metallization.

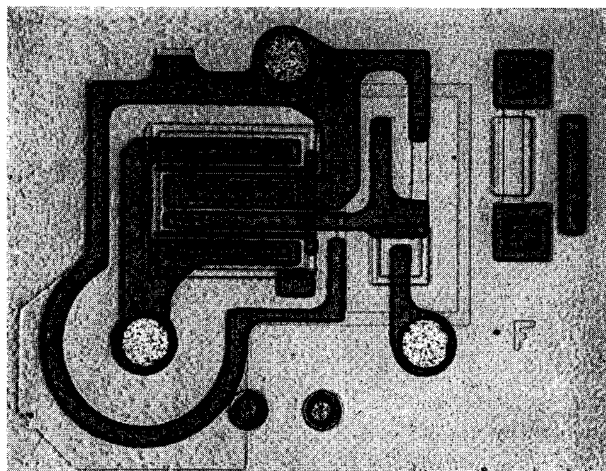


Figure 4 Semiconductor crosspoint with aluminum contacts and interconnections.

the signal path and the firing path. The gate control characteristics permit matrix selection; a typical matrix arrangement is illustrated in Fig. 2.

Design considerations

The basic structure is shown in Fig. 3; the aluminum interconnections between the various diffused regions are shown in Fig. 4. The pnp portion of the pnpn (SCR) device consists of a lateral transistor structure.[15] An n^+ buried layer is located under the SCR and diode. The functions of this n^+ layer are to improve the current gain of the lateral transistors[16] and to reduce parasitic transistor effects. A study of Figs. 3 and 4 indicates that there are a number of parasitic transistor effects. These effects are illustrated in Fig. 5 and will be considered in the design.

- *Breakover voltage*

The typical characteristic of an SCR with $I_G = 0$ is shown in Fig. 6. Breakover voltage is the voltage for which $\Delta V_{AK}/\Delta I_A$ equals zero. If the anode-to-cathode voltage exceeds this level, the device will exhibit negative resistance and switch to the low-voltage ON state. Thus the breakover voltage defines the maximum anode-to-cathode operating voltage.

In the analysis of SCR's it is convenient to think of the pnpn structure as interconnected pnp and npn transistors;[17,18] this is shown in Fig. 7. It may easily be shown that the breakover voltage condition is given by $(\alpha_{npn} + \alpha_{pnp})M = 1$, where α_{npn} and α_{pnp} are the respective common base current gains of the npn and pnp transistors and M is the avalanche multiplication factor of the common collector junction of the two transistor sections. (Here M is assumed equal for electrons and holes.) Therefore, the current and voltage dependence of α_{npn} and α_{pnp}, as well as the avalanche multiplication factor M, determine the breakover voltage. The SCR considered here has a resistor shunting the emitter-base junction of the npn transistor (Fig. 1), which in effect is much like the so-called "shorted emitter" of earlier work.[19] This resistor serves to degrade the low current gain of the npn transistor; this effect is shown in Fig. 8. The current gain of the lateral pnp transistor is generally low ($\alpha_{pnp} = 0.1$ to 0.9). Thus the value of $\alpha_{npn} + \alpha_{pnp}$ is less than one for low current values. This in turn requires that the avalanche multiplication factor be substantially greater than one to achieve the breakover voltage condition. Therefore, the breakover voltage is simply the breakdown voltage of the central p-n junction collector. The breakdown voltage of the central junction is determined primarily by the doping of the n-type epitaxial layer and the junction depth.[20]

- *Parasitic field-effect transistor action*

A study of Fig. 9 indicates that the aluminum land which contacts the n^+ cathode region acts as a gate for a field-

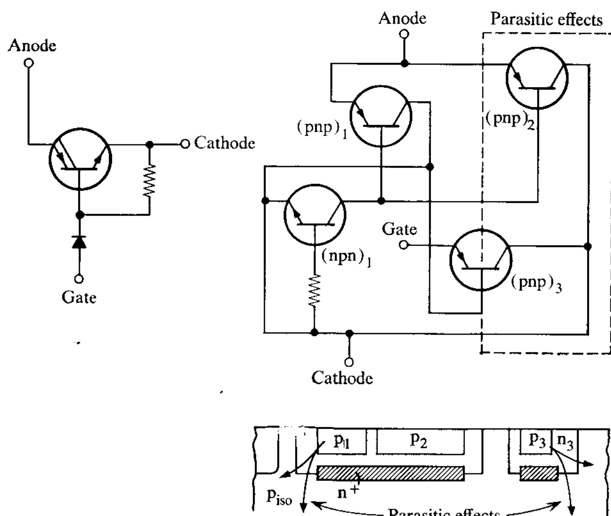


Figure 5 Representation of the various transistor interactions.

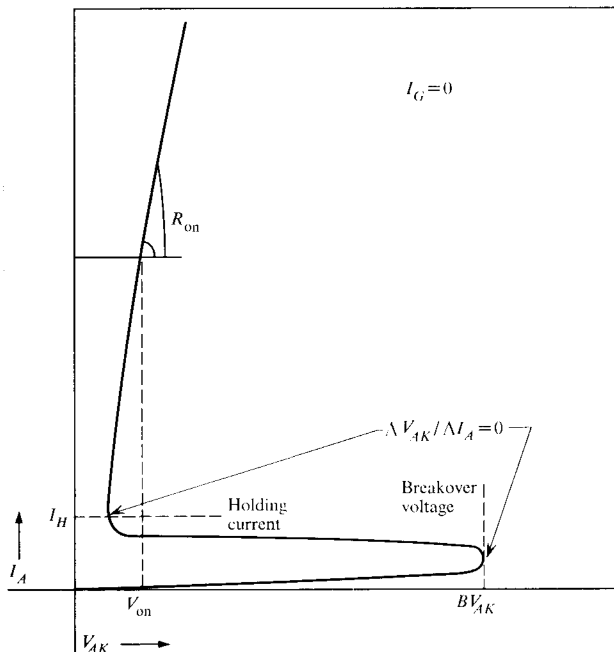


Figure 6 Anode-cathode characteristic of an SCR with gate open.

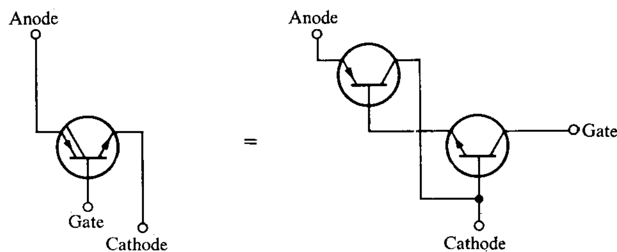


Figure 7 SCR representation.

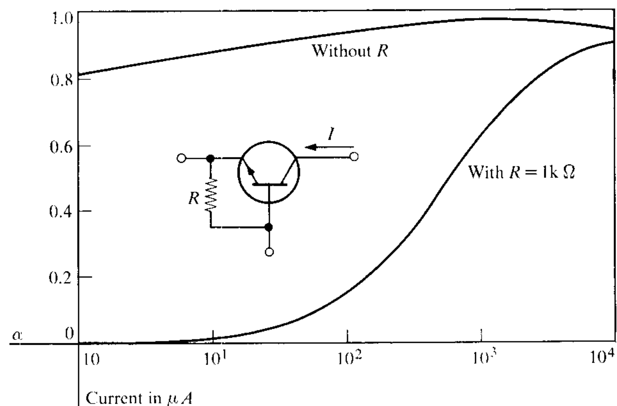


Figure 8 Degradation of low current gain by emitter-base shunting resistor.

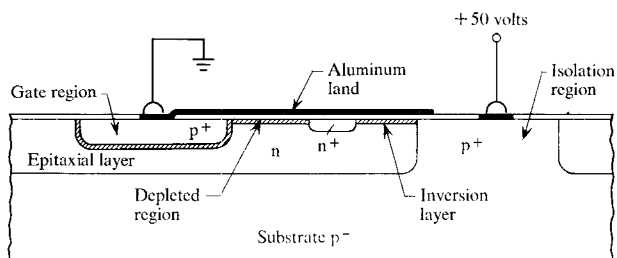


Figure 9 Elimination of parasitic field-effect transistor action by an n⁺ diffused region.

effect transistor whose source and drain are the gate and isolation diffused regions. A rather low voltage is required to invert the surface of the n-type epitaxial layer. The voltage required to invert the epitaxial layer surface will depend on such factors as oxide thickness and surface state charge; typical voltages required to invert this surface may range from 5 to 20 V. This effect would result in a low cathode-to-anode breakdown voltage condition. The parasitic field-effect transistor action can be eliminated by placing an n^+ region between the SCR and isolation diffused regions as shown in Fig. 9. Such an n^+ region is also used to eliminate the parasitic field-effect transistor action between the p-type diode and isolation diffused regions.

- *ON resistance*

The ON resistance is defined as $\Delta V_{AK}/\Delta I_A$. An accurate analysis of the ON resistance is quite complicated due to

the high injection levels and the two-dimensional nature of the current distribution. A first-order estimate of the ON resistance is

$$R_{ON} = (kT/qI_A) + R_{(\text{aluminum lands})}. \quad \text{(See footnote)} \qquad (1)$$

This expression is based on the assumption that both the pnp and npn components of the SCR are heavily saturated and at best (1) provides only a lower limit.

• *Holding current*

The holding current is defined as the anode current for which $\Delta V_{AK}/\Delta I_{AK} = 0$ with $I_G = 0$ (see Fig. 6). When the anode current drops below this value, the SCR will switch from the ON to the OFF condition.

An expression for the holding current may be obtained by considering the representation shown in Fig. 5. The base width and doping of the npn transistor are such that its common base current gain is very nearly equal to one; the low current gain characteristics of the npn transistor are thus determined solely by the shunting reisitor. The current which flows into the shunting resistor when the anode current is equal to the holding current, I_H, is simply $\alpha_{(pnp)_1} I_H$. The condition for $I_A = I_H$ is then given by

$$\alpha_{(pnp)_1} I_H = V_{BE}/R, \qquad (2)$$

where at best α_{pnp} can only be approximated. V_{BE} is the forward bias on the emitter-base junction of the npn transistor; this is typically 0.6 to 0.7 V. Holding current can then be expressed as

$$I_H = V_{BE}/R\alpha_{(pnp)_1}. \qquad (3)$$

The lateral transistor which forms $(pnp)_1$ is illustrated in Fig. 10. Lindmayer and Schneider[21] have developed a one-dimensional theory of the lateral transistor. Fulkerson[22] has considered a two-dimensional model. These treatments are not directly applicable in the present case, since this structure contains an n^+ buried layer as well as the substrate and isolation diffused regions which serve as a collector of minority carriers. In order to obtain an estimate of the design factors which determine $\alpha_{(pnp)_1}$ the following simplifying assumptions will be made:

(1) The n^+ buried layer acts as a perfect barrier to hole current flow from the n-type epitaxial layer into the n^+ buried layer. This is due to the large electric field created by the impurity gradient at the n-n^+ junction.
(2) The diffusion length of holes in the n-type epitaxial layer is large compared with the thickness of the epitaxial layer and the base width of the lateral $(pnp)_1$ transistor.
(3) Surface recombination effects are negligible.
(4) The p^+ anode has unity injection efficiency.

* Resistance of n^+ buried layer does not seem to play any role in the reduction of R_{ON}. Structures made with and without subcollector have shown the same ON resistance. A detailed discussion of the effect of the buried layer on the switching characteristic of SCR's is given in Ref. 16.

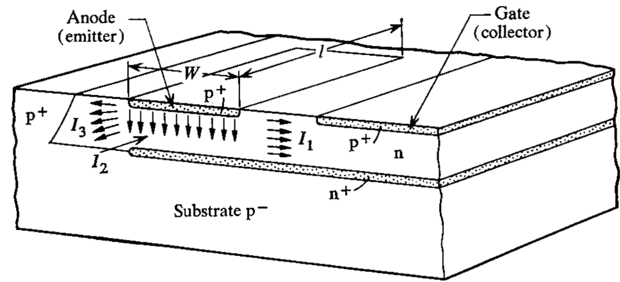


Figure 10 Cross section of $(pnp)_1$.

If we consider the various current components shown in Fig. 10, we see that $\alpha_{(pnp)_1}$ is given by

$$\alpha_{(pnp)_1} = I_1/(I_1 + I_2 + I_3), \qquad (4)$$

where I_1 = current injected toward the p^+ gate junction of the lateral transistor,
I_2 = current injected into the epitaxial region under the p^+ anode diffused region,
I_3 = current injected toward the p^- substrate and p^+ isolation diffused regions.

These current components may to a first-order approximation be given as

$$I_1 \approx \frac{qDtlp_0}{W_b}$$

$$I_2 \approx \frac{qWtlp_0}{\tau}$$

$$I_3 \approx \frac{qDtlp_0}{W_s},$$

where

W = width of the p^+ anode,
W_b = "effective" base width from the p^+ anode to the p^+ gate,
W_s = "effective" base width from the p^+ anode to the substrate,
t = epitaxial layer thickness,
l = length of the p^+ anode,
p_0 = injected hole density at the p^+-n junction,
τ = lifetime of holes in the n-type epitaxial region, and
D = diffusion constant for holes in the n-type epitaxial region.

Because the above expressions neglect the details of the two-dimensional nature of the current injected by the p^+ anode, $\alpha_{(pnp)_1}$ is given by

$$\alpha_{(pnp)_1} \approx \frac{\frac{1}{W_b}}{\frac{1}{W_b} + \frac{1}{W_s} + \frac{W}{L^2}}. \qquad (6)$$

This analysis indicates that $\alpha_{(\mathrm{pnp})_1}$ should lie in the range of 0.2 to 0.6.

Combination of Eqs. (3) and (6) gives

$$I_H \approx \frac{V_{BE}}{R}\left[1 + W_b\left(\frac{1}{W_e} + \frac{W}{L^2}\right)\right]. \tag{7}$$

Recombination within the epitaxial region and surface recombination will tend to increase the holding current above the limiting value given by Eq. (7).

- *Trigger current*

The trigger current is defined as the gate current necessary to switch the device from the high-impedance state to the low-impedance state. The triggering will occur when the emitter-base voltage, V_{BE}, on the $(\mathrm{npn})_1$ transistor reaches approximately 0.6 to 0.7 V. Since the current gain of $(\mathrm{npn})_1$ is high, the current which flows through the shunting resistor is just $[1 - \alpha_{(\mathrm{pnp})_3}]$ times the gate current. Thus, the gate triggering condition is given by

$$V_{BE} = R[1 - \alpha_{(\mathrm{pnp})_3}]I_{gt} \tag{8}$$

or

$$I_{gt} = \frac{V_{BE}}{R}\frac{1}{[1 - \alpha_{(\mathrm{pnp})_3}]}. \tag{9}$$

The value for $\alpha_{(\mathrm{pnp})_3}$ may be determined by considerations similar to those discussed in conjunction with the holding current analysis.

- *OFF impedance*

The OFF impedance is capacitive for frequencies above 1 kHz. An equivalent circuit of the device in the OFF state is shown in Fig. 11. The stray capacitance represents the capacitance from the aluminum anode conductor to the substrate. The isolation junction capacitance is generally several times larger than the central junction capacitance.

- *Rate-effect sensitivity*

One of the most important characteristics of an SCR is its so-called rate-effect sensitivity. A fast positive voltage pulse applied at the anode of an SCR in the OFF state causes a capacitive current to flow through the central junction of the device. If this current is sufficiently large, the device alpha's increase and the SCR will trigger even though the anode voltage is less than the breakover voltage. This rate effect places a limit on the frequency range with which the device may be used.

The rate-effect sensitivity involves the ac characteristics of each of the four transistors shown in Fig. 5. In order to obtain a lower limit on the rate-effect sensitivity we will consider the equivalent circuit shown in Fig. 12. The SCR will trigger when the voltage across the emitter shunt R reaches a critical value which is approximately the forward voltage, V_{BE}, of the emitter-base junction;[16] this value is approximately 0.6 to 0.7 V. If the anode voltage is a ramp with slope a, then the voltage across R is given by

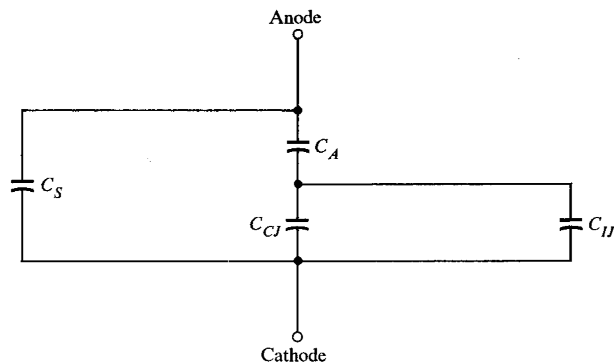
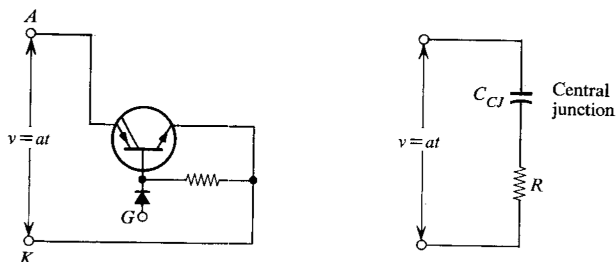


Figure 11 Equivalent circuit of the crosspoint in the OFF state.
Capacitances:
C_S = stray anode-substrate
C_A = anode junction
C_{IJ} = isolation junction
C_{CJ} = central junction

Figure 12 Rate-effect analysis.



$$v_R(t) = RC_{CJ}a(1 - e^{-t/RC_{CJ}}). \tag{10}$$

For $t \gg RC_{CJ}$,

$$v_R = RC_{CJ}a. \tag{11}$$

The SCR will trigger when $v_R = V_{BE}$ (0.6 to 0.7 V). Therefore the value of the slope of the ramp needed to produce triggering of the SCR is

$$a > \frac{V_{BE}}{RC_{CJ}}, \tag{12}$$

which is seen to be large if R is small[17] or if C_{CJ} is small. The rate-effect sensitivity will be somewhat higher than the lower limit given by Eq. (12) because of the frequency limitation of the npn and pnp transistors.[23]

In this design the substrate has been connected to the cathode.[17] This particular connection results in optimum rate-effect sensitivity since a capacitive current flowing through the isolation junction is shunted to the cathode

and does not enter the gate region. The substrate could also be connected to the gate region of the SCR. Such a connection would result in a smaller holding current; however, the rate-effect sensitivity would be degraded.

- *Switching speeds*

The switching speeds of this device are considerably higher than required for line switching applications. Typical turn-on and turn-off times are hundreds of nanoseconds and are typically governed by charge storage.

- *Summary of design considerations*

(1) The resistivity and thickness of the epitaxial layer are determined by breakover voltage requirements.
(2) OFF impedance and rate-effect sensitivity require that the area of the central junction be small. The ON resistance dictates a large central junction area. These two considerations call for a long, narrow structure.
(3) The substrate should be connected to the cathode to minimize rate-effect sensitivity.
(4) The doping of the buried n^+ layer should be as high as the technology will permit.
(5) The value of the shunting resistance determines the trade-offs between rate-effect sensitivity, holding current, and gate triggering current.

Process description

The major steps in the fabrication are conventional in integrated circuit manufacturing.

(1) Starting with a high-resistivity silicon wafer we form an n^+ subcollector using conventional diffusion, oxidation and photoresist techniques.
(2) n-type epitaxial layer is grown in which the SCR structure will be diffused.
(3) A p^+ isolation diffusion connected to the substrate delineates two areas, one for the SCR itself, and the other for the diode and the resistor.
(4) A boron diffusion is used to realize the p zones of the SCR (anode and gate), the resistance and the diode.
(5) A phosphorus diffusion will then form the cathode of the SCR and the ohmic contacts of the diode.
(6) The interconnection pattern is made by conventional methods of aluminum deposition.
(7) A glass passivation layer identical to that used in SLT is given to the device.[24]
(8) External metallization is used with the standard SLT processes.[25]

Several features such as field relief electrodes, an isolation junction surrounding the cathode, and double phosphorus glass, have been added in order to improve the reliability.

The device is then joined to a ceramic module using the SLT process, the basic module being composed of four elementary cells of 2 × 1 crosspoints. The encapsulated module is shown in Fig. 13.

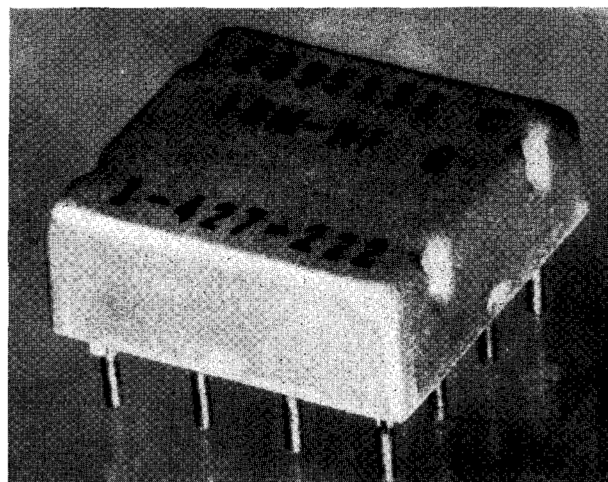


Figure 13 Encapsulated module.

Crosspoint characteristics

BV_{AK}	@ $I = 10\mu A$	> 35V
BV_{KA}	@ $I = 10\mu A$	> 35V
BV_{KG}	@ $I = 10\mu A$	> 35V
I_{AK}	@ $V = 3V$	< 100nA
I_{KA}	@ $V = 3V$	< 100nA
V_{ON}	@ $I = 30mA$	0.9 to 1.2V
R_{ON}	@ 800 Hz, $I = 30mA$	< 6Ω
I_{firing}		< 1.2mA
$I_{holding}$		< 4.5mA
C_{AK}	@ 0V	< 4pF
C_{GK}	@ 0V	< 2pF
T_{ON}		< 700ns
T_{OFF}		< 700ns
Rate effect		> 18V

Typical distributions of these parameters are shown on Fig. 14.

Conclusions

The design of a semiconductor crosspoint consisting of a SCR-diode-resistor circuit has been described. The central junction of the SCR should be small to maximize the OFF impedance and minimize the rate-effect sensitivity. The substrate should be connected to the cathode for minimum rate-effect sensitivity, as is now common practice in SCR design.[16] The value of the shunting resistance determines the trade-offs among rate-effect sensitivity, holding current, and gate triggering current.

The process employed here utilizes conventional chip fabrication and SLT packaging techniques. Eight crosspoints have been interconnected on a ceramic module to

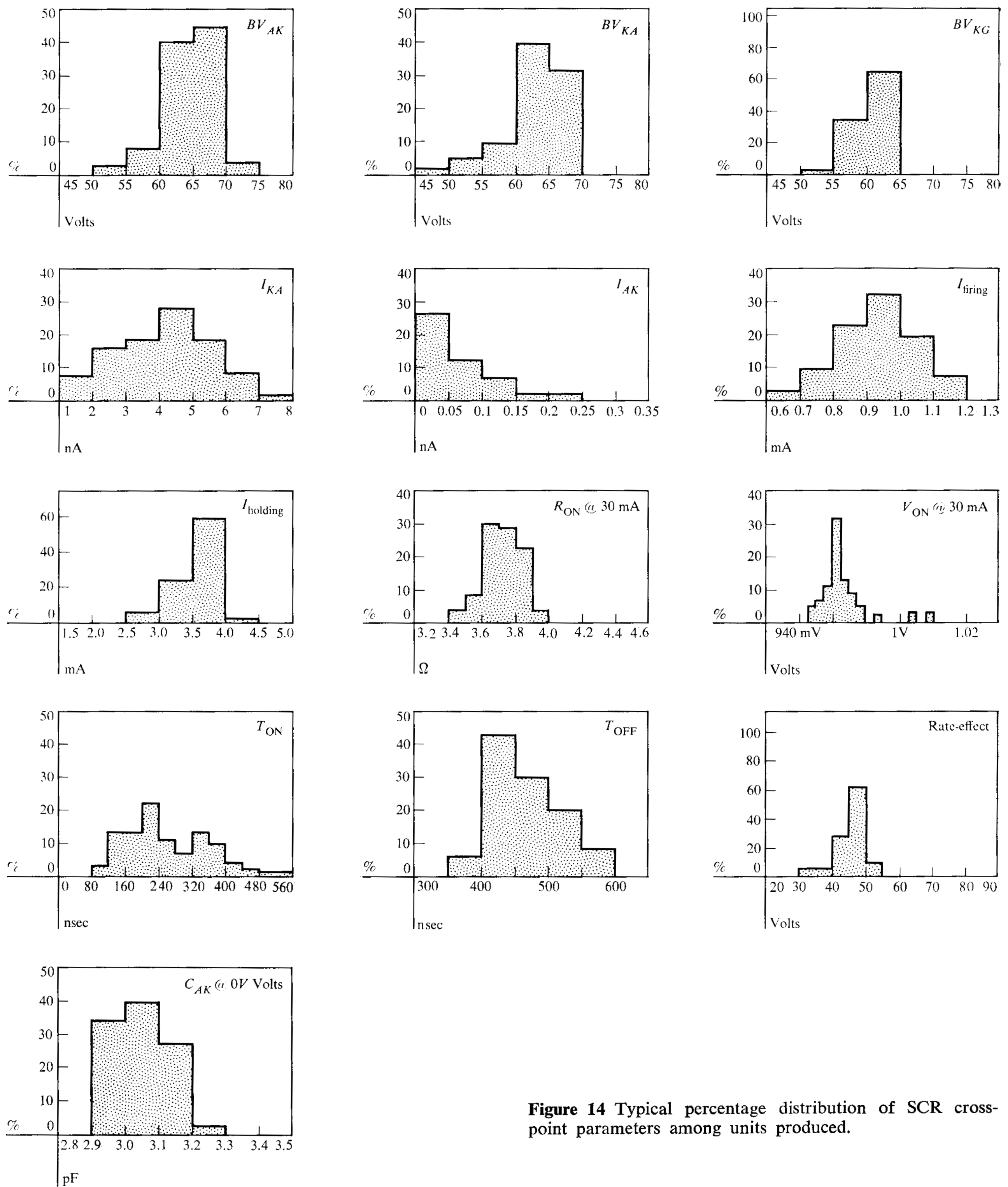


Figure 14 Typical percentage distribution of SCR crosspoint parameters among units produced.

form four elementary cells of two crosspoints each for use in line switching systems. These crosspoints have demonstrated an ON resistance of 3 to 4 ohms, a capacitance of 3.0 pF, and a breakdown voltage of 55 to 75 V.

The high performance, excellent reliability, and low cost which semiconductors have demonstrated in computer applications can now be utilized in line switching applications.

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