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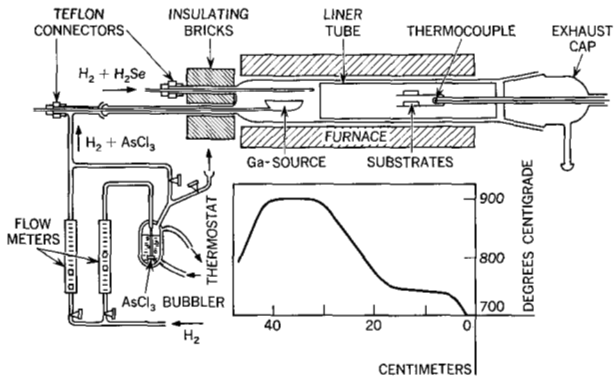
Gallium Arsenide Planar Technology

Abstract: Some of the main problems of the gallium arsenide planar technology are discussed. The most suitable starting material used has been obtained by vapor growth. Methods of zinc and tin diffusion have been studied in connection with masking by pyrolytic SiO_2/P_2O_5 layers. An alternative technique using doped silicon dioxide for the production of planar devices has been developed. The latter method features complete surface protection and easy control of the impurity concentration. The application of both methods to the production of *npn*, *pnp*, and four-layer devices is described. Using an epitaxial etch-refill technique it is possible to obtain electrically isolated devices on a common semi-insulating GaAs substrate.

Introduction

There are theoretical indications that gallium arsenide devices should be superior to germanium and silicon devices, because of the higher bandgap and the higher electron mobility of gallium arsenide. The availability of high-resistivity GaAs also suggests new methods for the design of integrated devices. On the other hand, the technology of gallium arsenide is more difficult and less advanced in comparison to that of elemental semiconductors. In the following, the main process steps for the fabrication of GaAs planar devices are described. These steps are epitaxial growth, diffusion from the vapor phase, and masking with silicon dioxide. The application of the solid-to-solid diffusion method which has been described in detail elsewhere[1,2] is also discussed briefly.

Figure 1 Apparatus for the epitaxial deposition of GaAs by the $Ga/AsCl_3$ process.



Epitaxial growth

Epitaxial layers of low doping level must be deposited on heavily doped substrates in order to obtain transistors with low collector capacitance and low collector series resistance. Since the active regions (emitter-to-base and base-to-collector junction) are built into the epitaxial layer, the quality of the epitaxially grown material will ultimately determine the limits of device performance.

The epitaxial deposition of GaAs by the $Ga/AsCl_3$ process yields a high quality material for device fabrication.[3,4] In this process, high-purity arsenic trichloride serves both as a transport agent for the gallium and as an arsenic source. Figure 1 shows a schematic diagram of the $Ga/AsCl_3$ epitaxial growth system and the temperature distribution during normal deposition.[5] In this system, the $AsCl_3$ dissociates at low temperatures (300–500°C):

$$4\ AsCl_3 + 6\ H_2 \rightarrow As_4 + 12\ HCl; \qquad (1)$$

and the resulting HCl chlorinates the gallium in the source boat:

$$2\ Ga + 2\ HCl \rightarrow 2\ GaCl + H_2. \qquad (2)$$

The arsenic at first goes into solution in the gallium:

$$4\ Ga + x\ As_4 \rightarrow 4\ GaAs_x \qquad (x < 1); \qquad (3)$$

and when this process is essentially complete, the arsenic remains in the vapor and reacts with the disproportionating GaCl to form GaAs in the deposition zone:

$$6\ GaCl + As_4 \rightarrow 4\ GaAs + 2\ GaCl_3. \qquad (4)$$

The operation of the $Ga/AsCl_3$ system must start with a saturation period. For this purpose, a flow-rate of 200 cc/min is maintained through the bubbler, the temperature

of which is held at 26°C during this period. Saturation of a 50-gram charge of Ga requires 6–10 hours under these conditions. It is difficult to judge when the process is complete, other than by attempting epitaxial growth to see if a reasonable growth rate is obtained. When a charge is saturated, it normally serves for 20–30 hours of epitaxial growth.

The substrates are cut from Czochralski-grown crystals (Se-doped, 10^{17} to 10^{18} electrons/cm^3) and chemically polished according to the technique described by Reisman and Rohr.[6] The wafers must undergo a re-etch treatment (0.7% NaOCl solution at 90°C), followed by a meticulous rinsing and drying operation just prior to insertion into the deposition system.

When the temperatures of source and seed zones have been stabilized at about 900 and 740°C, respectively, and the furnace has been thoroughly purged with H_2, the substrate wafers are pushed into the seed zone and allowed to heat up for five minutes under 1000 cc/min of pure H_2. The H_2 is then reduced to 200 cc/min and a 200 cc/min flow of $H_2/AsCl_3$ from the bubbler is mixed with it. The bubbler is held at 23.5°C, the vapor pressure of $AsCl_3$ being 10 Torr. This condition produces vapor etching of the substrates. It is allowed to proceed for 2 minutes, with removal of about 1 μm. Then the pure H_2 is shut off completely, and epitaxial growth begins. The deposition rate is about 30–40 μm/h. After growth for the required length of time, the pure H_2 is again turned on to 1000 cc/min, the $AsCl_3$ is shut off, and the system is flushed for about 5 minutes before the wafers are removed from the system.

Because of negligible growth on the reverse (111B) side, the thickness of (111A) layers can be measured quite accurately by weight change. "Talysurf" measurements reveal average deviations from planarity of about 0.05 μm for epitaxial growth on surfaces oriented between 0.5° and 1.5° off the (111A) plane.[5]

If the system is clean and no dopants are added intentionally, the layers are nearly always *n*-type, with an electron concentration normally in the low 10^{15} cm^{-3} range. *N*-type doping is achieved by adding a stream of H_2Se diluted in hydrogen (see Fig. 1). It is important to maintain a positive flow of hydrogen in the doping inlet at all times; otherwise gallium compounds may diffuse back and condense, thereby absorbing selenium from time to time and ruining the doping control.

From three-point measurements, it can be concluded that the doping level is uniform throughout the epitaxial layer, except for the interface region which appears to be more heavily doped, even on high-resistivity substrates.

Diffusion from the gas phase

A GaAs device technology can be established which is basically similar to the conventional silicon planar technique; i.e., the impurities forming *pn* junctions by diffusion at elevated temperatures are supplied from the gas phase, and SiO_2 (or SiO_2/P_2O_5) layers can serve for masking purposes. At the present state-of-the-art, the techniques of zinc and tin diffusion in GaAs are more advanced than the diffusion of any other impurity. Both *npn*- and *pnp*-structures can be produced with this pair of impurities.

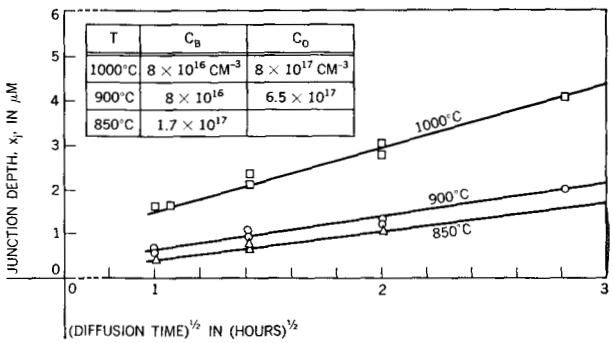


Figure 2 Junction depth vs square-root of diffusion time for Zn diffusion from 0.1% Zn/Ga source (C_B = bulk electron concentration, C_0 = surface hole concentration).

• *Low-concentration zinc diffusion*

An acceptor surface concentration in the low 10^{17} cm^{-3} range is required for the base region of *npn*-transistors. With a sealed tube diffusion utilizing a Zn/Ga alloy of proper composition, it is possible to achieve relatively low surface concentrations.[7] The addition of some arsenic (e.g., 0.1 mg As per cc ampoule volume) is helpful to avoid surface erosion. However, it is of particular importance to remove traces of oxidized arsenic by a heating cycle at 300°C before sealing the ampoules.

Results of a series of low-concentration zinc diffusion runs are shown in Fig. 2. The surface impurity concentration depends strongly on the concentration of Zn in Ga, but only slightly on the temperature. The diffusion coefficient at 1000°C with a 0.1% Zn/Ga source is $D = 1.2 \times 10^{-12}$ cm^2/sec. There are indications, however, that the diffusion coefficient also depends on the concentration of crystal imperfections, with higher diffusion rates in less perfect material.[8]

• *High-concentration zinc diffusion*

For *pnp* double-diffused transistors, an emitter diffusion with high surface concentration is desirable. A source of pure $ZnAs_2$ can be used for this purpose. The advantage of $ZnAs_2$ as an impurity source is that the amount of source material in the capsule has no significant influence on the diffusion[9] results in the range of 0.2 to 5 mg/cc.

Results of high-concentration zinc diffusion experiments for the temperature range from 650 to 800°C are plotted in Fig. 3. The surface hole concentration is close to

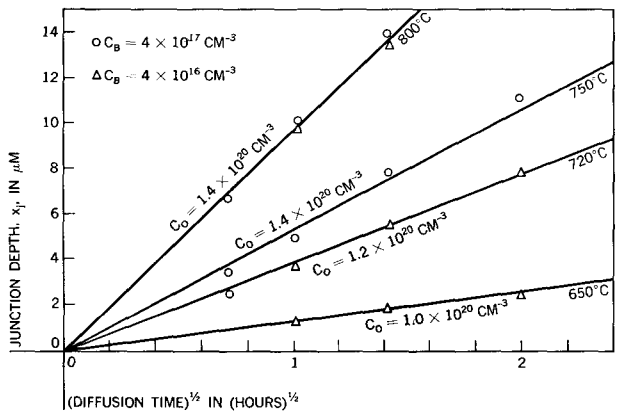


Figure 3 Junction depth vs square-root of diffusion time for Zn diffusion from $ZnAs_2$ source (C_B = bulk electron concentration, C_0 = surface hole concentration).

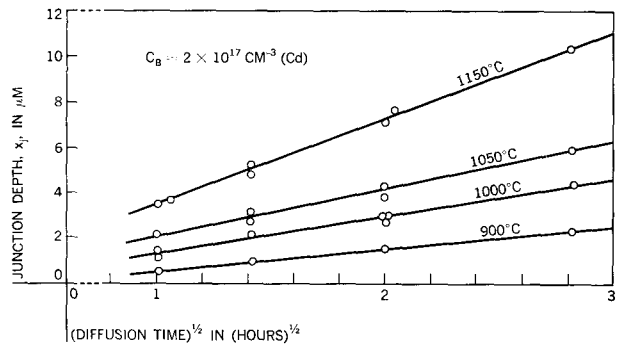


Figure 4 Junction depth vs square-root of diffusion time for Sn diffusion (C_B = bulk hole concentration).

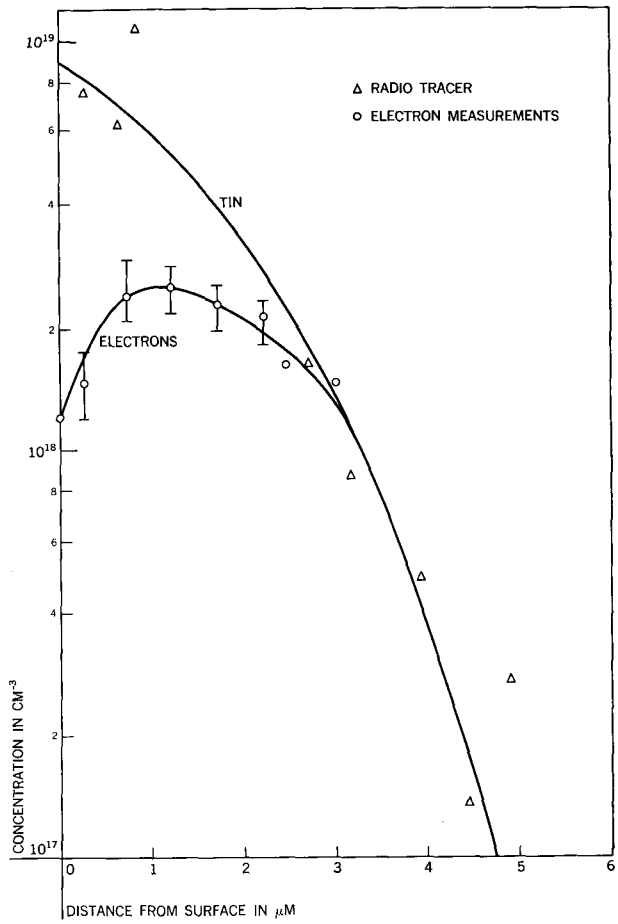


Figure 5 Example of tin and electron concentration profile after tin diffusion.

10^{20} cm^{-3} and varies only slightly with diffusion temperature.[8] As reported in the literature, the acceptor concentration profile approaches a step-function, due to an interstitial-substitutional diffusion mechanism.[10] This is helpful in obtaining a high emitter efficiency in *pnp* devices.

- *Tin diffusion*

In the present state of the art, tin is considered to be more convenient for donor diffusion than the Group VI elements since there is no chemical reaction between tin and gallium arsenide. Tin diffusion is performed in sealed ampoules with elemental tin as impurity source. In order to avoid surface erosion during tin diffusion, the wafers should be sandwiched between quartz flats, as described by Fane and Goss.[11] Normally, an arsenic pressure of 1 atm is maintained during the diffusion. Again it is important to remove any traces of oxidized arsenic before sealing the ampoules.

The junction depths for various tin diffusions between 900 and 1150°C are plotted vs square root of time in Fig. 4. The surface concentration, measured by radiotracer methods, is independent of the diffusion temperature within the experimental error ($C_0 = 10^{19}$ cm^{-3}). Figure 5 is a comparison between the tin concentration profile and the carrier concentration profile, determined by differential sheet resistivity and Hall measurements.[12] Figure 5 indicates that the maximum carrier concentration is 3×10^{18} cm^{-3}, with a slight decrease near the surface.

The junction depths revealed by staining and beveling techniques are generally somewhat smaller than those determined by radiotracer methods. Similar discrepancies have also been reported by other authors.[11]

- *Masking*

Silicon dioxide is a convenient diffusion mask for GaAs devices based on the sophisticated photolithography which already exists for the silicon planar technology. The deposition of SiO_2 on GaAs can be performed by means of pyrolytic decomposition of alkoxysilanes at sufficiently low temperatures (e.g., 700°C).[13] Due to thermal mismatch between SiO_2 and GaAs, however, the silicon dioxide layers tend to crack if their thicknesses exceed about

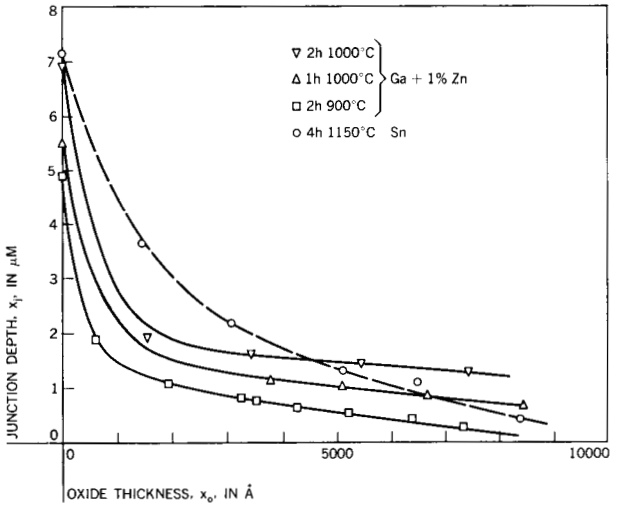
6000 Å.* The masking efficiency of pyrolytic SiO_2 layers has been studied by etching steps of different thickness into the oxide. The wafers were then subjected to an impurity diffusion process. In Fig. 6, the junction depth vs oxide thickness for different conditions of Zn diffusion is plotted. For instance, complete masking ($x_j = 0$) would require an oxide thickness of 9000 Å for a 2 h diffusion at 900°C. Because crack-free SiO_2 layers exceeding 6000 Å can hardly be obtained, reliable masking against Zn diffusion is impossible with the diffusion conditions indicated in Fig. 6. With slightly relaxed conditions (e.g., 1 h, 850°C) SiO_2 masking is just marginal. In fact, the very first *npn* transistors of this work were obtained using pure SiO_2 masking.

The masking efficiency of SiO_2 against tin diffusion is somewhat better. The dashed curve in Fig. 6 shows a masking experiment with a very severe tin diffusion condition (1150°C, 4 h). Masking for the emitter diffusion of *npn* devices (1000°C, 1–2 h) is feasible with pure SiO_2, but again the margin for the oxide thickness is not very large.

A considerably higher masking efficiency, especially against zinc diffusion, is achieved with SiO_2/P_2O_5-glass, as suggested by Flatley et al.[15] This glass can be produced by simultaneous pyrolytic decomposition of tetraethylsilicate and trimethylphosphate. For the tin diffusion, it is advantageous to avoid direct contact between GaAs and SiO_2/P_2O_5 glass by growing a thin, pure SiO_2 layer on the GaAs before switching to the glass deposition.

* On the (111) oriented substrate, the cracks are parallel to the ⟨211⟩ direction, the width being 0.5 to 1 μm. It has been suggested that use be made of these cracks for special device applications.[14]

Figure 6 Junction depth vs thickness of masking SiO_2 (bulk concentration for Zn-diffusion experiments: $n = 2 \times 10^{17}$ cm^{-3}, for Sn-diffusion experiment: $p = 7 \times 10^{17}$ cm^{-3}).



Diffusion from doped silicon dioxide layers

Although the conventional scheme of diffusion from the gas phase and SiO_2 masking can be applied to the GaAs planar technology, it is likely that the solid-to-solid diffusion method may be preferred in the future. In this technique, an appropriately doped solid layer is deposited on the semiconductor and serves as the dopant source during the diffusion cycle. Complete surface protection can be achieved in this manner, since no contact with a gaseous ambient is required.

Doped silicon dioxide layers are convenient to use as impurity sources, since the conventional photoresist techniques can be applied. Fortunately both tin and zinc have a sufficient diffusivity in silicon dioxide, as required for the solid-to-solid diffusion method.

The deposition of zinc-doped silicon dioxide on gallium arsenide by simultaneous reactive sputtering of silicon and zinc has been suggested by Shortes et al.[16] However, methods based on pyrolytic decomposition of suitable compounds seem more versatile and give more reliable doping control.

• *Tin diffusion from doped SiO_2*

Tin-doped silicon dioxide layers can be produced by adding a small amount of tetraethyltin to the tetraethylsilicate reservoir serving for the gas saturation in the conventional pyrolytic deposition equipment for silicon dioxide.[1] The vapor pressures of these two compounds are close enough to prevent significant variations in the doping level due to segregation.

The total amount of impurity atoms available for diffusion into the GaAs is determined by the impurity level in the oxide and the thickness of the oxide layer. However, only a certain fraction actually enters the gallium arsenide, depending on the experimental conditions. With a relatively thick oxide layer an "infinite source" condition can be obtained. The impurity concentration profile in the GaAs is then given by

$$C(x) = \frac{kC_0}{1 + k\sqrt{D/D_0}} \operatorname{erfc}\,(x/2\sqrt{Dt}), \qquad (5)$$

where k = segregation coefficient, C_0 = initial impurity concentration in SiO_2, D = diffusion constant in GaAs, and D_0 = diffusion constant in SiO_2. For a given C_0 the junction depth depends only on the diffusion time and the temperature.

With a smaller thickness of the doped layer a "finite source" condition may be established. The impurity profile then approaches a Gaussian distribution, with the surface concentration and the junction depth also depending on the thickness of the source layer.

Figure 7 shows the results of tin diffusion experiments at 1000°C with source layers having an impurity concentra-

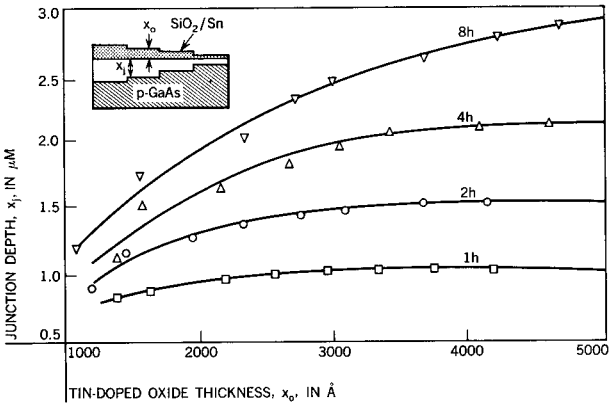


Figure 7 Junction depth vs thickness of Sn-doped SiO_2 layer (diffusion at 1000°C, bulk concentration: $p = 2.5 \times 10^{17}$ cm^{-3}).

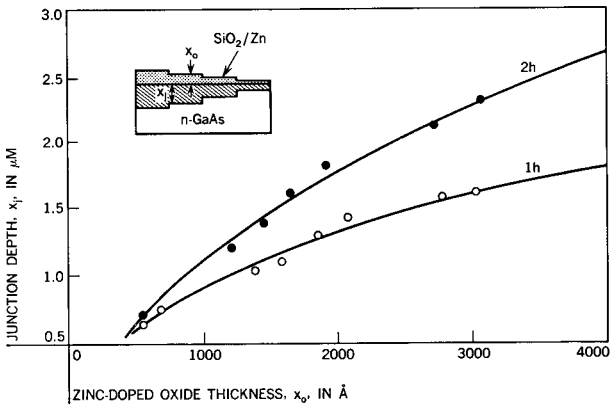


Figure 8 Junction depth vs thickness of Zn-doped SiO_2 layer (diffusion at 1000°C, bulk concentration $n = 2 \times 10^{17}$ cm^{-3}).

tion of 6×10^{18} cm^{-3}. For a diffusion time of 1 hour, the junction depth is nearly independent of the oxide thickness, which is indicative of the "infinite source" condition. A noticeable influence of the oxide thickness is seen for diffusion experiments at two, four and eight hours; this effect is apparently due to increasing source depletion during the diffusion.

- *Zinc diffusion from doped SiO_2*

The production of zinc-doped layers is rendered difficult by the fact that commercially available organometallic zinc compounds, such as diethylzinc, are spontaneously inflammable on contact with air. Diethylzinc also reacts with tetraethylsilicate at room temperature. It is, therefore, diluted in *n*-heptane and introduced through a separate saturator, the vapors being mixed immediately before entering the deposition furnace.[1]

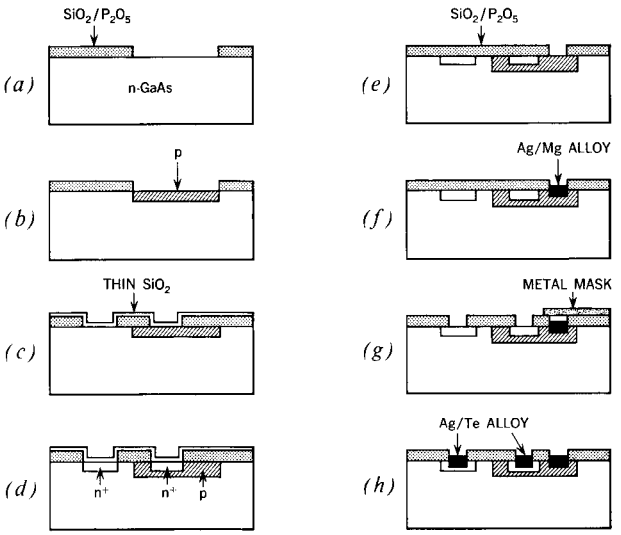
Due to the higher diffusivity of zinc in silicon dioxide and in gallium arsenide (as compared with tin at the same temperature), the "infinite source" condition can hardly be achieved with zinc at 1000°C. The dependence of the junction depth on oxide thickness is enhanced by the fact that the zinc diffusion constant decreases at lower zinc concentrations. A slightly lower surface concentration, due to partial source depletion, may therefore reduce the junction depth drastically. It is seen from Fig. 8 that there is a considerable variation in the junction depth with the oxide thickness, even at a diffusion time as low as one hour.

Planar devices

- *npn transistors*

There is only a small range for the doping level of the starting material for double-diffused *npn* devices. Lightly doped *n*-type material tends to convert during the diffusion heat-treatment. Hence, a lower doping limit will be in the

Figure 9 Production steps for planar *npn* transistors by diffusion from the gas phase.



low to medium 10^{16} cm^{-3} range, depending on the preparation of the material. Since the carrier concentration obtainable with tin diffusion in the emitter region is limited to about 3×10^{18} cm^{-3} the base donor concentration must not exceed 5×10^{17} cm^{-3} in order to get a reasonable emitter efficiency. This sets an upper limit of about $n = 10^{17}$ cm^{-3} for the collector region.

The base and emitter regions can be formed either by diffusion from the gas phase or by solid-to-solid diffusion. A combination of both methods is feasible, too.[17]

Figure 9 shows the main steps for the fabrication of *npn* transistors by gaseous diffusion. Masking for the base diffusion is accomplished by pyrolytic SiO_2 layers (5000 Å) containing about 5 to 6% phosphorous (Figs. 9a, b). The

Table 1. Diffusion conditions for *npn* transistors (sealed tube, 20 cm³)

	Source in mg	*Arsenic in mg*	*Temperature in °C*	*Time in min*	*Junction depth in μm*
Base	12, 0.1% Zn/Ga	2.5	850–900	45–120	0.6–0.8 (1.2–1.4 after emitter diffusion)
Emitter	12, Sn	40	1000	30–120	0.8–1.0

diffusion conditions are listed in Table 1. As previously mentioned, the quality of the starting material has some influence on the low-concentration zinc diffusion.

The masking oxide is stripped after the base diffusion and a thin layer of the GaAs (about 0.2 μm) is removed before the deposition of SiO_2/P_2O_5 for emitter masking. The areas exposed to the tin diffusion are protected by a very thin (500 Å) SiO_2 layer which is permeable to the diffusant at the diffusion conditions involved (Figs. 9c, d). During the emitter diffusion the base-collector junction moves further into the bulk. The base width is about 0.4 μm.

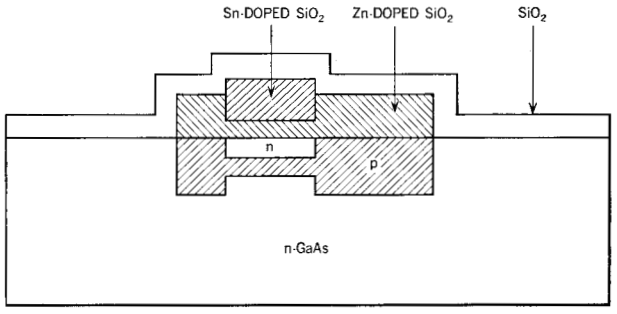
On the completed diffused *npn* structure ohmic contacts are provided by evaporation of Ag+2% Mg (base contact) and Ag+1% Te (emitter contact), with simultaneous alloying at 620°C. In order to avoid impurity compensation, the base contact is shielded by a metal mask during evaporation of the emitter contact alloy (Fig. 9g). For transistors requiring lands on top of the SiO_2 layer, it is necessary to improve the adhesion by forming a chromium pattern before the silver evaporation.[18]

The solid-to-solid diffusion method is of particular interest for the base diffusion of *npn* devices since it allows convenient control of the doping level in the required range ($\sim 10^{17}$ cm^{-3}). Simultaneously, a deeper, heavily doped region can be formed around the emitter in contact with the base area.[2] This reduces the base resistance and facilitates alloying of the ohmic base contact.

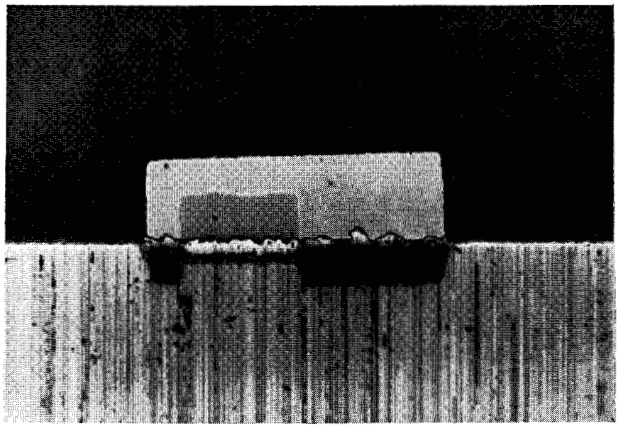
With the solid-to-solid diffusion technique it is possible to produce *npn* transistors also by a single-step diffusion.[2] An appropriate pattern of doped silicon dioxide is required for this process (Fig. 10a). A relatively thick Zn-doped layer provides the acceptors for the base contact and the area surrounding the emitter. The diffusion source for the active *npn* region comprises a thin Zn-doped layer, which is depleted during diffusion, and a thick Sn-doped layer. Finally, a thin protective SiO_2 layer is added. A single diffusion cycle then produces the complete *npn* transistor (Fig. 10b).

Most of the data on device performance presently available are taken from *npn* transistors produced by the gaseous diffusion method, using epitaxial layers and also bulk *n*-type material.

Figure 10 (a) Production of planar *npn* transistors by single-step diffusion from doped SiO_2. (b) Bevel through *npn* transistor obtained by single-step diffusion.



(a)



(b)

The collector-to-base breakdown voltage is normally in the range of 15 to 40 V. The breakdown characteristics are generally very sharp. Reverse currents are in the nanoampere region, but no special attention has been given to the low current performance. The emitter-to-base breakdown voltages are rather high, ranging between 8 and 15 V.

According to different experimental conditions and different materials used in our experiments, a wide spread

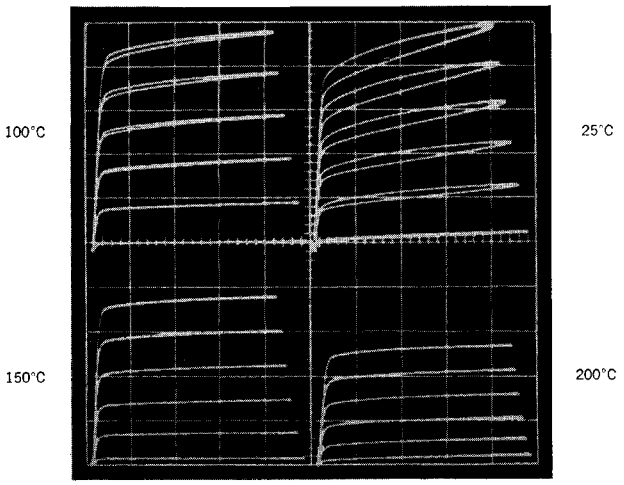


Figure 11 Common-emitter characteristics (I_C vs V_{CE}) of *npn* transistors at different temperatures. (Vertical scale: 1 mA/div; horizontal scale: 2 V/div; the parameter is I_B in 0.1 mA/step).

of values for the small-signal current amplification is observed. Maximum beta-values after metallization are the following:

	Material			
	Float-zone	*Czochralski*	*Boat-grown*	*Epitaxial*
β	15	20	55	70

A major drawback of present GaAs transistors is poor high-frequency performance. With a base-width of 0.4 μm one would expect a cutoff frequency well beyond 1 GHz. However, typical f_T values observed in this study are in the 100–300 MHz range. Most of the high-beta units also show hysteresis effects when the characteristics are displayed at 50 Hz. An example shown in Fig. 11, demonstrates the disappearance of the loops at higher temperatures. It is likely that the limitations in frequency response are due to trapping effects within the collector junction.

- *pnp transistors*

Due to the high electron/hole mobility ratio and the low carrier lifetime in GaAs, it is difficult to produce GaAs *pnp* transistors. In order to obtain a reasonable emitter efficiency and a transport factor close to unity, the doping ratio of the emitter region to the base region must be >200, and the base-width should not exceed 0.1 μm.

The first *pnp* devices with beta greater than unity have been obtained by diffusion from the gas phase.[19] The base region is formed by Sn diffusion (as described for the emitter of *npn* devices) and a high-concentration Zn diffusion process (with $ZnAs_2$ source) yields the emitter.

The very thin base width often causes small emitter-collector shorts so that the characteristics are shunted by leakage currents. This problem is all the more severe the higher the beta and hence the thinner the base width. For these *pnp* devices the maximum beta values which have been obtained with reasonable leakage currents (<0.1 mA at $V_{EC} = 2$V) are in the order of 5.

Replacing gaseous tin diffusion by a solid-to-solid diffusion process has made it possible to obtain smaller base concentrations. The resulting *pnp* devices have higher beta values (up to 10) with moderate leakage currents.[2] It appears that *pnp* transistors are superior to *npn* devices with respect to the transient behavior. The f_T values are in the range of 500–700 MHz, and there are no loops in the characteristics displayed at 100 Hz. This is probably due to the higher doping levels involved in *pnp* devices (i.e. relatively smaller influence of traps).

- *Four-layer devices*

The main difficulty in producing GaAs four-layer transistors is caused by the low lifetime of the minority carriers. It is necessary to form three *pn* junctions within a distance of a few tenths of a micron. With a proper combination of the diffusion processes described above for *npn* and *pnp* transistors, it has been possible to obtain four-layer devices exhibiting characteristics which are typical for *pnpn* switches.[20]

- *Isolated transistors*

High-resistivity GaAs can be used as an insulating substrate for integrated circuitry. For instance, an array of *n*-doped islands can be produced by epitaxial deposition into cavities in semi-insulating GaAs. With careful process control it is possible to obtain surface planarity within 1 μm. The wafers are then processed in the usual manner to form an *npn* transistor in each of the islands. A mounted chip with four isolated transistors is shown in Fig. 12. The characteristics of these devices are comparable to others made from epitaxial material.[21]

Conclusions

The feasibility of producing *npn*, *pnp* and four-layer devices by means of the planar gallium arsenide technology has been demonstrated. In addition, isolated devices can be obtained on high-resistivity gallium arsenide with the epitaxial etch-refill method.

It is possible to produce *npn* transistors with beta values in the range of 20–30 with reasonable yield. The devices, however, fall short with respect to high-frequency performance as compared to theoretical predictions from mobility data. Trapping effects are dominant with most of the GaAs material presently available; these pose formidable limitations to large-scale device fabrication with GaAs. Improvements have to be sought mainly along the

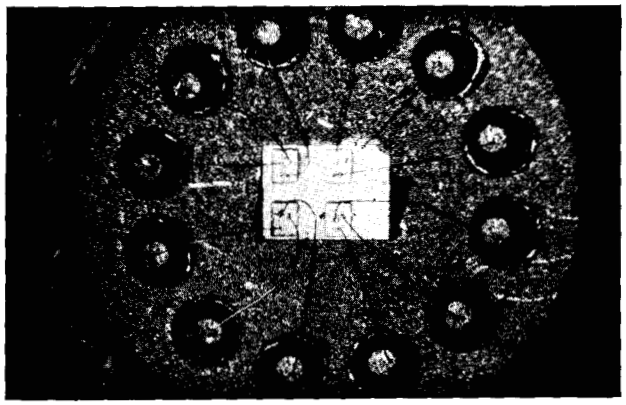


Figure 12 Chip with four isolated transistors on high-resistivity GaAs substrate.

lines of materials preparation and understanding of defects introduced during various process steps.

Some experiments on *pnp* transistors show promising results, mainly with respect to high-frequency performance. However, further refinement in the technology is required in order to obtain *pnp* devices with useful current amplification.

Acknowledgment

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