IBM System/360 Reference Data

NAME	MNEMONIC	TYPE	CODE	OPERAND
Add	AR	RR	1A	R1, R2
Add	A	RX	5A	R1, D2 (X2, B2)
Add Halfword	AH	RX	4A	R1, D2 (X2, B2)
Add Logical	ALR	RR	1E	R1, R2
Add Logical	AL	RX	5E	R1, D2 (X2, B2)
AND	NR	RR	14	R1, R2
AND	N	RX	54	R1, D2 (X2, B2)
AND	NI	SI	94	D1 (B1), I2
AND	NC	SS	D4	D1 (L, B1), D2 (B2)
Branch and Link	BALR	RR	05	R1, R2
Branch and Link	BAL	RX	45	R1, D2 (X2, B2)
Branch on Condition	BCR	RR	07	M1, R2
Branch on Condition	BC	RX	47	M1, D2 (X2, B2)
Branch on Count	BCTR	RR	06	R1, R2
Branch on Count	BCT	RX	46	R1, D2 (X2, B2)
Branch on Index High	BXH	RS	86	R1, R3, D2 (B2)
Branch on Index Low or Equal	BXLE	RS	87	R1, R3, D2 (B2)
Compare	CR	RR	19	R1, R2
Compare	C	RX	59	R1, D2 (X2, B2)
Compare Halfword	CH	RX	49	R1, D2 (X2, B2)
Compare Logical	CLR	RR	15	R1, R2
Compare Logical	CL	RX	55	R1, D2 (X2, B2)
Compare Logical	CLC	SS	D5	D1 (L, B1), D2 (B2)
Compare Logical	CLI	SI	95	D1 (B1), I2
Convert to Binary	CVB	RX	4F	R1, D2 (X2, B2)
Convert to Decimal	CVD	RX	4E	R1, D2 (X2, B2)
Diagnose		SI	83	
Divide	DR	RR	1D	R1, R2
Divide	D	RX	5D	R1, D2 (X2, B2)
Exclusive OR	XR	RR	17	R1, R2
Exclusive OR	X	RX	57	R1, D2 (X2, B2)
Exclusive OR	XI	SI	97	D1 (B1), I2
Exclusive OR	XC	SS	D7	D1 (L, B1), D2 (B2)
Execute	EX	RX	44	R1, D2 (X2, B2)
Halt I/O	HIO	SI	9E	D1 (B1)
Insert Character	IC	RX	43	R1, D2 (X2, B2)
Load	LR	RR	18	R1, R2
Load	L	RX	58	R1, D2 (X2, B2)
Load Address	LA	RX	41	R1, D2 (X2, B2)
Load and Test	LTR	RR	12	R1, R2
Load Complement	LCR	RR	13	R1, R2
Load Halfword	LH	RX	48	R1, D2 (X2, B2)
Load Multiple	LM	RS	98	R1, R3, D2 (B2)
Load Negative	LNR	RR	11	R1, R2
Load Positive	LPR	RR	10	R1, R2
Load PSW	LPSW	SI	82	D1 (B1)
Move	MVI	SI	92	D1 (B1), I2
Move	MVC	SS	D2	D1 (L, B1), D2 (B2)
Move Numerics	MVN	SS	D1	D1 (L, B1), D2 (B2)
Move with Offset	MVO	SS	F1	D1 (L1, B1), D2 (L2, B2)
Move Zones	MVZ	SS	D3	D1 (L, B1), D2 (B2)
Multiply	MR	RR	1C	R1, R2
Multiply	M	RX	5C	R1, D2 (X2, B2)
Multiply Halfword	MH	RX	4C	R1, D2 (X2, B2)
OR	OR	RR	16	R1, R2
OR	O	RX	56	R1, D2 (X2, B2)
OR	OI	SI	96	D1 (B1), I2
OR	OC	SS	D6	D1 (L, B1), D2 (B2)
Pack	PACK	SS	F2	D1 (L1, B1), D2 (L2, B2)
Set Program Mask	SPM	RR	04	R1
Set System Mask	SSM	SI	80	D1 (B1)
Shift Left Double	SLDA	RS	8F	R1, D2 (B2)
Shift Left Single	SLA	RS	8B	R1, D2 (B2)
Shift Left Double Logical	SLDL	RS	8D	R1, D2 (B2)
Shift Left Single Logical	SLL	RS	89	R1, D2 (B2)
Shift Right Double	SRDA	RS	8E	R1, D2 (B2)

STANDARD INSTRUCTION SET (Continued)

Shift Right Single	SRA	RS	8A	R1, D2 (B2)
Shift Right Double				
Logical	SRDL	RS	8C	R1, D2 (B2)
Shift Right Single				
Logical	SRL	RS	88	R1, D2 (B2)
Start I/O	SIO	SI	9C	D1 (B1)
Store	ST	RX	50	R1, D2 (X2, B2)
Store Character	STC	RX	42	R1, D2 (X2, B2)
Store Halfword	STH	RX	40	R1, D2 (X2, B2)
Store Multiple	STM	RS	90	R1, R3, D2 (B2)
Subtract	SR	RR	1B	R1, R2
Subtract	S	RX	5B	R1, D2 (X2, B2)
Subtract Halfword	SH	RX	4B	R1, D2 (X2, B2)
Subtract Logical	SLR	RR	1F	R1, R2
Subtract Logical	SL	RX	5F	R1, D2 (X2, B2)
Supervisor Call	SVC	RR	0A	I
Test and Set	TS	SI	93	D1 (B1)
Test Channel	TCH	SI	9F	D1 (B1)
Test I/O	TIO	SI	9D	D1 (B1)
Test Under Mask	TM	SI	91	D1 (B1), I2
Translate	TR	SS	DC	D1 (L, B1), D2 (B2)
Translate and Test	TRT	SS	DD	D1 (L, B1), D2 (B2)
Unpack	UNPK	SS	F3	D1 (L1, B1), D2 (L2, B2)

DECIMAL FEATURE INSTRUCTIONS

Add Decimal	AP	SS	FA	D1 (L1, B1), D2 (L2, B2)
Compare Decimal	CP	SS	F9	D1 (L1, B1), D2 (L2, B2)
Divide Decimal	DP	SS	FD	D1 (L1, B1), D2 (L2, B2)
Edit	ED	SS	DE	D1 (L, B1), D2 (B2)
Edit and Mark	EDMK	SS	DF	D1 (L, B1), D2 (B2)
Multiply Decimal	MP	SS	FC	D1 (L1, B1), D2 (L2, B2)
Subtract Decimal	SP	SS	FB	D1 (L1, B1), D2 (L2, B2)
Zero and Add	ZAP	SS	F8	D1 (L1, B1), D2 (L2, B2)

DIRECT CONTROL FEATURE INSTRUCTIONS

Read Direct	RDD	SI	85	D1 (B1), I2
Write Direct	WRD	SI	84	D1 (B1), I2

PROTECTION FEATURE INSTRUCTIONS

Insert Storage Key	ISK	RR	09	R1, R2
Set Storage Key	SSK	RR	08	R1, R2

BASIC INSTRUCTION FORMATS

FIRST HALFWORD	SECOND HALFWORD	THIRD HALFWORD

RR FORMAT — REGISTER OPERANDS 1 2

OP CODE	R₁	R₂

$$0 \quad\quad 7\,8 \quad\quad 11\,12 \quad\quad 15$$

RX FORMAT — REGISTER OPERAND 1, STORAGE OPERAND 2

OP CODE	R₁	X₂	B₂	D₂

$$0 \quad 7\,8 \quad 11\,12 \quad 15\,16 \quad 19\,20 \quad 31$$

RS FORMAT — REGISTER OPERANDS 1 3, STORAGE OPERAND 2

OP CODE	R₁	R₃	B₂	D₂

$$0 \quad 7\,8 \quad 11\,12 \quad 15\,16 \quad 19\,20 \quad 31$$

SI FORMAT — IMMEDIATE OPERAND 2, STORAGE OPERAND 1

OP CODE	I₂	B₁	D₁

$$0 \quad 7\,8 \quad 15\,16 \quad 19\,20 \quad 31$$

SS FORMAT — L, STORAGE OPERAND 1, STORAGE OPERAND 2

OP CODE	L₁	L₂	B₁	D₁	B₂	D₂

$$0 \quad 7\,8 \quad 11\,12 \quad 15\,16 \quad 19\,20 \quad 31 \quad\quad 47$$

FLOATING-POINT FEATURE INSTRUCTIONS

Add Normalized (Long)	ADR	RR	2A	R1, R2
Add Normalized (Long)	AD	RX	6A	R1, D2 (X2, B2)
Add Normalized (Short)	AER	RR	3A	R1, R2
Add Normalized (Short)	AE	RX	7A	R1, D2 (X2, B2)
Add Unnormalized (Long)	AWR	RR	2E	R1, R2
Add Unnormalized (Long)	AW	RX	6E	R1, D2 (X2, B2)
Add Unnormalized (Short)	AUR	RR	3E	R1, R2
Add Unnormalized (Short)	AU	RX	7E	R1, D2 (X2, B2)
Add Normalized (Extended)	* AXR	RR	36	R1, R2
Compare (Long)	CDR	RR	29	R1, R2
Compare (Long)	CD	RX	69	R1, D2 (X2, B2)
Compare (Short)	CER	RR	39	R1, R2
Compare (Short)	CE	RX	79	R1, D2 (X2, B2)
Divide (Long)	DDR	RR	2D	R1, R2
Divide (Long)	DD	RX	6D	R1, D2 (X2, B2)
Divide (Short)	DER	RR	3D	R1, R2
Divide (Short)	DE	RX	7D	R1, D2 (X2, B2)
Halve (Long)	HDR	RR	24	R1, R2
Halve (Short)	HER	RR	34	R1, R2
Load and Test (Long)	LTDR	RR	22	R1, R2
Load and Test (Short)	LTER	RR	32	R1, R2
Load Complement (Long)	LCDR	RR	23	R1, R2
Load Complement (Short)	LCER	RR	33	R1, R2
Load (Long)	LDR	RR	28	R1, R2
Load (Long)	LD	RX	68	R1, D2 (X2, B2)
Load Negative (Long)	LNDR	RR	21	R1, R2
Load Negative (Short)	LNER	RR	31	R1, R2
Load Positive (Long)	LPDR	RR	20	R1, R2
Load Positive (Short)	LPER	RR	30	R1, R2
Load (Short)	LER	RR	38	R1, R2
Load (Short)	LE	RX	78	R1, D2 (X2, B2)
Load Rounded (Extended to Long)	* LRDR	RR	25	R1, R2
Load Rounded (Long to Short)	* LRER	RR	35	R1, R2
Multiply (Long)	MDR	RR	2C	R1, R2
Multiply (Long)	MD	RX	6C	R1, D2 (X2, B2)
Multiply (Short)	MER	RR	3C	R1, R2
Multiply (Short)	ME	RX	7C	R1, D2 (X2, B2)
Multiply (Extended)	* MXR	RR	26	R1, R2
Multiply (Long/Extended)	* MXDR	RR	27	R1, R2
Multiply (Long/Extended)	* MXD	RX	67	R1, D2 (X2, B2)
Store (Long)	STD	RX	60	R1, D2 (X2, B2)
Store (Short)	STE	RX	70	R1, D2 (X2, B2)
Subtract Normalized (Long)	SDR	RR	2B	R1, R2
Subtract Normalized (Long)	SD	RX	6B	R1, D2 (X2, B2)
Subtract Normalized (Short)	SER	RR	3B	R1, R2
Subtract Normalized (Short)	SE	RX	7B	R1, D2 (X2, B2)
Subtract Unnormalized (Long)	SWR	RR	2F	R1, R2
Subtract Unnormalized (Long)	SW	RX	6F	R1, D2 (X2, B2)
Subtract Unnormalized (Short)	SUR	RR	3F	R1, R2
Subtract Unnormalized (Short)	SU	RX	7F	R1, D2 (X2, B2)
Subtract Normalized (Extended)	* SXR	RR	37	R1, R2

* extended floating point instructions, special feature.

CHARACTERISTICS FOR CONSTANTS

Code	Type	Machine Format
C	Character	8-Bit Code for each Character
X	Hexadecimal	4-Bit Code for each Hexadecimal Digit
B	Binary	Binary Digits (ones and zeros)
F	Fixed-point	Signed, Fixed-point Binary Format; Normally a Full Word
H	Fixed-point	Signed, Fixed-point Binary Format; Normally a Half Word
E	Floating-point	Short Floating-point Format; Normally a Full Word
D	Floating-point	Long Floating-point Format; Normally a Double Word
P	Decimal	Packed Decimal Format
Z	Decimal	Zoned Decimal Format
A	Address	Value of Address; Normally a Full Word
V	Address	Space Reserved for External Symbol Addresses; Each Address Normally a Full Word
S	Address	Address in Base Displacement Form
Y	Address	Value of Address; Normally a Half Word

EXTENDED MNEMONIC INSTRUCTION CODES

GENERAL

Extended Code		Machine Instruction		Meaning
B	D2(X2,B2)	BC	15, D2(X2,B2)	Branch Unconditionally
BR	R2	BCR	15, R2	Branch Unconditionally
NOP	D2(X2,B2)	BC	0, D2(X2,B2)	No Operation
NOPR	R2	BCR	0, R2	No Operation (RR)

AFTER COMPARE INSTRUCTIONS (A:B)

BH	D2(X2,B2)	BC 2,	D2(X2,B2)	Branch on A High
BL	D2(X2,B2)	BC 4,	D2(X2,B2)	Branch on A Low
BE	D2(X2,B2)	BC 8,	D2(X2,B2)	Branch on A Equal B
BNH	D2(X2,B2)	BC 13,	D2(X2,B2)	Branch on A Not High
BNL	D2(X2,B2)	BC 11,	D2(X2,B2)	Branch on A Not Low
BNE	D2(X2,B2)	BC 7,	D2(X2,B2)	Branch on A Not Equal B

AFTER ARITHMETIC INSTRUCTIONS

BO	D2(X2,B2)	BC 1,	D2(X2,B2)	Branch on Overflow
BP	D2(X2,B2)	BC 2,	D2(X2,B2)	Branch on Plus
BM	D2(X2,B2)	BC 4,	D2(X2,B2)	Branch on Minus
BZ	D2(X2,B2)	BC 8,	D2(X2,B2)	Branch on Zero
BNP	D2(X2,B2)	BC 13,	D2(X2,B2)	Branch on Not Plus
BNM	D2(X2,B2)	BC 11,	D2(X2,B2)	Branch on Not Minus
BNZ	D2(X2,B2)	BC 7,	D2(X2,B2)	Branch on Not Zero

AFTER TEST UNDER MASK INSTRUCTIONS

BO	D2(X2,B2)	BC 1,	D2(X2,B2)	Branch if Ones
BM	D2(X2,B2)	BC 4,	D2(X2,B2)	Branch if Mixed
BZ	D2(X2,B2)	BC 8,	D2(X2,B2)	Branch if Zeros
BNO	D2(X2,B2)	BC 14,	D2(X2,B2)	Branch if Not Ones

CNOP ALIGNMENT

Double Word							
Word				Word			
Half Word		Half Word		Half Word		Half Word	
Byte	Byte	Byte	Byte	Byte	Byte	Byte	Byte
0,4		2,4		0,4		2,4	
0,8		2,8		4,8		6,8	

EDIT AND EDIT & MARK SYMBOLS

Mask	Meaning	Mask	Meaning
hex 40	blank	hex 22	field separator character
hex 21	significance start character	hex 20	digit-select character

PERMANENT STORAGE ASSIGNMENT

DEC	ADDRESS HEX	BINARY	LENGTH	PURPOSE
0	0	0000 0000	double-word	Initial program loading PSW
8	8	0000 1000	double-word	Initial program loading CCW1
16	10	0001 0000	double-word	Initial program loading CCW2
24	18	0001 1000	double-word	External old PSW
32	20	0010 0000	double-word	Supervisor call old PSW
40	28	0010 1000	double-word	Program old PSW
48	30	0011 0000	double-word	Machine-check old PSW
56	38	0011 1000	double-word	Input/output old PSW
64	40	0100 0000	double-word	Channel status word
72	48	0100 1000	word	Channel address word
76	4C	0100 1100	word	Unused
80	50	0101 0000	word	Timer (uses bytes 50, 51 & 52)
84	54	0101 0100	word	Unused
88	58	0101 1000	double-word	External new PSW
96	60	0110 0000	double-word	Supervisor call new PSW
104	68	0110 1000	double-word	Program new PSW
112	70	0111 0000	double-word	Machine-check new PSW
120	78	0111 1000	double-word	Input/output new PSW
128	80	1000 0000	(1)	Diagnostic scan-out area

(1) The size of the diagnostic scan-out area depends on the particular model and I/O channels; for models 30 through 75, maximum size is 256 bytes.

CONDITION CODES

Condition Code Setting	0	1	2	3
Mask Bit Position	8	4	2	1

FLOATING-POINT ARITHMETIC

Add Normalized S/L	zero	$<$ zero	$>$ zero	– –
Add Unnormalized S/L	zero	$<$ zero	$>$ zero	– –
Compare S/L (A:B)	equal	A low	A high	– –
Load and Test S/L	zero	$<$ zero	$>$ zero	– –
Load Complement S/L	zero	$<$ zero	$>$ zero	– –
Load Negative S/L	zero	$<$ zero	– –	– –
Load Positive S/L	zero	– –	$>$ zero	– –
Subtract Normalized S/L	zero	$<$ zero	$>$ zero	– –
Subtract Unnormalized S/L	zero	$<$ zero	$>$ zero	– –

FIXED-POINT ARITHMETIC

Add H/F	zero	$<$ zero	$>$ zero	overflow
Add Logical	zero, no carry	not zero, no carry	zero, carry	not zero, carry
Compare H/F (A:B)	equal	A low	A high	– –
Load and Test	zero	$<$ zero	$>$ zero	– –
Load Complement	zero	$<$ zero	$>$ zero	overflow
Load Negative	zero	$<$ zero	– –	– –
Load Positive	zero	– –	$>$ zero	overflow
Shift Left Double	zero	$<$ zero	$>$ zero	overflow
Shift Left Single	zero	$<$ zero	$>$ zero	overflow
Shift Right Double	zero	$<$ zero	$>$ zero	– –
Shift Right Single	zero	$<$ zero	$>$ zero	– –
Subtract H/F	zero	$<$ zero	$>$ zero	overflow
Subtract Logical	– –	not zero, no carry	zero, carry	not zero, carry

DECIMAL ARITHMETIC

Add Decimal	zero	$<$ zero	$>$ zero	overflow
Compare Decimal (A:B)	equal	A low	A high	– –
Subtract Decimal	zero	$<$ zero	$>$ zero	overflow
Zero and Add	zero	$<$ zero	$>$ zero	overflow

LOGICAL OPERATIONS

AND	zero	not zero	– –	– –
Compare Logical (A:B)	equal	A low	A high	– –
Edit	zero	$<$ zero	$>$ zero	– –
Edit and Mark	zero	$<$ zero	$>$ zero	– –
Exclusive OR	zero	not zero	– –	– –
OR	zero	not zero	– –	– –
Test Under Mask	zero	mixed	– –	one
Translate and Test	zero	incomplete	complete	– –

STATUS SWITCHING

Test and Set	zero	one	– –	– –

INPUT/OUTPUT OPERATIONS

Halt I/O	interruption pending	CSW stored	burst op stopped	not oper
Start I/O	successful	CSW stored	busy	not oper
Test I/O	available	CSW stored	busy	not oper
Test Channel	available	interruption pending	burst mode	not oper

PROGRAM STATUS WORD

System Mask*		Key	AMWP*	Interruption Code	
0	7	8 11	12 15	16 23	24 31

ILC	CC	Prog. Mask*	Instruction Address		
32 33	34 35	36 39	40 47	48 55	56 63

0 Multiplexer channel mask
1 Selector channel 1 mask
2 Selector channel 2 mask
3 Selector channel 3 mask
4 Selector channel 4 mask
5 Selector channel 5 mask
6 Selector channel 6 mask
7 External mask
12 USACII mode (A)

13 Machine check mask (M)
14 Wait state (W)
15 Problem state (P)
32-33 Instruction Length code (ILC)
34-35 Condition code (CC)
36 Fixed-point overflow mask
37 Decimal overflow mask
38 Exponent underflow mask
39 Significance mask

* A one-bit equals on, and permits an interrupt.

CODE FOR PROGRAM INTERRUPTION

Interruption Code			Program Interrupt Cause	Interruption Code			Program Interrupt Cause
Dec	Hex	Binary		Dec	Hex	Binary	
1	1	0000 0001	Operation	9	9	0000 1001	Fixed-pt. divide
2	2	0000 0010	Privileged op.	10	A	0000 1010	Dec. overflow
3	3	0000 0011	Execute	11	B	0000 1011	Decimal divide
4	4	0000 0100	Protection	12	C	0000 1100	Exp. overflow
5	5	0000 0101	Addressing	13	D	0000 1101	Exp. underflow
6	6	0000 0110	Specification	14	E	0000 1110	Significance
7	7	0000 0111	Data	15	F	0000 1111	Float.-pt. divide
8	8	0000 1000	Fixed-pt. overflow				

HEXADECIMAL AND DECIMAL CONVERSION

To find the decimal number, locate the hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the hex number, locate the next lower decimal number and its hex equivalent. Each difference is used to obtain the next hex number until the entire number is developed.

BYTE				BYTE				BYTE			
0123		4567		0123		4567		0123		4567	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
6		5		4		3		2		1	

POWERS OF 16						POWERS OF 2			
16^n					n	2^n			n
				1	0			512	9
				16	1		1	024	10
				256	2		2	048	11
			4	096	3		4	096	12
			65	536	4		8	192	13
		1	048	576	5		16	384	14
		16	777	216	6		32	768	15
		268	435	456	7		65	536	16
	4	294	967	296	8		131	072	17
	68	719	476	736	9		262	144	18
1	099	511	627	776	10		524	288	19
17	592	186	044	416	11	1	048	576	20
281	474	976	710	656	12	2	097	152	21
4 503	599	627	370	496	13	4	194	304	22
72 057	594	037	927	936	14	8	388	608	23
1 152 921	504	606	846	976	15	16	777	216	24

RR FORMAT INSTRUCTIONS

Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-Bit Code
0	00			NUL		12-0-1-8-9	0000 0000
1	01			SOH		12-1-9	0000 0001
2	02			STX		12-2-9	0000 0010
3	03			ETX		12-3-9	0000 0011
4	04	SPM		PF		12-4-9	0000 0100
5	05	BALR		HT		12-5-9	0000 0101
6	06	BCTR		LC		12-6-9	0000 0110
7	07	BCR		DEL		12-7-9	0000 0111
8	08	SSK				12-8-9	0000 1000
9	09	ISK				12-1-8-9	0000 1001
10	0A	SVC		SMM		12-2-8-9	0000 1010
11	0B			VT		12-3-8-9	0000 1011
12	0C	(EBCDIC +)		FF		12-4-8-9	0000 1100
13	0D	(EBCDIC -)		CR		12-5-8-9	0000 1101
14	0E			SO		12-6-8-9	0000 1110
15	0F			SI		12-7-8-9	0000 1111
16	10	LPR		DLE		12-11-1-8-9	0001 0000
17	11	LNR		DC1		11-1-9	0001 0001
18	12	LTR		DC2		11-2-9	0001 0010
19	13	LCR		TM		11-3-9	0001 0011
20	14	NR		RES		11-4-9	0001 0100
21	15	CLR		NL		11-5-9	0001 0101
22	16	OR		BS		11-6-9	0001 0110
23	17	XR		IL		11-7-9	0001 0111
24	18	LR		CAN		11-8-9	0001 1000
25	19	CR		EM		11-1-8-9	0001 1001
26	1A	AR		CC		11-2-8-9	0001 1010
27	1B	SR		CU1		11-3-8-9	0001 1011
28	1C	MR		IFS		11-4-8-9	0001 1100
29	1D	DR		IGS		11-5-8-9	0001 1101
30	1E	ALR		IRS		11-6-8-9	0001 1110
31	1F	SLR		IUS		11-7-8-9	0001 1111
32	20	LPDR		DS		11-0-1-8-9	0010 0000
33	21	LNDR		SOS		0-1-9	0010 0001
34	22	LTDR		FS		0-2-9	0010 0010
35	23	LCDR				0-3-9	0010 0011
36	24	HDR		BYP		0-4-9	0010 0100
37	25	LRDR		LF		0-5-9	0010 0101
38	26	MXR		ETB		0-6-9	0010 0110
39	27	MXDR		ESC		0-7-9	0010 0111
40	28	LDR				0-8-9	0010 1000
41	29	CDR				0-1-8-9	0010 1001
42	2A	ADR		SM		0-2-8-9	0010 1010
43	2B	SDR		CU2		0-3-8-9	0010 1011
44	2C	MDR				0-4-8-9	0010 1100
45	2D	DDR		ENQ		0-5-8-9	0010 1101
46	2E	AWR		ACK		0-6-8-9	0010 1110
47	2F	SWR		BEL		0-7-8-9	0010 1111
48	30	LPER				12-11-0-1-8-9	0011 0000
49	31	LNER				1-9	0011 0001
50	32	LTER		SYN		2-9	0011 0010
51	33	LCER				3-9	0011 0011
52	34	HER		PN		4-9	0011 0100
53	35	LRER		RS		5-9	0011 0101
54	36	AXR		UC		6-9	0011 0110
55	37	SXR		EOT		7-9	0011 0111
56	38	LER				8-9	0011 1000
57	39	CER				1-8-9	0011 1001
58	3A	AER				2-8-9	0011 1010
59	3B	SER		CU3		3-8-9	0011 1011
60	3C	MER		DC4		4-8-9	0011 1100
61	3D	DER		NAK		5-8-9	0011 1101
62	3E	AUR				6-8-9	0011 1110
63	3F	SUR		SUB		7-8-9	0011 1111

(2) Add C (check bit) for odd or even parity as needed, except for even parity, decimal 64 is CA, the same as decimal 122.

(3) Decimal Feature instructions. (4) System/360 assembler programs require these codes.

RR FORMAT

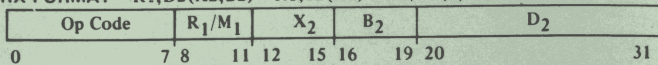| Op Code	R₁/M₁	R₂
0 7	8 11	12 15

R1, R2 – meaningful for all RR instructions except SPM, SVC

BASE AND INDEX REGISTERS

/////	Base Address or Index
0 7	8 31

Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-Bit Code	(4)
64	40	STH		SP	(2)	no punches	0100 0000	
65	41	LA				12-0-1-9	0100 0001	
66	42	STC				12-0-2-9	0100 0010	
67	43	IC				12-0-3-9	0100 0011	
68	44	EX				12-0-4-9	0100 0100	
69	45	BAL				12-0-5-9	0100 0101	
70	46	BCT				12-0-6-9	0100 0110	
71	47	BC				12-0-7-9	0100 0111	
72	48	LH				12-0-8-9	0100 1000	
73	49	CH				12-1-8	0100 1001	
74	4A	AH	.	¢	B A 8 2 1	12-2-8	0100 1010	
75	4B	SH	.	.	B A 8 4	12-3-8	0100 1011	
76	4C	MH	¤)	<	B A 8 4	12-4-8	0100 1100	
77	4D		[	(	B A 8 4 1	12-5-8	0100 1101	(
78	4E	CVD	<	+	B A 8 4 2	12-6-8	0100 1110	+
79	4F	CVB	‡	!	B A 8 4 2 1	12-7-8	0100 1111	
80	50	ST	& +	&	B A	12	0101 0000	
81	51					12-11-1-9	0101 0001	
82	52					12-11-2-9	0101 0010	
83	53					12-11-3-9	0101 0011	
84	54	N				12-11-4-9	0101 0100	
85	55	CL				12-11-5-9	0101 0101	
86	56	O				12-11-6-9	0101 0110	
87	57	X				12-11-7-9	0101 0111	
88	58	L				12-11-8-9	0101 1000	
89	59	C				11-1-8	0101 1001	
90	5A	A		!		11-2-8	0101 1010	
91	5B	S	$	$	B 8 2 1	11-3-8	0101 1011	
92	5C	M	*	*	B 8 4	11-4-8	0101 1100	
93	5D	D	]	)	B 8 4 1	11-5-8	0101 1101	)
94	5E	AL	;	¬	B 8 4 2	11-6-8	0101 1110	
95	5F	SL	Δ	¬	B 8 4 2 1	11-7-8	0101 1111	
96	60	STD	–	–	B	11	0110 0000	
97	61		/	/	A 1	0-1	0110 0001	
98	62					11-0-2-9	0110 0010	
99	63					11-0-3-9	0110 0011	
100	64					11-0-4-9	0110 0100	
101	65					11-0-5-9	0110 0101	
102	66					11-0-6-9	0110 0110	
103	67	MXD				11-0-7-9	0110 0111	
104	68	LD				11-0-8-9	0110 1000	
105	69	CD				0-1-8	0110 1001	
106	6A	AD				12-11	0110 1010	
107	6B	SD	.	.	A 8 2 1	0-3-8	0110 1011	
108	6C	MD	% (	%	A 8 4	0-4-8	0110 1100	
109	6D	DD	Y	_	A 8 4 1	0-5-8	0110 1101	
110	6E	AW	\	>	A 8 4 2	0-6-8	0110 1110	
111	6F	SW	⧣	?	A 8 4 2 1	0-7-8	0110 1111	
112	70	STE				12-11-0	0111 0000	
113	71					12-11-0-1-9	0111 0001	
114	72					12-11-0-2-9	0111 0010	
115	73					12-11-0-3-9	0111 0011	
116	74					12-11-0-4-9	0111 0100	
117	75					12-11-0-5-9	0111 0101	
118	76					12-11-0-6-9	0111 0110	
119	77					12-11-0-7-9	0111 0111	
120	78	LE				12-11-0-8-9	0111 1000	
121	79	CE				1-8	0111 1001	
122	7A	AE	♭	:	A	2-8	0111 1010	
123	7B	SE	# =	#	8 2 1	3-8	0111 1011	
124	7C	ME	@	@	8 4	4-8	0111 1100	'
125	7D	DE	:	'	8 4 1	5-8	0111 1101	
126	7E	AU	>	=	8 4 2	6-8	0111 1110	=
127	7F	SU	√	"	8 4 2 1	7-8	0111 1111	

RX FORMAT   R1,D2(X2,B2)   R1,S2(X2)   R1,D2(0,B2)   R1,S2

Op Code	R₁/M₁	X₂	B₂	D₂

0	7 8 11	12 15	16 19	20 31

SHORT FLOATING POINT NUMBER

S	Characteristic	Fraction
0 1	7 8	31
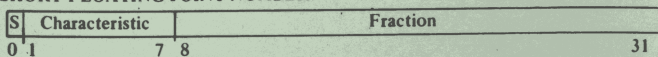
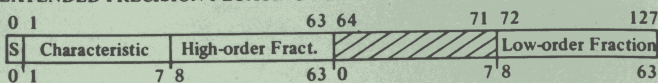**LONG FLOATING POINT NUMBER** – same as short floating point number except fraction is longer -- bits 8 through 63
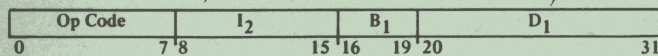
EXTENDED PRECISION FLOATING POINT NUMBER

0 1		63 64	71 72	127
S	Characteristic	High-order Fract.	/////////	Low-order Fraction
0 1	7 8	63 0	7 8	63

Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-Bit Code
128	80	SSM				12-0-1-8	1000 0000
129	81			a		12-0-1	1000 0001
130	82	LPSW		b		12-0-2	1000 0010
131	83	(Diagnose)		c		12-0-3	1000 0011
132	84	WRD		d		12-0-4	1000 0100
133	85	RDD		e		12-0-5	1000 0101
134	86	BXH		f		12-0-6	1000 0110
135	87	BXLE		g		12-0-7	1000 0111
136	88	SRL		h		12-0-8	1000 1000
137	89	SLL		i		12-0-9	1000 1001
138	8A	SRA				12-0-2-8	1000 1010
139	8B	SLA				12-0-3-8	1000 1011
140	8C	SRDL				12-0-4-8	1000 1100
141	8D	SLDL				12-0-5-8	1000 1101
142	8E	SRDA				12-0-6-8	1000 1110
143	8F	SLDA				12-0-7-8	1000 1111
144	90	STM				12-11-1-8	1001 0000
145	91	TM		j		12-11-1	1001 0001
146	92	MVI		k		12-11-2	1001 0010
147	93	TS		l		12-11-3	1001 0011
148	94	NI		m		12-11-4	1001 0100
149	95	CLI		n		12-11-5	1001 0101
150	96	OI		o		12-11-6	1001 0110
151	97	XI		p		12-11-7	1001 0111
152	98	LM		q		12-11-8	1001 1000
153	99			r		12-11-9	1001 1001
154	9A					12-11-2-8	1001 1010
155	9B					12-11-3-8	1001 1011
156	9C	SIO				12-11-4-8	1001 1100
157	9D	TIO				12-11-5-8	1001 1101
158	9E	HIO				12-11-6-8	1001 1110
159	9F	TCH				12-11-7-8	1001 1111
160	A0					11-0-1-8	1010 0000
161	A1					11-0-1	1010 0001
162	A2			s		11-0-2	1010 0010
163	A3			t		11-0-3	1010 0011
164	A4			u		11-0-4	1010 0100
165	A5			v		11-0-5	1010 0101
166	A6			w		11-0-6	1010 0110
167	A7			x		11-0-7	1010 0111
168	A8			y		11-0-8	1010 1000
169	A9			z		11-0-9	1010 1001
170	AA					11-0-2-8	1010 1010
171	AB					11-0-3-8	1010 1011
172	AC					11-0-4-8	1010 1100
173	AD					11-0-5-8	1010 1101
174	AE					11-0-6-8	1010 1110
175	AF					11-0-7-8	1010 1111
176	B0					12-11-0-1-8	1011 0000
177	B1					12-11-0-1	1011 0001
178	B2					12-11-0-2	1011 0010
179	B3					12-11-0-3	1011 0011
180	B4					12-11-0-4	1011 0100
181	B5					12-11-0-5	1011 0101
182	B6					12-11-0-6	1011 0110
183	B7					12-11-0-7	1011 0111
184	B8					12-11-0-8	1011 1000
185	B9					12-11-0-9	1011 1001
186	BA					12-11-0-2-8	1011 1010
187	BB					12-11-0-3-8	1011 1011
188	BC					12-11-0-4-8	1011 1100
189	BD					12-11-0-5-8	1011 1101
190	BE					12-11-0-6-8	1011 1110
191	BF					12-11-0-7-8	1011 1111

RS FORMAT

R1,R3,D2(B2) } BXH, BXLE
R1,R3,S2 } LM, STM

R1,D2(B2) } Shift
R1,S2 } instructions

Op Code	R₁	R₃	B₂	D₂
0	7 8 11	12 15	16 19	20 31
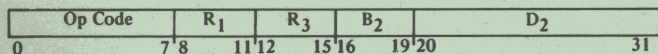
SI FORMAT

D1(B1) } LPSW, SSM, HIO, SIO
S1 } TIO, TCH, TS

D1(B1),I2 } All other SI
S1,I2 } instructions

Op Code	I₂	B₁	D₁
0	7 8 15	16 19	20 31

Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-Bit Code
192	C0		?		B A 8 2	12-0	1100 0000
193	C1		A	A	B A 1	12-1	1100 0001
194	C2		B	B	B A 2	12-2	1100 0010
195	C3		C	C	B A 2 1	12-3	1100 0011
196	C4		D	D	B A 4	12-4	1100 0100
197	C5		E	E	B A 4 1	12-5	1100 0101
198	C6		F	F	B A 4 2	12-6	1100 0110
199	C7		G	G	B A 4 2 1	12-7	1100 0111
200	C8		H	H	B A 8	12-8	1100 1000
201	C9		I	I	B A 8 1	12-9	1100 1001
202	CA					12-0-2-8-9	1100 1010
203	CB					12-0-3-8-9	1100 1011
204	CC					12-0-4-8-9	1100 1100
205	CD					12-0-5-8-9	1100 1101
206	CE					12-0-6-8-9	1100 1110
207	CF					12-0-7-8-9	1100 1111
208	D0		!		B 8 2	11-0	1101 0000
209	D1	MVN	J	J	B 1	11-1	1101 0001
210	D2	MVC	K	K	B 2	11-2	1101 0010
211	D3	MVZ	L	L	B 2 1	11-3	1101 0011
212	D4	NC	M	M	B 4	11-4	1101 0100
213	D5	CLC	N	N	B 4 1	11-5	1101 0101
214	D6	OC	O	O	B 4 2	11-6	1101 0110
215	D7	XC	P	P	B 4 2 1	11-7	1101 0111
216	D8		Q	Q	B 8	11-8	1101 1000
217	D9		R	R	B 8 1	11-9	1101 1001
218	DA					12-11-2-8-9	1101 1010
219	DB					12-11-3-8-9	1101 1011
220	DC	TR				12-11-4-8-9	1101 1100
221	DD	TRT				12-11-5-8-9	1101 1101
222	DE	ED (3)				12-11-6-8-9	1101 1110
223	DF	EDMK (3)				12-11-7-8-9	1101 1111
224	E0		‡		A 8 2	0-2-8	1110 0000
225	E1					11-0-1-9	1110 0001
226	E2		S	S	A 2	0-2	1110 0010
227	E3		T	T	A 2 1	0-3	1110 0011
228	E4		U	U	A 4	0-4	1110 0100
229	E5		V	V	A 4 1	0-5	1110 0101
230	E6		W	W	A 4 2	0-6	1110 0110
231	E7		X	X	A 4 2 1	0-7	1110 0111
232	E8		Y	Y	A 8	0-8	1110 1000
233	E9		Z	Z	A 8 1	0-9	1110 1001
234	EA					11-0-2-8-9	1110 1010
235	EB					11-0-3-8-9	1110 1011
236	EC					11-0-4-8-9	1110 1100
237	ED					11-0-5-8-9	1110 1101
238	EE					11-0-6-8-9	1110 1110
239	EF					11-0-7-8-9	1110 1111
240	F0	MVO	0	0	8 2	0	1111 0000
241	F1		1	1	1	1	1111 0001
242	F2	PACK	2	2	2	2	1111 0010
243	F3	UNPK	3	3	2 1	3	1!11 0011
244	F4		4	4	4	4	1111 0100
245	F5		5	5	4 1	5	1111 0101
246	F6		6	6	4 2	6	1111 0110
247	F7		7	7	4 2 1	7	1111 0111
248	F8	ZAP (3)	8	8	8	8	1111 1000
249	F9	CP (3)	9	9	8 1	9	1111 1001
250	FA	AP (3)				12-11-0-2-8-9	1111 1010
251	FB	SP (3)				12-11-0-3-8-9	1111 1011
252	FC	MP (3)				12-11-0-4-8-9	1111 1100
253	FD	DP (3)				12-11-0-5-8-9	1111 1101
254	FE					12-11-0-6-8-9	1111 1110
255	FF					12-11-0-7-8-9	1111 1111

SS FORMAT

Op Code	L₁	L₂	B₁	D₁	B₂	D₂

$$0 \quad\quad 7\ 8 \quad 11\ 12 \quad 15\ 16 \quad 19\ 20 \quad 31\ 32 \quad 35\ 36 \quad 47$$

D1(L,B1),D2(B2) } NC, OC, XC, CLC | D1(L1,B1),D2(L2,B2) } PACK, UNPK
S1(L),S2 } MVC, MVN, MVZ | S1(L1),S2(L2) } MVO, AP, CP
TR, TRT, ED, EDMK | DP, MP, SP, ZAP

PACKED DECIMAL NUMBER | digit | digit | ---- | digit | digit | digit | sign |

ZONED DECIMAL NUMBER | zone | digit | ---- | zone | digit | sign | digit |
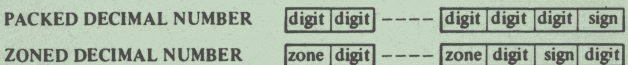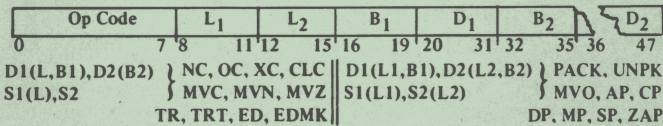
CHANNEL ADDRESS WORD

Key	0000	Command Address
0 3	4 7	8 15 16 23 24 31

CHANNEL COMMAND WORD

Command Code	Data Address
0 7	8 15 16 23 24 31

Flags	0000	/////////	Byte Count
32 36	37 39	40 47	48 55 56 63

CD	Bit 32 (80) causes use of address portion of next CCW
CC	Bit 33 (40) causes use of command code and data address of next CCW
SLI	Bit 34 (20) causes suppression of possible incorrect length indication
SKIP	Bit 35 (10) suppresses transfer of information to main storage
PCI	Bit 36 (08) causes an interruption as Program Control Interrupt

CHANNEL STATUS WORD

Key	0000	Command Address
0 3	4 7	8 15 16 23 24 31

Status	Byte Count
32 39 40 47	48 55 56 63

32 (8000) Attention	40 (0080) Program-control interrupt
33 (4000) Status modifier	41 (0040) Incorrect length
34 (2000) Control unit end	42 (0020) Program check
35 (1000) Busy	43 (0010) Protection check
36 (0800) Channel end	44 (0008) Channel data check
37 (0400) Device end	45 (0004) Channel control check
38 (0200) Unit check	46 (0002) Interface control check
39 (0100) Unit exception	47 (0001) Chaining check

Byte Count: bits 48−63 form the residual count for the last CCW used.

DASD CHANNEL COMMAND CODES (see A26-5988 and A26-3599)

Command for CCW		Count	(M-T)Off Hex	Dec	(M-T)On Hex	Dec
Control	No Op	(not zero)	03	03		
	Seek	6	07	07		
	Seek Cylinder	6	0B	11		
	Seek Head	6	1B	27		
	Set File Mask	1	1F	31		
	Space Count	(not zero)	0F	15		
	Transfer in Channel	X	X8			
	Recalibrate (Note 1)	(not zero)	13	19		
	Restore (2321 only)	X	17	23		
Sense Switching	Sense I/O	6	04	04		
	Release Device ⎫ (Note 2)	(not zero)	94	148		
	Reserve Device ⎭	(not zero)	B4	180		
Search†	Home Address EQ	4 (usually)	39	57	B9	185
	Identifier EQ	5 (usually)	31	49	B1	177
	Identifier HI	5 (usually)	51	81	D1	209
	Identifier EQ or HI	5 (usually)	71	131	F1	241
	Key EQ	1 to 255	29	41	A9	169
	Key HI	1 to 255	49	73	C9	201
	Key EQ or HI	1 to 255	69	105	E9	233
	Key & Data EQ		2D	45	AD	173
	Key & Data HI		4D	77	CD	205
Continue Scan	Key & Data EQ or HI		6D	109	ED	237
	Search EQ		25	37	A5	165
	Search HI	(Note 3)	45	69	C5	197
	Search HI or EQ		65	101	E5	229
	Set Status Modifier*		35	53	B5	181
	Set Status Modifier*		75	117	F5	245
Read†	No Status Modifier		55	85	D5	213
	Home Address	5	1A	26	9A	154
	Count	8	12	18	92	146
	Record R0		16	22	96	150
	Data	Number of bytes transferred	06	06	86	134
	Key & Data		0E	14	8E	142
	Count, Key & Data		1E	30	9E	158
	IPL		02	02		
Write	Home Address	5 (usually)	19	25		
	Record R0	8+KL+DL of R0	15	21		
	Count, Key & Data	8+KL+DL	1D	29		
	Special Count, Key & Data	8+KL+DL	01	01		
	Data	DL	05	05		
	Key & Data	KL+DL	0D	13		

*Sense byte determines which command is used.   X=not significant
†M-T On = M-T Off except during Search and Read, bit 0=1 in M-T On.
Note 1. For 2311 or 2314 only.   Note 2. Two channel switch required except for a 2314/2844 combination.   Note 3. Include mask bytes in search argument; these commands are a special feature on 2841.

CHANNEL COMMAND CODES

Device	Command for CCW		0	1	2	3	4	5	6	7	Hex	Dec
						8-Bit Code							
1052	Read Inquiry BCD		0	0	0	0	1	0	1	0	0A	10
	Read Reader 2 BCD		0	0	0	0	0	0	1	0	02	02
	Write BDC, Auto Carriage Return		0	0	0	0	1	0	0	1	09	09
	Write BDC, No Auto Carriage Return		0	0	0	0	0	0	0	1	01	01
	No Op		0	0	0	0	0	0	1	1	03	03
	Sense		0	0	0	0	0	1	0	0	04	04
	Alarm		0	0	0	0	1	0	1	1	0B	11
2540	Read, Feed, Select Stacker SS	Type AA	S	S	D	0	0	0	1	0		
	Read	Type AB	1	1	D	0	0	0	1	0		
	Read, Feed (1400 compatability mode only)		1	1	D	1	0	0	1	0		
	Feed, Select Stacker SS	Type BA	S	S	1	0	0	0	1	1		
	PFR Punch, Feed, Select Stacker SS	Type BA	S	S	D	1	0	0	0	1		
	Punch, Feed, Select Stacker SS	Type BB	S	S	D	0	0	0	0	1		

SS	Stacker		D	Data Mode
00	R1		0	EBCDIC
01	R2		1	Column Binary
10	RP3			

1442 N1

Command	M	M	M	M	Note		0	1	2	3	4	5	6	7
Read	M	M	M		Read		M	M	M	0	0	0	1	0
Read	0	0	X	Eject and SS1	Write		M	M	M	0	0	0	0	1
Read	1	0	X	Eject and SS1	Control		M	M	M	0	0	0	1	1
Read	0	1	X	Eject and SS2	No Op		0	0	0	0	0	0	1	1
Read	1	1	X	Eject and SS2	Sense		0	0	M	M	0	1	0	0
Write	0	0	X	SS1										
Write	1	0	X	Eject and SS1										
Write	0	1	X	SS2	X = 0 means EBCDIC mode									
Write	1	1	X	Eject and SS2	X = 1 means Column Binary Mode									
Control	1	0		Eject and SS1										
Control	0	1		SS2										
Control	1	1		Eject and SS2										
Sense			1	1	Punch diagnostic									
Sense			0	1	Read diagnostic									

Device	Command for CCW		0	1	2	3	4	5	6	7	Hex	Dec
1403 or 1443	Write, No Space		0	0	0	0	0	0	0	1	01	01
	Write, Space 1 After Print		0	0	0	0	1	0	0	1	09	09
	Write, Space 2 After Print		0	0	0	1	0	0	0	1	11	17
	Write, Space 3 After Print		0	0	0	1	1	0	0	1	19	25
	Write, Skip To Channel N After Print		1	C	H	A	N	0	0	1		
	Diagnostic Read (1403)		0	0	0	0	0	0	1	0	02	02
	Diagnostic Read (1443)		0	0	0	0	0	1	1	0	06	06
	Sense		0	0	0	0	0	1	0	0	04	04
Carriage Control	Space 1 Line Immediately		0	0	0	0	1	0	1	1	0B	11
	Space 2 Line Immediately		0	0	0	1	0	0	1	1	13	19
	Space 3 Line Immediately		0	0	0	1	1	0	1	1	1B	27
	Skip To Channel N Immediately		1	C	H	A	N	0	1	1		
	No Op		0	0	0	0	0	0	1	1	03	03

C	H	A	N	Channel		C	H	A	N	Channel
0	0	0	1	1		0	1	1	1	7
0	0	1	0	2		1	0	0	0	8
0	0	1	1	3		1	0	0	1	9
0	1	0	0	4		1	0	1	0	10
0	1	0	1	5		1	0	1	1	11
0	1	1	0	6		1	1	0	0	12

Device	Command for CCW		0	1	2	3	4	5	6	7	Hex	Dec
UCS	Allow buffer loading		1	1	1	0	1	0	1	1	EB	235
	Load buffer (no folding)		1	1	1	1	1	0	1	1	FB	251
	Load buffer (folding)		1	1	1	1	0	0	1	1	F3	243
	Block data check latch		0	1	1	1	0	0	1	1	73	121
	Reset block data check latch		0	1	1	1	1	0	1	1	7B	129
2400 Tape*	Read Backward (Overrides Data Converter On)		0	0	0	0	1	1	0	0	0C	12
	Sense		0	0	0	0	0	1	0	0	04	04
	Write	N N N	0	0	0	0	0	0	0	1	01	01
		0 0 0	1600 bpi P.E. **									
	Read	N N N	0	0	0	0	0	0	1	0	02	02
		0 0 1	800 bpi NRZI									
	Control		0	0	C	C	C	1	1	1		
			D	D	M	M	M	0	1	1		
			1	1	N	N	N	0	1	1		

	C	C	C	Control Codes	Hex	Dec
	0	0	0	REW	7	7
	0	0	1	RUN	0F	15
	0	1	0	ERG	17	23
	0	1	1	WTM	1F	31
	1	0	0	BSR	27	39
	1	0	1	BSF	2F	47
	1	1	0	FSR	37	55
	1	1	1	FSF	3F	63

D	D	7 Track Density
0	0	200
0	1	556
1	0	800**
1	1	***

M	M	M	(Mode Modifiers)	Set Density	Set Odd Parity	Set Even Parity	Data Converter On	Data Converter Off	Translator On	Translator Off	Request TIE (Track in Error)
0	0	0	No Op	—	—	—	—	—	—	—	—
0	0	1	Not Used	—	—	—	—	—	—	—	—
0	1	0	Reset Condition	X	X		X			X	
0	1	1	Nine-track only								X
1	0	0		X		X		X		X	
1	0	1		X		X		X	X		
1	1	0	Reset Condition	X	X		X			X	
1	1	1		X	X				X	X	

7 Track

*9 track op. forces 800 BPI and odd parity; also, it overrides 7 track but does not reset 7 track. Load/Sys Reset forces 7 track to 800 BPI, odd parity, data converter on, translator off.

** Reset condition

*** Set 9 Track mode, Models 4-6